Winbond Electronics Corp.

UART WITH FIFO AND PRINTER PORT CONTROLLER

GENERAL DESCRIPTION

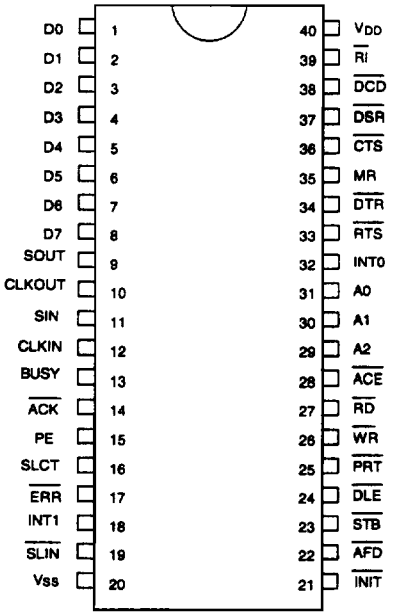
The W86C551 is an enhanced version of the existing W86C451. The device supports one 16550 compatible UART and one Centronics parallel interface.

FEATURES

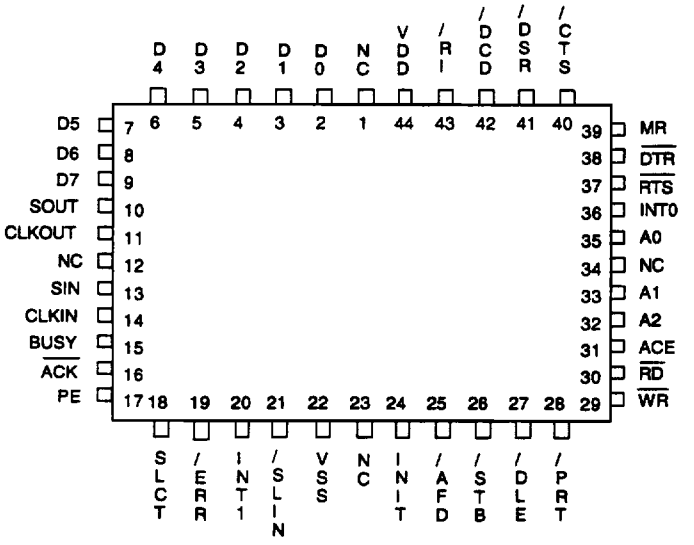
- Easily interfaces with most popular microprocessors
- Pin compatible and functionally compatible with the existing W86C451
- Centronics parallel interface
- Capable of running all existing 16450 and 16550 software
- Uses system's 14.31818MHz clock input
- In FIFO mode transmitter and receiver are each buffered with 16-byte FIFOs to reduce number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1.5, or 2-stop bit generation
  - Baud generation
- False start bit detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls
- 40-pin PDIP package for W86C551 and 44-pin PLCC package for W86C551P

PIN CONFIGURATION

40-pin PDIP



44-pin PLCC



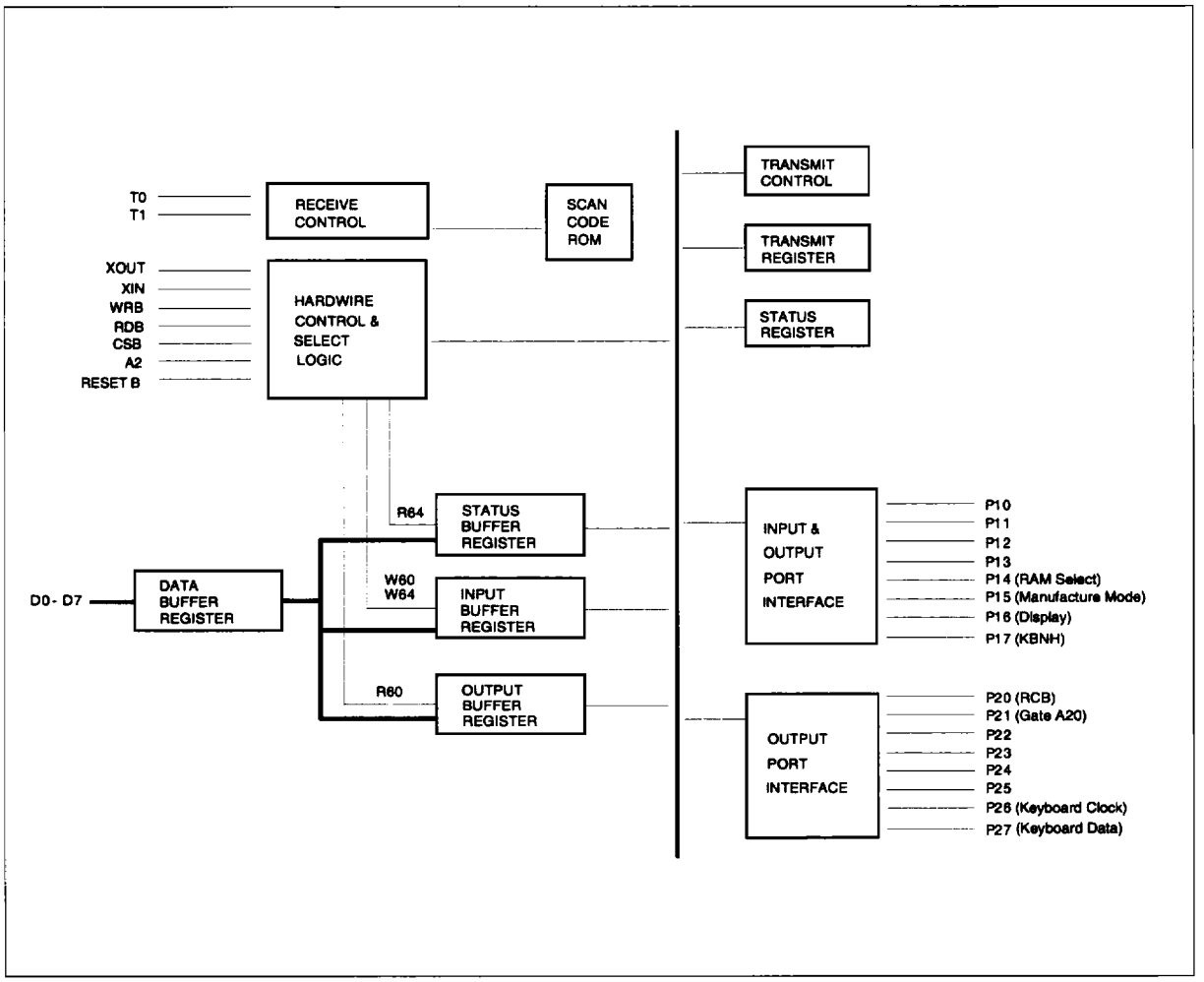
PIN DESCRIPTION

PIN # (40PDIP)	PIN # (44PLCC)	I/O	NAME	FUNCTION
1	2	I	T0	K/B Clock Input
2	3	I	XIN	Crystal Clock I/P
3	4	O	XOUT	Crystal Clock O/P
4	5	I	RESETB	Chip Reset
5	6	-	VCC	Optional +5V Power Supply
6	7	I	CSB	Chip Select
7	8	-	GND	Optional Ground Power
8	9	I	RDB	I/O Read
9	10	I	A2	Connect to Address A2
10	11	I	WRB	I/O Write
11, 26	1, 12, 13, 23, 29, 34	-	NC	Reserved
12, 13, 14, 15, 16, 17, 18, 19	14, 15, 16, 17, 18, 19, 20, 21	I/O	D0-D7	Data Bus D0 - D7
20	22	-	GND	Ground Power Supply
21	24	O	P20	Bit 0 of Port 2 (RCB: System Reset)
22	25	O	P21	Bit 1 of Port 2 (GA20: GATE A20)
23	26	I/O	P22	Bit 2 of Port 2
24	27	I/O	P23	Bit 3 of Port 2
25	28	-	VCC	Optional +5V Power Supply
27	30	I/O	P10	Bit 0 of Port 1
28	31	I/O	P11	Bit 1 of Port 1
29	32	I/O	P12	Bit 2 of Port 1
30	33	I/O	P13	Bit 3 of Port 1
31	35	I	P14	Bit 4 of Port 1 (RAM Jumper Select)
32	36	I	P15	Bit 5 of Port 1 (JUMP)
33	37	I	P16	Bit 6 of Port 1 (Display Select)
34	38	I	P17	Bit 7 of Port 1 (K/B Inhibit Switch)

Pin description, continued

35	39	O	P24	Bit 4 of Port 2 (OBF O/P Interrupt)
36	40	O	P25	Bit 5 of Port 2 (I/P Buffer Empty)
37	41	O	P26	Bit 6 of Port 2 (K/B Clock O/P)
38	42	O	P27	Bit 7 of Port 2 (K/B Data O/P)
39	43	I	T1	K/B Data Input
40	44	-	Vcc	+5V Power Supply

BLOCK DIAGRAM



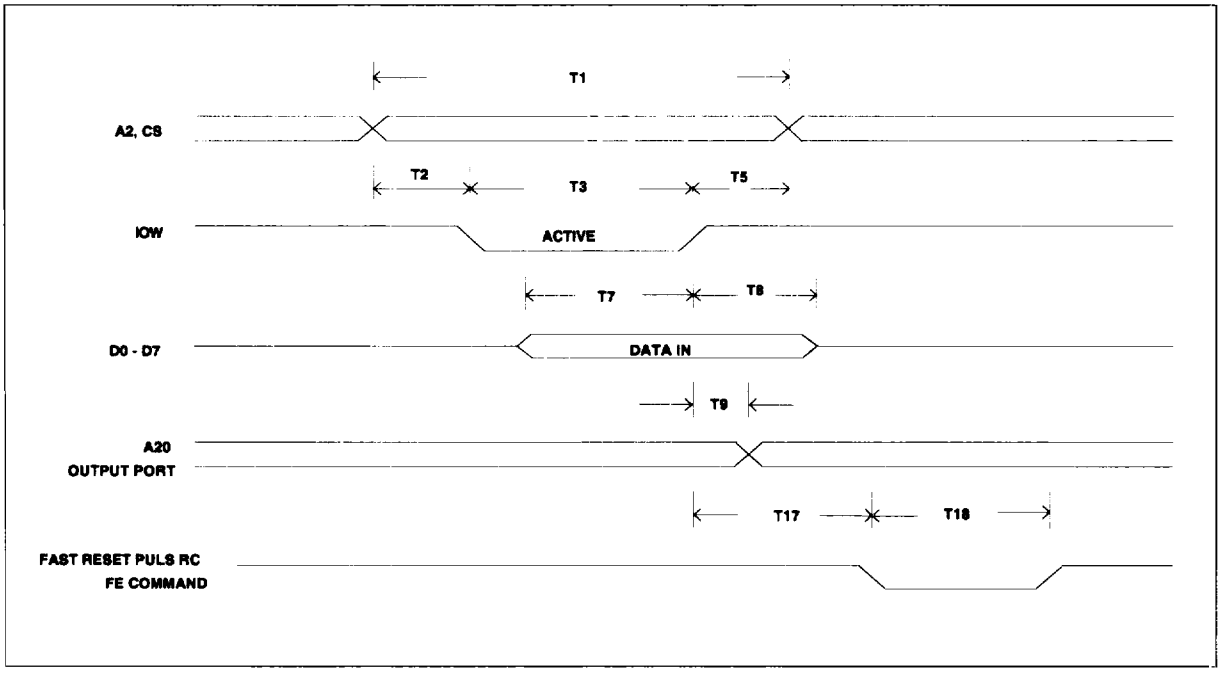
AC TIMING

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS

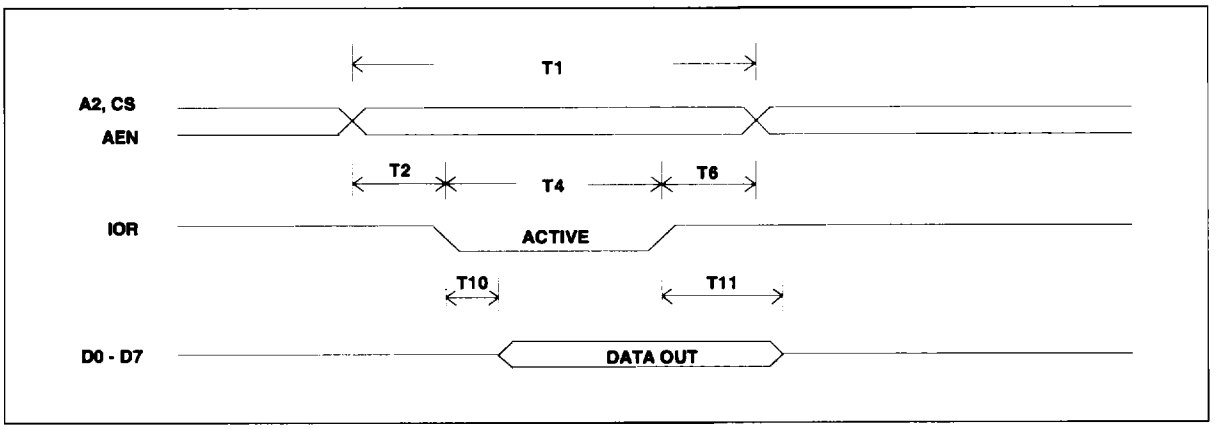
AC timing, continued

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10		nS
T10	RDB to Drive Data Delay		20	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T17	RC Fast Reset Pulse Delay (8 MHz)	2	3	µS
T18	RC Pulse Width (8 MHz)	6		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	XIN/XOUT Period (6-12 MHz)	83	167	nS

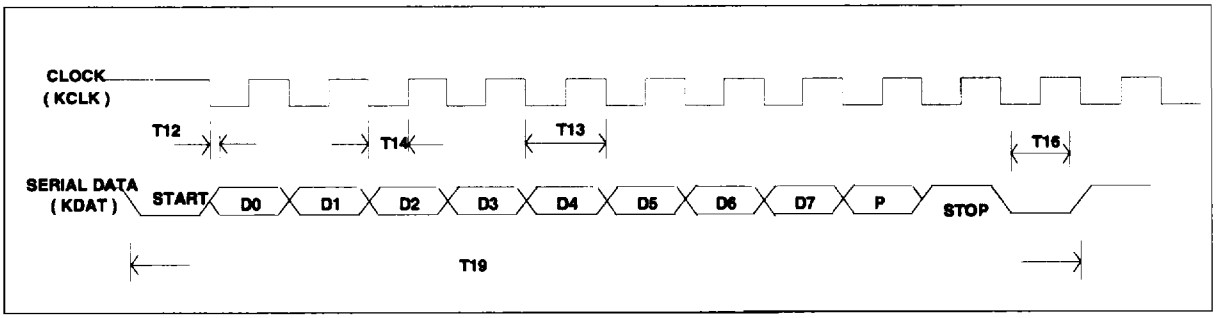
WRITE CYCLE TIMING



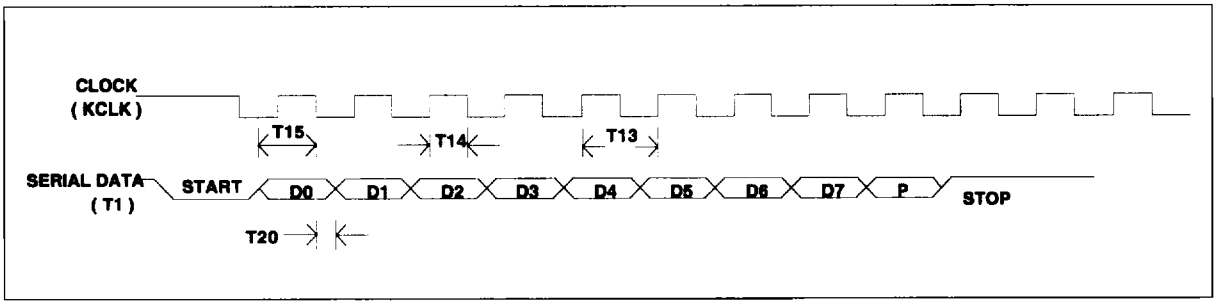
READ CYCLE TIMING



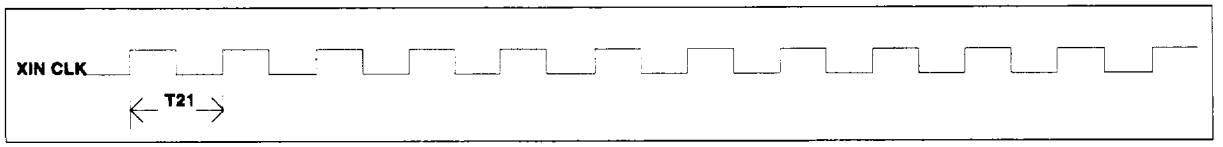
SEND DATA TO K/B



RECEIVE DATA FROM K/B



XIN/XOUT CLOCK



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Operating Temperature	-0 to +85	°C
Storage Temperature	-65 to +150	°C
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	50	mW

ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta= 0° C to +70° C, V_{DD}= +5V ±5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply	4.75	5.0	5.25	V
T_A	Operating Temperature	0	25	70	V
V_{IH}	High Level Voltage for TTL Min. I/P	2.0		V_{DD}	V
V_{IL}	Low Level Voltage for TTL Max. I/P	-0.3		0.8	V
V_{OH}	High Level Voltage for TTL Min. O/P	V_{DD}-0.5			V
V_{OL}	Low Level Voltage for TTL Max. O/P			0.5	V
R_{IP}	Min. I/P Resist	10K			Ω
I_{LI}	I/P Leakage Current	-10		10	µA
I_{LO}	O/P Leakage Current	-10		10	µA
I_{OL}	O/P Sink Current	4			mA
C_L	O/P Load Capacity	15		50	pF

STATUS REGISTER

The status register is an 8-bit read-only register at I/O address hex 64 that holds information about the state of the keyboard controller and interface. It may be read at any time.

BIT	BIT DESCRIPTION	FUNCTION
0	Output Buffer Full	0: Output Buffer Empty 1: Output Buffer Full

Status register, continued

BIT	BIT DESCRIPTION	FUNCTION
1	Input Buffer Full	0: Input Buffer Empty 1: Input Buffer Full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It is set to 0 after a power-on reset
3	Command/data	0: Data Byte 1: Command Byte
4	Inhibit Switch	0: Keyboard is Inhibited 1: Keyboard is Not Inhibited
5	Transmit Time Out	0: No Transmit Time Out Error 1: Transmit Time Out Error
6	Receive Time Out	0: No Receive Time Out Error 1: Receive Time Out Error
7	Parity Error	0: Odd Parity (No Error) 1: Even Parity (Error)

OUTPUT BUFFER

The output buffer is an 8-bit read-only register at I/O address hex 60. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by command to the system. The output buffer should be read only when the output buffer full bit in the register is 1.

INPUT BUFFER

The input buffer is an 8-bit write-only register at I/O address hex 60 or 64. Writing to address hex 60 sets a flag that indicates a data write; writing to address hex 64 sets a flag that indicates a command write. Data written to I/O address hex 60 is sent to the keyboard (unless the keyboard controller is expecting a data byte) following the controller's input buffer only if the input buffer full bit in the status register is set to 0.

I/O PORTS

The keyboard controller has two 8-bit I/O ports and two test inputs. One of the ports is assigned for input and the other for output. The controller uses the test inputs to read the state of the keyboard's clock line and data line.

The following figures show bit definitions for the input, output, and test-input ports.

(A) Input Port Defintions

BIT	FUNCTION
0	Undefined
1	Undefined
2	Undefined
3	Undefined
4	RAM on The System Board 0: Disable 2nd 256 KB of System Board RAM 1: Enable 2nd 256 KB of System Board RAM
5	Manufacturing Jumper Installed 0: Manufacturing Jumper 1: Jumper Not Installed
6	Display Type Switch 0: Primary Display Attached to Color/graphics 0: Primary Display Attached to Monochrome
7	Keyboard Inhibit Switch 0: Keyboard Inhibited 1: Keyboard Not Inhibited

(B) Output Port Defintions

BIT	FUNCTION
0	System Reset
1	Gate A20
2	Undefined
3	Undefined
4	Output Buffer Full
5	Input Buffer Empty
6	Keyboard Clock (Output)
7	Keyboard Data (Output)

(C) Test-Input Defintions

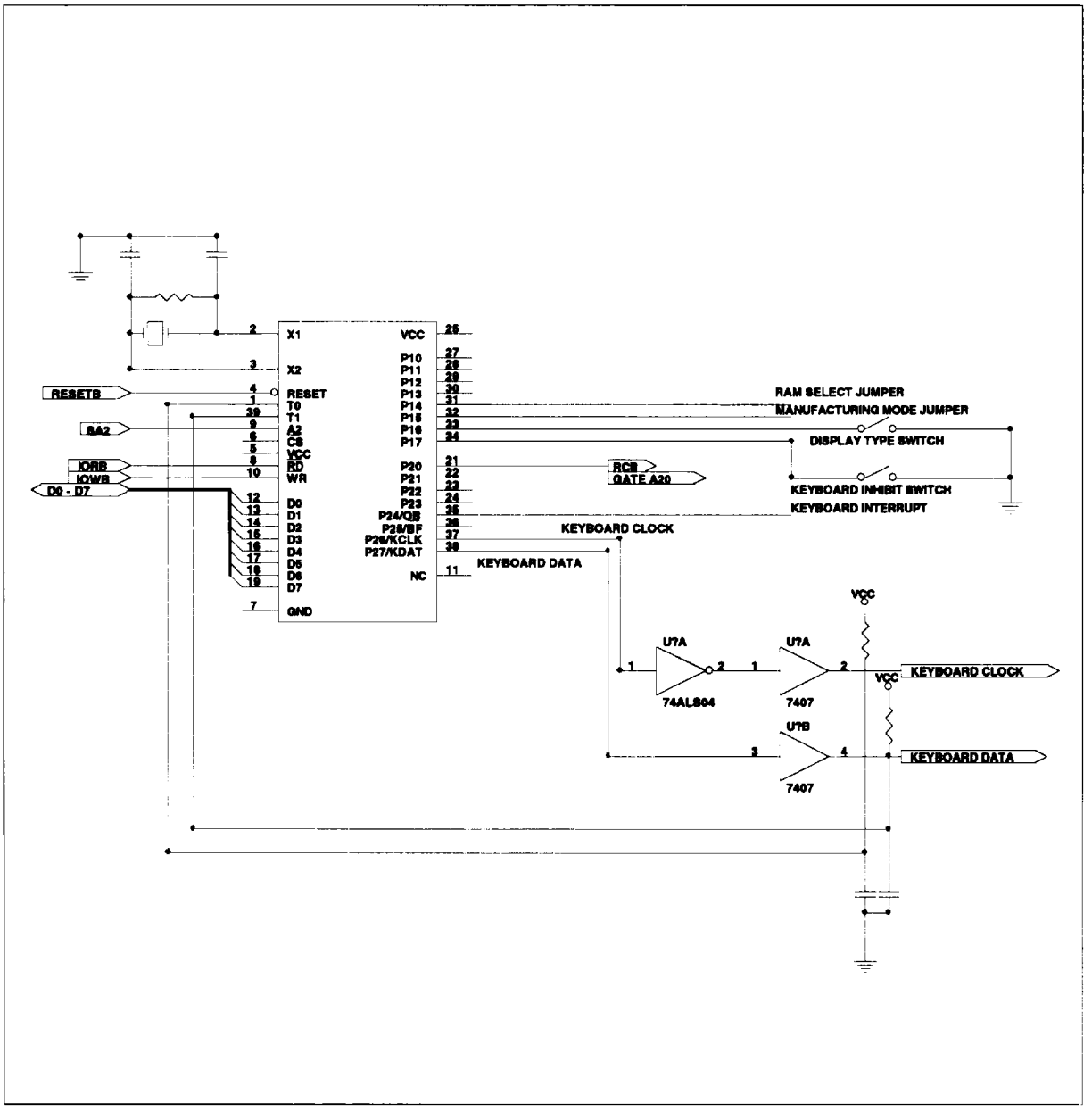
BIT	FUNCTION
0	Keyboard Clock (Input)
1	Keyboard Data (Input)

COMMANDS (I/O ADDRESS HEX 64)

COMMAND	FUNCTION
20	Read Command Byte of Keyboard Controller
60	Write Command Byte of Keyboard Controller **BIT** **BIT DEFINTIONS** 7 Reserved 6 IBM PC Compatible Mode 5 IBM PC Mode 4 Disable Keyboard 3 Inhibit Override 2 System Flag 1 Reserved 0 Enable Output Buffer Full Interrupt
AA	Self-test **BIT** **BIT DEFINTIONS** 00 No Error Detected 01 K/B Clock Line is Stuck Low 02 K/B Clock Line is Stuck High 03 K/B Data Line is Stuck Low 04 K/B Data Line is Stuck High
AB	Interface Test
AD	Disable Keyboard Feature
AE	Enable Keyboard Interface
C0	Read Input Port
D0	Read Output Port
D1	Write Output Port
E0	Read Test Inputs
F0-FF	Pulse Output Port

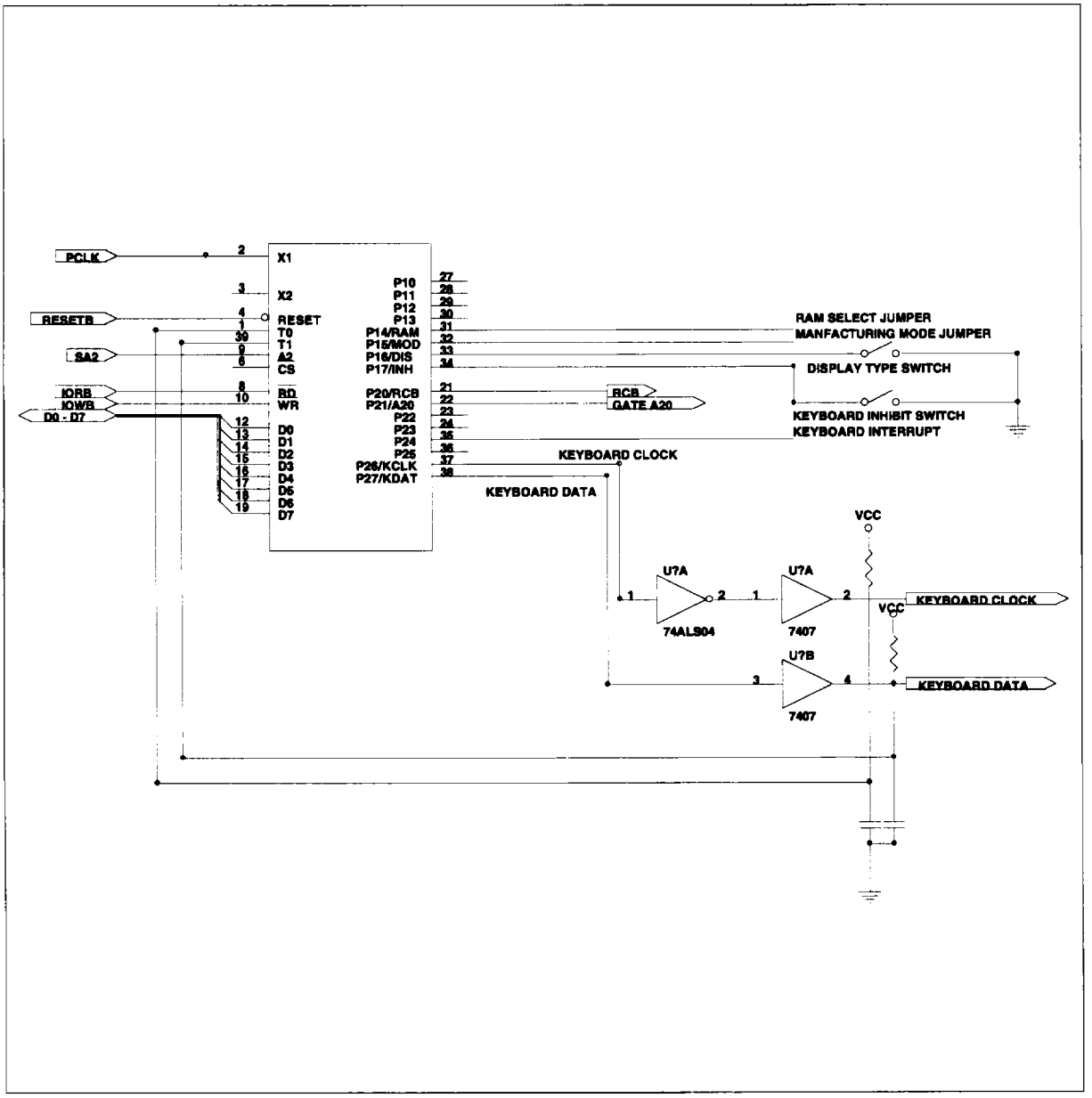
APPLICATION CIRCUIT

Asynchronous



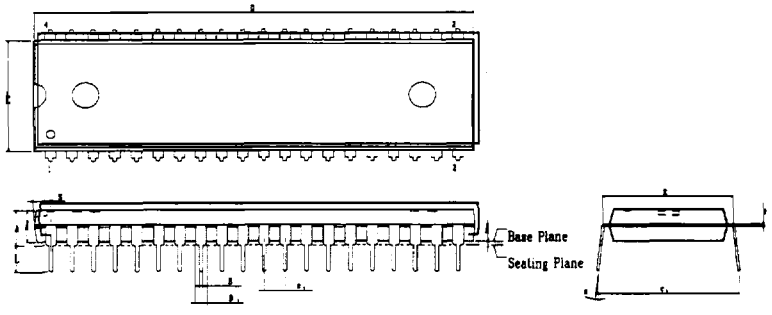
Application circuit, continued

Synchronous



PACKAGE INFORMATION

40-pin PDIP



Symb	Dimension			Dimension		
	Mi	Nc	Mc	Mi	Nc	Mc
A	—	—	0.21	—	—	5.3
A_1	0.01	—	—	0.2	—	—
A_2	0.15	0.15	0.16	3.8	3.9	4.0
B	0.01	0.01	0.02	0.4	0.4	0.5
B_1	0.04	0.05	0.05	1.2	1.2	1.3
C	0.00	0.01	0.01	0.2	0.2	0.3
D	—	2.05	2.07	—	52.2	52.5
E	0.59	0.60	0.61	14.5	15.2	15.4
E_1	0.54	0.54	0.55	13.7	13.8	13.9
e_1	0.09	0.10	0.11	2.2	2.5	2.7
L	0.12	0.13	0.14	3.0	3.3	3.5
a	0	—	15	0	—	15
e_A	0.63	0.65	0.67	16.0	16.5	17.0
S	—	—	0.09	—	—	2.2

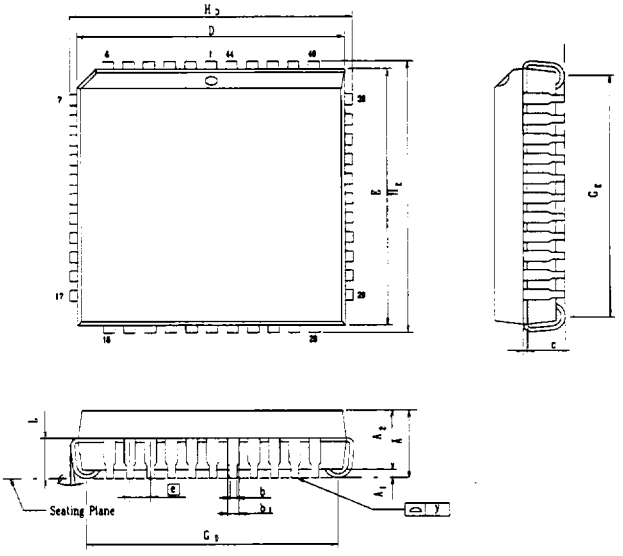
Not
1. Dimension D Max & S include tie bar
2. Dimension E does not include
3. Dimension D & E include mold are determined at the mold
4. Dimension B does not protrusion/intr
5. Controlling
6. General appearance spec. final visual

TITLE: 40LD P-DIP (600 mil) PACKAGE OUTLINE			
LEADFRAME MATERIAL:			
APPR.		DWG NO.	P040-SW1
R&D		REV NO.	B
Q.M		SCALE	
CHK.		DATE	
DEN.	Arvin Lain	SHT NO.	1/1

REV NO	DESCRIPTION	DATE
B	1.Update form . 2.The effective decimal 0.xx instead of 0.xxx n the metric	Mar,30

COPY CONTROLLED

44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Note:
1.Dimension D & E do not include interlead flash.
2.Dimension b does not include dambar protrusion/intrusion.
3.Controlling dimension : inch.
4.General appearance spec. should be based on final visual inspection spec.

TITLE: 44LD PLCC (0.653"SQ) PACKAGE OUTLINE			
LEADFRAME MATERIAL:	A151 3/4 H.		
APPR.		DWG NO.	CC44-SW1
R&D		REV NO.	B
Q.M		SCALE	
CHK.		DATE	
DEN.	Aven.Law	SHT NO.	1 / 1

REV NO	DESCRIPTION	DATE
B	1.Update form 2.The effective decimal 0.xx instead of 0.xxx in the metric system.	Feb,10

COPY CONTROLLED

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