# 1.0 INTRODUCTION

## 1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD7855 and WD7855LV System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances the WD7855 and WD7855LV operate similarly and are referred to in this document as the System Controller. Where there are differences, the devices are identified specifically.

## 1.2 FEATURES

***Features common to both versions of the WD7855***

- Single chip AT systems logic for desktops, notebooks, palmtops
- Supports 80386SX microprocessors at speeds up to 33 MHz
- Supports static, dynamic or cached CPUs
- Flexible DRAM support: 64K, 256K, 512K x 9, 1 Mbits, 4 Mbits, 1M x 18 bits or 2M x 9 bits
- Choice of non-page or page DRAM operating modes while supporting optional extra wait states for page mode
- Up to eight banks of two-way interleave memory support
- Support for major DRAM standards, including 88-pin DRAM card modules
- User-definable, non-cachable regions
- Supports external look aside cache
- Snoop interface to support cached CPUs
- Programmable full 16-bit I/O decode
- High-speed, local video bus (VLBI) support
- Slow Refresh
- Stop DMA clock
- 0.9 micron CMOS technology
- 160-pin MQFP package
- Three fully programmable Chip Selects in addition to standard Chip Selects
- AUTOFAST (automatic CPU speedup)
- SMI and I/O trapping
- Suspend/Resume modes
- Hibernation mode
- Multiple CPU speeds
- CPU Sleep/CPU Powerdown modes
- Peripheral and I/O power control
- System Activity Monitor (SAM) for idle detection

***WD7855LV Laptop Design***

- Supports 3.3 volt operation with on-chip translators for 5 volt AT bus (split rail operation)

## 1.3 GENERAL DESCRIPTION

Western Digital's® WD7855/LV single chip ISA System Controller is designed for high-performance IBM PC/AT compatible platforms. Available for desktop, portable or low voltage (LV) applications, the WD7855/LV supports the 80386SX microprocessor operating at speeds up to 33 MHz.

The WD7855/LV incorporates seven high-performance system controller functions which include the ISA bus interface, CPU interface, flexible memory controller, DMA controller, interrupt controller, timers and advanced power management. In combination with Western Digital's support devices, the WD7855/LV provides a highly flexible and powerful desktop or portable platform design.

The WD7855/LV is designed to work with all variations of 80386SX compatible microprocessors. It supports the traditional dynamic CPUs with the industry's only Processor Power-down feature to minimize power consumption. The WD7855/LV fully supports static microprocessors such as the AMD Am386SXL with CPU Stop Clock, System Management Interrupt and I/O trapping features. The WD7855/LV incorporates special circuitry which allows for optimizing the cache performance and maintaining cache coherency with cached CPUs such as the Cyrix Cx486SLC.

### 1.3.1 Desktop Applications

The WD7855 provides a high performance solution with a flexible memory controller architecture, including support for eight banks of two way interleave memory and EMS 4.0 hardware. The WD7855/LV can fully support an external look-aside cache or a combination primary and secondary cache. This feature makes it particularly suitable for use with cached microprocessors such as Cyrix Cx486SLC where it maintains cache coherency via its built-in bus snooping capability. In addition, the WD7855/LV supports Video Local Bus Interface (VLBI) for enhanced graphics performance.

### 1.3.2 Portable Applications

The WD7855LV is an ideal choice because of its advanced power management features and power saving 3.3 volt operation which delivers long battery life in a compact footprint. This makes it a perfect choice for laptop, notebook, penbased and palmtop computers.

The eight bank memory controller on the WD7855LV provides the user with great flexibility in the selection of 3.3 volt DRAMs to meet system memory requirements in low voltage platforms. The WD7855LV memory controller supports JEDEC standard 3.3 volt DRAM in various configurations, including the JEIDA standard 88-pin DRAM card.

The WD7855/LV can be paired with the appropriate support devices from Western Digital to deliver the most efficient solution for any platform. For 5 volt desktop or portable platforms, the WD7855LV can be used with the WD76C20 Peripheral Controller and the WD76C30 I/O Controller. Alternatively, the WD7855 can be used with the WD7615 Buffer Manager device and a generic Super I/O chip to implement a low cost desktop platform. For 3.3 volt applications, the WD7855LV can be used with the WD76C20ALV and WD76C30ALV, both of which incorporate level translators (split rail operation). For sub-notebook and palmtop type applications, WD7625LV buffer manager can be added to the WD7855LV based solution to achieve a very compact footprint.

The WD7855/LV is a fourth generation system controller device derived from core chips with proven compatibility and design maturity in several of the industry's leading desktop and portable platforms. Designed with the state of the art 0.9 micron high performance CMOS process, the WD7855/LV family maintains architectural compatibility with Western Digital's WD7600 and WD7700 systems logic chip sets while incorporating many additional performance enhancements.

### 1.3.3 WD7855/LV Power Management

With its built-in advanced power management features, the WD7855/LV delivers the lowest system power consumption and longest battery life in portable systems. The following information summarizes the key power management features offered by the WD7855/LV architecture.

#### 1.3.3.1 Automatic CPU Speedup

Depending on system activity, CPU speed automatically adjusts for slow speed when there is no activity and automatic speedup when activity is detected.

#### 1.3.3.2 CPU Sleep and Power-down

The processor is dynamically powered down during the idle periods (e.g. between keystrokes) and restored when any unmasked interrupt occurs. In case of a static processor, the CPU is simply operated at zero hertz during idle periods.

#### 1.3.3.3 Suspend and Resume Mode

Suspend is triggered by one of several user-defined events or a programmable timeout. During suspend, the system is shut down except for the WD7855/LV system memory, video memory and the video controller chip. These devices are sustained by a very slow clock until the WD7855/LV detects either the appropriate conditions or a modem ring indicator, and the power is restored.

#### 1.3.3.4 Peripheral Power Control

All peripherals are powered down during Suspend. The WD7855 features eight user-definable and eight dedicated outputs to control the LCD panel, backlight, keyboard controller, power supply and other user-selected functions. The power consumption of disk drives can be controlled by way of the drive's built-in power modes. I/O ports are managed through software control.

#### 1.3.3.5 System Activity Monitor

The system activity monitor watches all hardware inputs and allows better detection of idle conditions in the system following a programmable period of system inactivity.

#### 1.3.3.6 SMI Support

Supports the high-level power management interrupt and I/O trapping for more flexible power management.

#### 1.3.3.7 Hibernation Support

All registers within the WD7855/LV are readable including 8254 compatible timers, 8259 compatible interrupt controllers and 8237 DMA controllers. This allows for the entire system state to be easily stored to a file on the hard disk drive to allow complete system power-off and transparent restore.

#### 1.3.3.8 Slow Refresh

Slow 120 µs refresh is an option in both runtime and suspend operation.

#### 1.3.3.9 DMA Stop Clock

DMA clock automatically stops when there is no DMA activity and automatically restarts on any unmasked DMA request.

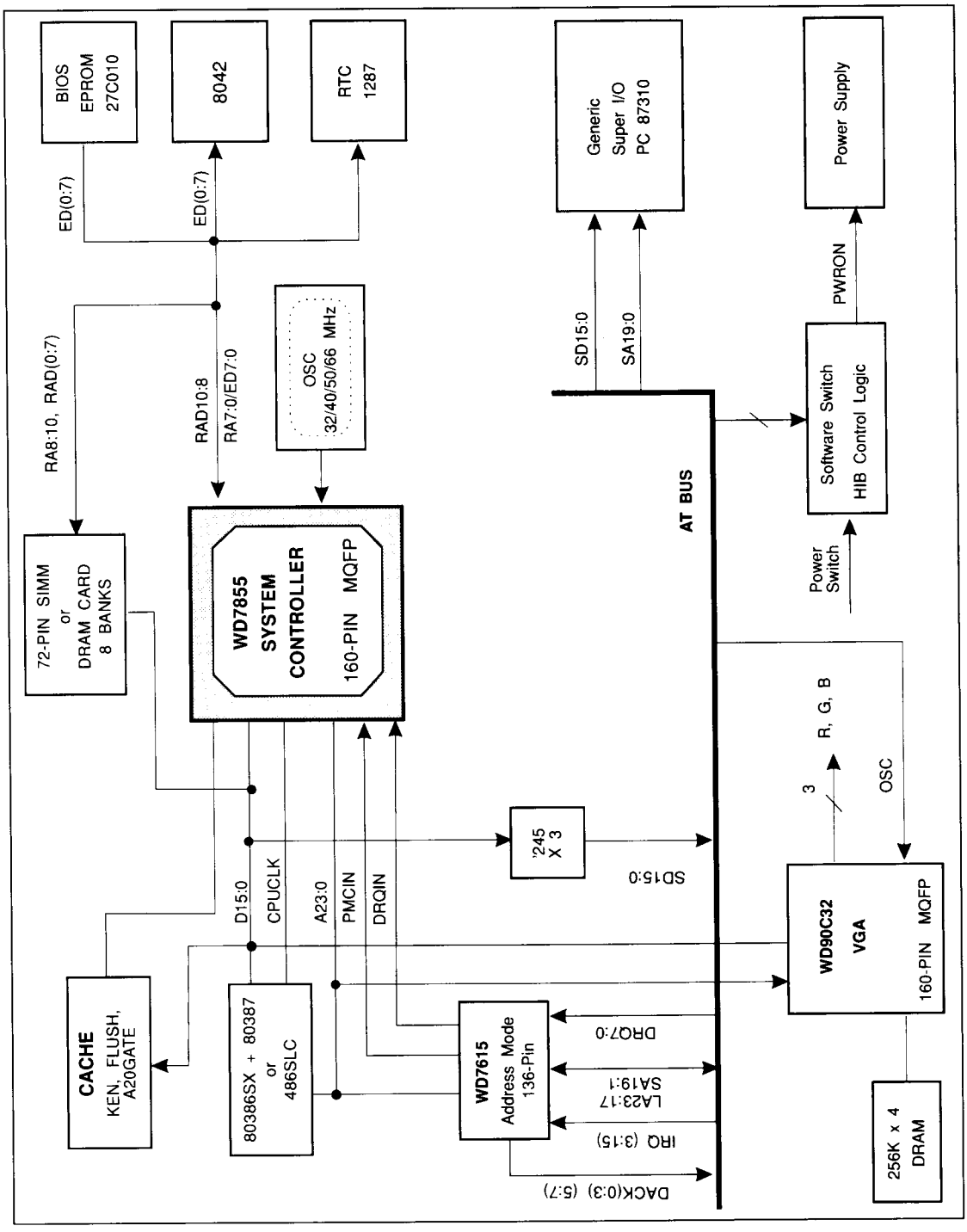


**FIGURE 1-1. POWER MANAGED DESKTOP SYSTEM BLOCK DIAGRAM**

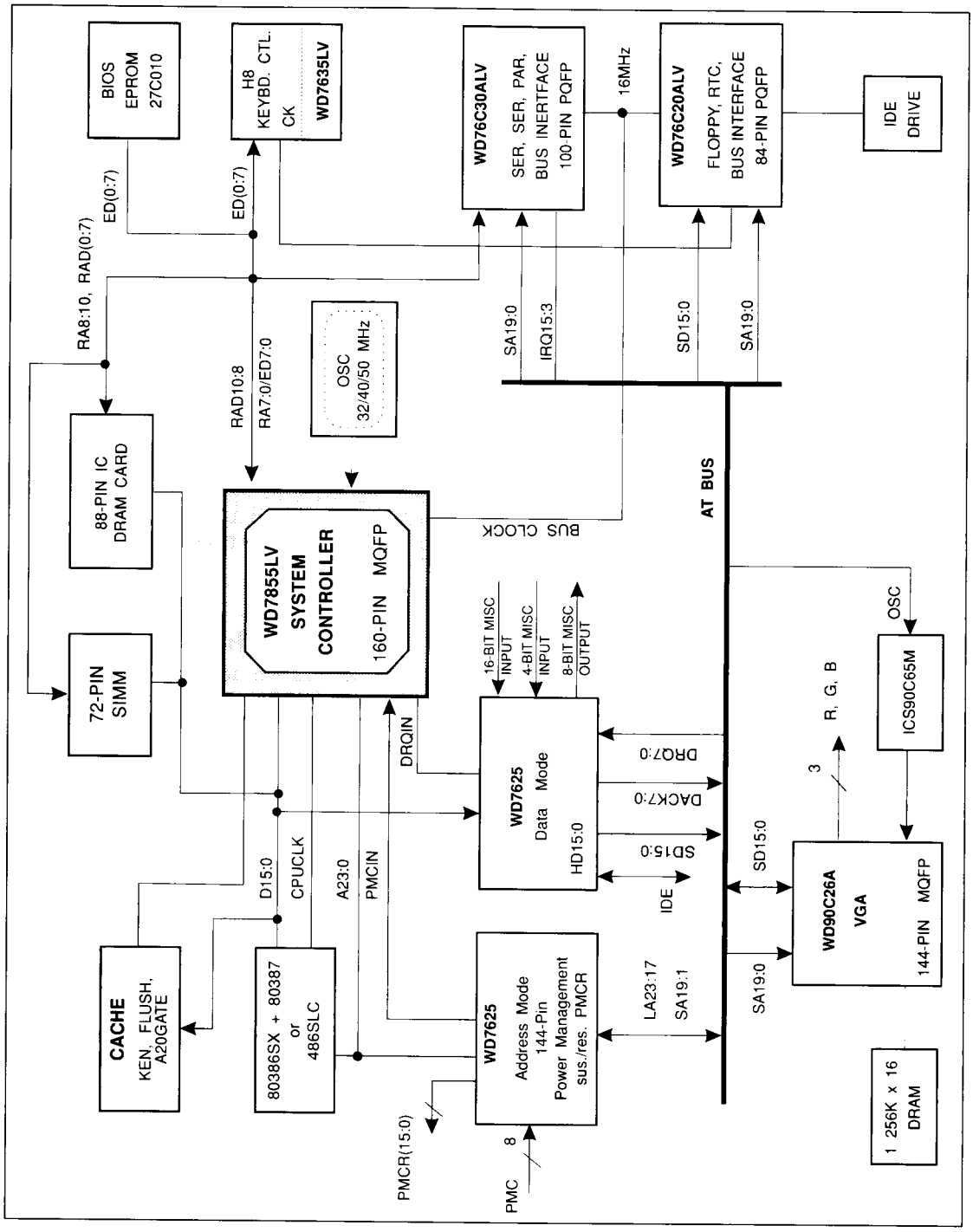


**FIGURE 1-2. NOTEBOOK SYSTEM BLOCK DIAGRAM**

# 2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80386SX processor control
- 80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control
- Register File
- Video Local Bus Interface (VLBI) control
- Cache control

Sections 2.1 through 2.10 provide an overview of these blocks and are described in more detail in sections 4 through 11.

## 2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the RSTIN signal, which it uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the RSTIN signal.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

## 2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests and speaker driver.

## 2.3 MAIN PROCESSOR CONTROL

This block controls whether the CPUCLK is to be an input or output. The WD7855/LV has the ability to reduce the processor clock rate and to stop the clock to the processor. The WD7855/LV also has the ability to power down the processor, at which time it tristates the CPUCLK, READY, HOLDR, INTRQ and NMI signals.

## 2.4 NUMERIC PROCESSOR CONTROL

Both System Controllers support an 80387SX processor.

## 2.5 DATA BUS

The Data Bus is a 16-bit (two bytes) bidirectional bus that connects to the processor's, System Controller, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

## 2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory. Both versions of the System Controller supports non-page mode memory and independent two-way interleave page mode access to the DRAM banks.

## 2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable notebook/laptop computers. When in a power down state, the WD7855/LV tristates the CPUCLK, READY, HOLDR, INTRQ and NMI output signals to the main processor. Also contained within this functional block are the SMI and SAM logic.

## 2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at Port Address 1872H, serve more than one area. In this instance the register description appears only in one section but is referred to in all appropriate sections.

The registers, and the section in which they are described, are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. Within the text, when the address is expressed as a three digit number, i.e., 092H - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at Port Address E072H and E872H and Port 70H Shadow Register at Port Address E472H, all registers located at Ports 1072H through FC72H are locked and inaccessible until unlocked by performing an eight-bit I/O write of DA to the Lock/Unlock Register at Port F073H. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72H twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

### 2.8.1 Lock Status Register

Port Address FC72H - Read only

Bits 11 through 03 are particularly useful in laptop applications by allowing the suspend/resume and Hibernation software to restore correct status to on-board devices.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| T | Not Used | | | DMA #2 CH3 | CH2 | CH1 | CH0 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| DMA #1 CH3 | CH2 | CH1 | CH0 | P4 | Not Used | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bit 15 - T,** Toggle

Changes state after every read of this port.

**Bits 14:12 -** Not used, state is ignored

**Bits 11:08 - DMA #2,** Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers, refer to Section 5.4.11.

1 = Channel enabled

0 = Channel disabled

**Bits 07:04 - DMA #1,** Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers, refer to Section 5.4.11.

1 = Channel enabled

0 = Channel disabled

**Bit 03 - P,** Parallel Port Direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit, refer to the WD76C30 Data Book, Section 4.3.

**Bits 02:00 -** Not used, state is ignored

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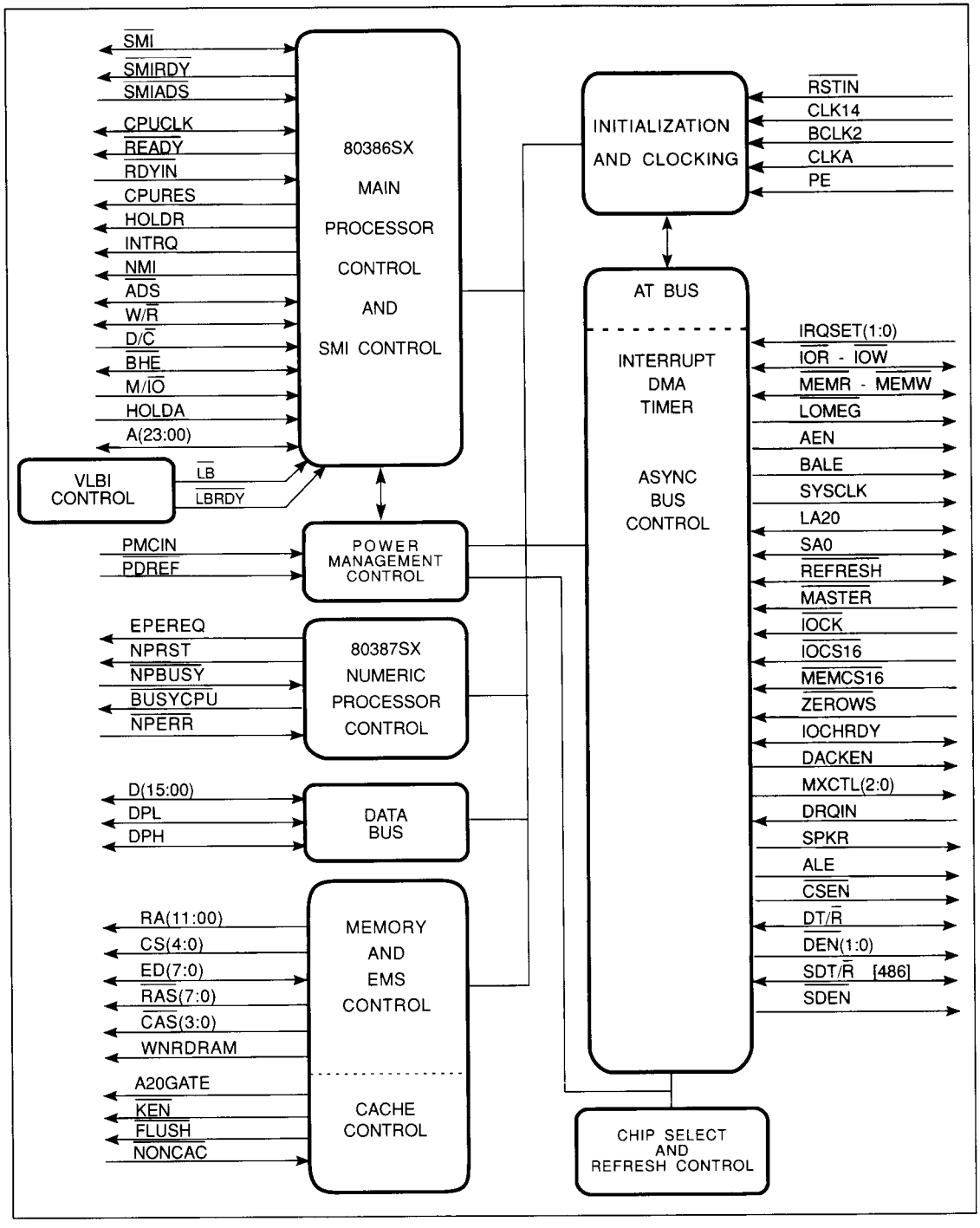


**FIGURE 2-1. WD7855/LV BLOCK DIAGRAM**

### 2.8.2 Lock/Unlock Register

Port Address F073H - Write only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| Not Used | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| L/UL = DA- | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals . . . . . | None |

**Bits 15:08** - Not used, state is ignored

**Bits 07:00 - L/UL,** Lock/Unlock

L/UL = DA -

11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -

Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

## 2.9 VLBI Control

The Video Local Bus Interface (VLBI) control is internal logic which interfaces with the WD90C56 VLBI controller. It has the ability to determine whether the current CPU cycle should be processed by the WD90C56 or other local bus devices or the WD7855/LV.

## 2.10 Cache Control

This functional block contains logic for controlling the cachable region for cached CPUs such as the Cyrix Cx486SLC. This functional block controls the $\overline{KEN}$ and $\overline{FLUSH}$ output signal pins.

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| PORT ADDRESS (HEX) | REGISTER NAME | LOCK/ UNLOCK | SECTION |
|---|---|---|---|
| 000 - 01F ① | DMA Control #1 (Channel 0:3) | No | 5.4, 5.6 * |
| 020 - 03F ② | Interrupt Controller #1 | No | 5.5 * |
| 040 | Timer 0, Time Of Day | No | 5.7 * |
| 041 | Timer 1, Refresh | No | 5.7 * |
| 042 | Timer 2, Speaker | No | 5.7 * |
| 043 | Control Word | No | 5.7 * |
| 060 - 06E even | Keyboard Controller | No | 8.5 * |
| 061 - 06F odd | Port B Parity Error And I/O Channel Check | No | 5.9 * |
| 070 | Real-Time Clock Address Register | No | 5.8.1 * |
| 071 | Real-Time Clock Data Register | No | 5.8.2 * |
| 080 - 09F | (except 092H) DMA Page Registers | No | 5.6.4 * |
| 092 | ALT A20 Gate and Hot Reset | No | 5.8.3 * |
| 0A0 - 0A1 ② | Interrupt Control Slave #2 | No | 5.4, 5.6 * |
| 0C0 - 0DE ① | DMA Control #2 (Channel 4:7) | No | 5.4 |
| 0F0 | Numeric Processor Busy Reset | No | 5.3.2 |
| 0F1 | Numeric Processor Reset | No | 5.3.3 |
| 1072 | CPU Clock Control | Yes | 4.2.4 |
| 1872 | Bus Timing And Power Down Control | Yes | 5.3.1 |
| 2072 | Refresh Control, Serial And Parallel Chip Selects | Yes | 8.1 |
| 2872 | RTC, PVGA And Disk Chip Selects | Yes | 8.2 |
| 2C72 | Bank 5 And Bank 4 Start Address | Yes | 6.2.2 |
| 3072 | Programmable Chip Select Address | Yes | 8.3 |
| 3472 | Bank 7 And Bank 6 Start Address | Yes | 6.2.2 |
| 3872 | Memory Control | Yes | 6.2.1 |
| 3C72 | DMA Shadow Register 1 | Yes | 9.13.1 |
| 4072 | Non-page Mode DRAM Memory Timing | Yes | 6.3.1 |
| 4472 | DMA Shadow Register 2 | Yes | 9.13.2 |
| 4872 | Bank 1 And Bank 0 Start Address | Yes | 6.2.2 |
| 4C72 | DMA Shadow Register 3 | Yes | 9.13.3 |
| 5072 | Bank 3 And Bank 2 Start Address | Yes | 6.2.2 |
| 5472 | SMI Auxiliary Control Register | Yes | 10.10 |
| 5872 | Split Start Address | Yes | 6.2.3 |
| 5C72 | Programmable CS2 and CS3 Control Register | Yes | 10.11 |
| 6072 | RAM Shadow And Write Protect | Yes | 6.2.4 |
| 6472 | Programmable CS2 Address Register | Yes | 10.12 |
| 6872 | EMS Control And Lower EMS Boundary | Yes | 6.4.1 |
| 6C72 | Programmable CS3 Address Register | Yes | 10.13 |
| 7072 | PMC Output Control 7:0 | Yes | 9.3 |
| 7472 | DRAM Size And SMI RAM Register | Yes | 6.2.6 |
| 7872 | PMC Output Control 15:8 | Yes | 9.3 |
| 7C72 | SMI I/O Trap Control Register | Yes | 10.2 |
| 8072 | PMC Timers | Yes | 9.4 |
| 8472 | SMI I/O Address Capture Register | Yes | 10.3 |
| 8872 | PMC Inputs 7:0 | Yes | 9.5 |
| 8C72 | I/O Data/Memory Address Capture Register Low | Yes | 10.4 |
| 9072 | NMI Status | Yes | 9.7 |
| 9472 | I/O Data/Memory Address Capture Register High | Yes | 10.5 |
| | | | * Tables 8-1:3 |

**TABLE 2-1. REGISTER INDEX**

| PORT ADDRESS (HEX) | REGISTER NAME | LOCK/ UNLOCK | SECTION |
|---|---|---|---|
| 9872 | Diagnostic | Yes | 11.1 |
| 9C72 | SMI I/O Timeout Control Register | Yes | 10.7 |
| A072 | Delay Line | Yes | 11.2 |
| A472 | SMI I/O Timeout Count Register 1 | Yes | 10.8 |
| A872 | Test Enable | Yes | 11.3 |
| AC72 | SMI I/O Timeout Count Register 2 | Yes | 10.9 |
| B072 | Activity Monitor Control | Yes | 9.11 |
| B472 | Noncachable Region 1, Lower Boundary | Yes | 7.5 |
| B872 | DMA Control Shadow | Yes | 5.4.15 |
| BC72 | Noncachable Region 1, Upper Boundary | Yes | 7.4 |
| C072 | High Memory Write Protect Boundary | Yes | 6.2.5 |
| C472 | Cache Control Register | Yes | 7.3 |
| C872 | PMC Interrupt Enables | Yes | 9.6 |
| CC72 | Noncachable Region 2, Lower Boundary | Yes | 7.6 |
| D072 | Serial/Parallel Shadow Register | Yes | 9.8 |
| D472 | Interrupt Controller Shadow | Yes | 9.9 |
| D872 | Activity Monitor Mask | Yes | 9.12 |
| DC72 | Test Status | Yes | 11.4 |
| E072 | EMS Page Register Pointer | No | 6.4.2 |
| E472 | Port 70H Shadow | No | 9.10 |
| E872 | EMS Page Register | No | 6.4.3 |
| F072 | 48 MHz Oscillator Disable | Yes | 8.5, Tables 8-1:3 |
| F472 | 48 MHz Oscillator Enable | Yes | 8.5, Tables 8-1:3 |
| F872 | Cache Flush | Yes | 7.7 |
| FC72 | Lock Status | Yes | 2.8.1 |
| F073 | Lock/Unlock | No | 2.8.2 |

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

**TABLE 2-1. REGISTER INDEX (Continued)**

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## 3.0 SIGNAL DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

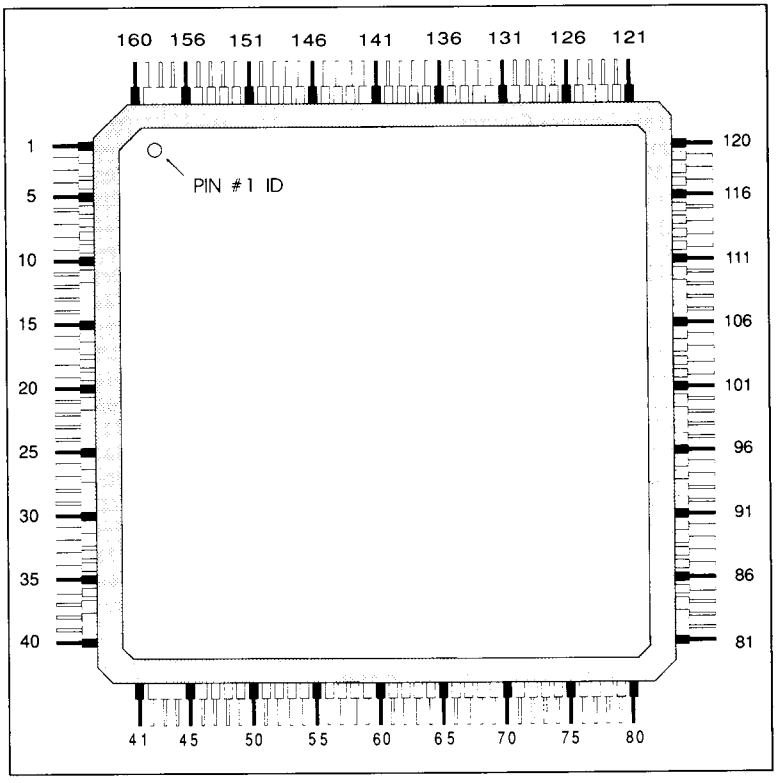


**FIGURE 3-1. 160-PIN MQFP PACKAGE**

| PIN - NAME | PIN - NAME | PIN - NAME | PIN - NAME |
|---|---|---|---|
| 1 - M/IO | 41 - PDREF | 81 - NC | 121 - CLKA/RDYIN/PE |
| 2 - W/R | 42 - PMCIN | 82 - NC | 122 - CPUCLK |
| 3 - BLE | 43 - WNRDRAM | 83 - NC | 123 - BUSYCPU |
| 4 - A1 | 44 - RAS0 | 84 - IOCK | 124 - NMI |
| 5 - ADS | 45 - LBRDY | 85 - IOCHRDY | 125 - NA |
| 6 - A20 | 46 - RAS1 | 86 - ZEROWS | 126 - INTRQ |
| 7 - A19 | 47 - CAS0 | 87 - IOCS16 | 127 - D0 |
| 8 - A18 | 48 - RAS2 | 88 - MASTER | 128 - D1 |
| 9 - A17 | 49 - RAS3 | 89 - MEMCS16 | 129 - D2 |
| 10 - VSS | 50 - VSS | 90 - CLK14 | 130 - VSS |
| 11 - A16 | 51 - CAS1 | 91 - VDDAT | 131 - D3 |
| 12 - A15 | 52 - RA10/CS2 | 92 - MEMW | 132 - D4 |
| 13 - A14 | 53 - RA9/CS1 | 93 - IOW | 133 - D5 |
| 14 - A13 | 54 - RA8/CS0 | 94 - IOR | 134 - D6 |
| 15 - ALE | 55 - SDT/R[486] | 95 - LA20 | 135 - VDD |
| 16 - A12 | 56 - VSS | 96 - SA0 | 136 - D7 |
| 17 - A11 | 57 - RA7/ED7 | 97 - MEMR | 137 - D8 |
| 18 - VSS | 58 - RA6/ED6 | 98 - REFRESH | 138 - D9 |
| 19 - VSS | 59 - SDEN | 99 - BALE | 139 - D10 |
| 20 - RA11 | 60 - NC | 100 - SYSCLK | 140 - NPBUSY |
| 21 - A10 | 61 - RA5/ED5 | 101 - AEN | 141 - VSS |
| 22 - VDD | 62 - VDD | 102 - VDD | 142 - D11 |
| 23 - A9 | 63 - RA4/ED4 | 103 - LB | 143 - VDD |
| 24 - A8 | 64 - RA3/ED3 | 104 - VSS | 144 - D12 |
| 25 - NONCAC | 65 - NC | 105 - EPERQ[VDD_VL] | 145 - NC |
| 26 - A7 | 66 - VDD | 106 - NPRST | 146 - D13 |
| 27 - A6 | 67 - RA2/ED2 | 107 - LOMEG | 147 - D14 |
| 28 - A5 | 68 - RA1/ED1 | 108 - SMI | 148 - D15 |
| 29 - A4 | 69 - RA0/ED0 | 109 - BHE | 149 - DT/R[VDDAT_VL] |
| 30 - FLUSH | 70 - VSS | 110 - SMIRDY | 150 - VSS |
| 31 - A3 | 71 - RAS4 | 111 - NPERR | 151 - DEN1 |
| 32 - A2 | 72 - RAS5 | 112 - D/C | 152 - DEN0 |
| 33 - IRQSET1 | 73 - CAS2 | 113 - SMIADS | 153 - A20GATE |
| 34 - IRQSET0 | 74 - RAS6 | 114 - READY | 154 - CPURES |
| 35 - MXCTLO | 75 - RAS7 | 115 - HOLDA | 155 - SPKR |
| 36 - VDD | 76 - DRQIN | 116 - HOLDR | 156 - VSS |
| 37 - MXCTL1 | 77 - CAS3 | 117 - NC | 157 - A23 |
| 38 - MXCTL2 | 78 - DPH/CS4 | 118 - NC | 158 - A22 |
| 39 - CSEN | 79 - DPL/CS3 | 119 - NC | 159 - A21 |
| 40 - DACKEN | 80 - RSTIN | 120 - BCLK2 | 160 - KEN |

**TABLE 3-1. 160-PIN MQFP - SIGNAL/PIN ASSIGNMENTS**

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | ***INITIALIZATION AND CLOCKING*** |
| 90 | CLK14 | I | **Clock 14** Translate +5<br>CLK14 is derived from a 14.318 MHz crystal and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume. For additional information, see Section 4, Initialization and Clocking. |
| 80 | $\overline{\text{RSTIN}}$ | I | **System Reset In** Translate +3<br>$\overline{\text{RSTIN}}$ drives a CMOS input level Schmitt Trigger and is used to reset the entire system at powerup. For additional information, see Section 4, Initialization and Clocking. |
| 120 | BCLK2 | I | **Bus Clock** Translate +3<br>BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz input signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input signal. BCLK2 may also be used to drive the processor clock. For additional information, see Section 4, Initialization and Clocking. |
| 121 | CLKA/<br>$\overline{\text{RDYIN}}$/<br>PE | I | **Clock A/Processor Ready In/Parity Error** Translate +3<br>Whether pin 121 is to be used as CLKA, $\overline{\text{RDYIN}}$ or PE is determined by the Memory Control Register at Port Address 3872H.<br><br>CLKA may be used as an alternate source for CPUCLK clock. For additional information, see Section 4, Initialization and Clocking.<br><br>$\overline{\text{RDYIN}}$ is used in a discrete cache system and indicates a hit or miss.<br><br>PE indicates a parity error from an external memory controller. |
| | | | ***AT BUS*** |
| 33 | IRQSET1 | I | **Interrupt Request Set 1** Translate +3<br>IRQSET1, along with MXCTL(2:0), selects one of the of the following: A20GT, IRQ1, IRQ(3:7), IRQ12. Refer to Table 5-1 and Figure 5-1. |

**Translate +3** - This signal may only be connected to a 3 volt signal bus when the System Controller VDD Core pins are powered by 3.3 volts.

**Translate +5** - This signal may be connected to a 5 volt signal bus when the System Controller core is powered by 3.3 volts. These signals are internally translated and require that the VDDAT pins be connected to a +5 volt source.

**TABLE 3-2. SIGNAL DESCRIPTION**

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *AT BUS (Cont.)* |
| 34 | IRQSET0 | I | **Interrupt Request Set 0** Translate +3<br>IRQSET0, along with MXCTL(2:0), selects one of the following: ROM8, $\overline{\text{RESCPU}}$, $\overline{\text{IRQ8}}$, IRQ(9:11), IRQ14 or IRQ15. Refer to Table 5-1 and Figure 5-1. |
| 35<br>37<br>38 | MXCTL0<br>MXCTL1<br>MXCTL2 | O | **Multiplexer Control(0:2)** Translate +3<br>MXCTL(0:2), along with DRQIN, DACKEN, IRQSET1, IRQSET0 and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, A20GT and $\overline{\text{RESCPU}}$. Refer to Table 5-1 and Figure 5-1. |
| 39 | $\overline{\text{CSEN}}$ | O | **Chip Select Enable** Translate +3<br>When $\overline{\text{CSEN}}$ is asserted, DPH, DPL, and RA10-RA8 are used to generate one of 30 different chip selects. Refer to Table 8-3. |
| 40 | DACKEN | O | **DACK Enable** Translate +3<br>When DACKEN is asserted, MXCTL(2:0) are used to generate DACK(7:5), (3:0) and BUS_RST. Refer to Table 5-1 and Figure 5-1. |
| 76 | DRQIN | I | **Multiplexed DRQ Inputs** Translate +3<br>DRQIN, along with MXCTL(2:0), selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1 |
| 85 | IOCHRDY | I/O | **I/O Channel Ready** Translate +5<br>Indicates extra wait states are required for the AT bus cycles. |
| 86 | $\overline{\text{ZEROWS}}$ | I | **Zero Wait States** Translate +5<br>Indicates the current AT bus cycle can be finished early. |
| 87 | $\overline{\text{IOCS16}}$ | I | **16-Bit I/O Cycle** Translate +5<br>Indicates the I/O device on the AT bus is a 16-bit slave. |
| 89 | $\overline{\text{MEMCS16}}$ | I | **16-Bit Memory Cycle** Translate +5<br>Indicates that the memory device on the AT bus is a 16-bit slave. |
| 155 | SPKR | O | **Speaker** Translate +3<br>SPKR drives the speaker transistor. |
| 96 | SA0 | I/O | **System Address 0** Translate +5<br>When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line.<br>When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0. |

**TABLE 3-2. SIGNAL DESCRIPTION (Continued)**

10

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *AT BUS (Cont.)* |
| 95 | LA20 | I/O | **Early Address 20** Translate +5<br>When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line.<br>When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20. |
| 88 | $\overline{\text{MASTER}}$ | I | **Master** Translate +5<br>$\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ to be selected as input signals. |
| 15 | ALE | O | **Address Latch Enable** Translate +3<br>ALE is used to clock the SA(19:1) address latches. |
| 101 | AEN | O | **Address Enable** Translate +5<br>AEN is asserted by the System Controller while performing DMA and Refresh cycles. |
| 59 | $\overline{\text{SDEN}}$ | O | **Swap Data Enable** Translate +3<br>$\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus. |
| 98 | $\overline{\text{REFRESH}}$ | I/O | **Refresh** Translate +5<br>As an output, $\overline{\text{REFRESH}}$ is asserted by the System Controller to refresh memory on the AT Bus.<br>As an input, $\overline{\text{REFRESH}}$ is asserted by the Bus Master in conjunction with $\overline{\text{MEMR}}$ to refresh memory on the AT Bus and DRAM controlled by the System Controller. |
| 107 | $\overline{\text{LOMEG}}$ | O | **First Megabyte** Translate +3<br>$\overline{\text{LOMEG}}$ is asserted when the AT bus address is below 1 Mbyte. Used with $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ to generate $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$. |
| 92 | $\overline{\text{MEMW}}$ | I/O | **Memory Write** Translate +5<br>$\overline{\text{MEMW}}$ is an output and is asserted by the System Controller when a memory write access to the AT bus is to take place.<br>$\overline{\text{MEMW}}$ is an input during Master Mode and is driven by the current Bus Master. |
| 97 | $\overline{\text{MEMR}}$ | I/O | **Memory Read** Translate +5<br>$\overline{\text{MEMR}}$ is an output and is asserted by the System Controller when a memory read access to the AT bus is to take place.<br>$\overline{\text{MEMR}}$ is an input during Master Mode and is driven by the current Bus Master. |

**TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)**

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *AT BUS (Cont.)* |
| 93 | $\overline{IOW}$ | I/O | **I/O Write** Translate +5<br>$\overline{IOW}$ is an output and is asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus.<br><br>$\overline{IOW}$ is an input during Master Mode and is driven by the current Bus Master. |
| 94 | $\overline{IOR}$ | I/O | **I/O Read** Translate +5<br>$\overline{IOR}$ is an output and is asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus.<br><br>$\overline{IOR}$ is an input during Master Mode and is driven by the current Bus Master. |
| 55 | SDT/$\overline{R}$[486] | I/O | **Swap Data Transmit/Receive** Translate +3<br>SDT/$\overline{R}$ controls the direction of the buffer between the low byte and high byte of the AT bus. SDT/$\overline{R}$ is tristated and pulled up by a 50K pullup resistor internal to the WD7855/LV when $\overline{RSTIN}$ at pin 80 is asserted. SDT/$\overline{R}$ pin may be forced low at reset with a 5K pulldown resistor, or an open collector or tristate driver driven by $\overline{RSTIN}$.<br><br>**SDT/$\overline{R}$ Mode - Output**<br>Forcing SDT/$\overline{R}$ high while $\overline{RSTIN}$ is low selects the SDT/$\overline{R}$ mode. Holding SDT/$\overline{R}$ high as $\overline{RSTIN}$ goes high maintains the SDT/$\overline{R}$ mode.<br><br>When SDT/$\overline{R}$ is high, it directs data from the low byte of the AT Bus to the high byte.<br><br>When SDT/$\overline{R}$ is low, it directs data from the high byte of the AT bus to the low byte.<br><br>**80486 Mode - Input**<br>Forcing SDT/$\overline{R}$ low while $\overline{RSTIN}$ is low selects the 80486 mode.<br>Holding SDT/$\overline{R}$ low as $\overline{RSTIN}$ goes high, maintains the 80486 mode.<br><br>Selecting 80486 mode sets the SRC bit in Port 1072H to 1. This causes CLKA at pin 121 to be the default processor clock source input. |

**TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)**

10

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | ***AT BUS (Cont.)*** |
| 149 | DT/$\overline{R}$ [VDDAT_VL] | I/O | **Data Transmit/Receive** Translate +3<br>DT/$\overline{R}$ controls the direction of the AT Data Bus D(15:00).<br><br>When DT/$\overline{R}$ is high, data is directed to the AT Bus.<br>When DT/$\overline{R}$ is low, data is transferred from the AT bus.<br><br>**VDDAT_VL**<br>When the AT Bus signals are powered by 3.3 volts, pin 149 must be connected to a 20K pull-down resistor. If no pull-down resistor is connected, a 5 volt AT Bus is enabled. The status of this strapping may be read at Port Address CC72H bit 02 (BS). |
| 151 | $\overline{DEN1}$ | O | **Data Bus Enable 1** Translate +3<br>When asserted, $\overline{DEN1}$ enables the high order byte data buffer. |
| 152 | $\overline{DEN0}$ | O | **Data Bus Enable 0** Translate +3<br>When asserted, $\overline{DEN0}$ enables the low order byte data buffer. |
| 100 | SYSCLK | O | **System Clock** Translate +5<br>The maximum frequency is 10 MHz.<br><br>In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz.<br><br>In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming. |
| 99 | BALE | O | **AT Bus Address Latch Enable** Translate +5<br>Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2). |
| 84 | $\overline{IOCK}$ | I | **I/O Channel Check** Translate +5<br>When asserted, $\overline{IOCK}$ indicates a bus or memory error is on the AT bus and generates an NMI to the processor. |
| | | | ***MAIN PROCESSOR CONTROL*** |
| 45 | $\overline{LBRDY}$ | I | **Local Bus Ready** Translate +3<br>Local bus cycle ready signal. $\overline{LBRDY}$ can be used by an external look-aside cache controller to signal cache hits. |
| 103 | $\overline{LB}$ | I | **Local Bus** Translate +3<br>Local bus cycle request signal. $\overline{LB}$ allows an alternate device to respond to a cycle normally mapped to the AT Bus. |
| 108 | $\overline{SMI}$ | I/O | **System Management Interrupt** Translate +3<br>SMI request to the processor. This mode of operation is selected by bit 13 at Port Address C472H. |

**TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)**

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | ***MAIN PROCESSOR CONTROL (Cont.)*** |
| 109 | $\overline{BHE}$ | I/O | **Bus High Enable** Translate +3<br>As an input, $\overline{BHE}$ indicates a transfer of the high byte on the processor data bus. $\overline{BHE}$ is an output during DMA transfers. |
| 110 | $\overline{SMIRDY}$ | O | **System Management Interrupt Ready** Translate +3<br>$\overline{SMIRDY}$ provides a ready signal to the processor during SMI cycles. $\overline{SMIRDY}$ is asserted according to the SMI CPU mode selected. This pin is not used by Cx486SLC (see pin 114). |
| 112 | D/$\overline{C}$ | I | **Data /Control** Translate +3<br>D/$\overline{C}$ is asserted by the CPU to indicate the status of the current instruction cycle. |
| 1 | M/$\overline{IO}$ | I/O | **Memory or I/O** Translate +3<br>When high, M/$\overline{IO}$ indicates a processor memory cycle<br>When low, M/$\overline{IO}$ indicates a processor $\overline{I/O}$ cycle.<br><br>When enabled during DMA or Master cycles, the System Controller drives this signal to maintain Cache coherency. |
| 5 | $\overline{ADS}$ | I/O | **Address Strobe** Translate +3<br>$\overline{ADS}$ signal from the processor initiates all memory and I/O cycles in the System Controller.<br><br>When enabled during DMA or Master cycles, the System Controller drives this signal to maintain Cache coherency. |
| 113 | $\overline{SMIADS}$ | I | **System Management Interrupt Address Strobe** Translate +3<br>For supported CPU's $\overline{SMIADS}$ indicates that the cycle is directed to SMI memory space. |
| 2 | W/$\overline{R}$ | I/O | **Write/Read** Translate +3<br>During normal CPU cycles, W/$\overline{R}$ is an input indicating whether a read or write cycle is to occur.<br><br>When W/$\overline{R}$ is high, a write to memory occurs.<br>When W/$\overline{R}$ is low, a read from memory occurs.<br><br>When operating with cached processors, W/$\overline{R}$ is an output signal used to invalidate the internal CPU cache line during DMA or Master mode memory write cycles. |
| 114 | $\overline{READY}$ | O | **Processor Ready** Translate +3<br>$\overline{READY}$ is an output to the processor signalling the completion of a cycle. For CPUs that do not have a separate $\overline{SMIRDY}$ pin, such as Cx486SLC, this signal is used for both SMI and non-SMI cycles. |
| 116 | HOLDR | O | **Hold Request** Translate +3<br>HOLDR is an output to the Processor requesting control of the CPU local bus. |

**TABL 3-2. SIGNAL DESCRIPTIONS (Continued)**

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| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | ***MAIN PROCESSOR CONTROL (Cont.)*** |
| 115 | HOLDA | I | **Hold Acknowledge** Translate +3<br>HOLDA is a response from the processor for the Hold Request. |
| 122 | CPUCLK | I/O | **Processor Clock** Translate +3<br>The speed of CPUCLK and whether it is to be an input or output, is selected by the CPU Clock Control Register at Port Address 1072H. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver. |
| 124 | NMI | O | **Non-maskable Interrupt** Translate +3<br>Processor non-maskable interrupt cycle request. |
| 125 | $\overline{NA}$ | O | **Next Address** Translate +3<br>NA is asserted by the System Controller to enable the CPU to operate in the Pipeline mode. |
| 126 | INTRQ | O | **Interrupt Request** Translate +3<br>Processor interrupt cycle request. |
| 154 | CPURES | O | **Main Processor Reset** Translate +3<br>CPURES is a synchronous processor reset signal. |
| 157:159<br>6:9<br>11:14<br>16:17<br>21<br>23:24<br>26:29<br>31:32<br>4, 3 | A(23:21)<br>A(20:17)<br>A(16:13)<br>A(12:11)<br>A10<br>A(9:8)<br>A(7:4)<br>A(3:2)<br>A1, $\overline{BLE}$ | I/O | **Processor Address A(23:A01)**<br>**Bus Low Enable (A0)** Translate +3<br>A(23:1) and $\overline{BLE}$ are address lines from the processor. During DMA or Master cycles, the lines are driven by the System Controller to represent the current memory address. |
| | | | ***NUMERIC PROCESSOR CONTROL*** |
| 140 | $\overline{NPBUSY}$ | I | **Numeric Processor Busy** Translate +3<br>$\overline{NPBUSY}$ is the busy signal from the numeric processor. |
| 105 | EPERQ<br>[VDD_VL] | O | **Extend Processor Extension Request** Translate +3<br>EPERQ extends PERQ to the 80386SX for IRQ13 handling.<br><br>**VDD_VL**<br>When the System Controller core signals are powered at 3.3 volts, pin 105 must be connected to a 20K pull-down resistor. When no pull-down resistor is connected, a 5 volt core is enabled. The status of this strapping may be read at port address CC72H bit 03 (CS). |
| 106 | NPRST | O | **Numeric Processor Reset** Translate +3<br>Reset to the numeric processor 80387SX. |

**TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)**

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | ***NUMERIC PROCESSOR CONTROL (Cont.)*** |
| 111 | $\overline{\text{NPERR}}$ | I | **Numeric Processor Error** Translate +3<br>Error signal from the numeric processor 80387SX. |
| 123 | $\overline{\text{BUSYCPU}}$ | O | **Coprocessor Busy** Translate +3<br>Coprocessor Busy signal to the processor. |
| | | | ***DATA BUS*** |
| 78 | DPH/CS4 | I/O | **Data Parity High Byte [Chip Select 4]** Translate +3<br>For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit 4 of the encoded chip select bus. |
| 79 | DPL/CS3 | I/O | **Data Parity Low Byte [Chip Select 3]** Translate +3<br>For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit 3 of the encoded chip select bus. |
| 148:146<br>144<br>142<br>139:136<br>134:131<br>129:127 | D(15:13)<br>D12<br>D11<br>D(10:7)<br>D(6:3)<br>D(2:0) | I/O | **Data Bits (15:0)** Translate +3<br>The Data Bits are connected directly to the Local and Numeric processors, DRAM data and AT Bus data transceivers. |
| | | | ***MEMORY AND EMS CONTROL*** |
| 25 | $\overline{\text{NONCAC}}$ | I | **Noncacheable** Translate +3<br>Externally decoded non-cacheable region. |
| 30 | $\overline{\text{FLUSH}}$ | O | **Flush** Translate +3<br>Flush signal to external (CPU) cache controller. $\overline{\text{FLUSH}}$ is asserted by writing any data to port address F872H. |
| 43 | WNRDRAM | O | **Write Not Read To DRAM** Translate +3<br>Write Not Read signal to DRAM. |
| 20<br>52<br>53<br>54 | RA11<br>RA10/CS2<br>RA9/CS1<br>RA8/CS0 | O | **DRAM Address Bits 11:8**<br>**Chip Select Bits 2:0** Translate +3<br>The DRAM Address Bus is multi-functional. During DRAM cycles, RA(11:0) select the DRAM row and column. |
| 57<br>58<br>61<br>63<br>64<br>67<br>68<br>69 | RA7/ED7<br>RA6/ED6<br>RA5/ED5<br>RA4/ED4<br>RA3/ED3<br>RA2/ED2<br>RA1/ED1<br>RA0/ED0 | I/O | **DRAM Address Bits 7:0**<br>**EDATA Bits 7:0** Translate +3<br>During I/O cycles, CS(2:0), along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED(7:0) represents the data from such devices as the Keyboard Controller on the EDATA bus. |

**TABLE 3-2. SIGNAL DESCRIPTION (Continued)**

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| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | ***MEMORY AND EMS CONTROL (Cont.)*** |
| 75<br>74<br>72<br>71<br>49<br>48<br>46<br>44 | $\overline{RAS7}$<br>$\overline{RAS6}$<br>$\overline{RAS5}$<br>$\overline{RAS4}$<br>$\overline{RAS3}$<br>$\overline{RAS2}$<br>$\overline{RAS1}$<br>$\overline{RAS0}$ | O | **Row Address Strobe 7:0** Translate +3<br>$\overline{RAS7:0}$ provide control of up to eight banks of 16 bit memory without external drivers. The outputs are strength controlled to provide optimum drive over process and load. The assertion of RAS signals is impacted by the programmed configuration of memory allowing for 2-way page interleave. |
| 77<br>73<br>51<br>47 | $\overline{CAS3}$<br>$\overline{CAS2}$<br>$\overline{CAS1}$<br>$\overline{CAS0}$ | O | **Column Address Strobe 3:0** Translate +3<br>$\overline{CAS(3:0)}$ are used to separately enable the upper and lower bytes of the active banks. |
| 153 | A20GATE | O | **A20 Gate** Translate +3<br>A20 Gate signal to external cache controller. |
| 160 | $\overline{KEN}$ | O | **Cache Enable** Translate +3<br>When asserted, $\overline{KEN}$ signals non-cacheable regions decoded by the System Controller to the CPU cache controller. |
| | | | ***POWER MANAGEMENT CONTROL*** |
| 41 | $\overline{PDREF}$ | I | **Power-down Refresh** Translate +3<br>$\overline{PDREF}$ is a 64 KHz signal from the WD76C20. During power-down, $\overline{PDREF}$ is passed internally to pin 98 ($\overline{REFRESH}$). |
| 42 | PMCIN | I | **Power Management Control Input** Translate +3<br>PMCIN is used to sample eight PMC inputs selected by MXCTL(2:0). See Table 5-1 and Figure 5-1. |
| | | | ***MISCELLANEOUS*** |
| 10, 18, 19, 50, 56, 70, 104, 130, 141, 150, 156 | VSS | I | **Ground** |
| 91 | VDDAT | I | **5 Volts Power for signals interfaced to 5 volt busses.** |
| 22, 36, 62, 66, 102, 135, 143 | VDD | I | **3.3 volt or 5 Volt power (core)** |
| 60, 65, 81, 82, 83, 117, 118, 119, 145 | N. C. | | Not connected. Reserved for future use. |

**TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)**

# 4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK) and the processor clock (CPUCLK).

## 4.1 POWER UP RESET

The system reset signal, RSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor. At this time the System Controller also resets the AT bus by asserting DACKEN and MXCTL(2:0) = 100, which are decoded externally as BUS_RST (DACK4), see sections 5.1, 5.1.1, Table 5-1 and Figure 5-1. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. During RSTIN with BUSYCPU asserted the processor may perform its self-test operation immediately following the power up reset.

## 4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CLKA and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

### 4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.318 MHz crystal and is used for the control of the 8254 compatible timers. CLK14 is switched by the System Controller to 32 KHz during save and resume operations.

### 4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872H. SYSCLK is always one half or one fourth the value of the selected input clock (refer to Figure 4-1).

### 4.2.3 Processor Clock (CPUCLK)

The processor clock may be either an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. In portable applications CPU clock is most likely an output to allow AUTOFAST and Stop clock modes. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CLKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872H. The PMC control output 0 tristates the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by SCHH or SCH (CPU Clock Control Register - bits 01 or 00, at Port Address 1072H) or divided down by CLK_SPD (bits 14:12). When CPUCLK is stopped it is in phase two of the 80386SX. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so CLK_SPD also provides some choices of clock duty cycle. The other method can be used when the CPUCLK is an output or input and generated by an external oscillator. In this case, EXT_HOLD is used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, CLKA is used in place of the BCLK2. This choice is determined by SRC (CPU Clock Control Register bit 15 at Port Address 1072H). SRC is set automatically at power up reset.

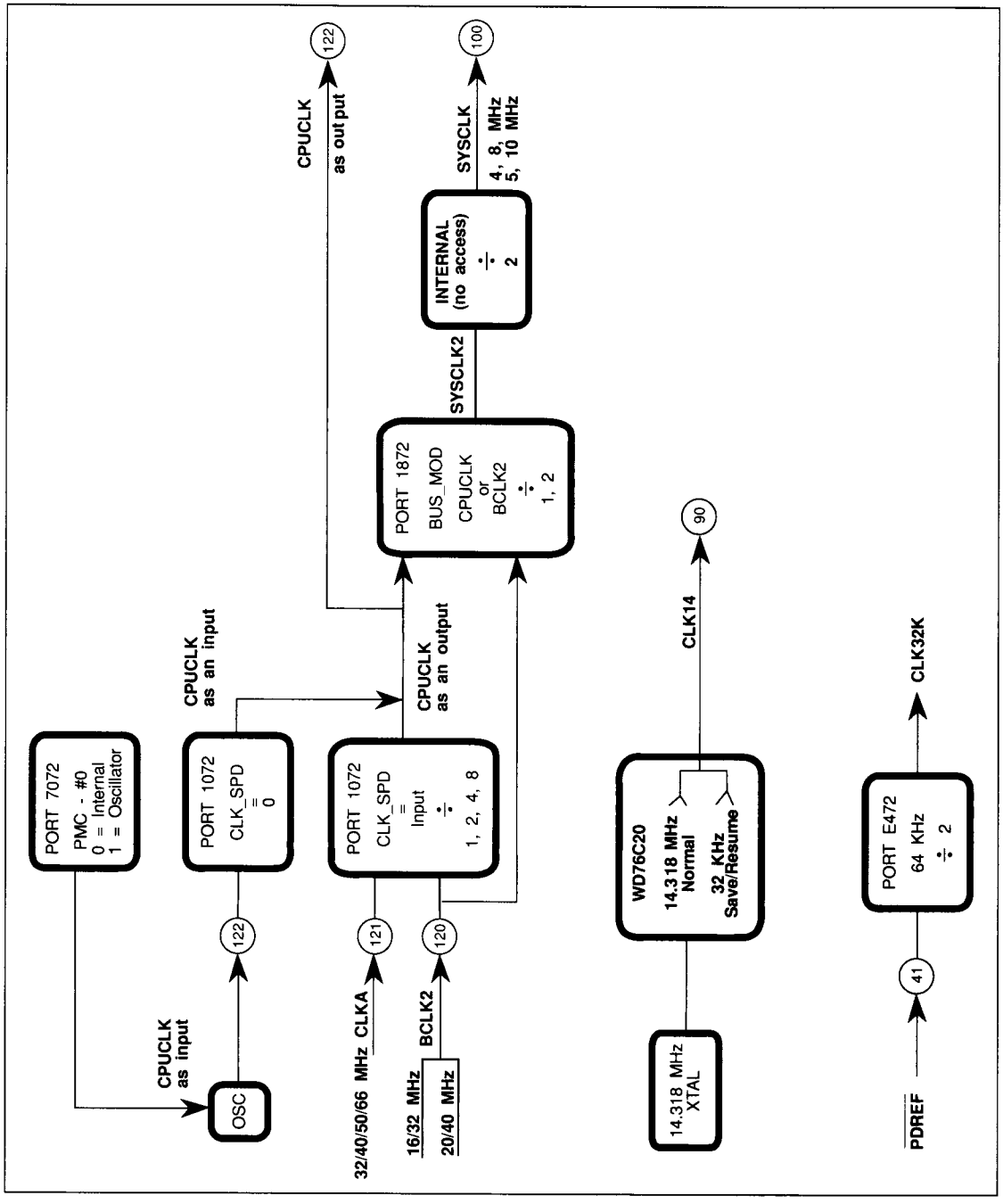


**FIGURE 4-1. CLOCK CONTROL**

### 4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| SRC | CLK_SPD | | | AUT_ FST | ALT_CLK_SPD | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| EXT_HOLD | | | | | | SCHH | SCH |

| Signal Name | Default At RSTIN |
|---|---|
| SRC | 0/1 |
| CLK_SPD | 000/001 |
| AUT FST | 0 |
| ALT CLK SPD | 000 |
| EXTEND HOLD | 0000 |
| Bits 03, 02 | None |
| SCH | 0 |
| SCHH | 0 |

**Bit 15 - SRC,** CPUCLK Clock Source

When CPUCLK is selected as an output by bits 14 through 12, SRC determines whether it is to be driven by BCLK2 or CLKA.

**Default Value**

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CLKA does not change state within 64 clocks after $\overline{\text{RSTIN}}$ is de-asserted.

SRC is set to 1 and CLKA is used as the CPUCLK clock source if CLKA changes state within 64 clocks after $\overline{\text{RSTIN}}$ is de-asserted, or when operating in the 80486 Mode. The 80486 Mode is selected by holding SDT/$\overline{\text{R}}$ low during $\overline{\text{RSTIN}}$ transition from low to high.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CLKA is the CPUCLK source.

**Bits 14:12 - CLK_SPD,** CPUCLK Clock Speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD *defaults to 000 or 001 at power up. Changing the CPUCLK from an input (CLK_SPD = 000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One millisecond later, CPUCLK becomes active as an output. One millisecond and 16 CPUCLK clocks (or one millisecond) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated due to the clock driver not being able to synchronously switch the clock. The one millisecond and 16 clocks or one millisecond selection is made through the Diagnostic Register at Port 9872H.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source (* Default value).
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (* Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

* Based upon the value of CLOCK_DIR_IN at power up (refer to Table 5-1, Figure 5-1 and section 5.1.2).

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**Bit 11 - AUT_FST,** Automatic Processor Clock Speed Switching

When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external TURBO signal is de-asserted when auto switching is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-2. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external TURBO signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCHH or SCH field is programmed to stop the clock. The clock restarts or returns to the faster rate when any interrupt occurs.

Table 4-2 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
Automatic Clock Switching is disabled. TURBO determines whether CLK_SPD or ALT_CLK_SPD is to be used as the CPU clock. Refer to Table 4-1 for the appropriate selection, as determined by TURBO.

AUT_FST = 1 -
Automatic CPUCLK Switching between CLK_SPD and ALT_CLK_SPD is enabled when TURBO is de-asserted. CLK_SPD is selected when TURBO is asserted. Refer to Table 4-1. The EXT_HOLD field must be 0000 when AUT_FST = 1.

| TURBO | AUTO_FST | CPU CLOCK SPEED |
|---|---|---|
| 0 | 0 | CLK_SPD |
| 0 | 1 | CLK_SPD |
| 1 | 0 | ALT_CLK_SPD |
| 1 | 1 | CLK_SPD or ALT_CLK_SPD |

**TABLE 4-1. CLOCK SWITCH SELECTION**

| SPEEDUP ACTIVITY | TIME PERIOD |
|---|---|
| Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O | 1 second |
| Keyboard interrupt | 1 second or until next video access |
| Video access or processor reset | 1 millisecond |
| Any NMI or IRQ interrupt, except keyboard or hard disk | 1 millisecond |

**TABLE 4-2. SPEEDUP ACTIVITY**

**Bits 10:08 - ALT_CLK_SPD,** Alternate Clock Speed

ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD.
0 0 1 - Equals source.
0 1 0 - Equals source div by 2.
0 1 1 - Equals source div by 4, 25% duty cycle.
1 0 0 - Equals source div by 4, 75% duty cycle.
1 0 1 - Equals source div by 8, 12% duty cycle.
1 1 0 - Equals source div by 8, 88% duty cycle.

**Bits 07:04 - EXT_HOLD,** Extend Processor Hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external TURBO signal is asserted, EXT_HOLD is forced to 0000. When the external TURBO signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension
0 0 0 1 - 1 µs hold after refresh.
0 0 1 0 - 2 µs hold after refresh.
0 0 1 1 - 3 µs hold after refresh.
0 1 0 0 - 4 µs hold after refresh.
↕
1 1 0 1 - 13 µs hold after refresh.
1 1 1 0 - 14 µs hold after refresh.
1 1 1 1 - 15 µs hold after refresh.

**Bits 03:02 -** Reserved for future use, must be set to zero

**Bit 01 - SCHH,** Stop CPUCLK at next Halt and Hold.

SCHH is applicable only for Am386SXL or other static type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7855 rather than an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected.

SCHH = 0 -
Normal processor clock.

SCHH = 1 -
Stop processor clock at next halt and hold cycle.

**Bit 00 - SCH,** Stop CPUCLK at next Hold

SCH is applicable only for Am386SXL or other static type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7855 instead of an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped.

SCH = 0 -
Normal processor clock.

SCH = 1 -
Stop processor clock at next processor hold cycle.

10

# 5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

## 5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL(2:0) and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL(2:0) are set to 100 during a System Reset ($\overline{RSTIN}$) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8) and processor clock (CPUCLK) pin direction. See Table 5-1.

### 5.1.1 Data Acknowledge DACK(7:5), (3:0)

For desktop systems, either a Western Digital WD7615 or a 74F138 3-to-8 Decoder uses MXCTL(2:0) to generate the DACK(7:5) and DACK(3:0), which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). For Laptop systems a WD7625 or 74ACT138 3-to-8 Decoder is used instead of the WD7615 or 74F138, 3-to-8 Decoder. The decoder is enabled by the DACKEN signal from the System Controller.

### 5.1.2 Data Request DRQIN

The MXCTL(2:0) signals are used to develop the DRQIN signal received by the System Controller by an external 74F151 8-to-1 Multiplexer for desktop systems, or by a 74ACT151 8-to-1 Multiplexer for laptop systems. The MXCLT(2:0) signals are held stable during DMA transfers. A Western Digital WD7615 may be used in place of the 74F151 and a WD7625 in place of the 74ACT151.

Immediately following a System Reset ($\overline{RSTIN}$), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after $\overline{RSTIN}$ is de-asserted. See Table 5-1 and Figure 5-1. This controls the default value of CLK_SPD in the CPU Clock (CPUCLK) Control Register at Port 1072H. See section 4.2.4.

### 5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA, DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a $\overline{RSTIN}$ to determine ROM data width (ROM8). The $\overline{RESCPU}$ and A20GT inputs come from the 8042 keyboard controller.

### 5.1.4 AT Address Bus, Data Bus and Terminal Count (TC) Signal

The AT Address Bus SA(19:00) and $\overline{BLE}$ are generated from A(19:00) with external latches and tristate buffers.

The AT Data Bus SD(15:00) uses D(15:00) and external bidirectional buffers.

The TC signal is generated by the WD76C20 when DACKEN and $\overline{CSEN}$ are both asserted.

## 5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an 8-to-1multiplexer, controlled by the MXCTL(2:0) signals from the System Controller. In the WD7855/LV, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of Port 1872H (Section 5.3) control the power down of the processor and peripheral.

| MXCTL 2 1 0 | DRQIN | DACKEN | IRQSET0 | IRQSET1 | PMCIN |
|---|---|---|---|---|---|
| 000 | DRQ0 | DACK0 | $\overline{IRQ8}$ | IRQ12 | $\overline{TURBO}$ |
| 001 | DRQ1 | DACK1 | IRQ9 | IRQ1 | PROC_PWR_GOOD |
| 010 | DRQ2 | DACK2 | IRQ10 | A20GT | LCL_REQ or User Defined |
| 011 | DRQ3 | DACK3 | IRQ11 | IRQ3 | User Defined |
| 100 | CLOCK_ DIR_IN | BUS_RST | ROM8 | IRQ4 | User Defined |
| 101 | DRQ5 | DACK5 | $\overline{RESCPU}$ | IRQ5 | User Defined |
| 110 | DRQ6 | DACK6 | IRQ14 | IRQ6 | User Defined |
| 111 | DRQ7 | DACK7 | IRQ15 | IRQ7 | User Defined |

**TABLE 5-1. MXCTL(2:0) DECODING**

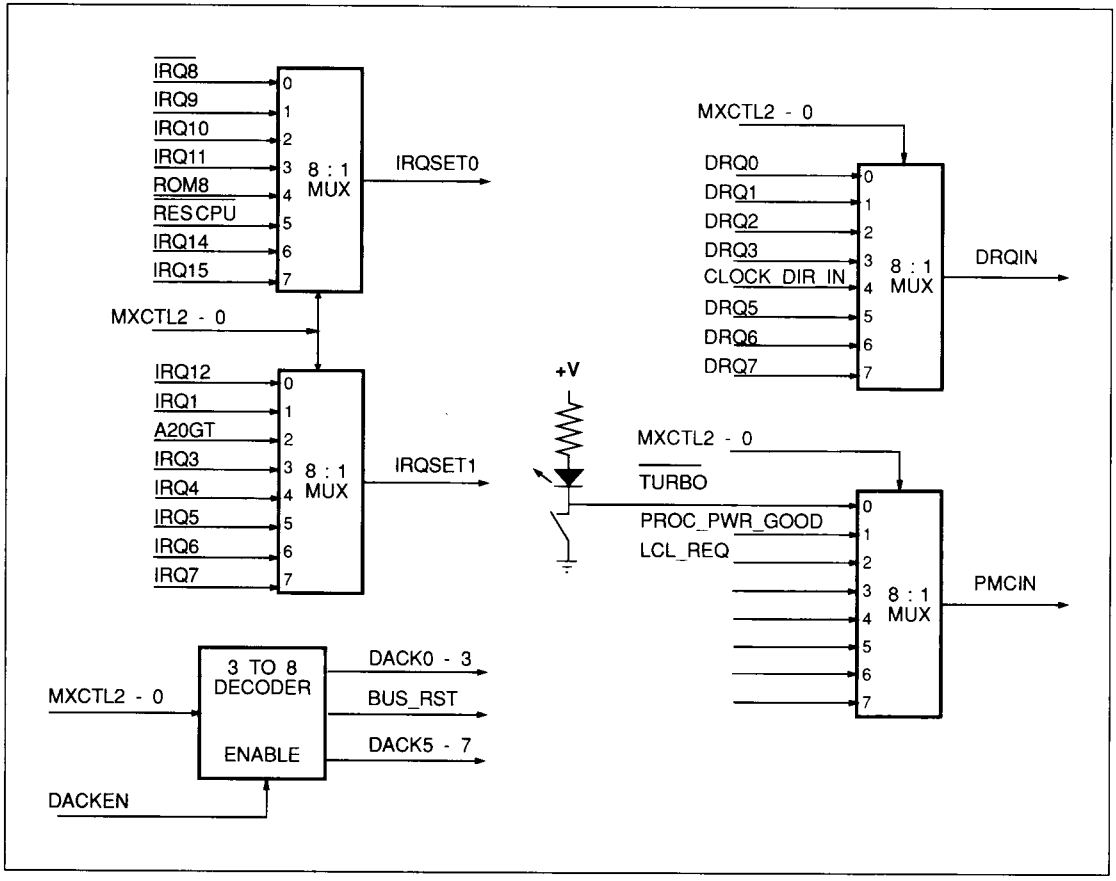


**FIGURE 5-1. MXCTL(2:0) MULTIPLEXING**

## 5.3 NUMERIC PROCESSOR

### 5.3.1 Numeric Processor Busy, Bus Timing, and Power Down Register

Port Address 1872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | PRO_ PD | FPD | | BUS_MOD | | BRQ_DEL | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| BAK_DEL | | WSI 16 | WSM 16 | WS18 | | WSM8 | |

| Signal Name | Default At RSTIN |
|---|---|
| PRO_PD | 0 |
| FPD | 0 |
| BUS_MOD | 00 |
| BRQ_DEL | 00 |
| BAK_DEL | 11 |
| WSI_16 | 0 |
| WSM_16 | 0 |
| WS18 | 10 |
| WSM8 | 10 |

**Bit 15 -** Ignored by the System Controller, may be 0 or 1.

**Bit 14 - PRO_PD,** Processor Power Down

When PRO_PD has been changed from zero to one, a power down sequence for the 80386SX processor is initiated at the next Halt State and the expansion bus continues to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD7855/LV to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from Port 7072H (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor are tristated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a Processor Power Good (PPG) signal. The PPG signal is sampled by bit 01 of the PMC Input Register at Port Address 8872H. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power.

PRO_PD = 1 -
Start processor power down sequence.

**Bit 13 - FPD,** Full Power-down

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and RA/ED bus are tristated and all inputs except RSTIN, CLK14 and PMC inputs are ignored. CAS before RAS refresh is performed if enabled by Port 2072H. All circuitry except the PMC and refresh timer logic is stopped and PMC output 7 (Full Power-down) from Port 7072H is set. This enables the powering down of all chips except DRAM, WD7855/LV, WD76C20, WD76C30 and WD90C2X Video Controller. The WD76C20 provides PDREF (a 64 KHz refresh signal on input pin 41) during the power-down mode. This signal is then gated by the System Controller to the REFRESH signal as an output on pin 98.

When a PMC interrupt occurs, PMC output 7 at Port 7072H is reset, enabling the power up sequence. A CPURES and BUS_RST (see Figure 5-1) are asserted until the PMCIN 01 PPG at Port 8872H input is high. The tristated outputs are restored and the inputs are no longer masked. Refer to Section 9.15 for more details regarding suspend and resume.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down.

FPD = 1 -
Full power down and in standby mode.

**Bit 12 -** Ignored by the System Controller, may be 0 or 1.

**Bits 11:10 - BUS_MOD,** Bus Mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be faster than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are not needed. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

- 0 0 - Bus logic uses BCLK2 divided by 2.
- 0 1 - Bus logic uses BCLK2 divided by 1.
- 1 0 - Bus logic uses CPUCLK divided by 2.
- 1 1 - Bus logic uses CPUCLK divided by 1.

**Bits 09:08 - BRQ_DEL,** Bus Request Delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

- 0 0 - 1 Bus clock delay
- 0 1 - .5 Bus clock delay
- 1 0 - No clock delay
- 1 1 - Reserved

**Bits 07:06 - BAK_DEL,** Bus Acknowledge Delay

The AT bus state machine has several options available for signaling the CPU control logic that an AT bus cycle has completed. The timing of this signal determines AT bus hold time for the data and address. Proper timing is determined by the CPU speed, AT bus speed and whether they are synchronous or asynchronous. The delay settings listed here are referenced to the trailing edge of the AT command strobe.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

- 0 0 - No delay
- 0 1 - -.5 Bus clock delay
- 1 0 - -1 Bus clock delay
- 1 1 - +.5 Bus clock delay

10

| CPU SPEED | AT BUS SPEED | AT BUS MODE | BUS_ MOD | BRQ_ DEL | BAK_ DEL |
|---|---|---|---|---|---|
| 33.3 MHz | 8 MHz | ASYNC | 0X | 01 | 11 |
| 25.0 MHz | 8 MHz | ASYNC | 0X | 01 | 00 |
| 20.0 MHz | 10 MHz | SYNC | 10 | 10 | 10 |
| 20.0 MHz | 8 MHz | ASYNC | 0X | 01 | 00 |
| 16.0 MHz | 8 MHz | SYNC | 10 | 10 | 10 |
| 12.5 MHz | 8 MHz | ASYNC | 0X | 01 | 10 |

**TABLE 5-2. BUS TIMING PARAMETERS**

**Bit 05 - WSI16,** Wait State for 16 bit I/0

WSI16 = 0 -
1 Bus clock wait state

WSI16 = 1 -
2 Bus clock wait state

**Bit 04 - WSM16,** Wait State for 16 bit Memory

WSM16 = 0 -
1 Bus clock wait state

WSM16 = 1 -
2 Bus clock wait state.

**Bits 03:02 - WSI8,** Wait State for 8 bit I/O

WSI8
03 02

0 0 - 2 Bus clock wait state.
0 1 - 3 Bus clock wait state.
1 0 - 4 Bus clock wait state
1 1 - 5 Bus clock wait state.

**Bits 01:00 - WSM8,** Wait State for 8 bit Memory

WSM8
01 00

0 0 - 2 Bus clock wait state.
0 1 - 3 Bus clock wait state.
1 0 - 4 Bus clock wait state
1 1 - 5 Bus clock wait state.

### 5.3.2 Numeric Processor Busy ($\overline{\text{NPBUSY}}$) Reset

Port Address 0F0H - Write only

Writing any data to this port resets the 80387SX busy signal (de-asserts $\overline{\text{NPBUSY}}$). The data is ignored.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Signal Name | Default At $\overline{\text{RSTIN}}$ |
|---|---|
| All signals | None |

### 5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1H - Write only

Writing any data to this port asserts NPRST and resets the 80387SX. The main processor is wait stated for 128 clocks when writing to this port. The data is ignored.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Signal Name | Default At $\overline{\text{RSTIN}}$ |
|---|---|
| All signals | None |

## 5.4 DMA CONTROL

The System Controller contains two DMA controllers. DMA Controller 1 is in the I/O address space from 000H to 00FH and is used for 8-bit transfers. DMA Controller 2 is in the I/O space from 0C0H to 0DEH and is used for 16-bit transfers. Channel 0 of DMA Controller 2 is used to cascade DMA controller #1. Table 5-4 identifies the Controller/-Channel location and function.

| AT Bus DMA Channel | DMA Controller | Transfer Type |
|---|---|---|
| 0 | #1 Channel 0 | 8-bit |
| 1 | #1 Channel 1 | 8-bit |
| 2 | #1 Channel 2 | 8-bit |
| 3 | #1 Channel 3 | 8-bit |
| 4 | #2 Channel 0 | Cascade DMA Cont. #1 |
| 5 | #2 Channel 1 | 16-bit |
| 6 | #2 Channel 2 | 16-bit |
| 7 | #2 Channel 3 | 16-bit |

**TABLE 5-3. DMA TRANSFER TYPES**

### 5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

**Demand Mode - 00**

In demand mode, a transfer continues to take place until DRQ is de-asserted or a Terminal Count (TC) is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

**Single Transfer Mode - 01**

In single transfer mode, the channel makes one transfer for each request. The word count is decremented, and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000H to FFFFH, a Terminal Count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

**Block Transfer Mode - 10**

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

**Cascade Mode - 11**

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tristated when the $\overline{MASTER}$ signal is asserted.

### 5.4.2 Transfer Types

There are three types of transfers: verify, write and read.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

**Verify - 00**

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or $\overline{MEMW}$ signals.

**Write - 01**

A write transfers data from an I/O device to memory.

**Read - 10**

A read transfers data from memory to an I/O device.

10

### 5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

### 5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority.

### 5.4.5 Extended Write

In normal timing, the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

### 5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A(23:16) (from the page register) and bits A(10:0) (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

### 5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

| 10-BIT MODE I/O ADDRESS IN HEX | 16-BIT MODE I/O ADDRESS IN HEX | READ/WRITE | DMA CONTROLLER | FUNCTION |
|---|---|---|---|---|
| 000 | 0000 | Read/Write | 1 | Channel 0 Address |
| 001 | 0001 | Read/Write | 1 | Channel 0 Word Count |
| 002 | 0002 | Read/Write | 1 | Channel 1 Address |
| 003 | 0003 | Read/Write | 1 | Channel 1 Word Count |
| 004 | 0004 | Read/Write | 1 | Channel 2 Address |
| 005 | 0005 | Read/Write | 1 | Channel 2 Word Count |
| 006 | 0006 | Read/Write | 1 | Channel 3 Address |
| 007 | 0007 | Read/Write | 1 | Channel 3 Word Count |
| 008 | 0008 | Read | 1 | Status |
| 008 | 0008 | Write | 1 | Command Register |
| 009 | 0009 | Write | 1 | Request Register |
| 00A | 000A | Write | 1 | Single Mask |
| 00B | 000B | Write | 1 | Mode Register |
| 00C | 000C | Write | 1 | Clear Pointer |
| 00D | 000D | Write | 1 | Master Clear |
| 00E | 000E | Write | 1 | Clear Mask |
| 00F | 000F | Write | 1 | Mask All |
| 080-09F | 0080-008F | | | DMA Page Register |
| 0C0 | 00C0 | Read/Write | 2 | Channel 0 Address |
| 0C2 | 00C2 | Read/Write | 2 | Channel 0 Word Count |
| 0C4 | 00C4 | Read/Write | 2 | Channel 1 Address |
| 0C6 | 00C6 | Read/Write | 2 | Channel 1 Word Count |
| 0C8 | 00C8 | Read/Write | 2 | Channel 2 Address |
| 0CA | 00CA | Read/Write | 2 | Channel 2 Word Count |
| 0CC | 00CC | Read/Write | 2 | Channel 3 Address |
| 0CE | 00CE | Read/Write | 2 | Channel 3 Word Count |
| 0D0 | 00D0 | Read | 2 | Status |
| 0D0 | 00D0 | Write | 2 | Command Register |
| 0D2 | 00D2 | Write | 2 | Request Register |
| 0D4 | 00D4 | Write | 2 | Single Mask |
| 0D6 | 00D6 | Write | 2 | Mode Register |
| 0D8 | 00D8 | Write | 2 | Clear Pointer |
| 0DA | 00DA | Write | 2 | Master Clear |
| 0DC | 00DC | Write | 2 | Clear Mask |
| 0DE | 00DE | Write | 2 | Mask All |
| B872 | B872 | Read | 1, 2 | DMA Mode Shadow |

**TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP**

### 5.4.8 Command Register

Port Addresses 008H, 0D0H - Write only

The Command Register is reset by $\overline{\text{RSTIN}}$ or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | EX_ WR | RO_ PRI | 0 | CO_ DIS | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 07:06 -** Not used, state is ignored

**Bit 05 - EX_WR,** Extended Write

**Bit 04 - RO_PRI**, Rotating Priority

**Bit 03** - Must be set to 0

**Bit 02 - CO_DIS**, Controller Disabled

**Bits 01:00 -** Not used, state is ignored

### 5.4.9 Status Register

Port Addresses 008H, 0D0H - Read only

Bits 03:00 are reset by $\overline{\text{RSTIN}}$, writing any data to Port Address 00DH or 0DAH (see section 5.4.14) or when read by a Status Read Command.

Channels 7:5 are accessed at Port Address 0D0H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 008H

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| CH3_ DRQ | CH2_ DRQ | CH1_ DRQ | CH0_ DRQ | CH3_ TC | CH2_ TC | CH1_ TC | CH0_ TC |

| Signal Name | Default At RSTIN |
|---|---|
| CH3_DRQ - CH0_DRQ | None |
| CH3_TC - CH0_TC | 0 |

**Bit 07 - CH3_DRQ**, Channel 3, 7 DRQ active

**Bit 06 - CH2_DRQ**, Channel 2, 6 DRQ active

**Bit 05 - CH1_DRQ**, Channel 1, 5 DRQ active

**Bit 04 - CH0_DRQ**, Channel 0 DRQ active

**Bit 03 - CH3_TC,** Channel 3, 7 has reached TC

**Bit 02 - CH2_TC**, Channel 2, 6 has reached TC

**Bit 01 - CH1_TC**, Channel 1, 5 has reached TC

**Bit 00 - CH0_TC**, Channel 0 has reached TC

### 5.4.10 Request Register

Port Addresses 009H, 0D2H - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by $\overline{\text{RSTIN}}$ or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

Channels 7:5 are accessed at Port Address 0D2H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 009H

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | CRQ | CH# | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 07:03** - Not used, state is ignored

**Bit 02 - CRQ**, Channel Requested

**Bits 01:00 - CH#**, Channel Number Requested

| CH# | 1 | 0 |
|---|---|---|
| | 0 | 0 - Channel 0 |
| | 0 | 1 - Channel 1, 5 |
| | 1 | 0 - Channel 2, 6 |
| | 1 | 1 - Channel 3, 7 |

### 5.4.11 Mask Registers

Each channel has a mask bit associated with it If it is set, the channel is disabled. The bits may be set or reset by software, or set by a Terminal Count (TC) if the channel is not in autoinitialize mode. All the bits are set by a $\overline{RSTIN}$, or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

#### 5.4.11.1 Single Mask Register

Port Addresses 00AH, 0D4H - Write only

Channels 7:5 are accessed at Port Address 0D4H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00AH

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | SE_ MA | CH# | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 1 |

**Bits 07:03 -** Not used, state is ignored

**Bit 02 - SE_MA**, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

**Bits 01:00 - CH#**, Channel Number Requested

CH# 1 0

0 0 - Channel 0
0 1 - Channel 1, 5
1 0 - Channel 2, 6
1 1 - Channel 3, 7

#### 5.4.11.2 Clear Mask Register

Port Addresses 00EH, 0DCH - Write only

Writing any data to these registers resets all Masks. The data is ignored.

Channels 7:5 are accessed at Port Address 0DCH
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00EH

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:00 -** Not used, state is ignored

#### 5.4.11.3 Mask Multiple Register

Port Addresses 00FH, 0DEH - Write only

Channels 7:5 are accessed at Port Address 0DEH
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00FH

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | CH3_ MA | CH2_ MA | CH1_ MA | CH0_ MA |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 1 |

**Bits 07:04 -** Not used, state is ignored

**Bit 03 - CH3_MA**, Channel 3, 7 Mask

**Bit 02 - CH2_MA**, Channel 2, 6 Mask

**Bit 01 - CH1_MA**, Channel 1, 5 Mask

**Bit 00 - CH0_MA**, Channel 0 Mask

10

### 5.4.12 Mode Register

Port Addresses 00BH, 0D6H - Write only

These registers are shadowed and may be read back through DMA Shadow Registers 1:3 described in sections 9.13.(1:3).

These registers select the mode and type of transfer for each channel. Refer to sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types and section 5.4.3 for a description of Autoinitialize.

Channels 7:5 are accessed at Port Address 0D6H
Channel 4 is not available
Channels 3:0 are accessed at Port Address 00BH

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| TRA_MOD | | AD_DEC | AUTO | TRA_TYP | | CHA#_SEL | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:06 - TRA_MOD**, Transfer Mode

TRA_MOD
7 6

0 0 - Demand
0 1 - Single
1 0 - Block
1 1 - Cascade

**Bit 05 - AD_DEC**, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

**Bit 04 - AUTO**, Autoinitialize

AUTO = 0
Autoinitialization is disabled.

AUTO = 1
Autoinitialization is enabled.

**Bits 03:02 - TRA_TYP**, Transfer Type

TRA_TYP
3 2

0 0 - Verify
0 1 - Write
1 0 - Read
1 1 - Not used

**Bits 01:00 - CHA#_SEL**, Channel Select

CHA#_SEL
1 0

0 0 - Channel 0
0 1 - Channel 1, 5
1 0 - Channel 2, 6
1 1 - Channel 3, 7

### 5.4.13 Clear Pointer Register

Port Addresses 00CH, 0D8H - Write only

Each DMA controller has a pointer flip-flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip-flop is reset, bits 7:0 are accessed, and when it is set, bits 15:8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register, or to Port Address 00DH or 0DAH (see section 5.4.14). In either case, the data is ignored.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:00 -** Not used, state is ignored

### 5.4.14 Master Clear Register

Port Addresses 00DH, 0DAH - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip-Flop

All data is ignored.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:00** - Not used, state is ignored

### 5.4.15 DMA Mode Shadow Register

Port Address B872H - Read only

This register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices. Refer to Section 2.8.1 and 9.14 for more information regarding the DMA Shadow registers.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| DMA1 MODE | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| DMA2 MODE | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| DMA1 MODE | 0 |
| DMA 2 MODE | 0 |

**Bits 15:08 - DMA1 MODE**

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00BH (see Table 5-4).

**Bits 07:00 - DMA 2 MODE**

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6H (see Table 5-4).

## 5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two interrupt controllers. Interrupt Controller 1 is in the I/O space of 020H to 021H and Interrupt Controller 2 is in the I/O space of 0A0H to 0A1H. Interrupt 2 of Interrupt Controller 1 is used to cascade Interrupt Controller 2.

### 5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may only be programmed to be edge sensitive. In this mode, the interrupt must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

| System Interrupt | Interrupt Controller | Use |
|---|---|---|
| 0 | #1 Level 0 | Timer |
| 1 | #1 Level 1 | Keyboard |
| 2 | #1 Level 2 | Cascade |
| 3:7 | #1 Level 3:7 | AT Bus |
| 8 | #2 Level 0 | RTC |
| 9:12 | #2 Level 1:4 | AT Bus |
| 13 | #2 Level 5 | Co-Processor |
| 14:15 | #2 Level 6:7 | AT Bus |

**TABLE 5-5. INTERRUPT SEQUENCE**

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2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

   **Fixed**

   In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

   **Automatic Rotation**

   In automatic rotation, the last interrupt serviced has the lowest priority.

   **Specific Rotation**

   In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA, causing the interrupt controller to send a vector to the CPU, set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's, Specific, Non-specific and Automatic.

   **Specific**

   An EOI is issued by software for a specific interrupt.

   **Non-Specific**

   A non-specific EOI is also issued by software. The hardware generates an EOI for the highest level active interrupt.

   **Automatic**

   An automatic EOI is a non-specific EOI that is caused by the second INTA.

   The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

   When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

| Interrupt Controller | Address Hex | Function | Read/Write |
|---|---|---|---|
| 1 | 020 | ICW1 | Write |
| 1 | 021 | ICW2 | Write |
| 1 | 021 | ICW3 | Write |
| 1 | 021 | ICW4 | Write |
| 1 | 021 | OCW1 | Write |
| 1 | 020 | OCW2 | Write |
| 1 | 020 | OCW3 | Write |
| 1 | 020 | IRR | Read |
| 1 | 020 | ISR | Read |
| 1 | 021 | Mask | Read |
| 1 | 020, 021 | Interrupt Level | Read |
| 2 | 0A0 | ICW1 | Write |
| 2 | 0A1 | ICW2 | Write |
| 2 | 0A1 | ICW3 | Write |
| 2 | 0A1 | ICW4 | Write |
| 2 | 0A1 | OCW1 | Write |
| 2 | 0A0 | OCW2 | Write |
| 2 | 0A0 | OCW3 | Write |
| 2 | 0A0 | IRR | Read |
| 2 | 0A0 | ISR | Read |
| 2 | 0A1 | Mask | Read |
| 2 | 0A0, 0A1 | Interrupt Level | Read |

**TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP**

### 5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are set up by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

#### 5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020H, 0A0H - Write only

Bit 4 of this register must be set to 1 or it will be interpreted as OCW2 or OCW3.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | S_S | L_T | | NC_M | ICW4 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:05 -** Not used, state is ignored

**Bit 04 - S_S,** Start Sequence

S_S Must be set to 1

**Bit 03 - L_T**, Level Trigger

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

L_T = 0 -
Edge Triggered Mode is selected.

L_T = 1 -
Level Triggered Mode is selected. EN_LVL (bit 00) in Port A872H must first be set to 1.

**Bit 02** - Not Used, state is ignored

**Bit 01 - N C_M,** Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

**Bit 00 - ICW4**, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

### 5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021H, 0A1H - Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 9.10.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| Interrupt Vector | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:03 - Interrupt Vector**

**Bits 02:00** - Not used, state is ignored

### 5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021H - Write only

This address accesses only Interrupt Controller 1.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | I2 H_L | 0 | 0 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:03** - Not used, must be set to 0

**Bit 02 - I2 H_L**, Interrupt 2 Has Slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

**Bits 01:00 -** Not used, must be set to 0

Port Addresses 0A1H - Write only

This address accesses only Interrupt Controller 2.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Slave ID | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:03** - Not used, must be set to 0

**Bits 02:00 - Slave ID**

#### 5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021H, 0A1H - Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 9.10.

A Slave does not have ICW4.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | SFNM | 0 | 0 | AUTEOI | 1 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:05 -** Not used, must be set to 0

**Bit 04 - S F N M**, Special Fully Nested Mode

S F N M = 0 -
Not Special Fully Nested Mode

S F N M = 1 -
Special Fully Nested Mode

**Bits 03:02 -** Not used, must be set to 0

**Bit 01 - AUT_EOI,** Auto End Of Interrupt

AUT_EOI = 0 -
Normal End Of Interrupt

AUT_EOI = 1 -
Automatic End Of Interrupt

**Bit 00 -** Not used, must be set to 1

### 5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

#### 5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021H, 0A1H - Write only

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| INT 7_M | INT 6_M | INT 5_M | INT 4_M | INT 3_M | INT 2_M | INT 1_M | INT 0_M |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bit 07** - Interrupt 7 Mask

**Bit 06** - Interrupt 6 Mask

**Bit 05** - Interrupt 5 Mask

**Bit 04** - Interrupt 4 Mask

**Bit 03** - Interrupt 3 Mask

**Bit 02** - Interrupt 2 Mask

**Bit 01** - Interrupt 1 Mask

**Bit 00** - Interrupt 0 Mask

#### 5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020H, 0A0H - Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 9.10.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| EOI_CONT | | | 0 | 0 | INT_LEV | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 07:05 - EOI_CONT**, End Of Interrupt

EOI_CONT
7 6 5

0 0 0 - Clear Rotate On Automatic EOI
0 0 1 - Non-specific EOI
0 1 0 - Not used
0 1 1 - Specific EOI
1 0 0 - Set Rotate on Automatic EOI
1 0 1 - Rotate on Non-Specific EOI
1 1 0 - Set Priority
1 1 1 - Rotate on Specific EOI

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**Bits 04:03** - Must be set to 0

**Bits 02:00 - INT_LEV,** Interrupt Level

To enable the setting of the interrupt level (INT_LEV), EOI_CONT must be set to 1 1 0 (Set Priority).

INT_LEV
2 1 0

0 0 0 - Interrupt Level 0

↕

1 1 1 - Interrupt Level 7

### 5.5.3.3 OCW3 - Operation Control Word 3

Port Address 020H, 0A0H - Write only

For Suspend/Resume or Hibernation operations this register may be read at Port Address D472H. Refer to Section 9.10.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| 0 | SMM | | 0 | 1 | P_C | IRR_ISR | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals . . . . . | None |

**Bit 07** - Must be set to 0

**Bits 06:05 - SMM**, Special Mask Mode

SMM
6 5

0 0 Not used
0 1 Not used
1 0 Reset Special Mask Mode
1 1 Set Special Mask Mode

**Bit 04** - Must be set to 0

**Bit 03** - Must be set to 1

**Bit 02 - P_C,** Poll Command

P_C = 0 -
No Poll Command

P_C = 1 -
Poll Command

**Bits 01:00 - IRR_ISR,** Interrupt Request Register and Interrupt Service Register

IRR_ISR
1 0

0 0 - Not used
0 1 - Not used
1 0 - Read Interrupt Request Register
1 1 - Read Interrupt Service Register

## 5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61H, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written, followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

| I/O Address | Use | Read/Write |
|---|---|---|
| 040H | Timer 0 Count/Status | Read/Write |
| 041H | Timer 1 Count/Status | Read/Write |
| 042H | Timer 2 Count/Status | Read/Write |
| 043H | Control Word | Write |

| Timer Channel | Use |
|---|---|
| 0 | Time of Day (Interrupt) |
| 1 | Refresh Request |
| 2 | Speaker |

| CONTROL WORD (FORMAT 1) - I/O Address 043H - Counter Latch Command | | | |
|---|---|---|---|
| 0 | BCD | | |
| 1-3 | Mode | 000 | Mode 0 |
| | | 001 | Mode 1 |
| | | X10 | Mode 2 |
| | | X11 | Mode 3 |
| | | 100 | Mode 4 |
| | | 101 | Mode 5 |
| 4-5 | Function | 00 | Counter Latch Command |
| | | 01 | Read/Write Low Byte |
| | | 10 | Read/Write High Byte |
| | | 11 | Read/Write Low Byte then High Byte |
| 6-7 | Counter | 00 | Counter 0 |
| | | 01 | Counter 1 |
| | | 10 | Counter 2 |
| **CONTROL WORD (FORMAT 2) - I/O Address 043H - Read Back Command** | | | |
| 0 | | 0 | |
| 1 | | Select Counter 0 | |
| 2 | | Select Counter 1 | |
| 3 | | Select Counter 2 | |
| 4 | | Latch Status | |
| 5 | | Latch Count | |
| 6-7 | | 11 | |

**TABLE 5-7. CONTROL WORD FORMAT**

### 5.6.1 Setup

Each counter may be set in one of six modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

#### 5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

#### 5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

#### 5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

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OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

#### 5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

#### 5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

#### 5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

### 5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1.) This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2.) This command is the equivalent of multiple Counter Latch Commands.

### 5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2.) Bits 0:5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

| STATUS WORD | |
|---|---|
| 0 | BCD |
| 1:3 | Mode |
| 4:5 | Function |
| 6 | New Count Written |
| 7 | Out Status |

### 5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the CPU.

### 5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

### 5.6.6 Timer Shadow

For both Suspend/Resume and Hibernation the state of the write only registers in the timer may be read. Refer to section 9.14.5 Timer Count for details.

## 5.7 SYSTEM CONTROLLER DECODE

The WD7855/LV supports both the 100% IBM-AT compatible I/O decoding (10-bit mode) and the newer IBM PS/2 compatible I/O decoding (16-bit mode). The mode is selected by EN_16 (bit 05) at Port Address 2872H. Refer to Section 8.2.

| Address | Decode |
|---|---|
| 0087H | DMA Channel 0 |
| 0083H | DMA Channel 1 |
| 0081H | DMA Channel 2 |
| 0082H | DMA Channel 3 |
| 008BH | DMA Channel 5 |
| 0089H | DMA Channel 6 |
| 008AH | DMA Channel 7 |
| 008FH | Refresh |

**TABLE 5-9. PAGE REGISTER DECODES**

**NOTE**

Page register data appears on address bits A(23:16) during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5:7), the LSB of the page register does not appear.

| DEVICE | 10-BIT MODE ADDRESS IN HEX | 16-BIT MODE ADDRESS IN HEX |
|---|---|---|
| DMA Controller 1 (Ch 0:3) | 000:01F | 0000:000F |
| Interrupt Controller Master | 020:03F | 0020:0021 |
| Timer | 040:05F | 0040:0043 |
| Port B - Parity Error And I/O Channel Check | 061:06F (odd) | 0061 |
| Real-Time Clock (Address) | 070 | 0070 |
| Real-Time Clock (Data) | 071 | 0071 |
| Page Register (except 092H) | 080:091<br>093:09F | 0080:008F |
| ALT 20 GATE, Hot Reset (Port 92H) | 092 | 0092 |
| Interrupt Controller Slave | 0A0:0BF | 00A0:00A1 |
| DMA Controller 2 (Ch 5:7) | 0C0:0DF | 00C0:00DE (even) |

**TABLE 5-8. DEVICE ADDESSES**

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## 5.8 NMI AND REAL TIME CLOCK

### 5.8.1 Real Time Clock Address Register

Port Address 070H in 10-bit mode
0070H in 16-bit mode.

- Write only

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| D_ NMI | RTC_ A6 | RTC_ A5 | RTC_ A4 | RTC_ A3 | RTC_ A2 | RTC_ A1 | RTC_ A0 |

| Signal Name | Default At RSTIN |
|---|---|
| D_NMI | 1 |
| RTC6 - RTC0 | None |

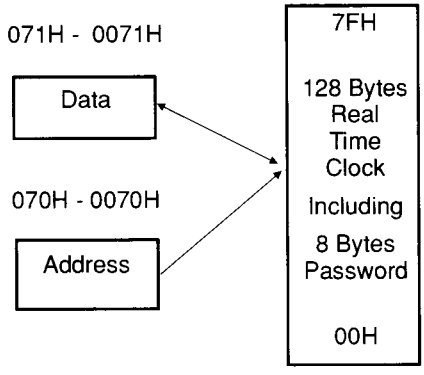
**Bit 07 - D_NMI**, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled.

D_NMI = 1 -
Non-Maskable Interrupt disabled

**Bits 06:00 - RTCA6 through RTCA0**, Real-Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real-Time Clock area. The data selected by one of these addresses is available by reading the RTC Data Register at 071H in 10-bit mode or 0071H in 16-bit mode.




### 5.8.2 Real-Time Clock Data Register

Port Address 071H in 10-bit mode
0071H in 16-bit mode.

- Read and Write

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at Port Address 2872H (refer to section 7.2).

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| Real-Time Clock Data | | | | | | | |

### 5.8.3 Lock Pass, Alternate A20G and Hot Reset

Port Address 092H in 10-bit mode
0092H in 16-bit mode

- Read and Write

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | LOCK PASS | | ALT_ A20G | HOT_ RST |

| Signal Name | Default At RSTIN |
|---|---|
| Bits 7:4, 2 | None |
| LOCK_PASS | 0 |
| ALT_A20G | 0 |
| HOT_RST | 0 |

**Bit 03 - LOCK_PASS**

LOCK_PASS is used to prevent access to the eight byte password located in the Real-Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at Port Address 2872H must be set to 0. Once LOCK_PASS is set, it can only be reset by RSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

**Bit 01 - ALT_A20G**, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872H to automatically change state to match that of the Keyboard's A20GATE.

**Bit 00 - HOT_RST**, Hot Reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

## 5.9 PORT B - PARITY ERROR AND I/O CHANNEL CHECK

Port B is accessed at any odd numbered Port Address 061H:06FH in 10-bit mode, or at 0061H in 16-bit mode. This provides access to parity error and I/O Channel Check of the expansion bus.

Bits 7:4 - Read only
Bits 3:0 - Read and Write

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PE | IOCK | OUT 2 | REF_ DT | D_ IOC | D_ PE | ENS PK | TMR 2G |

| Signal Name | Default At RSTIN |
|---|---|
| PE | 0 |
| IOCK | 0 |
| OUT2 | NA |
| REFDT | 1 |
| D_IOC | 0 |
| D_PE | 0 |
| ENSPK | 0 |
| TMR2G | 0 |

**Bit 07 - PE**, Parity Error

PE = 0 -
No Parity Error.

PE = 1 -
Parity Error.

**Bit 06 - IOCK**, I/O Channel Check from the expansion bus

IOCK = 0 -
No I/O Channel Check Error.

IOCK = 1 -
I/O Channel Check Error.

**Bit 05 - OUT2**, from timer channel 2

OUT2 represents the state of the Timer 2 output.

**Bit 04 - REF_DT**, Refresh Detect

Changes state on each refresh.

REF_DT is not affected by S_REF (bit 03 at Port Address BC72H.

**Bit 03 - D_IOC**, Disable I/O Channel Check

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

**Bit 02 - D_PE**, Disable Parity Error Check

D_PE = 0 -
Parity error checking not disabled. This may be overridden by PAR_DIS (bit 10 at Port Address 6072H) for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled.

**Bit 01 - ENSPK**, Enable Speaker

ENSPK = 0 -
Speaker is not enabled.

ENSPK = 1 -
Speaker is enabled.

**Bit 00 - TMR2G**, Gate for Timer Channel 2

TMR2G = 0 -
Timer Channel 2 gated low.

TMR2G = 1 -
Timer Channel 2 output enabled.

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# 6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

## 6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA11 through RA0. During I/O cycles, RA10 through RA08 (CS2:0 and DPH, DPL) are used to decode 32 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA11 through RA0 are capable of driving 350 pF at 5 volts or 220 pF at 3.3 volts. The equivalent load of two banks of 1-bit wide RAM, plus two banks of 4-bit wide RAM (48 DRAMs) are only capable of driving 350 pF at 5 volts.

The W/$\overline{R}$ signal at pin 2 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{MEMW}$ at pin 92 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128 Kbyte to 640 Kbyte, 256 Kbyte to 640 Kbyte and 512 Kbyte to 640 Kbyte.

When disabling any on-board DRAM, the register at Port Address 6872H must not be programmed to enable the on-board Lower EMS Page Frame.

All versions of the System Controller provide support for DRAM banks to be independent or two-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size.

## 6.2 MEMORY CONFIGURATION

### 6.2.1 Memory Control

Port Address 3872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| PG_CAS | ILV_7,5 | CA | | PG | ILV_6,4 | ILV_3,1 | ILV_2,0 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| EN_BNK7 | EN_BNK6 | EN_BNK5 | EN_BNK4 | SIZE BNK7:4 | | SIZE BNK3:0 | |

| Signal Name | Default At RSTIN |
|---|---|
| PG_CAS | 0 |
| ILV_7,5 | 0 |
| CA | 00 |
| PG | 0 |
| ILV_6:0 | 000 |
| EN_BNK7:4 | 0000 |
| SIZE_BNK7:0 | 0000 |

**Bit 15 - PG_CAS**, Page Mode CAS Width

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks.

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks.

**Bit 14 - ILV_7, 5**, Interleave Banks 7 and 5

ILV_7, 5 = 0 -
Banks 7 and 5 are not interleaved.

ILV_7, 5 = 1 -
Banks 7 and 5 are interleaved.

**Bits 13:12 - CA,** Cache Mode

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles.

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

0 0 - Cache Mode not enabled. Pin 121 may be used as the alternate clock CLKA.

0 1 - External Cache Mode or VLBI mode enabled.

1 0 - External Memory Controller. Pin 121 becomes PE and is connected to the parity error line of the external memory controller.

1 1 - Pin 121 may be used as the alternate clock CLKA. When $\overline{CAS}$ Input Mode is enabled, PE on pin 121 becomes an input and represents an error.

**Bit 11 - PG,** Page Mode

PG = 0 - Non-page mode
Word interleaving is employed when bank interleaving is enabled by an ILV. Non-page mode is **not** supported in 1 Mbit by 16 chips and 2 Mbits by 16 configurations.

PG = 1 - Page mode
The WD7855/LV operates in Page Mode regardless of the state of ILV, interleaving is performed when bank interleaving is enabled by ILV.

**Bit 10 - ILV_6, 4,** Interleave Banks 6 and 4

**Bit 09 - ILV_3, 1,** Interleave Banks 3 and 1

**Bit 08 - ILV_2, 0,** Interleave Banks 2 and 0

**Bit 07 - EN_BNK7,** Enable Bank 7

EN_BNK7 = 0 -
Bank 7 is disabled

EN_BNK7 = 1 -
Bank 7 is enabled

**Bit 06 - EN_BNK6,** Enable Bank 6

EN_BNK6 = 0 -
Bank 6 is disabled

EN_BNK6 = 1 -
Bank 6 is enabled

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**Bit 05 - EN_BNK5,** Enable Bank 5

EN_BNK5 = 0 -
Bank 5 is disabled

EN_BNK5 = 1 -
Bank 5 is enabled

**Bit 04 - EN_BNK4,** Enable Bank 4

EN_BNK4 = 0 -
Bank 4 is disabled

EN_BNK4 = 1 -
Bank 4 is enabled

**Bits 03:02 - SIZE_BNK7:4,** Size of Banks 7:4

Both versions of the System Controller support all DRAM sizes. Although the DRAM sizes within banks 7:4 must be the same, they may differ from those in banks 3:0. SIZE_BNK7:4 functions with bit 13 of DRAM Size and SMI RAM Register at Port 7472H.

**Port 7472H bit 13 = 0**

| SIZE_BNK7:4 03 02 | DRAM Type | RAS/CAS Matrix |
|---|---|---|
| 0 0 | 64 Kbit × 16 | 8 X 8 |
| 0 1 | 256 Kbit × 16 | 9 X 9 |
| 1 0 | 1 Mbit × 16 | 10 X 10 |
| 1 1 | 4 Mbit × 16 | 12 X 11 |

**Port 7472H bit 13 = 1**

| SIZE_BNK7:4 03 02 | DRAM Type | RAS/CAS Matrix |
|---|---|---|
| 0 0 | 512 Kbits x 16 | 10 X 9 |
| 0 1 | 1 Mbits x 16 | 12 X 8 |
| 1 0 | 2 Mbits x 16 | 11 X 10 |
| 1 1 | Reserved | Reserved |

**Bits 01:00 - SIZE_BNK3:0,** Size of Banks 3:0

Both versions of the System Controller support all DRAM sizes. Although the DRAM sizes within banks 3:0 must be the same, they may differ from those in banks 7:4. SIZE_BNK3:0 functions with bit 12 of DRAM Size and SMI RAM Register at Port 7472H.

**Port 7472H bit 12 = 0**

| SIZE_BNK3:0 01 00 | DRAM Type | RAS/CAS Matrix |
|---|---|---|
| 0 0 | 64 Kbit × 16 | 8 X 8 |
| 0 1 | 256 Kbit × 16 | 9 X 9 |
| 1 0 | 1 Mbit × 16 | 10 X 10 |
| 1 1 | 4 Mbit × 16 | 12 X 11 |

**Port 7472H bit 12 = 1**

| SIZE_BNK3:0 01 00 | DRAM Type | RAS/CAS Matrix |
|---|---|---|
| 0 0 | 512 Kbits x 16 | 10 X 9 |
| 0 1 | 1 Mbits x 16 | 12 X 8 |
| 1 0 | 2 Mbits x 16 | 11 X 10 |
| 1 1 | Reserved | Reserved |

### 6.2.2 Memory Bank 7 Through Bank 0 Starting Address

Port Address 4872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 1 Start Address | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 0 Start Address | | | | | | | |

Port Address 5072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 3 Start Address | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 2 Start Address | | | | | | | |

Port Address 2C72H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 5 Start Address | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 4 Start Address | | | | | | | |

Port Address 3472H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 7 Start Address | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| Bank 6 Start Address | | | | | | | |

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave. For example, if bank 0 has 1 Mbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes. For three banks of the same size, in which two are interleaved, the two interleaved banks must be placed at a lower starting address than the third bank.

| RAM SIZE | PAGE SIZE | BANK SIZE |
|---|---|---|
| 64 Kbits x 16 | 512 Bytes | 128 Kbytes |
| 256 Kbits x 16 | 1024 Bytes | 512 Kbytes |
| 1 Mbits x 16 | 2048 Bytes | 2048 Kbytes |
| 4 Mbits x 16 | 4096 Bytes | 8192 Kbytes |
| 512 Kbits x 16 | 1024 Bytes | 1024 Kbytes |
| 1 Mbit x 16 chips | 512 Bytes | 2048 Kbytes |
| 2 Mbits x 16 | 2048 Bytes | 4096 Kbytes |

### 6.2.3 Split Starting Address

Port Address 5872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| EN_ BNK3 | EN_ BNK2 | EN_ BNK1 | EN_ BNK0 | DRAM_DRV | | SPLIT_SIZE | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A22 | A21 | A20 | A19 | | |
| Split Starting Address | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| EN_BNK3 | 0 |
| EN_BNK2 | 0 |
| EN_BNK1 | 0 |
| EN_BNK0 | 0 |
| DRAM_DRV | 00 |
| SPLIT_SIZE | 00 |
| Bits 01, 00 | None |

**Bit 15 - EN_BNK3,** Enable Bank 3

EN_BNK3 = 0 -
Bank 3 is disabled

EN_BNK3 = 1 -
Bank 3 is enabled

**Bit 14 - EN_BNK2,** Enable Bank 2

EN_BNK2 = 0 -
Bank 2 is disabled

EN_BNK2 = 1 -
Bank 2 is enabled

**Bit 13 - EN_BNK1,** Enable Bank 1

EN_BNK1 = 0 -
Bank 1 is disabled

EN_BNK1 = 1 -
Bank 1 is enabled

**Bit 12 - EN_BNK0,** Enable Bank 0

EN_BNK0 = 0 -
Bank 0 is disabled

EN_BNK0 = 1 -
Bank 0 is enabled

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**Bits 11:10 - DRAM_DRV,** DRAM Driver Strength

Typically, 33 ohm series resistors are used on the DRAM address lines RAD(10:0) to reduce the bouncing, overshoot and undershoot. These registers are not required with the WD7855/LV and, when used, the setup time of the column address to CAS assertion is marginal.

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot are minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage and manufacturing process.

The proper setting of DRAM_DRV is dependent upon several factors: Total load capacitance of installed DRAMs, trace lengths, bouncing, overshoot, undershoot and number of DRAM banks installed. Typically when one bank is installed, medium strength is selected. Two banks require high strength. Three or four banks require full strength.

**NOTE**

33 MHz or 3.3 volt designs require full strength (DRAM_DRV = 0 0).

DRAM_DRV
11 10

- 0 0 - Full strength DRAM address drive, up to 350 pF
- 0 1 - Low strength DRAM address drive, up to 100 pF
- 1 0 - Medium strength DRAM address drive, up to 180 pF
- 1 1 - High strength DRAM address drive, up to 260 pF

**Bits 09:08 - SP SIZE,** Split Size

The split is implemented by moving the block of memory between 0A0000H through 0FFFFFH to another area. The destination area must start on a 512 Kbyte boundary. If BIOS is to be shadowed, the split size must be 320 Kbyte for a 64 Kbyte shadow or 256 Kbyte for a 128 Kbyte shadow, and the RAM Shadow and Write Protect Register (Port 6072H) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000H (640 Kbyte) to 100000H (1024 Kbyte) is available for remapping. The remapping may start at 100000H, providing 384 Kbyte of extended memory, or may start at 0F0000H to allow BIOS shadowing, with 320 Kbyte of extended memory. Only a single bank may be split. The bank to be split must be at least 512 Kbyte or larger.

SPLIT SIZE
09 08

- 0 0 - No split
- 0 1 - 256 Kbyte split, memory moved from 0A0000H to 0DFFFFH
- 1 0 - 320 Kbyte split, memory moved from 0A0000H to 0EFFFFH
- 1 1 - 384 Kbyte split, memory moved from 0A0000H to 0FFFFFH

**Bits 07:02 - A24:A19,** Split Starting Address

**Bits 01:00 -** Not used, state is ignored

**PROGRAMMING NOTE**

BIOS Shadow requires that a split size of either 256K or 320K be allocated. The split starting address must also be programmed. This means that there must be a split or BIOS cannot be shadowed.

For a system with a full 32M of memory, this presents some unique issues. As stated previously, shadow BIOS requires both a split and split starting address. In a system with 32M of memory there is no empty area in which to assign the split starting address. There are two options: Do not shadow the BIOS in a full 32M system (i.e. assign no split), or shadow the BIOS by assigning the starting address to just below the 32M boundary (i.e. for a 64K shadow, start 320K below the 32M boundary, for a 128K shadow, start 256K below the 32M boundary.) Furthermore, to avoid conflict with the memory already at this location, program the high memory write boundary (C072H bits 07:00) to the same value as the split starting address to write protect this area. Also enable the high memory write protect (6072H bit 13). This effectively disables the top 320K or 256K of memory.

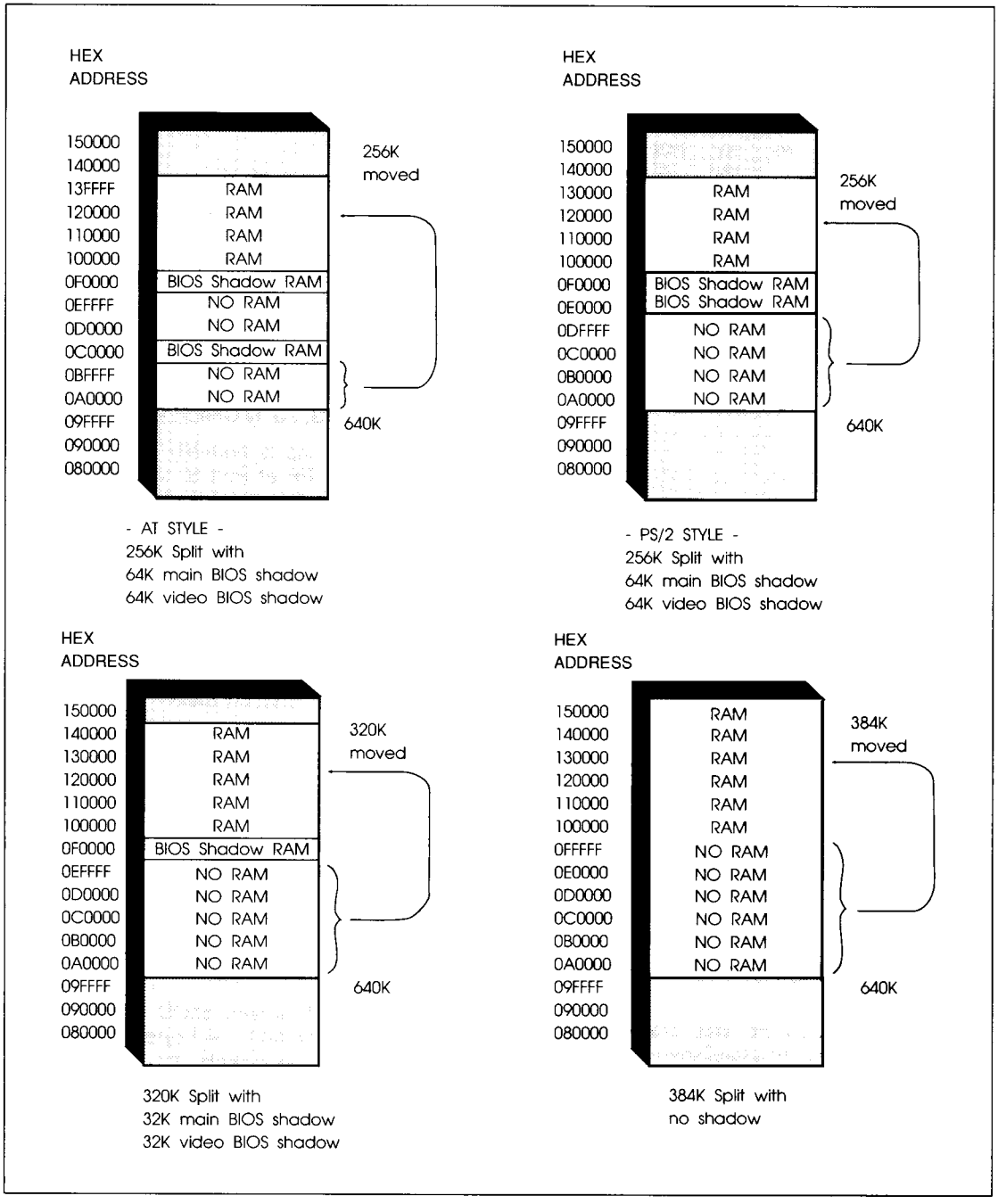


**FIGURE 6-1. SPLIT SIZE**

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### 6.2.4 RAM Shadow and Write Protect

Port Address 6072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| DIS_MEM | | HM_ WP | WP | INV_ PAR | PAR_ DIS | SHD | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| X_ MEM | ERS PWS | VB_SIZ | | ROM_TYP | | BL_MOU | |

| Signal Name | Default At RSTIN |
|---|---|
| DIS_MEM | 00 |
| HM_WP | 0 |
| WP | 0 |
| INV_PAR | 0 |
| PAR_DIS | 0 |
| SHD | 00 |
| ERSPWS | 0 |
| X_MEM | 0 |
| Bit 06 | 0 |
| VB_SIZ | 00 |
| ROM_TYP | 00 |
| BL_MOU | 00 |

**Bits 15:14 - DIS_MEM,** Disable On-board Memory

DIS_MEM
15 14

0 0 - On-board memory from 128 KB to 640 KB not disabled.

0 1 - On-board memory from 512 KB to 640 KB disabled.

1 0 - On-board memory from 256 KB to 640 KB disabled.

1 1 - On-board memory from 128 KB to 640 KB disabled.

**Bit 13 - HM_WP,** High Memory Write Protect Enable

This bit enables the write protection for the memory boundary established by the register at Port C072H.

HM_WP = 0 -
High memory write protect not enabled.

HM_WP = 1 -
High memory write protect enabled.

**Bit 12 - WP,** Shadowed BIOS Write Protect Enable

WP = 0 -
Write protect for shadowed BIOS not enabled.

WP = 1 -
Write protect for shadowed BIOS enabled.

**Bit 11 - INV_PAR,** Invert Parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM.

INV_PAR = 1 -
Invert parity when writing to on-board DRAM.

**Bit 10 - PAR_DIS,** Parity Checking Disabled

Parity checking is normally enabled or disabled by D_PE at Port B (see Section 5.9). Setting PAR_DIS overrides the D_PE setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by D_PE.

PAR_DIS = 1 -
Parity checking disabled.

**Bits 09:08 - SHD,** Shadow BIOS

Before the BIOS can be shadowed, the SPLIT_SIZE field in the Split Starting Address Register at Port 5872H must be programmed to non-zero.

ROM at FE0000H - FFFFFFH, the top of 16 MByte address space is never shadowed.

Option SHD 11 should be used when Video Remap Function is desired (i.e. Video BIOS in the lower half of EPROM shows up at C0000H).

64 Kbyte of system BIOS at 0F0000H - 0FFFFFH, and up to 64 Kbyte of video BIOS at 0C0000H - 0CFFFFH, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000H - 0FFFFFH. When SHD is set to 11, the video BIOS appears at 0C0000H - 0CFFFFH rather than 0E0000H - 0EFFFFH.

The video shadow size at 0C0000H - 0CFFFFH is determined by VB_SIZ, the video BIOS size field.

SHD
09 08

☆ 0 0 - No BIOS shadowing, allows 384 KB remap.

0 1 - 64 KB system BIOS shadow, 0F0000H - 0FFFFFH, allows 320 KB remap.

1 0 - 128 KB system BIOS shadow, 0E0000H - 0FFFFFH, allows 256 KB remap.

☆ 1 1 - 64 KB system BIOS shadow, 0F0000 - 0FFFFF and video BIOS shadow, allows 256 KB remap.

☆ See note following bits 01, 00.

**Bit 07 - X_MEM,** Shadow BIOS for Read/Write Memory

When SHD (bits 09 and 08) equals 11, X_MEM provides the means of using RAM from E8000H through EFFFFH not being used for video BIOS shadowing, to be used as read/write memory.

X_MEM = 0 - SHD = 11
ROM_TYP = 10 - VB_SIZ = 01

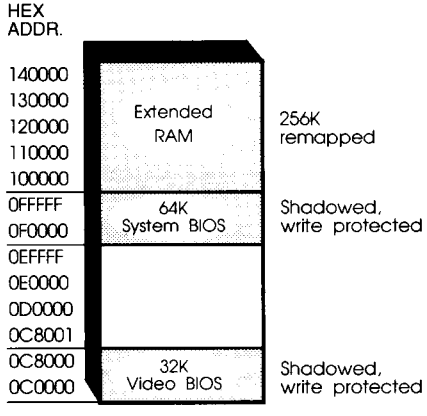


**FIGURE 6-2. X_MEM = 0**

X_MEM = 1 - SHD = 11
ROM_TYP = 10 - VB_SIZE = 01

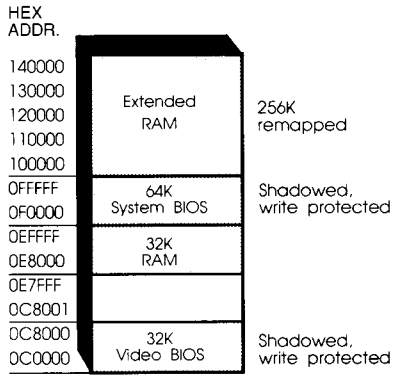


**FIGURE 6-3. X_MEM = 1**

**Bit 06 - ERPWS**, Extra RAS Precharge Wait State

ERPWS should be set to 1 when using slow DRAMs with a fast CPU clock rate. For example: 120 ns. DRAMs at 25 MHz. This should be used in conjunction with X_WS, bit 02 at Port Address B472H

ERPWS = 0 -
Extra RAS Precharge Wait State not enabled.

ERPWS = 1 -
Extra RAS Precharge Wait State enabled. Two CLK2s are added to increase the RAS precharge time in page mode.

**Bits 05:04 - VB_SIZ,** Video BIOS Size

VB_SIZ ☆
05 04

0 0 - 16 KB video BIOS

0 1 - 32 KB video BIOS

1 0 - 48 KB video BIOS

1 1 - 64 KB video BIOS

☆ See note following bits 01, 00.

**Bits 03:02 - ROM_TYP,** ROM Type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000H - 0FFFFFH or FE0000H - FFFFFFH.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000H - 0FFFFFH or FF0000H - FFFFFFH.

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For ROM type 10, CSPROM is asserted when the address is 0F0000H - 0FFFFFH, FF0000H - FFFFFFH or 0C0000H - 0CXFFFH where X is determined by VB_SIZ. This allows either a 128 Kbyte BIOS with a 64 Kbyte system BIOS and a 64 Kbyte video BIOS, or a 64 Kbyte BIOS with a 32 Kbyte system BIOS and a 32 Kbyte video BIOS. The 32 Kbyte video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000H - CX000H and F0000H - FX000H. A 64 Kbyte EPROM needs addresses SA15 through SA0. A 128 Kbyte EPROM needs addresses SA16 through SA0. Neither EPROM needs translated addresses.

$\overline{\text{CSPROM}}$ is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

- 0 0 - 128 KB system BIOS, located at E0000H - FFFFFH
- 0 1 - 64 KB system BIOS, located at F0000H - FFFFFH
- ☆ 1 0 - 64 KB or 128 KB shared BIOS System BIOS located at F0000H - FFFFFH, video BIOS located at C0000H - CX000H
- 1 1 - Reserved

☆ See note following bits 01, 00.

**Bits 01:00 - BL_MOU**, Backlight Mouse Control

Enabling the Backlight Mouse Control increases the CPU speed for one second if Auto Clock Switching is on. The AUT_FST bit is located at Port 1072H bit 11. Enabling the Backlight Mouse Control also affects the Back/light and LCD timers in the PMC Timer Register at Port Address 8072H.

BL_MOU
01 00

- 0 0 - No mouse control
- 0 1 - INT12 mouse
- 1 0 - INT4 mouse
- 1 1 - INT3 mouse

☆ **NOTE**

When SHD = 11 and X_MEM = 0, or SHD = 00 and ROM_TYP = 10, the portion of 0E0000H DRAM memory that is not mapped to 0C0000H (as determined by VB_SIZ) is not accessible. Once a portion of 0E0000H segment is mapped to 0C0000H, all 0E0000H accesses go to the expansion bus without generation of $\overline{\text{CSPROM}}$. This allows AT bus plug-in boards and/or drivers to access the E0000H segment.

### 6.2.5 High Memory Write Protect Boundary

Port Address C072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A24 | A23 | A2 | A21 | A20 | A19 | A18 | A17 |
| Boundary Address | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| Bits 15:08 | None |
| A24:17 | 00 |

**Bits 15:08** - Not used, state is ignored

**Bits 07:00 - A24:17**, Boundary Address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at Port 6072H. This provides an additional write protect region for disk caching.

### 6.2.6 DRAM Size and SMI RAM Register

Port Address 7472H - Read and Write

This register is used to set up the starting address of the SMI DRAM and support extra DRAM types.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | DRAM Type | | | SMI_ A24 | HS_R PD | SMI_R ENB |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A23 | A22 | A21 | SMI_RAM A20 | A19 | A18 | A17 | A16 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 15:14 -** Must be set to 0

**Bits 13:12 - DRAM Type**

These bits are used with Bits 3:0 of Register 3872H to determine the DRAM size of Banks 7:0.

Bit 13 is used with bits 03, 02 of 3872H for Banks 7:4.
Bit 12 is used with bits 01, 00 of 3872H for Banks 3:0.

*See Section 6.2.1, Memory Configuration.*

**Bit 11**, Reserved

**Bit 10 - SMI_A24**, SMI RAM Address bit 24

SMI_A24 is used in conjunction with bits 7:0 (SMI_RAM starting address A23:16) when SMI RAM is located above 16 Mbyte.

**Bit 09 - HSRPD,** Holdoff SMI When Reset Pending Disable

When HSRPD is set to 0, all SMI sources except I/O traps, are held off whenever a reset-pending condition is detected. The sources remain active internally but do not cause the SMI output to be asserted until the reset-pending condition is cleared.

When HSRPD is set to a 1, the reset pending condition does not gate off the assertion of SMI. Reset pending is defined as: (1) Port 92H reset pending, (2) KB controller ports 60H or 64H have been written within the last 14 µs or (3) the CPU is in a halt state.

HSRPD = 0 -
SMI is held off when reset is pending

HSRPD = 1 -
SMI is not held off

**Bit 08 - SMI_R ENB**, SMI RAM Enable

Setting SMI_R ENB enables the SMI RAM remapping and protection. The system BIOS should load the SMI service routine into the SMI RAM before setting this bit.

SMI_R ENB = 0 -
SMI RAM disable

SMI_R ENB = 1 -
SMI RAM enable

**Bits 07:00 - SMI_RAM,** SMI RAM Starting Address

SMI_RAM determine the physical location of the SMI DRAM. These are also used to read/write protect the SMI RAM when the SMI RAM Enable bit is set.

## 6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of $\overline{MEMR}$ and $\overline{MEMW}$. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at Port 4072H, the memory timing mode changes immediately. The code that programs this register should be in ROM and not shadowed in RAM. This register only applies to Non-Page Mode operation and has no effect on Page Mode operations. This allows Power Management code to use this register as a scratch pad during Page Mode operations.

Except for optional extra wait states and/or extra RAS precharge timing, Page Mode timing is not programmable. Refer to registers at Port Address B472H bit 02, A872H bit 01 and 6072H bit 06 for details.

### 6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | NP_MODE | | NP_ RAW | NP_WCAS | | NP_RCAS | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | NP_RAS_ HLD | | NP_PWE | | | NP_WS | |

| Signal Name | Default At RSTIN |
|---|---|
| Bits 15, 07 | None |
| NP_MODE | 00 |
| NP_RAW | 0 |
| NP_WCAS | 00 |
| NP_RCAS | 00 |
| NP_RAS_HLD | 00 |
| NP_PWE | 000 |
| NP_WS | 00 |

**Bit 15 -** Not used, state is ignored

**Bits 14:13 - NP_MODE**, Non-Page Mode

There are two non-page modes available, Mode-00 and Mode-01. Mode-00 provides one processor clock of row address hold time and is used for 1, 2 or 3 wait state memory cycles. Mode-01 provides a half processor clock of row address hold time and is used for 0 wait state memory cycles. Because the memory timing may be adjusted in increments of half a processor clock, Mode-00 is suited for all DRAM and processor speeds.

Mode-01 provides a half processor clock row address hold time, which is usually sufficient for system speeds of 12.5 MHz and slower. This compressed timing allows zero wait state operation.

Table 6-1 shows typically required DRAM speeds and register programming values for various processor speeds. Because DRAM timing varies among manufacturers, the required DRAM speed may differ from those listed in the table.

NP_MODE
14 13

0 0 - Minimum 1 wait state.
0 1 - Minimum 0 wait state.

| PROCESSOR SPEED | NP_ MODE | DRAM SPEED | WAIT STATES | REGISTER 4072H |
|---|---|---|---|---|
| 16.0 MHz | 01 | 53 ns | 0 | 3560H |
| 16.0 MHz | 00 | 80 ns | 1 | 1025H |
| 20.0 MHz | 00 | 80 ns | 1 | 1025H |
| 20.0 MHz | 00 | 100 ns | 2 | 107AH |
| 25.0 MHz | 00 | 80 ns | 2 | 107AH |

**TABLE 6-1. TYPICAL DRAM SPEEDS**

**Bit 12 - NP_RAW**, Non-page disable Read After Write

EMS accesses and interleave miss cycles (I/O cycle to device on RAD) may add one additional wait state.

NP_RAW = 0 -
Memory read cycles immediately following a write cycle causes an automatic wait state to be added before initiating the read cycle.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

**Bits 11:10 - NP_WCAS,** Non-page Write CAS Delay

NP_WCAS
11 10

0 0 - CAS write delay 1.0 CLK2
0 1 - CAS write delay 1.5 CLK2
1 0 - CAS write delay 2.0 CLK2
1 1 - CAS write delay 2.5 CLK2

**Bits 09:08 - NP_RCAS**, Non-page Read CAS Delay

NP_RCAS
09 08

0 0 - CAS read delay 1.0 CLK2
0 1 - CAS read delay 1.5 CLK2
1 0 - CAS read delay 2.0 CLK2
1 1 - CAS read delay 2.5 CLK2

**Bit 07 -** Not used, state is ignored

**Bits 06:05 - NP_RAS_HLD,** Non-page CAS to RAS Hold Time

The RAS active delay is reduced by half a clock during writes if NP_WCAS is set to 1X, or during reads if NP_RCAS is set to 1X.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS.
0 1 - RAS active until 1.5 clock after CAS.
1 0 - RAS active until 2.0 clock after CAS.
1 1 - RAS active until 2.5 clock after CAS.

**Bits 04:02 - NP_PWE,** Non-page CAS Pulse Width Extension

The pulse width is reduced by half a clock during writes if NP_WCAS is set to X1, or during reads if NP_RCAS is set to 1X.

NP_PWE
04 03 02

0 0 0 - No extension (2 CLK2 norm.)
0 0 1 - Extended by 0.5 CLK2
0 1 0 - Extended by 1.0 CLK2
0 1 1 - Extended by 1.5 CLK2
1 0 0 - Extended by 2.0 CLK2
1 0 1 - Extended by 2.5 CLK2
1 1 0 - Extended by 3.0 CLK2
1 1 1 - Extended by 3.5 CLK2

**Bits 01:00 - NP_WS,** Non-page Wait States

NP_WS makes it possible to unconditionally add wait states to all DRAM cycles. Conditional wait states may be added to read after write cycles, EMS accesses and interleave miss cycles, with NP_RAW (bit 12).

NP_WS
01 00

0 0 - No wait states added
0 1 - 1 Wait state added
1 0 - 2 Wait states added
1 1 - 3 Wait states added

10

| TIMING | NUMBER OF CLK2'S | |
|---|---|---|
| | MODE-00 | MODE-01 |
| Row address to RAS | 2 | 2 |
| RAS width | 3 + NPH + NPHB / 2 | 1 + NPH + NPHB / 2 |
| Row address hold | 1 | 0.5 |
| Column address setup (read) | 1 + NPRF / 2 | 0.5 + NPRF / 2 |
| Column address setup (write) | 1 + NPWF / 2 | 1 + NPWF / 2 |
| RAS hold (read from CAS) | 1 + NPHB / 2 - NPRF / 2 + NPH | 0.5 - NPRF / 2 + NPH |
| RAS hold (write) | 1 + NPHB / 2 - NPWF / 2 + NPH | 0.5 - NPWF / 2 + NPH |
| CAS width (read) | ① + NPCAS + NPCB / 2 - NPRF / 2 | ① + NPCAS + NPCB / 2 - NPRF / 2 |
| CAS width (write) | ① + NPCAS + NPCB / 2 - NPWF / 2 | ① + NPCAS + NPCB / 2 - NPWF / 2 |
| RAS precharge | 2 × (2 + NP_WS) - RAS width | 2 × (2 + NP_WS) - RAS width |
| Column address hold | 1 - NPCB / 2 | 1 - NPCB / 2 |

① 2 if NPCAS = 0 or 1
1 if NPCAS = 2 or 3

NPWF = Bit 10 NPRF = Bit 08 NPH = Bit 06 NPHB = Bit 05
NPCAS = Bits 04, 03 NPCB = Bit 02 NP_WS = Bits 01, 00

**TABLE 6-2. NON-PAGE MODE TIMING**

### 6.3.2 Page Mode

Table 6-3 identifies the type of DRAM cycle and number of wait states for the 80386SX processor.

| | PAGE MODE DRAM CYCLE | WAIT STATES |
|---|---|---|
| 80386SX | Write page hit, pipeline mode | 0 |
| | Write page hit, non-pipeline mode | 1 |
| | Write page first access, pipeline mode ☆ | 1 |
| | Write page miss, pipeline mode | 2 |
| | Write page miss, non-pipeline mode | 3 |
| | Write page miss, pipeline extra RAS precharge | 3 |
| | Write page miss, non-pipeline extra RAS precharge | 4 |
| | Read page hit, pipeline mode | 0 |
| | Read page hit, non-pipeline mode | 1 |
| | Read after write page hit, pipeline mode ☆ | 1 |
| | Read page first access non-pipeline mode ☆ | 3 |
| | Read page miss, pipeline mode | 3 |
| | Read page miss, non-pipeline mode | 4 |
| | Read page miss, pipeline extra RAS precharge | 4 |
| | Read page miss, non-pipeline extra RAS precharge | 5 |
| 80386SX With Discrete Cache | Write page hit | 0 |
| | Write page first access ☆ | 1 |
| | Write page miss | 2 |
| | Read cache hit | 0 |
| | Read cache miss, page hit | 1 |
| | Read cache miss, page first access ☆ | 3 |
| | Read cache miss, page miss | 4 |

☆ Equal Bank sizes, non-EMS cycle

First access is a page mode memory cycle which immediately follows a refresh, DMA or master cycle. It is not necessary for the DRAMs to be precharged for a first access cycle, since all $\overline{RAS}$ signals have been high in the previous cycle. This shortens a first access page mode cycle by one wait state. For example, a read page miss, non-pipeline mode in 80386SX mode is four wait states. A read page miss, non-pipeline mode, first access in 80386SX mode is three wait states. All installed DRAMs must be the same size and configuration and the memory cycle cannot be an EMS cycle for a first access to occur.

**TABLE 6-3. PAGE MODE WAIT STATES**

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### 6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64 Kbyte, 256 Kbyte, 1 Mbyte or 4 Mbyte SIMM memory modules.

| | RA11 | RA10 | RA9 | RA8 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **64 KBITS NON-INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **64 KBITS 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **256K 2-WAY INTERLEAVE, 1MBITS NON-INTERLEAVE OR 512 KBITS X 8 2-WAY INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A19 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **1 MBITS 2-WAY INTERLEAVE, OR 4 MBITS NON-INTERLEAVE** | | | | | | | | | | | |
| ROW | A11 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A21 | A19 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **4 MBITS 2-WAY INTERLEAVE** | | | | | | | | | | | |
| ROW | A11 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A23 | A21 | A19 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **512K X 8 DRAM: NON-INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A22 | A19 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **1M X 16 DRAM: NON-INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A9 | A19 | A18 | A16 | A15 | A14 | A20 | A12 | A11 | A10 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **1M X 16 DRAM: 2-WAY INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A10 | A21 | A18 | A16 | A15 | A14 | A20 | A12 | A11 | A19 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **2M X 8 DRAM: NON-INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A21 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A19 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **2M X 8 DRAM: 2-WAY INTERLEAVE** | | | | | | | | | | | |
| ROW | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A21 | A19 | A17 |
| COL | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
| | **REFRESH ADDRESS** | | | | | | | | | | | |
| ROW | | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**TABLE 6-4. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION**

| | RA11 | RA10 | RA9 | RA8 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ROW | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | ALL |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | 64 Kb |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A17 | 256 Kb |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A11 | A19 | A17 | 1 Mb or 512 Kb x 8 |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A13 | A12 | A21 | A19 | A17 | 4 Mb |

**NOTE:** 1M X 16 or 18 and 2M X 8 or 9 are not supported.

**TABLE 6-5. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION**

| | RA11 | RA10 | RA9 | RA8 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ROW | A13 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A13 | ALL |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A17 | A12 | A11 | A10 | A9 | 64 Kb |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A19 | A12 | A11 | A10 | A17 | 256 Kb |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A21 | A12 | A11 | A19 | A17 | 1 Mb or 512 Kb x 8 |
| COL | A13 | A22 | A20 | A18 | A16 | A15 | A14 | A12 | A23 | A21 | A19 | A17 | 4 Mb |

**NOTE:** 1M X 16 or 18 and 2M X 8 or 9 are not supported.

**TABLE 6-6. NON-PAGE, 2-WAY INTERLEAVE ADDRESS CONFIGURATION**

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## 6.4 EMS

### 6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| INC | PF_LOC | | | EMS_EN | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| EN_ RES | A23 | A22 | A21 | A20 | A19 | A18 | A17 |
| | Lower_EMS_Boundary | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| INC | 0 |
| PF_LOC | 00 |
| Bits 12, 09, 08 | None |
| EMS_EN | 00 |
| EN_RES | 0 |
| A23-A17 | 0 |

**Bit 15 - INC,** Increment EMS Pointer

INC controls whether or not the EMS Pointer at Port E072H is to be incremented after each read or write of the EMS Page Register at Port E872H.

INC = 0 -
The EMS pointer does not increment.

INC = 1 -
EMS pointer increments after access to EMS Page Register.

**Bits 14:13 - PF_LOC,** Upper Page Frame Location

PF_LOC determines the starting location of a block eight frames. See Table 6-7 for the upper page frame assignments.

PF_LOC
14 13

- 0 0 - Upper page frame starts at C4000H
- 0 1 - Upper page frame starts at C8000H
- 1 0 - Upper page frame starts at CC000H
- 1 1 - Upper page frame starts at D0000H

**Bit 12 -** Not used, state is ignored

**Bits 11:10 - EMS_EN,** EMS Enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-7 and 6-8 show the upper and lower page frame assignments.

EMS_EN
11 10

- 0 0 - Disable EMS
- 0 1 - Enable EMS Register programming without having to enable a Page Frame. This is useful for initializing the lower Page Frame.
- 1 0 - Enable upper Page Frame assignments and EMS register programming.
- 1 1 - Enable upper and lower Page Frame assignments and EMS register programming.

**Bits 09:08 -** Not used, state is ignored

**Bit 07 - EN_RES,** Enable Lower Boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the Lower_EMS_Boundary is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore Lower_EMS_Boundary

EN_RES = 1 -
Enable Lower_EMS_Boundary

**Bits 06:00 - A23:17,** Lower_EMS_Boundary

The Lower_EMS_Boundary provides address bits A23:17 and determines the starting address.

This address must be set to 128 Kbyte below the actual start address. For example, to start EMS at the 1 Mbyte boundary, this field should be set to 07H.

**NOTE**

When EMS is not desired in systems with 16 MB or more of system DRAM installed, the EMS Control And Lower Boundary Register at Port Address 6872H should be programmed with a value of 00FEH. When EMS is desired, a value of XX8XH should be programmed.

When EMS is not desired in systems with less than 16 MB of system DRAM installed, the EMS Control And Lower Boundary Register at Port Address 6872H should be programmed with a value of 0000H. When EMS is desired, a value of XX8XH should be programmed.

### 6.4.2 EMS Page Register Pointer

Port Address E072H - Bits 15:06 Read only,
Bits 05:00 Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| DLT | | | | | | | |
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| DLT | | POINTER | | | | | |
| 8 | 7 | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| DLT | 0 |
| POINTER | 0 |

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in Port 6872H, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at Port E872H. Tables 6-7 and 6-8 shows the EMS Page Register Pointer value and the page frame assignments.

**Bits 15:06 - DLT,** Delay Line Test

In the Delay Line Test Mode, these bits represent the state of internal Delay Line signals.

The Delay Line Test is initiated by bit 8 (TDL) in the Test Enable Register at Port Address A872H.

**Bits 05:00 - POINTER,** EMS Page Register Number

Decimal number, 00 through 39. When programming this field, the hex equivalent 00 through 27H should be used.

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| EMS REG NUM | PF_LOC = 00 | EMS REG NUM | PF_LOC = 01 | EMS REG NUM | PF_LOC = 10 | EMS REG NUM | PF_LOC = 11 |
|---|---|---|---|---|---|---|---|
| 32 | E0000-E3FFF | 33 | E4000-E7FFF | 34 | E8000-EBFFF | 35 | EC000-EFFFF |
| 39 | DC000-DFFFF | 32 | E0000-E3FFF | 33 | E4000-E7FFF | 34 | E8000-EBFFF |
| 38 | D8000-DBFFF | 39 | DC000-DFFFF | 32 | E0000-E3FFF | 33 | E4000-E7FFF |
| 37 | D4000-D7FFF | 38 | D8000-DBFFF | 39 | DC000-DFFFF | 32 | E0000-E3FFF |
| 36 | D0000-D3FFF | 37 | D4000-D7FFF | 38 | D8000-DBFFF | 39 | DC000-DFFFF |
| 35 | CC000-CFFFF | 36 | D0000-D3FFF | 37 | D4000-D7FFF | 38 | D8000-DBFFF |
| 34 | C8000-CBFFF | 35 | CC000-CFFFF | 36 | D0000-D3FFF | 37 | D4000-D7FFF |
| 33 | C4000-C7FFF | 34 | C8000-CBFFF | 35 | CC000-CFFFF | 36 | D0000-D3FFF |

EMS registers 32 through 39 (decimal) can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See Port E872H description.

**TABLE 6-7. UPPER PAGE FRAME ASSIGNMENTS**

| EMS REG NUM | HEX | DEC | EMS REG NUM | HEX | DEC |
|---|---|---|---|---|---|
| 23 | 5C000-5FFFF | 368K-384K | 7 | 9C000-9FFFF | 624K-640K |
| 22 | 58000-5BFFF | 352K-368K | 6 | 98000-9BFFF | 608K-624K |
| 21 | 54000-57FFF | 336K-352K | 5 | 94000-97FFF | 592K-608K |
| 20 | 50000-53FFF | 320K-336K | 4 | 90000-93FFF | 576K-592K |
| 19 | 4C000-4FFFF | 304K-320K | 3 | 8C000-8FFFF | 560K-576K |
| 18 | 48000-4BFFF | 288K-304K | 2 | 88000-8BFFF | 544K-560K |
| 17 | 44000- 47FFF | 272K-288K | 1 | 84000-87FFF | 528K-544K |
| 16 | 40000-43FFF | 256K-272K | 0 | 80000-83FFF | 512K-528K |
| 15 | 3C000-3FFFF | 240K-256K | 31 | 7C000-7FFFF | 496K-512K |
| 14 | 38000-3BFFF | 224K-240K | 30 | 78000-7BFFF | 480K-496K |
| 13 | 34000-37FFF | 208K-224K | 29 | 74000-77FFF | 464K-480K |
| 12 | 30000-33FFF | 192K-208K | 28 | 70000-73FFF | 448K-464K |
| 11 | 2C000-2FFFF | 176K-192K | 27 | 6C000-6FFFF | 4320-448K |
| 10 | 28000-2BFFF | 160K-176K | 26 | 68000-6BFFF | 416K-432K |
| 9 | 24000-27FFF | 144K-160K | 25 | 64000-67FFF | 400K-416K |
| 8 | 20000-23FFF | 128K-144K | 24 | 60000-63FFF | 384K-400K |

EMS registers 0 through 31 (decimal) are enabled or disabled as a block. If the EMS_EN field of Port 6872H is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See Port E872H description.

**TABLE 6-8. LOWER PAGE FRAME ASSIGNMENTS**



### 6.4.3 EMS Page Register

Port Address E872H - Bits 14:12 Read only, Bits 15, 11:00 Read and Write

There are 40 EMS Page Registers accessible through Port E872H. Only EMS registers 32 through 39 are initialized to zero. EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at Port E072H provides the offset location for Port E872H.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| EN | 0 | 0 | 0 | P11 | P10 | P9 | P8 |
| | | | | EMS Page Number | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | | | EMS Page Number | | | |

| Signal Name | Default At RSTIN |
|---|---|
| EN | 0 |
| Bits 14:12 | 0 |
| P11:P0 | 0 |

**Bit 15 - EN,** Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at Port 6872H. When EMS_EN equals 11, the EN bit in this register is treated as a one for the lower Page Frame.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

**Bits 14:12 -** Read only, not used by the System Controller

**Bits 11:00 - P11 through P00,** EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MBytes of EMS memory. The memory address is generated by reading the EMS Page Number from the System Controller and multiplying it by 16 Kbytes, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128 Kbytes of memory and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MBytes, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMCS16}}$ and IOCHRDY to make the transfer.

**NOTE**

When using external EMS memory with P11 = 1, EN (bit 15) must be 0. P10:0 correspond to address bits A24:14 respectively

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# 7.0 CACHE CONTROLLER

## 7.1 NON-CACHABLE CONTROL

The System Controller provides the $\overline{KEN}$ signal to an external cache controller to identify non-cachable memory regions.

Two user-definable and twelve standard non-cachable regions are provided. Ten of the twelve standard regions are 16 KB increments from C8000H - EFFFFH. These regions can be used as EMS memory or for DOS 5.0 Upper Memory Blocks and can be enabled or disabled individually. The other two standard non-cachable regions are the video BIOS area (C0000-CXFFF or E0000-EFFFF) and the system BIOS area (F0000-FFFFF). The Non-cachable control logic allows the external cached CPU caching of these regions to be enabled or disabled individually by monitoring the $\overline{KEN}$ signal.

The two user-definable non-cachable regions can also be enabled individually. The non-cachable regions are set by the upper and lower limit registers. These regions are assigned on 4 Kbyte boundaries anywhere in the 16 MB physical address space of the 80386SX.

The typical applications of these user defined noncachable areas are the memory between 512 KB and 640 KB, and the memory accessed on the AT bus. When powered up, the WD7855/LV assumes that all the memory from 0 KB to 640 KB and 1M to 16 MB are cachable. It is necessary to have the BIOS to program the noncachable region registers.

## 7.2 EXTERNAL CACHE CONTROLLER

The System Controller can support an external look-aside cache controller via the $\overline{LBRDY}$ signal on pin 45. This allows a cache to prevent memory cycles by asserting $\overline{LBRDY}$ prior to the end of T2.

## 7.3 CACHE CONTROL REGISTER

Port Address C472H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | C_BSC | | HI_MEM9:8 | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| High Memory Location HI_MEM7:0 | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| C_BSC | 00 |
| HI_MEM9:0 | 0 |

**Bit 15:12 -** Reserved, must be set to 0

**Bit 11:10 - C_BSC**, Core Bus Strength Control

Bits 11:10 become the Core Bus Strength Control if the Core Strap is 3 volts, as determined by bit 03 at Port Address CC72H.

Bits 11:10 are ignored if the Bus Strap is 5 volts.

C_BSC
11 10

0 0 - Default
0 1 - Reserved
1 0 - Reserved
1 1 - Reserved

**Bits 09:00 - HI-MEM,** High memory region $\overline{KEN}$ control.

HI-MEM controls whether or not $\overline{KEN}$ is to be asserted during access to the designated high region, disabling external caching of that region.

BIT 9 EC000H - EFFFFH
BIT 8 E8000H - EBFFFH
BIT 7 E4000H - E7FFFH
BIT 6 E0000H - E3FFFH
BIT 5 DC000H - DFFFFH
BIT 4 D8000H - DBFFFH
BIT 3 D4000H - D7FFFH
BIT 2 D0000H - D3FFFH
BIT 1 CC000H - CFFFFH
BIT 0 C8000H - CBFFFH

HI_MEM 9:0 = 0 -
$\overline{KEN}$ is de-asserted during access to this region, disabling external caching of this region.

HI_MEM 9:0 = 1 -
$\overline{KEN}$ is asserted during access to this region, therefore external caching of this region is allowed.

## 7.4 NONCACHABLE REGION 1 UPPER BOUNDARY

Port Address BC72H - Bits 15:02, 00 Read and Write
Bit 01 Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 |
| Upper Address Boundary | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | S_ | INT_ | INT_ | SN_ |
| Upper Address Boundary | | | | $\overline{REF}$ | $\overline{DIS}$ | $\overline{ST}$ | $\overline{RDY}$ |

| Signal Name | Default At RSTIN |
|---|---|
| A23:12 | 0 |
| S_REF | 0 |
| INT_DIS | 0 |
| INT_ST | 0 |
| SN_RDY | 0 |

**Bits 15:04 - A23:12,** Upper Address Boundary

A23:12 determine the upper address boundary of the user definable noncachable region 1.

**Bit 03 - S_REF,** Slow Refresh

When S_REF is set, the DRAM refresh rate is slowed down to 120 ms. S_REF does not affect the refresh toggle bit REF_DT at Port B (see Section 5.9).

S_REF = 0 -
Disable Slow Refresh

S_REF = 1 -
Enable Slow Refresh

**Bit 02 - INT_DIS,** Interrupt Disable

When INT_DIS is set, the interrupt from the interrupt controller is disabled. The command will not take effect immediately if the interrupt request signal from the interrupt controller is active. The command will take effect immediately if the interrupt request signal is inactive. This allows control of the interrupt regardless of the Operating System Privilege Level, since 'CLI' and 'STI' CPU instructions may be trapped.

10

INT_DIS = 0 -
Enable hardware interrupt

INT_DIS = 1 -
Disable the hardware interrupt from the interrupt Controller

**Bit 01 - INT_ST**, Interrupt Disable Status

This enables reading of Interrupt Status regardless of Operating System privilege Level.

INT_ST = 0 -
Indicates the Interrupt Disable command is processed

INT_ST = 1 -
Indicates the Interrupt Disable command is pending

**Bit 00 - SN_RDY**, SNOOP with IOCHRDY active

During periods when the CPU Clock is slower than the AT BUS clock (slowed for power savings), the Snoop Logic may be unable to properly track the memory cycle during DMA or BUS Master Cycles. Setting SN_RDY enables the System Controller to use the IOCHRDY signal to lengthen the cycle.

SN_RDY = 0 -
Disable IOCHRDY for DMA/Master cycle

SN_RDY = 1 -
Enable IOCHRDY for DMA/Master cycle

## 7.5 NONCACHABLE REGION 1 LOWER BOUNDARY

Port Address B472H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 |
| Lower Address Boundary | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | S_ | X_ | AT_BSC | |
| Lower Address Boundary | | | | DCLK | WS | | |

| Signal Name | Default At RSTIN |
|---|---|
| A23:12 | 0 |
| S_DCLK | 0 |
| X_WS | 0 |
| AT_BSC | 00 |

**Bits 15:04 - A23:12,** Lower Address Boundary.

A23:12 determine the lower address boundary of the user definable noncachable region 1. Noncachable region 1 is disabled when the upper boundary is set below the lower boundary.

**Bit 03 - S_DCLK,** Stop DMA Clock

Setting S_DCLK causes the DMA clock to stop while there is no DMA activity. Upon any unmasked DMA request (DRQIN), the DMA clock starts up again and continues to run until 16 DMA clocks after the end of the DMA Acknowledge (DACKEN).

S_DCLK = 0 -
Disable Stop DMA Clock

S_DCLK = 1 -
Enable Stop DMA Clock

**Bit 02 - X_WS,** Extra Wait State for Page Mode

If X_WS is active, an extra wait state is added to all the memory cycles. This feature allows system designers to use slower DRAMs for the System Controller without loss of huge performance, and achieve saving since the majority of the memory accesses are directly to the internal cache. X_WS may used in conjunction with ERPWS, bit 06 at Port Address 6072H.

X_WS = 0 -
Extra Wait States are not added

X_WS = 1 -
Extra Wait States are added

**Bits 01:00 - AT_BSC**, AT Bus Strength Control

Bits 01:00 become the AT Bus Strength Control if the Bus Strap is 3 volts as determined by bit 02 at Port Address CC72H.

Bits 01:00 are ignored if the Bus Strap is for 5 volts.

AT_BSC
11 10

0 0 - Default
0 1 - Reserved
1 0 - Reserved
1 1 - Reserved

## 7.6 NONCACHABLE REGION 2 LOWER BOUNDARY

Port Address CC72H - Bits 15:12, 01:00 Read and and Write
Bits 03:02 Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 |
| Lower Address Boundary | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | CS | BS | | NR2C |
| Lower Address Boundary | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| A25:12 | 0 |
| CS, BS | None |
| NR2C | 0 |

**Bits 15:04,** A23:12 Lower Address Boundary

A23:12 are used to determine the lower address boundary of the user definable non-cachable region 2. Any address above or equal to this address is considered non-cachable.

**Bit 03 - CS,** Core Strap

CS represents the state of VDD_VL at pin 105

CS = 0 -
Core Strap = 5 volts

CS = 1 -
Core Strap = 3 volts

**Bit 02 - BS,** Bus Strap

BS represents the state of VDDAT_VL at pin 149

BS = 0 -
Bus Strap = 5 volts

BS = 1 -
Bus Strap = 3 volts

**Bit 01** - Reserved

**Bit 00 - NR2C,** Non-cachable Region 2

NR2C = 0 -
Disables non-cachable Region 2

NR2C = 1 -
Enables non-cachable Region 2

## 7.7 FLUSH

Port Address F872H - Write Only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

The $\overline{\text{FLUSH}}$ signal at pin 30 is asserted by writing any data to this I/O port or when a DMA/MASTER Memory write occurs. Asserting the $\overline{\text{FLUSH}}$ signal invalidates all TAG entries in the cached CPU or external cache controller.

An I/O write to this port is ordinarily used by the EMS driver to clear the cache when there is a change to the EMS Page Register and also causes the System Controller to output Chip Select number 13H.

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# 8.0 PORT CHIP SELECT AND REFRESH

This section describes refresh control logic used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- Real-Time Clock bus location
- Access to the CMOS RAM password

Table 8-3 identifies the ports, their Chip Select number, I/O address and function.

## 8.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| M_ REF | V_ RF | CBR_ REF | CBR_ SR | SCSI | PAR | | PAR_ L |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| SER_A | | | SER_ AL | SER_B | | | SER_ BL |

| Signal Name | Default At RSTIN |
|---|---|
| M_REF | 0 |
| V_REF | 0 |
| CBR_REF | 0 |
| CBR_SR | 0 |
| SCSI | 0 |
| PAR | 00 |
| PAR_L | 0 |
| SER_A | 000 |
| SER_AL | 0 |
| SER_B | 000 |
| SER_BL | 0 |

**Bit 15 - M_REF,** Memory Refresh Power Down Mode

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and M_REF = 1, the on-board DRAM is refreshed with every eighth $\overline{PDREF}$. $\overline{PDREF}$ is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory.

M_REF = 1 -
Slow refresh main on-board memory.

**Bit 14 - V_REF**, Video Refresh Power Down Mode

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and V_REF = 1, the on-board DRAM is refreshed with every eighth $\overline{PDREF}$. $\overline{PDREF}$ is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory

V_REF = 1 -
Slow refresh video memory

**Bit 13 - CBR_REF,** CAS Before RAS Refresh For On-board DRAM

Most standard DRAMs support this type of CAS before RAS refresh, while special DRAMs do not. CBR_REF must always be set to 1 for portable systems that support suspend/resume.

CBR_REF = 0 -
Normal refresh for on-board DRAM

CBR_REF = 1 -
CAS before RAS refresh

**Bit 12 - CBR_SR**, CAS Before RAS Self Refresh

CAS before RAS self refresh is supported only by special DRAMs.

CBR_SR = 0 -
No CAS before RAS self refresh

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

**Bit 11 - SCSI**, Small Computer System Interface Chip Select

The SCSI is selected by chip select number 12. See Table 8-3.

SCSI = 0 -
SCSI chip select disabled

SCSI = 1 -
SCSI chip select at I/O port 353XH

**Bits 10:09 - PAR**, Parallel Port Chip Select

The parallel port is selected by chip select number 0FH and may be located at I/O address 278H through 27FH, 378H through 37FH, or 3BCH through 3BFH. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 8-3.

PAR
10 09

0 0 - PAR chip select disabled
0 1 - PAR chip select at I/O port 3BCH - 3BFH
1 0 - PAR chip select at I/O port 378H - 37FH
1 1 - PAR chip select at I/O port 278H - 27FH

**Bit 08 - PAR_L**, Parallel Port Bus Location

PAR_L = 0 -
Parallel port is located on the RA0:7/ED0:7 bus. This is typical when the WD76C30A is used.

PAR_L = 1 -
Parallel port is located on the expansion data bus. This is typical when the WD7615 is used.

**Bits 07:05 - SER_A**, Serial Port A Chip Select

The Serial Port A is selected by chip select number 0EH and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 07:05 may disable the chip select or locate it at one of the four areas. See Table 8-3.

It is possible to select the same I/O port address for Serial Port A and Serial Port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial Port A chip select disabled
0 0 1 - Serial Port A chip select at I/O port 3F8H - 3FFH
0 1 0 - Serial Port A chip select at I/O port 2F8H - 2FFH
0 1 1 - Serial Port A chip select at I/O port 3E8H - 3EFH
1 0 0 - Serial Port A chip select at I/O port 2E8H - 2EFH

**Bit 04 - SER_AL**, Serial A Port Bus Location

SER_AL = 0 -
Serial Port A is located on the RA0:7/ED0:7 bus. This is typical when the WD76C30A is used.

SER_AL = 1 -
Serial Port A is located on the expansion data bus.

**Bits 03:01 - SER_B** Serial Port B Chip Select

The Serial Port B is selected by chip select number 10 and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 03:01 may disable the chip select or locate it at one of the four areas. See Table 8-3.

It is possible to select the same I/O port address for Serial Port B and Serial Port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_B
03 02 01

0 0 0 - Serial Port B chip select disabled
0 0 1 - Serial Port B chip select at I/O port 3F8H - 3FFH
0 1 0 - Serial Port B chip select at I/O port 2F8H - 2FFH
0 1 1 - Serial Port B chip select at I/O port 3E8H - 3EFH
1 0 0 - Serial Port B chip select at I/O port 2E8H - 2EFH

**Bit 00 - SER_BL,** Serial B Port Bus Location

SER_BL = 0 -
Serial Port B is located on the RA0:7/ED0:7 bus. This is typical when the WD76C30A is used.

SER_BL = 1 -
Serial Port B is located on the expansion data bus

## 8.2 RTC, PVGA, AND DISK CHIP SELECTS

Port Address 2872H - Read and Write

Bits 12:07 and Port Address 3072H control the use and location of the Programmable Chip Select #1.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| RTC_ L | FST_ VGA | FST_ SCSI | EN_ PCS1 | U_ MSK1 | L_MSK1 | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PRG_ L | HS_ HD | EN_ 16 | P/S | | LK_ PSW | DS_ HD | DS_ FLP |

| Signal Name | Default At RSTIN |
|---|---|
| RTC_L | 0 |
| FST_VGA | 0 |
| FST_SCSI | 0 |
| EN_PCS1 | 0 |
| U_MSK1 | 00 |
| L_MSK1 | 00 |
| PRG L | 0 |
| HS HD | 000 |
| EN_16 | 0 |
| P/S | 000 |
| LK PSW | 0 |
| DS HD | 0 |
| DS FLP | 0 |

**Bit 15 - RTC_L,** Real-Time Clock

The Real-Time Clock is normally on the RA0:7/ED0:7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real-Time Clock is on the RA0:7/ED0:7 bus.

RTC_L = 1 -
Real-Time Clock is on the expansion data bus. This is the required setting when the WD76C20 is used.

**Bit 14 - FST_VGA,** Fast VGA Video

The performance of Western Digital PVGA display controllers may be enhanced by reducing wait states for access to video I/O. This feature should only be used with Western Digital PVGA1A, WD90C90, WD90C30, WD90C20, WD90C11 and WD90C10 devices. I/O cycles to eight-bit ports 3C0H - 1H, 3C4H - 5H and 3CEH - FH are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control

FST_VGA = 1 -
One wait state I/O cycle to PVGA

**Bit 13 - FST_SCSI,** Fast SCSI

The performance of the WD33C93 SCSI Controller is enhanced by performing eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States

FST_SCSI = 1 -
One Wait State

**Bit 12 - EN_PCS1,** Enable Programmable Chip Select 1

The Programmable Chip Select logic is selected with Chip Select 11 and may be disabled or enabled. See Table 8-3.

EN_PCS1 = 0 -
Disable Programmable Chip Select #1

EN_PCS1 = 1 -
Enable Programmable Chip Select #1

**Bit 11 - U_MSK1,** Upper Address Bits Masked

U_MSK1 determines whether or not the upper address bits A15:10 are to be used as designated in the Programmable Chip Select Address Register at Port Address 3072H.

U_MSK1 = 0 -
A15:10 are ignored

U_MSK1 = 1 -
A15:10 are included in the address

**Bits 10:08 - L_MSK1,** Lower Address Bits Masked

L_MSK1 determines whether the lower four address bits A03:00 are to be used as designated in the Programmable Chip Select Address Register at Port Address 3072H.

L_MSK1
10 09 08

0 0 0 - A09:00 are included in the address
0 0 1 - A00 is ignored
0 1 0 - A00:01 are ignored
0 1 1 - A00:02 are ignored
1 0 0 - A00:03 are ignored

**Bit 07 - PRG_L,** Programmable Chip Select Bus Location

PRG_L = 0 -
Programmable Chip Select is on the RA0:7/ED0:7 bus

PRG_L = 1 -
Programmable Chip Select is on the expansion bus

**Bit 06 - HS_HD,** High Speed Hard Disk Data Transfer Rate

Enabling the high-speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high-speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with $\overline{IOCS16}$ ignored and the WD76C20 hard disk chip select remaining stable.

**NOTE**

This feature requires the use of the WD76C20 and should only be used with Western Digital IDE drives WD-AC280, WD-AC140, WD-AC160, WD-AC2120, WD-AP4200, WD-AB130 and WD-AH260.

HS_HD = 0 -
Compatible bus timing enabled

HS_HD = 1 -
High-speed hard disk accesses enabled

**Bit 05 - EN_16,** Enable 16-Bit I/O Decoding

The WD7855/LV supports both the 100% IBM-AT compatible I/O decoding (10-bit mode) and the newer IBM PS/2 compatible I/O decoding (16-bit mode). The mode is selected by this bit.

EN_16 = 0 -
AT Compatible 10-bit decode. Address bits A15:10 are ignored. See Table 8-1.

EN_16 = 1 -
The enhanced 16-bit mode enabled. See Table 8-2.

**Bit 04 - P/S,** Primary Or Secondary Disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 8-3, chip select numbers 08H through 0BH.

P/S = 0 -
Primary hard disk and Floppy address selected

P/S = 1 -
Secondary hard disk and Floppy address selected

**Bit 03 -** Reserved

10

**Bit 02 - LK_PSW,** Prevent Locking Password

Port 092H bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092H bit 3, Lock_Pass can be set.

LK_PSW = 1 -
Port 092H bit 3, Lock_Pass can not be set.

**Bit 01 - DS_HD,** Hard Disk Chip Select 0CH, 0DH

DS_HD = 0 -
Hard disk chip select is enabled.

DS_HD = 1 -
Hard disk chip select is not generated.

**Bit 00 - DS_FLP,** Floppy Disk Chip Select 08H, 09H, 0AH, 0BH

DS_FLP = 0 -
Floppy disk chip select is enabled.

DS_FLP = 1 -
Floppy disk chip select is not generated.

| ADDRESS * | DEVICE |
|---|---|
| 000:01F | DMA Controller 1 (Ch 0:3) |
| 020:03F | Interrupt Controller Master |
| 040:05F | Timer |
| 060:06E (even) | Keyboard Port |
| 061:06F (odd) | Port B - Parity Error And I/O Channel Check |
| 070 bit 7 | NMI Mask |
| 070 | RTC Address |
| 071 | RTC Data |
| 080:08F, 090:091 093:09F | DMA Page |
| 092 | ALT 20 GATE, Hot Reset Port 92 |
| 0A0:0BF | Interrupt Controller Slave |
| 0C0:0DF | DMA Controller 2 (Ch 5:7) |
| 0F0:0F1 | Numeric Processor Clear And Reset |
| 1F0:1F7 | Hard Disk Chip Select (primary) |
| 170:177 | Hard Disk Chip Select (secondary) |
| 278:27F | Parallel Port 3 |
| 2E8:2EF | Serial Port 4 |
| 2F8:2FF | Serial Port 2 |
| 378:37F | Parallel Port 2 |
| 3BC:3BF | Parallel Port 1 |
| 3E8:3EF | Serial Port 3 |
| 3F0:3F7 | Floppy and Hard Disk (primary) |
| 370:377 | Floppy and Hard Disk (secondary) |
| 3F8:3FF | Serial Port 1 |
| * A15:10 are ignored. | |

**TABLE 8-1. AT COMPATIBLE 10-BIT MODE**

| ADDRESS * | DEVICE |
|---|---|
| 0000:000F | DMA Controller 1 (Ch 0:3) |
| 0010:001F | AT Bus |
| 0020:0021 | Interrupt Controller Master |
| 0022:003F | AT Bus |
| 0040:0043 | Timer |
| 0044:005F | AT Bus |
| 0060, 0064 | Keyboard Port |
| 0061 | Port B - Parity Error And I/O Channel Check |
| 0062, 0063 0065:006F | AT Bus |
| 0070 Bit 7 | NMI Mask |
| 0070 | RTC Address |
| 0071 | RTC Data |
| 0072:007F | AT Bus |
| 0080:008F | DMA Page |
| 0090:0091 | AT Bus |
| 0092 | ALT 20 GATE, Hot Reset Port 92 |
| 0093:009F | AT Bus |
| 00A0:00A1 | Interrupt Controller Slave |
| 00A2:00BF | AT Bus |
| 00C0:00DE (even) | DMA Controller 2 (Ch 5:7) |
| 00C1:00DF (odd) | AT Bus |
| 00E0:00EF | AT Bus |
| 00F0:00F1 | Numeric Processor Clear And Reset |
| 00F2:00FF | AT Bus |
| 01F0:01F7 | Hard Disk Chip Select (primary) |
| 0170:0177 | Hard Disk Chip Select (secondary) |
| 0278:027F | Parallel Port 3 |
| 02E8:02EF | Serial Port 4 |
| 02F8:02FF | Serial Port 2 |
| 0378:037F | Parallel Port 2 |
| 03BC:03BF | Parallel Port 1 |
| 03E8:03EF | Serial Port 3 |
| 03F0:03F7 | Floppy and Hard Disk (primary) |
| 0370:0377 | Floppy and Hard Disk (secondary) |
| 03F8:03FF | Serial Port 1 |
| * A15:10 equal 0 | |

**TABLE 8-2. ENHANCED 16-BIT MODE**

## 8.3 PROGRAMMABLE CHIP SELECT #1 ADDRESS

Port Address 3072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | A11 | A10 | A09 | A08 |
| Chip Select Address | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A07 | A06 | A05 | A04 | A03 | A02 | A01 | A00 |
| Chip Select Address | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals . . . . . | None |

10

## 8.4 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 8-3 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

I/O to the addresses listed in Table 8-3 automatically cause the System Controller to output $\overline{CSEN}$ along with the corresponding encoded chip select value on CS4:0 (DPH, DPL, RA10:8). This is decoded by either the WD76C20/ALV or descrete logic which in turn asserts individual chip select signals to the various peripherals. Some of these chip selects can be individually enabled or disabled by way of registers 2072H and 2872H.

| PORT | I/O ADDRESS 10-BIT MODE (HEX) | I/O ADDRESS 16-BIT MODE (HEX) | CHIP SELECT NUMBER (HEX) | FUNCTION |
|---|---|---|---|---|
| ROM Chip Select | N/A | N/A | 00 | Chip select for BIOS ROM |
| Keyboard Control | 060:06E even | 0060, 0064 | 01 | Chip select for 8042 |
| Power Control | 7072 | 7072 | 03 | PMC Write Strobe 0 |
| Reserved | | | 04 | Reserved |
| Real-time Clock | 070 | 0070 | 05 | RTC ALE |
| Real-time Clock | 071 | 0071 | 06 | RTC Write Strobe |
| Real-time Clock | 071 | 0071 | 07 | RTC Read Strobe |
| Floppy Operation Chip Select | 3F2<br>372 | 03F2<br>0372 | 08 | Primary address<br>Secondary address |
| Floppy Chip Select | 3F4, 3F5<br>374, 375 | 03F4, 03F5<br>0374, 0375 | 09 | Primary address<br>Secondary address |
| Floppy Control Chip Select | 3F7<br>377 | 03F7<br>0377 | 0A | Primary address<br>Secondary address (Floppy enabled, HD disabled) |
| Floppy and HD Control Chip Select | 3F7<br>377 | 03F7<br>0377 | 0B | Primary address<br>Secondary address (Floppy enabled, HD enabled) |
| Hard Disk Chip Select | 1F0:1F7<br>170:177 | 01F0:01F7<br>0170:0177 | 0C | Primary address<br>Secondary address |
| Hard Disk Chip Select | 3F6<br>3F7 ①<br>376<br>377 ① | 03F6<br>03F7 ①<br>0376<br>0377 ① | 0D | Primary Address<br><br>Secondary address |
| Serial Port A Chip Select | 2E8:2EF<br>2F8:2FF<br>3E8:3EF<br>3F8:3FF | 02E8:02EF<br>02F8:02FF<br>03E8:03EF<br>03F8:03FF | 0E ② | |
| Parallel Port 0 Chip Select | 278:27F<br>378:37F<br>3BC:3BF | 0278:027F<br>0378:037F<br>03BC:03BF | 0F | |

**TABLE 8-3. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS**

| PORT | I/O ADDRESS 10-BIT MODE (HEX)① | I/O ADDRESS 16-BIT MODE (HEX) | CHIP SELECT NUMBER (HEX) | FUNCTION |
|---|---|---|---|---|
| Serial Port B Chip Select | 2E8:2EF<br>2F8:2FF<br>3E8:3EF<br>3F8:3FF | 02E8:02EF<br>02F8:02FF<br>03E8:03EF<br>03F8:03FF | 10 ② | |
| Program Chip Select 1 | PROG 1 | PROG 1 | 11 | |
| SCSI | 3530:353X | 3530:353X | 12 | |
| Cache Flush | F872 | F872 | 13 | |
| EMS | | | 14 | External EMS |
| | F072 | F072 | 15 | 48 MHz Clock Disabled |
| | F472 | F472 | 16 | 48 MHz Clock Enabled |
| Power Control | 7872 | 7872 | 17 | PMC Write Strobe 1 |
| Floppy Chip Select | 3F0:3F1<br>370:371 | 03F0:03F1<br>0370:0371 | 18 | Primary address<br>Secondary address |
| Floppy Chip Select | 3F3<br>373 | 03F3<br>0373 | 19 | Primary address<br>Secondary address |
| Program Chip Select 2 | PROG 2 | PROG 2 | 1A | |
| Program Chip Select 3 | PROG 3 | PROG 3 | 1B | |
| Reserved | | | 1E | Reserved |
| Reserved | | | 1F | Reserved |

① IDE Hard disk enabled, floppy disabled

② The Chip Select Number is the decoded value of CS4:CS0. If the Programmed Chip Select corresponds to any other decode, the Programmed Chip Select is suppressed. If Serial Port A and B are programmed for the same address, Serial Port B Chip Select is suppressed.

**TABLE 8-3. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS (Continued)**

# 9.0 POWER MANAGEMENT CONTROL

The WD7855/LV supports all PMC inputs, output and interrupt functions.

## 9.1 SYSTEM ACTIVITY MONITOR (SAM)

The System Activity Monitor (SAM) found in the WD7855/LV is a hardware solution to monitoring system activity. SAM was conceived to solve the problems associated with system activity detection in various operating environments such as DOS, Windows, OS/2, VCPI and Microsoft APM.

With previous System Controllers such as the WD76C10 a software approach was employed to determine system activity. This software approach was accomplished using a watchdog timer. As a part of the watchdog timer service, the sources of activity are checked and a determination is then made on the state of system activity. This approach does not consider the state of the system activity between watchdog timer interrupts. However, with SAM, the system activity state is continuously monitored through hardware, thus providing a more universal approach to activity detection.

With the help of SAM it is now possible to:

- Provide a trigger when a pre-programmed period of system inactivity time elapses.
- Enable/disable the sources that constitute system activity.
- Select either coarse or fine timeout values for system inactivity period.

**System Activity**
System activity denotes periods of time in which the system performs useful tasks. The sources of System Activity are:

- Unmasked pending interrupts.
- Unmasked interrupts in service.
- Access to hard disk data port.
- I/O Access to programmable chip select port.
- DMA transfers.
- Coprocessor cycles.
- A programmable PCU input.
- NMI.

SAM allows for excluding the following interrupt sources from contributing to system activity:

- IRQ0, used by DOS to keep track of the system time.
- IRQ7, used for spurious interrupts and parallel port interrupts.
- IRQ8, used by Windows, OS/2 and other multitasking environments to keep the scheduler running.
- A programmable interrupt level used as a power management interrupt.

SAM also takes into account programs such as MOUSE.COM which, in an attempt to locate a mouse on a communication port, generates interrupts on interrupt levels 3 and 4, and leaves them pending. To overcome this problem, SAM allows only the unmasked pending interrupts on 3 and 4 to constitute system activity.

**Using SAM for System Power Management:**

a) System Timeout Capability

SAM can be programmed to determine coarse periods of inactivity, with the minimum period as one minute, four seconds, up to a maximum period of 16 minutes. It is also possible to extend the maximum limit to any value by reading the Activity Before bit (ACTBEF) in the Activity Monitor Control Register at Port Address B072H.

On reaching the programmed period, SAM generates a Local Attention signal. Typically, the Local Attention is tied to a power management interrupt. In response to Local Attention, the power management interrupt handler makes it possible to prepare the system for a Suspend operation.

b) Responding to a Suspend Request

SAM can be programmed to determine a clean breakpoint for suspending the system upon receiving the Suspend request. At the time the Suspend request is received, it is possible that the system is busy performing an indivisible operation, and it is necessary to wait for the system to finish this indivisible operation before initiating suspend. In order to do this, control to the CPU must be relin-

quished for just enough time for the CPU to complete the operation. This is referred as Suspend arbitration.

In addition to performing Suspend arbitration, SAM is also responsible for determining the earliest opportunity to initiate the Suspend sequence. For instance, if a Suspend request is caused by a low battery condition, it is imperative that the system be placed in the suspend state as soon as possible. Here, the fine granularity of SAM may be used to determine brief periods of inactivity from as low as 7.8 milliseconds to as high as 117.2 milliseconds and establish a clean breakpoint for suspending the system.

**Advantages of SAM:**

1. SAM is a reliable and consistent approach to detecting system activity.

2. SAM is hardware based making it truly non-obtrusive.

3. SAM is independent of the operating environment and the execution mode of the processor.

4. SAM can perform in two modes:

- Detection of system activity for extended periods of time for the purposes of system timeout.
- Detection of brief periods of inactivity for initiating Suspend.

5. Programmability allows for the control of sources of system activity and setting up coarse and fine timeout values.

6. SAM generates a signal called Local Attention (LCL_ATN, PMC #4) on reaching programmed periods of timeout. This signal is generally tied to an unused IRQ level to invoke the Power Management program. Optionally, SAM can generate a System Management Interrupt (SMI on pin 108) rather than LCL_ATN.

7. SAM also carries information on DMA activity state. This is used to determine whether it is appropriate to place the processor in the Sleep Mode.

8. SAM makes it possible to read the state of the interrupt controllers and, if needed, reprogram them on Resume. This is provided to handle the spurious interrupts that are generated by devices at power-up time on Resume.

**NOTE**

SAM cannot be used to determine when the processor should be placed in the Sleep Mode. This determination is intimately tied to the operating environment and is handled either by Western Digital's Power Management drivers DOS/VCPI, Windows and OS/2 or by Microsoft APM.

The System Activity Monitor is controlled by the Activity Monitor Control Register at Port Address B072H, Activity Monitor Mask Register at Port Address D872H and bit 09 of the Test Enable Register at Port Address A872H.

## 9.2 PROCESSOR POWER DOWN MODE

The Processor Power Down Mode is initiated by setting bit 13 of the register at Port Address 1872H to one. The CPURES signal is asserted, then tristated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC #5) signal from the PMC Control Register is used to control the power converter from the processor. The WD7855/LV holds CPUCLK, READY, HOLDR, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the Power Up Mode. The Power Up Mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change, resulting in an unmasked NMI to Port 9072H. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms, PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, READY, HOLDR, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

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The PMC unit is composed of either two 74HCT273 chips and one 74HCT151 chip, or a Western Digital WD7625 Buffer Manager. The two 74HCT273 octal latches are used for the 16 PMC outputs from data bus ED(0:7) and the 74HCT151 8:1 multiplexer is used for the PMCIN signal, while the WD7625 internal multiplexers perform both functions. The PMC output latches are cleared at power up (see Figure 5-1).

## 9.3 LOCAL ACCESS BY KEYBOARD CONTROLLER

The keyboard processor may access the WD7855/LV internal registers by way of the PMC logic. The keyboard processor starts a local access by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at Port 8872H (see Figure 5-1 and Table 9-2). The WD7855/LV arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HOLDA), the WD7855/LV asserts LCL_ACK (PMC output 3 from Port 7072H) on the ED(0:7) data bus. The keyboard processor then passes the opcode/address byte to the WD7855/LV on the data bus and drops the LCL_REQ. The WD7855/LV responds by de-asserting LCL_ACK.

If the opcode specified a register write, data high (D15:08) and data low (D07:00), bytes are passed to the WD7855/LV. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD7855/LV to the keyboard processor.

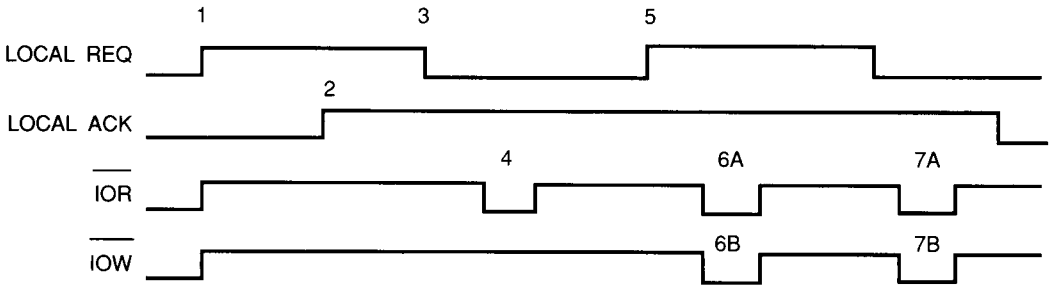
All special operation registers within the WD7855/LV may be accessed in this manner without first unlocking the register. See Section 2.8.2, Port Address F073H, for Lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

If a particular design uses processor-power-down on a non-static CPU and also uses this local access feature, then an additional AND gate is required.

Local access during CPU power-down depends on ADDR2 coming from the CPU through the 74ACT373 bus latch. If the CPU is powered down, ADDR2 can be either high or low, depending on the last CPU address. PROC_PWR_GOOD should be ANDed with ADDR2 going to the 8742. This forces ADDR2 low, making local accesses possible during CPU power-down conditions. This also passes ADDR2 during normal operation.

Figure 9-1 shows the handshake procedure, followed by the keyboard controller and the WD7855/LV.

Figures 9-2 and 9-3 represents the power-down (suspend) and power-up (resume) sequence and control.




1 8042 Requests local data transfer

2 WD7855/LV returns LOCAL_ACK after receiving HOLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD7855/LV reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD7855/LV Reads high byte

7A WD7855/LV Read low byte, writes to internal register

FOR READ CYCLE OF WD7855/LV INTERNAL REGISTER:

6B WD7855/LV Writes high byte to 8042

7B WD7855/LV writes low byte to 8042

OP_CODE FORMAT

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIR | RSV | A15 | A14 | A13 | A12 | A11 | A10 |

DIR = 1 - Read register (generates IOW to 8042)

DIR = 0 - Write register (generates IOR to 8042)

**FIGURE 9-1. REGISTER ACCESS BY KEYBOARD CONTROLLER**

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## 9.4 PMC OUTPUT CONTROL REGISTERS

Port Address 7072H - Bits 07:00 are Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| OUT 7 | OUT 6 | OUT 5 | OUT 4 | OUT 3 | OUT 2 | OUT 1 | OUT 0 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**PMC Output Control Bits 7:0**

Port Address 7872H - Bits 07:00 are Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| OUT F | OUT E | OUT D | OUT C | OUT B | OUT A | OUT 9 | OUT 8 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**PMC Output Control Bits 15:08**

| PMC NO. | PMC OUTPUT SIGNAL PORT 7072H | PMC NO. | PMC OUTPUT SIGNAL PORT 7872H |
|---|---|---|---|
| 0H | CPU Clock Driver Enable | 8H | User Defined |
| 1H | LCD Enable | 9H | User Defined |
| 2H | Backlight Enabled | AH | User Defined |
| 3H | LCL_ACK | BH | User Defined |
| 4H | LCL_ATN | CH | User Defined |
| 5H | Processor power Down | DH | User Defined |
| 6H | Gate A20 | EH | User Defined |
| 7H | Full Power Down | FH | User Defined |

**TABLE 9-1. PMC OUTPUT SIGNALS**

## 9.5 PMC TIMERS

Port Address 8072H - Read and Write

When no Keyboard or Mouse interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072H (see Table 9-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a Keyboard or Mouse interrupt. The Mouse Interrupts are programmed by bits 01 and 00 (BL_MOU) in the RAM Shadow and Write Protect Register at Port Address 6072H. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 10 seconds.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| BL_TIMEOUT | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| LCD_TIMEOUT | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| BL_TIMEOUT | 0 |
| LCD_TIMEOUT | 0 |

**Bits 15:08 - BL_TIMEOUT,** Backlight Time Out

00H - Backlight always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 x 5 seconds
FFH - Backlight enabled

**Bits 07:00 - LCD_TIMEOUT,** LCD Time Out

00H - LCD always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 x 5 seconds
FFH - LCD enabled

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## 9.6 PMC INPUTS

Port Address 8872H - Bits 15:08 Read and Write
Bits 07:00 Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| PMC_ UPD | EN_ LCL | AF 7 | AF 6 | AF 5 | AF 4 | AF 3 | AF 2 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| IN 7 | IN 6 | IN 5 | IN 4 | IN 3 | IN 2 | IN 1 | IN 0 |

| Signal Name | Default At RSTIN |
|---|---|
| PMC_UPD | 0 |
| EN_LCL | 0 |
| AF7:AF2 | 0 |
| IN7:IN0 | None |

**Bit 15 - PMC_UPD,** Enable PMC Update

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of the PMC outputs 15 through 0 (Port Address 7072H and 7872H) or the internal A20 GATE causes an update cycle of the PMC 15:0 output latch.

**Bit 14 - EN_LCL**, Enable Local Request

EN_LCL either enables the PMCIN 2 to be defined by the user or to initiate a local access of the WD7855/LV internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined.

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ.

**Bits 13:08 - AF7:AF2**, Local Attention Flags

Local attention flags AF7 through AF2 are set to indicate which PMC input(s) have caused LCL_ATN in PMC Interrupt Enable Register at Port C872H to be asserted. To clear the flag and corresponding IN bit in the PMC Inputs Register, it is necessary to clear the corresponding EA bit in PMC Interrupt Enable Register. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and AF flag.

AF7 - AF2 = 0 -
This PMC input did not cause LCL_ATN to be asserted.

AF7 - AF2 = 1 -
This PMC input caused LCL_ATN to be asserted.

**Bits 07:00 - IN7:IN0,** PMC Inputs 7:0

The Activity Monitor Mask Register at Port Address D872H may be used to select one of the PMC inputs IN7 through IN2 as a source of activity for power management purposes.

IN7:0 are status flags which provide information about the corresponding PMC input IN7 through IN0. IN1 and IN0 represent the current state of the input, while IN7 through IN2 represent either the current state or a latched transition. An IN7 through IN2 status is unlatched when both the corresponding EI and EA bits in the PMC Interrupt Enable Register at Port C872H are reset. It becomes a latched status when either the corresponding EI or EA bit is set. See Table 9-2.

## 9.7 PMC INTERRUPT ENABLE

Port Address C872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| EI7 | EI6 | EI5 | EI4 | EI3 | EI2 | | |
| Non-maskable Interrupt Enable | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| EA7 | EA6 | EA5 | EA4 | EA3 | EA2 | | |
| Local Attention Enable | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| EI7-EI2 | 0 |
| EA7-EA2 | 0 |

**Bits 15:10 - EI7:EI2,** Non-maskable Interrupt Enable 7 through 2

EI7:EI2 enable the generation of an NMI when the corresponding PMC inputs IN_7:IN_2 at Port Address 8872H change state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7:EI2 = 0 -
Non-maskable Interrupt not enabled

EI7:EI2 = 1 -
Non-maskable Interrupt is enabled

**Bits 09:08 -** Not used, state is ignored

**Bits 07:02 - EA7:EA2,** Local Attention Enable

EA7 through EA2 enable the assertion of LCL_ATN by the corresponding IN_7 through IN_2. LCL_ATN is PMC output number 4.

EA7-EA2 = 0 -
LCL_ATN is not enabled

EA7-EA2 = 1 -
LCL_ATN is enabled. If LAEN at Port Address 7C72H is set, SMI will occur. Refer to Section 10.2.

**Bits 01:00 -** Not used, state is ignored

| PMC INPUT NUMBER ① | PMC INPUT NAME | INTERRUPT ON | SETS FLAG NUMBER ② |
|---|---|---|---|
| 00H | TURBO | | |
| 01H | PROC_PWR_GOOD | | |
| 02H | LCL_REQ or User Defined | Transition | IF2 or AF2 |
| 03H | User Defined | Transition | IF3 or AF3 |
| 04H | User Defined | Transition | IF4 or AF4 |
| 05H | User Defined | Transition | IF5 or AF5 |
| 06H | User Defined | Transition | IF6 or AF6 |
| 07H | User Defined | Active Edge | IF7 or AF7 |

① Port Address 8872H, section 9.6
② Port Address 9072H, section 9.8
Port Address 8872H, section 9.6

**TABLE 9-2. PMCIN INPUTS**

## 9.8 NMI STATUS

Port Address 9072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| IF7 | IF6 | IF5 | IF4 | IF3 | IF2 | 0 | 0 |
| | Non-maskable Interrupt Flags | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| IF7:IF2 | 0 |

**Bits 15:08** - Not used, must be 0

**Bits 07:02 - IF7:IF2**, Non-maskable Interrupt Flags 7 through 2

NMI interrupt flags IF7:IF2 are set to indicate which PMC input(s), if any, have caused NMI to be asserted. To reset the flag and corresponding IN status bit in the PMC Input Register at Port Address 8872H, it is necessary to reset the corresponding bit in the PMC Interrupt Enable Register at Port Address C872H. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and IF flag.

**Bits 01:00** - Not used, must be 0

## 9.9 SERIAL/PARALLEL SHADOW REGISTER

Port Address D072H - Read only

The Shadow Register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board serial and parallel devices.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| SP_A Serial Port A | | SP_B Serial Port B | | PP_2 Parallel Port 2 | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PP_0 Parallel Port 0 | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bits 15:14 - SP_A**, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

**Bits 13:12 - SP_B,** Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

**Bits 11:08 - PP_2**, Parallel Port Register 2

This field represents bits 3:0 of Parallel Port Register 2.

**Bits 07:00 - PP_0,** Parallel Port Register 0

This field represents bits 7:0 of Parallel Port Register 0.

## 9.10 INTERRUPT CONTROLLER SHADOW REGISTER

Port Address D472H - Read only

When performing a resume operation, it may be advantageous to reset and reinitialize the interrupt controllers in the System Controller. Since many of the interrupt control registers are write only, it is impossible to determine the state of the interrupt controllers at suspend time. This register makes it possible to determine the state of selected signals internal to the master and slave interrupt controllers. With this information, when the interrupt control registers are reinitialized during resume, they can be returned to the state in which they were before suspend.

ICW2, ICW4, OCW2 and OCW3 referred to in this text is further defined in Sections 5.5.2.2, 5.5.2.4, 5.5.3.2 and 5.5.3.3.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| AMT OUT | DEV | | TM7 | TS7 | SF NM | AUT_ EOI | RA_ EOI |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PLM2 PLM1 PLM0 Priority Level Master | | | PLS2 PLS1 PLS0 Priority Level Slave | | | SMM M | SMM S |

| Signal Name | Default At RSTIN |
|---|---|
| DEV | 0 |
| All other signals | None |

**Bit 15 - AMTOUT,** Activity Monitor Timeout

AMTOUT represents the current state of the timeout comparator in the activity monitor. It is for test purposes only

**Bits 14:13 - DEV,** Device

DEV identifies the device as WD7855, WD7710 or WD76C10A and is used in conjunction with SVER at Port Address A872H. DEV and SVER are defined in Table 11.2.

**Bit 12 - TM7**, Master Interrupt Vector Bit 7

TM7 represents bit 7 of the Interrupt Vector in the Master Interrupt Controller as set by ICW2. Bits 6:3 of the Interrupt Vector may be read from D6:3 by a Poll Command to the Master Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

**Bit 11 - TS7**, Slave Interrupt Vector Bit 7

TS7 represents bit 7 of the Interrupt Vector in the Slave Interrupt Controller as set by ICW2. Bits 6:3 of the Interrupt Vector may be read from D6:3 by a Poll Command to the Slave Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

**Bit 10 - SFNM,** Special Fully Nested Mode

SFNM represents the state of ICW4 - bit 4 in the Master Interrupt Controller. The WD7855/LV does not require SFNM for the slave interrupt controller and ignores its state.

**Bit 09 - AUT_EOI**, Auto End Of Interrupt

AUT_EOI represents the state of ICW4 - bit 1 in the Master Interrupt Controller. The WD7855/LV does not require AUT_EOI for the slave interrupt controller and ignores its state.

**Bit 08 - RA_EOI,** Rotate Auto End Of Interrupt

RA_EOI indicates whether or not Rotate On Automatic End Of Interrupt has been selected in the Master Interrupt Controller by EOI_CONT (bits 7:5 of OCW2). The WD7855/LV does not require Rotate On End Of Interrupt for the slave interrupt controller and ignores its state.

RA_EOI = 0 -
Rotate On Auto End Of Interrupt has not been selected.

RA_EOI = 1-
Rotate On Auto End Of Interrupt has been selected.

**Bits 07:05 - PLM2:PLM0,** Priority Level Master

PLM2:PLM0 represent the bottom priority level programmed into the Master Interrupt Controller by INT_LEV (OCW2 bits 2:0).

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**Bits 04:02 - PLS2:PLS0,** Priority Level Slave

PLS2:PLS0 represent the bottom priority level programmed into the Slave Interrupt Controller by INT_LEV (OCW2 bits 2:0).

**Bit 01 - SMMM,** Special Mask Mode Master

SMMM indicates whether Special Mask Mode has been set in the Master Interrupt Controller by a write to SMM in OCW3.

SMMM = 0 -
Special Mask Mode is not enabled.

SMMM = 1 -
Special Mask Mode is enabled.

**Bit 00 - SMMS,** Special Mask Mode Slave

SMMS indicates whether Special Mask Mode has been set in the Slave Interrupt Controller by a write to SMM in OCW3.

SMMS = 0 -
Special Mask Mode is not enabled.

SMMS = 1 -
Special Mask Mode is enabled.

## 9.11 PORT 70H SHADOW REGISTER

Port Address E472H - Bits 15:12, 10:00 Read only
Bit 11 Read and Write

This register provides information on the status of interrupts and DMA which is useful for determining when the processor may be placed in the sleep mode. Two bits are also provided for generating software delays without incurring the operating system traps that would result from accessing I/O Port Address 0061H in virtual 86 mode. This register also contains a shadow of the Real Time Clock Address Register, a write only I/O port. It is necessary to access the Real Time Clock CMOS RAM during Suspend/Resume operations. This shadow of Port Address 0070H allows it to be restored to the same state it was in at suspend time.

This register can be read without first unlocking the WD7855/LV. This is important since the CLK32K, REFDET, and TODUN bits may need to be read frequently.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| CLK 32K | REF_ DET | INTRQ | NO_ DMA | TOD UN | Reserved | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| D NMI | RTC A6 | RTC A5 | RTC A4 | RTC A3 | RTC A2 | RTC A1 | RTC A0 |

| Signal Name | Default At RSTIN |
|---|---|
| D_NMI | 1 |
| Reserved | 0 |
| All other signals | None |

**Bit 15 - CLK32K**

CLK32K is $\overline{\text{PDREF}}$ at input pin 41 divided by two. CLK32K may be read to provide a stable timing reference, not subject to reprogramming of the refresh rate. CLK32K has a 30.5 µs period and 50% duty cycle.

**Bit 14 - REF_DET,** Refresh Detect

REF_DET is a copy of the REF_DET bit available from I/O Port Address 0061H, Bit 4 described in Section 5.9.

**Bit 13 - INTRQ**, Interrupt Request

INTRQ represents the state of the INTRQ output pin 126 to the CPU.

**Bit 12 - NO_DMA**, No DMA

NO_DMA = 0
A DMA or Bus Master Cycle has occurred within the last 61 µs

NO_DMA = 1
A DMA or Bus Master Cycle has not occurred within the last 30.5 µs

**Bit 11 - TODUN,** Time of Day Update Needed

This is a general purpose storage bit which can be written and read but has no effect on internal logic. Its purpose is to allow an SMI handler to signal the operating system that the time of day has been corrupted. This bit is checked by the Timer 0 Interrupt Handler. Note that although this bit is readable without unlocking the WD7855/LV, it cannot be written unless the WD7855/LV is unlocked.

**Bits 10:08 -** Reserved

**Bit 07 - D_NMI,** Disable Non-Maskable Interrupt Shadow

D_NMI represents the state of the D_NMI bit as it was set the last time I/O Port Address 0070H described in Section 5.8.1 was written.

**Bits 06:00 - RTC_A6:RTC_A0,** Real Time Clock Address Shadow

RTC_A(6:0) represents the state of the Real Time Clock Address Register as it was set the last time I/O Port Address 0070H was written.

## 9.12 ACTIVITY MONITOR CONTROL REGISTER

Port Address B072H - Bits 15, 13:11, 08:00 Read and Write
Bits 14, 10, 09 Read only

For an overview of the Activity Monitor Register, see the general description of the Activity Monitor Mask Register in Section 9.13.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| IRR_ AE | CB12 | AM TM | ACT LCH | IND ET | ACT AFT | ACT BEF | AM EN |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| Coarse Timeout Count AMC7 AMC6 AMC5 AMC4 | | | | Fine Timeout Count AMC3 AMC2 AMC1 AMC0 | | | |

| Signal Name | Default At RSTIN |
|---|---|
| IRRAE | 0 |
| CB12 | None |
| AMTM | 0 |
| ACTLCH | None |
| INDET | None |
| ACTAFT | None |
| ACTBEF | None |
| AMEN | 0 |
| AMC7:AMC0 | 0 |

**Bit 15 - IRRAE,** Interrupt Request Register Activity Enable

IRRAE controls whether or not the IRR (Interrupt Request Register) bits from the Interrupt Controller at Port Address 020H, 0A0H may be a source of activity (refer to Section 5.5).

IRRAE = 0 -
No IRR bits can be used as an activity source.

IRRAE = 1 -
IRR bits can be a source of activity. IRR8, IRR7 and IRR0 may still be masked by Port Address D872H.

**Bit 14 - CB12,** Counter Bit 12

For factory use only.

The activity monitor circuitry contains a 17-bit timeout counter for generating long timeouts. For test purposes, CB12 represents the twelfth bit of that counter.

**Bit 13 - AMTM,** Activity Monitor Test Mode

AMTM = 0 -
Activity Monitor functions normally.

AMTM = 1 -
Activity Monitor is in Test Mode. Activity Monitor State Machine is clocked faster than normal and nine stages of the 17-bit timeout counter are bypassed.

**Bit 12 - ACTLCH,** Activity Latch

This latch is always enabled, regardless of other enable bit settings. Writing a 1 to ACTLCH has no effect.

ACTLCH = 0 -
The Activity Latch is reset by writing 0 to ACTLCH.

ACTLCH = 1 -
Activity by an unmasked source has occurred.

**Bit 11 - INDET,** Inactivity Detect

Writing a 1 to INDET has no effect.

INDET = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

INDET = 1 -
System is idle and the Activity Monitor has requested the local attention output be set. This occurs when there has been no unmasked activity, allowing the predetermined timeout (bits 07:00) to be reached.

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**NOTE**

PMCIN transitions may also cause the local attention (LCL_ATN PMC 4) output to be set.

**Bit 10 - ACTAFT,** Activity After INDET

ACTAFT is a read only bit and its state is ignored during writes.

ACTAFT = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTAFT = 1 -
Activity has occurred after INDET had been set. This would happen when activity occurs during the time it takes to reach the interrupt service routine invoked by the local attention output request.

**Bit 09 - ACTBEF,** Activity Before INDET

ACTBEF is a read only bit and its state is ignored during writes.

ACTBEF = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTBEF = 1 -
Activity did occur and reset the timeout counter before INDET was set. This is important if consecutive timeout periods are being counted in a service routine to obtain a system timeout period other than that available using AMC(7:0) (bits 07:00). It would be necessary for the routine to clear the software counter if ACTBEF were set, since there would have been no activity only for the period of time programmed in AMC(7:0).

**Bit 08 - AMEN,** Activity Monitor Enable

This is the master enable for the Activity Monitor.

AMEN = 0 -
Writing 0 to AMEN places the Activity Monitor in the idle state.

AMEN = 1 -
Writing 1 to AMEN causes the Activity Monitor to start clocking the timeout counter. Each time an unmasked source of activity is detected, the counter is cleared. If no unmasked source of activity is detected before the timeout counter reaches the value programmed by ACM(7:0), INDET and the local attention output are set. The timeout counter is then cleared and a new timeout sequence begins.

**Bits 07:04 - AMC7:AMC4,** Activity Monitor Counter Coarse

AMC(7:4) establish the timeout values from 64 seconds to 16 minutes in 64-second increments. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

| AMC 7 | 6 | 5 | 4 | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | - 0 seconds |
| 0 | 0 | 0 | 1 | - 1 minute, 4 seconds |
| 0 | 0 | 1 | 0 | - 2 minutes, 8 seconds |
| 0 | 0 | 1 | 1 | - 3 minutes, 12 seconds |
| 0 | 1 | 0 | 0 | - 4 minutes, 16 seconds |
| 0 | 1 | 0 | 1 | - 5 minutes, 20 seconds |
| 0 | 1 | 1 | 0 | - 6 minutes, 24 seconds |
| 0 | 1 | 1 | 1 | - 7 minutes, 28 seconds |
| 1 | 0 | 0 | 0 | - 8 minutes, 32 seconds |
| 1 | 0 | 0 | 1 | - 9 minutes, 36 seconds |
| 1 | 0 | 1 | 0 | - 10 minutes, 40 seconds |
| 1 | 0 | 1 | 1 | - 11 minutes, 44 seconds |
| 1 | 1 | 0 | 0 | - 12 minutes, 48 seconds |
| 1 | 1 | 0 | 1 | - 13 minutes, 52 seconds |
| 1 | 1 | 1 | 0 | - 14 minutes, 56 seconds |
| 1 | 1 | 1 | 1 | - 16 minutes, 0 seconds |

**Bits 03:00 - AMC3:AMC0,** Activity Monitor Counter Fine

AMC(3:0) establish the timeout values from 7.8 milliseconds to 117.2 milliseconds in 7.8 millisecond increments. Tolerance on time delays is -0, +3.9 milliseconds. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

| AMC 3 | 2 | 1 | 0 | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | - 0 milliseconds |
| 0 | 0 | 0 | 1 | - 7.8 milliseconds |
| 0 | 0 | 1 | 0 | - 15.6 milliseconds |
| 0 | 0 | 1 | 1 | - 23.4 milliseconds |
| 0 | 1 | 0 | 0 | - 31.3 milliseconds |
| 0 | 1 | 0 | 1 | - 39.1 milliseconds |
| 0 | 1 | 1 | 0 | - 46.9 milliseconds |
| 0 | 1 | 1 | 1 | - 54.7 milliseconds |
| 1 | 0 | 0 | 0 | - 62.5 milliseconds |
| 1 | 0 | 0 | 1 | - 70.3 milliseconds |
| 1 | 0 | 1 | 0 | - 78.1 milliseconds |
| 1 | 0 | 1 | 1 | - 85.9 milliseconds |
| 1 | 1 | 0 | 0 | - 93.8 milliseconds |
| 1 | 1 | 0 | 1 | - 101.6 milliseconds |
| 1 | 1 | 1 | 0 | - 109.4 milliseconds |
| 1 | 1 | 1 | 1 | - 117.2 milliseconds |

**NOTE**

The fine timeout delay (AMC3 through AMC0) is added to the coarse timeout delay (AMC7 through AMC4) to obtain the total timeout delay.

## 9.13 ACTIVITY MONITOR MASK REGISTER

Port Address D872H - Read and Write

The activity monitor provides a hardware solution for determining inactivity in a system. Knowing when a system is inactive is key to performing such power reduction activities as suspend. When the Activity Monitor is enabled by the Activity Monitor Control Register at Port Address B072H, the Activity Monitor clocks a counter and invokes a service routine using local attention when the counter reaches a programmed timeout value. However, while the counter is being clocked, the Activity Monitor continuously monitors for any of several events that would indicate that the system is active. If any of these events occur, the counter is reset and the timeout starts over. Thus the service routine is only invoked when the system has been inactive for a programmed period of time.

To provide a high degree of flexibility in determining what is active and what is not, many sources are routed to the Activity Monitor. These include the IRR (Interrupt Request Register) and ISR (In Service Register) bits from the Interrupt Controller, the PMC inputs, NMI output, DMA (or AT Master) cycles and I/O accesses to either the numeric coprocessor, hard disk data port or programmable chip select. All of these sources are considered activity unless masked.

The interrupt input masks are controlled in the lower byte. All ISR and IRR bits are detected as activity except those specifically masked. Note, however, that ISR2 and IRR2 are not examined since they are cascade interrupts only. Also, IRR3 and IRR4 are qualified by the Mask Register in the Interrupt Controller before being passed to the Activity Monitor. The master mask for all IRR bits is the IRRAE bit in the register at Port Address B072H.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| PCSM | PMCILS | PMCIS2 | PMCIS1 | PMCIS0 | NMIM | HDDM | COPM |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| IMS1 | IMS0 | IRR8M | IRR7M | IRR0M | ISR8M | ISR7M | ISR0M |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - PCSM,** Programmable Chip Select #1 Mask

PCSM = 0 -
Read or write I/O accesses to the ports defined by the programmable chip select #1 in the WD7855/LV are considered activity.

PCSM = 1 -
Read or write I/O accesses to the ports defined by the programmable chip select #1 in the WD7855/LV are ignored.

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**Bit 14 - PMCILS,** Power Management Control Input Level Select

PMCILS determines which logic level on the selected PMC input is to be considered active. (See bits 13:11, PMCIS2:0.)

PMCILS = 0 -
PMCIN is active low.

PMCILS = 1 -
PMCIN is active high.

**Bits 13:11 - PMCIS(2:0),** Power Management Control Input Select

One of the PMC inputs IN7 through IN2 at Port Address 8872H may be selected for detection as a source of activity.

**NOTE**

The EI and EA bits at Port Address C872H, corresponding to the selected IN signal, should be cleared to prevent the IN signal from being latched internally.

| PMCIS 2 | 1 | 0 | | |
|---|---|---|---|---|
| 0 | 0 | 0 | - | PMC input 2 selected |
| 0 | 0 | 1 | - | PMC input 3 selected |
| 0 | 1 | 0 | - | PMC input 4 selected |
| 0 | 1 | 1 | - | PMC input 5 selected |
| 1 | 0 | 0 | - | PMC input 6 selected |
| 1 | 0 | 1 | - | PMC input 7 selected |
| 1 | 1 | 0 | - | Reserved |
| 1 | 1 | 1 | - | Disabled, no PMC inputs checked |

**Bit 10 - NMIM,** Non-maskable Interrupt Mask

NMIM = 0 -
The NMI output is used as a source of activity.

NMIM = 1 -
The NMI output is ignored.

**Bit 09 - HDDM,** Hard Disk Data Port Mask

HDDM = 0 -
If the hard disk chip select has been enabled by bit 01 at Port Address 2872H, I/O read and write operations to the 16-bit hard disk data port are allowed as a source of activity.

HDDM = 1 -
The hard disk data port I/O is ignored.

**Bit 08 - COPM,** Coprocessor Mask

COPM = 0 -
I/O cycles to the coprocessor are treated as a source of activity. For an 80386SX system, this is when A23 is high and M/$\overline{IO}$ is low.

COPM = 1 -
I/O to the coprocessor is ignored.

**Bits 07:06 - IMS1:0,** Interrupt Mask Select

The local attention generated by the Activity Monitor will be routed to an available interrupt input to invoke a service routine. That interrupt is not to be detected as a source of activity. IMS(1:0) provide a selection of four possible inputs to be used for this function and masks the corresponding IRR and ISR bits as sources of activity.

| IMS 1 | 0 | | |
|---|---|---|---|
| 0 | 0 | - | IRQ5 masked |
| 0 | 1 | - | IRQ10 masked |
| 1 | 0 | - | IRQ11 masked |
| 1 | 1 | - | IRQ15 masked |

**Bit 05 - IRR8M,** Interrupt Request Register 8 Mask

IRR8M = 0 -
Real-Time Clock Interrupt (IRR8) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR8M = 1 -
Real-Time Clock Interrupt (IRR8) is ignored.

**NOTE**

See Test Enable Register (A872H), Section 11.3 for information about IRQ9 enable control.

See SMI Auxiliary Control Register (5472H), Section 10.10, for a definition of the activity masks for PCS2 and PCS3.

**Bit 04 - IRR7M,** Interrupt Request Register 7 Mask

IRR7M = 0 -

Parallel Port or Spurious Interrupt (IRR7) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR7M = 1 -

Parallel Port or Spurious Interrupt (IRR7) is ignored.

**Bit 03 - IRR0M,** Interrupt Request Register 0 Mask

IRR0M = 0 -

Time Of Day Interrupt (IRR0) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR0M = 1 -

Time Of Day Interrupt (IRR0) is ignored.

**Bit 02 - ISR8M,** Interrupt Service Register 8 Mask

ISR8M = 0 -

Real-Time Clock Interrupt (ISR8) may be detected as a source of activity.

ISR8M = 1 -

Real-Time Clock Interrupt (ISR8) is ignored.

**Bit 01 - ISR7M,** Interrupt Service Register 7 Mask

ISR7M = 0 -

Parallel Port or Spurious Interrupt (ISR7) may be detected as a source of activity.

ISR7M = 1 -

Parallel Port or Spurious Interrupt (ISR7) is ignored.

**Bit 00 - ISR0M,** Interrupt Service Register 0 Mask

ISR0M = 0 -

Time of Day Interrupt (ISR0) may be detected as a source of activity.

ISR0M = 1 -

Time Of Day Interrupt (ISR0) is ignored.

## 9.14 3V SUSPEND (HIBERNATION) SHADOW REGISTERS

The 3V suspend mode provides maximum power savings for the system. The contents of the DRAM, Chip Set Registers, CPU Registers and Video RAM are all written to the hard disk and then all voltages are shut down, including the power supply. The only logic left on in this mode is the real-time clock and a 3 volt suspend controller. The real-time clock and the 3 volt suspend controller run off of the real-time clock battery. When the resume request is sampled by the suspend controller, the suspend controller enables the power supply and resumes the system.

To maintain compatibility with the IBM AT, the timer and DMA registers cannot be read back. To overcome this, these registers are shadowed and read back through other registers. (See the descriptions for register B872H in Section 5.4.15, register D072H in Section 9.9, register D472H in Section 9.10, registers 3C72H, 4472H and 4C72H in Section 9.14.1, 9.14.2 and 9.14.3.)

### 9.14.1 DMA Shadow Register 1

Port Address 3C72H - Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| AD_ DEC2 | AUTO 2 | TRA_TYP2 | | TRA_MOD1 | | AD_ DEC1 | AUTO 1 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| TRA_TYP1 | | TRA_MOD0 | | AD_ DEC0 | AUTO 0 | TRA_TYP0 | |

| Signal Name | Default At RSTIN |
|---|---|
| All Signals | 0 |

**Bit 15 - AD_DEC2,** Address Decrement 2

AD_DEC bit of register at Port Address 00BH for DMA channel 2.

**Bit 14 - AUTO2,** Autoinitialize 2

AUTO bit of register 00BH for DMA channel 2.

**Bits 13:12 - TRA_TYP2,** Transfer Type 2

TRA_TYP bits of register at Port Address 00BH for DMA channel 2.

**Bits 11:10 - TRA_MOD1**, Transfer Mode 1

TRA_MOD bits of register at Port Address 00BH for DMA channel 1.

**Bit 09 - AD_DEC1,** Address Decrement 1

AD_DEC bit of register at Port Address 00BH for DMA channel 1.

**Bit 08 - AUTO1,** Autoinitialize 1

AUTO bit of register at Port Address 00BH for DMA channel 1.

**Bits 07:06 - TRA_TYP1,** Transfer Type 1

TRA_TYP bits of register at Port Address 00BH for DMA channel 1.

**Bits 05:04 - TRA_MOD0,** Transfer Mode 0

TRA_MOD bits of register at Port Address 00BH for DMA channel 0.

**Bit 03 - AD_DEC0,** Address Decrement 0

AD_DEC bit of register at Port Address 00BH for DMA channel 0.

**Bit 02 - AUTO0**, Autoinitialize 0

AUTO bit of register at Port Address 00BH for DMA channel 0.

**Bits 01:00 - TRA_TYP0,** Transfer Type 0

TRA_TYP bits of register at Port Address 00BH for DMA channel 0.

### 9.14.2 DMA Shadow Register 2

Port Address 4472H - Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| TRA_TYP6 | | TRA_MOD5 | | AD_ DEC5 | AUTO 5 | TRA_TYP5 | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| TRA_MOD3 | | AD_ DEC3 | AUTO 3 | TRA_TYP3 | | TRA_MOD2 | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 15:14 - TRA_TYP6,** Transfer Type 6

TRA_TYP bits of register at Port Address 0D6H for DMA channel 6.

**Bits 13:12 - TRA_MOD5**, Transfer Mode 5

TRA_MOD bits of register at Port Address 0D6H for DMA channel 5.

**Bit 11 - AD_DEC5**, Address Decrement 5

AD_DEC bit of register at Port Address 0D6H for DMA channel 5.

**Bit 10 - AUTO5,** Autoinitialize 5

AUTO bit of register at Port Address 0D6H for DMA channel 5.

**Bits 09:08 - TRA_TYP5**, Transfer Type 5

TRA_TYP bits of register at Port Address 0D6H for DMA channel 5.

**Bits 07:06 - TRA_MOD3,** Transfer Mode 3

TRA_MOD bits of register at Port Address 00BH for DMA channel 3.

**Bit 05 - AD_DEC3,** Address Decrement 3

AD_DEC bit of register at Port Address 00BH for DMA channel 3.

**Bit 04 - AUTO3**, Autoinitialize 3

AUTO bit of register at Port Address 00BH for DMA channel 3.

**Bits 03:02 - TRA_TYP3,** Transfer Type 3

TRA_TYP bits of register at Port Address 00BH for DMA channel 3.

**Bits 01:00 - TRA_MOD2,** Transfer Mode 2

TRA_MOD bits of register at Port Address 00BH for DMA channel 2.

### 9.14.3 DMA Shadow Register 3

Port Address 4C72H - Bit 15 Read and Write
Bits14:0 Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| SCB | | EX_ WR | RO_ PRI | | CO_ DIS | TRA_MOD7 | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| AD_ DEC7 | AUTO 7 | TRA_ TYP7 | | TRA_ MOD6 | | AD_ DEC6 | AUTO 6 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - SCB**, Shadow Control Bit

For more information regarding SCB see Sections 9.14.4 and 9.14.5)

SCB = 0 -
EX_WR, RO_PRI and CO_DIS from the Command Register at Port Address 0D0H is presented on bits 13, 12 and 10.

SCB = 1 -
EX_WR, RO_PRI and CO_DIS from the Command Register at Port Address 008H is presented on bits 13, 12 and 10.

**Bit 14,** Reserved

**Bit 13 - EX_WR,** Extended Write

If SCB = 0, this is EX_WR of Port Address 008H.

If SCB = 1, this is EX_WR of Port Address 0D0H.

**Bit 12 - RO_PRI**, Rotating Priority

If SCB = 0, this is RO_PRI of Port Address 008H.

If SCB = 1, this is RO_PRI of Port Address 0D0H.

**Bit 11,** Reserved

**Bit 10 - CO_DIS**, Controller Disabled

If SCB = 0, this is CO_DIS of Port Address 008H.

If SCB = 1, this is CO_DIS of Port Address 0D0H.

**Bits 09:08 - TRA_MOD7**, Transfer Mode 7

TRA_MOD bits of register at Port Address 0D6H for DMA channel 7.

**Bit 07 - AD_DEC7,** Address Decrement 7

AD_DEC bit of register at Port Address 0D6H for DMA channel 7.

**Bit 06 - AUTO7**, Autoinitialize 7

AUTO bit of register at Port Address 0D6H for DMA channel 7.

**Bits 05:04 - TRA_TYP7,** Transfer Type 7

TRA_TYP bits of register at Port Address 0D6H for DMA channel 7.

**Bits 03:02 - TRA_MOD6**, Transfer Mode 6

TRA_MOD bits of register at Port Address 0D6H for DMA channel 6.

**Bit 01 - AD_DEC6,** Address Decrement 6

AD_DEC bit of register at Port Address 0D6H for DMA channel 6.

**Bit 00 - AUTO6**, Autoinitialize 6

AUTO bit of register at Port Address 0D6H for DMA channel 6.

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### 9.14.4 DMA Base Address and Count Register

When the SCB (bit 15 of DMA Shadow Register 3) is high, the DMA base address and base count can be read back from channels 0 through 7. When SCB is low, channels 0 through 7 represents the current address and current count.

### 9.14.5 Timer Count

When SCB (bit 15 of DMA Shadow Register 3) is high, the timer base count can be read back from registers at Port Addresses 040H:043H. When SCB is low, the registers at Port Addresses 040H:043H represents the timer current count. Refer to Sections 5.6 through 5.6.6

## 9.15 SUSPEND AND RESUME

When the WD7855/LV is in the Suspend Mode, it typically draws less than 500 µA. Figures 9-2 and 9-3 illustrate the steps that the WD7855/LV goes through during suspend and resume.

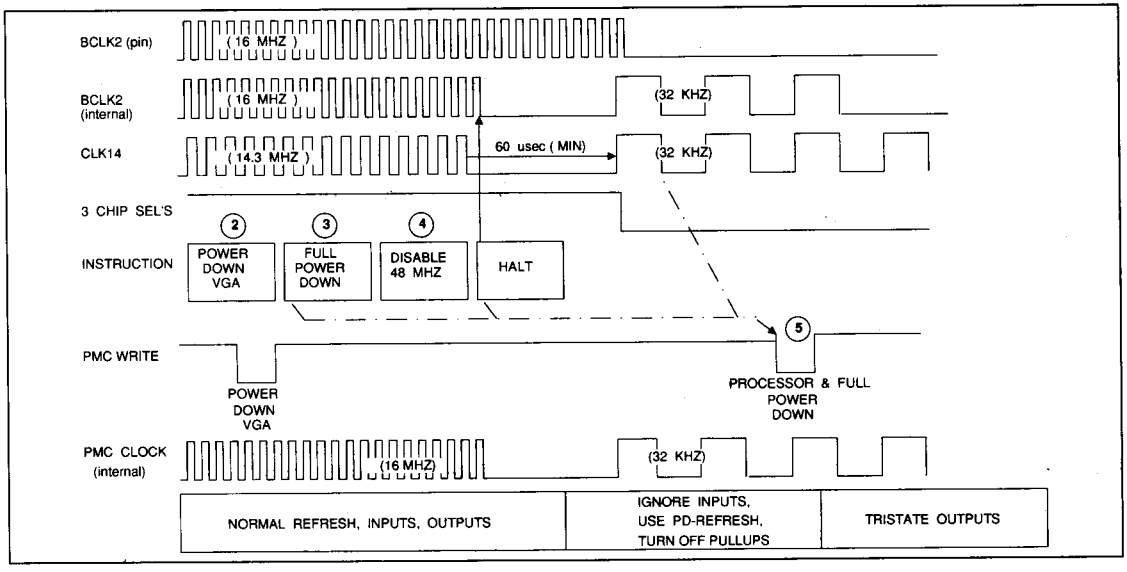


**FIGURE 9-2. SUSPEND**

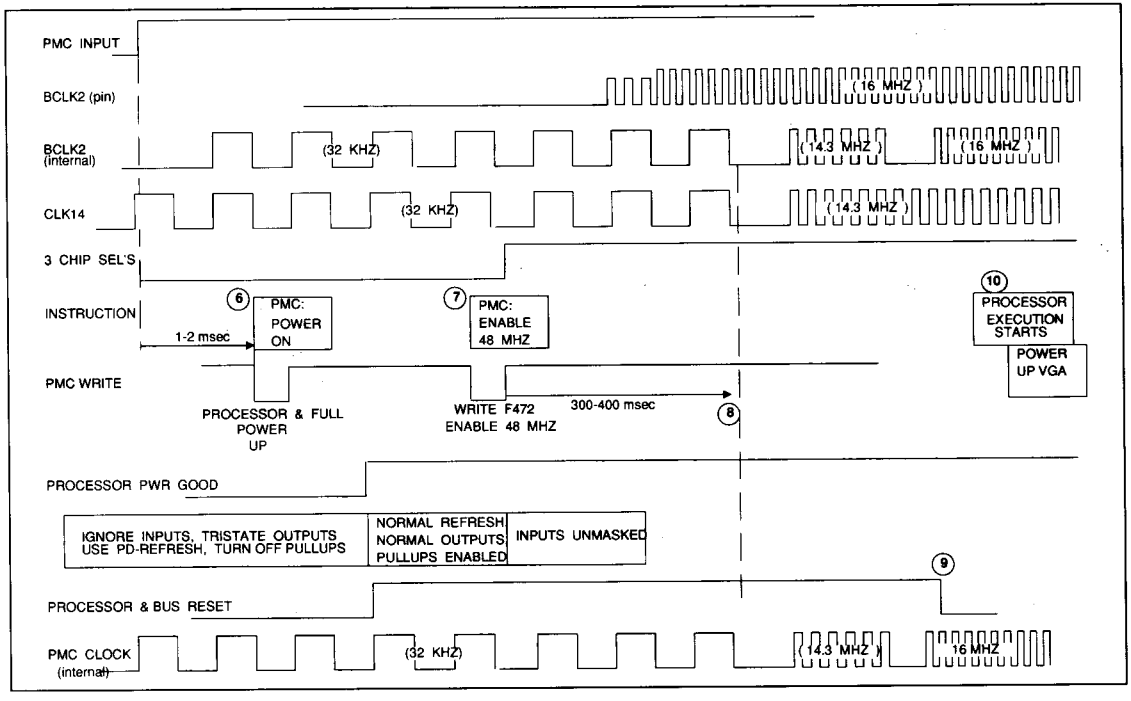


**FIGURE 9-3. RESUME**

### 9.15.1 Suspend/Resume Sequence

This section describes the suspend/resume sequence shown in Figures 9-2 and 9-3. It is an approach for a low power mode for the WD7855/LV chip set that offers the lowest power drain possible, but still allows the main system DRAM and video DRAM to be kept alive. This power-down mode requires specialized suspend/resume SMI Code software to control the operation. Figure 9-4 highlights the inter-connection within the chip set.

#### 9.15.1.1 Going into Suspend Mode

1. A change in the PMC input signals the WD7855/LV to generate either SMI or LCL_ATN. The processor vectors to the power-down routine and the processor saves its internal states and the states of the peripherals that are to be powered down. The processor saves the states into a protected area of the system DRAM.

2. The power-down routine writes to the full-power-down bit (FPD bit 13 at Port Address 1872H) which enables the power-down sequence. The WD7855/LV switches to sampling of the PMC inputs with the 14.318 MHz clock instead of the AT BUS clock.

3. The processor then writes to an I/O register in the WD7855/LV that switches a PMC output that is connected to the PWRDN input pin of the WD90C2X. Upon assertion of the PWRDN signal, the VGA controller enters the power-down mode which refreshes the video DRAM via the AT BUS REFRESH signal. CAS before RAS refresh is the preferred way of refreshing the DRAMs because it allows lower power operation without the generation of a DRAM refresh address.

4. The processor then writes to the Disable 48 MHz register (F072H) which sends a code of 15 to the WD7855/LV encoded chip select bus (ENCSBUS). The WD76C20 decodes this write and disables its 48 MHz oscillator, glitchlessly switches the 14.318 MHz oscillator signal to a 32 KHz, 50% duty cycle signal and then disables the 14.318 MHz oscillator. The WD76C20 also asserts the CSSERA, CSSERB and CSPAR signals simultaneously which signals the WD76C30A to disable its 48 MHz oscillator. When this oscillator is disabled, the AT BUS CLOCK, KEYBOARD CLOCK and 80287 CLOCK are disabled. The processor executes a halt instruction and the WD7855/LV detects the halt status from the processor and switches from the AT compatible refresh to the PDREF controlled refresh. The WD7855/LV then switches the AT bus compatible REFRESH output signal to reflect that of the PDREF input signal.

   The PDREF input is a CMOS level clock signal that has a 124 µs period and a low going pulse of 200 ns to 1 µs. This signal is always active and is adequate for refreshing low power DRAMs. This signal is generated by the WD76C20.

5. Upon detecting that the 14.318 MHz clock has been changed to 32 KHz, the WD7855/LV tristates all outputs except the PMC controls, DRAM controls, RAD bus and AT bus REFRESH signal. The CPURES signal is asserted and then tristated and is pulled high through a 200K pull-up resistor. All inputs except RSTIN, CLK14 and the PMC are ignored, and all circuitry except the PMC and refresh logic is stopped.

   The power is now turned off to the CPU, BUS, etc., by the assertion of the FULLPWDN PMC output from the WD7855/LV.

6. The processor-power-good PMC input must now go low in order for this state machine to start monitoring a resume condition as described in Section 9.15.1.2

#### 9.15.1.2 Coming Out Of Suspend Mode (Resume)

1. The WD7855/LV is now sampling the PMC inputs at 32 KHz. At this time, the change of any enabled PMC input causes the FULLPWDN PMC output described in step 5 to switch, which powers up the processor, bus etc. After 1 ms (timed from the 32 KHz clock input), the WD7855/LV samples the processor-power-good PMC input. When active the CPURES is driven high and the rest of the WD7855/LV control outputs are driven to their correct states, a BUS RESET is issued also.

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2. Upon detecting the power-good signal, the WD7855/LV state machine performs a write to the ENABLE 48 MHz register which sends a code of 16 on the ENCSBUS.

3. The WD76C20 receives the code, enables the 48 MHz and 14.318 MHz oscillators and de-asserts the CSSERA, CSSERB and CSPAR signals. After approximately 100 ms (enable time for the oscillators), the WD76C20 glitch-lessly switches the 32 KHz signal to 14.318 MHz.

4. The WD76C30A enables its 48 MHz oscillator upon the de-assertion of its CSSERA, CSSERB and CSPAR input signals.

5. When the WD7855/LV detects that the 32 KHz has been switched to 14.318 MHz, it switches the PMC sampling to the AT BUS CLOCK. The WD7855/LV then switches from the PDREF controlled refresh to the AT compatible refresh. The WD7855/LV also switches the AT bus REFRESH signal from the PDREF input to the AT compatible refresh rate. The WD7855/LV de-asserts the CPURESET signal and the processor comes out of reset and checks the shutdown status in the RTC RAM. This tells the processor that it is coming out of full-power-down mode as opposed to a warm or cold boot. The processor then restores the states of the machine.

6. The processor writes to the WD7855/LV register that causes the WD7855/LV to de-assert its PMC output. This output is connected to PWRDN input of the WD90C2X signaling the WD90C2X to come out of the power-down mode.

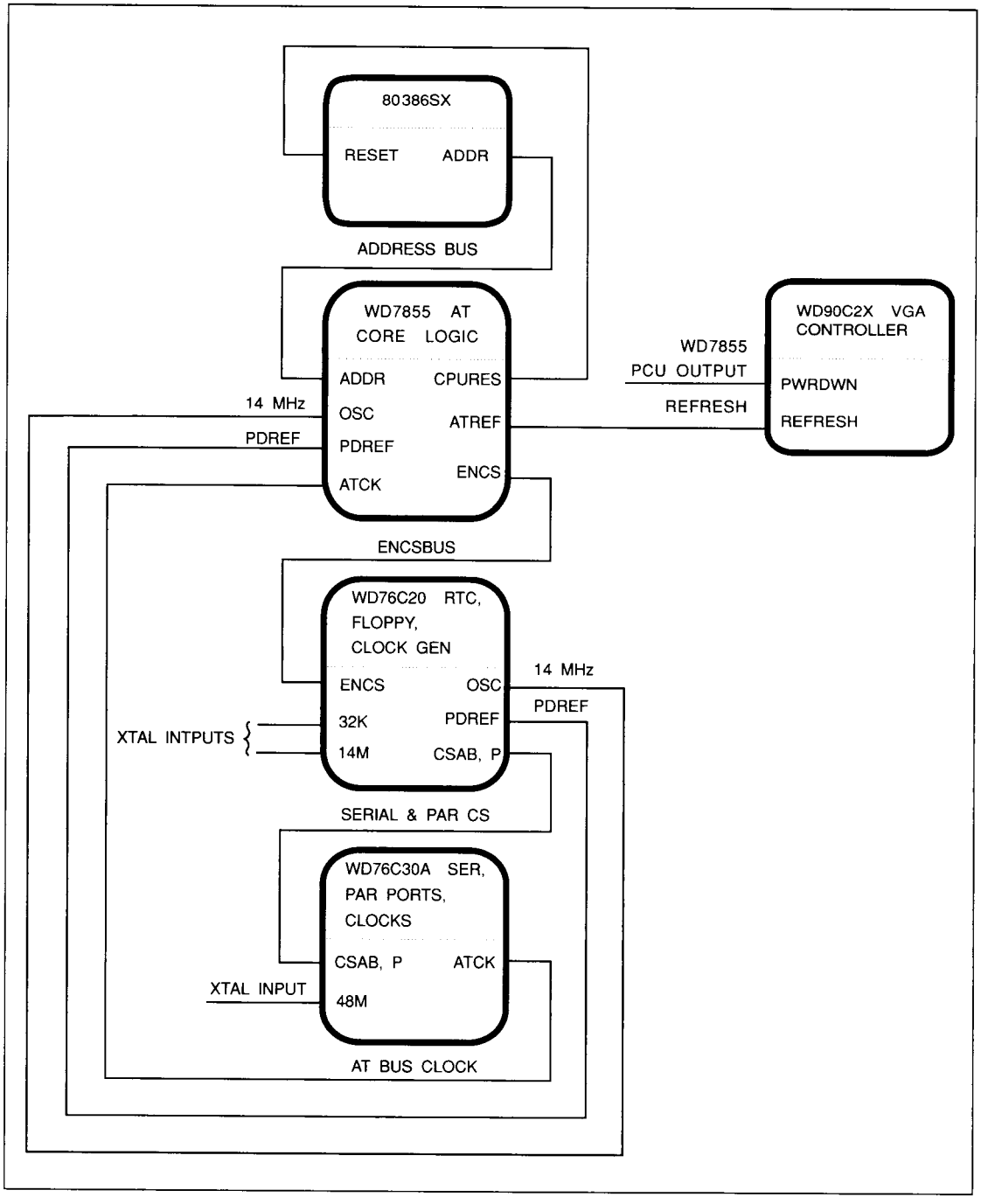


**FIGURE 9-4. FULL POWER-DOWN MODE SYSTEM BLOCK DIAGRAM**

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# 10.0 SYSTEM MANAGEMENT INTERRUPT (SMI)

## 10.1 I/O TRAPS

In order to conserve power, certain I/O peripherals can be put to sleep when they are not in use. To accomplish this in a transparent manner, hardware must intercept (trap) any accesses made to the sleeping device and wake it up before allowing the access to proceed. The System Controller can trap accesses to I/O devices controlled by the following chip selects:

- Programmable Chip Select 1
- Programmable Chip Select 2
- Programmable Chip Select 3
- Serial Port A Chip Select
- Serial Port B Chip Select
- Parallel Port Chip Select

When access to an I/O device is trapped, the System Controller asserts the $\overline{SMI}$ pin 108 to the CPU. Control is transferred to the SMI handler routine which determines which I/O access caused the SMI handler to be invoked. The handler looks at Registers 7C72H and 8472H to determine the I/O address accessed and how many bytes have been read or written. If the I/O access was unaligned, up to three I/O transfers may have taken place since SMI only breaks CPU execution on an instruction boundary. A memory write can also occur if the CPU is executing a string input instruction. If unaligned, the memory write can also involve up to three transfers.

Registers 8C72H and 9472H contain either the data written to the I/O device or the memory address written while trapping a string input instruction. Using this information allows the SMI handler to reconstruct the events causing the I/O trap. The handler can then wake up the I/O device, repeat the I/O instruction, rewrite memory if needed, and finally exit to allow normal code execution to continue.

The SMI handler is located in SMI RAM. SMI RAM consists of 64 Kbytes of DRAM space taken from the top of the DRAM space specified by Register 7472H. Once the SMI service routine is loaded into SMI RAM space, the SMI RAM space can be hidden from system access and remapped to SMI address space 6000:0H. The only way to access the SMI address space after remap is to put the CPU in SMI mode.

## 10.2 SMI I/O TRAP CONTROL REGISTER

Port Address 7C72H - Bits 15:08 Read and Write
Bit 07 Read and Clear
Bits 06:00 Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| LAEN | NAC_1:0 | | PCS TPE | PC2 TPE | SPA TPE | SPB TPE | PAR TPE |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| TRPS | IOWS | IOS_2:0 | | | MS_2:0 | | |

| Signal Name | Default At RSTIN |
|---|---|
| LAEN | 0 |
| NAC_1:0 | 0 |
| PCSTPE | 0 |
| SPATPE | 0 |
| PARTPE | 0 |

**Bit 15 - LAEN,** Local Attention Enable

There are three sources that can cause the Local Attention PMC output to be asserted. One is a transition on an unmasked PMC input pin (see description for Registers 8872H and C872H). The second is a signal from the system activity monitor (see description for Registers B072H and D872H). The third is a watch-dog timer. These sources will also cause an SMI if LAEN is set high. The SMI is based on an internal version of Local Attention and occurs even if PMC updates are disabled.

LAEN = 0 -
Disables generation of $\overline{SMI}$ by a Local Attention

LAEN = 1 -
Enables $\overline{SMI}$ to be caused by a Local Attention

**Bits 14:13 - NAC_(1:0),** Next Address Control 1:0

NAC_(1:0) control the function of the $\overline{NA}$ output at pin 125. These bits **must not** be changed while in SMI Mode.

| NAC1 | NAC0 | FUNCTION |
|---|---|---|
| 0 | 0 | $\overline{NA}$ is always deasserted, forcing all 80386SX cycles to be nonpipelined. |
| 0 | 1 | $\overline{NA}$ is always asserted, allowing the 80386SX to run pipelined whenever possible. |
| 1 | 0 | Reserved setting. Do not use. |
| 1 | 1 | $\overline{NA}$ is normally asserted allowing pipelined cycles. However, $\overline{NA}$ is de-asserted during T1P (pipelined cycle) or the first T2 (nonpipelined cycle) of all I/O cycles, except coprocessor cycles. $\overline{NA}$ is asserted again in the next T state unless SMI is active. This setting must be used if pipelining is allowed when I/O traps are enabled. |

**Bit 12 - PCSTPE,** Programmable Chip Select Trap Enable

PCSTPE, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Programmable Chip Select (See Registers 2872H and 3072H).

PCSTPE = 0 -
Disable Trap

PCSTPE = 1 -
Enable Trap

**Bit 11 - PC2TPE,** Programmable Chip Select 2 Trap Enable

PC2TPE, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the second programmable chip select (see Registers 5C72H and 6472H). This trap occurs even if the ENPCS2 bit in Register 5C72H is not set.

PC2TPE = 0 -
Disable Trap

PC2TPE = 1 -
Enable Trap

**Bit 10 - SPATPE,** Serial Port A Chip Select Trap Enable

SPATPE, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port A Chip Select (see Register 2072H).

SPATPE = 0 -
Disable Trap

SPATPE = 1 -
Enable Trap

**Bit 09 - SPBTPE,** Serial Port B Chip Select Trap Enable

SPBTPE, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port B Chip Select (see Register 2072H).

SPBTPE = 0 -
Disable Trap

SPBTPE = 1 -
Enable Trap

**Bit 08 - PARTPE,** Parallel Port Chip Select Trap Enable

PARTPE, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Parallel Port Chip Select (see Register 2072H).

PARTPE = 0 -
Disable Trap

PARTPE = 1 -
Enable Trap

**Bit 07 - TRPS,** Trap Status

When read as a 1, TRPS indicates an I/O trap has occurred. If read as a zero, no I/O trap has occurred. The SMI handler can poll this status bit to determine if an I/O trap caused the SMI. When SMI is written as a zero, the TRPS, IOWS, IOS2:0 and MS2:0 status bits are all reset to 0, readying the I/O trap state machines to capture future I/O and memory cycles. This should be done by the SMI handler each time it services an I/O trap. Writing a 1 to TRPS has no effect.

**Bit 6 - IOWS,** I/O Write Status

IOWS is set when the I/O cycle that caused the trap is a write operation. This tells the SMI handler that the contents of Registers 8C72H and 9472H hold the data that was written to the I/O device. This bit is cleared during reset or when a 0 is written to TRPS.

**Bits 5:3 - IOS2:0,** I/O Address Status 2:0

IOS2:0 provide information about the I/O Cycles captured by the I/O trap (See Table 10-1). This information, along with the I/O address of the first transfer stored in Register 8472H, can be used to reconstruct the complete sequence that may have occurred due to an unaligned transfer. These bits are cleared during reset or when a 0 is written to TRPS.

**Bits 2:0 - MS2:0,** Memory Address Status 2:0

MS2:0 provide information about memory write cycles, if any, captured by the I/O trap (See Table 10-2). Memory write cycles will only be captured if an indivisible string input instruction is being executed. The status information from MS2:0, along with the memory address of the first transfer stored in Registers 8C72H and 9472H, can be used to reconstruct the complete sequence that may have occurred due to an unaligned transfer. MS2:0 are cleared during reset or when a 0 is written to TRPS.

## 10.3 SMI I/O ADDRESS CAPTURE REGISTER

Port Address 8472H - Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| Captured I/O Address | | | | | | | |
| CIOA 15 | CIOA 14 | CIOA 13 | CIOA 12 | CIOA 11 | CIOA 10 | CIOA 09 | CIOA 08 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| Captured I/O Address | | | | | | | |
| CIOA 07 | CIOA 06 | CIOA 05 | CIOA 04 | CIOA 03 | CIOA 02 | CIOA 01 | CIOA 00 |

| Signal Name | Default At RSTIN |
|---|---|
| CIOA15:0 | 0 |

**Bits 15:0 - CIOA15:0,** Captured I/O Address

CIOA15:0 hold the I/O address being written or read which caused the I/O trap to occur. If multiple I/O cycles were required due to an unaligned transfer, then this is the first address and may need to be adjusted as discussed in the description of the ISO2:0 bits in Register 7C72H. These bits are cleared during reset or when a 0 is written to TRPS (Register 7C72H).

| IOS2 | IOS1 | IOS0 | BIT 0 OF 8472H | TRANSFER TYPE | ADJUSTMENT TO REG. 8472H TO OBTAIN ACTUAL I/O ADDRESS |
|---|---|---|---|---|---|
| 0 | 0 | 0 | X | None | Only occurs after a clear |
| 0 | 0 | 1 | X | 16-bit | No adjustment needed |
| 0 | 1 | 0 | X | 32-bit | No adjustment needed |
| 0 | 1 | 1 | X | 32-bit | Subtract 2 |
| 1 | 0 | 0 | X | 32-bit | Subtract 1 |
| 1 | 0 | 1 | X | 8-bit | No adjustment needed |
| 1 | 1 | 0 | 0 | 16-bit | Subtract 1 |
| 1 | 1 | 0 | 1 | 16-bit | No adjustment needed |
| 1 | 1 | 1 | X | 32-bit | Subtract 3 |
| X = Don't Care | | | | | |

**TABLE 10-1. I/O ADDRESS STATUS**

## 10.4 I/O DATA/MEMORY ADDRESS CAPTURE REGISTER LOW

Port Address 8C72H - Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| Memory Address or I/O Data | | | | | | | |
| MAID 15 | MAID 14 | MAID 13 | MAID 12 | MAID 11 | MAID 10 | MAID 09 | MAID 08 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| Memory Address or I/O Data | | | | | | | |
| MAID 07 | MAID 06 | MAID 05 | MAID 04 | MAID 03 | MAID 02 | MAID 01 | MAID 00 |

| Signal Name | Default At RSTIN |
|---|---|
| MAID15:0 | 0 |

**Bits 15:0 - MAID 15:0,** Memory Address or I/O Data Bits

MAID 15:0 holds 16 bits of either the memory address being written after $\overline{SMI}$ was asserted or the I/O data being written to the I/O address which caused the I/O trap to occur. The IOWS bit in Register 7C72H indicates the type of data. If IOWS is a 1, then this register holds data being written to the I/O device. If IOWS is 0, then this register holds the address of the memory being written, if any. This register is cleared during reset or when a 0 is written to TRPS (Register 7C72H).

When capturing the memory write address, this register holds the 16 least significant bits of the address of the first memory write cycle (Register 9472H holds the eight most significant bits). More cycles will be completed if the transfer was unaligned. Status bits MS2:0 in Register 7C72H show how many bytes were written and indicate how to adjust the captured address to get the actual address.

When capturing I/O write data, this register holds up to 16 bits of data, and Register 9472H holds the rest, if any. The data bytes may be stored in a jumbled order if it was an unaligned transfer. The format of the stored data bytes can be obtained from the IOS2:0 bits in Register 7C72H using Table 10-3.

| IOS2 | IOS1 | IOS0 | BIT 0 OF 8472H | TRANSFER TYPE | ADJUSTMENT TO REG. 8C72H AND 9472H TO OBTAIN ACTUAL MEMORY ADRESS |
|---|---|---|---|---|---|
| 0 | 0 | 0 | X | None | No memory write cycles occurred |
| 0 | 0 | 1 | X | 16-bit | No adjustment needed |
| 0 | 1 | 0 | X | 32-bit | No adjustment needed |
| 0 | 1 | 1 | X | 32-bit | Subtract 2 |
| 1 | 0 | 0 | X | 32-bit | Subtract 1 |
| 1 | 0 | 1 | X | 8-bit | No adjustment needed |
| 1 | 1 | 0 | 0 | 16-bit | Subtract 1 |
| 1 | 1 | 0 | 1 | 16-bit | No adjustment needed |
| 1 | 1 | 1 | X | 32-bit | Subtract 3 |
| X = Don't Care | | | | | |

**TABLE 10-2. MEMORY ADDRESS STATUS**

## 10.5 I/O DATA/MEMORY ADDRESS CAPTURE REGISTER HIGH

Port Address 9472H - Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| Memory Address or I/O Data | | | | | | | |
| MAID 31 | MAID 30 | MAID 29 | MAID 28 | MAID 27 | MAID 26 | MAID 25 | MAID 24 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| Memory Address or I/O Data | | | | | | | |
| MAID 23 | MAID 22 | MAID 21 | MAID 20 | MAID 19 | MAID 18 | MAID 17 | MAID 16 |

| Signal Name | Default At RSTIN |
|---|---|
| MAID31:16 . . . . . | 0 |

**Bits 15:0 - MAID 31:16,** Memory Address or I/O Data Bits

MAID 31:16 holds either 8 bits of the memory address being written after $\overline{SMI}$ is asserted; or the 16 bits of I/O data being written to the I/O address which caused the I/O trap to occur. The IOWS bit in Register 7C72H indicates the type of information. If IOWS is a 1, then this register holds data being written to the I/O device. If IOWS is 0, then this register holds the address of the memory being written, if any. This register is cleared during reset or when TRPS (Register 7C72H) is written with a 0.

When capturing the memory write address, MAID(23:16) holds the eight most significant bits of the address of the first memory write cycle (Register 8C72H holds the 16 least significant bits). More cycles will be done if the transfer is unaligned. Status bits MS(2:0) in Register 7C72H show how many bytes were written and indicate how to adjust the captured address to get the actual address.

When capturing I/O write data, this register holds 16 bits of data if it is a 32-bit I/O write. Register 8C72H holds the rest of the data. See Table 10-3.

| IOS2 | IOS1 | IOS0 | BIT 0 OF 8472H | DATA SIZE | REGISTER 9472H HI BYTE | REGISTER 9472H LO BYTE | REGISTER 8C72H HI BYTE | REGISTER 8C72H LO BYTE |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | X | None | | | | |
| 0 | 0 | 1 | X | 16-bit | | | B1 | B0 |
| 0 | 1 | 0 | X | 32-bit | B3 | B2 | B1 | B0 |
| 0 | 1 | 1 | X | 32-bit | B1 | B0 | B3 | B2 |
| 1 | 0 | 0 | X | 32-bit | B0 | B3 | B2 | B1 |
| 1 | 0 | 1 | 0 | 8-bit | | | - | B0 |
| 1 | 0 | 1 | 1 | 8-bit | | | B0 | - |
| 1 | 1 | 0 | X | 16-bit | | | B0 | B1 |
| 1 | 1 | 1 | X | 32-bit | B2 | B1 | B0 | B3 |

Where:
B0 = least significant byte
B1 = next most significant byte (MSB for 16-bit data)
B2 = next most significant byte (32-bit data only)
B3 = most significant byte (32-bit data only)
X = Don't Care

**TABLE 10-3. DATA FORMAT DESCRIPTION**

## 10.6 SMI I/O TIMEOUT

As a power conservation measure, it is desirable to put some I/O peripherals in the Sleep Mode when they are not in use. This may involve shutting off clocks or removing power. In order to do this, there must be a mechanism for determining that a device is not in use. In the System Controller, timers are included for each I/O device that is a candidate for power reduction measures. Each timer causes an $\overline{SMI}$ when no access is made to an I/O device for a programmable amount of time. The timers are reset by I/O read or write operations to any address which falls within the range of its chip select.

When an $\overline{SMI}$ is generated, the SMI handler takes whatever action is appropriate to power down the I/O peripheral. The handler then enables the I/O trap for that device so that it can be awakened the next time it is accessed.

## 10.7 SMI I/O TIMEOUT CONTROL REGISTER

Port Address 9C72H - Bits 15, 04:00 Read and Write
Bits 14:05 Read only

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| FSMI | PCS ADS | PC2 ADS | SPA ADS | SPB ADS | PAR ADS | PCS TOS | PC2 TOS |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| SPA TOS | SPB TOS | PAR TOS | PCS TOE | PC2 TOE | SPA TOE | SPB TOE | PAR TOE |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - FSMI**, Force $\overline{SMI}$

FSMI provides a means to invoke the SMI handler through software. When this bit is set to 1, the $\overline{SMI}$ pin 108 is asserted. FSMI should be cleared by the SMI handler before it exits to prevent another $\overline{SMI}$.

FSMI = 0 -
Force $\overline{SMI}$ Disable

FSMI = 1 -
Force $\overline{SMI}$ Enable

**Bit 14 - PCSADS,** Programmable Chip Select Activity Detect Status

PCSADS can be polled by the SMI handler to determine if the programmable chip select I/O address range has been accessed since PCSTOS was set. If PCSADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PCSADS is cleared by reset or when PCSTOE is cleared.

**Bit 13 - PC2ADS,** Programmable Chip Select 2 Activity Detect Status

PC2ADS can be polled by the SMI handler to determine if the second Programmable Chip Select's I/O address range has been accessed since PC2TOS was set. If PC2ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PC2ADS is cleared by reset or when PC2TOE is cleared.

**Bit 12 - SPAADS,** Serial Port A Chip Select Activity Detect Status

SPAADS can be polled by the SMI handler to determine if the Programmable Chip Select's I/O address range has been accessed since SPATOS was set. If SPAADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPAADS is cleared by reset or when SPATOE is cleared.

**Bit 11 - SPBADS,** Serial Port B Chip Select Activity Detect Status

SPBADS can be polled by the SMI handler to determine if the Programmable Chip Select's I/O address range has been accessed since SPBTOS was set. If SPBADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPBADS is cleared by reset or when SPBTOE is cleared.

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**Bit 10 - PARADS,** Parallel Port Chip Select Activity Detect Status

PARADS can be polled by the SMI handler to determine if the programmable chip select I/O address range has been accessed since PARTOS was set. If PARADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PARADS is cleared by reset or when PARTOE is cleared.

**Bit 09 - PCSTOS,** Programmable Chip Select Timeout Status

PCSTOS can be polled by the SMI handler to determine the source of the SMI. PCSTOS is set when an I/O access timeout has occurred for the Programmable Chip Select I/O address range. PCSTOS is cleared by reset or when PCSTOE is cleared.

**Bit 08 - PC2TOS,** Programmable Chip Select 2 Timeout Status

PC2TOS can be polled by the SMI handler to determine the source of the SMI. PC2TOS is set when an I/O access timeout has occurred for the second Programmable Chip Select I/O address range. PC2TOS is cleared by reset or when PC2TOE is cleared.

**Bit 07 - SPATOS,** Serial Port A Chip Select Timeout Status

SPATOS can be polled by the SMI handler to determine the source of the SMI. SPATOS is set when an I/O access timeout has occurred for the Serial Port A Chip Select I/O address range. SPATOS is cleared by reset or when SPATOE is cleared.

**Bit 06 - SPBTOS,** Serial Port B Chip Select Timeout Status

SPBTOS can be polled by the SMI handler to determine the source of the SMI. SPBTOS is set when an I/O access timeout has occurred for the Serial Port B Chip Select's I/O address range. SPBTOS is cleared by reset or when SPBTOE is cleared.

**Bit 05 - PARTOS,** Parallel Port Chip Select Timeout Status

PARTOS can be polled by the SMI handler to determine the source of the SMI. PARTOS is set when an I/O access timeout has occurred for the Parallel Port Chip Select I/O address range. PARTOS is cleared by reset or when PARTOE is cleared.

**Bit 04 - PCSTOE,** Programmable Chip Select Timeout Enable

PCSTOE = 0 -
Programmable Chip Select Timeouts disabled and PCSTOS cleared.

PCSTOE = 1 -
I/O access timeout for the Programmable Chip Select I/O address range enabled.

**Bit 03 - PCSTOE,** Programmable Chip Select 2 Timeout Enable

PCSTOE = 0 -
Programmable Chip Select 2 timeouts disabled and PC2TOS cleared.

PCSTOE = 1 -
I/O access timeout for the second Programmable Chip Select I/O address range enabled.

**Bit 02 - SPATOE,** Serial Port A Chip Select Timeout Enable

SPATOE = 0 -
Serial Port A Chip Select timeouts disabled and SPATOS cleared.

SPATOE = 1 -
I/O access timeout for the Serial Port A Chip Select I/O address range enabled.

**Bit 01 - SPBTOE,** Serial Port B Chip Select Timeout Enable

SPBTOE = 0 -
Serial Port B Chip Select timeouts disabled and SPBTOS cleared.

SPBTOE = 1 -
I/O access timeout for the Serial Port B Chip Select I/O address range enabled.

**Bit 00 - PARTOE,** Parallel Chip Select Timeout Enable

PARTOE = 0 - Parallel Port Chip Select timeouts disabled and PARTOS cleared.

PARTOE = 1 - I/O access timeout for the Parallel Port Chip Select I/O address range enabled.

## 10.8 SMI I/O TIMEOUT COUNT REGISTER 1

Port Address A472H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| SMI WUE | PCS TC4 | PCS TC3 | PCS TC2 | PCS TC1 | PCS TC0 | PC2 TC4 | PC2 TC3 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PC2 TC2 | PC2 TC1 | PC2 TC0 | SPA TC4 | SPA TC3 | SPA TC2 | SPA TC1 | SPA TC0 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - SMIWUE,** SMI Wake Up Enable

SMIWUE, when set to 1, causes the assertion of SMI to wake up the processor from a power-down or stop clock state. An INTR, NMI, or DMA request continues to wake up the processor as in the WD76C10A, regardless of the state of this bit. Note that setting SMIWUE does not enable SMI to initiate a resume from suspend.

SMIWUE = 0 -
Disable SMI Wakeup

SMIWUE = 1 -
Enable SMI Wakeup

**Bits 14:10 - PCSTC 4:0**, Programmable Chip Select Timeout Count

PCSTC 4:0, along with the timeout clock select PCSTCS (Register AC72H), determine the time period during which an I/O peripheral, selected by the Programmable Chip Select, must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PCSTCS = 0 -
(Count in PCSTC4:0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PCSTCS = 1 -
(Count in PCSTC4:0) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

**Bits 09:05 - PC2TC 4:0,** Programmable Chip Select 2 Timeout Count

PC2TC 4:0, along with the timeout clock select PC2TCS (Register AC72H), determine the time period during which an I/O peripheral, selected by Programmable Chip Select 2, must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PC2TC = 0 -
(Count in PC2TC4:0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC2TC = 1 -
(Count in PC2TC4:0) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

**Bits 4:0 - SPATC4:0,** Serial Port A Chip Select Timeout Count

SPATC4:0, along with the timeout clock select SPATCS (Register AC72H), determine the time period during which Serial Port A must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

SPATCS = 0 -
(Count in SPATC4:0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPATCS = 1 -
(Count in SPATC4:0) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

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## 10.9 SMI I/O TIMEOUT COUNT REGISTER 2

Port Address AC72H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| IOT CTM | SPB TC4 | SPB TC3 | SPB TC2 | SPB TC1 | SPB TC0 | PAR TC4 | PAR TC3 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PAR TC2 | PAR TC1 | PAR TC0 | PCS TCS | PC2 TCS | SPA TCS | SPB TCS | PAR TCS |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - IOTCTM,** I/O Timeout Counter Test Mode

IOTCTM is for factory use only. When = 1, the timeout counters are placed into test mode.

**Bits 14:10 - SPBTC4:0,** Serial Port B Chip Select Timeout Count

SPBTC4:0, along with the timeout clock select SPBTCS (Register AC72H), determine the time period during which Serial Port B must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

SPBTCS = 0 -
(Count in SPBTC4:0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPBTCS = 1 -
(Count in SPBTC4:0) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

**Bits 09:05 - PARTC4:0,** Parallel Port Chip Select Timeout Count

PARTC4:0, along with the timeout clock select PARTCS (Register AC72H), determine the time period during which the parallel port must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PARTCS = 0 -
(Count in PARTC4:0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PARTCS = 1 -
(Count in PARTC4:0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

**Bit 04 - PCSTCS,** Programmable Chip Select Timeout Clock Select

PCSTCS selects the clock to be used for the Programmable Chip Select Timeout Counter.

PCSTCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

PCSTCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PCSTC4:0 (Register A472H) for more details.

**Bit 03 - PC2TCS,** Programmable Chip Select 2 Timeout Clock Select

PC2TCS selects the clock to be used for the second Programmable Chip Select Timeout Counter.

PC2TCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

PC2TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PC2TC4:0 (Register A472H) for more details.

**Bit 02 - SPATCS,** Serial Port A Chip Select Timeout Clock Select

SPATCS selects the clock to be used for the Serial Port A Timeout Counter.

SPATCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

SPATCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPATC4:0 (Register A472H) for more details.

**Bit 01 - SPBTCS,** Serial Port B Chip Select Timeout Clock Select

SPBTCS selects the clock to be used for the Serial Port B Timeout Counter.

SPBTCS = 0 -
A high-speed clock is used to obtain 4-second timing resolution for timeout periods of 2 minutes or less.

SPBTCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPBTC4:0 (Register A472H) for more details.

**Bit 00 - PARTCS,** Parallel Port Chip Select Timeout Clock Select

PARTCS selects the clock to be used for the Parallel Port Timeout Counter.

PARTCS = 0 -
A high-speed clock is used to obtain 4-second timing resolution for timeout periods of 2 minutes or less.

PARTCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PARTC4:0 (Register A472H) for more details.

## 10.10 SMI AUXILIARY CONTROL REGISTER

Port Address 5472H - Bits 15, 13, 11:08, 05:00 Read and Write
Bits 07:06 Read only
Bit 12 Read and clear

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| TOM SK | | WDO GEN | WDO GST | PCS 3M | PCS 2M | PC3 TPE | PC3 TOE |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PC3 TOS | PC3 ADS | PC3 TC4 | PC3 TC3 | PC3 TC2 | PC3 TC1 | PC3 TC0 | PC3 TCS |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - TOMSK**, Timeout Mask

When set to one, TOMSK masks I/O device timeouts from causing assertion of the SMI output. If enabled, the I/O device timers continue to count down. If a timeout occurs, the SMI output is asserted after TOMSK is cleared. Also, when TOMSK is set, the I/O device timers will not detect I/O activity, thus preventing the timer from being reset.

**Bit 14 -** Reserved

**Bit 13 - WDOGEN,** Watchdog Timer Interrupt Enable

WDOGEN = 0 -
The interrupt is cleared either by writing a zero to WDOGST or WDOGEN to disable further watchdog interrupts. Note that the first interrupt after the watchdog timer is enabled can occur anytime from 62.5 ms to 125 ms later.

WDOGEN = 1 -
Enables a periodic interrupt to be generated every 125 ms. Each interrupt causes LCL_ATN to be set, so that it is useful both with or without SMI support.

10

**Bit 12 - WDOGTS,** Watchdog Timer Interrupt Status

When WDOGTS equals 1, LCL_ATN has been set due to a Watchdog Timer Interrupt Request. WDOGST is cleared by writing a zero to it. The watchdog timer continues to run and will set WDOGST at 125 ms intervals. WDOGST is also cleared when WDOGEN is set to a zero. Writing a 1 to WDOGST has no effect.

**Bit 11 - PCS3M,** Programmable Chip Select 3 Mask

PCS3M is an extension to the register at Port Address D872H.

PCS3M = 0 -
I/O accesses to the third Programmable Chip Select address range (see registers at Port Address 5C72H and 6C72H) may be observed as a source of activity by the system activity monitor.

PCS3M = 1 -
I/O accesses to the third Programmable Chip Select are masked from being seen by the system activity monitor. Note that the setting of ENPCS3 in the register at Port Address 5C72H has no effect on I/O activity detection.

**Bit 10 - PCS2M,** Programmable Chip Select 2 Mask

PCS2M is an extension to Register D872H.

PCS2M = 0 -
I/O accesses to the second Programmable Chip Select address range (see registers at Port Address 5C72H and 6472H) are allowed to be observed as a source of activity by the system activity monitor.

PCS2M = 1 -
I/O accesses to the second Programmable Chip Select are masked from being seen by the system activity monitor. Note that the setting of ENPCS2 in the register at Port Address 5C72H has no effect on I/O activity detection.

**Bit 09 - PC3TPE,** Programmable Chip Select 3 Trap Enable

PC3TPE = 0 -
Trap not enabled

PC3TPE = 1 -
An I/O trap will occur whenever an I/O read or write occurs at an address within the range covered by the third Programmable Chip Select (see registers at Port Address 5C72H and 6C72H). This trap occurs even if the ENPCS3 bit in the register at Port Address 5C72H is not set.

**Bit 08 - PC3TOE,** Programmable Chip Select 3 Timeout Enable

PC3TOE = 0 -
Programmable Chip Select 3 timeouts are disabled and PC3TOS cleared.

PC3TOE = 1 -
I/O access timeout for the third Programmable Chip Select I/O address range are enabled. The timeout count will be reset by I/O to the Programmable Chip Select 3 address range even if the ENPCS3 bit in Register 5C72H is not set.

**Bit 07 - PC3TOS,** Programmable Chip Select 3 Timeout Status

PC3TOS is set to 1 when an I/O access timeout has occurred for the third Programmable Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PC3TOS is cleared by reset or when PC3TOE is cleared.

**Bit 06 - PC3ADS,** Programmable Chip Select 3 Activity Detect Status

PC3ADS can be polled by the SMI Handler to see if the third Programmable Chip Select I/O address range has been accessed since PC3TOS was set. If PC3ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI Handler would ignore the timeout and restart the timeout counter. PC3ADS is cleared by reset or when PC3TOE is cleared.

**Bit 05:01 - PC3TC4:0,** Programmable Chip Select 3 Timeout Count

PC3TC4:0, along with the timeout clock select PC3TCS, determine the time period during which an I/O peripheral (selected by Programmable Chip Select 3) must not be accessed in order to be considered inactive. The timeout setting is determined as follows:

PC3TCS = 0 -
(Count in PC3TC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC3TCS = 1 -
(Count in PC3TC4-0) x 40 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

**Bit 00 - PC3TCS,** Programmable Chip Select 3 Timeout Clock Select

PC3TCS selects the clock to be used for the third Programmable Chip Select timeout counter.

PC3TCS = 0 -
A high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less.

PC3TCS = 1 -
A low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PC3TC4:0 for more details.

## 10.11 PROGRAMMABLE CS2 AND CS3 CONTROL REGISTER

Port Address 5C72H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| PCS 2L | ENP CS2 | UMS K2 | 2LM SK4 | 2LM SK3 | 2LM SK2 | 2LM SK1 | 2LM SK0 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PCS 3L | ENP CS3 | UMS K3 | 3LM SK4 | 3LM SK3 | 3LM SK2 | 3LM SK1 | 3LM SK0 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bit 15 - PCS2L**, Programmable Chip Select 2 Location

PCS2L = 0 -
The device is located on the RA0:7/ED0:7 bus.

PCS2L = 1 -
The I/O device selected by the second Programmable Chip Select is located on the expansion bus.

**Bit 14 - ENPCS2,** Enable Programmable Chip Select 2

ENPCS2 = 0 -
The second Programmable Chip Select is not enabled.

ENPCS2 = 1 -
The second Programmable Chip Select is enabled.

**Bit 13 - UMSK2,** Upper Address Bits Mask 2

UMSK2 = 0 -
Bits A15:10 from the register at Port Address 6472H are ignored.

UMSK2 = 1 -
A15:10 from the register at Port Address 6472H are compared against CPU address Bits 15:10 when qualifying the second programmable chip select.

10

**Bits 12:08 - 2LMSK4:0,** Programmable CS2 Lower Address Bits MASK4:0

2LMSK4:0 bits allow individual qualification of the lower five address bits in the register at Port Address 6472H.

2LMSK4:0 = 0 -
The corresponding bit in the register at Port Address 6472H is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (2LMSK4:0 would all be zeroes), as well as unusual requirements such as odd addresses only.

2LMSK4:0 = 1 -
The corresponding bit in the register at Port Address 6472H is compared against that CPU address bit.

**Bit 07 - PCS3L,** Programmable Chip Select 3 Location

PCS3L = 0 -
The device is located on the RA0:7/ED0:7 bus.

PCS3L = 1 -
The I/O device selected by the third Programmable Chip Select is located on the expansion bus.

**Bit 06 - ENPCS3,** Enable Programmable Chip Select 3

ENPCS3 = 0 -
The third Programmable Chip Select is not enabled.

ENPCS3 = 1 -
The third Programmable Chip Select is enabled.

**Bit 05 - UMSK3,** Upper Address Bits Mask 3

UMSK3 = 0 -
Bits A15:10 are ignored.

UMSK3 = 1 -
A15:10 from the register at Port Address 6C72H are compared against CPU address bits 15:10 when qualifying the third Programmable Chip Select.

**Bits 04:00 - 3LMSK4:0,** Programmable CS3 Lower Address Bits Mask

3LMSK4:0 allow individual qualification of the lower five address bits in the register at Port Address 6C72H.

3LMSK4:0 = 0 -
The corresponding bit in the register at Port Address 6C72H is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (3LMSK4:0 would all be zeroes), as well as unusual requirements such as odd addresses only.

3LMSK4:0 = 1 -
The corresponding bit in the register at Port Address 6C72H is compared against that CPU address bit.

## 10.12 PROGRAMMABLE CS2 ADDRESS REGISTER

Port Address 6472H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| PC2 A15 | PC2 A14 | PC2 A13 | PC2 A12 | PC2 A11 | PC2 A10 | PC2 A9 | PC2 A8 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PC2 A7 | PC2 A6 | PC2 A5 | PC2 A4 | PC2 A3 | PC2 A2 | PC2 A1 | PC2 A0 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 15:00 - PC2A15:00**, Programmable Chip Select 2 Address

PC2A15:00 determine the base address of the I/O device corresponding to the second programmable chip select. The register at Port Address 5C72H provides the enable for Programmable Chip Select 2 and allows selective masking of some of the address bits.

## 10.13 PROGRAMMABLE CS3 ADDRESS REGISTER

Port Address 6C72H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| PC3 A15 | PC3 A14 | PC3 A13 | PC3 A12 | PC3 A11 | PC3 A10 | PC3 A9 | PC3 A8 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| PC3 A7 | PC3 A6 | PC3 A5 | PC3 A4 | PC3 A3 | PC3 A2 | PC3 A1 | PC3 A0 |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 15:00 - PC3A15:00,** Programmable Chip Select 3 Address

PC3A15:00 determine the base address of the I/O device corresponding to the third Programmable Chip Select. The register at Port Address 5C72H provides the enable for Programmable Chip Select 3 and allows selective masking of some of the address bits.

# 11.0 DIAGNOSTIC MODE

Two testing modes are provided for board testing. One chip test mode is provided for leakage testing.

### Tristate Output Mode

Simultaneously asserting MASTER, MEMR and MEMW with A1 and A2 low while RSTIN is asserted, causes all output pins to become tristated. The outputs remain tristated if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted and any of the MASTER, MEMR or MEMW are not asserted. The output tristate mode allows an in-circuit board tester to drive the System Controller's output pins.

### I/O Pin Mapping Mode

The I/O Pin Mapping Mode provides the in-circuit tester for evaluating the connectivity of the WD7855/LV to the printed circuit board. Simultaneously asserting MASTER, MEMR, MEMW when A1 is high, A2 is low, and RSTIN is asserted, causes the WD7855/LV to switch to I/O Mapping Mode. The WD7855/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR, and MEMW are asserted.

### Full Tristate Mode

Simultaneously asserting MASTER, MEMR, and MEMW with A1 low and A2 high while RSTIN is asserted, causes all the output pins of the WD7855/LV to tristate and disables all the pullup and pulldown resistors. The WD7855/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with either MASTER, MEMR or MEMW de-asserted. This allows the tester to test for leakage current of the device.

### Pullup and Pulldown Test Mode

Simultaneously asserting MASTER, MEMR, MEMW with A1 and A2 high while RSTIN is asserted, causes all the output pins of the WD7855/LV to become tristated and enables all the pullup and pulldown resistors. The WD7855/LV stays in this mode if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted while either MASTER, MEMR or MEMW is de-asserted. This allows the tester to test the pullup and pulldown resistors of the device.

## 11.1 DIAGNOSTIC REGISTER

Port Address 9872H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| Reserved | | | CLK_TST | REF_MAS | AUT_20 | | CLK SW |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| SX | DS | DIAG | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| Reserved | None |
| CLK_TST | 0 |
| REF_MAS | 0 |
| AUT_A20 | 0 |
| Bit 09 | None |
| CLK_SW | 0 |
| SX | None |
| DS | 0 |
| DIAG | 0 |

**Bits 15:13,** Reserved

**Bit 12 - CLK_TST,** Clock Test

Diagnostics for factory use only.

**Bit 11 - REF_MAS**, Bus Master Refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh.

REF_MAS = 1 -
Supports bus master initiated refresh.

**Bit 10 - AUT_A20,** Automatic Gate A20

Normally, the Alternate Gate A20 signal from Port 092H is OR'ed with the 8042 Gate A20.

When the AUT_A20 bit is set, the Alternate Gate A20 control bit automatically changes

state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of Port 092H is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 status bit is replaced by that of AUT_A20.

The state of the A20 gating signal is available on PMC output 6 by reading Port 7072H (see Table 9-1).

AUT_A20 = 0 -
Normal Alternate Gate A20

AUT_A20 = 1 -
Automatic Gate A20

**Bit 09 -** Not used, state is ignored.

**Bit 08 - CLK_SW,** Clock Switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs. The 80486 processor requires a 1 ms clock switch. (See Section 4.2.3)

CLK_SW = 0 -
Short clock switch reset width

CLK_SW = 1 -
1 ms clock switch reset width

**Bit 07 - SX,** 80386SX Processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

**Bit 06 - DS,** Diagnostic Signal

DS represents the state of the diagnostic signal selected by DIAG.

**Bits 05:00 - DIAG,** Diagnostic Function/Speaker Disable

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected.

DIAG = 000000 - Diagnostic output disabled, speaker normal.

DIAG = 000001 - Diagnostic output disabled, speaker disabled. This is a method of disabling the speaker without hardware gates.

DIAG = 000010:111111 - Reserved

## 11.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| LAT | DL | DELAY | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| Bits 15:08 | None |
| LAT | 0 |
| DL | 0 |
| DELAY | None |

**Bit 07 - LAT,** Latch Output Strength

The delay line count value (bits 05:00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

**Bit 06 - DL,** Delay Freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05:00.

DL = 0 -
Normal delay line operation

DL = 1 -
Freeze delay line

10

**Bits 05:00 - DELAY**, Delay Counter Value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL (bit 06) is set to one.

### 11.3 TEST ENABLE REGISTER

Port Address A872H - Bits 15:10 Read only
Bits 09:00 Read and Write

The test function bits 07:03 are for factory use only.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| SVER | | | | BF40 | BC40 | IRQ9_EN | TDL |

| 07 | 06 | 055 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| OLD_HLDA | BFC 3 | BIST 3 | BFC40 | BIST 40 | EN_PLD | DIS FA | EN_LVL |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | 0 |

**Bits 15:12 - SVER,** Secondary Version Number.

| DEVICE PORT ADDRESS D472H | | | SECONDARY VERSION PORT ADDRESS A872H | | | | |
|---|---|---|---|---|---|---|---|
| 14 | 13 | Device | 15 | 14 | 13 | 12 | Rev |
| 0 | 0 | WD76C10 | 0 | 0 | 0 | 0 | A |
| 0 | 1 | WD7710/7910 | 0 | 0 | 0 | 1 | B |
| 1 | 0 | WD7855 | 0 | 0 | 1 | 0 | C |
| 1 | 1 | Reserved | - | - | - | - | - |
| | | | 1 | 1 | 1 | 1 | P |

**TABLE 11-1. EXTENDED VERSION NUMBER**

**Bit 11 - BF40,** EMS Register Self Test Status

**Bit 10 - BC40,** EMS Register Self Test Status

**Bit 09 - IRQ9EN**, IRQ9 Enable

IRQ9EN is used to mask IRR9 and ISR9 so that the System Activity Monitor does not detect these signals. This prevents vertical retrace from being a source of activity for SAM.

IRQ9EN = 0 -
Masking of IRR9 and ISR9 enabled

IRQ9EN = 1
Masking disabled

**Bit 08 - TDL,** Test Delay Line.

**Bit 07 - OLD_HLDA,**

Test bit for factory use only. Must be set to 0.

**Bit 06 - BFC3,**

DMA Register file test bit, for factory use only. Must be set to 0.

**Bit 05 - BIST3,**

DMA Register file test bit, for factory use only. Must be set to 0.

**Bit 04 - BFC40,**

EMS Mapping RAM test bit, for factory use only. Must be set to 0.

**Bit 03 - BIST40,**

EMS Mapping RAM test bit, for factory use only. Must be set to 0.

**Bit 02 - EN_PLD,** Enable Pulldown

EN_PLD = 0 -
Pulldown resistors are not enabled.

EN_PLD = 1 -
40K to 100K internal pulldown resistors will be enabled during processor power down or full power down on processor address lines A23:00, and on processor data lines D15:00.

**Bit 01 - DISFA,** Disable First Access

DISFA should be set to 1 when any of the following conditions are true:

1. 33 MHz operation.

2. External lookaside cache mode enabled (Port Address 3872H bits 13 and 12 = 01).

3. Whenever an odd number of memory banks of equal size are enabled, i.e. 3 banks of 512K X 9 memory.

DISFA = 0 -
First access Page Mode cycles are not disabled.

DISFA = 1 -
First access Page Mode cycles are disabled. Page Miss cycles occur instead.

**Bit 00 - EN_LVL,** Enable Level

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability. See Section 5.5.2.1.

EN_LVL = 0 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is not supported. L_T (bit 3) at Port 020H has no effect.

EN_LVL = 1 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is supported. L_T (BIT 3) at Port 020H now controls the selection of edge-sensed or level-sensed interrupts.

## 11.4 TEST STATUS REGISTER

Port Address DC72H - Read only
For factory use only.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| Delay Line Status CAL MED SLOW | | | DLT6 | DLT5 | DLT4 | DLT3 | DLT2 |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| DLT1 | DLR0 | BF34 | BF33 | BF32 | BF31 | BF30 | BC |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

**Bit 15 - CAL,** Calibration

CAL = 0 -
Internal delay line has not completed initial calibration.

CAL = 1 -
Internal delay line has completed initial calibration.

**Bits 14:13 - MED, SLOW,** Medium and Slow

These bits provide information regarding the output buffer strength.

| MED | SLOW | |
|---|---|---|
| 0 | 0 | Output buffers are set to low strength (fast WD7855/LV). |
| 0 | 1 | Invalid |
| 1 | 0 | Output buffers are set to medium strength (medium speed WD7855/LV). |
| 1 | 1 | Output buffers are set to full strength (slow WD7855/LV). |

**Bits 12:06 - DLT6:DLT0,**

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7855/LV.

**Bits 05:01 - BF34:BF30,**

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7855/LV.

**Bit 00 - BC**

This bit provides information about internal nodes and are for test purposes only. Its state is dependent upon the test mode selected and the speed of the WD7855/LV.

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# 12.0 DC ELECTRICAL SPECIFICATIONS

This section provides the DC Operating Characteristics for the WD7855. The parameters for the WD7855LV that differ from these are marked with an * and appear in the appendix.

## 12.1 MAXIMUM RATINGS

Supply Voltage ($V_{DD}$) with respect to Vss (ground) . . . . . $V_{DD}$ - Vss ≤ 7.0 Volts
Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to $V_{DD}$ +0.3 Volts
Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)
Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)
Power Dissipation . . . . . 600 mW *

**NOTE**

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

Pins 84:101 pass ESD at 700V, all others pass at 2000V.

## 12.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
$V_{DD}$AT = +5V ±.25V (5%) for WD7855 *
$V_{DD}$ = +5V ±.25V (5%) *

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Leakage | | ± 10 | µA | Vin = .4 to $V_{DD}$ |
| IOZ | Tristate and Open Drain Output Leakage | | ± 10 | mA | Vout = .4 to $V_{DD}$ |
| VIH | Input High Voltage | 2.0 | | V | |
| VIL | Input Low Voltage | | .8 | V | |
| VIHC | CPUCLK Input High * | 3.6 | | V | |
| VIL | CPUCLK Input Low | | .6 | V | |
| VIH | $\overline{RSTIN}$ Input High Voltage | $V_{DD}$ -0.5 | | V | |
| VIL | $\overline{RSTIN}$ Input Low Voltage | | 0.5 | V | |
| ICC | Supply Current * | | 200 | mA | Inputs at 2.0V |
| | | | 140 | mA | Inputs at 5.0V Outputs Open, CPUCLK = 50 MHz |
| | | | 240 | mA | Inputs at 2.0V |
| | | | 180 | mA | Inputs at 5.0V Outputs Open, CPUCLK = 66 MHz |
| ICCAT | Supply Current | | 15 | mA | Inputs at 2.0V |
| | | | 10 | mA | Inputs at 5.0V |
| ICCSB | Typical Supply Current, Power Down Mode for WD7855/LV | .5 | | mA | Typical, CPUCLK Off, CLK14 = 32 KHz |

**TABLE 12-1. DC OPERATING CHARACTERISTICS**

**FOR PINS WITH INTERNAL PULLUPS:**

$\overline{MASTER}$, $\overline{IOCK}$, $\overline{IOCS16}$, $\overline{MEMCS16}$, $\overline{ZEROWS}$, IOCHRDY, $\overline{RDYIN}$, $\overline{PDREF}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -45 | -160 | µA | Not suspend and resume mode |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

M//$\overline{IO}$, $\overline{NPERR}$, $\overline{NPBUSY}$, NPRST, CPURES, DPH, DPL, $\overline{NONCAC}$, $\overline{ADS}$, D/$\overline{C}$, W/$\overline{R}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -45 | -160 | µA | Not processor power down or suspend mode |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

PMCIN, IOCHRDY, $\overline{ZEROWS}$, $\overline{IOCS16}$, $\overline{MEMCS16}$, $\overline{MASTER}$, $\overline{PDREF}$, $\overline{REFRESH}$, $\overline{BHE}$, $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -45 | -160 | µA | Not suspend mode |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

SDT/$\overline{R}$, CAS3, CAS2

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -45 | -160 | µA | $\overline{RESET}$ IN = 0 |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

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**FOR PINS WITH INTERNAL PULLDOWNS:**

A(23:00), D(15:00), $\overline{BLE}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pulldown Current * | -45 | -160 | µA | Processor power down or suspend mode |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

DACKEN, D(15:00), $\overline{\text{READY}}$, CPURES, HOLDR, INTRQ, A(23:00), NMI, DPH, DPL, RA(11:08), RA7/ED7:RA0/ED0, $\overline{\text{BHE}}$, $\overline{\text{RAS}}$(7:0), $\overline{\text{CAS}}$(3:0), W/$\overline{\text{R}}$, DT/$\overline{\text{R}}$, $\overline{\text{DEN1}}$, $\overline{\text{DEN0}}$, SDT/$\overline{\text{R}}$, $\overline{\text{SDEN}}$, $\overline{\text{CSEN}}$, $\overline{\text{LOMEG}}$, A20GATE, $\overline{\text{KEN}}$, $\overline{\text{FLUSH}}$, $\overline{\text{SMI}}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage * | $V_{DD}$ -.8 | | V | IOUT = -100 µA |
| VOH | Output High Voltage * | 2.4 | | V | IOUT = -2 mA |
| VOL | Output Low Voltage * | | .4 | V | IOUT = 2 mA |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

MXCTL2:0

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage | $V_{DD}$ -.8 | | V | IOUT = -100 µA |
| VOH | Output High Voltage * | 2.4 | | V | IOUT = -2 mA |
| VOL | Output Low Voltage * | | .4 | V | IOUT = 2 mA |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

$\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, AEN, SYSCLK, BALE, LA20, SA0

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage | 2.4 | | V | IOUT = -3 mA |
| VOL | Output Low Voltage * | | .5 | V | IOUT = 24 mA |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

$\overline{\text{REFRESH}}$, IOCHRDY

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOL | Output Low Voltage * | | .5 | V | IOUT = 24 mA |

**TABLE 12-1. DC OPERATING CHARACTERISTICS (Continued)**

## 13.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into three major categories: Memory Timing (Section 13.1), AT Bus Timing (Section 13.2) and Processor Timing (Section 13.3).

This section provides the AC Operating Characteristics for the WD7855. The parameters for the WD7855LV that differ from these are marked with an * and appear in the appendix.

Table 13-1 lists the timing tables and figures, and their section location.

| TABLE NUMBER | FIGURE NUMBER | TITLE | SECTION |
|---|---|---|---|
| 13-3 | | 80386SX - Page Mode Memory Timing | 13.1.1 |
| | 13-1 ↕ 13-6 | 80386SX - Page Mode, First Access Read/Write ... 80386SX - Page Mode, Write Miss Following a Write | |
| 13-4 | | 80386SX - Non-Page Mode 00 and Mode 01 | 13.1.2 |
| | 13-7 ↕ 13-16 | Page Read/Write Hit With Extra Wait State Enabled ... 80386SX - Non-Page Mode 01 - 0 Wait State Write | |
| 13-5 | | CPU Initiated AT Bus Cycles | 13.2.1 |
| | 13-17 ↕ 13-26 | AT Bus I/O or Memory Read: 8-Bit, Default Timing ... AT Bus I/O or Memory Write: 16-Bit, Default Timing | |
| 13-6 | | Entering the AT Bus | 13.2.2 |
| | 13-27 | 80386SX CPU - BREQ Delay = 1/2 Clock | |
| | 13-28 | 80386SX CPU - BREQ Delay = 1 Clock | |
| | 13-29 | 80386SX CPU - Synchronous CPUCLK to SYSCLK | |
| 13-7 | | Exiting the AT Bus | 13.2.3 |
| | 13-30 ↕ 13-33 | Synchronous AT Bus Cycle Completion, AT Bus Clock = 1/2 CPUCLK ... Asynchronous AT Bus Cycle Completion, BAK_DEL = 0 or +0.5 AT Bus Cycles | |
| 13-8 | | DMA Cycles | 13.2.4 |
| | 13-34 | Basic DMA Cycle, Default Timing | |
| | 13-35 | DMA Cycle, 8-Bit I/O to On-board Memory | |
| | 13-36 | DMA Cycle, On-board Memory to 8-Bit I/O | |
| 13-9 | | AT Bus Master Cycle | 13.2.5 |
| | 13-37 | AT Bus Master, Bus Acquisition/Release | |
| | 13-38 | AT Bus Master, Write to On-board Memory | |
| | 13-39 | AT Bus Master, Read from On-board Memory | |
| 13-10 | | AT Bus Refresh Cycle, Default Timing | 13.2.6 |
| | 13-40 | AT Bus Refresh Cycle, Default Timing | |
| 13-11 | | 80386SX CPU Timing | 13.3 |
| | 13-41 ↕ 13-48 | 80386SX - CPURES and NPRST During Power Up ... 80386SX - Output Delay Timing | |
| 13-12 | | WD7855 SMI Timing | 13.3 |
| | 13-49 | I/O Trap Cycle With Am386SXLV | |

**TABLE 13-1. TIMING FIGURE/TABLE NUMBERS**

10

| SIGNAL | LOAD | SIGNAL | LOAD | SIGNAL | LOAD |
|---|---|---|---|---|---|
| $\overline{SMI}$ | 50 pF | $\overline{NA}$ | 50 pF | $\overline{SMIRDY}$ | 50 pF |
| $\overline{KEN}$ | 50 pF | A20GATE | 50 pF | $\overline{FLUSH}$ | 50 pF |
| CPURES | 50 pF | NPRST | 50 pF | $\overline{BHE}$ | 50 pF |
| W/$\overline{R}$ | 50 pF | ALE | 50 pF | $\overline{DEN1}$, $\overline{DEN0}$ | 50 pF |
| $\overline{SDEN}$ | 50 pF | DT/$\overline{R}$ | 50 pF | $\overline{SDT/R}$ | 50 pF |
| MXCTL(2:0) | 50 pF | DACKEN | 50 pF | $\overline{CSEN}$ | 50 pF |
| $\overline{LOMEG}$ | 50 pF | SPKR | 50 pF | $\overline{READY}$ | 50 pF |
| $\overline{HOLDR}$ | 50 pF | INTRQ | 50 pF | NMI | 50 pF |
| $\overline{BUSYCPU}$ | 50 pF | EPEREQ | 50 pF | A(23:00) | 60 pF |
| CPUCLK | 70 pF | SYSCLK | 75 pF | $\overline{DPH}$ | 100 pF |
| $\overline{CAS}$(3:0) | 100 pF | D(15:00) | 100 pF | $\overline{IOW}$ | 200 pF |
| DPL | 100 pF | $\overline{RAS}$(7:0) | 75 pF | $\overline{MEMR}$ | 200 pF |
| $\overline{IOR}$ | 200 pF | $\overline{MEMW}$ | 200 pF | AEN | 200 pF |
| LA20 | 200 pF | SA0 | 200 pF | RA(11:00) * | 350 pF |
| BALE | 200 pF | $\overline{REFRESH}$ | 200 pF | | |

**TABLE 13-2. SIGNAL LOADING**

## 13.1 MEMORY TIMING

Sections 13.1.1 and 13.1.2 present the memory timing for Page Mode and Non-Page Mode, for the 80386SX processor.

Categories are grouped as follows:

80386SX
- Page Mode
- Non-Page Mode 00 and 01

### 13.1.1 80386SX Page Mode Timing

| SYMBOL | CHARACTERISTIC | MAX 20 MHz | MAX 25 MHz | MAX 33 MHz |
|---|---|---|---|---|
| T200 | Processor address to RAM address valid, Page Hit | 34 | 27 | 27 |
| T201 | CPUCLK rise to $\overline{CAS}$ fall, 2.5 CLK $\overline{CAS}$ | 31 | 25 | 20 |
| T202 | CPUCLK fall to $\overline{CAS}$ rise | 24 | 21 | 21 |
| T203 | CPUCLK fall to $\overline{CAS}$ fall, 2.0 CLK $\overline{CAS}$ | 27 | 22 | 22 |
| T204 | Processor data to parity valid | 25 | 20 | 20 |
| T205 | CPUCLK rise to RAM address valid, Page Miss | 48 | 43 | 43 |
| T206 | CPUCLK rise to WNRDRAM rise | 31 | 28 | 28 |
| T207 | CPUCLK fall to $\overline{RAS}$ fall, first access | 27 | 21 | 21 |
| T208 | CPUCLK rise to COLUMN address valid | 49 | 33 | 30 |
| T209 | CPUCLK rise to WNRDRAM fall | 31 | 28 | 28 |
| T212 | CPUCLK rise to $\overline{RAS}$ rise, Page Miss | 27 | 24 | 24 |
| T213 | CPUCLK fall to $\overline{RAS}$ fall, Page Miss | 27 | 24 | 24 |
| T214 | CPUCLK rise to $\overline{READY}$ fall * | 19 | 18 | 18 |
| T215 | CPUCLK rise to $\overline{READY}$ rise * | 19 | 18 | 18 |

**TABLE 13-3. 80386SX - PAGE MODE MEMORY TIMING**

10

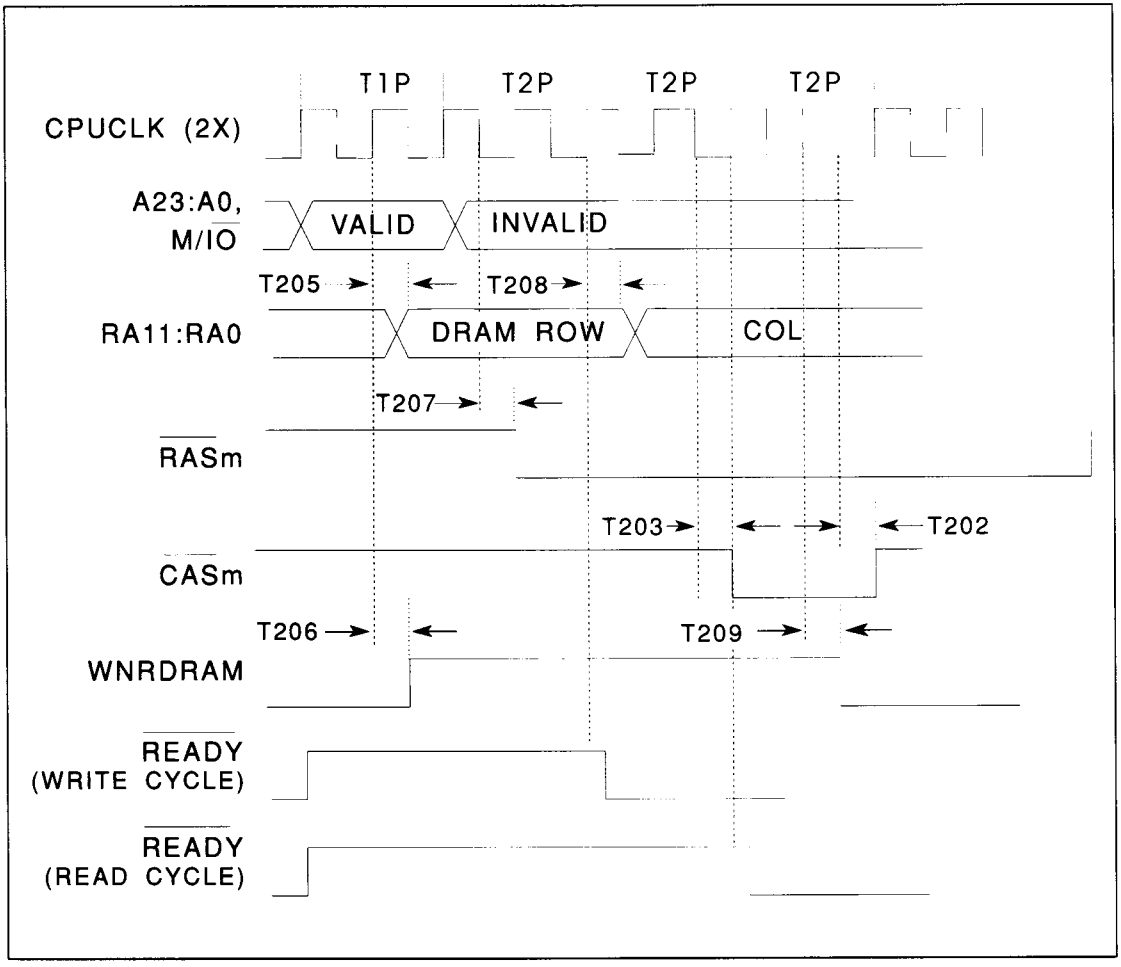


**FIGURE 13-1. 80386SX - PAGE MODE, FIRST ACCESS READ/WRITE**

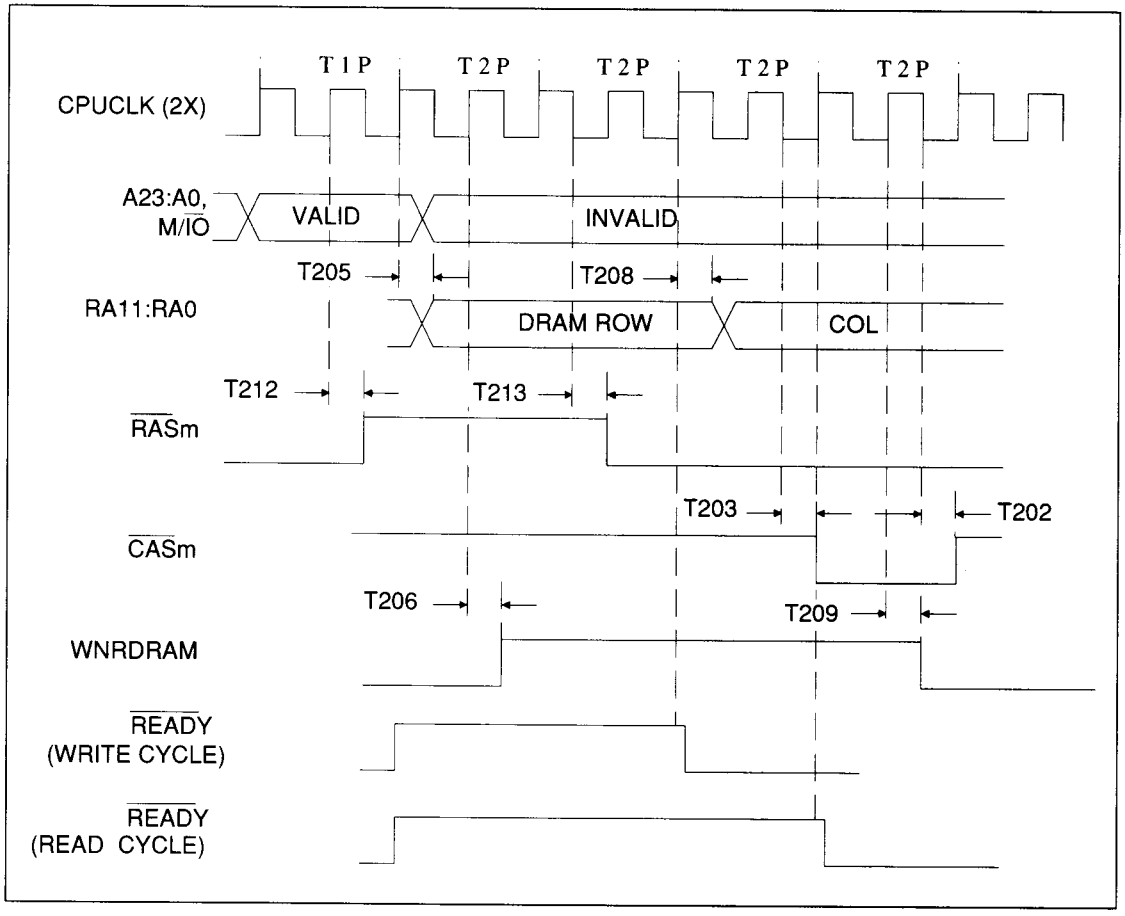


**FIGURE 13-2. 80386SX - PAGE MODE, PAGE MISS READ/WRITE**

10

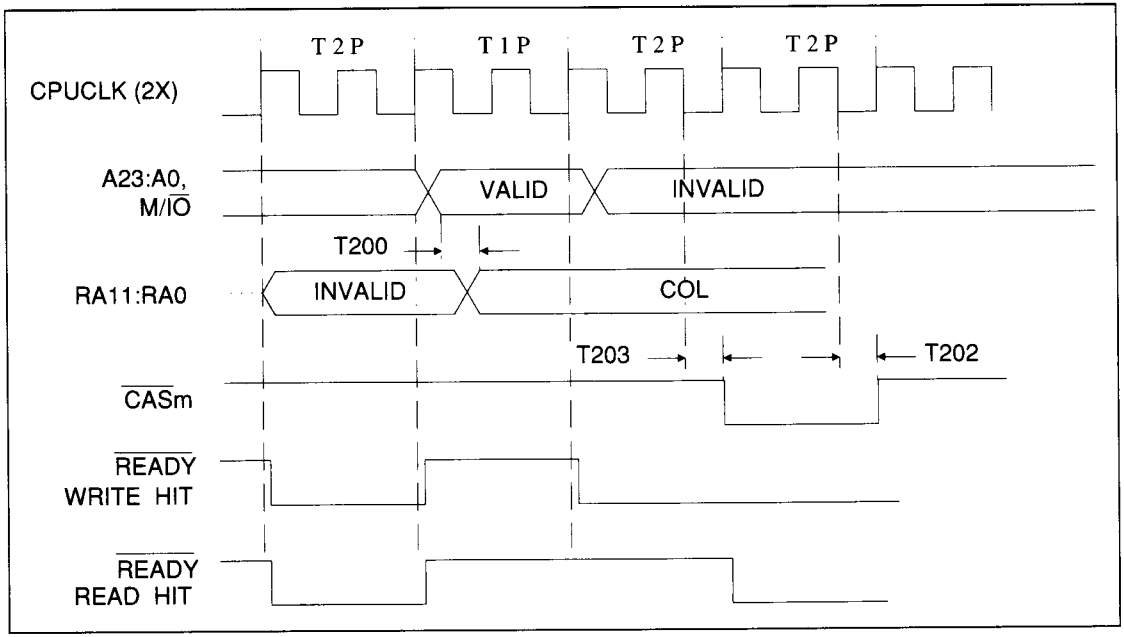


**FIGURE 13-3. 80386SX - PAGE MODE, READ CYCLE FOLLOWED BY A PAGE HIT**

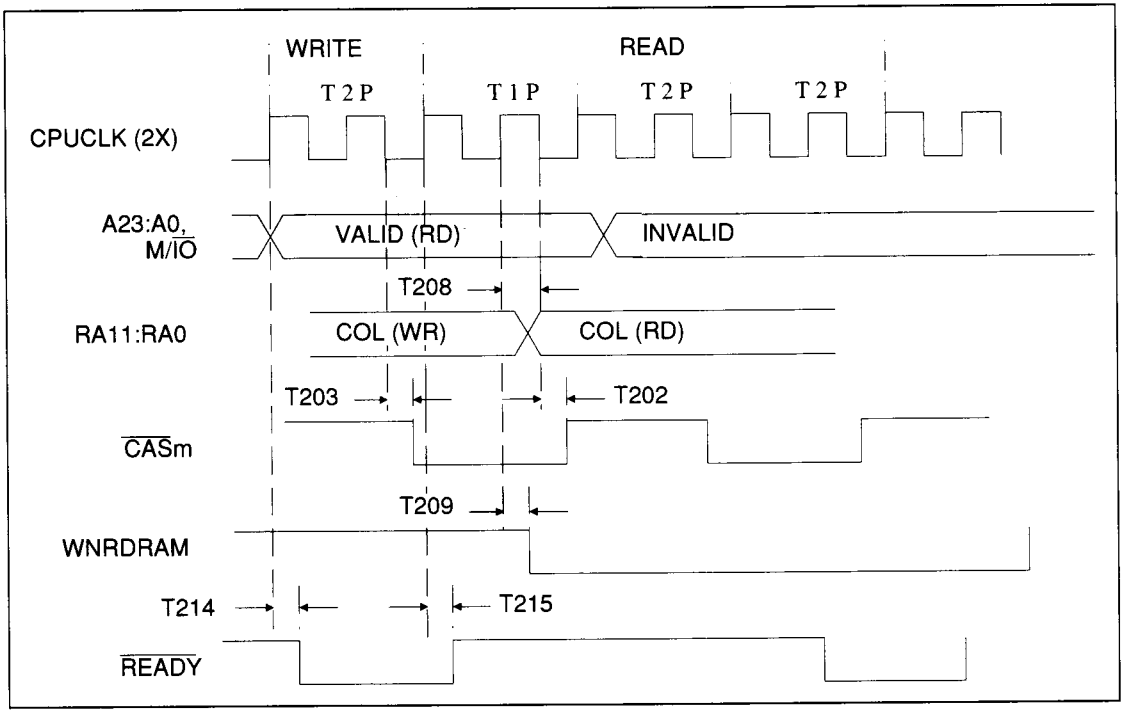


**FIGURE 13-4. 80386SX - PAGE MODE, READ AFTER WRITE**

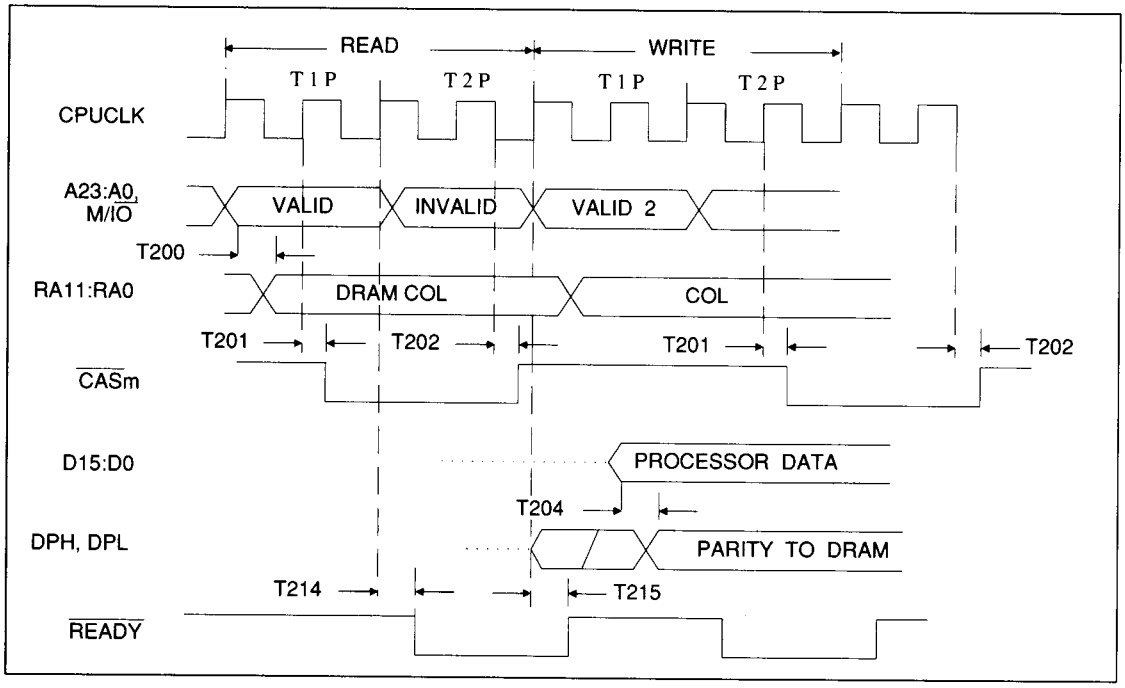


**FIGURE 13-5. 80386SX - PAGE MODE, READ HIT FOLLOWED BY A WRITE HIT**

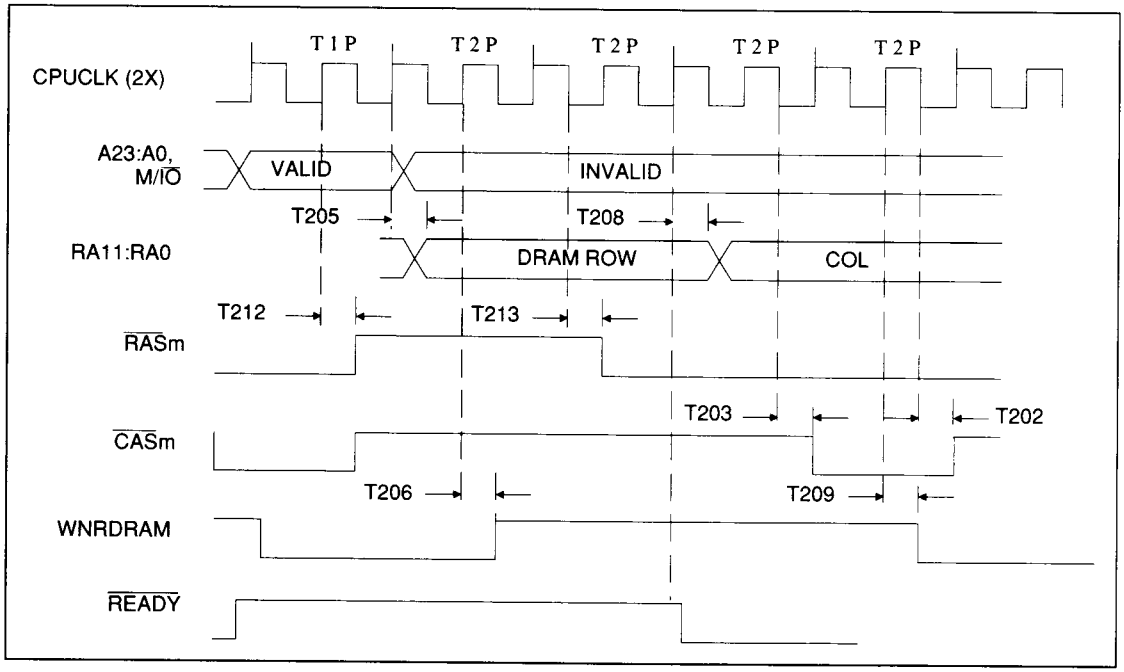


**FIGURE 13-6. 80386SX - PAGE MODE, WRITE MISS CYCLE FOLLOWING A WRITE CYCLE**

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### 13.1.2 80386SX Non-Page Mode 00 and Mode 01 Timing

| SYMBOL | CHARACTERISTIC | MAX 20 MHz | MAX 25 MHz | MAX 33 MHz |
|---|---|---|---|---|
| T204 | See Table 13-3 | | | |
| T214 | See Table 13-3 | | | |
| T215 | See Table 13-3 | | | |
| T240 | CPUCLK rise to ROW address valid | 42 | 42 | 42 |
| T241 | CPUCLK fall to $\overline{CAS}$ fall | 27 | 27 | 27 |
| T242 | CPUCLK rise to $\overline{CAS}$ rise | 28 | 24 | 24 |
| T243 | CPUCLK rise to WNRDRAM fall | 28 | 28 | 28 |
| T244 | CPUCLK rise to WNRDRAM rise | 28 | 28 | 28 |
| T245 | CPUCLK rise to $\overline{RAS}$ fall | 25 | 23 | 23 |
| T246 | CPUCLK rise to $\overline{RAS}$ rise | 25 | 23 | 23 |
| T247 | CPUCLK fall to $\overline{RAS}$ rise | 29 | 29 | 29 |
| T248 | CPUCLK fall to COLUMN address valid | 44 | 44 | 44 |
| T249 | CPUCLK rise to $\overline{CAS}$ fall | 29 | 29 | 29 |
| T260 | CPUCLK rise to COLUMN address | 43 | 41 | 41 |

**TABLE 13-4. 80386SX - NON-PAGE MODE 00, 01 MEMORY TIMING**

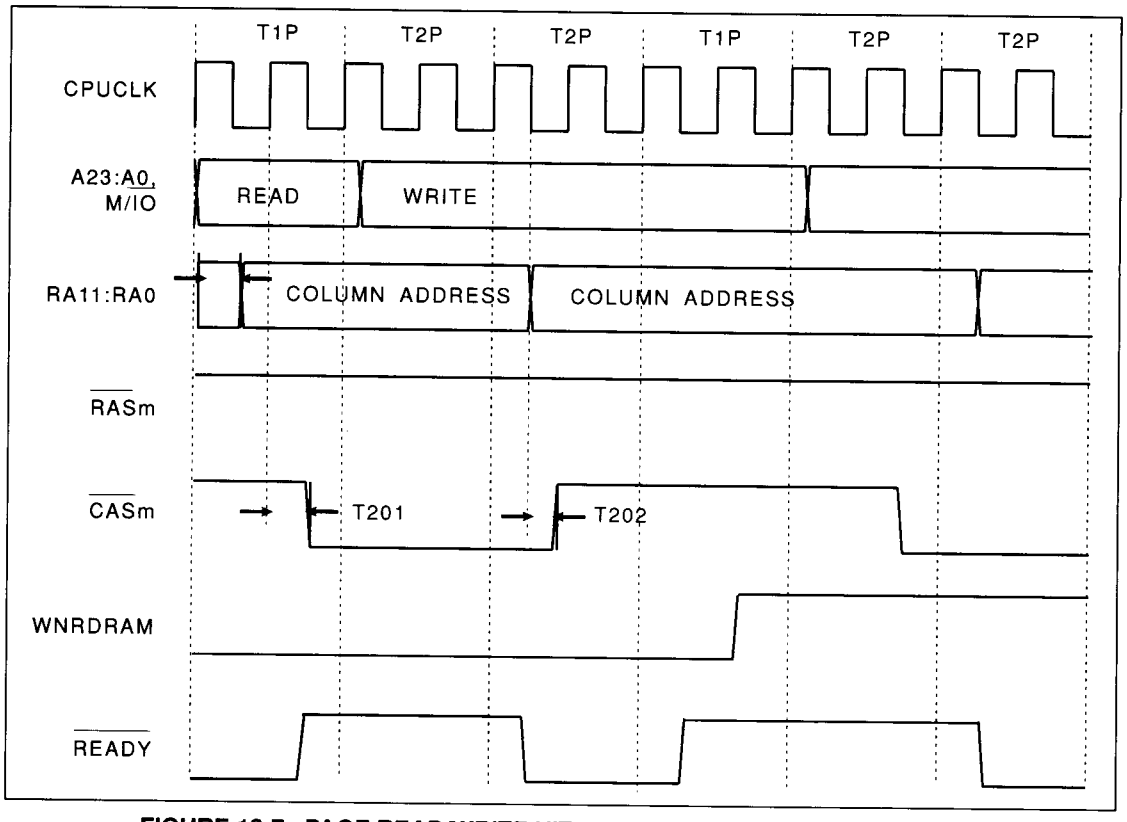


**FIGURE 13-7. PAGE READ/WRITE HIT WITH EXTRA WAIT STATE ENABLE**

10

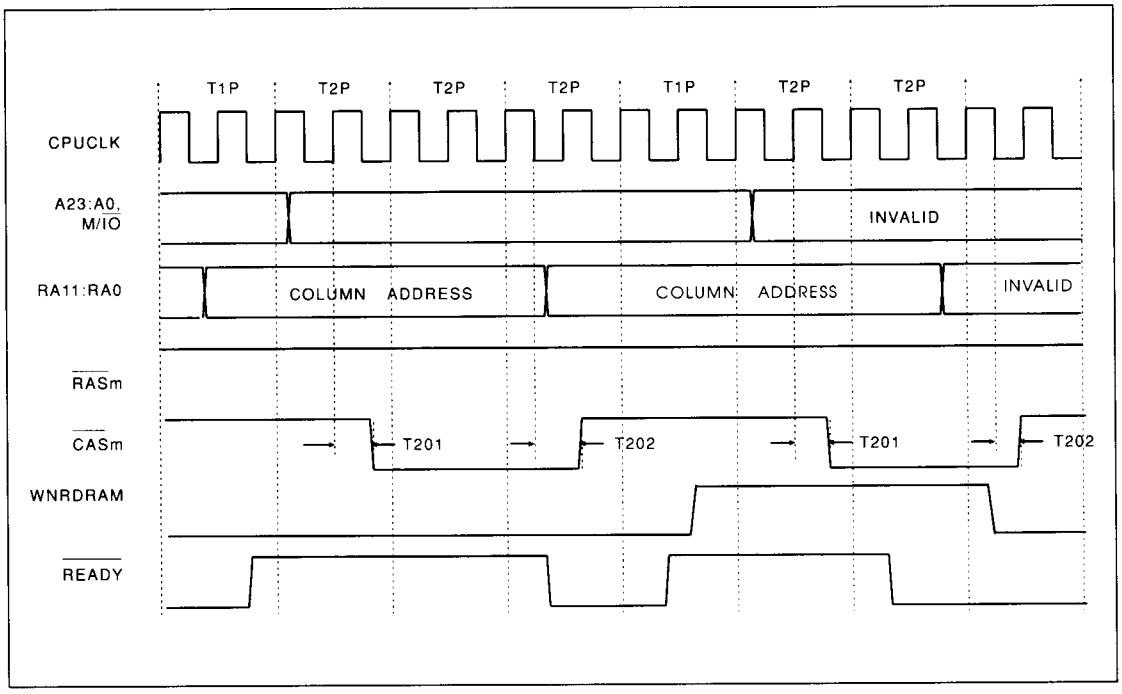


**FIGURE 13-8. READ PAGE HIT FOLLOWED BY WRITE PAGE HIT WITH EXTERNAL CACHE ENABLE AND EXTRA WAIT STATE ENABLE**

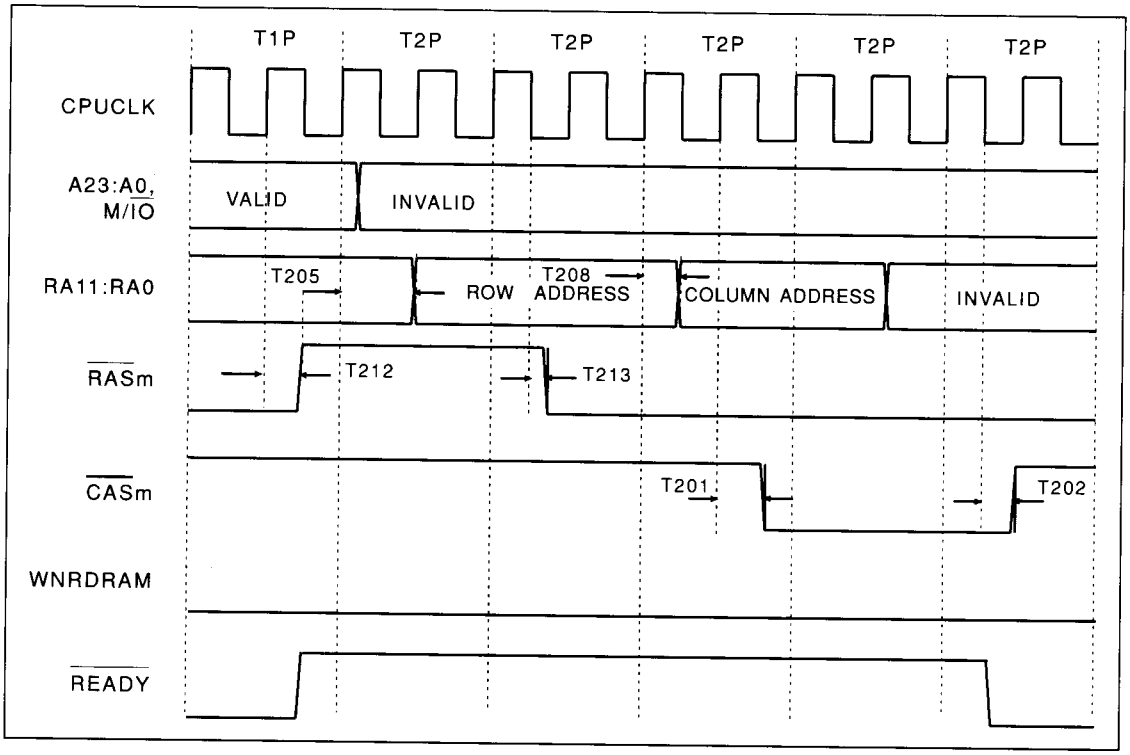


**FIGURE 13-9. PAGE READ MISS WITH EXTRA WAIT STATE ENABLE**

10

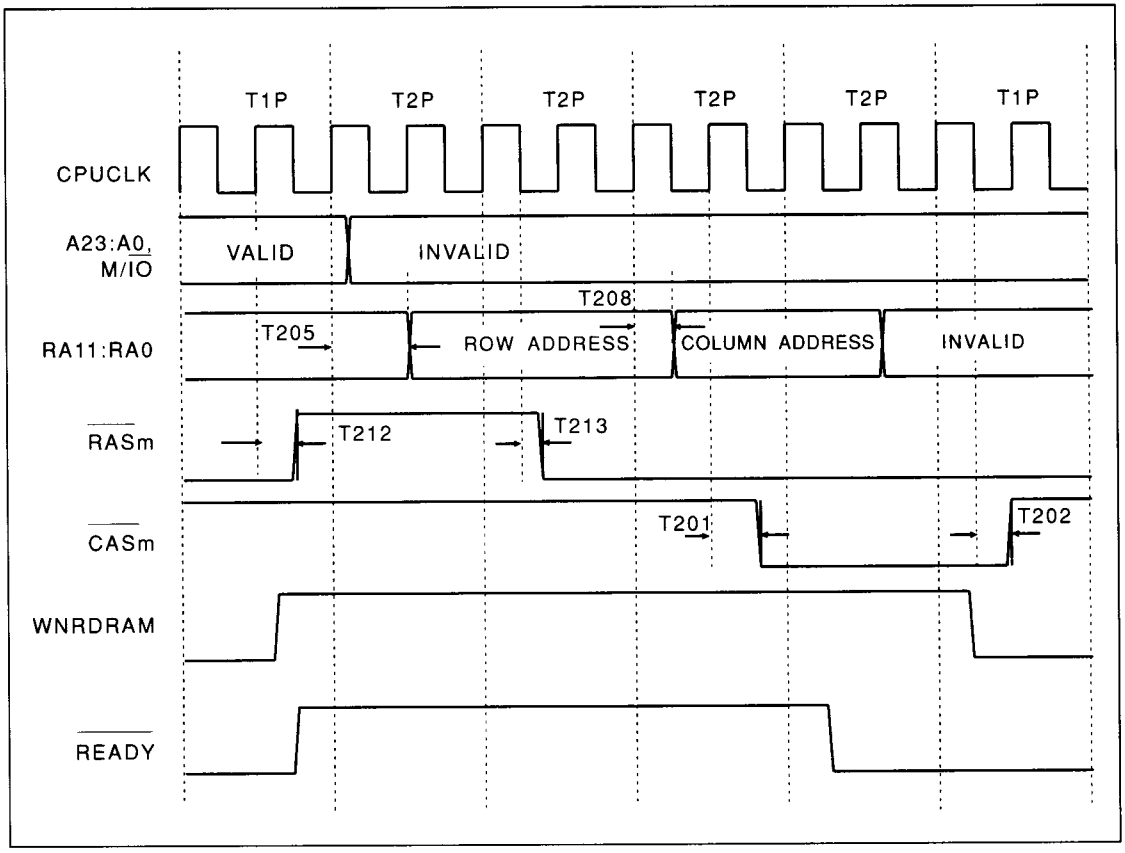


**FIGURE 13-10. PAGE WRITE MISS WITH EXTRA WAIT STATE ENABLE**

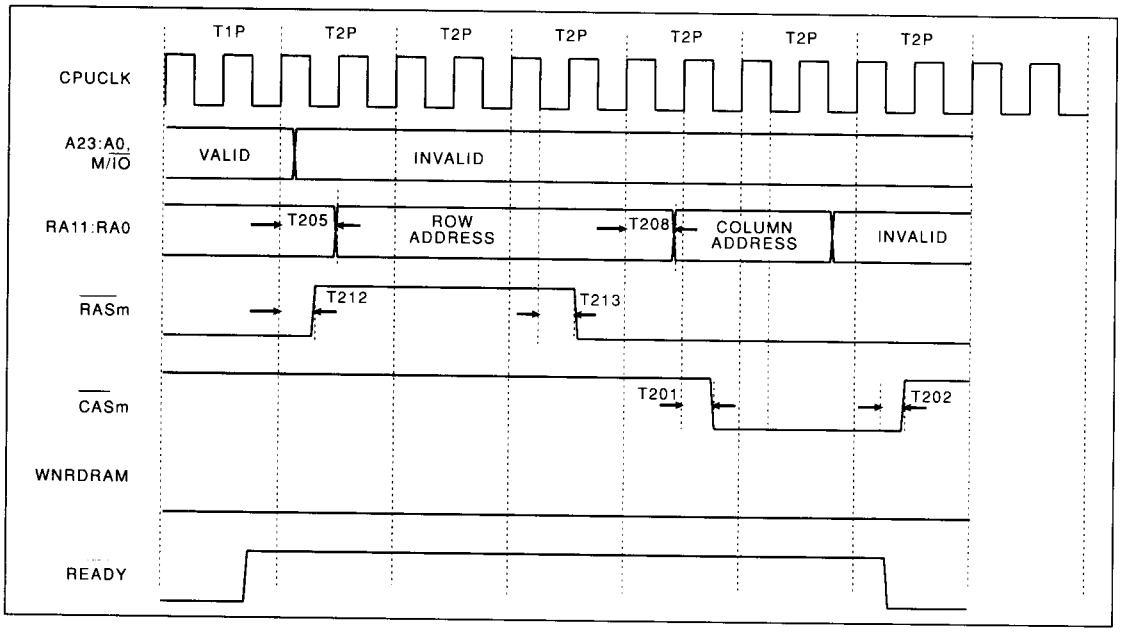


**FIGURE 13-11. READ PAGE MISS WITH EXTERNAL CACHE ENABLE AND EXTRA WAIT STATE ENABLE**

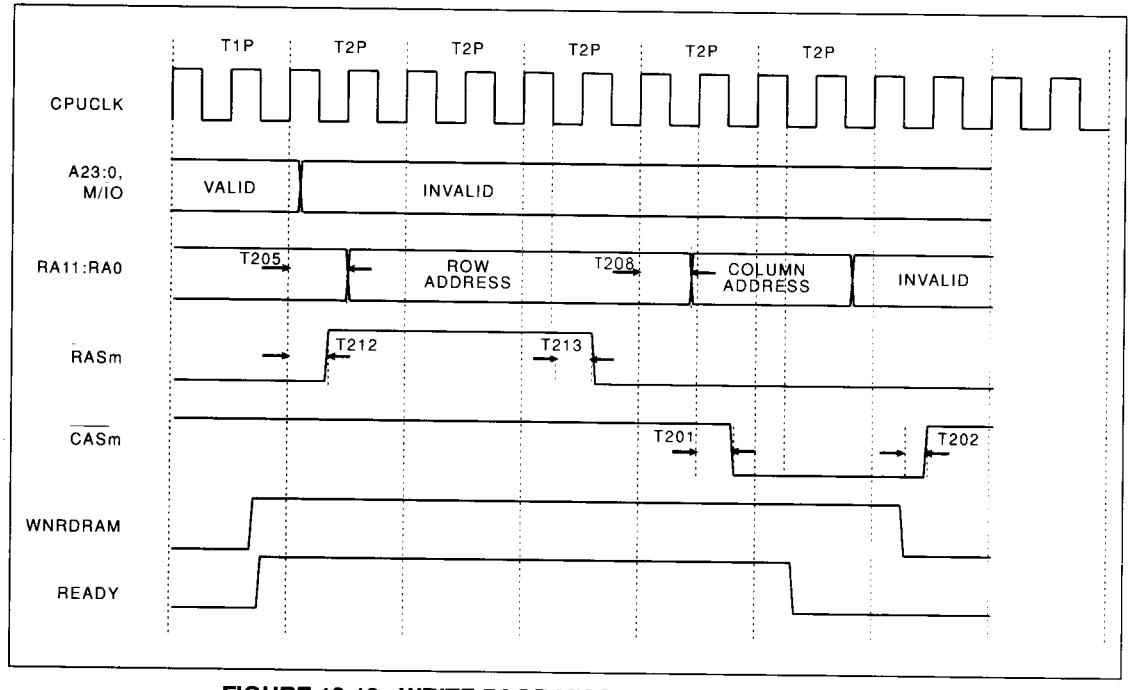


**FIGURE 13-12. WRITE PAGE MISS WITH EXTERNAL CACHE ENABLE AND EXTRA WAIT STATE ENABLE**

10

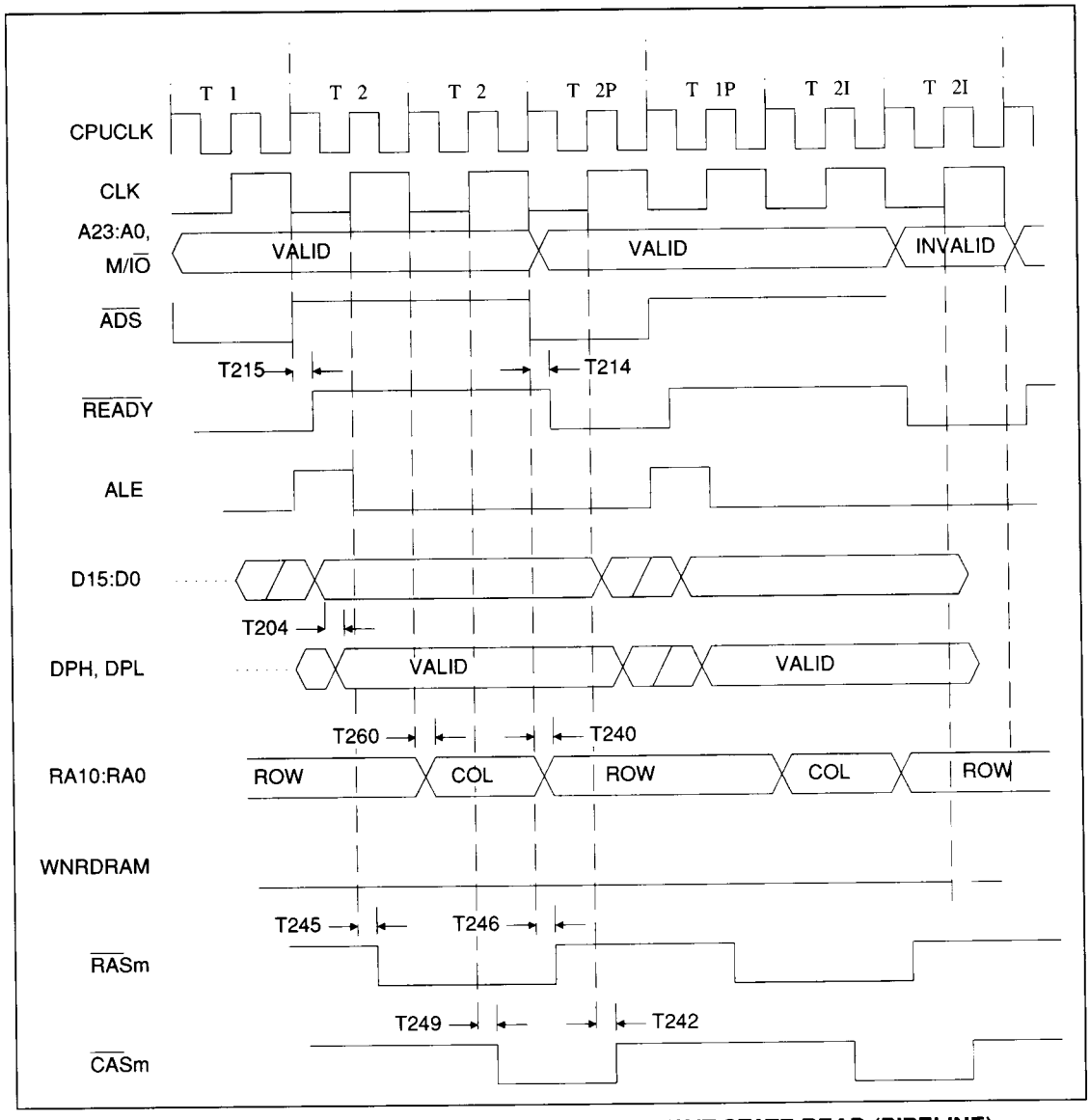


**FIGURE 13-13. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE READ (PIPELINE) (4072H = 0001)**

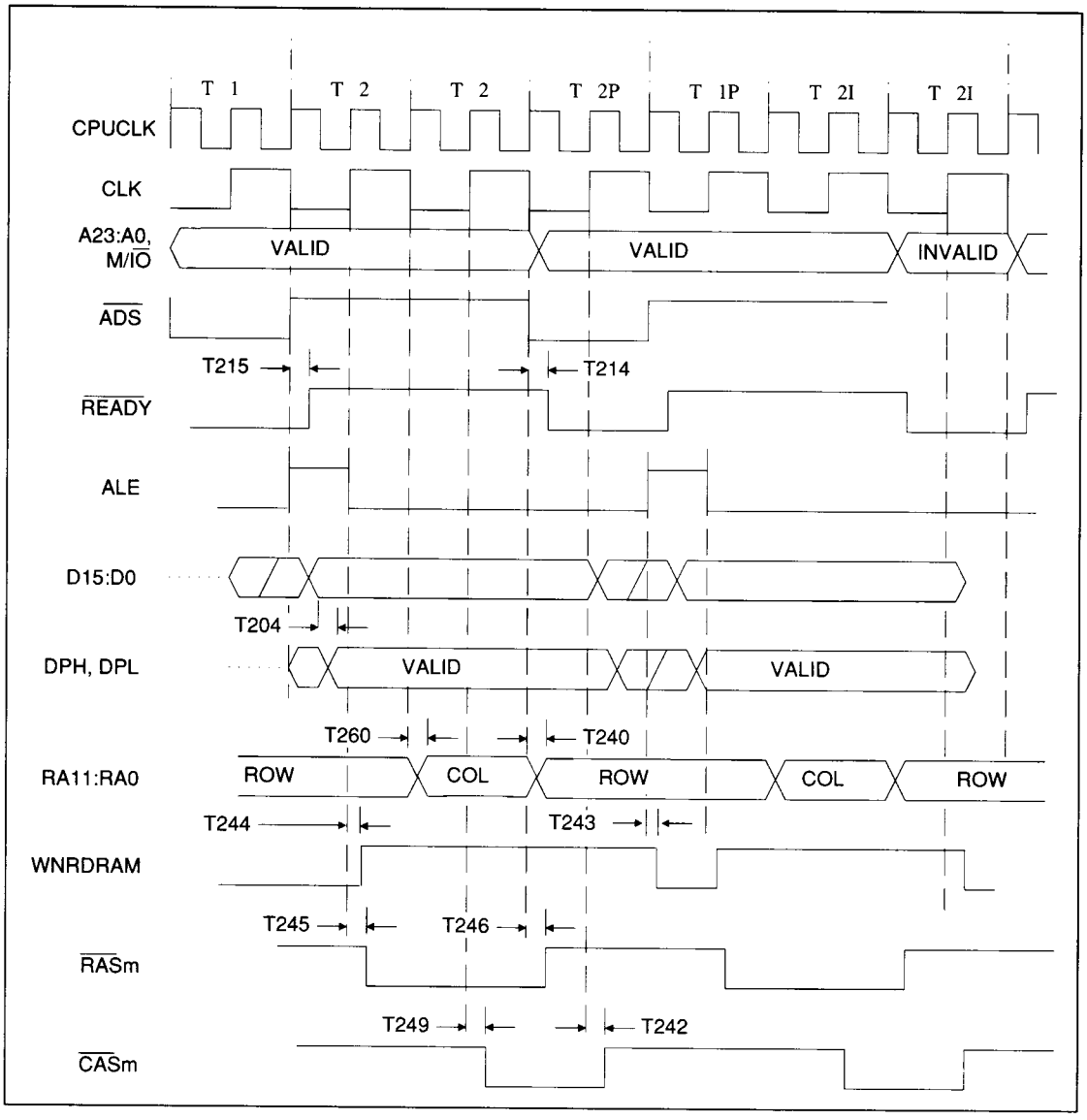


**FIGURE 13-14. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE WRITE (PIPELINE) (4072H = 0001)**

10

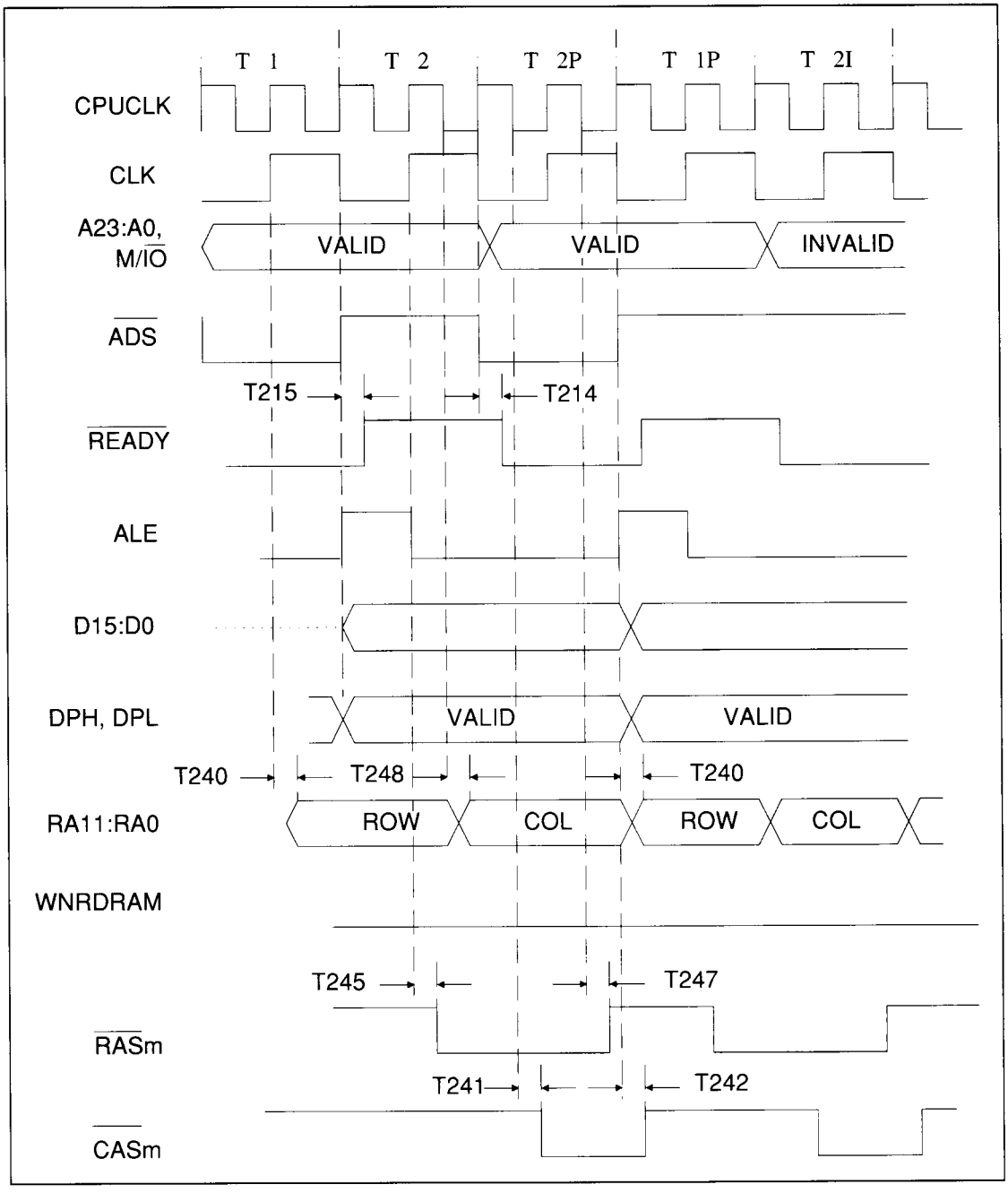


**FIGURE 13-15. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)**

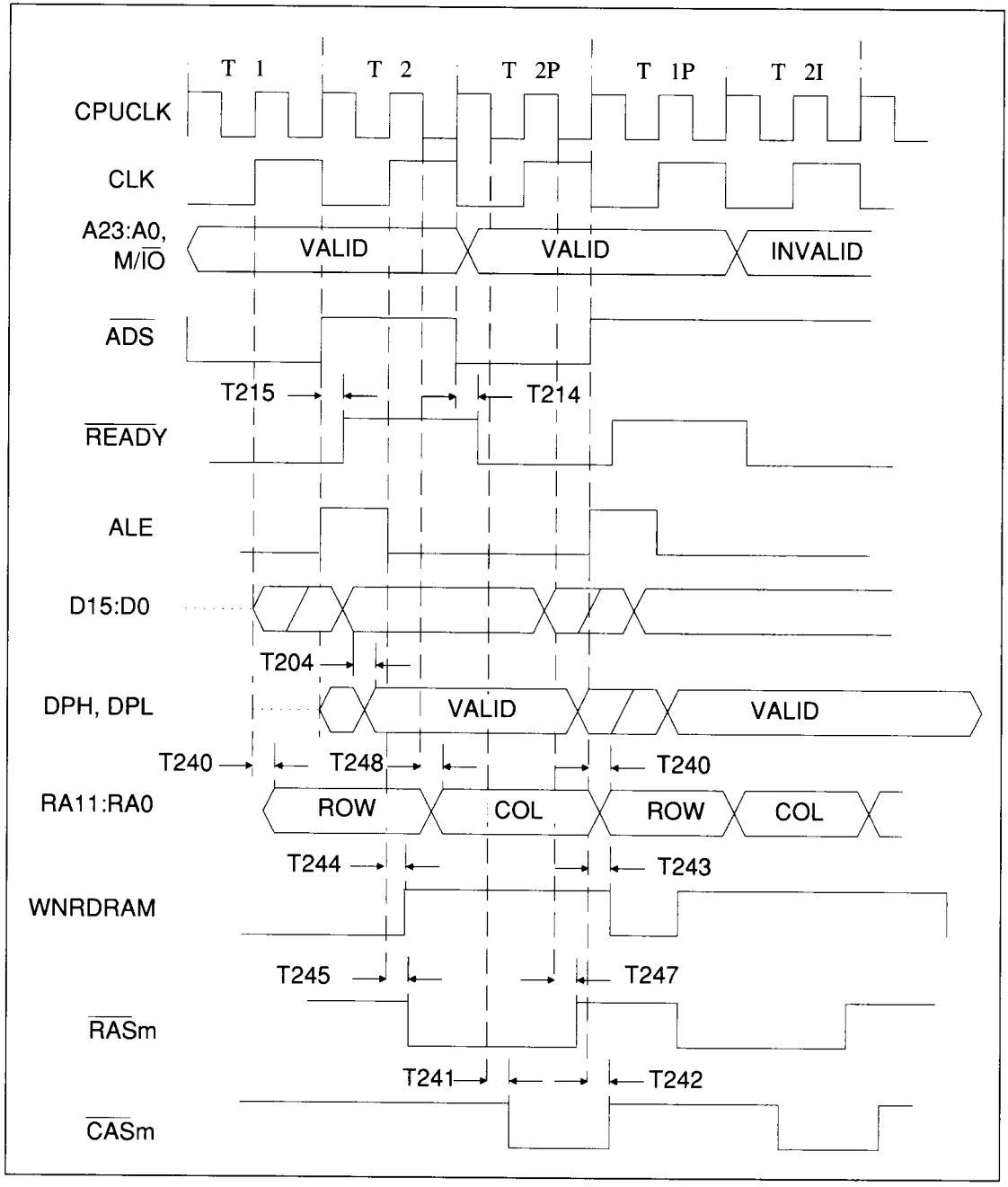


**FIGURE 13-16. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE WRITE (PIPELINE) (4072H = 3560H)**

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## 13.2 AT BUS TIMING

The AT Bus timing is divided into six major categories:

1. CPU initiated AT Bus cycles.
2. Entering the AT Bus.
3. Exiting the AT Bus.
4. DMA cycles.
5. AT Bus Master cycles.
6. AT Bus Refresh cycle.

Some figures in this section are included only to show the sequence of the signals during certain operations. In these figures, no timing parameters are provided.

### 13.2.1 CPU Initiated AT Bus Cycles

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T00 | SYSCLK Cycle Time | 100 | | ns | |
| T01 | SYSCLK fall to BALE rise | | 12 | ns | |
| T02 | SYSCLK rise to BALE fall | | 9 | ns | |
| T03 | SYSCLK fall to $\overline{\text{MEMR}}$ fall | | 9 | ns | 8-bit cycle |
| T04 | SYSCLK rise to $\overline{\text{MEMR}}$ rise | | 6 | ns | |
| T05 | SYSCLK fall to $\overline{\text{IOR}}$ fall | | 10 | ns | |
| T06 | SYSCLK rise to $\overline{\text{IOR}}$ rise | | 7 | ns | |
| T07 | SYSCLK rise to $\overline{\text{DEN0}}$ fall | | 7 | ns | Read Cycle |
| T08 | SYSCLK rise to $\overline{\text{DEN0}}$ rise | | 11 | ns | Read Cycle |
| T09 | SYSCLK rise to $\overline{\text{DEN1}}$ fall | | 7 | ns | Read Cycle |
| T10 | SYSCLK rise to $\overline{\text{DEN1}}$ rise | | 9 | ns | Read Cycle |
| T11 | SYSCLK fall to DTR fall | | 19 | ns | Delay is number given plus (T00 × 0.25) |
| T12 | SYSCLK rise to DTR rise | | 14 | ns | Delay is number given plus (T00 × 0.25) |
| T13 | SYSCLK fall to $\overline{\text{SDEN}}$ fall | | 10 | ns | |
| T14 | SYSCLK rise to $\overline{\text{SDEN}}$ rise | | 8 | ns | |
| T15 | SYSCLK fall to SDTR rise | | 14 | ns | Delay is number given plus (T00 × 0.25) |
| T16 | SYSCLK rise to SDTR fall | | 11 | ns | Delay is number given plus (T00 × 0.25) |
| T17 | $\overline{\text{MEMCS16}}$ setup time to SYSCLK rise | 25 | | ns | |
| T18 | $\overline{\text{MEMCS16}}$ hold time from SYSCLK rise | 0 | | ns | |
| T19 | $\overline{\text{IOCS16}}$ setup time to SYSCLK fall | 23 | | ns | |
| T20 | $\overline{\text{IOCS16}}$ hold time from SYSCLK fall | 0 | | ns | 8-bit cycle |
| T21 | IOCHRDY setup time to SYSCLK rise | 22 | | ns | |
| T22 | IOCHRDY hold time from SYSCLK rise | 0 | | ns | |

**TABLE 13-5. CPU INITIATED AT BUS CYCLES**

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T23 | $\overline{\text{ZEROWS}}$ setup time to SYSCLK fall | 24 | | ns | |
| T24 | $\overline{\text{ZEROWS}}$ hold time from SYSCLK fall | 0 | | ns | |
| T25 | AT Bus data setup time to SYSCLK rise | 22 | | ns | Total setup time is number given plus delay through AT Bus data buffers. |
| T26 | AT Bus data hold time from SYSCLK rise | 0 | | ns | |
| T27 | SYSCLK fall to $\overline{\text{MEMW}}$ fall | | 9 | ns | |
| T28 | SYSCLK rise to $\overline{\text{MEMW}}$ rise | | 5 | ns | |
| T29 | SYSCLK fall to $\overline{\text{IOW}}$ fall | | 10 | ns | |
| T30 | SYSCLK rise to $\overline{\text{IOW}}$ rise | | 8 | ns | |
| T31 | SYSCLK fall to $\overline{\text{DEN0}}$ fall | | 10 | ns | Write cycle |
| T32 | SYSCLK fall to $\overline{\text{DEN0}}$ rise | | 9 | ns | Write cycle |
| T33 | SYSCLK fall to $\overline{\text{DEN1}}$ fall | | 10 | ns | Write cycle |
| T34 | SYSCLK fall to $\overline{\text{DEN1}}$ rise | | 9 | ns | Write cycle |
| T35 | SYSCLK fall to $\overline{\text{SDEN}}$ rise | | 11 | ns | |
| T36 | SYSCLK fall to SA0 rise | | 16 | ns | Word to byte conversion cycle |
| T37 | SYSCLK rise to $\overline{\text{MEMR}}$ fall | | 6 | ns | 16-bit cycle |
| T38 | $\overline{\text{IOCS16}}$ hold time from SYSCLK rise | 0 | | ns | 16-bit cycle |
| T39 | SYSCLK high time | -4 | 0 | ns | (T00 ÷ 2) plus number given |

**TABLE 13-5. CPU INITIATED AT BUS CYCLES (Continued)**

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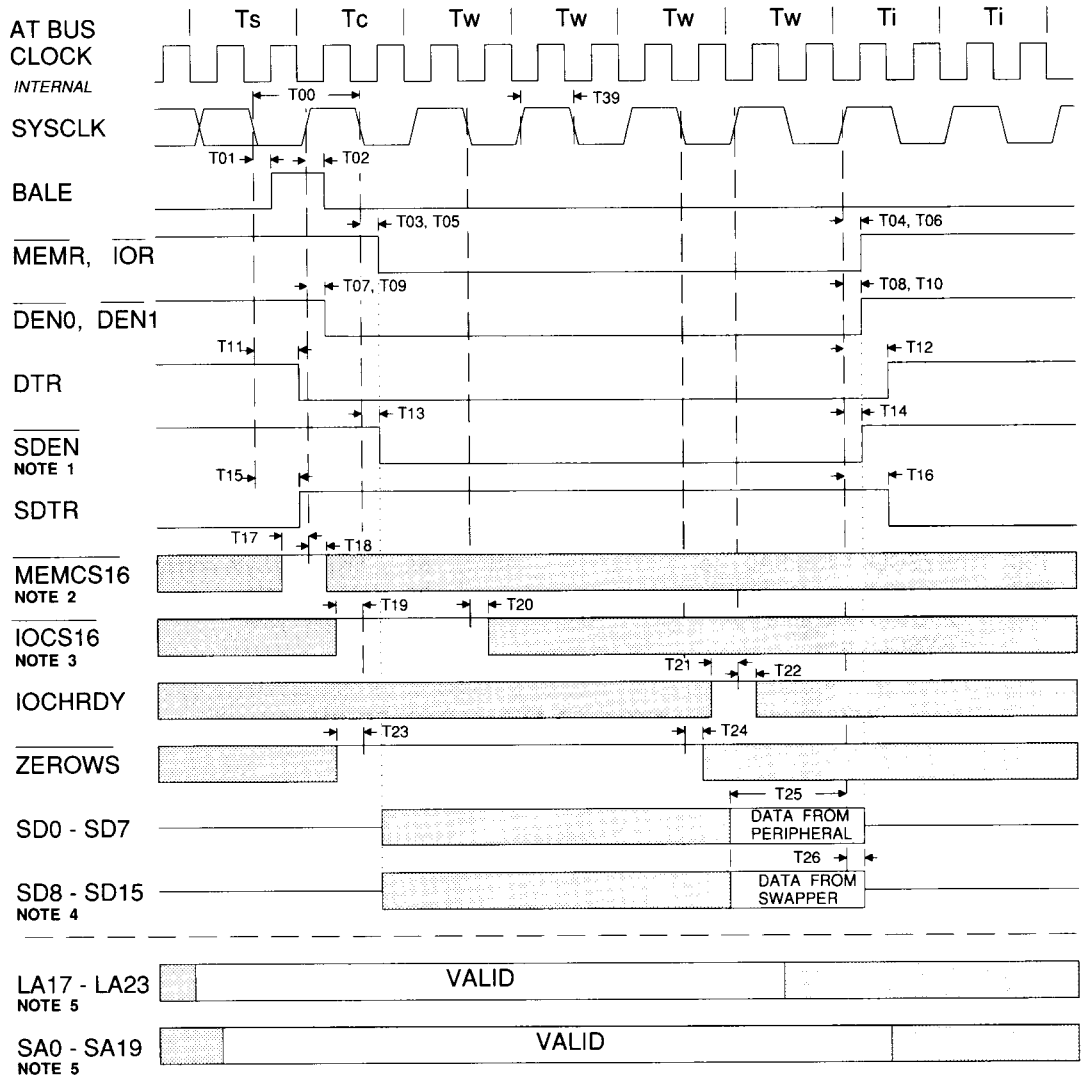
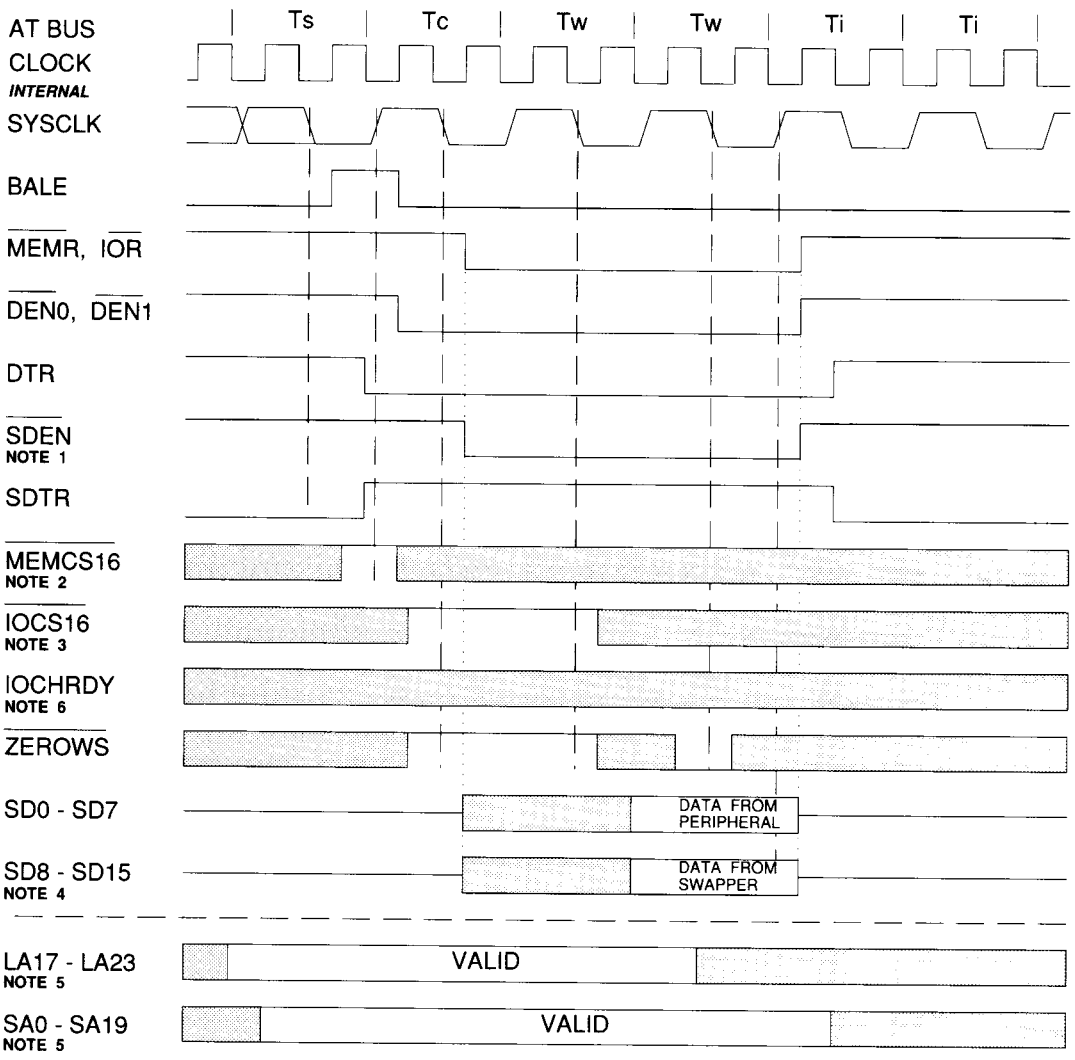



NOTE 1: SDEN is asserted only when SA0 is high.
NOTE 2: MEMCS16 is sampled only during memory cycles.
NOTE 3: IOCS16 is sampled only during I/O cycles.
NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).
NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-17. AT BUS I/O OR MEMORY READ: 8-BIT, DEFAULT TIMING**




NOTE 1: SDEN is asserted only when SA0 is high.

NOTE 2: MEMCS16 is sampled only during memory cycles.

NOTE 3: IOCS16 is sampled only during I/O cycles.

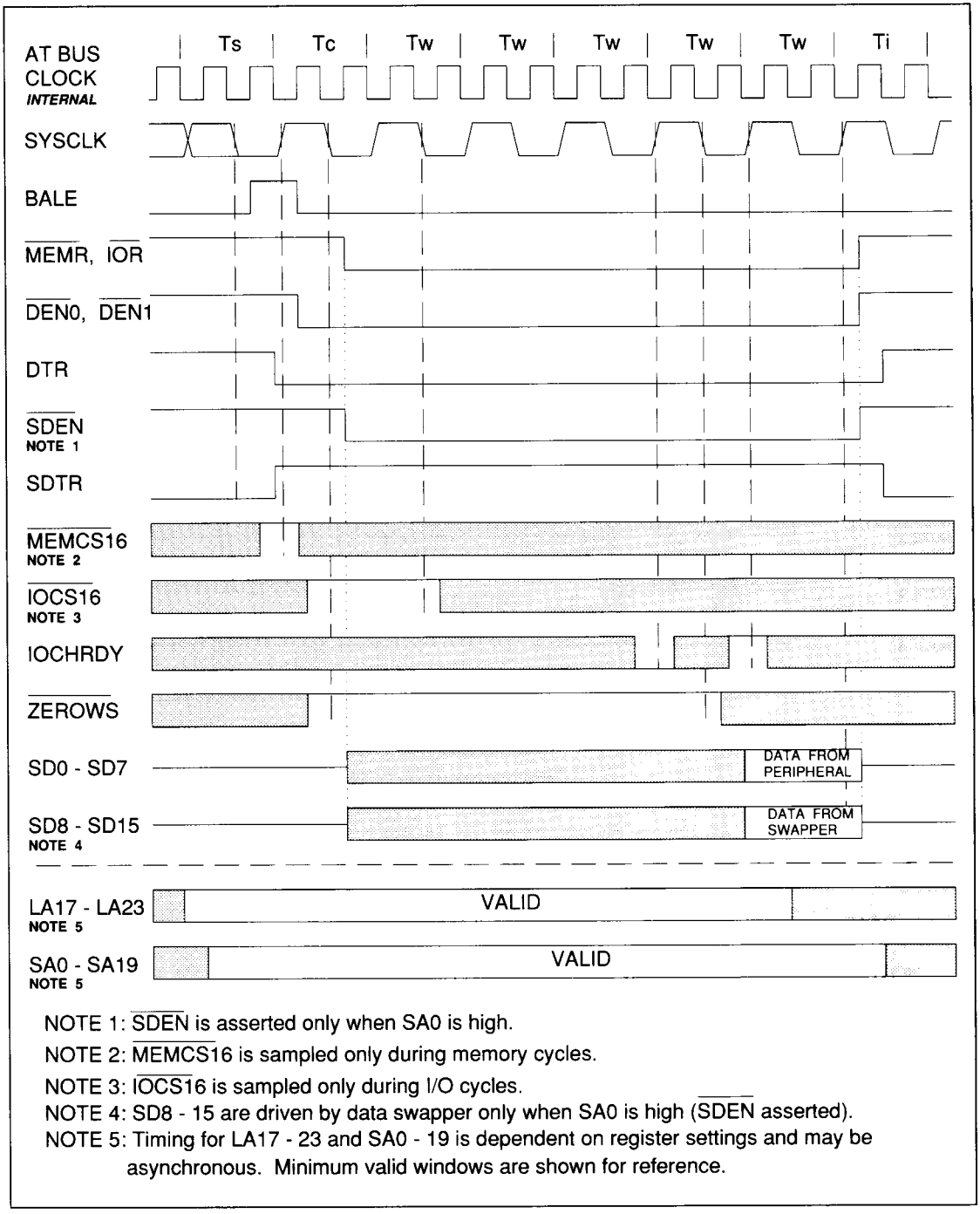
NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

NOTE 6: IOCHRDY overrides ZEROWS only during the first cycle of a word to byte conversion.

**FIGURE 13-18. AT BUS I/O OR MEMORY READ: 8-BIT, ZEROWS ASSERTED**

10




NOTE 1: $\overline{\text{SDEN}}$ is asserted only when SA0 is high.

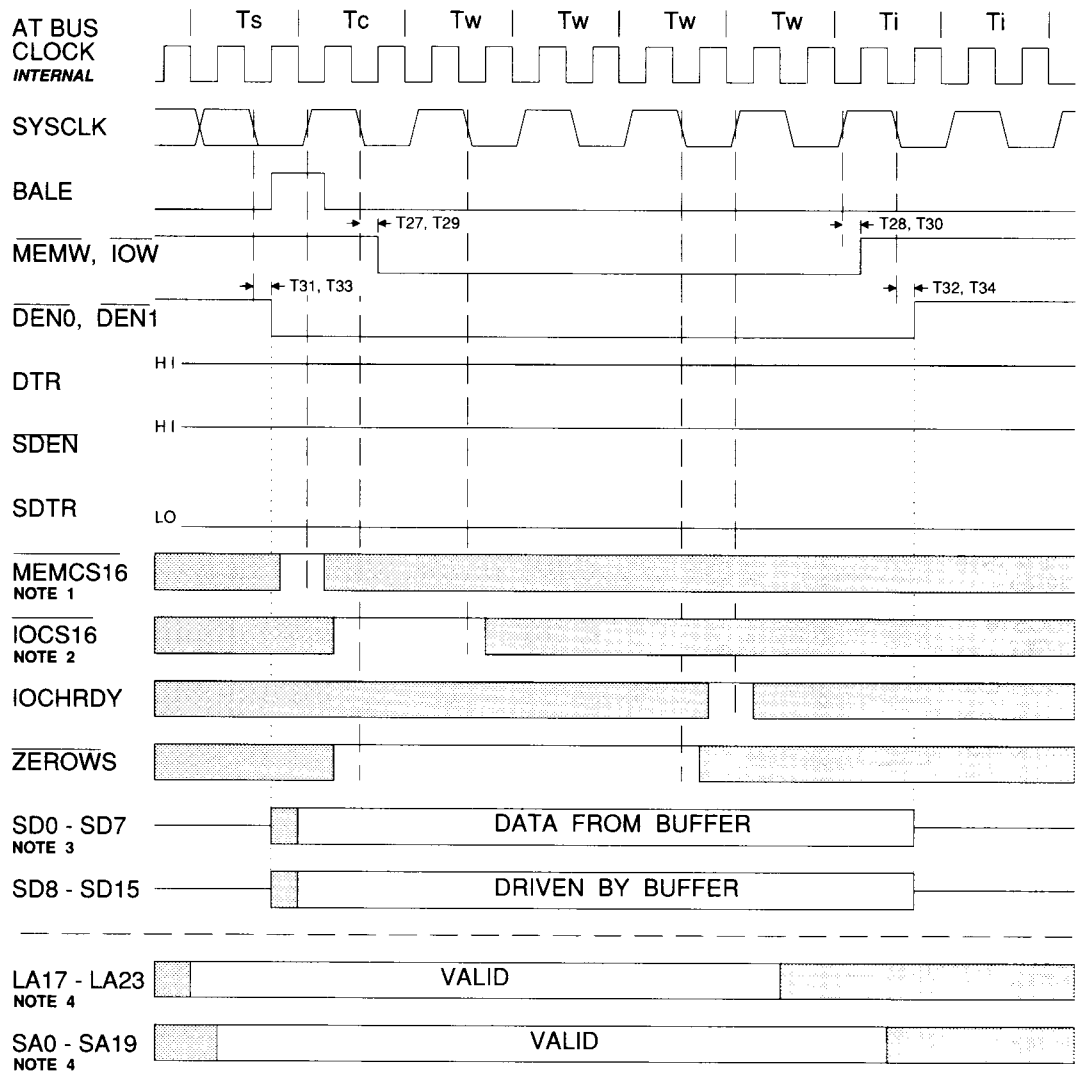
NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 3: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by data swapper only when SA0 is high ($\overline{\text{SDEN}}$ asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-19. AT BUS I/O OR MEMORY READ: 8-BIT, EXTRA WAIT STATE ADDED**




NOTE 1: MEMCS16 is sampled only during memory cycles.

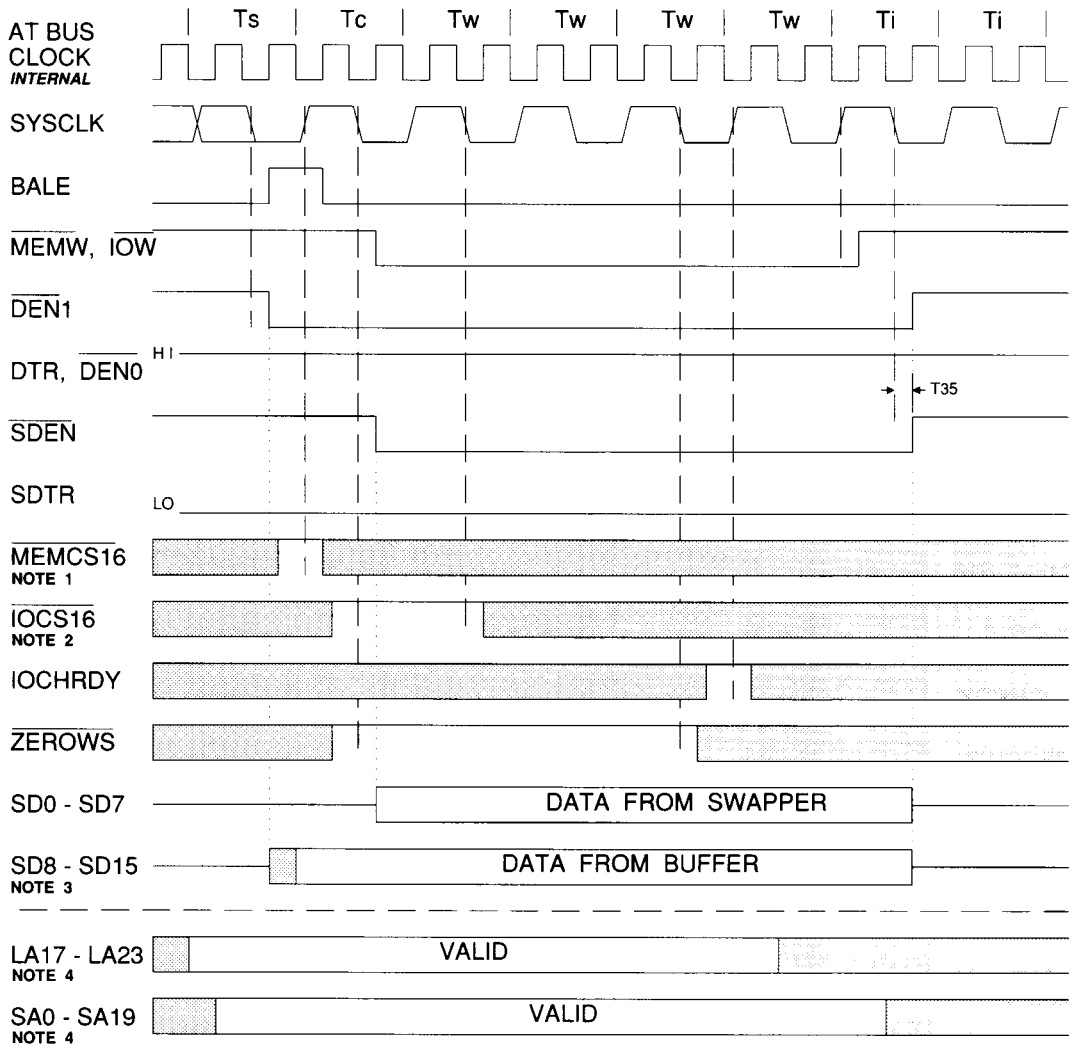
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when DEN0 is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-20. AT BUS I/O OR MEMORY WRITE: 8-BIT, EVEN BYTE, DEFAULT TIMING**

10



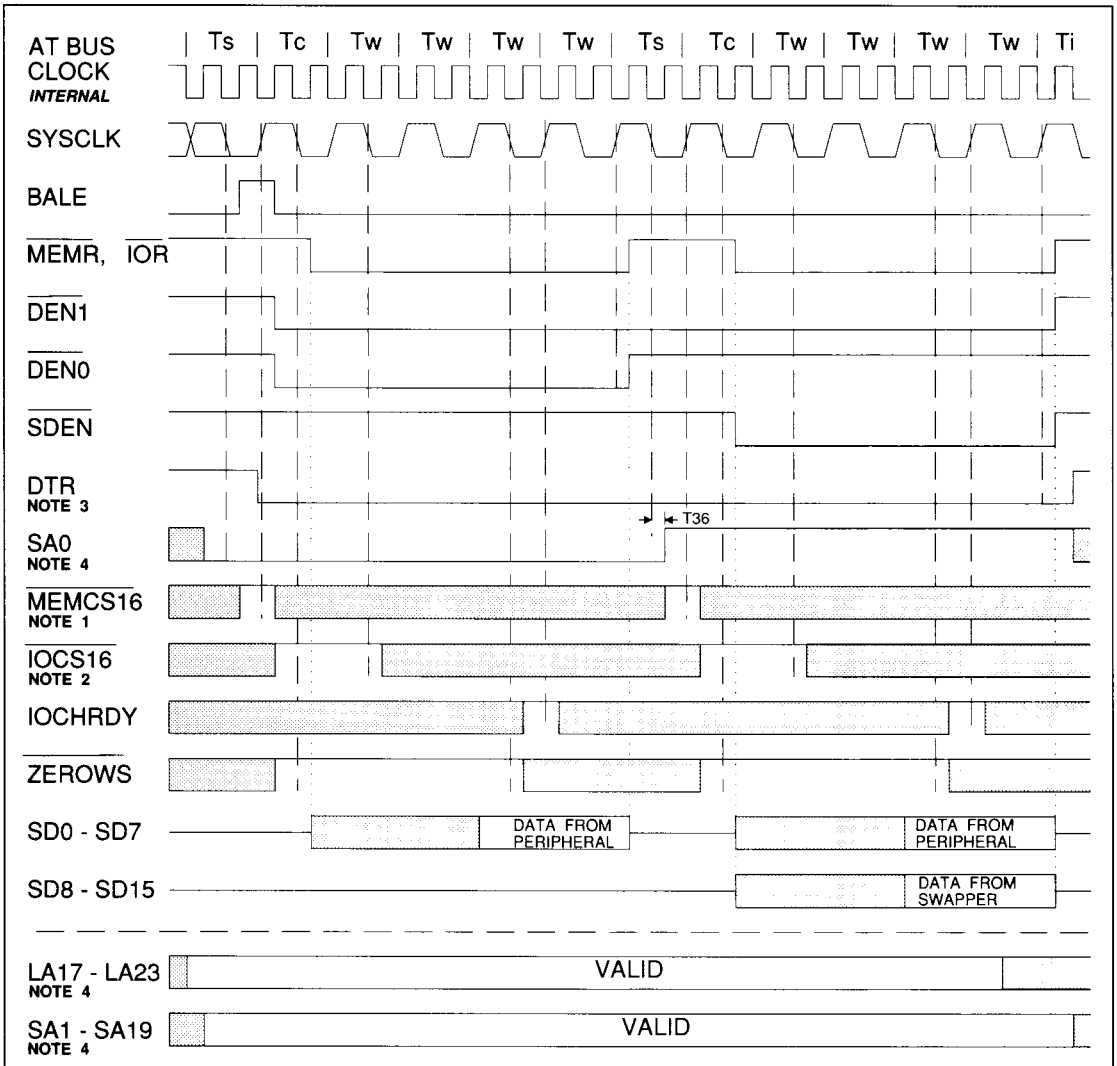

NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD8 - 15 when $\overline{\text{DEN1}}$ is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-21. AT BUS I/O OR MEMORY WRITE: 8-BIT, ODD BYTE, DEFAULT TIMING**




NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

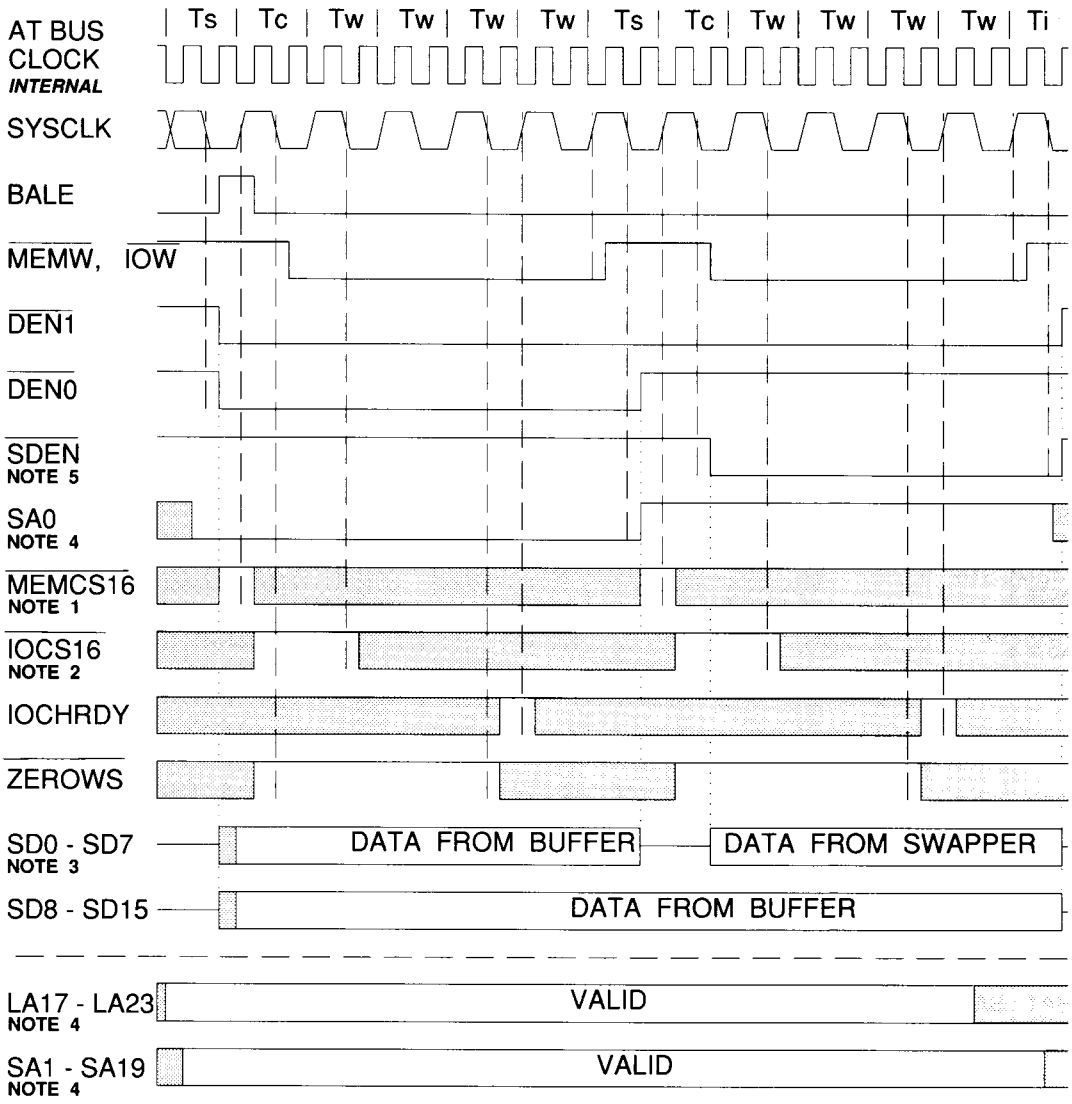
NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: SDTR is the inversion of DTR during CPU transfer cycles.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-22. AT BUS I/O OR MEMORY READ: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING**

10




NOTE 1: MEMCS16 is sampled only during memory cycles.

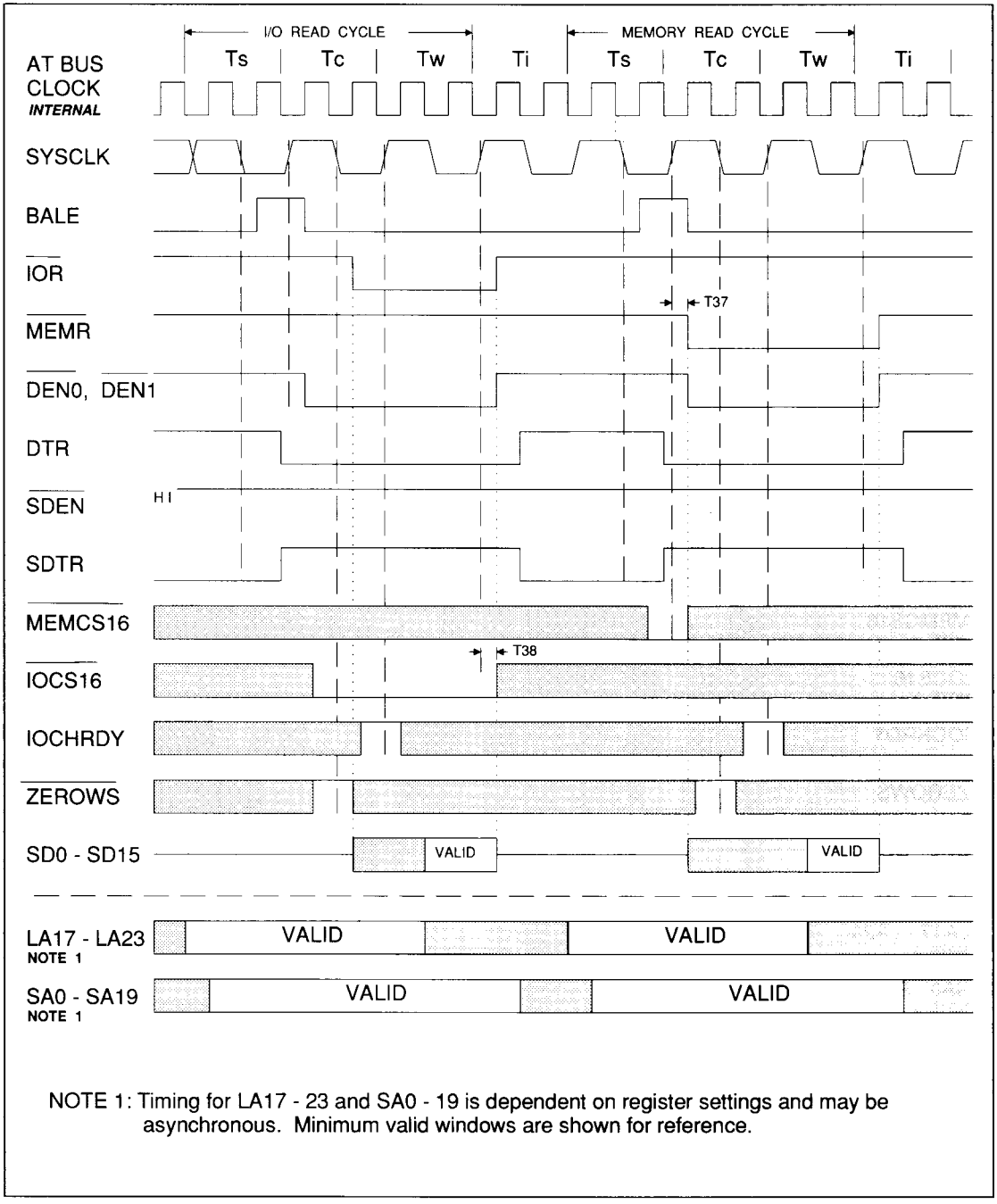
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when DEN0 is asserted is dependent on register settings and may be synchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

NOTE 5: SDTR remains low and DTR remains high for this cycle.

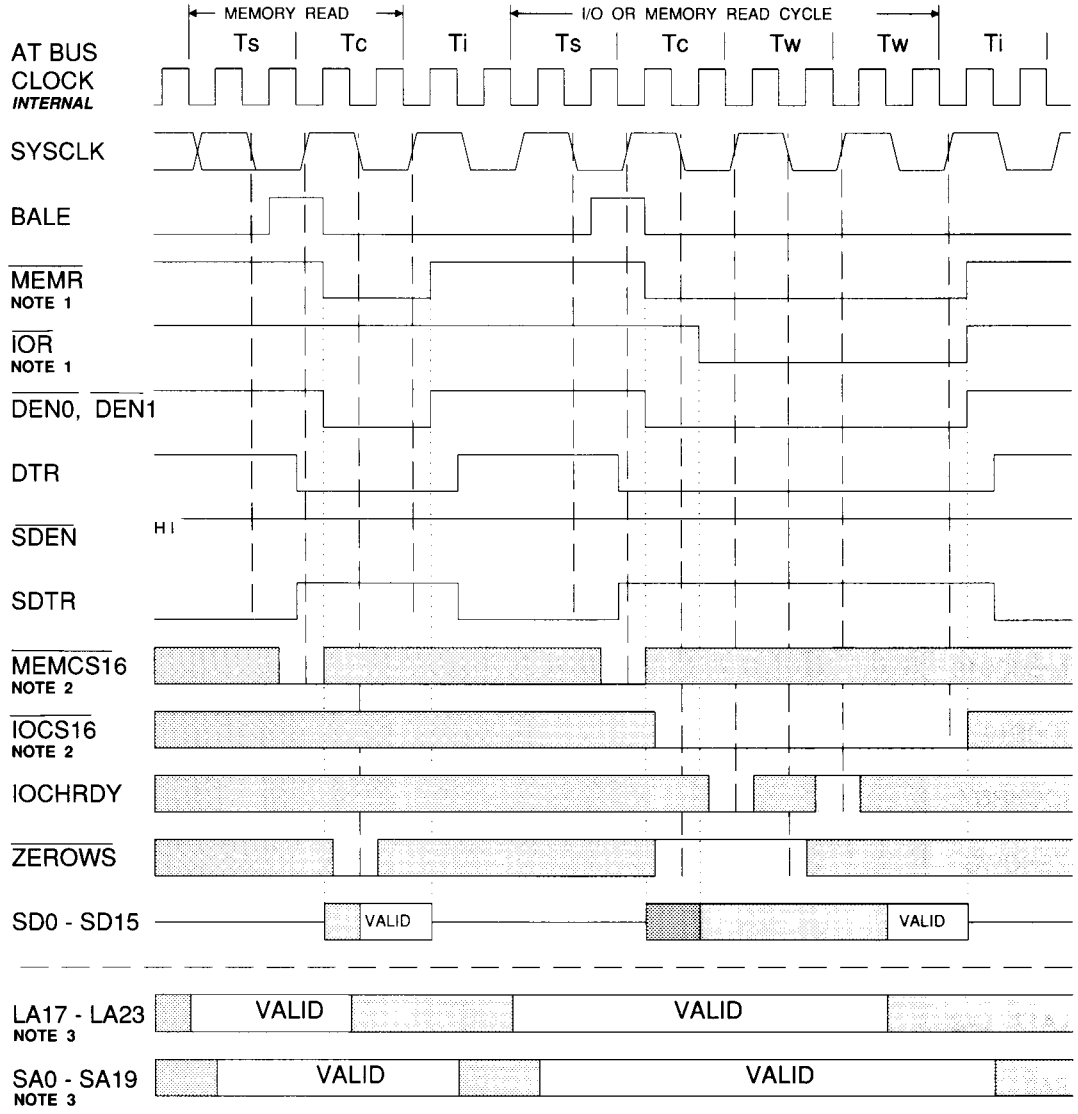
**FIGURE 13-23. AT BUS I/O OR MEMORY WRITE: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING**




NOTE 1: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-24. AT BUS I/O OR MEMORY READ: 16-BIT, DEFAULT TIMING**

10

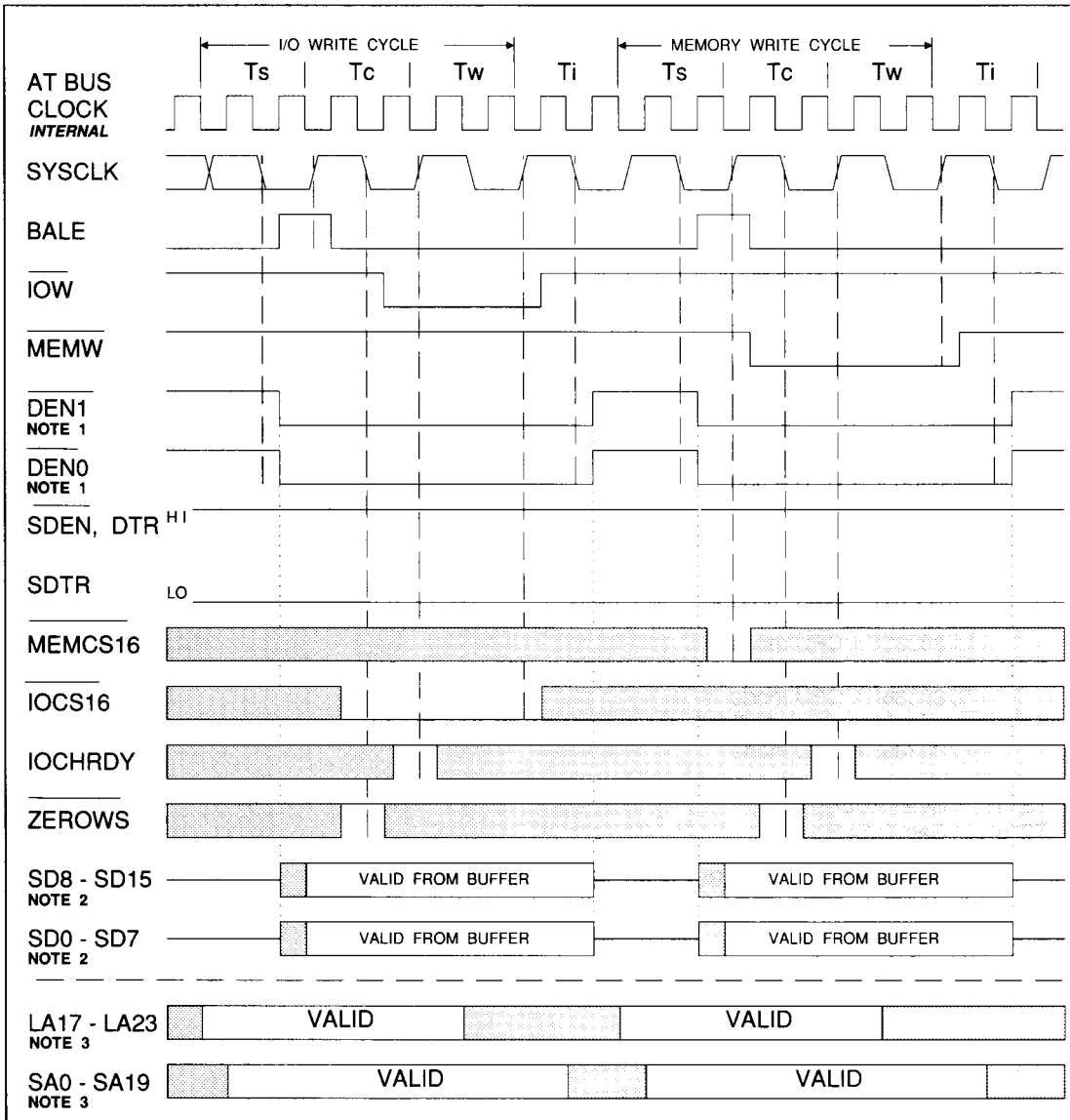



NOTE 1: $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ will not be asserted simultaneously. The first cycle must be to memory, as zero wait state I/O cycles are not supported.

NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles. $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-25. AT BUS I/O OR MEMORY READ: 16-BIT, 0WS ASSERTED AND EXTRA WAIT STATE ADDED**




NOTE 1: $\overline{\text{DEN0}}$ is asserted only in cycles where SA0 is low. $\overline{\text{DEN1}}$ is asserted only in cycles where $\overline{\text{SBHE}}$ is low.

NOTE 2: SD8 - SD15 are driven when $\overline{\text{DEN1}}$ is low. SD0 - SD7 are driven when $\overline{\text{DEN0}}$ is low. The small period of unknown data is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

**FIGURE 13-26. AT BUS I/O OR MEMORY WRITE: 16-BIT, DEFAULT TIMING**

10

### 13.2.2 Entering the AT Bus

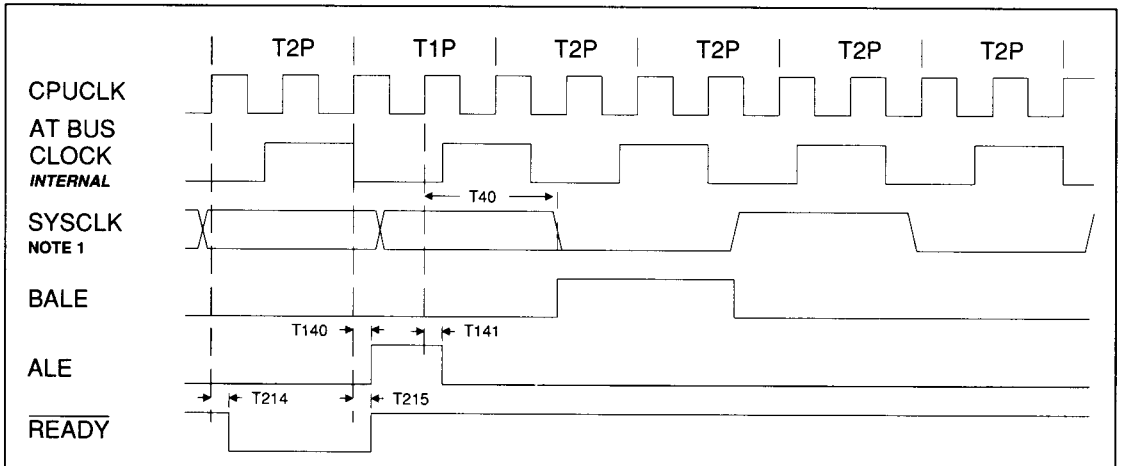
The timing in this section is presented in the following sequence:

80386SX CPU

Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T40 | CPUCLK rise to SYSCLK fall 80386SX CPU mode. | 4 | | ns | Register 1872H: BRQ_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25) |
| T41 | CPUCLK rise to SYSCLK fall 80386SX CPU mode. | 9 | | ns | Register 1872H: BRQ_DEL = 00 BUS_MOD = 0X Delay is number given plus (T00 × 0.5) |
| T42 | CPUCLK fall to SYSCLK fall 80386SX CPU mode. | | 29 | ns | Register 1872H: BRQ_DEL = 10 BUS_MOD = 11 |
| T43 | CPUCLK rise to SYSCLK fall 80386SX CPU mode. | | 35 | ns | Register 1872H: BRQ_DEL = 10 BUS_MOD = 10 |
| T140 | CPUCLK rise to ALE rise 80386SX CPU mode. | | 20 | ns | |
| T141 | CPUCLK rise to ALE fall 80386SX CPU mode. | | 20 | ns | |
| T214 | See TABLE 13-3 | | | | |
| T215 | See TABLE 13-3 | | | | |

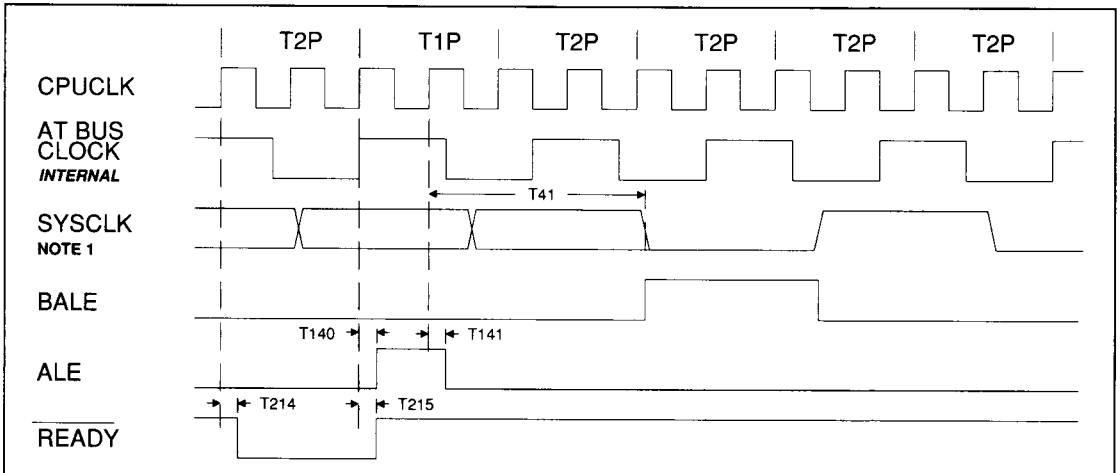
**TABLE 13-6. ENTERING THE AT BUS**




NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

**FIGURE 13-27. 80386SX CPU - BREQ DELAY = 1/2 CLOCK**

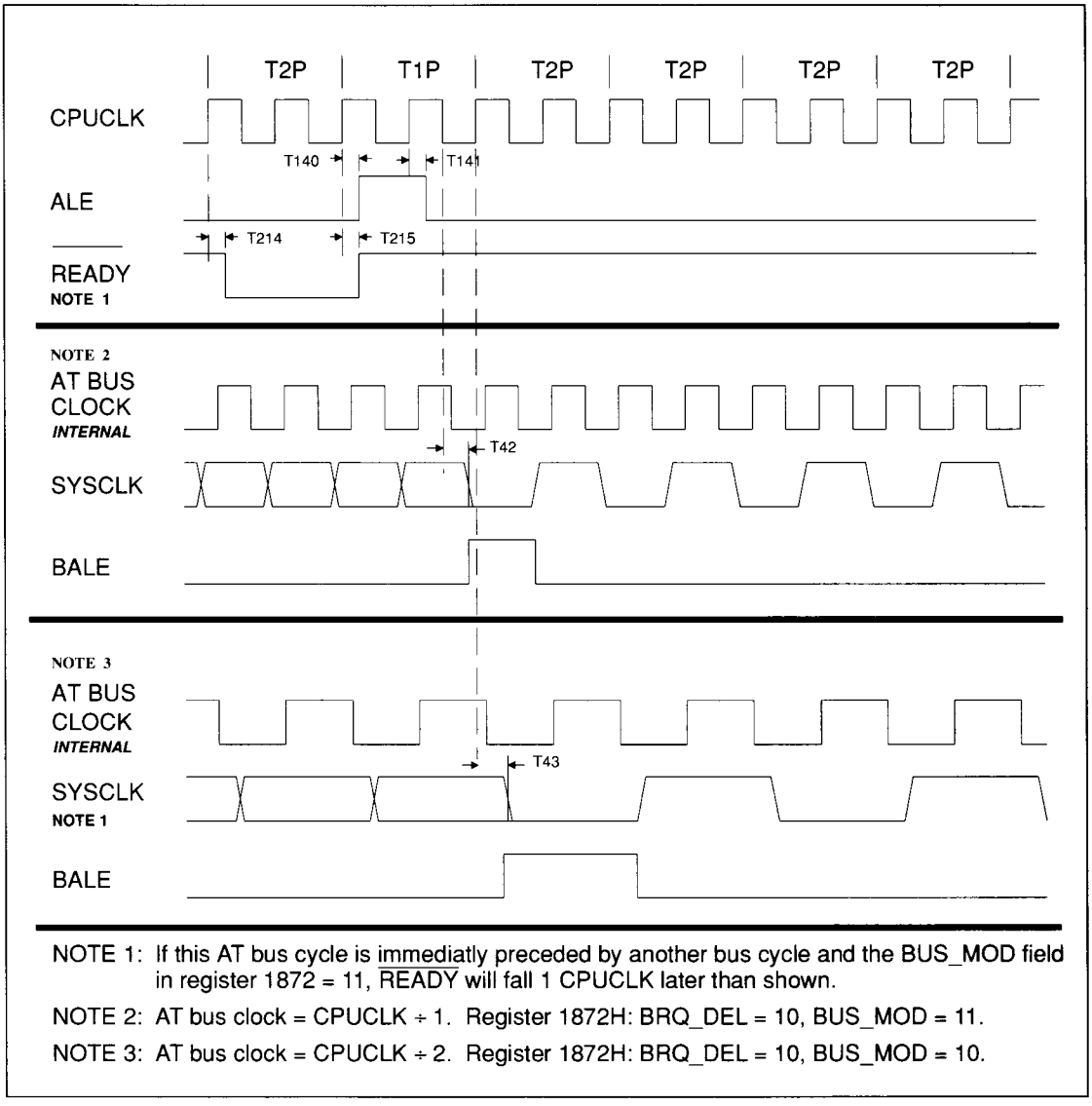



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

**FIGURE 13-28. 80386SX CPU - BREQ DELAY = 1 CLOCK**

10




NOTE 1: If this AT bus cycle is immediatly preceded by another bus cycle and the BUS_MOD field in register 1872 = 11, $\overline{\text{READY}}$ will fall 1 CPUCLK later than shown.

NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.

NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

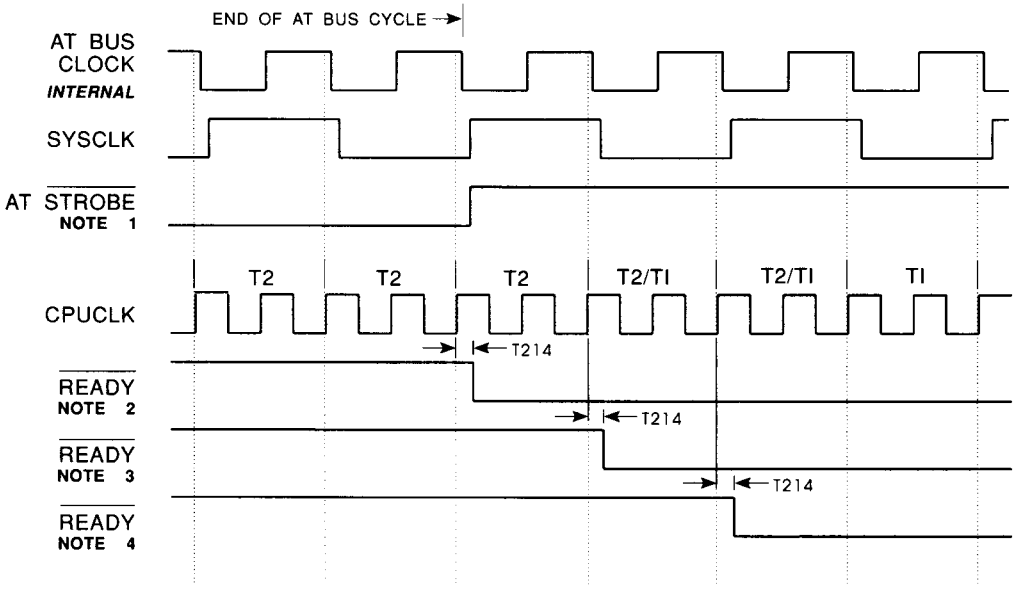
**FIGURE 13-29. 80386SX CPU - SYCNHRONOUS CPUCLK TO SYSCLK**

### 13.2.3 Exiting the AT Bus

Exiting a synchronous AT bus is covered first, followed by the asynchronous bus.

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T46 | SYSCLK fall to CPUCLK | -5 | | ns | Register 1872H: BAK_DEL = 10 BUS_MOD = 0X |
| T47 | SYSCLK fall to CPUCLK | -15 | | ns | Register 1872H: BAK_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25) |
| T48 | SYSCLK rise to CPUCLK | -10 | | ns | Register 1872H: BAK_DEL = 00 BUS_MOD = 0X |
| T49 | SYSCLK rise to CPUCLK | -15 | | ns | Register 1872H: BAK_DEL = 11 BUS_MOD = 0X Delay is number given plus (T00 × 0.25) |
| T214 | See TABLE 13-3 | | | | |
| T215 | See TABLE 13-3 | | | | |

**TABLE 13-7. EXITING THE AT BUS**




NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.
NOTE 2: Register 1872H: BUS_MOD = 10, BAK_DEL = 10 (-1 AT Bus Clock).
NOTE 3: Register 1872H: BUS_MOD = 10, BAK_DEL = 01 or 00 (-0.5 AT Bus Clock or no delay).
NOTE 4: Register 1872H: BUS_MOD = 10, BAK_DEL = 11 (+0.5 AT Bus Clock).

**FIGURE 13-30. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 2**

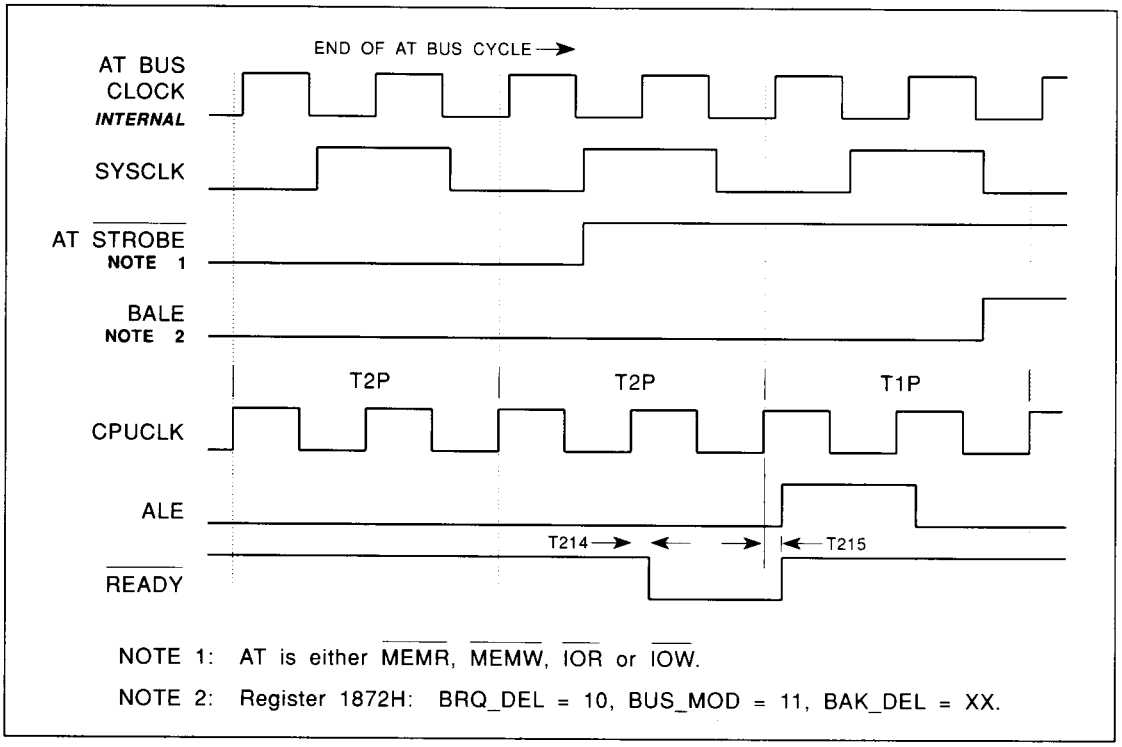
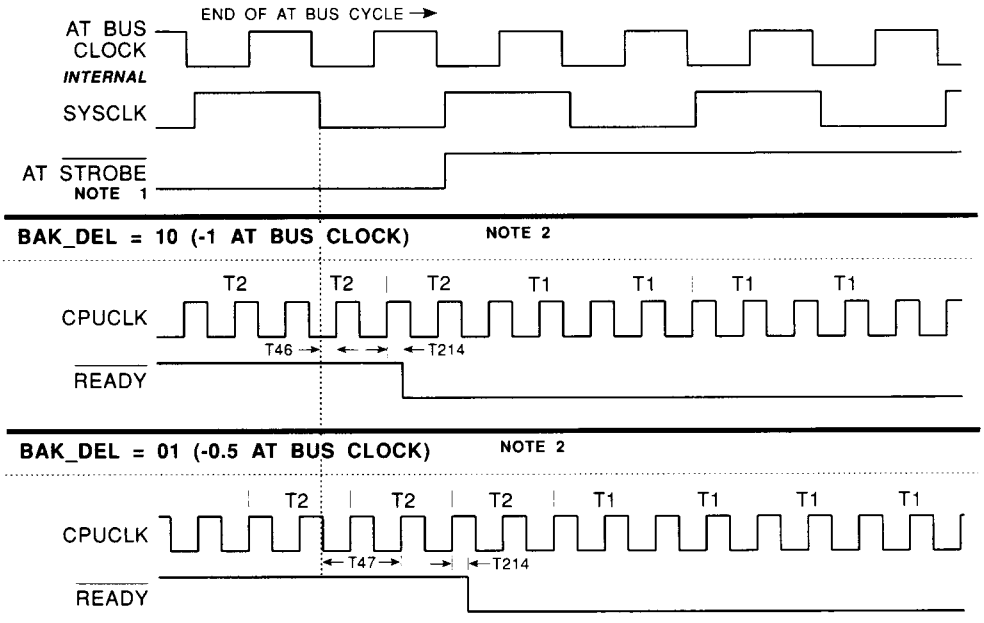


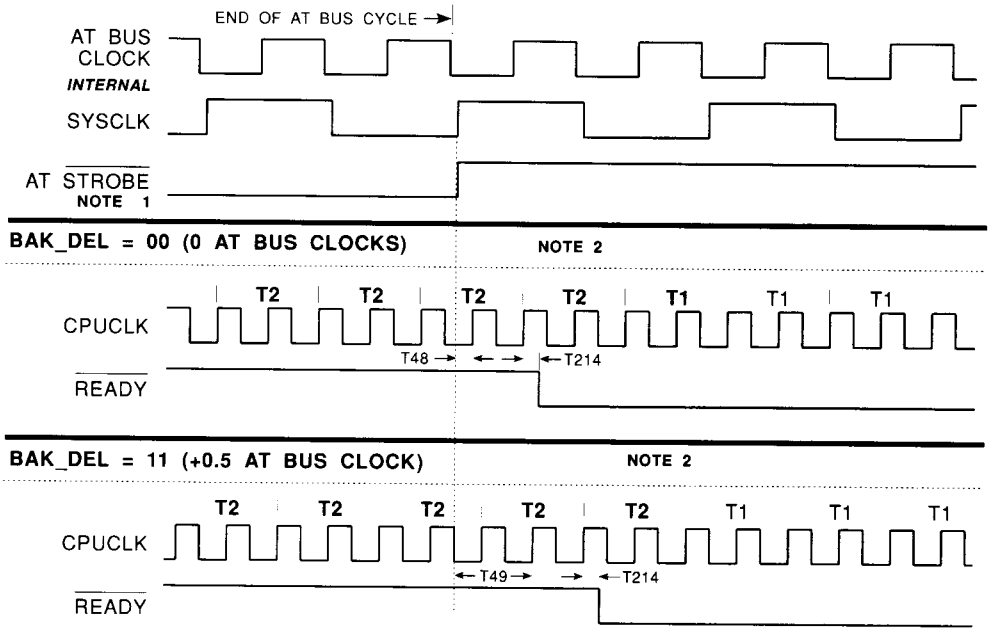

**FIGURE 13-31. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 1**

10




NOTE 1: AT STROBE is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.
NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.
NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for $\overline{\text{READY}}$ to be asserted is shown here. Reducing the delay further would cause $\overline{\text{READY}}$ to be asserted one CPU "T" state later.

**FIGURE 13-32. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = -1 OR -0.5 AT BUS CLOCKS**




NOTE 1: AT STROBE is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.
NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.
NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

**FIGURE 13-33. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = 0 OR +0.5 AT BUS CLOCKS**

10

### 13.2.4 DMA Cycles

Basic default timing is covered first, followed by 8-bit I/O to onboard memory, then onboard memory to 8-bit I/O.

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T50 | SYSCLK rise to ALE valid high | | 15 | ns | |
| T51 | SYSCLK rise to BALE valid high | | 15 | ns | |
| T52 | SYSCLK rise to AEN valid high | | 15 | ns | |
| T53 | SYSCLK rise to Address driven | 0 | | ns | |
| T54 | SYSCLK rise to Address valid | | 60 | ns | |
| T55 | Address hold from SYSCLK rise | 0 | | ns | |
| T56 | SYSCLK rise to LA20 valid | | 49 | ns | |
| T57 | LA20 hold from SYSCLK rise | 0 | | ns | |
| T58 | SYSCLK rise to SA0 valid | | 40 | ns | |
| T59 | SA0 hold from SYSCLK rise | 0 | | ns | |
| T60 | SYSCLK rise to $\overline{BHE}$ driven | 0 | | ns | |
| T61 | SYSCLK rise to $\overline{BHE}$ valid | | 36 | ns | |
| T62 | $\overline{BHE}$ hold from SYSCLK rise | 0 | | ns | |
| T63 | SYSCLK fall to MXCTL valid | | 2 | ns | |
| T64 | SYSCLK rise to DACKEN rise | | 28 | ns | |
| T65 | SYSCLK rise to DACKEN fall | | 31 | ns | |
| T66 | SYSCLK rise to $\overline{CSEN}$ fall | | 32 | ns | |
| T67 | SYSCLK rise to $\overline{CSEN}$ rise | | 33 | ns | |
| T68 | IOCHRDY setup to SYSCLK rise | 12 | | ns | |
| T69 | IOCHRDY hold from SYSCLK rise | 0 | | ns | |
| T70 | SYSCLK rise to $\overline{IOR}$ fall | | 28 | ns | |
| T71 | SYSCLK rise to $\overline{IOR}$ rise | | 35 | ns | |
| T72 | SYSCLK rise to $\overline{MEMW}$ fall | | 47 | ns | |
| T73 | SYSCLK rise to $\overline{MEMW}$ rise | | 35 | ns | |
| T74 | SYSCLK rise to $\overline{DEN1}$ fall | | 32 | ns | I/O to memory |
| T75 | SYSCLK rise to $\overline{DEN1}$ rise | | 42 | ns | I/O to memory |
| T76 | SYSCLK rise to $\overline{DEN0}$ fall | | 32 | ns | I/O to memory |
| T77 | SYSCLK rise to $\overline{DEN0}$ rise | | 42 | ns | I/O to memory |
| T78 | SYSCLK rise to $\overline{SDEN}$ fall | | 21 | ns | |
| T79 | SYSCLK rise to $\overline{SDEN}$ rise | | 37 | ns | I/O to memory |
| T80 | SYSCLK rise to SDTR rise | | 30 | ns | |
| T81 | SYSCLK rise to SDTR fall | | 20 | ns | |
| T82 | SYSCLK rise to $\overline{IOW}$ fall | | 53 | ns | |
| T83 | SYSCLK rise to $\overline{IOW}$ rise | | 37 | ns | |
| T84 | SYSCLK rise to $\overline{MEMR}$ fall | | 17 | ns | |
| T85 | SYSCLK rise to $\overline{MEMR}$ rise | | 38 | ns | |
| T86 | SYSCLK rise to $\overline{DEN1}$ fall | | 22 | ns | I/O to memory |
| T87 | SYSCLK rise to $\overline{DEN1}$ rise | | 116 | ns | I/O to memory |
| T88 | SYSCLK rise to $\overline{DEN0}$ fall | | 22 | ns | I/O to memory |
| T89 | SYSCLK rise to $\overline{DEN0}$ rise | | 116 | ns | I/O to memory |
| T90 | SYSCLK rise to $\overline{SDEN}$ rise | | 116 | ns | I/O to memory |
| T91 | SYSCLK rise to DTR rise | | 31 | ns | |
| T92 | SYSCLK rise to DTR fall | | 22 | ns | |

**TABLE 13-8. DMA CYCLES**

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T100 | $\overline{MEMW}$ fall to $\overline{RAS}$n fall | | 27 | ns | |
| T101 | $\overline{MEMW}$ rise to $\overline{RAS}$n rise | | 29 | ns | |
| T102 | $\overline{MEMW}$ fall to $\overline{CAS}$n fall | | 108 | ns | |
| T103 | $\overline{MEMW}$ rise to $\overline{CAS}$n rise | | 30 | ns | |
| T105 | $\overline{MEMW}$ fall to RA(11:00) valid | | 100 | ns | |
| T107 | $\overline{MEMW}$ fall to W/$\overline{R}$ high | | 29 | ns | |
| T108 | $\overline{MEMW}$ rise to W/$\overline{R}$ low | 10 | | ns | |
| T120 | $\overline{MEMR}$ fall to $\overline{RAS}$n fall | | 28 | ns | |
| T121 | $\overline{MEMR}$ rise to $\overline{RAS}$ rise | | 29 | ns | |
| T122 | $\overline{MEMR}$ fall to $\overline{CAS}$n fall | | 110 | ns | |
| T123 | $\overline{MEMR}$ rise to $\overline{CAS}$ rise | | 31 | ns | |
| T125 | $\overline{MEMR}$ fall to RA(10:00) valid | | 100 | ns | |
| T126 | $\overline{MEMR}$ fall to DPH, DPL float | | 25 | ns | |
| T127 | $\overline{MEMR}$ rise to DPH, DPL driven | 35 | | ns | |
| T303 | D(15:00) valid to DPH, DPL valid | | 27 | ns | |
| T305 | D(15:00) setup to $\overline{MEMR}$ rise | 18 | | ns | |
| T306 | DPH, DPL setup to $\overline{MEMR}$ rise | 10 | | ns | |

**TABLE 13-8. DMA CYCLES (Continued)**

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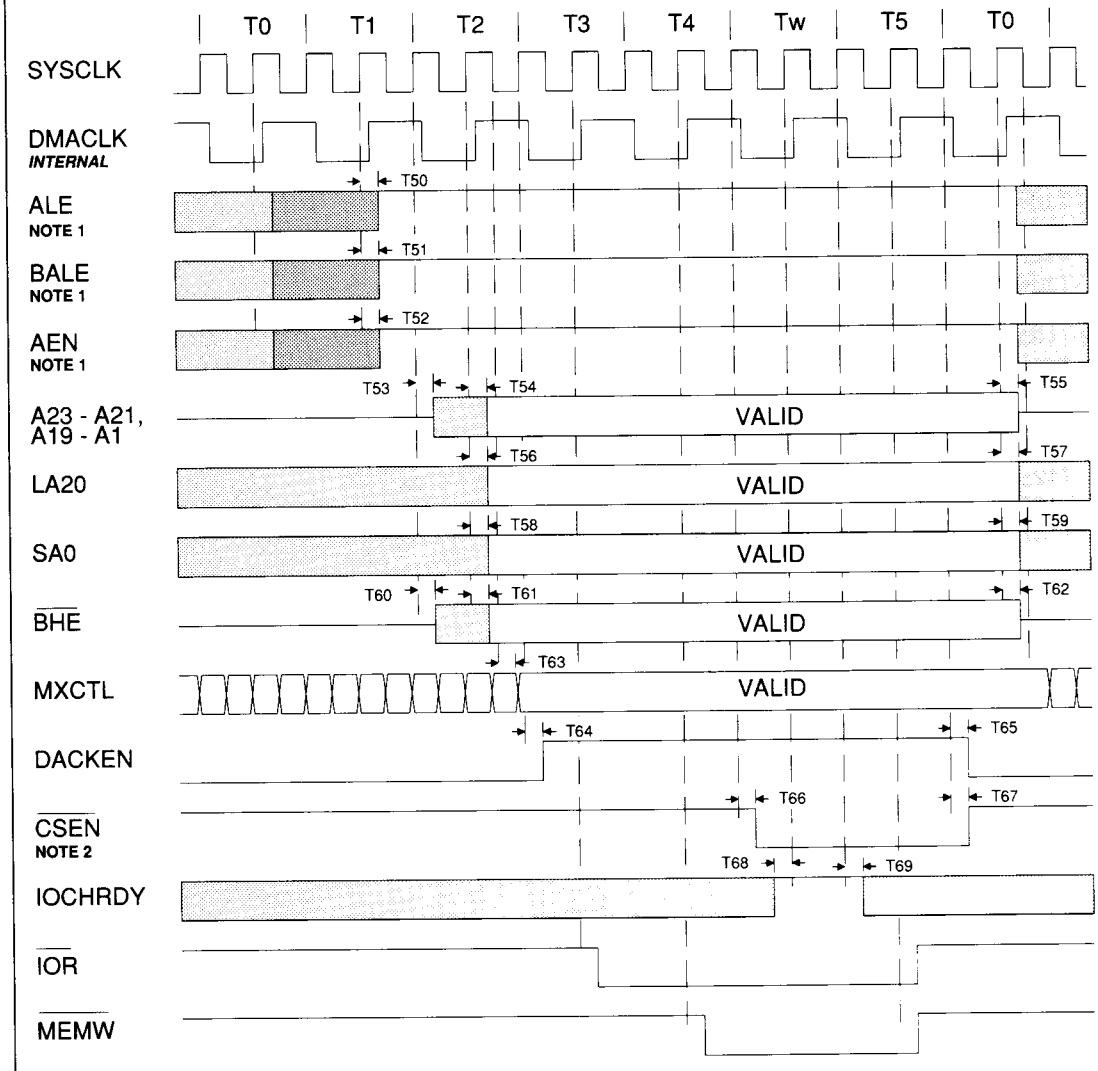
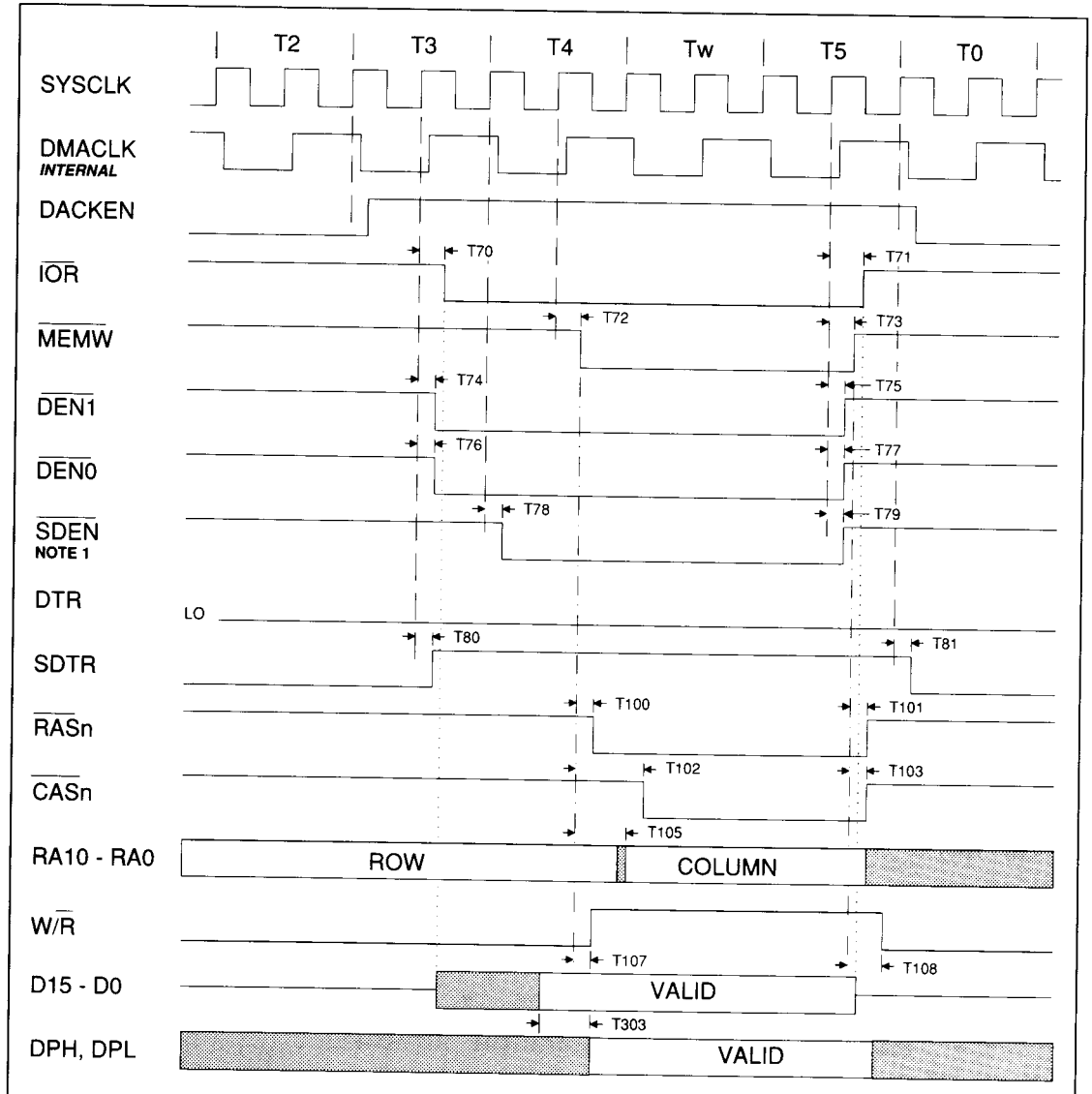



NOTE 1: ALE, BALE and AEN may be asynchronous. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid time as shown by the alternate shaded region.

NOTE 2: $\overline{\text{CSEN}}$ is used to generate the terminal count signal and pulses low only during the last transfer in a block.

**FIGURE 13-34. BASIC DMA CYCLE, DEFAULT TIMING**




NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.

**FIGURE 13-35. DMA CYCLE, 8-BIT I/O TO ON-BOARD MEMORY**

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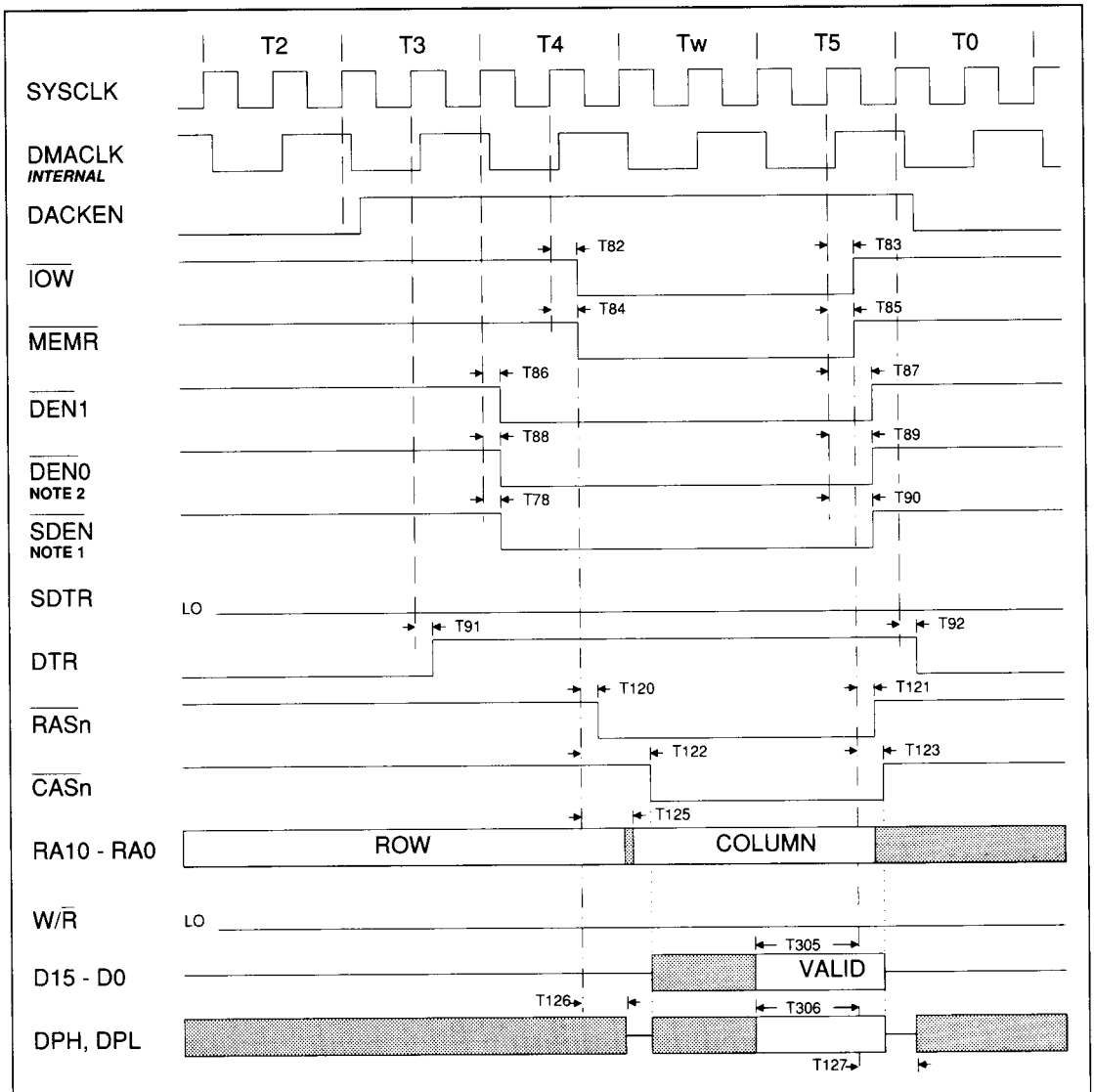


NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.

NOTE 2: $\overline{\text{DEN0}}$ is asserted only in cycles with an even numbered address.

**FIGURE 13-36. DMA CYCLE, ON-BOARD MEMORY TO 8-BIT I/O**

### 13.2.5 AT Bus Master

The AT bus master timing is covered in the following sequence:

- Bus acquisition and release
- Writing to the onboard memory
- Reading from the onboard memory

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T50 | SYSCLK rise to ALE valid high | | 15 | ns | |
| T51 | SYSCLK rise to BALE valid high | | 15 | ns | |
| T52 | SYSCLK rise to AEN valid high | | 15 | ns | |
| T53 | SYSCLK rise to Address driven | 0 | | ns | |
| T55 | Address hold from SYSCLK rise | 0 | | ns | |
| T60 | SYSCLK rise to $\overline{BHE}$ driven | 0 | | ns | |
| T61 | SYSCLK rise to $\overline{BHE}$ valid | | 36 | ns | |
| T62 | $\overline{BHE}$ hold from SYSCLK rise | 0 | | ns | |
| T63 | SYSCLK fall to MXCTL valid | | 2 | ns | |
| T64 | SYSCLK rise to DACKEN rise | | 28 | ns | |
| T65 | SYSCLK rise to DACKEN fall | | 31 | ns | |
| T150 | $\overline{MASTER}$ fall to AEN fall | | 30 | ns | |
| T151 | $\overline{MASTER}$ rise to AEN rise | | 30 | ns | |
| T152 | $\overline{MASTER}$ fall to A(23:21), A(19:01) float | | 30 | ns | |
| T153 | $\overline{MASTER}$ rise to A(23:21), A(19:01) driven | 15 | | ns | |
| T154 | $\overline{MASTER}$ fall to LA20 float | | 23 | ns | |
| T155 | $\overline{MASTER}$ rise to LA20 driven | 10 | | ns | |
| T156 | $\overline{MASTER}$ fall to SA0 float | | 24 | ns | |
| T157 | $\overline{MASTER}$ rise to SA0 driven | 10 | | ns | |
| T158 | $\overline{MASTER}$ fall to $\overline{BHE}$ float | | 30 | ns | |
| T159 | $\overline{MASTER}$ rise to $\overline{BHE}$ driven | 10 | | ns | |
| T160 | $\overline{MASTER}$ fall to $\overline{CSEN}$ fall | | 32 | ns | |
| T161 | $\overline{MASTER}$ rise to $\overline{CSEN}$ rise | | 35 | ns | |
| T162 | $\overline{MASTER}$ fall to $\overline{MEMR}$ float | | 24 | ns | |
| T163 | $\overline{MASTER}$ rise to $\overline{MEMR}$ driven | 10 | | ns | |
| T164 | $\overline{MASTER}$ fall to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, float | | 23 | ns | |
| T165 | $\overline{MASTER}$ rise to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$ driven | 10 | | ns | |
| T166 | A(23:21), A(19:01) setup to $\overline{MEMR}$, $\overline{MEMW}$ | 45 | | ns | |
| T167 | LA20 setup to $\overline{MEMR}$, $\overline{MEMW}$ | 50 | | ns | |
| T168 | $\overline{BHE}$ setup to $\overline{MEMR}$, $\overline{MEMW}$ | 0 | | ns | |
| T169 | SA0 setup to $\overline{MEMR}$, $\overline{MEMW}$ | 0 | | ns | |
| T170 | A(23:21), A(19:01) hold from $\overline{MEMR}$, $\overline{MEMW}$ | 15 | | ns | |
| T171 | LA20 hold from $\overline{MEMR}$, $\overline{MEMW}$ | 15 | | ns | |
| T172 | $\overline{BHE}$ hold from $\overline{MEMR}$, $\overline{MEMW}$ | 15 | | ns | |
| T173 | SA0 hold from $\overline{MEMR}$, $\overline{MEMW}$ | 15 | | ns | |
| T174 | SA0 in to A0 out delay | | 45 | ns | |
| T175 | $\overline{MEMW}$ fall to $\overline{DEN1}$ fall | | 30 | ns | |
| T176 | $\overline{MEMW}$ fall to $\overline{DEN0}$ fall | | 30 | ns | |
| T177 | $\overline{MEMW}$ rise to $\overline{DEN1}$ rise | | 83 | ns | |
| T178 | $\overline{MEMW}$ rise to $\overline{DEN0}$ rise | | 83 | ns | |

**TABLE 13-9. AT BUS MASTER CYCLE**

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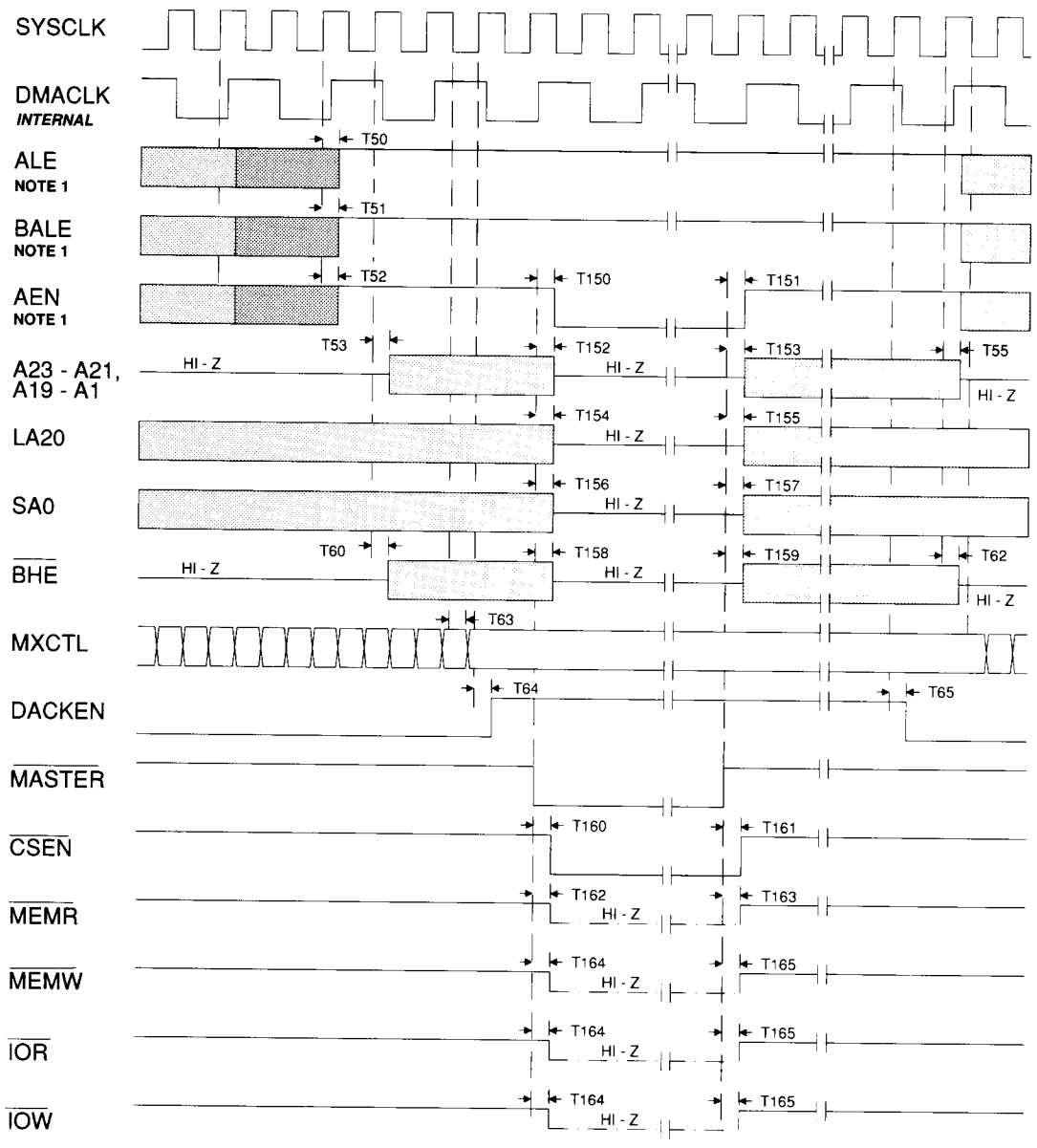
| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T179 | $\overline{MEMR}$ fall to $\overline{DEN1}$ fall | | 85 | ns | |
| T180 | $\overline{MEMR}$ fall to $\overline{DEN0}$ fall | | 85 | ns | |
| T181 | $\overline{MEMR}$ rise to $\overline{DEN1}$ rise | | 32 | ns | |
| T182 | $\overline{MEMR}$ rise to $\overline{DEN0}$ rise | | 32 | ns | |
| T183 | $\overline{MEMR}$ fall to DTR rise | | 29 | ns | |
| T184 | $\overline{MEMR}$ rise to DTR fall | | 82 | ns | |
| T190 | $\overline{MEMR}$, $\overline{MEMW}$ fall to $\overline{RASn}$ fall | | 83 | ns | |
| T191 | $\overline{MEMR}$, $\overline{MEMW}$ rise to $\overline{RASn}$ rise | | 33 | ns | |
| T192 | $\overline{MEMR}$, $\overline{MEMW}$ fall to $\overline{CASn}$ fall | | 126 | ns | |
| T193 | $\overline{MEMR}$, $\overline{MEMW}$ rise to $\overline{CASn}$ rise | | 33 | ns | |
| T194 | $\overline{MEMR}$, $\overline{MEMW}$ fall to RA(10:00) column address valid | | 120 | ns | |
| T196 | $\overline{MEMR}$, $\overline{MEMW}$ fall to RA(10:00) row address valid | | 42 | ns | |
| T197 | RA(10:00) column address hold from $\overline{MEMR}$, $\overline{MEMW}$ rise | 5 | | ns | |
| T300 | $\overline{MEMW}$ fall to W/$\overline{R}$ rise | | 33 | ns | |
| T301 | $\overline{MEMW}$ rise to W/$\overline{R}$ fall | 10 | | ns | |
| T302 | $\overline{MEMW}$ fall to DPH, DPL valid | | 32 | ns | |
| T303 | D(15:00) valid to DPH, DPL valid | | 27 | ns | |
| T304 | DPH, DPL hold from $\overline{MEMW}$ rise | 5 | | ns | |
| T305 | D(15:00) setup to $\overline{MEMR}$ rise | 18 | | ns | |
| T306 | DPH, DPL setup to $\overline{MEMR}$ rise | 10 | | ns | |
| T307 | $\overline{MEMR}$ fall to DPH, DPL float | | 35 | ns | |
| T308 | $\overline{MEMR}$ rise to DPH, DPL driven | 58 | | ns | |

**TABLE 13-9. AT BUS MASTER CYCLE (Continued)**




NOTE 1: The shaded regions of ALE, BALE and AEN show a possible asynchronous relarionship. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid HI time as shown by the alternate shading.

**FIGURE 13-37. AT BUS MASTER, BUS ACQUISITION/RELEASE**

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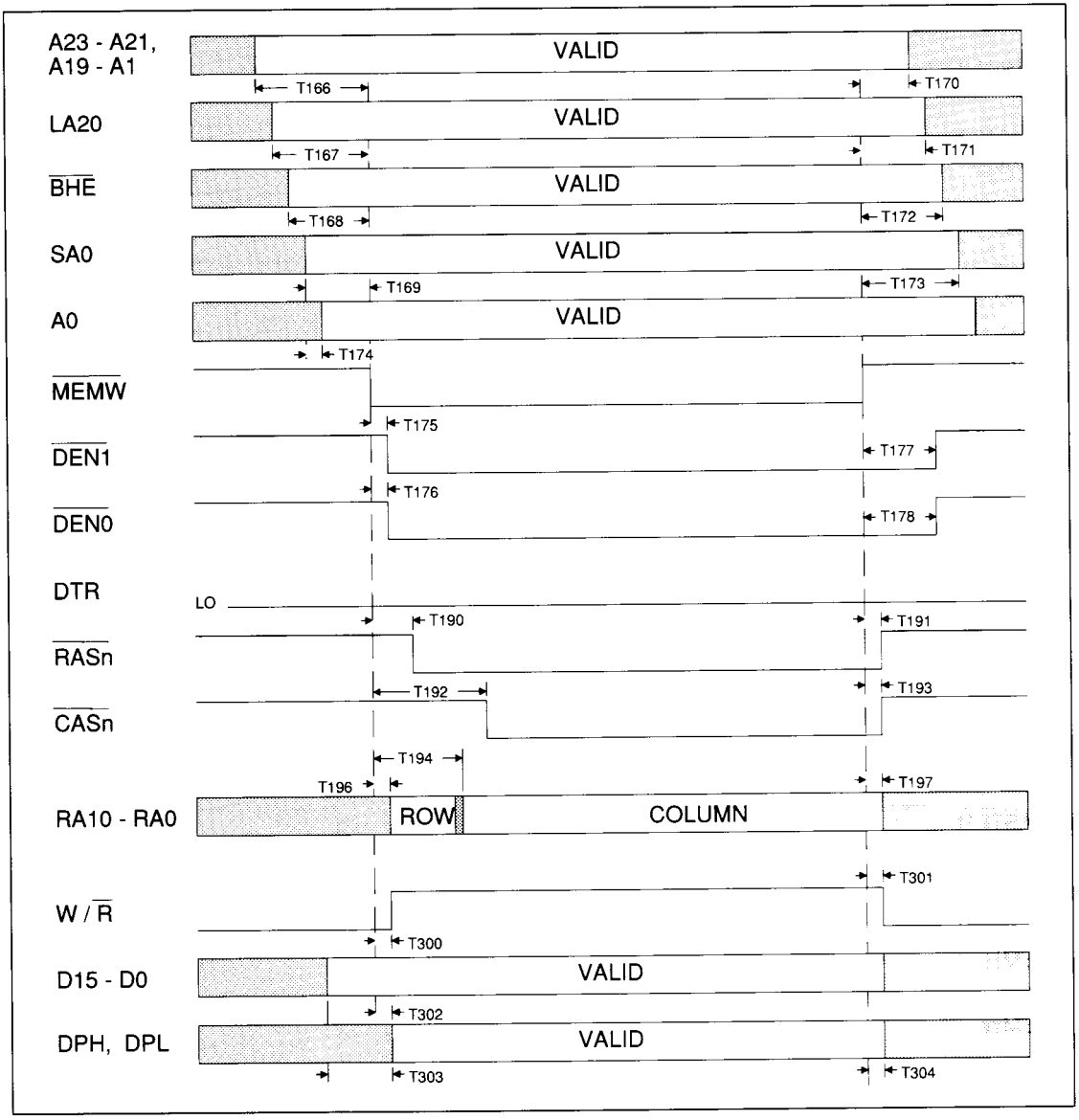


**FIGURE 13-38. AT BUS MASTER, WRITE TO ON-BOARD MEMORY**

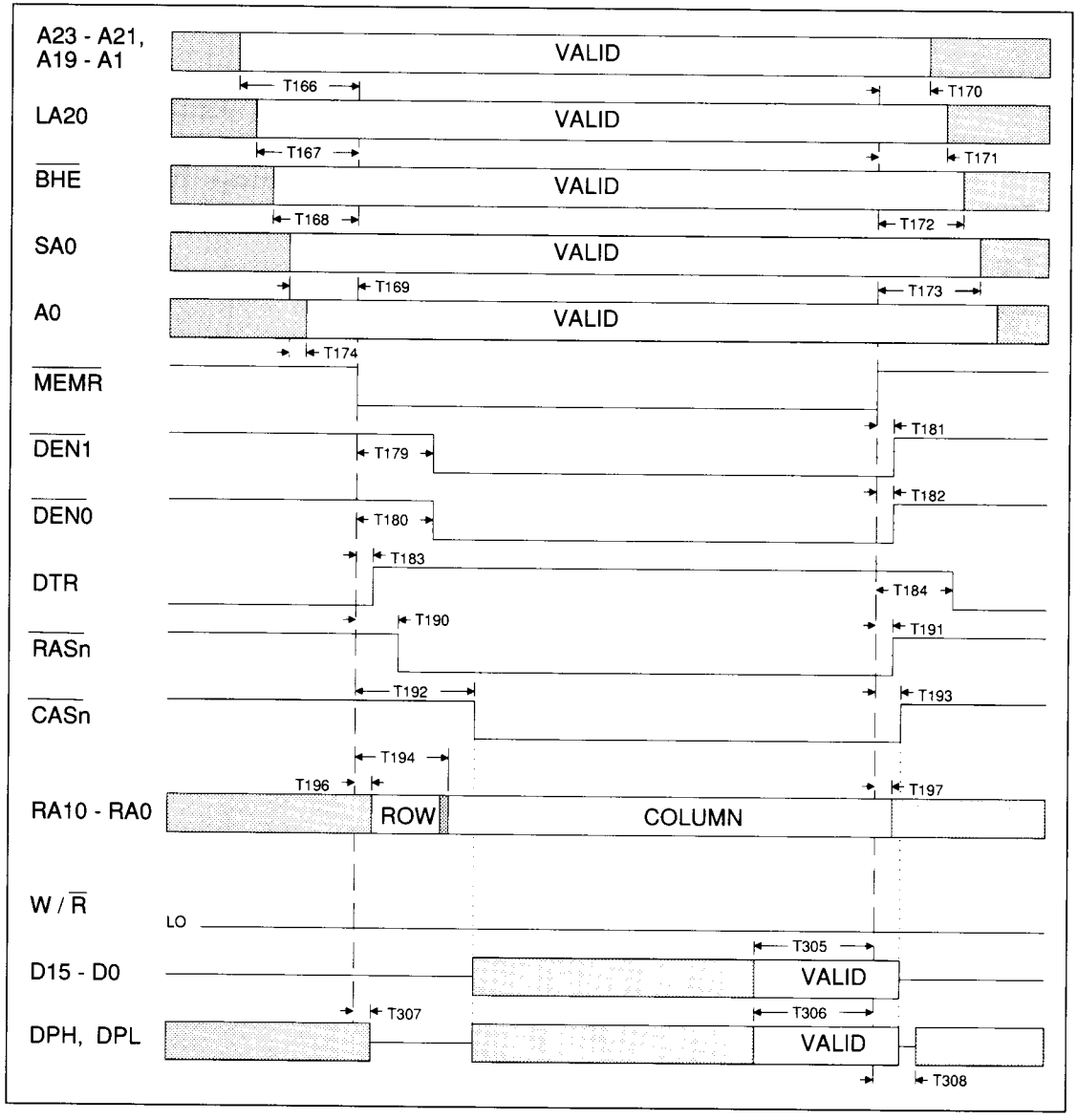


**FIGURE 13-39. AT BUS MASTER, READ FROM ON-BOARD MEMORY**

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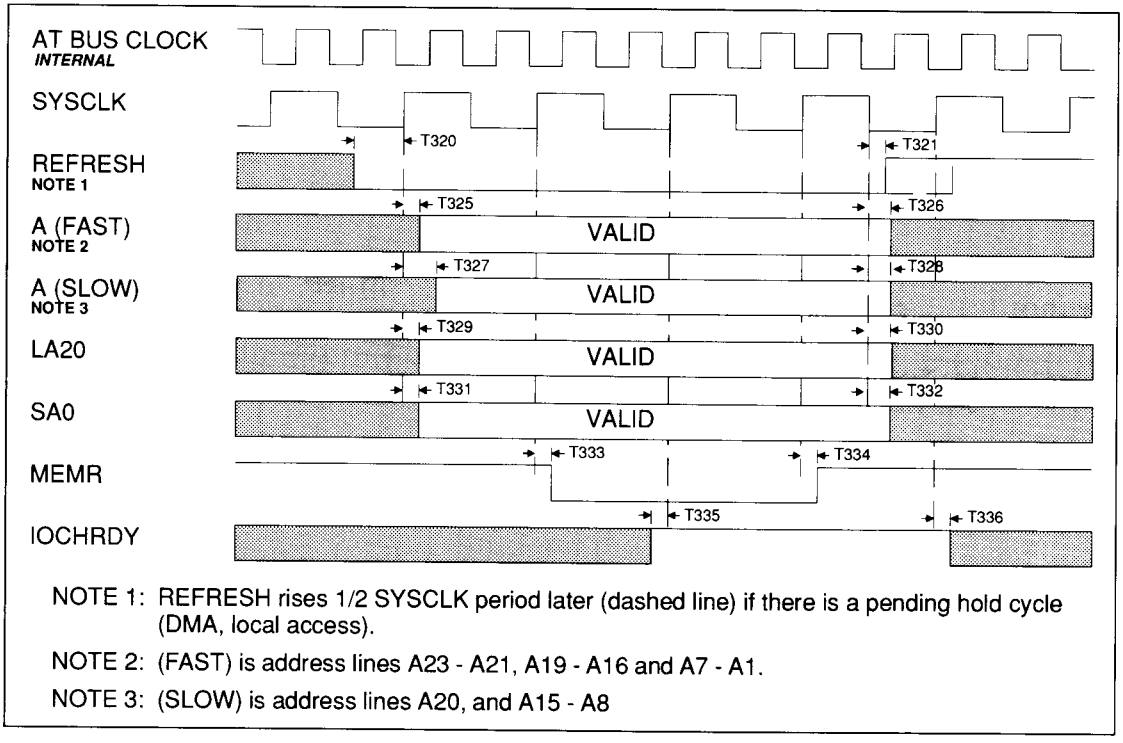
### 13.2.6 AT Bus Refresh

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| T320 | $\overline{\text{REFRESH}}$ low before SYSCLK rise | 4 | | ns | $\overline{\text{REFRESH}}$ setup is number given plus (T00 × 0.25) |
| T321 | SYSCLK fall to $\overline{\text{REFRESH}}$ rise | | 16 | ns | |
| T325 | SYSCLK rise to A(23:21), A(19:16) and A(07:01) valid | | 35 | ns | |
| T326 | SYSCLK fall to A(23:21), A(19:16) and A(07:01) invalid | 2 | | ns | |
| T327 | SYSCLK rise to A20, A(15:08) valid | | 45 | ns | |
| T328 | SYSCLK fall to A20, A(15:08) invalid | 2 | | ns | |
| T329 | SYSCLK rise to LA20 valid | | 30 | ns | |
| T330 | SYSCLK fall to LA20 invalid | 2 | | ns | |
| T331 | SYSCLK rise to SA0 valid | | 30 | ns | |
| T332 | SYSCLK fall to SA0 invalid | 2 | | ns | |
| T333 | SYSCLK rise to $\overline{\text{MEMR}}$ low | | 8 | ns | |
| T334 | SYSCLK rise to $\overline{\text{MEMR}}$ high | | 7 | ns | |
| T335 | IOCHRDY setup to SYSCLK rise | 23 | | ns | |
| T336 | IOCHRDY hold time from SYSCLK rise | 0 | | ns | |

**TABLE 13-10. AT BUS REFRESH CYCLE, DEFAULT TIMING**




NOTE 1: REFRESH rises 1/2 SYSCLK period later (dashed line) if there is a pending hold cycle (DMA, local access).

NOTE 2: (FAST) is address lines A23 - A21, A19 - A16 and A7 - A1.

NOTE 3: (SLOW) is address lines A20, and A15 - A8

**FIGURE 13-40. AT BUS REFRESH CYCLE, DEFAULT TIMING**

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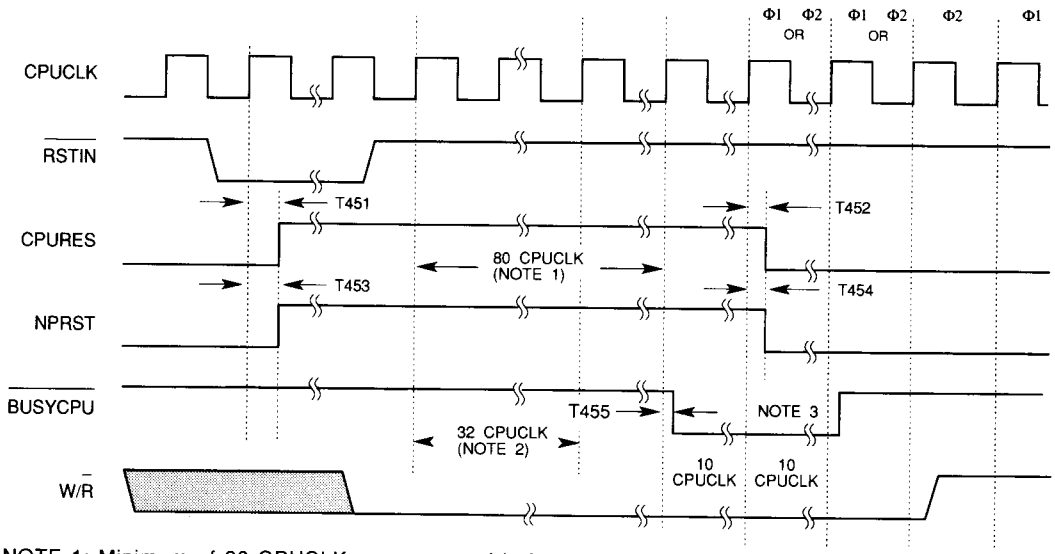
### 13.3 PROCESSOR TIMING

This section covers the 80386SX CPU timing. The parameters for the WD7855LV that differ from these are marked with an * and appear in the appendix.

| SYMBOL | CHARACTERISTICS | 20 MHz | | 25 MHz | | 33 MHz | | |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| T140 | See Table 13-6 | | | | | | | |
| T141 | See Table 13-6 | | | | | | | |
| T204 | See Table 13-3 | | | | | | | |
| T214 | See Table 13-3 | | | | | | | |
| T215 | See Table 13-3 | | | | | | | |
| T451 | CPUCLK rise to CPURES rise delay | | 14 | | 10 | | 10 | ns |
| T452 | CPUCLK rise to CPURES fall delay | | 13 | | 10 | | 10 | ns |
| T453 | CPUCLK rise to NPRST rise delay | | 14 | | 10 | | 10 | ns |
| T454 | CPUCLK rise to NPRST fall delay | | 13 | | 10 | | 10 | ns |
| T455 | CPUCLK rise to BUSYCPU fall delay | | 35 | | 35 | | 35 | ns |
| T456 | CPUCLK rise to BUSYCPU rise delay | | 35 | | 30 | | 30 | ns |
| T457 | NPBUSY fall to BUSYCPU fall delay | | 30 | | 30 | | 30 | ns |
| T458 | NPBUSY rise to BUSYCPU rise delay | | 35 | | 35 | | 35 | ns |
| T460 | NPERR fall to EPEREQ rise delay | | 30 | | 30 | | 30 | ns |
| T462 | ADS setup time to CPUCLK rise * | 14 | | 10 | | 10 | | ns |
| T463 | ADS hold time from CPUCLK rise | 5 | | 4 | | 4 | | ns |
| T464 | W/R setup time to CPUCLK rise * | 14 | | 8 | | 8 | | ns |
| T465 | W/R hold time from CPUCLK rise | 5 | | 4 | | 4 | | ns |
| T466 | D/C setup time to CPUCLK rise * | 14 | | 6 | | 6 | | ns |
| T467 | D/C hold time from CPUCLK rise | 5 | | 4 | | 4 | | ns |
| T468 | M/IO setup time to CPUCLK rise * | 17 | | 15 | | 15 | | ns |
| T469 | M/IO hold time from CPUCLK rise | 5 | | 4 | | 4 | | ns |
| T470 | BHE setup time to CPUCLK rise | 17 | | 15 | | 15 | | ns |
| T471 | BHE hold time from CPUCLK rise | 3 | | 4 | | 4 | | ns |
| T472 | HOLDA setup time to CPUCLK rise | 10 | | 6 | | 6 | | ns |
| T473 | HOLDA hold time from CPUCLK rise | 3 | | 4 | | 4 | | ns |
| T474 | HOLDR valid delay from CPUCLK rise * | | 26 | | 20 | | 20 | ns |
| T475 | DPH setup time to CPUCLK rise | 5 | | 5 | | 5 | | ns |
| T476 | DPH hold time from CPUCLK rise | 19 | | 19 | | 19 | | ns |
| T477 | D(15:00) setup time to CPUCLK rise | 5 | | 5 | | 5 | | ns |
| T478 | D(15:00) hold time from CPUCLK rise | 19 | | 19 | | 15 | | ns |
| T479 | A(23:01), BLE setup time to CPUCLK rise * | 40 | | 38 | | 30 | | ns |
| T480 | A(23:01), BLE hold time from CPUCLK rise | 3 | | 4 | | 4 | | ns |

**TABLE 13-11. 80386SX CPU TIMING**

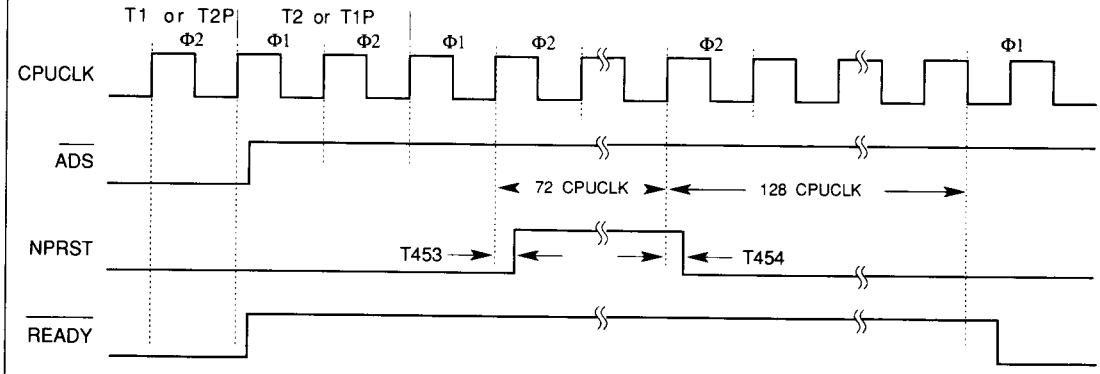



NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R, the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

**FIGURE 13-41. 80386SX - CPURES AND NPRST DURING POWER UP**



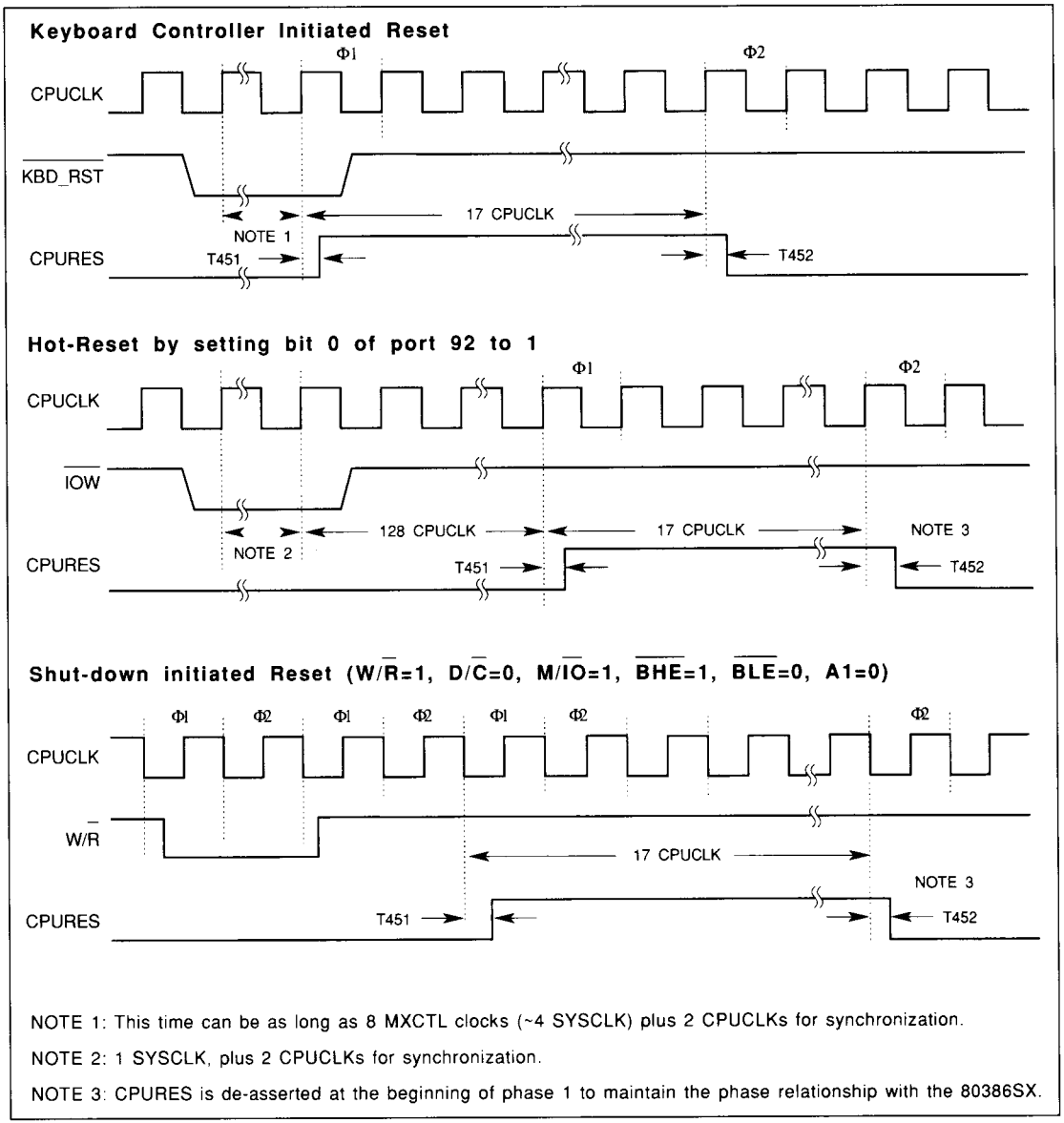

NOTE 1: The trailing edge of NPRST occurs during phase 2 to maintain the correct phase of 80387SX with the 80386SX.

NOTE 2: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80387SX.

NOTE 3: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed.

NOTE 4: 25 MHz and 33 MHz operation requires a minimum of 8 MHz for AT Bus Clock.

**FIGURE 13-42. 80386SX - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1**




NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is de-asserted at the beginning of phase 1 to maintain the phase relationship with the 80386SX.

**FIGURE 13-43. 80386SX - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET**

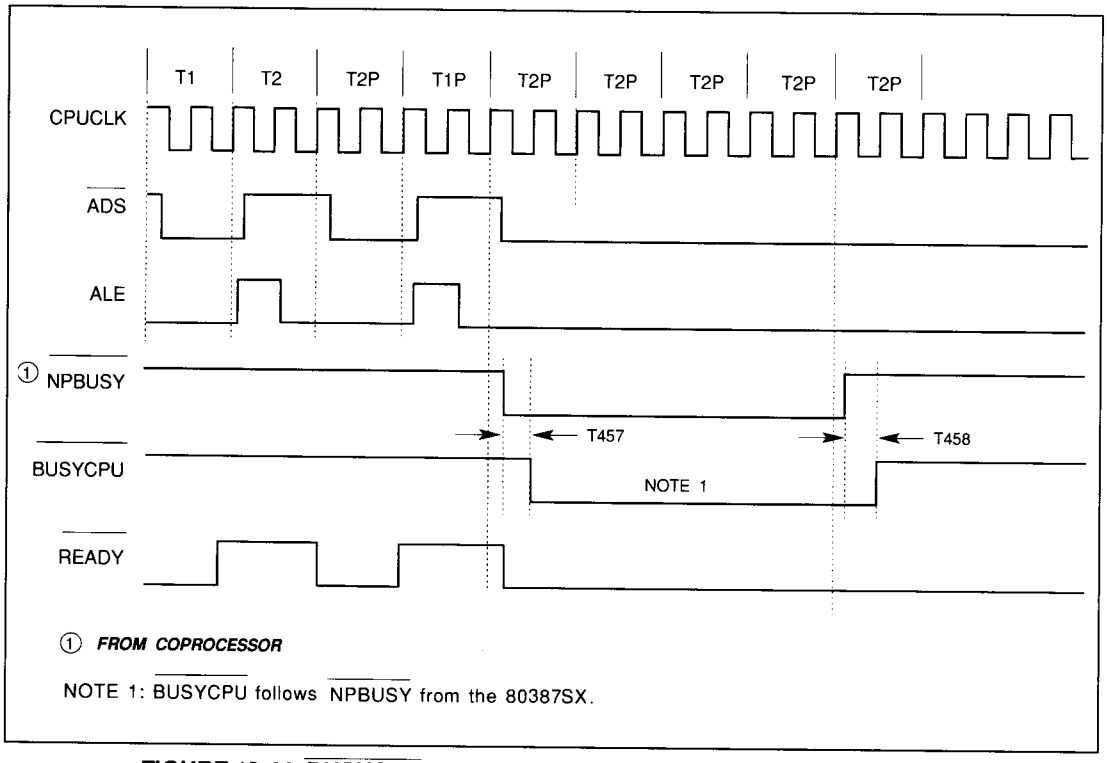



**FIGURE 13-44. BUSYCPU ASSERTION DURING COPROCESSOR ACCESS**

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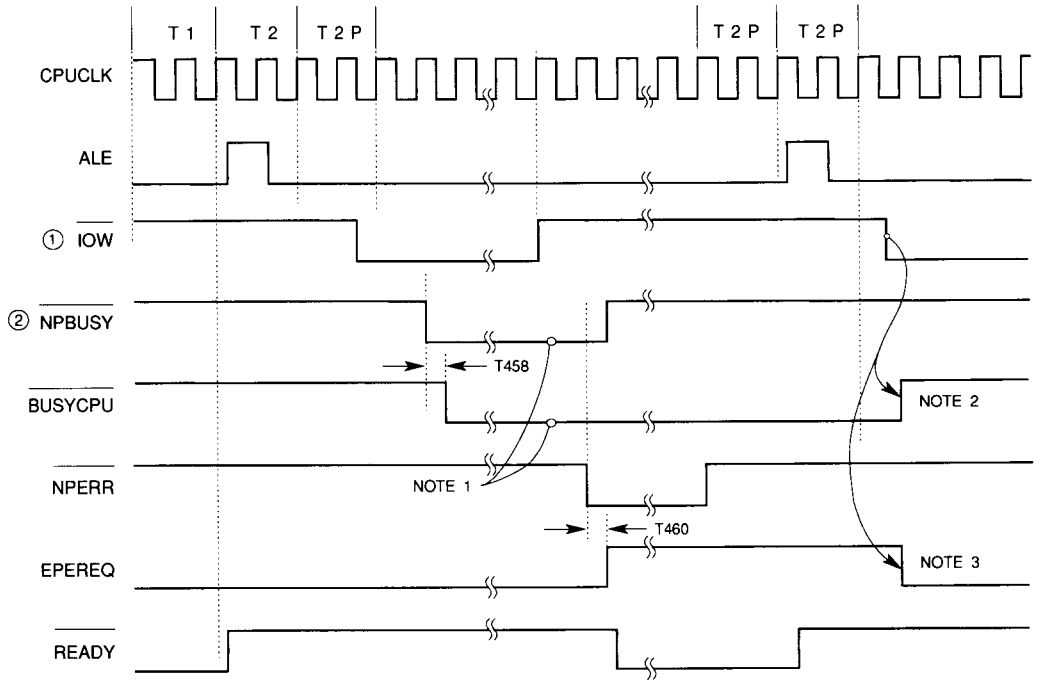


① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW delayed by a low half of SYSCLK when any data is written to port F0. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

NOTE 3: EPEREQ is asserted if NPERR occurs while NPBUSY from the coprocessor is active. EPEREQ is de-asserted by the leading edge of IOW delayed by the low half of SYSCLK when any data is written to port F0. EPEREQ can be asynchronous to the processor and is shown for reference only.

**FIGURE 13-45. 80386SX - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0**

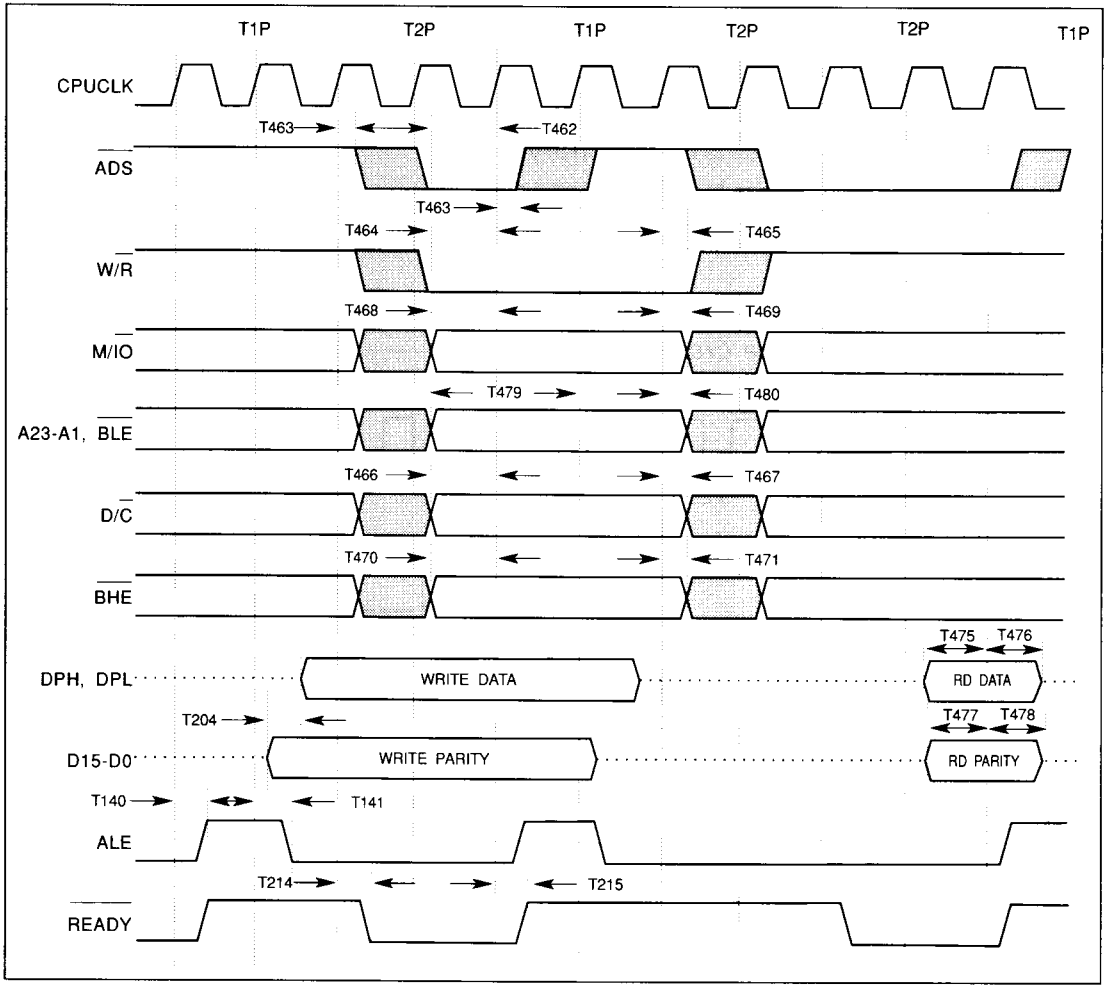


**FIGURE 13-46. 80386SX - MISCELLANEOUS TIMING**

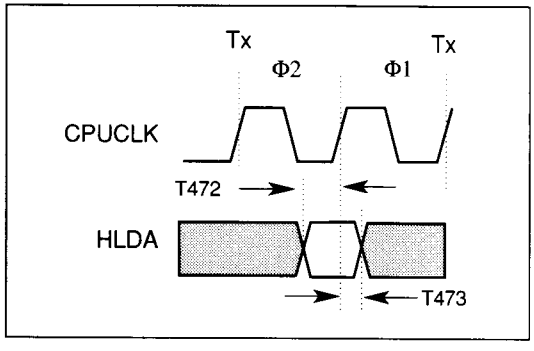


**FIGURE 13-47. 80386SX - INPUT SETUP AND HOLD TIMING**

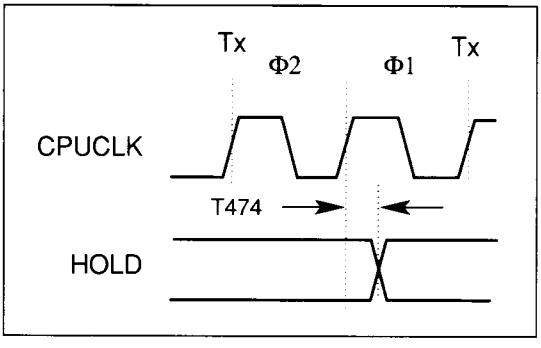


**FIGURE 13-48. 80386SX - OUTPUT DELAY TIMING**

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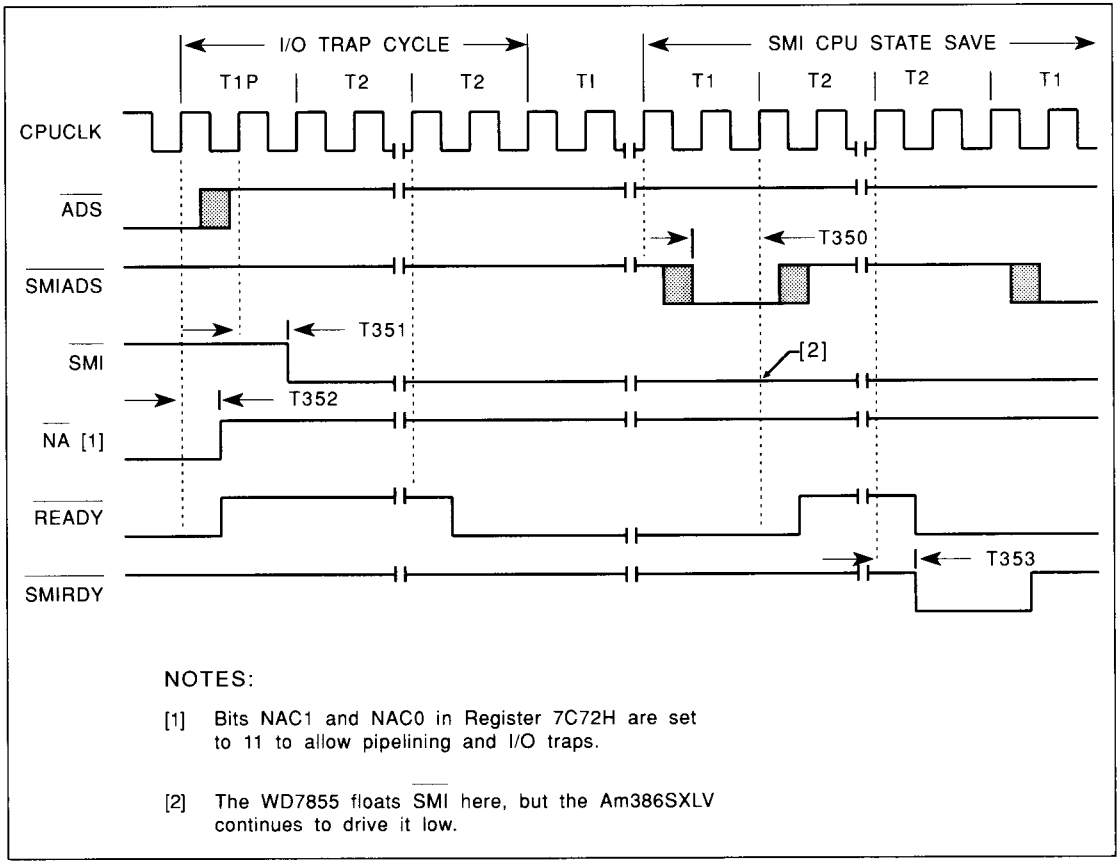
| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT |
|---|---|---|---|---|
| T350 | $\overline{SMIADS}$ setup time to CPUCLK rise | 10 | | ns |
| T351 | CPUCLK rise to $\overline{SMI}$ low output delay | | 25 | ns |
| T352 | CPUCLK rise to $\overline{NA}$ output delay | | 15 | ns |
| T353 | CPUCLK rise to $\overline{SMIRDY}$ output delay | | 18 | ns |

**TABLE 13-12. WD7855 SMI TIMING**




NOTES:

[1] Bits NAC1 and NAC0 in Register 7C72H are set to 11 to allow pipelining and I/O traps.

[2] The WD7855 floats $\overline{SMI}$ here, but the Am386SXLV continues to drive it low.

**FIGURE 13-49. I/O TRAP CYCLE WITH Am386SXLV**

# 14.0 PIN STATES DURING CHIP RESET, SUSPEND AND CPU POWER DOWN

| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN | | FULL POWER DOWN | |
|---|---|---|---|---|---|---|
| | | | Input | Output | Input | Output |
| | | ***AT BUS*** | | | | |
| 94 | $\overline{IOR}$ ③ | High ① | I | O | IH | Z |
| 93 | $\overline{IOW}$ ③ | High ① | I | O | IH | Z |
| 97 | $\overline{MEMR}$ ③ | High ① | I | O | IH | Z |
| 92 | $\overline{MEMW}$ ③ | High ① | I | O | IH | Z |
| 107 | $\overline{LOMEG}$ | High | | O | | Z |
| 88 | $\overline{MASTER}$ ③ | Input | I | | IH | |
| 84 | $\overline{IOCK}$ ③ | Input | I | | IH | |
| 101 | AEN | Low | | O | | Z |
| 100 | SYSCLK | Low | | O | | Z |
| 87 | $\overline{IOCS16}$ ③ | Input | I | | IH | |
| 89 | $\overline{MEMCS16}$ ③ | Input | I | | IH | |
| 86 | $\overline{ZEROWS}$ ③ | Input | I | | IH | |
| 85 | IOCHRDY ③ | Input | I | | IH | |
| 98 | $\overline{REFRESH}$ ③ | High | I | O | IH | O |
| 99 | BALE | Low | | O | | Z |
| 38 | MXCTL2 | High | | O | | O |
| 37 | MXCTL1 | Low | | O | | O |
| 35 | MXCTL0 | Low | | O | | O |
| 40 | DACKEN | High | | O | | O |
| 33 | IRQSET1 | Input | I | | IH | |
| 34 | IRQSET0 | Input | I | | IH | |
| 76 | DRQIN | Input | I | | IL | |
| 95 | LA20 | High ① ② | I | O | IH | Z |
| 96 | SA0 | Low ① ② | I | O | IH | Z |

①: This pin is tristated if master = 0. For test purposes, if MASTER is asserted, outputs are tristated and the pins become inputs.
②: Assumes processor address = FFFFF0 during reset.
③: Internal 50 kohm pullup, disabled in power-down mode.
IH: Input internally forced high in power-down mode.
IL: Input internally forced low in power-down mode.
Z: Output tristated in power-down mode.

**TABLE 14-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD.**

| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN | | FULL POWER DOWN | |
|---|---|---|---|---|---|---|
| | | | Input | Output | Input | Output |
| | | ***AT BUS (Continued)*** | | | | |
| 155 | SPKR | Low | | O | | O |
| 149 | DT/$\overline{R}$ | High | | O | | Z |
| 152 | $\overline{DEN0}$ | High | | O | | Z |
| 151 | $\overline{DEN1}$ | High | | O | | Z |
| 15 | ALE | High | | O | | Z |
| 55 | SDT/$\overline{R}$ ⑤ | Input ⑥ | I | O | IL | Z |
| 59 | $\overline{SDEN}$ | High | | O | | Z |
| 39 | $\overline{CSEN}$ | Low | | O | | O |
| | | ***VLBI CONTROL*** | | | | |
| 103 | $\overline{LB}$ ③ | Input | | Z | | Z |
| 45 | $\overline{LBRDY}$ ③ | Input | | Z | | Z |
| | | ***SMI CONTROL*** | | | | |
| 110 | $\overline{SMIRDY}$ | Output | | Z | | Z |
| 113 | $\overline{SMIADS}$ | Input | IH | Z | IH | Z |
| 5 | $\overline{ADS}$ | Input | IH | Z | IH | Z |
| 108 | $\overline{SMI}$ | Input | IH | Z | IH | Z |
| | | ***80386SX PROCESSOR*** | | | | |
| 122 | CPUCLK | Same as BCLK2 | IL | Z | IL | Z |
| 114 | $\overline{READY}$ ③ | Low | | Z | | Z |
| 154 | CPURES | High | | Z | | Z |
| 116 | HOLDR | Low | | Z | | Z |
| 126 | INTRQ | Low | | Z | | Z |
| 124 | NMI | Low | | Z | | Z |
| 109 | $\overline{BHE}$ ③ | Input | IH | Z | IH | Z |
| 112 | D/$\overline{C}$ | Input | IL | | IL | |
| 1 | M/$\overline{IO}$ ③ | Input | IL | Z | IL | Z |
| 115 | HOLDA ③ | Low | IL | | IL | |

③ Internal 50 kohm pullup, disabled in power-down mode.
⑤ Internal 80 kohm pullup, disabled in processor power-down mode and in full power-down mode.
⑥ Returns to output when $\overline{RSTIN}$ is de-asserted.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

**TABLE 14-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)**

| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN Input | PROCESSOR POWER DOWN Output | FULL POWER DOWN Input | FULL POWER DOWN Output |
|---|---|---|---|---|---|---|
| | | ***80386SX PROCESSOR Continued*** | | | | |
| 123 | $\overline{\text{BUSYCPU}}$ | High | | Z | | Z |
| 125 | $\overline{\text{NA}}$ | Output | | Z | | Z |
| 157 | A23 ⑦ | Input | IL | Z | IL | Z |
| 158 | A22 ⑦ | Input | IL | Z | IL | Z |
| 159 | A21 ⑦ | Input | IL | Z | IL | Z |
| 6 | A20 ⑦ | Input | IL | Z | IL | Z |
| 7 | A19 ⑦ | Input | IL | Z | IL | Z |
| 8 | A18 ⑦ | Input | IL | Z | IL | Z |
| 9 | A17 ⑦ | Input | IL | Z | IL | Z |
| 11 | A16 ⑦ | Input | IL | Z | IL | Z |
| 12 | A15 ⑦ | Input | IL | Z | IL | Z |
| 13 | A14 ⑦ | Input | IL | Z | IL | Z |
| 14 | A13 ⑦ | Input | IL | Z | IL | Z |
| 16 | A12 ⑦ | Input | IL | Z | IL | Z |
| 17 | A11 ⑦ | Input | IL | Z | IL | Z |
| 21 | A10 ⑦ | Input | IL | Z | IL | Z |
| 23 | A9 ⑦ | Input | IL | Z | IL | Z |
| 24 | A8 ⑦ | Input | IL | Z | IL | Z |
| 26 | A7 ⑦ | Input | IL | Z | IL | Z |
| 27 | A6 ⑦ | Input | IL | Z | IL | Z |
| 28 | A5 ⑦ | Input | IL | Z | IL | Z |
| 29 | A4 ⑦ | Input | IL | Z | IL | Z |
| 31 | A3 ⑦ | Input | IL | Z | IL | Z |
| 32 | A2 ⑦ | Input | IL | Z | IL | Z |
| 4 | A1 ⑦ | Input | IL | Z | IL | Z |
| 3 | $\overline{\text{BLE}}$ ⑦ | Input | IL | Z | IL | Z |
| 2 | W/$\overline{\text{R}}$ | Input | IL | Z | IL | Z |

⑦ 100 Kohm pulldown resistors are turned on when the processor is in power-down or suspend mode to prevent the data bus or address bus from floating. In normal operation these pull down resistors are turned off.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

**TABLE 14-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)**

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| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN Input | PROCESSOR POWER DOWN Output | FULL POWER DOWN Input | FULL POWER DOWN Output |
|---|---|---|---|---|---|---|
| | | ***DRAM CONTROL*** | | | | |
| 78 | DPH/CS4 ④ | Low | I | O | I | O |
| 79 | DPL/CS3 ④ | Low | I | O | I | O |
| 20 | RA11 | Output | | O | | O |
| 52 | RA10/CS2 | High ② | | O | | O |
| 53 | RA9/CS1 | High ② | | O | | O |
| 54 | RA8/CS0 | High ② | | O | | O |
| 57 | RA7/ED7 | High ② | I ⑨ | O | I | O |
| 58 | RA6/ED6 | High ② | I ⑨ | O | I | O |
| 61 | RA5/ED5 | High ② | I ⑨ | O | I | O |
| 63 | RA4/ED4 | High ② | I ⑨ | O | I | O |
| 64 | RA3/ED3 | High ② | I ⑨ | O | I | O |
| 67 | RA2/ED2 | High ② | I ⑨ | O | I | O |
| 68 | RA1/ED1 | High ② | I ⑨ | O | I | O |
| 69 | RA0/ED0 | High ② | I ⑨ | O | I | O |
| 75 | $\overline{RAS7}$ ④ | High | | O | | O |
| 74 | $\overline{RAS6}$ ④ | High | | O | | O |
| 72 | $\overline{RAS5}$ ④ | High | | O | | O |
| 71 | $\overline{RAS4}$ ④ | High | | O | | O |
| 49 | $\overline{RAS3}$ ④ | High | | O | | O |
| 48 | $\overline{RAS2}$ ④ | High | | O | | O |
| 46 | $\overline{RAS1}$ ④ | High | | O | | O |
| 44 | $\overline{RAS0}$ ④ | High | | O | | O |

② Assumes processor address = FFFFF0 during reset.
④ Internal 50 kohm pullup, disabled in processor power-down mode and in full power-down mode.
⑨ Bidirectional buffer.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

**TABLE 14-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)**

| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN Input | PROCESSOR POWER DOWN Output | FULL POWER DOWN Input | FULL POWER DOWN Output |
|---|---|---|---|---|---|---|
| | | ***DRAM CONTROL (Continued)*** | | | | |
| 77 | $\overline{CAS3}$ ⑤ | Input ⑧ | | O | IH | Z |
| 73 | $\overline{CAS2}$ ⑤ | Input ⑧ | | O | IH | Z |
| 51 | $\overline{CAS1}$ ④ | High | | O | | O |
| 47 | $\overline{CAS0}$ ④ | High | | O | | O |
| 43 | WNRDRAM | Output | | Z | | Z |
| | | ***CACHE CONTROL*** | | | | |
| 153 | A20GATE | Output | | Z | | Z |
| 25 | $\overline{NONCAC}$ | Input | IL | | IL | |
| 30 | $\overline{FLUSH}$ | Output | | Z | | Z |
| 160 | $\overline{KEN}$ | Output | | Z | | Z |
| | | ***INITIALIZATION AND CLOCKING*** | | | | |
| 90 | CLK14 | Input | I | | I | |
| 120 | BCLK2 | Input | I | | IL | |
| 80 | $\overline{RSTIN}$ | Input | I | | I | |
| | | ***POWER MANAGEMENT CONTROL*** | | | | |
| 42 | PMCIN ③ | Input | I | | I | |
| 41 | $\overline{PDREF}$ ③ | Input | I | | I | |

③ Internal 50 kohm pullup, disabled in power-down mode.
④ Internal 50 kohm pullup, disabled in processor power-down mode and in full power-down mode.
⑤ Internal 80 kohm pullup, disabled in processor power-down mode and in full power-down mode.
⑧ In 80486 mode ($\overline{CAS2}$ low at trailing edge of $\overline{RSTIN}$) this remains an input after $\overline{RSTIN}$ is de-asserted.
In 80386 mode ($\overline{CAS2}$ high at trailing edge of $\overline{RSTIN}$) it switches to output after $\overline{RSTIN}$ is de-asserted.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

**TABLE 14-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)**

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| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN | | FULL POWER DOWN | |
|---|---|---|---|---|---|---|
| | | | Input | Output | Input | Output |
| | ***DATA BUS*** | | | | | |
| 121 | CLKA/$\overline{\text{RDYIN}}$/PE | Input | | | | |
| 148 | D15 ⑦ | Input | IL | Z | IL | Z |
| 147 | D14 ⑦ | Input | IL | Z | IL | Z |
| 146 | D13 ⑦ | Input | IL | Z | IL | Z |
| 144 | D12 ⑦ | Input | IL | Z | IL | Z |
| 142 | D11 ⑦ | Input | IL | Z | IL | Z |
| 139 | D10 ⑦ | Input | IL | Z | IL | Z |
| 138 | D9 ⑦ | Input | IL | Z | IL | Z |
| 137 | D8 ⑦ | Input | IL | Z | IL | Z |
| 136 | D7 ⑦ | Input | IL | Z | IL | Z |
| 134 | D6 ⑦ | Input | IL | Z | IL | Z |
| 133 | D5 ⑦ | Input | IL | Z | IL | Z |
| 127 | D0 ⑦ | Input | IL | Z | IL | Z |
| 132 | D4 ⑦ | Input | IL | Z | IL | Z |
| 131 | D3 ⑦ | Input | IL | Z | IL | Z |
| 129 | D2 ⑦ | Input | IL | Z | IL | Z |
| 128 | D1 ⑦ | Input | IL | Z | IL | Z |
| | ***NUMERIC PROCESSOR CONTROL*** | | | | | |
| 105 | EPEREQ | Low | | Z | | Z |
| 106 | NPRST | High | | Z | | Z |
| 111 | $\overline{\text{NPERR}}$ ③ | Input | IH | | IH | |
| 140 | $\overline{\text{NPBUSY}}$ ③ | Input | IH | | IH | |

③ Internal 50 kohm pullup, disabled in power-down mode.
⑦ 100 Kohm pulldown resistors are turned on when the processor is in power-down or suspend mode to prevent the data bus or address bus from floating. In normal operation these pull down resistors are turned off.
IH Input internally forced high in power-down mode.
IL Input internally forced low in power-down mode.
Z Output tristated in power-down mode.

**TABLE 14-1. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD. (Continued)**

| Pin Number | Signal Name |
|---|---|
| 10 | VSS |
| 18 | VSS |
| 19 | VSS |
| 50 | VSS |
| 56 | VSS |
| 70 | VSS |
| 104 | VSS |
| 130 | VSS |
| 141 | VSS |
| 150 | VSS |
| 156 | VSS |
| 22 | VDD |
| 36 | VDD |
| 62 | VDD |
| 66 | VDD |
| 102 | VDD |
| 135 | VDD |
| 143 | VDD |
| 91 | VDDAT |

**TABLE 14-2. POWER AND GROUND**

## 15.0 PACKAGE DIMENSIONS

Figure 15-1 Illustrates the 160-Pin MQFP package showing the dimensions in inches.

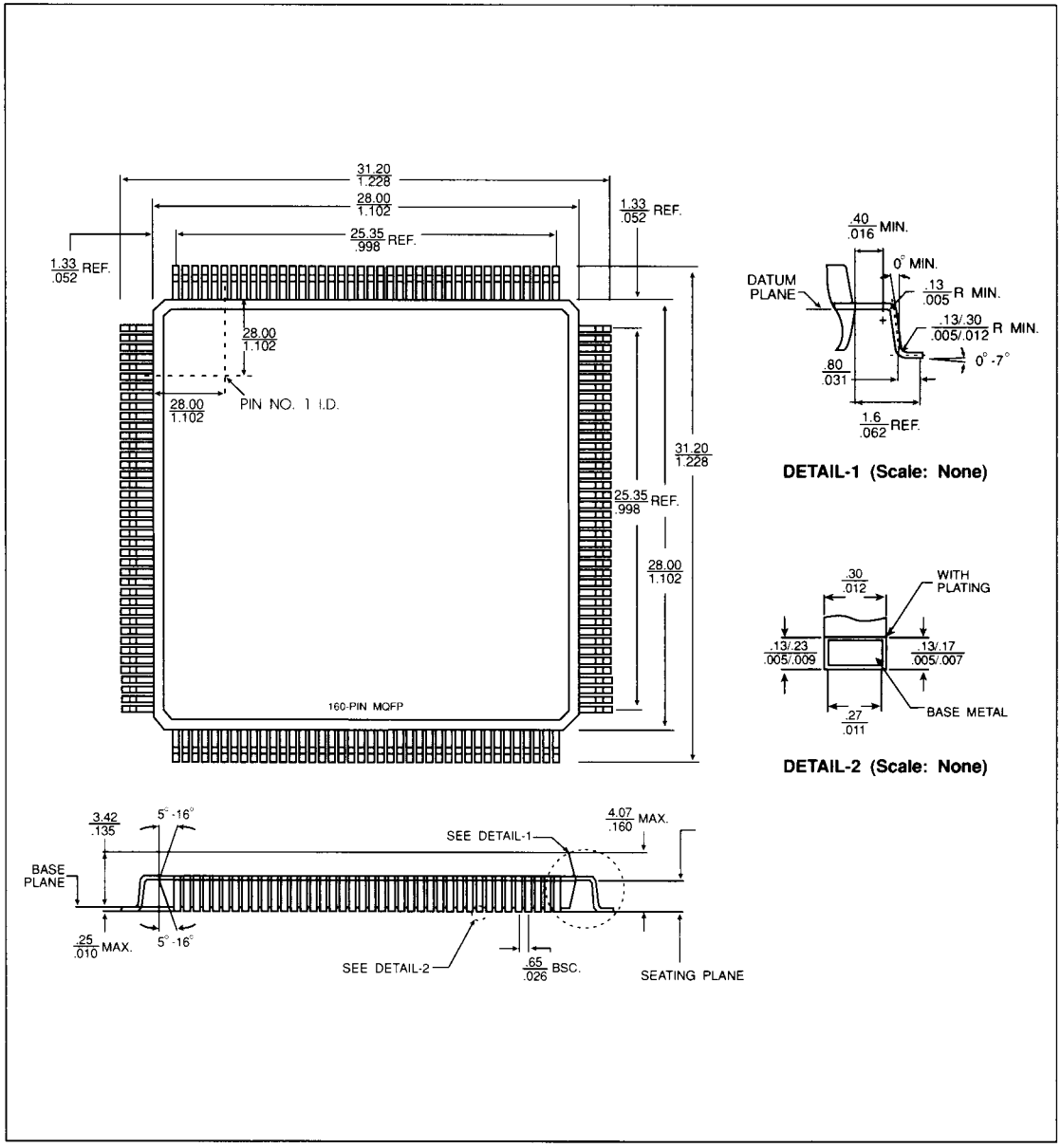


**FIGURE 15-1. 160-PIN MQFP PACKAGE DIMENSIONS**

# APPENDIX

## A.0 ELECTRICAL SPECIFICATIONS FOR WD7855LV

This section provides the Operating Characteristics for the WD7855LV. The parameters that differ from the WD7855 are marked with an * .

### A.1 MAXIMUM RATINGS

Supply Voltage ($V_{DD}$) with respect to Vss (ground) . . . . . $V_{DD}$ - Vss ≤ 7.0 Volts
Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to $V_{DD}$ +0.3 Volts
Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)
Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)
Power Dissipation . . . . . 400 mW *

**NOTE**

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

### A.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
$V_{DD}$AT = +3.3V ±.0.3V for WD7855LV *
$V_{DD}$ = +3.3V ±.0.3V for WD7855LV *

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Leakage | | ± 10 | µA | Vin = .4 to $V_{DD}$ |
| IOZ | Tristate And Open Drain Output Leakage | | ± 10 | µA | Vout = .4 to $V_{DD}$ |
| VIH | Input High Voltage | 2.0 | | V | |
| VIL | Input Low Voltage | | .8 | V | |
| VIHC | CPUCLK Input High * | $V_{DD}$ -0.8 | | V | |
| VIL | CPUCLK Input Low | | .6 | V | |
| VIH | $\overline{\text{RSTIN}}$ Input High Voltage | $V_{DD}$ -0.5 | | V | |
| VIL | $\overline{\text{RSTIN}}$ Input Low Voltage | | 0.5 | V | |
| ICC | Supply Current * | | 150<br>100 | mA<br>mA | Inputs at 2.0V<br>Inputs at 3.3V<br>Outputs Open,<br>CPUCLK = 50 MHz |
| ICCAT | Supply Current | | 15<br>7 | mA<br>mA | Input at 2.0 V<br>Input at 3.3V |
| ICCSB | Typical Supply Current, Power Down Mode for WD7855/LV | | .5 | mA | Typical,<br>CPUCLK Off,<br>CLK14 = 32 KHz |

**TABLE A-1. DC OPERATING CHARACTERISTICS**

10

**FOR PINS WITH INTERNAL PULLUPS:**

$\overline{\text{MASTER}}$, $\overline{\text{IOCK}}$, $\overline{\text{IOCS16}}$, $\overline{\text{MEMCS16}}$, $\overline{\text{ZEROWS}}$, IOCHRDY, $\overline{\text{RDYIN}}$, $\overline{\text{PDREF}}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -27 | -90 | µA | Not suspend and resume mode |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

M/$\overline{\text{IO}}$, $\overline{\text{NPERR}}$, $\overline{\text{NPBUSY}}$, $\overline{\text{NPRST}}$, CPURES, DPH, DPL, $\overline{\text{NONCAC}}$, $\overline{\text{ADS}}$, D/$\overline{\text{C}}$, W/$\overline{\text{R}}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -27 | -90 | µA | Not processor power-down or suspend mode |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

PMCIN, IOCHRDY, $\overline{\text{ZEROWS}}$, $\overline{\text{IOCS16}}$, $\overline{\text{MEMCS16}}$, $\overline{\text{MASTER}}$, $\overline{\text{PDREF}}$, $\overline{\text{REFRESH}}$, $\overline{\text{BHE}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -27 | -90 | µA | Not suspend mode |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

SDT/$\overline{\text{R}}$, CAS3, CAS2

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pullup Current * | -27 | -90 | µA | $\overline{\text{RESET}}$ IN = 0 |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR PINS WITH INTERNAL PULLDOWNS:**

A(23:00), D(15:00), $\overline{\text{BLE}}$

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| IIL | Input Pulldown Current * | -27 | -90 | µA | Processor power-down or suspend mode |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

DACKEN, D(15:00), READY, CPURES, HOLDR, INTRQ, A(23:00), NMI, DPH, DPL, RA(11:08), RA7/ED7:RA0/ED0, BHE, RAS(7:0), CAS(3:0), W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG, A20GATE, KEN, FLUSH, SMI

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage * | $V_{DD}$ -0.2 | | V | IOUT = -100 µA |
| VOH | Output High Voltage * | 2.4 | | V | IOUT = -1 mA |
| VOL | Output Low Voltage * | | .4 | V | IOUT = 1.5 mA |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

MXCTL2:0

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage | $V_{DD}$ - .8 | | V | IOUT = -200 µA |
| VOH | Output High Voltage * | 2.4 | | V | IOUT = -3 mA |
| VOL | Output Low Voltage * | | .4 | V | IOUT = 3 mA |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUTS:**

IOR, IOW, MEMR, MEMW, AEN, SYSCLK, BALE, LA20, SA0

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage | 2.4 | | V | IOUT = -3 mA |
| VOL | Output Low Voltage * | | .5 | V | IOUT = 12 mA |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

**FOR OUTPUT:**

REFRESH, IOCHRDY

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOL | Output Low Voltage * | | .4 | V | IOUT = 12 mA |

**TABLE A-1. DC OPERATING CHARACTERISTICS (Continued)**

## A.3 AC OPERATING CHARACTERISTICS

This section provides the WD7855LV AC Operating Characteristics for the 80386SX Page Mode and 80386SX CPU Mode. The parameters that differ from the WD7855 are marked with an * .

| SIGNAL | LOAD | SIGNAL | LOAD | SIGNAL | LOAD |
|---|---|---|---|---|---|
| $\overline{SMI}$ | 50 pF | $\overline{NA}$ | 50 pF | $\overline{SMIRDY}$ | 50 pF |
| $\overline{KEN}$ | 50 pF | A20GATE | 50 pF | $\overline{FLUSH}$ | 50 pF |
| CPURES | 50 pF | NPRST | 50 pF | $\overline{BHE}$ | 50 pF |
| W/$\overline{R}$ | 50 pF | ALE | 50 pF | $\overline{DEN1}$, $\overline{DEN0}$ | 50 pF |
| $\overline{SDEN}$ | 50 pF | DT/$\overline{R}$ | 50 pF | SDT/$\overline{R}$ | 50 pF |
| MXCTL(2:0) | 50 pF | DACKEN | 50 pF | $\overline{CSEN}$ | 50 pF |
| $\overline{LOMEG}$ | 50 pF | SPKR | 50 pF | $\overline{READY}$ | 50 pF |
| $\overline{HOLDR}$ | 50 pF | INTRQ | 50 pF | NMI | 50 pF |
| $\overline{BUSYCPU}$ | 50 pF | EPEREQ | 50 pF | A(23:00) | 60 pF |
| CPUCLK | 70 pF | SYSCLK | 75 pF | $\overline{DPH}$ | 100 pF |
| $\overline{CAS}$(3:0) | 100 pF | D(15:00) | 100 pF | $\overline{IOW}$ | 200 pF |
| $\overline{DPL}$ | 100 pF | $\overline{RAS}$(7:0) | 100 pF | $\overline{MEMR}$ | 200 pF |
| $\overline{IOR}$ | 200 pF | $\overline{MEMW}$ | 200 pF | AEN | 200 pF |
| LA20 | 200 pF | $\overline{SA0}$ | 200 pF | RA(11:00) * | 220 pF |
| BALE | 200 pF | $\overline{REFRESH}$ | 200 pF | | |

**TABLE A-2. SIGNAL LOADING**

## A.4 80386SX PAGE MODE TIMING

| SYMBOL | CHARACTERISTIC | MAX 20 MHz | MAX 25 MHz |
|---|---|---|---|
| T200 | Processor ADDRESS to RAM address valid, Page Hit | 34 | 27 |
| T201 | CPUCLK rise to $\overline{CAS}$ fall, 2.5 CLK $\overline{CAS}$ | 31 | 25 |
| T202 | CPUCLK fall to $\overline{CAS}$ rise | 24 | 21 |
| T203 | CPUCLK fall to $\overline{CAS}$ fall, 2.0 CLK $\overline{CAS}$ | 27 | 22 |
| T204 | Processor data to parity valid | 25 | 20 |
| T205 | CPUCLK rise to RAM address valid, Page Miss | 48 | 43 |
| T206 | CPUCLK rise to WNRDRAM rise | 31 | 28 |
| T207 | CPUCLK fall to $\overline{RAS}$ fall, first access | 27 | 21 |
| T208 | CPUCLK rise to COLUMN address valid | 49 | 33 |
| T209 | CPUCLK rise to WNRDRAM fall | 31 | 28 |
| T212 | CPUCLK rise to $\overline{RAS}$ rise, Page Miss | 27 | 24 |
| T213 | CPUCLK fall to $\overline{RAS}$ fall, Page Miss | 27 | 24 |
| T214 | CPUCLK rise to $\overline{READY}$ fall * | 25 | 25 |
| T215 | CPUCLK rise to $\overline{READY}$ rise * | 25 | 25 |

**TABLE A-3. 80386SX - PAGE MODE MEMORY TIMING**

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This table covers the 80386SX CPU timing. The WD7855LV parameters that differ from the WD7855 are marked with an * .

| SYMBOL | CHARACTERISTIC | 20 MHz | | 25 MHz | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| T140 | See Table 13-6 | | | | | |
| T141 | See Table 13-6 | | | | | |
| T204 | See Table 13-3 | | | | | |
| T214 | See Table 13-3 | | | | | |
| T215 | See Table 13-3 | | | | | |
| T451 | CPUCLK rise to CPURES rise delay | | 14 | | 12 | ns |
| T452 | CPUCLK rise to CPURES fall delay | | 13 | | 12 | ns |
| T453 | CPUCLK rise to NPRST rise delay | | 14 | | 10 | ns |
| T454 | CPUCLK rise to NPRST fall delay | | 13 | | 10 | ns |
| T455 | CPUCLK rise to $\overline{\text{BUSYCPU}}$ fall delay | | 35 | | 35 | ns |
| T456 | CPUCLK rise to $\overline{\text{BUSYCPU}}$ rise delay | | 35 | | 30 | ns |
| T457 | $\overline{\text{NPBUSY}}$ fall to $\overline{\text{BUSYCPU}}$ fall delay | | 30 | | 30 | ns |
| T458 | $\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay | | 35 | | 35 | ns |
| T460 | $\overline{\text{NPERR}}$ fall to EPEREQ rise delay | | 30 | | 30 | ns |
| T462 | $\overline{\text{ADS}}$ setup time to CPUCLK rise * | 14 | | 14 | | ns |
| T463 | $\overline{\text{ADS}}$ hold time from CPUCLK rise | 5 | | 4 | | ns |
| T464 | W/$\overline{\text{R}}$ setup time to CPUCLK rise * | 14 | | 12 | | ns |
| T465 | W/$\overline{\text{R}}$ hold time from CPUCLK rise | 5 | | 4 | | ns |
| T466 | D/$\overline{\text{C}}$ setup time to CPUCLK rise * | 14 | | 10 | | ns |
| T467 | D/$\overline{\text{C}}$ hold time from CPUCLK rise | 5 | | 4 | | ns |
| T468 | M/$\overline{\text{IO}}$ setup time to CPUCLK rise * | 17 | | 19 | | ns |
| T469 | M/$\overline{\text{IO}}$ hold time from CPUCLK rise | 5 | | 4 | | ns |
| T470 | $\overline{\text{BHE}}$ setup time to CPUCLK rise | 17 | | 15 | | ns |
| T471 | $\overline{\text{BHE}}$ hold time from CPUCLK rise | 3 | | 4 | | ns |
| T472 | HOLDA setup time to CPUCLK rise * | 10 | | 10 | | ns |
| T473 | HOLDA hold time from CPUCLK rise | 3 | | 4 | | ns |
| T474 | HOLDR valid delay from CPUCLK rise * | | 26 | | 26 | ns |
| T475 | DPH setup time to CPUCLK rise | 5 | | 5 | | ns |
| T476 | DPH hold time from CPUCLK rise | 19 | | 19 | | ns |
| T477 | D(15:00) setup time to CPUCLK rise | 5 | | 5 | | ns |
| T478 | D(15:00) hold time from CPUCLK rise | 19 | | 19 | | ns |
| T479 | A(23:01), $\overline{\text{BLE}}$ setup time to CPUCLK rise * | 42 | | 42 | | ns |
| T480 | A(23:01), $\overline{\text{BLE}}$ hold time from CPUCLK rise | 3 | | 4 | | ns |

**TABLE A-4. 80386SX CPU TIMING**

# B.0 SPECIAL FEATURE REGISTERS

This section describes the registers peculiar to the special features. Except for Port Addresses F073H and FC72H all Port Addresses described in this section are peculiar to these special features.

## B.1 ENABLING THE SPECIAL FEATURES

To enable the special features, the WD7855/LV must first be unlocked by writing DAH to the Lock/Unlock Register at Port Address F073H and then writing DA00H to the Lock Status Register at Port Address FC72H. As stated in Section 2.8.1, Port Address FC72H is normally a read only register, but will respond to a write value of DA00H.

These registers are described in detail in Sections 2.8, 2.8.1 and 2.8.2.

## B.2 ENABLE PRIVY REGISTER

Port Address 0FBH - Write only

The special features must first be enabled, as described in Section B.1, and then writing any data to this register enables PRIVY. When PRIVY is enabled, 4 KB of RAM, starting at 0F0000H to 0F0FFFH, is enabled for both read and write access.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PRIVY ENABLED | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

## B.3 DISABLE PRIVY REGISTER

Port Address 0F9H - Write only

Writing any data to this register disables PRIVY. When PRIVY is disabled, the 4 KB RAM is treated as the rest of memory in the F000H segment.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PRIVY DISABLE | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

## B.4 BUSY BYPASS CONTROL REGISTER

Port Address 0ECH - Read and Write

Before the Bypass Mode can be enabled or disabled, PRIVY must first be set by writing any data to Port Address 0FBH.

Bypass Mode is enabled by writing any data to Port Address 0ECH.

When the Bypass Mode is enabled, ERROR from the Numeric Processing Unit (NPU) does not cause an IRQ13 and the BUSY signal is not sent to the CPUBUSY output without modification.

Bypass Mode is disabled by reading Port Address 0ECH.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BUSY BYPASS | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

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## B.5 FAST A20 GATE CONTROL REGISTER

Port Address 0EEH - Read and Write

Before the special feature FAST A20 GATE can be enabled or disabled, PRIVY must first be set by writing any data to Port Address 0FBH.

FAST A20 GATE is enabled by writing any data to Port Address 0EEH.

The special feature FAST A20 GATE is ORed with the A20GT signal from the Keyboard Controller and with Port 92 A20 gate signal.

FAST A20 GATE is disabled by reading Port Address 0EEH.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Special Feature FAST A20 GATE | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

## B.6 FAST CPU RESET CONTROL REGISTER

Port Address 0EFH - Read only

Before the FAST CPU RESET can be initiated, PRIVY must be set by writing any data to Port Address 0FBH.

A processor reset is initiated by reading Port Address 0EFH. The processor reset pulse is 16 CPUCLKs. This processor reset signal is ORed with the Hot Reset at Port 092H and with the Keyboard Controller processor reset.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FAST CPU RESET CONTROL | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

## B.7 PARITY CONTROL REGISTER

Port Address 0F2H - Write only

Before normal/inverted parity can be changed, PRIVY must be set by writing any data to Port Address 0FBH.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | PAR I/N | CHIP SELECT 1FH | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| All signals | None |

Writing to any bit with PRIVY set also initiates a Chip Select 1FH on the encoded chip select pins CS(4:0). Section 8.4 describes the encoded chip selects.

**Bit 6 - PAR I/N**, Parity Inversion

PAR I/N = 0 -
Parity is inverted at the next write of on-board memory.

PAR I/N = 1 -
Normal parity is generated.

# C.0 IBM FEATURES

This section describes the pin signals and register bits peculiar to IBM 386SLC and 486SLC2 applications.

## C.1 PIN SIGNAL DESCRIPTION

| PIN NUMBER | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| 108 | PWI | O | **System Management Interrupt** Translate +3<br>PWI request to the processor. This mode of operation is selected by bit 13 of Port Address C472H. |
| 145 | $\overline{\text{DFSREQ}}$ | O | **Dynamic Frequency Shift Request** Translate +3<br>$\overline{\text{DFSREQ}}$ is asserted by the System Controller to request a change in the CPUCLK frequency or duty cycle. |
| 156 | $\overline{\text{DFSRDY}}$ | I | **Dynamic Frequency Shift Ready** Translate +3<br>$\overline{\text{DFSRDY}}$ is the response to the $\overline{\text{DFSREQ}}$ by the processor, indicating permision to change the CPUCLK frequency. When the WD7855/LV samples $\overline{\text{DFSRDY}}$ it will change the CPUCLK frequncy. |

**TABLE C-1. SIGNAL DESCRIPTION**

## C.2 CACHE CONTROL REGISTER

Port Address C472H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| DFS | 0 | PWI | 0 | C_BSC | | HI_MEM9:8 | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| High Memory Location HI_MEM7:0 | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| DFS | 0 |
| PWI | 0 |

**Bit 15 - DFS,** Dynamic Frequency Shift

When DFS is enabled, any request to change the CPUCLK speed or duty cycle from AUTOFAST or writing to Port 1072H causes the WD7855/LV to generate a $\overline{\text{DFSREQ}}$ to the processor. Upon receiving a $\overline{\text{DFSRDY}}$ from the processor, the CPUCLK will be changed.

DFS = 0 -
DFS disabled.

DFS = 1 -
DFS enabled.

**Bit 13 - PWI**, Not SMI protocol.

For IBM applications this bit must be set to 1.

PWI = 0 -
AMD/Cyrix SMI mode enabled.

PWI = 1 -
PWI mode enabled.

**For bits 14, 12:00** refer to Section 7.3

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## C.3 NONCACHEABLE REGION 2 LOWER BOUNDARY

Port Address CC72H - Read and Write

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---|---|---|---|---|---|---|---|
| A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 |
| Lower Address Boundary | | | | | | | |

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | CS | BS | E_ PWI | NR2C |
| Lower Address Boundary | | | | | | | |

| Signal Name | Default At RSTIN |
|---|---|
| A25:12 | 0 |
| CS, BS | None |
| E_PWI | 0 |
| NR2C | 0 |

**Bit 01 - E_PWI**

E_PWI controls how the System Controller is to determine the end of an SMI/PWI interrupt. In AMD and Cyrix implementation pin 108 ($\overline{SMI}$) is bidirectional and can be used to make this determination. In IBM implementation this pin is an output only (PWI) and the end of an SMI is determined internally.

E_PWI = 0 -
Standard setting for AMD and Cyrix CPUs.

E_PWI = 1 -
Required for IBM CPUs.

**For bits 15:02 and 00** refer to Section 7.6

## C.4 PIN STATES DURING CHIP RESET, SUSPEND AND CPU POWER DOWN

Table C-2 presents the status of pins 108, 145 and 156 during chip reset, suspend and CPU power down. This is a continuation of Table 14-1.

| PIN NUMBER | SIGNAL NAME | RESET STATE | PROCESSOR POWER DOWN | | FULL POWER DOWN | |
|---|---|---|---|---|---|---|
| | | | Input | Output | Input | Output |
| | | ***PROCESSOR*** | | | | |
| 108 | PWI | Input | IH | Z | IH | Z |
| 145 | $\overline{DFSREQ}$ | High | | Z | | Z |
| 156 | $\overline{DFSRDY}$ | Input | IL | | IL | |

IH Input internaly forced high in power-down mode.
IL Input internaly forced low in power-down mode.
Z Output tristated in power-down mode.

**TABLE C-2. PIN STATES DURING CHIP RESET, SUSPEND, CPU PWD.**

**NOTE**

For IBM applications Table 13-2 Signal Loading would include $\overline{DFSREQ}$ as 50 pF.

Table 14-2 Power and Ground would not include pin 156 as VSS. This pin is $\overline{DFSRDY}$.