T-52.09

WD7615

Desktop Buffer

Manager Device

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WESTERN DIGITAL

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1.0 INTRODUCTION

The WD7615 is a buffer management chip for WD7600 16-bit chip sets. The WD7615 is a 136-pin MQFP device.

1.1 FEATURES

- Allows the WD7XC10 based designs to work with a generic "Super I/O" device or with the WD76C20 and WD76C30

- Replaces majority of external "glue" logic, up to 13 devices:

   - AT bus address buffers with 24 mA drive

   - AT bus interrupt multiplexing, and interrupt pull ups.

   - AT bus DRQ multiplexing and internal pull downs.

   - Keyboard/mouse interrupt latching and clearing functions

   - A20 Gate logic

   - Controlling the IDE data bit 7 at address 3F7H.

- Allows implementation of a desktop system with only three external devices

- Direct connect to AT address bus SA1 through SA19 and LA17 through LA23 with 24 mA drive

- DAC multiplexing and RESET generation

- DRAM WE signal from WD76C10 inversion and buffering

- $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ generation with 24mA direct drive

- Divide by 2 or divide by 4 clock output

- 136-pin MQFP package

1.2 GENERAL DESCRIPTION

The WD7615 desktop buffer manager is designed to work with the WD7XC10 family of desktop system controllers including:

   - WD76C10LR
   - WD76C10LR-25
   - WD76C10ALR
   - WD76C10ALR-33

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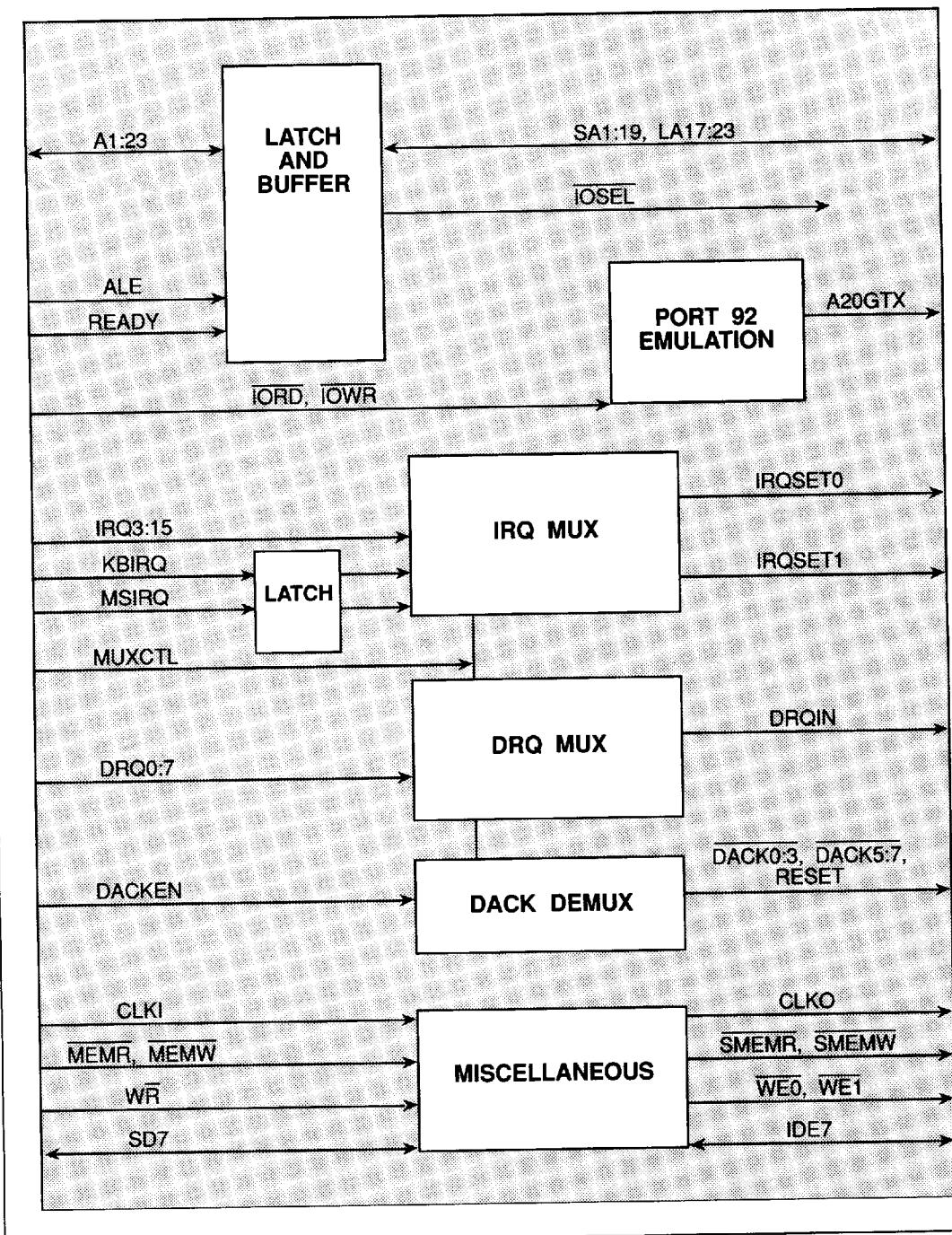
FIGURE 1-1. WD7615 INTERNAL BLOCK DIAGRAM

WESTERN DIGITAL CORP   54E D   ■■■ 9718228 0013040 TT4 ■■WDC
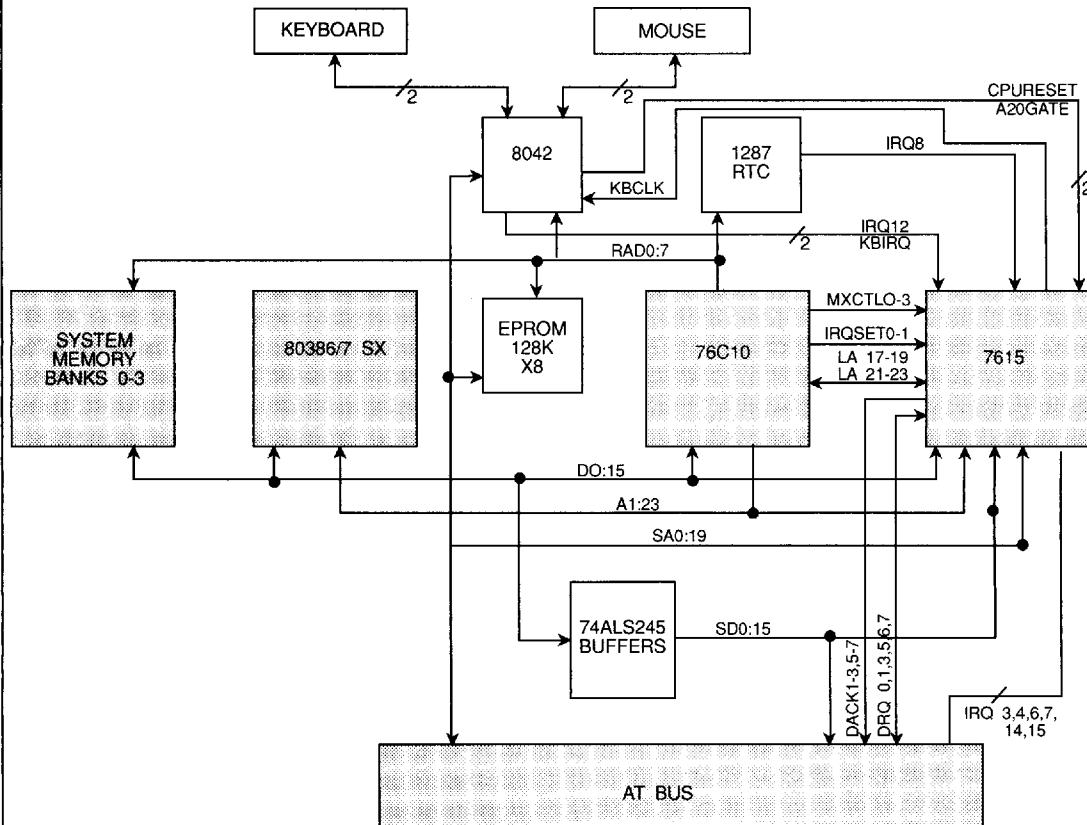
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FIGURE 1-2. WD7615 SYSTEM CONFIGURATION

WESTERN DIGITAL CORP   54E D ■ 9718228 0013041 930 ■ WDC
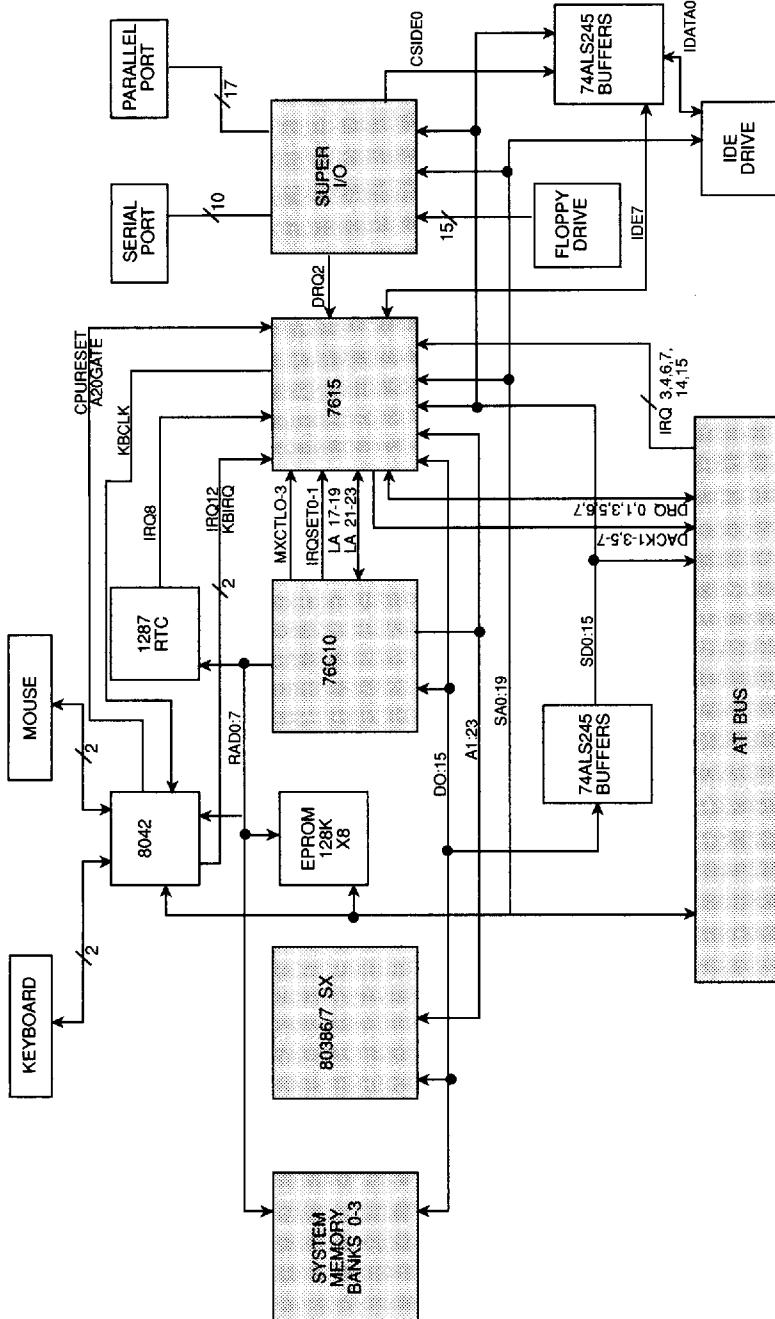
FIGURE 1-3. WD7615 SUPER I/O CONFIGURATION

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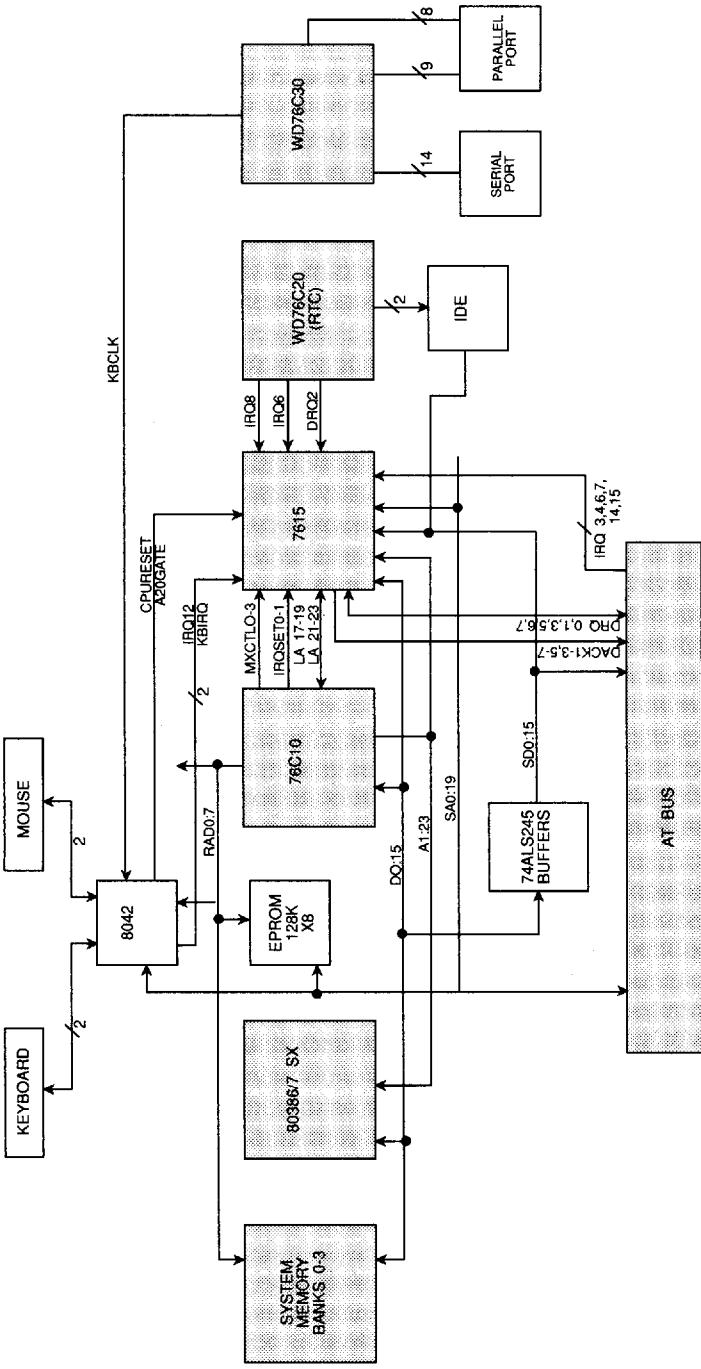
FIGURE 1-3. WD7615 WITH WD76C20/WD76C30 CONFIGURATION

WESTERN DIGITAL CORP   54E D ■ 9718228 0013043 703 ■ WDC

2.0 ARCHITECTURE

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The WD7615 is a 136-pin device supporting 16-bit processors. The functions of various internal blocks are described herein.

2.1 AT ADDRESS BUS

This block takes in A1 through A23 from the processor and latches it internally with ALE and READY signals. When MASTER is high, the address is driven to SA1 through SA19 and LA17 through LA23. The buffers on the lines can drive 24 mA for compatibility with the AT address bus. When MASTER is low, the address from the AT bus is driven to A1 through A23.

2.2 DRQ, IRQ MUTLIPLEXING AND DACK DEMULTIPLEXING

The WD7615 multiplexes the DRQ signals on to DRQIN with MUXCTL0:2 signals. Similarly, all the IRQs are pulse stretched and multiplexed onto IRQSET0 and IRQSET1 lines. The IRQ signals are passed through SCHMITT trigger inputs for better noise immunity. Together with the DACKEN signal the MUXCTL0:2 are demultiplexed onto DACK0:3 DACK5:7 signals. See Table 2-1, Multiplexer Assignments.

2.3 A20GATE LOGIC

This logic generates final A20GTX0 signals to be used for external cache designs in WD76C10A based systems. The KBA20GT signal is ORed with port 92 bit 1 (ALT_A20_GATE) bit. The WD7615 captures IO writes to port 92 bit 1. The latched bit 1 is ORed with KBA20GT from the keyboard controller and driven onto A20GTX0.

2.4 KEYBOARD CONTROLLER AND MOUSE INTERRUPT LATCHING

A latch is set by the logic in WD7615 when KBIRQ or MSIRQ from the keyboard controller is active. IORD at the keyboard controller chip select clears both latches.

This function allows MOUSE Interrupt to be cleared automatically by reading the 8042 data port. MSIRQ is dedicated to IRQ12 for onboard PS/2 mouse and this line should not be connected to the AT bus.

2.5 WE SIGNAL BUFFERING

The WD7615 takes in active high WE (Write Enable) from the WD7610A and drives two active low write enable signals for DRAM banks. WE0 and WE1 can each drive a high capacitance load of 300 pf and can each handle two banks of DRAMs.

MUXCTL	IRQSET0 SIGNAL	IRQSET1 SIGNAL	DRQIN SIGNAL	DACK SIGNAL
0 0 0	IRQ8	MSIRQ	DRQ0	DACK0
0 0 1	IRQ9	KBIRQ	DRQ1	DACK1
0 1 0	IRQ10	A20GT	DRQ2	DACK2
0 1 1	IRQ11	IRQ3	DRQ3	DACK3
1 0 0	ROM8	IRQ4	CLK_DIR_IN	RESET
1 0 1	RESCPU	IRQ5	DRQ5	DACK5
1 1 0	IRQ14	IRQ6	DRQ6	DACK6
1 1 1	IRQ15	IRQ7	DRQ7	DACK7

TABLE 2-1. MULTIPLEXER ASSIGNMENTS

2.6   SMEMR and SMEMW SIGNAL GENERATION

This logic takes in LOMEG, MEMR, and MEMW signals. When LOMEG is low, SMEMR or SMEMW will be driven low depending on the MEMR or MEMW signals. The SMEMR and SMEMW signals support 24 mA drives and can be directly connected to an AT bus.

2.7   POWER-ON-RESET SIGNAL GENERATION

The RESET active signal is generated from MUXCTL0:2 and DACKEN from WD76C10A. The RESET signal drives 24 mA and can be inverted externally for active low reset generation.

2.8   SD7, IDE7

This logic controls the data bit 7 for IDE Read/Write. At address 3F7H Read, SD7 will be turned off to avoid contention with the disk change signal of the floppy drive. If on board IDE interface is not designed in. SD7 and IDE7 should be left unconnected.

2.9   IOSEL SIGNAL

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For interfacing with super I/O chips, this signal is active whenever SA15 through SA10 are all low. This signal enables super I/O to decode all 16-bit for I/O addresses. It is also used to select the internal divider to generate the desired clock frequency for the keyboard controller.

2.10   TRISTATING THE OUTPUTS

If MEMR, MEMW, IOR and IOW are all low, the chip is put in tristate mode where all outputs are tristated for board testing except for the following three signals: DRQIN, WE0, WE1

2.11   IO MAPPING

The WD7615 is put in I/O mapping mode when IOR, IOW, and MEMR are all low, MEMW is high, and there is a low-to-high transition on the INT15 line. A group of inputs is multiplexed onto output pins in I/O mapping mode to ensure that the chip is properly soldered onto the PCB. See Appendix B for I/O Mapping details.

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3.0 SIGNAL DESCRIPTIONS

Figure 3-1 illustrates the pin locations on the WD7615 136-pin MQFP package. Table 3-1 lists all the signal names by pin number. Table 3-2 provides a description of each signal name grouped by function.
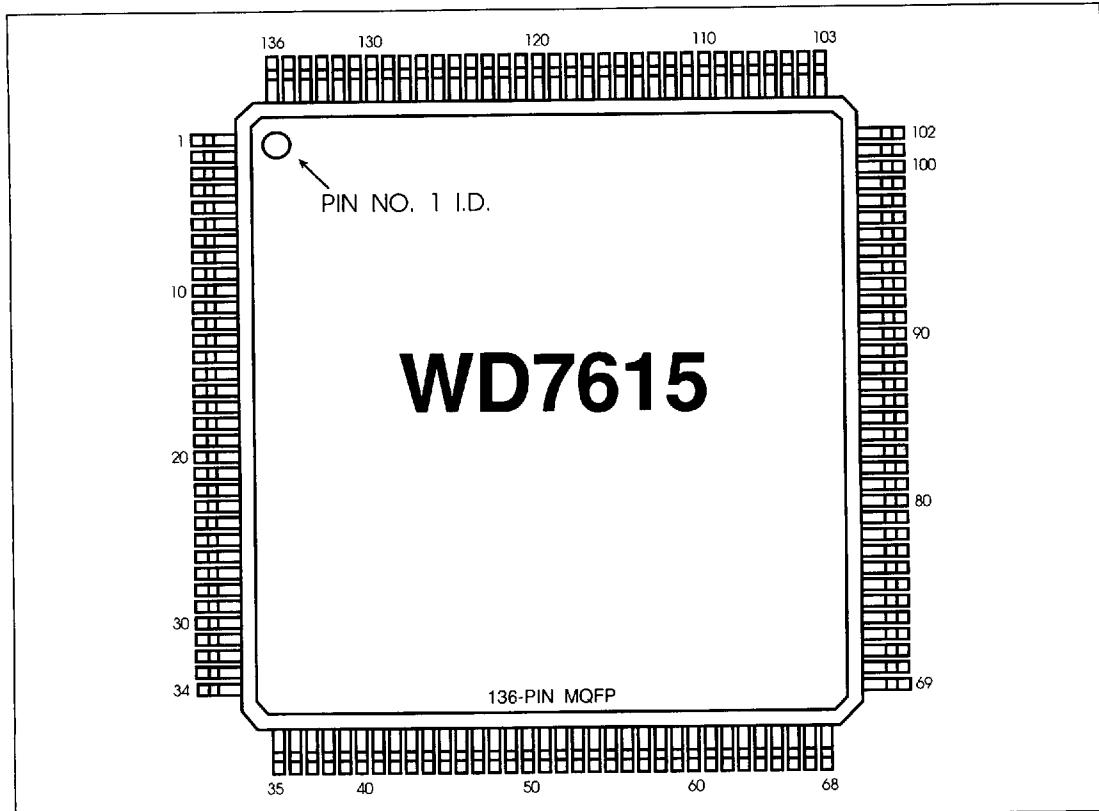

FIGURE 3-1. 136-PIN MQFP PIN ASSIGNMENTS

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PIN	-	NAME	PIN	-	NAME	PIN	-	NAME	PIN	-	NAME
1	-	SA0	35	-	KBIRQ	69	-	MEMW	103	-	DRQ0
2	-	CLKO	36	-	DRQ5	70	-	IDE7	104	-	DRQ1
3	-	D1	37	-	$\overline{BHE}$	71	-	$\overline{MEMR}$	105	-	DRQ2
4	-	KBA20GT	38	-	A20GTX0	72	-	DRQ6	106	-	DRQ3
5	-	RESCPUKB	39	-	$\overline{WE0}$	73	-	TEST1	107	-	GND
6	-	VCC	40	-	GND	74	-	TEST2	108	-	A1
7	-	SD7	41	-	VCC	75	-	GND	109	-	A2
8	-	GND	42	-	LA17	76	-	VCC	110	-	A3
9	-	A17	43	-	LA18	77	-	SA9	111	-	A4
10	-	A18	44	-	LA19	78	-	SA10	112	-	A5
11	-	A19	45	-	GND	79	-	SA11	113	-	A6
12	-	A21	46	-	LA21	80	-	GND	114	-	A7
13	-	A22	47	-	LA22	81	-	SA12	115	-	A8
14	-	A23	48	-	LA23	82	-	SA13	116	-	$\overline{GIOW}$
15	-	DRQ7	49	-	GND	83	-	SA14	117	-	$\overline{GIOR}$
16	-	VCC	50	-	VCC	84	-	VCC	118	-	VCC
17	-	GND	51	-	GND	85	-	GND	119	-	GND
18	-	DRQIN	52	-	VCC	86	-	SA15	120	-	A9
19	-	IRQSET0	53	-	$\overline{SBHE}$	87	-	SA16	121	-	A10
20	-	IRQSET1	54	-	SA1	88	-	SA17	122	-	A11
21	-	CLKI	55	-	SA2	89	-	GND	123	-	A12
22	-	GND	56	-	GND	90	-	SA18	124	-	A13
23	-	IRQ15	57	-	SA3	91	-	SA19	125	-	A14
24	-	IRQ14	58	-	SA4	92	-	RESET	126	-	A15
25	-	MSIRQ	59	-	SA5	93	-	VCC	127	-	A16
26	-	IRQ11	60	-	GND	94	-	GND	128	-	GND
27	-	IRQ10	61	-	VCC	95	-	$\overline{SMEMR}$	129	-	$\overline{IOSEL}$/DIV4-2N
28	-	IRQ9	62	-	SA6	96	-	$\overline{SMEMW}$	130	-	$\overline{DACK0}$/CLK_DIR
29	-	$\overline{IRQ8}$	63	-	SA7	97	-	$\overline{WE1}$	131	-	$\overline{DACK1}$
30	-	IRQ7	64	-	SA8	98	-	$\overline{MASTER}$	132	-	$\overline{DACK2}$
31	-	IRQ6	65	-	MXCTL0	99	-	ALE	133	-	$\overline{DACK3}$
32	-	IRQ5	66	-	MXCTL1	100	-	$\overline{READY}$	134	-	$\overline{DACK5}$
33	-	IRQ4	67	-	MXCTL2	101	-	W/$\overline{R}$	135	-	$\overline{DACK6}$
34	-	IRQ3	68	-	$\overline{LOMEG}$	102	-	DACKEN	136	-	$\overline{DACK7}$

TABLE 3-1. PIN ASSIGNMENTS

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PIN	MNEMONIC	I/O	SIGNAL NAME/DESCRIPTION
			AT BUS
1	SA0	I	**System Address 0** An input signal used for internal decoding of the keyboard controller chip select.
116 3	GIOW D1	I I	**Gate I/O Write** **Data Bit 1**
38	A20GTXO	I/O	**A20GATE** The D1 pin is used to trap IO writes to port 92. The A20GTXO output is OR of KBA20GT and port 92, bit 1. During power-on-reset when RESET is high, the A20GTXO pin is input and configures the 8- or 16-bit ROM signal. If the ROM8 signal is high, the platform is configured for an 8-bit width ROM. If the ROM8 signal is low the platform is configured for a 16-bit width ROM. Default ROM8 is pulled high with internal pull-up resistor.
7	SD7	I/O	Bit 7 of SD bus. SD7 is an input during IDE write and is an output during IDE read, except at 3F7H read, where SD7 is tristated. Connect is AT bus only if board IDE interface is implemented.
18	DRQIN	O	**Multiplexed DRQ Inputs** DRQIN selects the multiplexed DRQ0:7 to be connected to the WD76C10.
19	IRQSET0	O	**Interrupt Request Set 0** This pin outputs IRQSET0 for multiplexed Interrupt Request.
20	IRQSET1	O	**Interrupt Request Set 1** This pin outputs IRQSET1, the second set of multiplexed IRQ's for WD76C10A chips.
24, 23 28-26	IRQ 14-15 IRQ 9-11	I	Interrupt Request 14 and 15. Interrupt Request 9 through 11.
29	IRQ8	I	**Interrupt Request 8** This IRQ8 signal is inverted internally to generate IRQ8.
34-30	IRQ3-7	I	Interrupt Request 3 through 7.

TABLE 3-2. SIGNAL DESCRIPTONS

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PIN	MNEMONIC	I/O	SIGNAL NAME/DESCRIPTION
			AT BUS (Continued)
65	MXCTL0	I	**Multiplexer Control 0** MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1 and IRQSET0 control the internal multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, A20GT and RESCPU.
66	MXCTL1	I	**Multiplexer Control 1**
67	MXCTL2	I	**Multiplexer Control 2**
68	$\overline{\text{LOMEG}}$	I	**First Megabyte** $\overline{\text{LOMEG}}$ is asserted when the AT bus address is below 1 Mbyte. Used with $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ to generate $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$.
69	$\overline{\text{MEMW}}$	I	**Memory Write** The active low memory write stobe in AT mode for 8-/16-bit data transfers.
71	$\overline{\text{MEMR}}$	I	**Memory Read** The active low memory read stobe in AT mode for 8-/16-bit data transfers.
53	$\overline{\text{SBHE}}$	I/O	**System Byte High Enable** This signal is driven by the current bus owner to indicate that valid data resides on the SD8-SD15 lines.
54-55 57-59 62-64 77-79 81-83 86-88 90-91	SA1,SA2 SA3-SA5 SA6-SA8 SA9-11 SA12-14 SA15-17 SA18-19	I/O	**System Address SA9-SA19** Output AT address bus when MASTER is high. A1 through A23 and $\overline{\text{BHE}}$ are then latched internally with ALE and driven onto these pins. If $\overline{\text{MASTER}}$ is low, these pins are input and driven onto $\overline{\text{BHE}}$ A1 through A23.
92	RESET	O	**RESET** Active high reset signal for AT bus. 24 mA drive.
95	$\overline{\text{SMEMR}}$	O	**System Memory Read** The $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ are memory read/write signals which are active only within the first 1 Mbyte of the address space. Direct drive 24 mA derived from $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ and $\overline{\text{LOMEG}}$.
96	$\overline{\text{SMEMW}}$	O	**System Memory Write**

TABLE 3-2. SIGNAL DESCRIPTONS (Continued)

PIN	MNEMONIC	I/O	SIGNAL NAME/DESCRIPTION
			AT BUS (Continued)
98	MASTER	I	**Master** This signal is asserted by the Bus Master to indicate that a Bus Master cycle is occuring.
99	ALE	I	**Address Latch Enable** Used to clock the address latches
100	READY	I	**Processor Ready** This signal is an output enable to the processor.
102	DACKEN	I	**DACK Enable** DACKEN input, together with the MUXCTL0:2 demultiplexes the DACKs (DMA Acknowledge).
130	DACK0 /CLK_DIR	I/O	During power-on-reset if CLK_DIR is high, CPUCLK is the crystal output. If CLK_DIR is low, CPUCLK is the processor clock output and RDYIN is the crystal input
131-136	DACK1-3 DACK 5-7	O	DACKEN input, together with MUXCTL0:2 demultiplexes the DACKs.
103-106 36 72 15	DRQ0-3 DRQ5 DRQ6 DRQ7	I	**DMA Request Input Signals** These inputs are to be muxed onto DRQIN for WD76C10A. Internally they are pulled down by 2.2K.
117	GIOR	I	**Gated I/O Read** Active low. See Appendix A.

TABLE 3-2. SIGNAL DESCRIPTONS (Continued)

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PIN	MNEMONIC	I/O	SIGNAL NAME/DESCRIPTION
			MAIN PROCESSOR CONTROL
4	KBA20GT	I	**Keyboard Address Bit 20 Gate Signal** Input from the keyboard controller generated gate A20 signal.
5	RESCPUKB	I	**Keyboard Reset CPU** This input to Reset CPU is generated by the keyboard controller.
21	CLKI	I	**Clock Input** Clock input to the divider by 4 or divider by 2 circuitry.
2	CLK0	O	**Clock Output** Divided by 4 or divided by 2 clock frequency of CLKI depending on the trap input selection at IOSEL/DIV4-2N.
35	KBIRQ	I	**Keyboard Interrupt** Keyboard Interrupt from the keyboard controller.
37	$\overline{BHE}$	I/O	**Buffer High Enable**
108-115 120-127 9-14	A1-8 A9-16 A17-23	I/O	**Processor Address A1-A23** Input from the CPU or DMA when $\overline{MASTER}$ is high. The CPU address bus A1 through A23 and $\overline{BHE}$ is directly connected to these pins. The address bus is latched and output onto LA17 through LA23 and SA1 through SA19. $\overline{BHE}$ is latched and output onto $\overline{SBHE}$.
25	*MSIRQ	I	**Mouse Interrupt** Mouse Interrupt input from PS2 8042 chip.

* MSIRQ is dedicated to IRQ12 for onboard PS/2 mouse.

TABLE 3-2. SIGNAL DESCRIPTONS (Continued)

PIN	MNEMONIC	I/O	SIGNAL NAME/DESCRIPTION
			MISCELLANEOUS
39 97	$\overline{WE0}$ $\overline{WE1}$	O	**Write Enable 0 and 1** Active low buffered DRAM Write signal. One signal for 2 banks. Each can drive 300 pf.
70	IDE7	I/O	During IDE read, IDE7 is an input and is driven on to SD7. During IDE write, IDE7 is an output and the input source is SD7.
73 74	TEST1 TEST2	I	**TEST1** **TEST2** These are test input signals for scan design. In normal system operation, they are tied to Vcc.
101	W/$\overline{R}$	I	**Write Read Not** Active high W/$\overline{R}$ signal from WD76C10A for DRAM write. Generates $\overline{RW1}$ and $\overline{RW2}$.
129	$\overline{IOLSEL}$/ DIV4-2	I/O	Active low $\overline{IOSEL}$ signal. Used for full I/O address decode of super I/O chips. Goes active whenever SA15 through SA10 is low. It is an input during power-up-reset to select the internal divide by 4 or divide by 2 divider. If pulls low it will select divide by 2.
8,17,22,40,45, 49,51,56,60, 75,80,85,89, 94,107,119, 128	GND	I	Ground (17 pins)
6,16,41,50,52, 61,76,84,93, 118	Vcc	I	+5 Volts (10 pins)

TABLE 3-2. SIGNAL DESCRIPTONS (Continued)

4.0   ELECTRICAL SPECIFICATIONS

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4.1   DC OPERATING CHARACTERISTICS

MAXIMUM RATINGS
VCC = 5V ±10%
TA = 0°C (32°F) to + 70°C (158°F)

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SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vil	Input Low Voltage		0.6	V	
Vih	Input High Voltage	2.4		V	
Vol	Output Low Voltage		0.4	V	
Voh	Output High Voltage	3.5		V	
Icc	Power Supply Current				
	Leakage Current		1	uA	
	Pull Up Current	60	570	uA	$60 \leq Ipu \leq 570$ uA Typical Ipu = 220 uA Vin = GND
	Pull Down Current	60	570	uA	$60 \leq Ipd \leq 570$ uA Typical Ipd = 220 uA Vin = VCC

TABLE 4-1. DC OPERATING CHARACTERISTICS

4.2   AC OPERATING CHARACTERISTICS

This section contains tables for the valid output and input timing.

SIGNAL	REFERENCE	CAPLOAD	IOL+ IOH-	INTERNAL TERMINATION	DELAY (NS)
SA1-SA19 SBHE	ALE (falling edge)	200 pf	+ 24 mA - 12 mA		29 ns
LA17-LA23	READY (low)	200 pf	+ 24 mA - 12 mA		29 ns
A1-A23 BHE	SA1:16, LA17:23	100 pf	+8 mA - 2 mA		25 ns
A20GTXO	KBA20GT	50 pf	±2 mA	20 K Pull up	15 ns
IRQSET0 IRQSET1	MXCTL0:2 INT2-INT15	50 pf	±2 mA	20 K Pull up	20 ns
DRQIN	MXCTL0:3 DRQ0-DRQ7	50 pf	±2 mA		25 ns
SMEMR	MEMR LOMEG	200 pf	+ 24 mA - 12 mA	20 K Pull up	20 ns
SMEMW	MEMW LOMEG	200 pf	+ 24 mA - 12 mA	20 K Pull up	20 ns
RESET	DACKEN	200 pf	+ 24 mA - 12 mA	20 K Pull up	20 ns
WE0 WE1	W/R	300 pf	+ 24 mA		25 ns
DACK0:3 DACK5:7	DACKEN	50 pf	± 2 mA	20 K Pull up	15 ns
IOSEL	SA10-SA15	50 pf	±2 mA	20 K Pull up	20 ns
CLK0	CLKI	50 pf	±2 mA	20 K Pull up	25 ns
SD7	IDE7 GIOR	200 pf	±2 mA	20 K Pull up	20 ns

TABLE 4-2. OUTPUT TIMING

SIGNAL	REFERENCE	Iih Iil	INTERNAL TERMINATION	SETUP/HOLD
A1-A16	ALE (falling edge)	± 20 µA		10/5 ns
A17:23	READY (rising edge)	± 20 µA		10/5 ns
D1	GIOW	± 20 µA		10/5 ns
KBIRQ, MSIRQ, IRQ3-IRQ15	MXCTL0:2	± 400 µA	20K Pull up	
DRQ0:7		± 100 µA	10K Pull down	

TABLE 4-3. INPUT TIMING

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5.0   PACKAGE DIMENSIONS

Figure 5-1 illustrates the 136-Pin MFQP package.
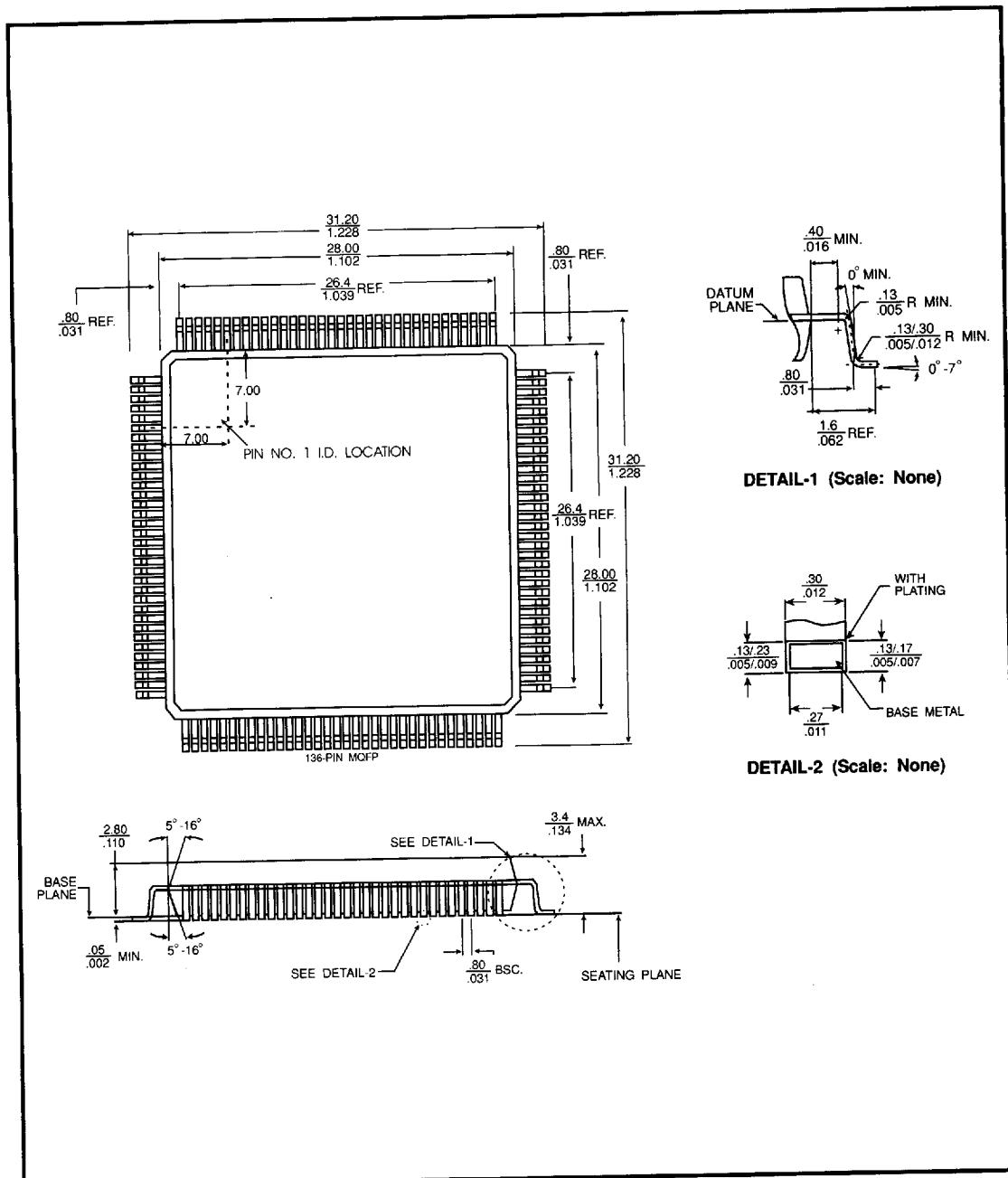
FIGURE 5-1. 136-PIN MQFP PACKAGE DIMENSIONS

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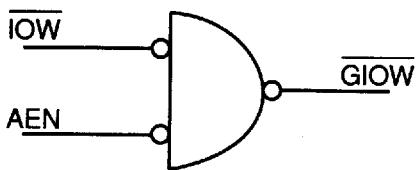
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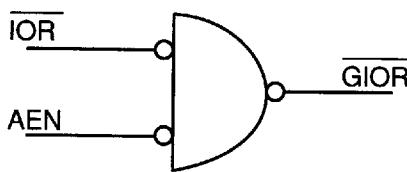
A.0   GATED I/O WRITE, I/O READ

The $\overline{\text{IOW}}$ and $\overline{\text{IOR}}$ signals need to qualify with AEN signals externally to generate I/O cycles only. GIOW and GIOR for WD7615 as shown in Figure A-1.


FIGURE A-1. GATED I/O WRITE AND I/O READ

B.0 I/O MAPPING

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In I/O mapping mode the input pins are multiplexed to the output pins as shown in Figure B-1.

| Inputs	Output
SD7, MXCTL1, DRQ0, DRQ6, SA2, $\overline{DRQ}$, $\overline{READY}$, ALE, SA11, KBA20GT, CLKI	A20GTX0
IRQ7, $\overline{GIOR}$, IRQ9, $\overline{LOMEG}$, IRQ11, IRQ14	IRQSET0
$\overline{MEMW}$, $\overline{MEMR}$, $\overline{GIOW}$, IRQ8, IRQ10, WR	$\overline{IOSEL}$
$\overline{DRQ5}$, $\overline{MASTER}$, RESCPUKB, MXCTL0, DACKEN	RESET
KBIRQ, MSIRQ, LA18, IRQ4, LA22, IRQ6	IRQSET1
SA0, SA1, DRQ1, SA3, DRQ3, SA5	$\overline{DACK0}$
SA6, SA13, SA8, A9, SA10, SA11	$\overline{DACK1}$
SA12, SA7, SA14, SA15, SA10, SA17	$\overline{DACK2}$
LA17, IRQ3, LA19, LA21, IRQ5, LA23	$\overline{DACK3}$
A1, A3, A5, A7, A10, A12	$\overline{DACK5}$
A2, A4, A6, A8, A9, A11	$\overline{DACK6}$
A14, A16, A18, A21, A23, SA18	$\overline{DACK7}$
DRQ7, MXCTL2, D1, $\overline{BHE}$, $\overline{SBHE}$, IRQ15	$\overline{SMEMR}$
A13, A15, A17, A19, A22, SA19	$\overline{SMEMW}$

FIGURE B-1. I/O MAPPING MODES