1.0 INTRODUCTION

1.1 DESCRIPTION

The WD6022 devices form part of Western Digital's® innovative WD6500 chip set, which facilitates the design and implementation of 32-bit Micro Channel system boards. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, also reducing system cost and increasing system reliability.

The chip set contains two WD6022 devices, one configured as an Address Buffer Device, and the other as a Data Buffer Device. Configuration is determined by a Mode pin. When this is zero, the device is configured as an address buffer; when it is one, the device is configured as a data buffer.

The block diagram in Figure 1 illustrates a typical system using the WD6500 chip set, and shows the two WD6022 devices. Devices with bold outlines are available from Western Digital Corporation.

1.2 FEATURES

- Provides Address and Data Buffers that interface to the Micro Channel
- Meets Micro Channel AC/DC Specifications
- Contains Peripheral Bus Address and Data Buffers
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

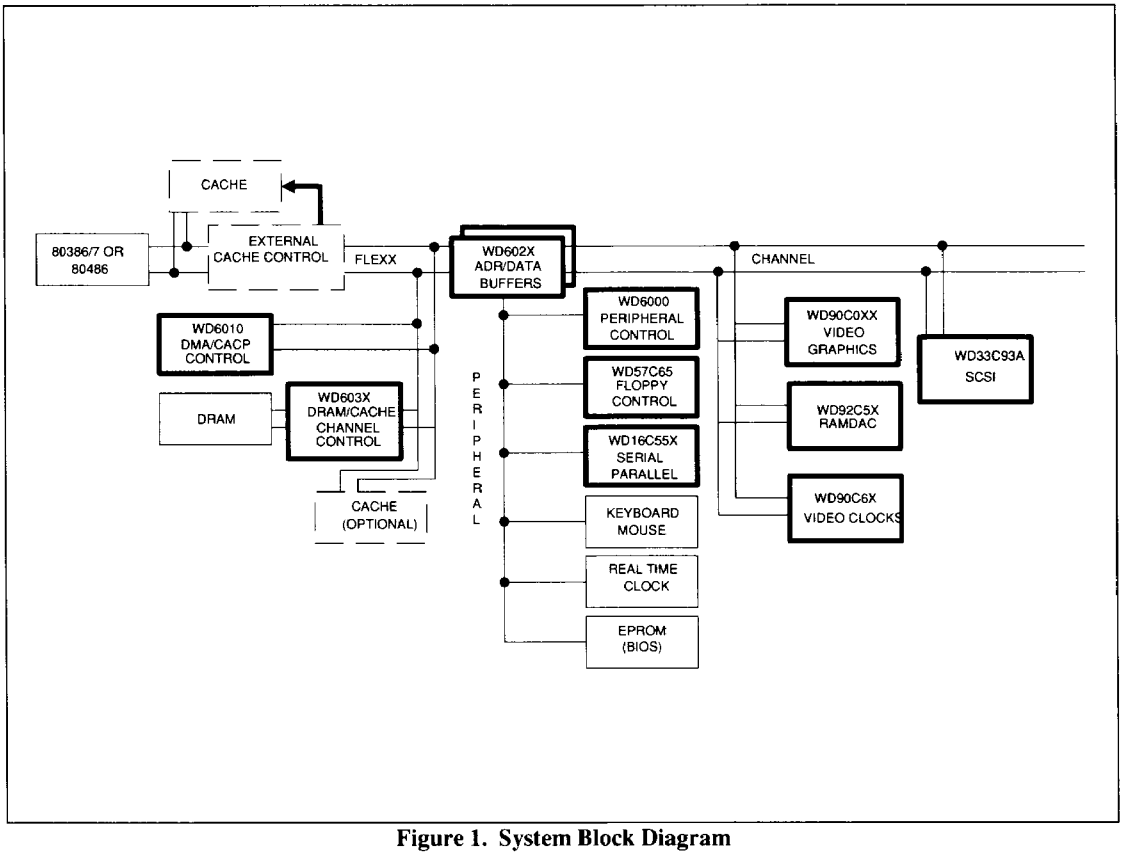

Figure 1. System Block Diagram

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2.0 ADDRESS AND DATA BUFFER DEVICES

The WD6500 chip set contains two WD6022 Address and Data Buffer Devices, one configured as an Address Buffer Device, and the second as a Data Buffer Device.

Address Buffer Configuration

To configure the WD6022 as an address buffer, the MODE signal (pin 66) is tied to ground. When configured as an address buffer, the WD6022 performs address bus latches, implements the Central Translator function for the Micro Channel and provides decodes for the BIOS EPROMs.

Data Buffer Configuration

To configure the WD6022 as a data buffer, the MODE signal is tied to power. In this mode, the WD6022 performs data bus latches, Micro Channel data steering and data swaps for 80386/80486 and DMA operations.

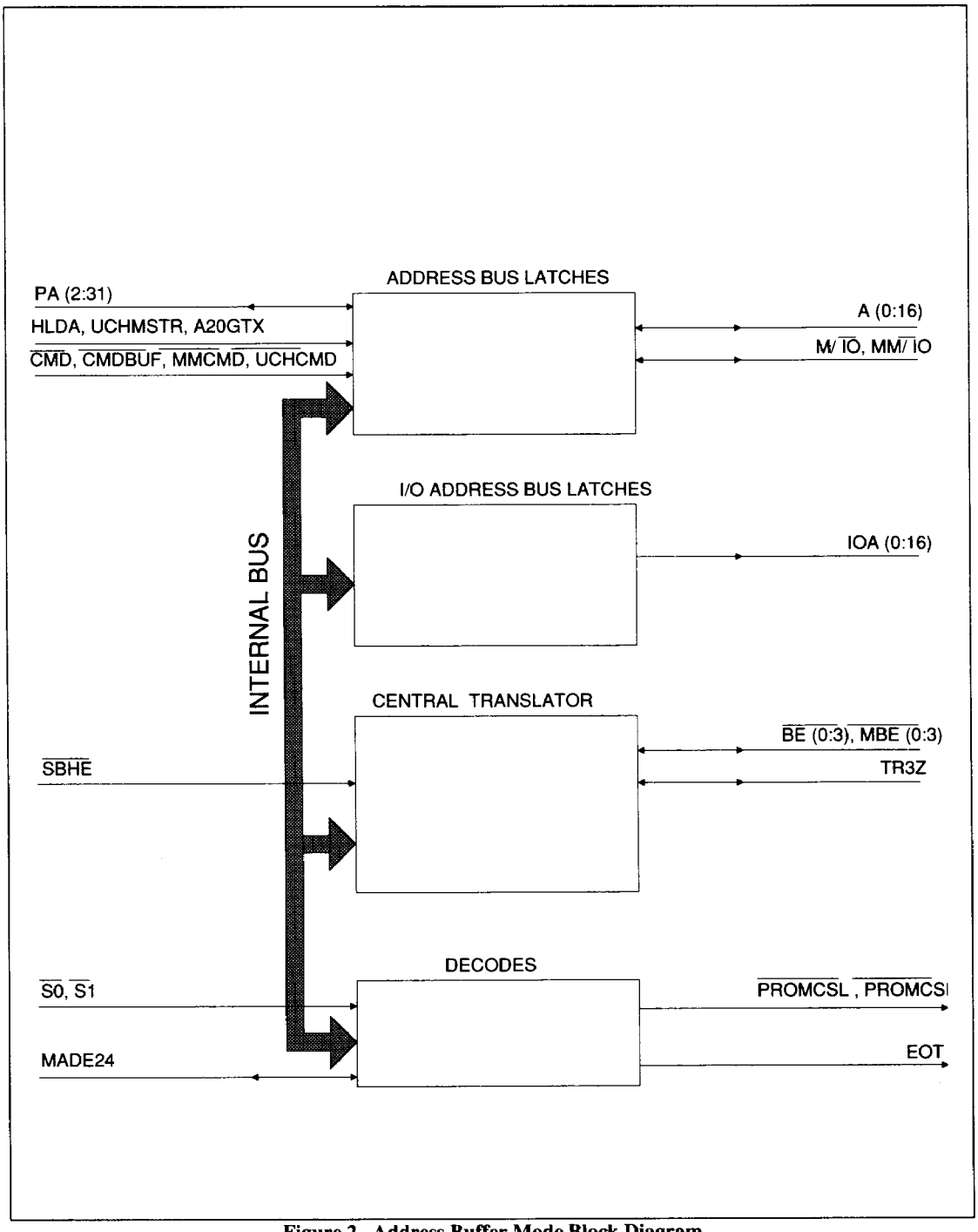

Figure 2. Address Buffer Mode Block Diagram

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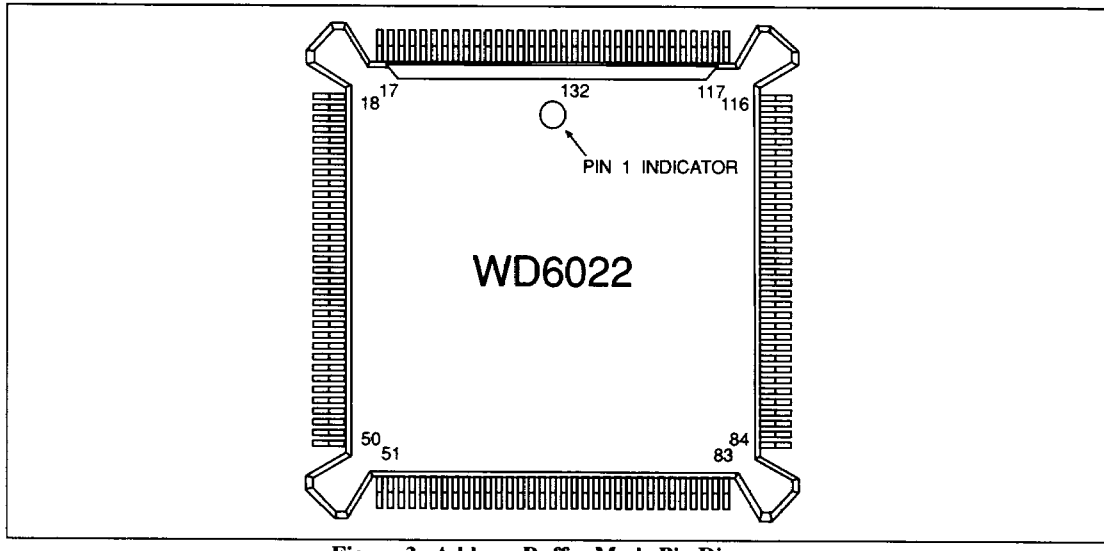

Figure 3. Address Buffer Mode Pin Diagram

PIN	–	NAME	PIN	–	NAME	PIN	–	NAME	PIN	–	NAME
1	–	IOA9	34	–	A9	67	–	$\overline{\text{TEST}}$	100	–	V_{DD}
2	–	IOA8	35	–	V_{DD}	68	–	MM/$\overline{\text{IO}}$	101	–	PA20
3	–	V_{DD}	36	–	A10	69	–	UCHCMD	102	–	PA19
4	–	IOA7	37	–	A11	70	–	$\overline{\text{EOT}}$	103	–	PA18
5	–	IOA6	38	–	V_{SS}	71	–	$\overline{\text{PROMCSL}}$	104	–	PA17
6	–	IOA5	39	–	A12	72	–	PROMCSH	105	–	PA16
7	–	IOA4	40	–	A13	73	–	$\overline{\text{RESERVED}}$	106	–	PA15
8	–	IOA3	41	–	A14	74	–	$\overline{\text{BE2}}$	107	–	PA14
9	–	IOA2	42	–	A15	75	–	$\overline{\text{BE3}}$	108	–	PA13
10	–	IOA1	43	–	V_{SS}	76	–	V_{SS}	109	–	V_{SS}
11	–	IOA0	44	–	A16	77	–	$\overline{\text{MBE0}}$	110	–	PA12
12	–	MADE24	45	–	A17	78	–	$\overline{\text{MBE1}}$	111	–	PA11
13	–	$\overline{\text{TR32}}$	46	–	V_{DD}	79	–	$\overline{\text{MBE2}}$	112	–	PA10
14	–	$\overline{\text{CMDBUF}}$	47	–	A18	80	–	$\overline{\text{MBE3}}$	113	–	PA9
15	–	$\overline{\text{A20GTX}}$	48	–	A19	81	–	M/$\overline{\text{IO}}$	114	–	PA8
16	–	$\overline{\text{S1}}$	49	–	A20	82	–	BIAS	115	–	PA7
17	–	V_{SS}	50	–	V_{SS}	83	–	V_{DD}	116	–	V_{DD}
18	–	V_{SS}	51	–	V_{SS}	84	–	$\overline{\text{HLDA}}$	117	–	V_{SS}
19	–	$\overline{\text{S0}}$	52	–	A21	85	–	$\overline{\text{MMCMD}}$	118	–	PA6
20	–	$\overline{\text{CMD}}$	53	–	A22	86	–	SBHE	119	–	PA5
21	–	UCHMSTR	54	–	A23	87	–	V_{SS}	120	–	PA4
22	–	A0	55	–	A24	88	–	PA31	121	–	PA3
23	–	A1	56	–	A25	89	–	PA30	122	–	$\overline{\text{PA2}}$
24	–	V_{DD}	57	–	V_{DD}	90	–	PA29	123	–	$\overline{\text{BE1}}$
25	–	A2	58	–	A26	91	–	PA28	124	–	$\overline{\text{BE0}}$
26	–	A3	59	–	A27	92	–	PA27	125	–	IOA16
27	–	V_{SS}	60	–	V_{SS}	93	–	PA26	126	–	IOA15
28	–	A4	61	–	A28	94	–	PA25	127	–	IOA14
29	–	A5	62	–	A29	95	–	PA24	128	–	IOA13
30	–	A6	63	–	A30	96	–	PA23	129	–	IOA12
31	–	A7	64	–	A31	97	–	PA22	130	–	IOA11
32	–	V_{SS}	65	–	V_{SS}	98	–	V_{SS}	131	–	IOA10
33	–	A8	66	–	MODE	99	–	PA21	132	–	V_{SS}

Table 1. Address Buffer Mode (Mode = 0) Pinout

2.1 ADDRESS BUFFER MODE PIN DESCRIPTIONS

PIN NO.	NAME	TYPE	FUNCTION
			ADDRESS BUS LATCHES
22 23 25 26 28 29 30 31 33 34 36 37 39 40 41 42 44 45 47 48 49 52 53 54 55 56 58 59 61 62 63 64	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A34 A25 A26 A27 A28 A29 A30 A31	I	CHANNEL ADDRESS BUS This Channel address bus interfaces directly to the Channel. It is an input during 80386/DMA cycles. Note that A0 is always an input, and is generated by the WD6030 during 80386/DMA cycles.
124 123 122 121 120 119 118 115 114 113 112 111 110 108 107 106	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15	I/0	PROCESSOR ADDRESS BUS This is the local processor address bus on the motherboard, and interfaces directly with the processor address bus. It is an input for 80386/80486/DMA cycles and output for master cycles.

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PIN NO.	NAME	TYPE	FUNCTION
105 104 103 102 101 99 97 96 95 94 93 92 91 90 89 88	PA16 PA17 PA18 PA19 PA20 PA21 PA22 PA23 PA24 PA25 PA26 PA27 PA28 PA29 PA30 PA31	I/O	PROCESSOR ADDRESS BUS (CONT)
11 10 9 8 7 6 5 4 2 1 131 130 129 128 127 126 125	IOA0 IOA1 IOA2 IOA3 IOA4 IOA5 IOA6 IOA7 IOA8 IOA9 IOA10 IOA11 IOA12 IOA13 IOA14 IOA15 IOA16	O	I/O ADDRESS BUS This is the I/O address bus on the system board. It is the latched version of the addresses on the Channel. The I/O address bus supplies the addresses to all the Channel peripherals on the system board, such as the video, floppy, serial port, parallel port, timer and interrupt controllers, and EPROM.
84	HLDA 80386/ 80486	I	HOLD ACKNOWLEDGE The CPU generates this signal in response to a HOLD signal from the DMA controller. When active, it indicates that the CPU has relinquished control of the local bus.
21	UCHMSTR	I	CHANNEL MASTER This signal is generated by the CXACP in the WD6010. When active, it indicates that a Channel master has control ofthe bus. It is used to control the direction of the address buffers.
15	A20GTX	I	ADDRESS BIT 20 GATE SIGNAL This signal is generated by the WD6010, and has no effect on the address when the DMA or Micrh Channel master is generating the addresses. It is encoded in the following manner: **HLDA UCHMSTR A20GTX A20 SOURCE DEVICE** **0 0 0 0 80386/80486** **0 0 1 PA20 80386/80486** **1 0 x PA20 DMA** **1 1 x A20 Micro Channel Master**

PIN NO.	NAME	TYPE	FUNCTION
20	$\overline{\text{CMD}}$	I	$\overline{\text{COMMAND}}$ The Command signal generates the latch signal that latches the Channel addresses when a Channel master has the bus.
14	$\overline{\text{CMDBUF}}$	I	$\overline{\text{BUFFERED CHANNEL COMMAND}}$ This signal latches the Channel addresses for the IOA (16:0) address bus. The input to this signal is the $\overline{\text{CMD}}$ signal which is generated by the WD6030.
85	$\overline{\text{MMCMD}}$	I	$\overline{\text{CHANNEL MATCHED MEMORY COMMAND}}$ This is the Matched Memory Command signal on the Channel. This signal is pulled-up as MMC is not supported.
69	UCHCMD	O	CHANNEL COMMAND This signal is the logical OR of the $\overline{\text{CMD}}$ and $\overline{\text{MMCMD}}$ signals, and indicates that a command is present on the Channel. It is used in the WD6010 diagnostic interface.
81	M/$\overline{\text{IO}}$	I/O	LOCAL BUS M/IO The M/IO signal is on the local bus, and interfaces directly with the M/$\overline{\text{IO}}$ signal on the CPU. When a Channel master accesses the system board DRAM, this signal is a latched version of the MM/IO signal.
68	MM/$\overline{\text{IO}}$	I/O	CHANNEL M/$\overline{\text{IO}}$ This signal interfaces directly with the Channel M/$\overline{\text{IO}}$ signal, a delayed version of the $\overline{\text{CMD}}$ signal generated by the WD6000. When the 80386 or the DMA accesses the Channel, this signal is the same as M/IO.
			CENTRAL TRANSLATOR
86	$\overline{\text{SBHE}}$	I	$\overline{\text{SYSTEM BYTE HIGH ENABLE}}$ The System Byte High Enable signal on the Channel interfaces directly to $\overline{\text{SBHE}}$ on the Channel. When the address flow is from the processor bus to the Channel bus, the WD6030 generates this signal as a decode of $\overline{\text{BE}}$ (0:3). When the address flow goes from the Channel bus to the processor bus, this signal is used in the central translator function.
13	TR32	I/O	TRANSLATE 32 The Translate 32 signal on the Channel is used in the central translator logic. When it is active, the central translator translates A0, A1, and $\overline{\text{SBHE}}$ to $\overline{\text{BE}}$ (0:3). TR32 is used for a 16-bit master communicating with a 32-bit slave.
124 123 74 75	$\overline{\text{BE0}}$ $\overline{\text{BE1}}$ $\overline{\text{BE2}}$ $\overline{\text{BE3}}$	I/O	$\overline{\text{BYTE ENABLES}}$ These byte enables on the local bus interface directly with the 80386/80486 byte enables. When the address flow is from the processor address bus to the Channel address bus, these signals generate Address Bit 1 (A1). A0 is generated by the WD6030. When the address flow is from the Channel address bus to the processor address bus, these signals are generated by a 32-bit master on the Channel or the central translator for a 16-bit master.
77 78 79 80	$\overline{\text{MBE0}}$ $\overline{\text{MBE1}}$ $\overline{\text{MBE2}}$ $\overline{\text{MBE3}}$	I/O	$\overline{\text{CHANNEL BYTE ENABLES}}$ These Channel byte enable signals interface directly to the $\overline{\text{BE}}$ (0:3) on the Micro Channel. During an 80386/80486/DMA cycle, these signals are outputs. For a master cycle they are not input signals.
			DECODES
19 16	$\overline{\text{S0}}$ S1	I	CHANNEL CONTROL SIGNALS These two signals interface directly to the Channel $\overline{\text{S}}$(0:1) signals. Together with MADE24, MM/IO, and the Channel address, it generates the PROM chip selects.

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PIN NO.	NAME	TYPE	FUNCTION
12	MADE24	I/O	CHANNEL MADE24 SIGNAL This signal directly interfaces with the Channel MADE24 signal. In combination with S(0:1) and MM/IO, it generates the PROM chip selects. During 80386/80486/DMA cycles, this signal is an output signal. **ADDRESSES** **MADE24** 0-16 MBytes 1 >16 MBytes 0
71 72	PROMCSL PROMCSH	O O	PROM CHIP SELECT (Low) PROM CHIP SELECT (High) These signals select the two 64K by 8 (27512) PROMs which together form the 128K of PROM on the system board. The two PROMs are organized into even and odd banks, providing a 16-bit wide interface. PROMCSL selects the even banks and PROMCSH selects the odd banks. Configurations with 8-bit wide, 1 M bit PROMs (27010) are also possible. In such a case, PROM Chip Select is generated by executing a logical OR of PROMCSL and PROMCSH. To get the BIOS to execute faster, the PROM can be mapped to the DRAM and executed from there. The PROMs are located at 000E0000H - 000FFFFFH and at FFFE0000 - FFFFFFFFH. An access to either of these locations generates the chip selects for the PROM. However, a Channel cycle to access the PROM will only be run if an access is made to FFFE0000 - FFFFFFFFH, or if a read access is made to E0000 -FFFFF, and the PROM is not mapped to RAM. Writes to these addresses are ignored.
70	EOT	O	END-OF-TRANSFER This signal is activated when $\overline{CMD}$ and $\overline{S}$(1:0) are inactive. The CACP controller inside the WD6010 uses this signal and BURST to detect an End-of-Transfer condition.
			MISCELLANEOUS
66	MODE	I	MODE PIN This pin determines the mode of operation for the WD6022 device. When tied to V_{DD}, it puts the WD6022 into the data buffer mode; when it is tied to ground, it puts it into the address buffer mode
67	TEST	I	$\overline{TEST}$ PIN This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines so that an ATE tester can drive these signals instead.
82	BIAS	I	BIAS PIN This pin controls the biasing of the internal buffers, and should be pulled low with a 1.25K ±1% resistor.
3, 24, 35, 46,57, 83, 100, 116	V_{DD}	I	+5 V Power Supply
17, 18, 27, 32, 38, 43, 50, 51, 60, 65, 76, 87, 98, 109, 117, 132	V_{SS}	I	O V Ground

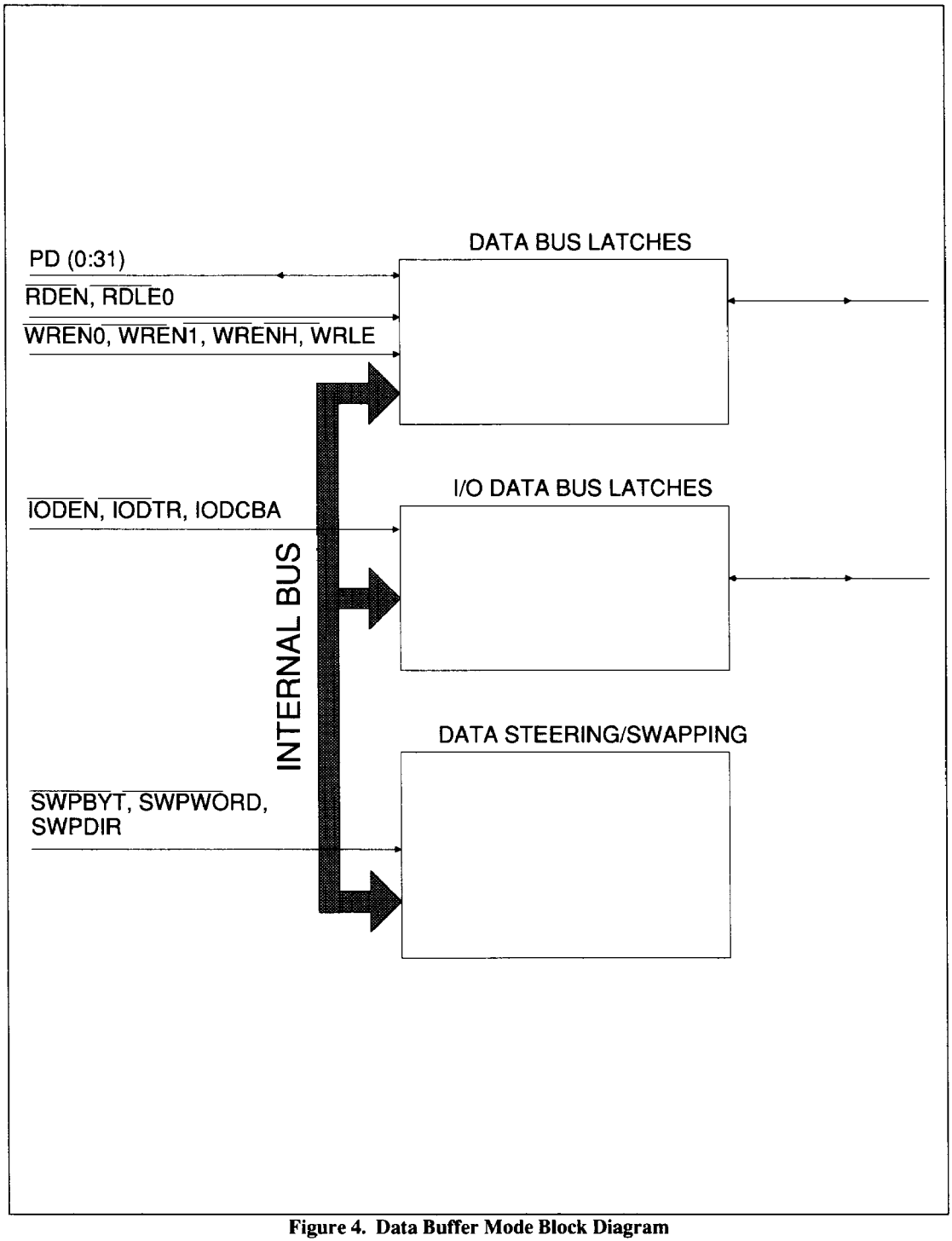

Figure 4. Data Buffer Mode Block Diagram

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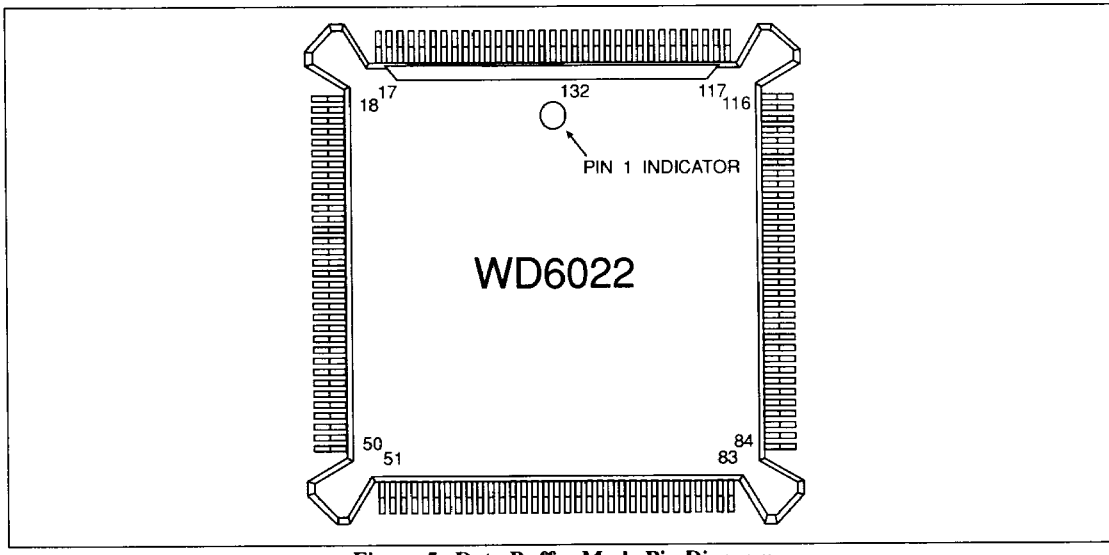

Figure 5. Data Buffer Mode Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	IOD9	34	D9	67	$\overline{\text{TEST}}$	100	V_{DD}
2	IOD8	35	V_{DD}	68	RESERVED	101	PD20
3	V_{DD}	36	D10	69	RESERVED	102	PD19
4	IOD7	37	D11	70	RESERVED	103	PD18
5	IOD6	38	V_{SS}	71	RESERVED	104	PD17
6	IOD5	39	D12	72	RESERVED	105	PD16
7	IOD4	40	D13	73	RESERVED	106	PD15
8	IOD3	41	D14	74	RESERVED	107	PD14
9	IOD2	42	D15	75	RESERVED	108	PD13
10	IOD1	43	V_{SS}	76	V_{SS}	109	V_{SS}
11	IOD0	44	D16	77	RESERVED	110	PD12
12	$\overline{\text{IODEN}}$	45	D17	78	RESERVED	111	PD11
13	IODTR	46	V_{DD}	79	RESERVED	112	PD10
14	$\overline{\text{WRLE}}$	47	D18	80	RESERVED	113	PD9
15	$\overline{\text{WRENH}}$	48	D19	81	RESERVED	114	PD8
16	$\overline{\text{WREN1}}$	49	D20	82	BIAS	115	PD7
17	V_{SS}	50	V_{SS}	83	V_{DD}	116	V_{DD}
18	V_{SS}	51	V_{SS}	84	$\overline{\text{SWPDIR}}$	117	V_{SS}
19	$\overline{\text{WREN0}}$	52	D21	85	$\overline{\text{SWPWORD}}$	118	PD6
20	$\overline{\text{RDLE0}}$	53	D22	86	$\overline{\text{SWPBYT}}$	119	PD5
21	$\overline{\text{RDEN}}$	54	D23	87	V_{SS}	120	PD4
22	D0	55	D24	88	PD31	121	PD3
23	D1	56	D25	89	PD30	122	PD2
24	V_{DD}	57	V_{DD}	90	PD29	123	PD1
25	D2	58	D26	91	PD28	124	PD0
26	D3	59	D27	92	PD27	125	IODCBA
27	V_{SS}	60	V_{SS}	93	PD26	126	IOD15
28	D4	61	D28	94	PD25	127	IOD14
29	D5	62	D29	95	PD24	128	IOD13
30	D6	63	D30	96	PD23	129	IOD12
31	D7	64	D31	97	PD22	130	IOD11
32	V_{SS}	65	V_{SS}	98	V_{SS}	131	IOD10
33	D8	66	MODE	99	PD21	132	V_{SS}

Table 2. Data Buffer Mode (Mode = 1) Pinout

2.2 DATA BUFFER MODE PIN DESCRIPTIONS

PIN NO.	NAME	TYPE	FUNCTION
			DATA BUS LATCHES
22 23 25 26 28 29 30 31 33 34 36 37 39 40 41 42 44 45 47 48 49 52 53 54 55 56 58 59 61 62 63 64	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31	I/O	CHANNEL DATA BUS These Channel data bus signal lines connect directly to the Channel data bus.
124 123 122 121 120 119 118 115 114 113 112 111 110 108 107 106	PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7 PD8 PD9 PD10 PD11 PD12 PD13 PD14 PD15	I/O	PROCESSOR DATA BUS These processor data bus signal lines connect directly to the 80386 data bus.

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PIN NO.	NAME	TYPE	FUNCTION
105 104 103 102 101 99 97 96 95 94 93 92 91 90 89 88	PD16 PD17 PD18 PD19 PD20 PD21 PD22 PD23 PD24 PD25 PD26 PD27 PD28 PD29 PD30 PD31	I/O	PROCESSOR DATA BUS (CONT)
11, 9-4, 3-1, 13-125	IOD (0:15) to IOD (0:0)	I/O	16-BIT I/O DATA BUS This is the 16-bit I/O data bus, which provides support for devices eight bits or sixteen bits wide.
21	$\overline{\text{RDEN}}$	I	$\overline{\text{READ ENABLE}}$ This read-enable signal enables for the processor data bus (PD (0:31)) when data flows from the Channel data bus to the processor data bus. This signal is active when the CPU or the DMA performs a read from the Channel, or when a Channel master writes to the system board DRAM.
20	$\overline{\text{RDLE0}}$	I	$\overline{\text{READ LATCH ENABLE 0}}$ This signal is the latch enable signal for Byte 0 (0:7). When the CPU or the DMA performs a cycle to an 8-bit device on the Channel, the cycle is split in two. This signal latches the first 8 bits (0:7) during the first cycle, reads the next 8 bits (8:15) during the second cycle, and this presents the 16 bits to the CPU.
19 16 15	$\overline{\text{WREN0}}$ $\overline{\text{WREN1}}$ WRENH	I	$\overline{\text{WRITE ENABLE (HIGH, 0:1)}}$ This signal enables the buffer during data flow from the processor data bus to the Channel data bus D (0:31). These signals control Byte 0 (0:7) (WREN0), byte 1 (8:15) (WREN1), and the upper word (16:31) (WRENH). These signals are valid when the CPU or the DMA performs a write operation to the Channel or when a Channel master performs a read from the motherboard DRAM.
14	$\overline{\text{WRLE}}$	I	$\overline{\text{WRITE LATCH ENABLE}}$ This write latch enable signal latches the write data during a CPU or DMA write operation to the Channel. It also provides the write-data-hold time required by the Channel during these operations. This signal also latches the data when the CPU or DMA writes to an 8-bit port and the cycle has to be split in two.
12	$\overline{\text{IODEN}}$	I	$\overline{\text{I/O DATA ENABLE}}$ The I/O Data Enable signal enables the I/O data buffers and is generated by the WD6000. When it is active, the WD6022 drives either D(0:15) or IOD(0:15), depending on the direction set by the IODTR signal.
13	IODTR	I	I/O DATA TRANSMIT/RECEIVE The I/O Data Transmit/Receive signal controls the direction of the I/O data buffers inside the WD6022. The signal itself is generated by the WD6000 device. **IODTR** — **DIRECTION** 1 — D(0:15) to IOD(0:15) 0 — IOD(0:15) to D(0:15)

PIN NO.	NAME	TYPE	FUNCTION
125	IODCBA	I	I/O DATA CLOCK The I/O Data Clock signal is used to latch the data during reads from the Channel peripherals on the I/O bus. The MEMRD, MEMWR, IORD, and IOWR commands to the peripherals are shorter than the Channel CMD signal. This signal ensures that the data being read meets the timings of the Channel CMD signal.
			DATA STEERING/SWAPPING
86	$\overline{\text{SWPBYT}}$	I	$\overline{\text{BYTE SWAP}}$ When the CPU or DMA accesses an 8-bit port the cycle is split into two. This signal is used to swap the data to the correct byte: D(0:7) are swapped to D(8:15) for a read operation; D(8:15) are swapped to D(0:7) for a write operation.
85	$\overline{\text{SWPWORD}}$		$\overline{\text{WORD SWAP}}$ This signal swaps words when a 16-bit Channel master communicates with a 32-bit slave. The cycle is split into two and SWPWORD is used to swap data to the correct word: D(16:31) is swapped to D(0:15) for a Channel master read operation and D(0:15) is swapped to D(16:31) for a Channel master write operation. This function is known as data steering.
84	SWPDIR (COPRES)	I	SWAP DIRECTION At power-up, the state of this signal is latched by the WD6030 to determine the presence of the numeric coprocessor. At all other times, SWPDIR determines the direction of the byte and word swap buffers. A low on SWPDIR indicates a read operation (byte swap D(0:7) to D(8:15) or a Channel master write operation (word swap D(0:15) to D(16:31)). A high on SWPDIR indicates a write operation (byte swap D(8:15) to D(0:7)).
			MISCELLANEOUS
66	MODE	I	MODE PIN This pin determines the mode of operation for the WD6022 device. When tied to V_{DD}, it puts the WD6022 into the data buffer mode; when it is tied to ground, it puts it into the address buffer mode..
67	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines so that an ATE tester can drive these signals instead.
82	BIAS	I	BIAS PIN This pin controls the biasing of the internal buffers, and should be pulled low with a 1.25K ±1% resistor.
3, 24, 35, 46,57, 83, 100, 116	V_{DD}	I	+5 V Power Supply
17, 18, 27, 32, 38, 43, 50, 51, 60, 65, 76, 87, 98, 109, 117, 132	V_{SS}	I	0 V Ground

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PIN NO.	NAME	TYPE	FUNCTION
68, 69, 70, 71, 72, 73, 74, 75, 77, 78, 79, 80, 81	Reserved	-	RESERVED PINS These pins should not be connected.

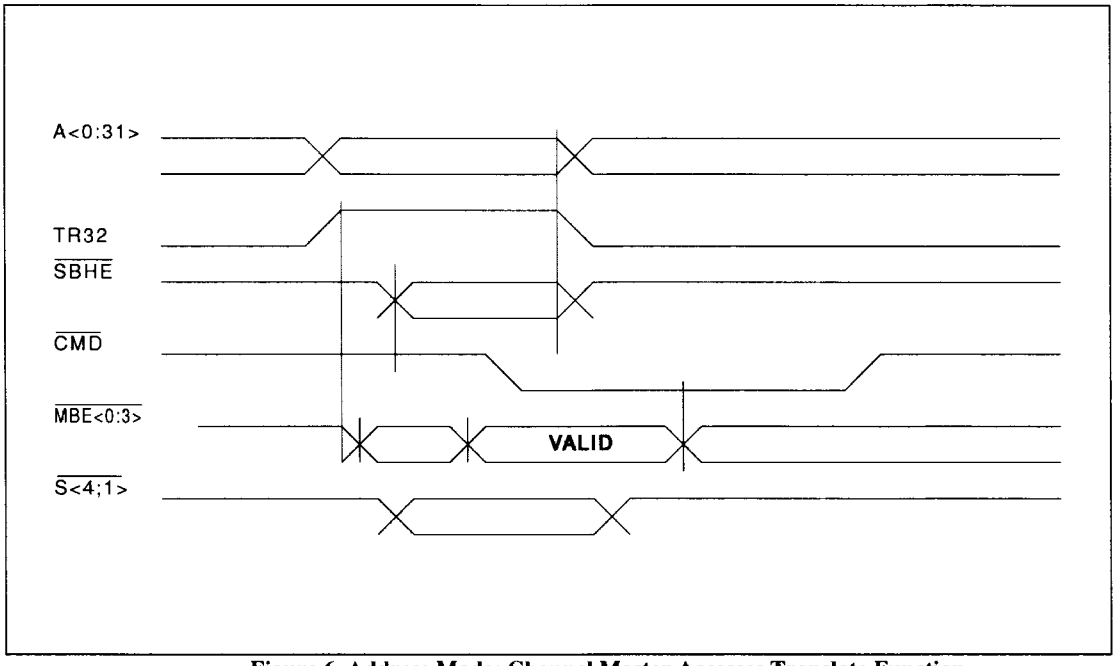


Figure 6. Address Mode: Channel Master Accesses Translate Function

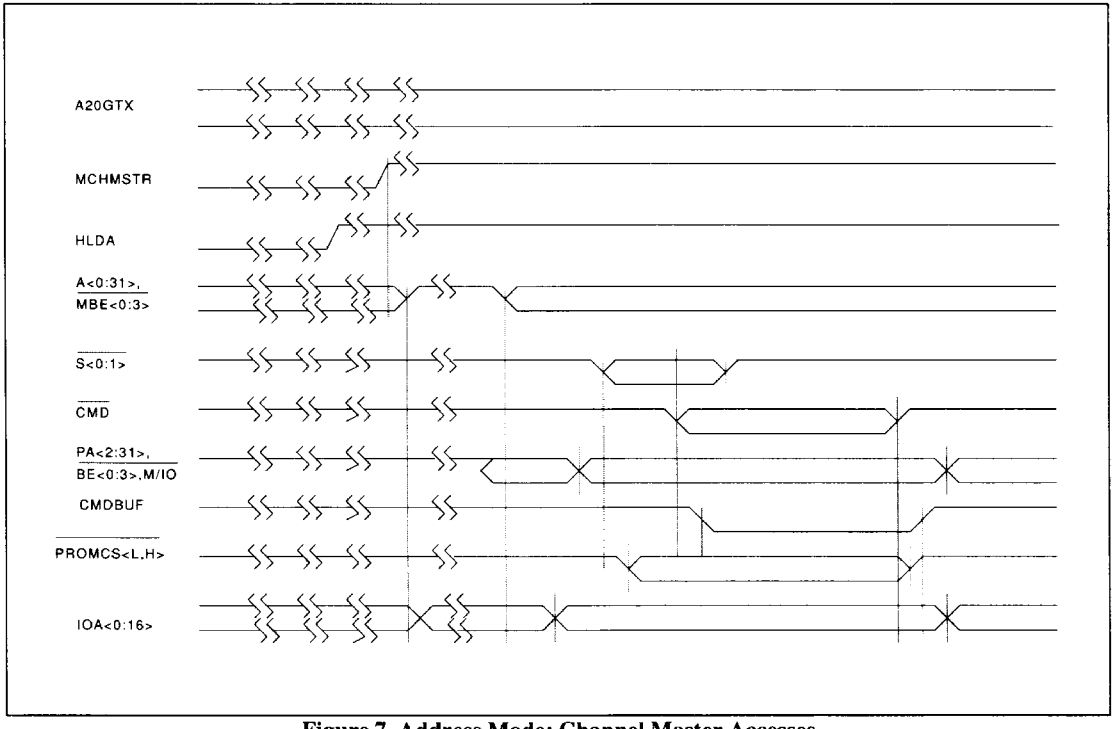


Figure 7. Address Mode: Channel Master Accesses

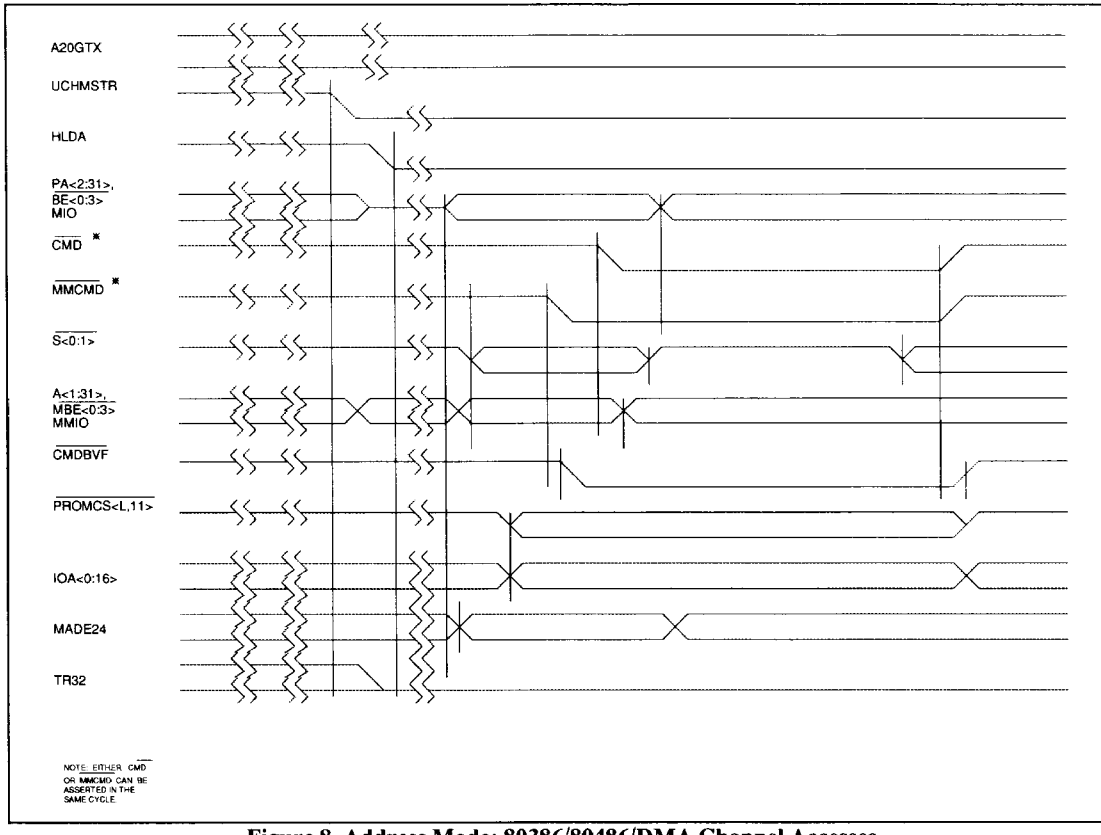


Figure 8. Address Mode: 80386/80486/DMA Channel Accesses

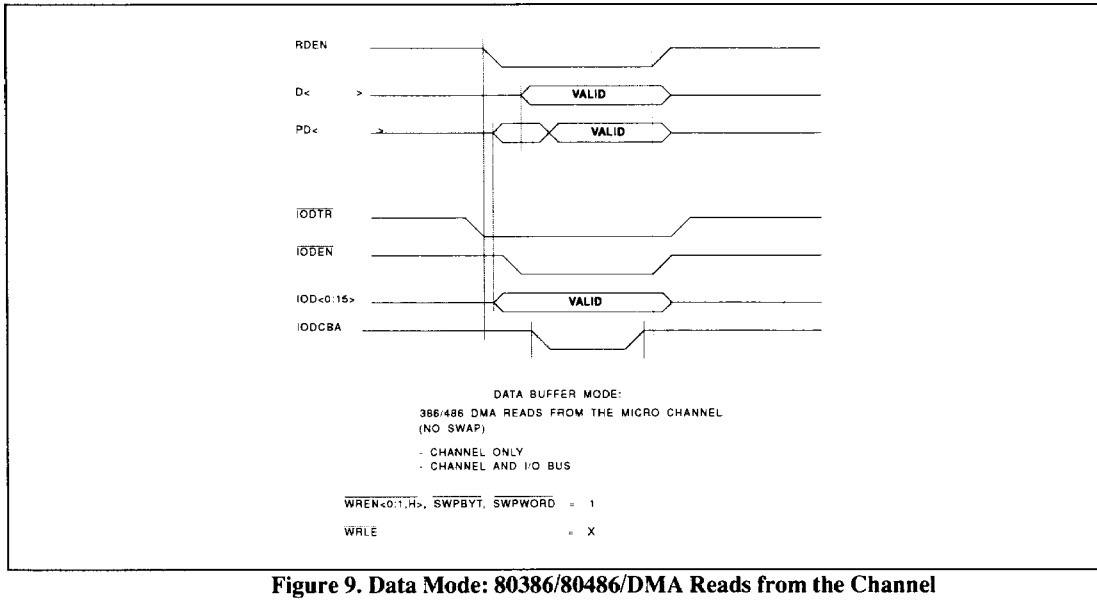
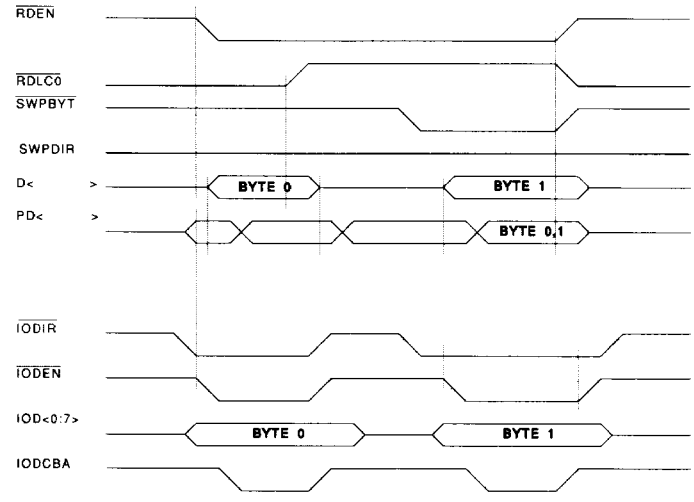


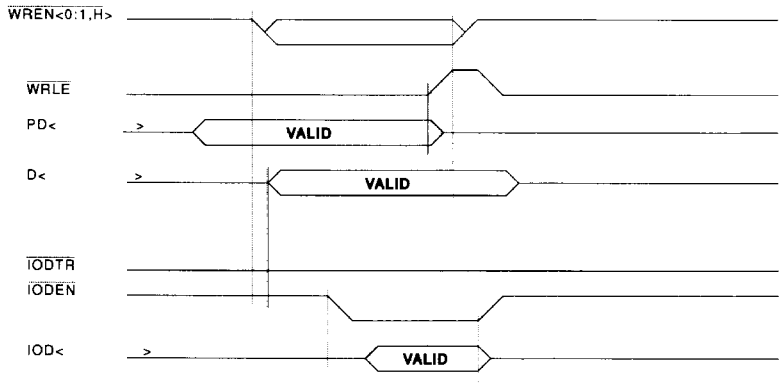
Figure 9. Data Mode: 80386/80486/DMA Reads from the Channel



WD6021: 386/486 DMA READS FROM THE MICRO CHANNEL
(WITH SWAP)
- CHANNEL ONLY
- CHANNEL AND I/O BUS

$\overline{WREN}$<0:1,H>, $\overline{SWPWORD}$ = 1
$\overline{WRLE}$ = X

Figure 10. Data Mode: 80386/80486/DMA Reads from the Channel with Swap



WD6021: 386/486 DMA - WRITES TO THE MICRO CHANNEL
(NO SWAP)
- CHANNEL ONLY
- CHANNEL AND I/O BUS

$\overline{RDEN}$, $\overline{SWPBYT}$, $\overline{SWPWORD}$ = 1
$\overline{RDLE0}$, SWPDIR, IODCBA = X

Figure 11.Data Mode: 80386/80486/DMA Writes to the Channel

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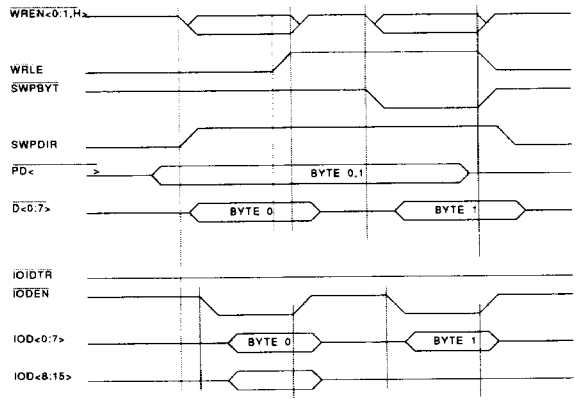

Figure 12. Data Mode: 80386/80486/DMA Writes to the Channel with Swap

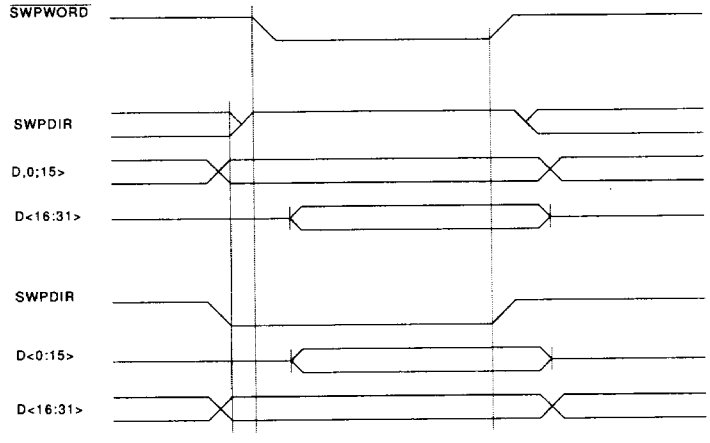

Figure 13. Data Mode: Channel Master Word Swap

3.0 TECHNICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for the WD6022 devices are tabulated below. Permanent damage to the devices could result from exposing it to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD} - V_{SS}	0	7	V
Input Voltage	V_{IABS}	VSS - 0.3	V_{DD} + 0.3	V
Bias on Output Pin	V_{OABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	T_S	-40	125	°C

3.2 NORMAL OPERATING CONDITIONS

Exposing the WD6022 to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

VSS = 0 V

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	VDD + 0.3	V
Power Dissipation	P_W	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

3.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ fc = 1 MHz	C_I	-	5	pF
I/O Capacitance	C_{IO}	-	10	pF
Logic High Input Voltage	V_{IH}	2.0	-	V
Logic Low Input Voltage	V_{IL}	-	0.8	V
Input Leakage	I_{IL}	-	+-10	µA
Tristate Output Leakage	I_{OL}	-	+-30	µA
I/O Pin Leakage	I_{IOL}	-	+-40	µA
WD6022 ADDRESS BUFFER MODE (MODE = 0)				
OUTPUTS $\overline{\text{PROMCSL}}$, $\overline{\text{PROMCSH}}$, EOT, UCHCMD, PA(2:31)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	-	mA
OUTPUTS $\overline{\text{BE}}$(0:3), M/$\overline{\text{IO}}$*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	-	mA
OUTPUT IOA(0:16)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	8	-	mA
ALL OTHER OUTPUTS*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	24	-	mA

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PARAMETER	SYMBOL	MIN	MAX	UNITS
WD6022 DATA BUFFER MODE (MODE = 1)				
OUTPUTS PD(0:31)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	-	mA
OUTPUTS IOD(0:15)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	-	mA
OUTPUT D(0:31)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	24	-	mA

*The following signals are bi-directional: PA(31:2), $\overline{BE}$(3:0), M/$\overline{IO}$, MADE24, TR32, MM/$\overline{IO}$, $\overline{MBE}$(3:0), A(31:1), $\overline{SBHE}$, PD(31:0), IOD(15:0), and D(31:0).

NOTE
1. The input pin "BIAS" is connected externally to ground through a 1% 1.25 K ohm resistor, and is part of an internal biasing circuit. Capicitance, leakage, and threshold measurements on this pin do not apply.
2. The following signals have internal pullups of 20K: $\overline{BE}$(3:2), $\overline{MBE}$(3:0), MM/$\overline{IO}$, M/$\overline{IO}$.
3. When $\overline{TEST}$ = 0, all outputs and bi-directional signal lines are tristated.

PARAMETER	SYMBOL	MIN	MAX	UNITS
WD6022 ADDRESS BUFFER MODE (MODE = 0)				
$\overline{PROMCSL}$, $\overline{PROMCSH}$, EOT, UCHCMD	CL	50	-	pF
$\overline{BE}$(0:3), M/$\overline{IO}$*	CL	120	-	pF
PA(2:31), IOA(0:16)*	CL	120	-	pF
MADE24, TR32, MM/$\overline{IO}$, $\overline{MMC}$, $\overline{MBE}$(0:3), A(1:31), $\overline{SBHE}$*	CL	240	-	pF
WD6022 DATA BUFFER MODE (MODE = 1)				
PD(0:31), IOD(0:15)*	CL	120	-	pF
D(0:31)*	CL	240	-	pF

3.4 A.C. LOAD SPECIFICATIONS

*The following signals are bi-directional: PA(31:2), $\overline{BE}$(3:0), M/$\overline{IO}$, MADE24, TR32, MM/$\overline{IO}$, $\overline{MBE}$(3:0), A(31:1), $\overline{SBHE}$, PD(31:0), IOD(15:0), and D(31:0).

NOTE
1. The following signals have internal pullups of 20K: $\overline{BE}$(3:2), $\overline{MBE}$(3:0), MM/$\overline{IO}$, M/$\overline{IO}$.

4.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	UNITS
T1	Propagation Delay			ns
	A1, SBHE, MBE(0:3) to BE(0:3)		28	ns
	PA(2:31), to A(2:32)		26	ns
	A(0:31) to PA(2:31), BE(0:3)		26/28	ns
	A20GTX to A20		26	ns
	M/IO to MM/IO		25	ns
	MM/IO to M/IO		25	ns
	TR32, A(0:1), SBHE to MBE(0:3) or		28	ns
	BE(0:3)	-	28	ns
T2	CMD, MMCMD, to UCHCMD	-	20	ns
T3	S(0:1), CMD to EOT	-	25	ns
T4A	M/IO, S(0:1), MADE24, A(0, 31:17)	-	27	ns
	SBHE to PROMCSL, PROMCSH	-	27	ns
T4B	PA(13:17), A20GTX, HLDA, UCHMSTR to	-	54	ns
	PROMCSL, PROMCSH	-	54	ns
T5A	A(0:16), to IOA(0:16)	-	25	ns
T5B	PA(2:16), BE(3:0) to IOA(0:16)	-	50	ns
T6	HLDA to MMC or MADE24	-	25	ns
T7A	Setup to Falling Edge of CMD, MADE24, 5432, M/IO,	10	-	ns
	MM/IO, PA(2:31), BE(0:3), A(0:31), MBE(0:3),	10	-	ns
	SBHE, S(0:1)	10	-	ns
T7B	Setup to Falling Edge of CMD	40	-	ns
	A20GTX, UCHMSTR, HLDA	40	-	ns
T8A	Hold from Falling Edge of MCMD, MADE24, TR32,	10	-	ns
	M/IO, MM/IO, PA(2:31), BE(0:3), A(0:31),	10	-	ns
	MBE(0:3), SBHE, S(0:1)	10	-	ns
T8B	Hold from Falling Edge of CMD	15	-	ns
	A20GTX, UCHMSTR, HLDA	15	-	ns
T9	CMD Inactive Pulse Width	30	-	ns
T10A	Setup to Rising Edge of CMDBUF	10	-	ns
	PA(2:31), BE(0:3), A(0:15)	10	-	ns
T10B	Setup to Rising Edge of CMD	5	-	ns
T11	Hold from Rising Edge of CMDBUF	5	-	ns
	PA (2:31), BE(0:3), A(0:15)	5	-	ns
T12	CMDBUF Inactive Pulse Width	30	-	ns
T13A	Disable - from UCHMSTR	21	-	ns
	A(1:31), MBE(0:3), MM/IO, MADE24,	21	-	ns
	TR32, SBHE, PA(2:31), BE(0:3), M/IO	21	-	ns
T13B	Enable - from UCHMSTR	26	-	ns
	A(1:31), MBE(0:3), MM/IO, MADE24	26	-	ns
	TR32, SBHE, PA(2:31), BE(0:3), M/IO	26	-	ns

Table 3. Address Buffer Mode Timings (ns)

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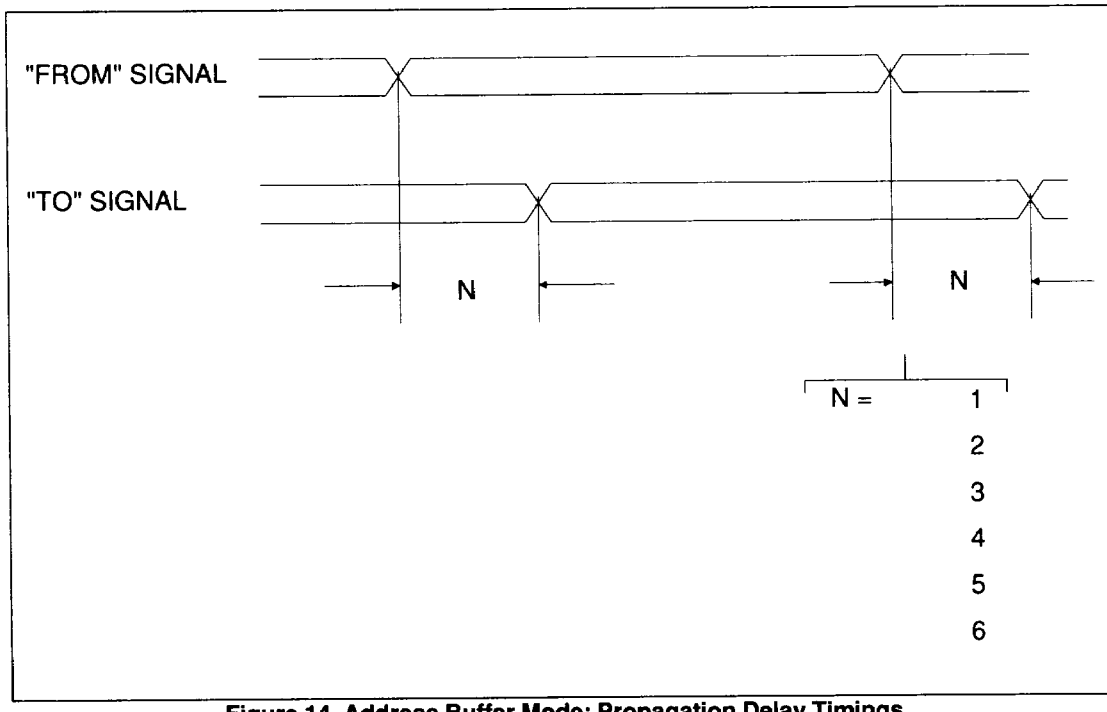


Figure 14. Address Buffer Mode: Propagation Delay Timings

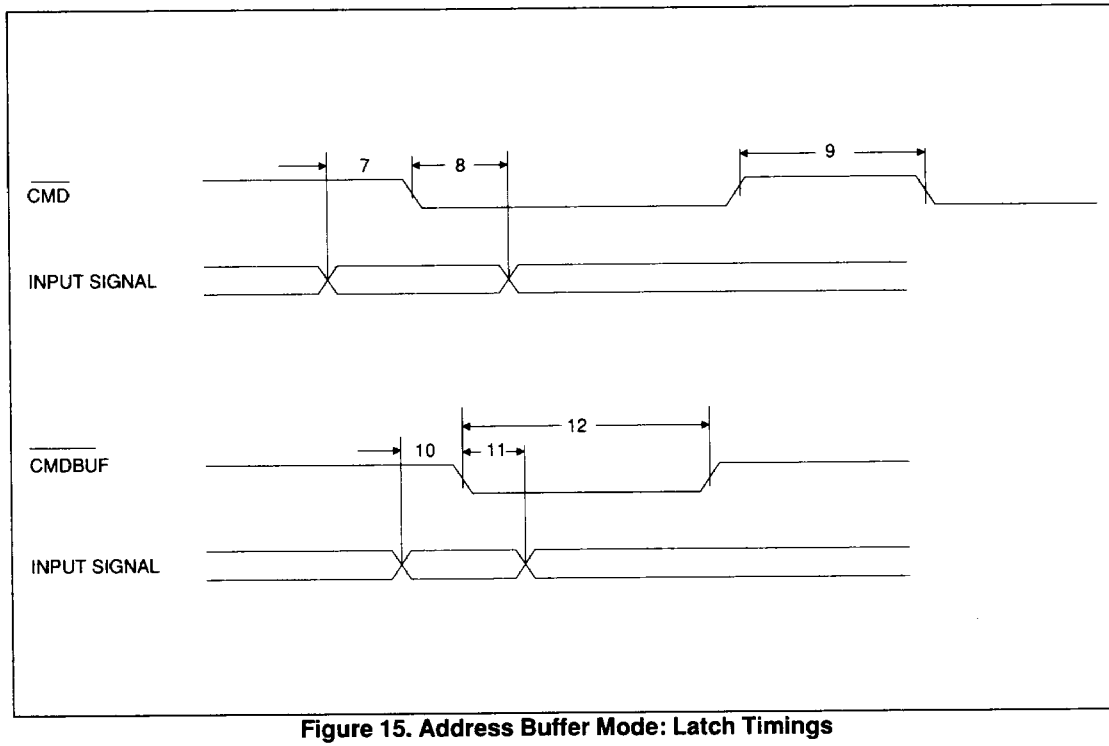


Figure 15. Address Buffer Mode: Latch Timings

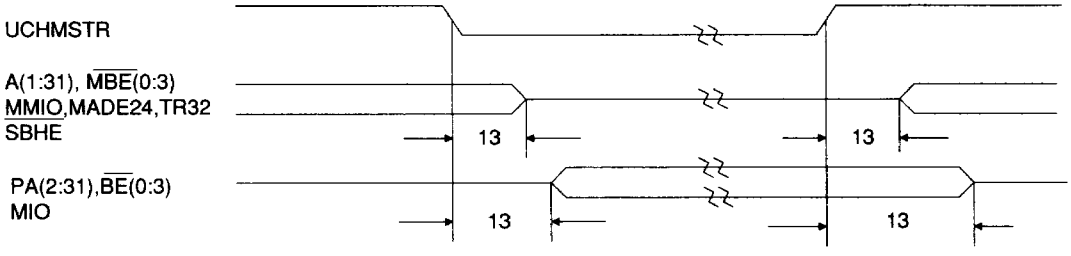


Figure 16. Address Buffer Mode: Float/Enable Timings

PARAM	DESCRIPTION	MIN	MAX	UNITS
T1	Output Enable/Disable	-	-	ns
	$\overline{\text{WREN0}}$ to D(0:7)	-	26	ns
	$\overline{\text{WREN1}}$ to D(8:15)	-	26	ns
	$\overline{\text{WRENH}}$ to D(16:31)	-	26	ns
	$\overline{\text{RDEN}}$ to PD(0:31)	-	28	ns
	$\overline{\text{IODEN}}$ or $\overline{\text{IODTR}}$ to D(0:15) or IOD(0:15)	-	25	ns
T2	Propagation Delay in Transparent Mode	-	-	ns
	PD(0:31) to D(0:31)	-	26	ns
	D(0:31) to PD(0:31)	-	26	ns
T3	Latch Enable to Data	-	-	ns
	$\overline{\text{WRLE}}$ to D(0:31) ($\overline{\text{WRENX}}$ active)	-	15	ns
	$\overline{\text{RDLE0}}$ to PD(0:7) ($\overline{\text{RDENL}}$ active)	-	15	ns
T4A	Data Setup to Latch Enable	-	-	ns
	D(0:7) to $\overline{\text{RDLE0}}$	10	-	ns
	IOD(0:15) to IODCBA	10	-	ns
T4B	Data Setup to Latch Enable	20	-	ns
	PD(0:31) to $\overline{\text{WRLE}}$	20	-	ns
T5	Data Hold from Latch Enable	5	-	ns
	D(0:7) from $\overline{\text{RDLE0}}$	5	-	ns
	IOD(0:15) from IODCBA	5	-	ns
	PD(0:31) from $\overline{\text{WRLE}}$	5	-	ns
T6A	Latch Enable Active Pulse Width	15	-	ns
	$\overline{\text{WRLE}}$, $\overline{\text{RDLE0}}$, IODCBA	15	-	ns
T6B	Latch Enable Active Pulse Width	30	-	ns
	$\overline{\text{WRLE}}$, $\overline{\text{RDLE0}}$, IODCBA	30	-	ns
T7	Propagation Delay	-	-	ns
	SWPDIR to D( ) or PD( )	-	30/28	ns
	$\overline{\text{SWPBYT}}$ to D( ) or PD( )	-	28/28	ns
	$\overline{\text{SWPWORD}}$ to D( ) or PD( )	-	28/28	ns

Table 4. Data Buffer Mode Timings (ns)

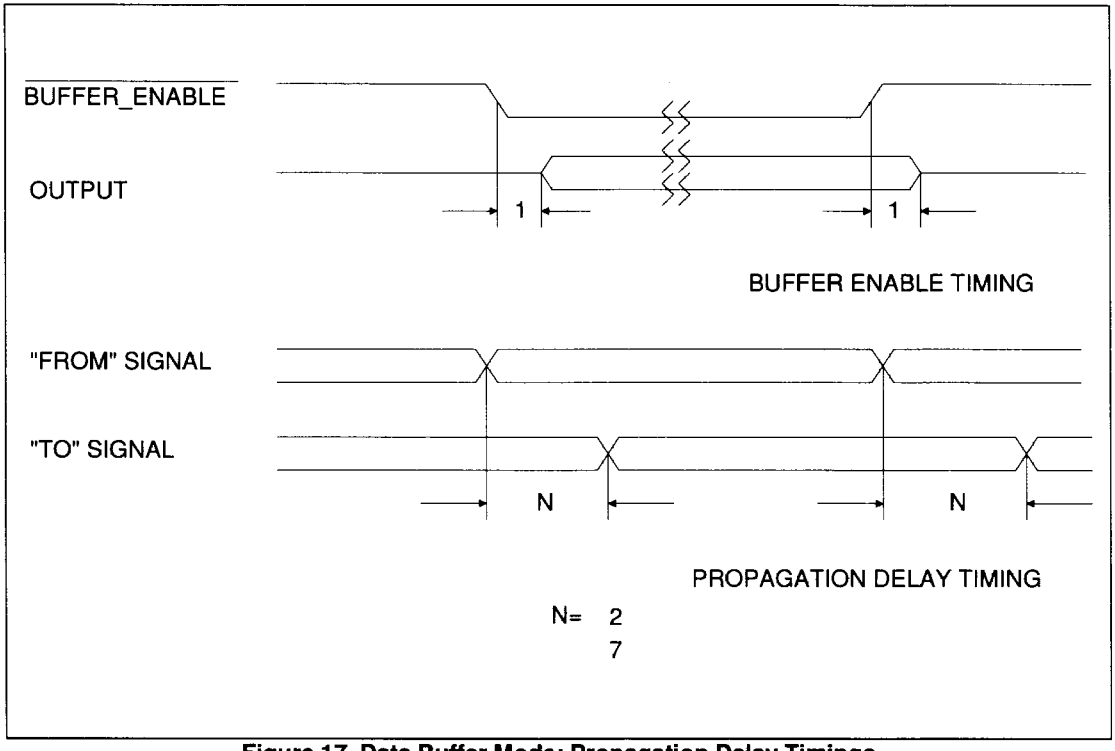


Figure 17. Data Buffer Mode: Propagation Delay Timings

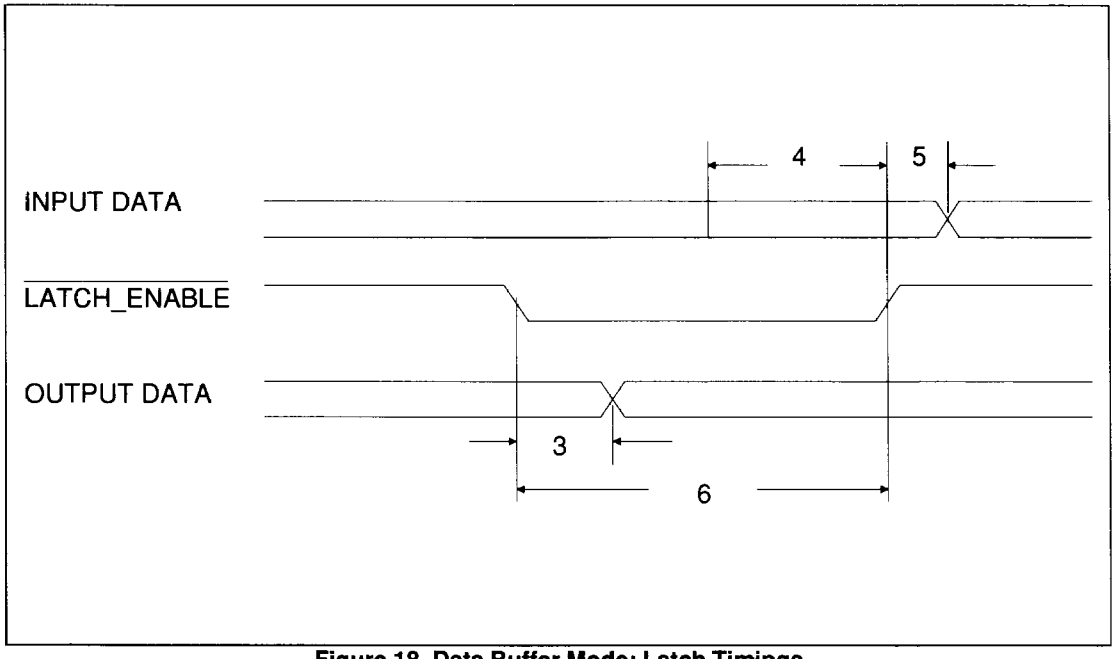


Figure 18. Data Buffer Mode: Latch Timings

14

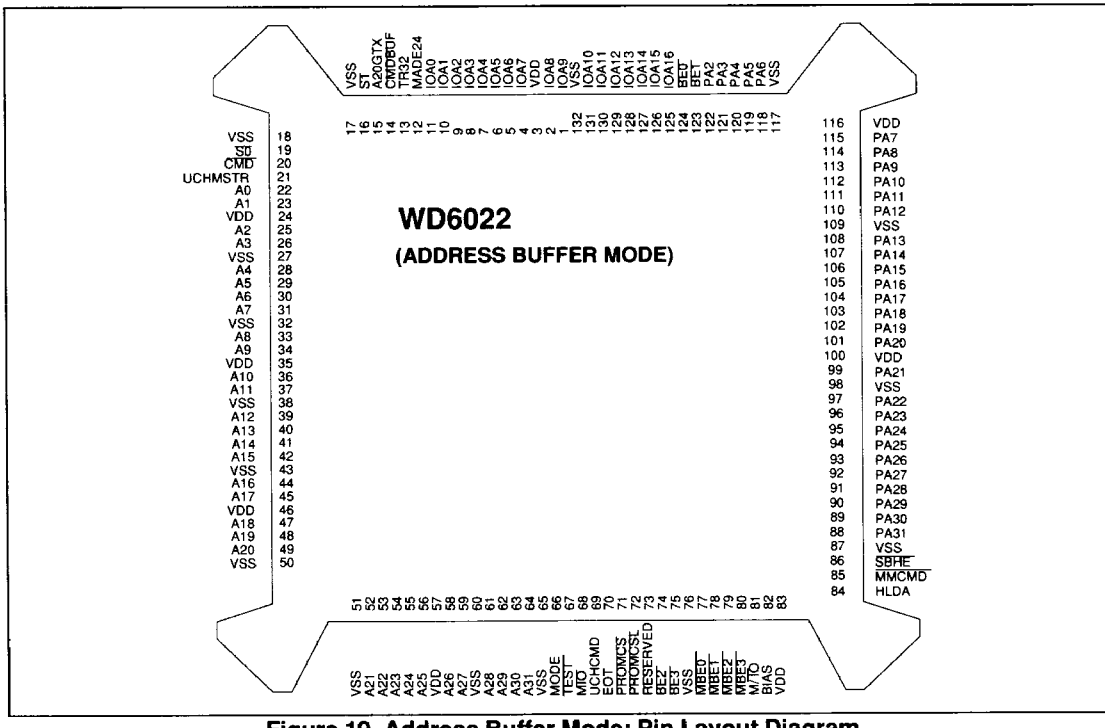


Figure 19. Address Buffer Mode: Pin Layout Diagram

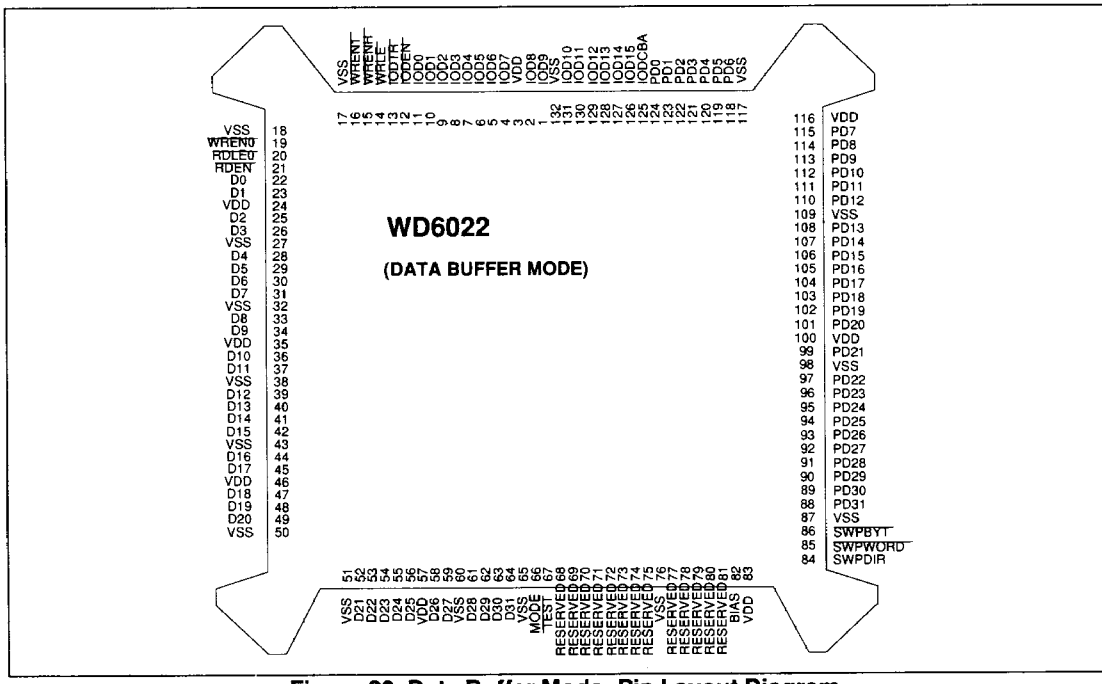


Figure 20. Data Buffer Mode: Pin Layout Diagram

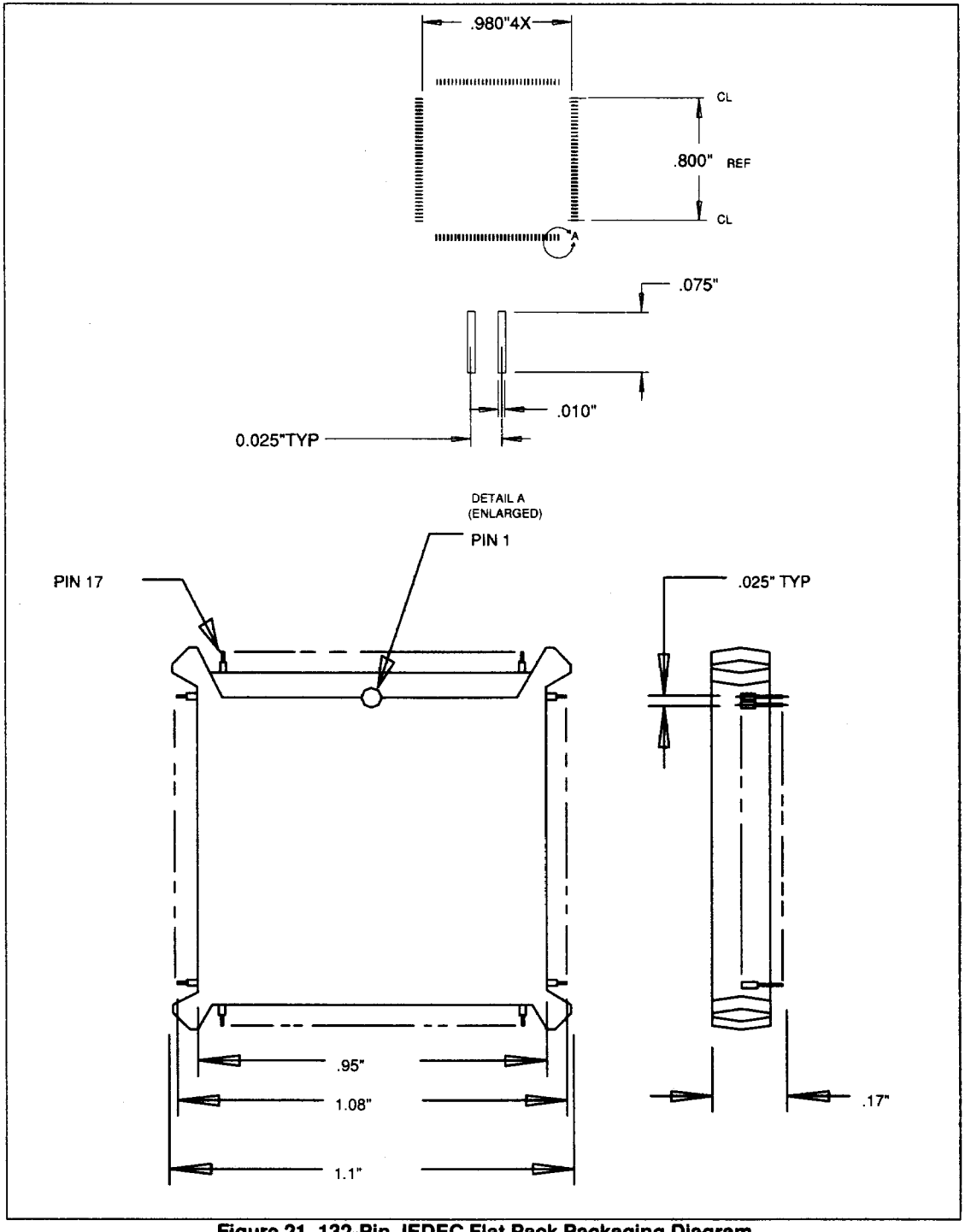
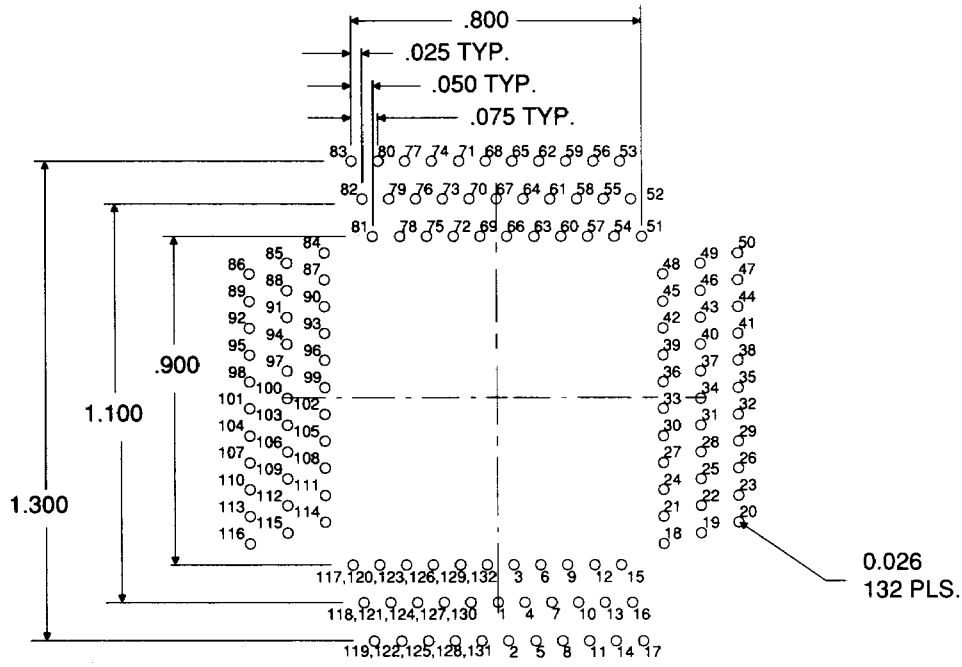


Figure 21. 132-Pin JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

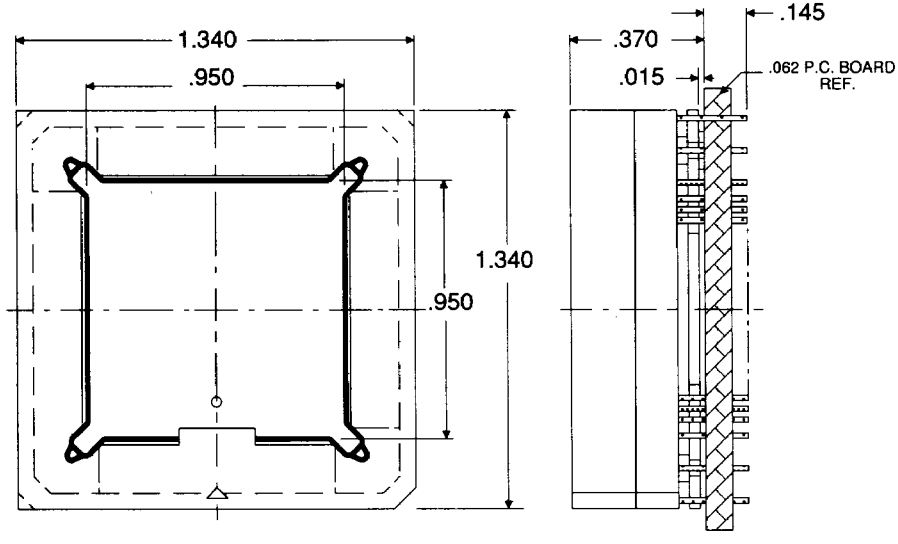


Figure 22. Socket Diagram