1.0 INTRODUCTION

1.1 DESCRIPTION

As part of the Western Digital WD6400SX or WD6400SX/LP Chip Set, the WD6020 Address and Data Buffer Device significantly facilitates the design and implementation of an 80386SX based IBM PS/2 compatible system boards. By combining functionality normally implemented in 10 discrete components, the WD6020 decreases design complexity, saves space, reduces system cost, and increases system reliability. Figure 1-1 shows a typical system diagram using the WD6400 Chip Set.

1.2 FEATURES

- Provides Address and Data Buffers that Interface to the Micro Channel
- Meets Micro Channel AC/DC Specifications
- Contains Peripheral Bus Address and Data Buffers
- Runs in Systems with Clock Speeds to 25 MHz
- 24 Milliamp Output Drive Capability
- Low Power 1.25 Micron CMOS Technology
- Surface Mountable 132 Lead JEDEC Plastic Quad Flat Pack

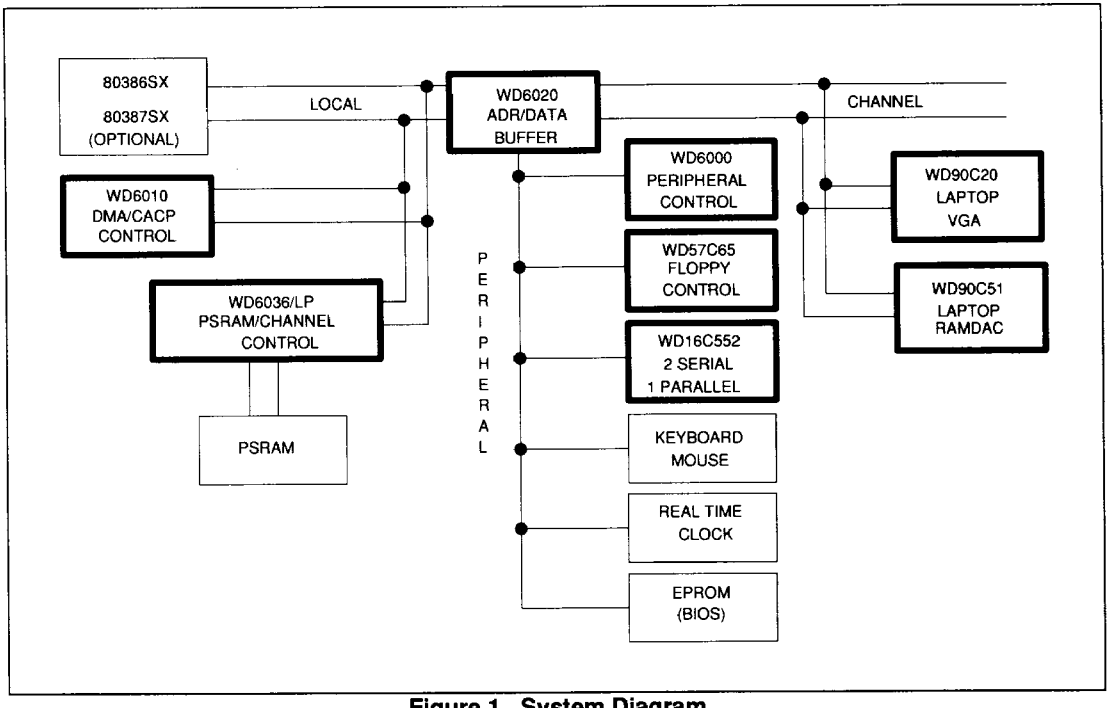

Figure 1. System Diagram

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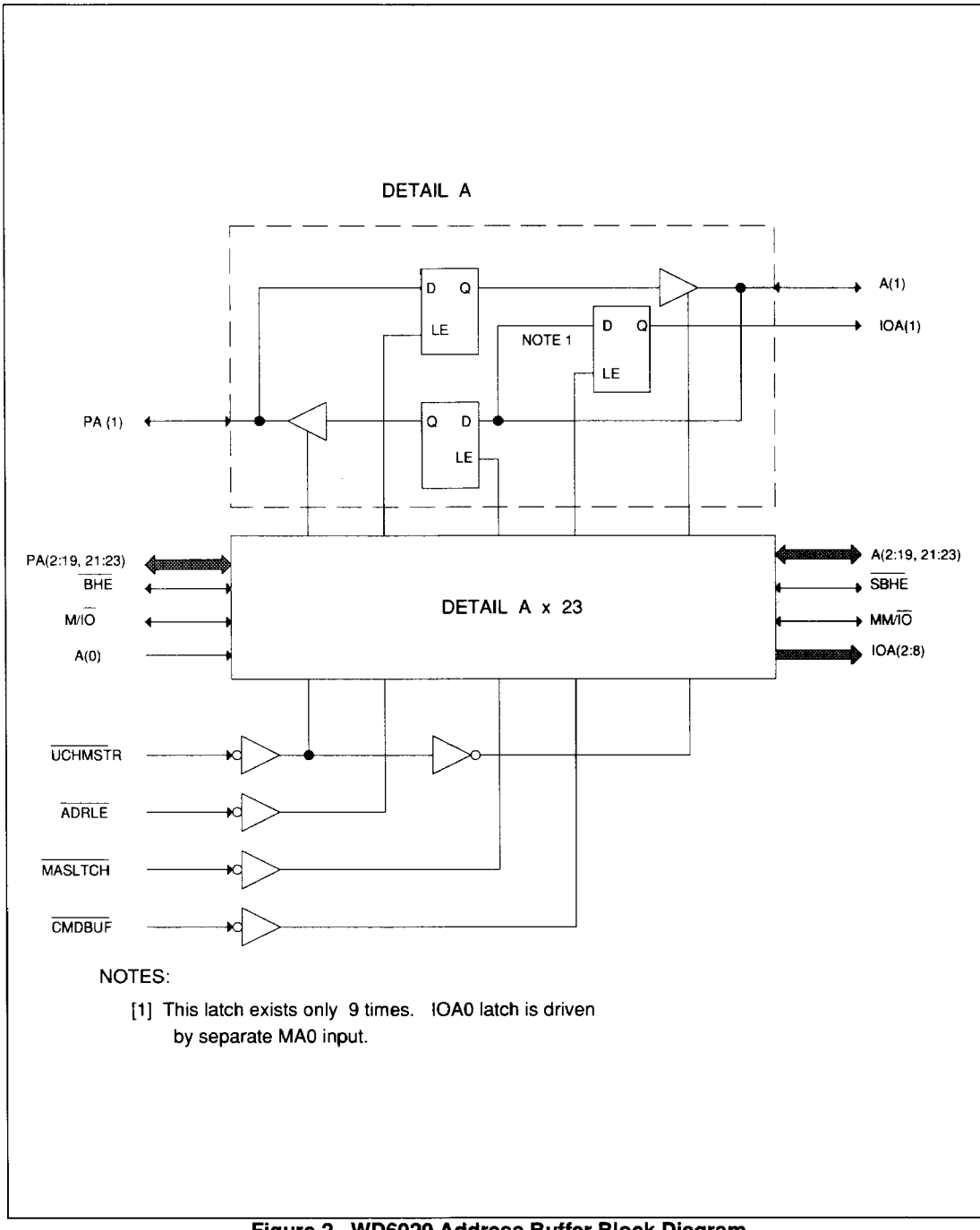


NOTES:

[1] This latch exists only 9 times. IOA0 latch is driven by separate MA0 input.

Figure 2. WD6020 Address Buffer Block Diagram

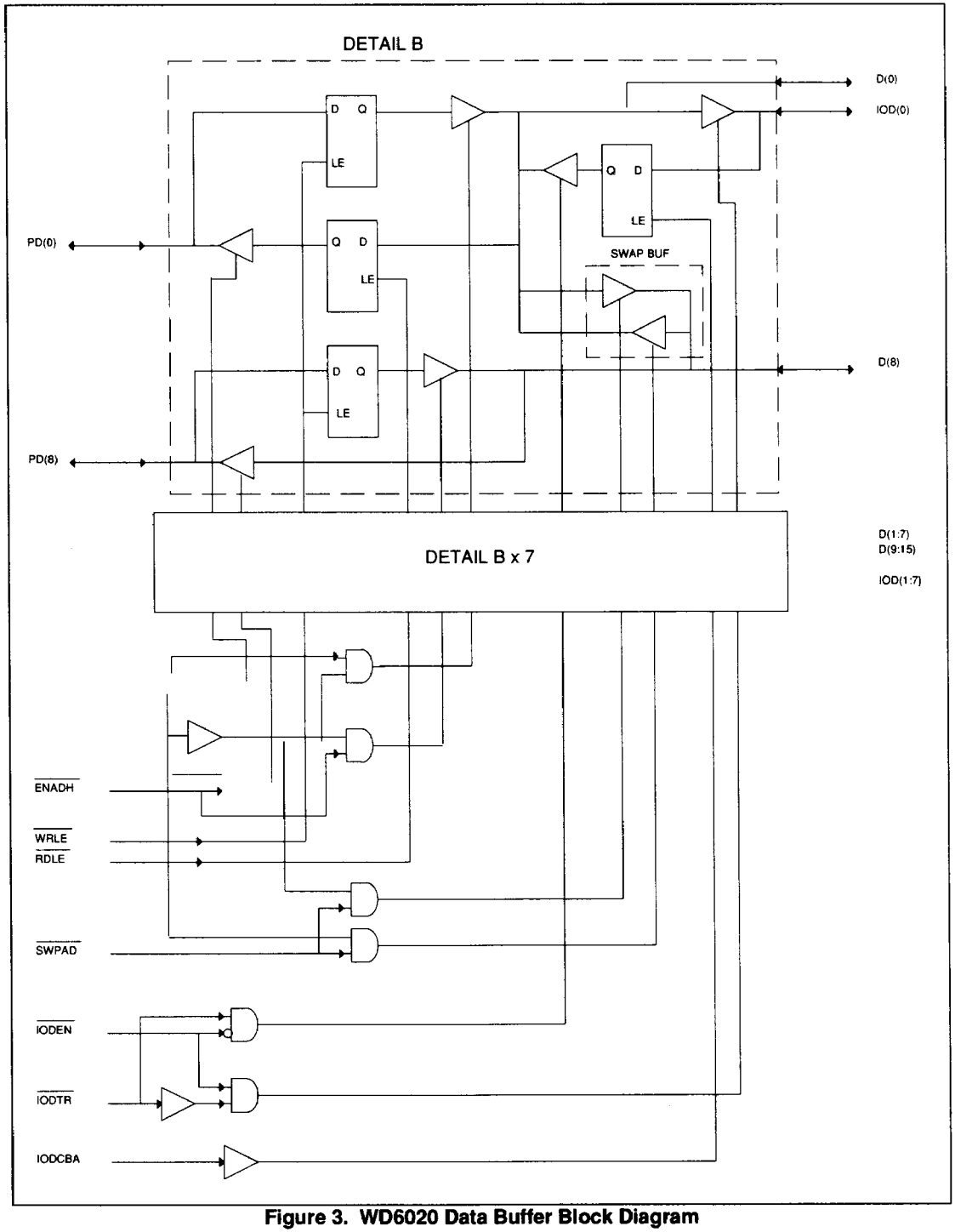
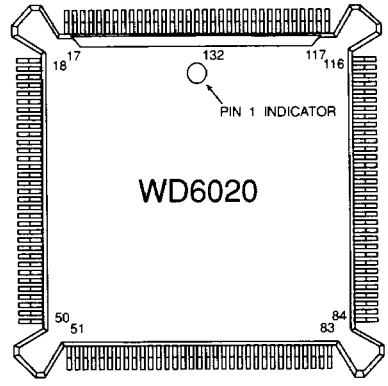


Figure 3. WD6020 Data Buffer Block Diagram



132 Pin JEDEC Flat Pack

Figure 4. Pin Diagram

PIN – NAME	PIN – NAME	PIN – NAME	PIN – NAME
1 – A12	34 – PA16	67 – D6	100 – IOD7
2 – A11	35 – PA17	68 – V_{SS}	101 – IOD6
3 – A10	36 – PA18	69 – D7	102 – IOD5
4 – V_{SS}	37 – PA19	70 – D8	103 – IOD4
5 – A9	38 – PA21	71 – D9	104 – IOD3
6 – A8	39 – PA22	72 – V_{SS}	105 – IOD2
7 – A7	40 – PA23	73 – D10	106 – IOD1
8 – V_{SS}	41 – V_{SS}	74 – D11	107 – IOD0
9 – A6	42 – ENADL	75 – D12	108 – V_{SS}
10 – A5	43 – IODTR	76 – V_{SS}	109 – M/IO
11 – A4	44 – WRLE	77 – D13	110 – BHE
12 – V_{SS}	45 – ADRLE	78 – D14	111 – IOA8
13 – A3	46 – MASLTCH	79 – D15	112 – IOA7
14 – A2	47 – RDLE	80 – BIAS	113 – IOA6
15 – A1	48 – IODCBA	81 – V_{DD}	114 – IOA5
16 – V_{DD}	49 – CMDBUF	82 – PD0	115 – IOA4
17 – PA1	50 – UCHMSTR	83 – PD1	116 – IOA3
18 – PA2	51 – A0	84 – PD2	117 – IOA2
19 – PA3	52 – IODEN	85 – PD3	118 – IOA1
20 – PA4	53 – ENADH	86 – PD4	119 – IOA0
21 – PA5	54 – DTRAD	87 – PD5	120 – A23
22 – PA6	55 – SWPAD	88 – PD6	121 – A22
23 – PA7	56 – V_{DD}	89 – PD7	122 – A21
24 – V_{DD}	57 – MM/IO	90 – PD8	123 – V_{SS}
25 – PA8	58 – SBHE	91 – PD9	124 – A19
26 – PA9	59 – D0	92 – PD10	125 – A18
27 – PA10	60 – V_{SS}	93 – V_{SS}	126 – A17
28 – PA11	61 – D1	94 – PD11	127 – A16
29 – V_{SS}	62 – D2	95 – PD12	128 – V_{SS}
30 – PA12	63 – D3	96 – PD13	129 – A15
31 – PA13	64 – V_{SS}	97 – PD14	130 – A14
32 – PA14	65 – D4	98 – PD15	131 – A13
33 – PA15	66 – D5	99 – V_{DD}	132 – V_{SS}

Table 1. WD6020 Pin Assignments

2.0 PIN DESCRIPTIONS

PIN NO.	NAME	TYPE	FUNCTION
			ADDRESS BUS LATCHES
17 18 19 20 21 22 23 25 26 27 28 30 31 32 33 34 35 36 37 38 29 40	PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15 PA16 PA17 PA18 PA19 PA21 PA22 PA23	I/O	PROCESSOR ADDRESS BUS Bi-directional address bus connected to the 80386SX and the WD6010. A0 and A20 come directly from the WD6010.
51 15 14 13 11 10 9 7 6 5 3 2 1 131 130 129 127 126 125 124 122 121 120	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A21 A22 A23	I/O	CHANNEL ADDRESS BUS Bi-directional Channel address bus.

Table 2. Pin Descriptions

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
110	$\overline{BHE}$	I/O	$\overline{BYTE\ HIGH\ ENABLE}$ This signal is connected to the WD6010 and CPU and indicates whether a high byte is being transferred during the current cycle.
109	M/$\overline{IO}$	I/O	MEMORY $\overline{INPUT/OUTPUT}$ This signal is connected to the WD6010 and CPU and is used to encode the local bus cycle type information.
58	$\overline{SBHE}$	I/O	$\overline{SYSTEM\ BYTE\ HIGH\ ENABLE}$ This signal is connected to the Channel and indicates whether a high byte is being transferred during the current cycle.
57	MM/$\overline{IO}$	I/O	CHANNEL MEMORY INPUT/$\overline{OUTPUT}$ This signal and CHS(0:1) from the WD6010 encode the Channel bus cycle type information.
50	$\overline{UCHMSTR}$	I	$\overline{CHANNEL\ MASTER}$ This signal determines the direction of the address.
49	$\overline{CMDBUF}$	I	$\overline{BUFFERED\ CHANNEL\ COMMAND}$ This signal latches the address for the local bus.
46	$\overline{MASLTCH}$	I	$\overline{MASTER\ LATCH}$ This signal latches the address from the Channel.
45	$\overline{ADRLE}$	I	$\overline{ADDRESS\ LATCH\ ENABLE}$ This signal latches the address to the Channel.
119 118 117 116 115 114 113 112 111	IOA0 IOA1 IOA2 IOA3 IOA4 IOA5 IOA6 IOA7 IOA8	O	I/O ADDRESS BUS These signals are the address bus to the on-board peripherals.
			DATA BUS LATCHES
82 83 84 85 86 87 88 89 90 91 92	PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7 PD8 PD9 PD10	I/O	PROCESSOR DATA BUS Bi-directional data bus connected to the CPU and the WD6010.

Table 2. Pin Descriptions (Contd)

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
94 95 96 97 98	PD11 PD12 PD13 PD14 PD15	I/O	PROCESSOR DATA BUS (contd) Bi-directional data bus connected to the CPU and the WD6010.
59 61 62 63 65 66 67 69 70 71 73 74 75 77 78 79	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	I/O	CHANNEL DATA BUS Bi-directional Channel data bus.
107 106 105 104 103 102 101 100	IOD0 IOD1 IOD2 IOD3 IOD4 IOD5 IOD6 IOD7	I/O	I/O DATA BUS These signals are the peripheral data bus.
55	$\overline{\text{SWPAD}}$	I	$\overline{\text{ENABLE SWAP ADDRESS}}$ This signal enables a byte swap on the Channel.
54	$\overline{\text{DTRAD}}$	I	$\overline{\text{DATA TRANSFER DIRECTION}}$ This signal indicates the direction of the data transfer on the Channel. When asserted low, Channel to CPU is enabled.
53	$\overline{\text{ENADH}}$	I	$\overline{\text{ENABLE DATA HIGH}}$ This signal enables the high byte from the Channel.
52	$\overline{\text{IODEN}}$	I	$\overline{\text{I/O DATA ENABLE}}$ This signal enables the local data bus.
48	IODCBA	I	I/O DATA CLOCK This signal latches the data from the peripheral bus.
47	$\overline{\text{RDLE}}$	I	$\overline{\text{READ LATCH ENABLE}}$ This signal latches Channel low read data.
44	$\overline{\text{WRLE}}$		$\overline{\text{WRITE LATCH ENABLE}}$ This signal latches write data to the Channel.

Table 2. Pin Descriptions (Contd)

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O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
43	$\overline{\text{IODTR}}$	I	I/O DATA TRANSMIT/RECEIVE This signal indicates the direction of the local data bus.
42	$\overline{\text{ENADL}}$	I	ENABLE DATA LOW This signal enables the low byte from the Channel.
			MISCELLANEOUS
80	$\overline{\text{BIAS}}$	I	$\overline{\text{BIAS}}$ This pin provides a bias for internal current drivers. It should be connected through a 1% 1.25K Ohm resistor to ground externally.
16,24,56, 81,99	V_{DD}	I	+5V Power Supply
4,8,12, 29,41,60, 64,68,72, 76,93,108, 123,128, 132	V_{SS}	I	0V Ground

Table 2. Pin Descriptions (Contd)

O = Output, I = Input, I/O = Bidirectional

3.0 TECHNICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

These are absolute maximum stress ratings for the device. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}–V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}–0.3	V_{DD}+0.3	V
Bias on Output Pin	V_{OABS}	VSS–0.3	V_{DD}+0.3	V
Storage Temperature	T_S	–40	125	°C

3.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	–0.3	VDD+0.3	V
Power Dissipation	P_W	—	TBD	mW
Supply Current	I_{DD}	—	TBD	mA

3.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input Capacitance @ f_C= 1 MHz	C_I	—	10	pF
I/O Capacitance	C_{IO}	—	15	pF
*Logic High Input Voltage	V_{IH}	2.0	—	V
*Logic Low Input Voltage	V_{IL}	—	0.8	V
*Input Leakage	I_{IL}	—	±10	uA
Tri-state Output Leakage	I_{OL}	—	±30	uA
I/O Pin Leakage	I_{IOL}	—	±40	uA
OUTPUTS A [23:21], A [19:1], D [15:0], MM/$\overline{IO}$, $\overline{SBHE}$				
Source Current @ V_{OH}= 2.4 V	I_{OH}	4	—	mA
Sink Current @ V_{OL}= 0.4 V	I_{OL}	24	—	mA
ALL OTHER OUTPUTS				
Source Current @ V_{OH}= 2.4 V	I_{OH}	1	—	mA
Sink Current @ V_{OL}= 0.4 V	I_{OL}	4	—	mA

Note: The input pin "BIAS" is connected externally to ground through a 1% 1.25K Ohm resistance and is part of an internal biasing circuit. Capacitance, leakage, and threshold measurements on this pin do not apply.

4.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	PA(21:23,1:19) delay to A(21:23,1:19)	0	25	1
T2	PA(21:23,1:19) delay to A(21:23,1:19)	0	25	1
T3	PA(1:8) delay to IOA(1:8)	0	50	1
T4	PA(1:8) delay to IOA(1:8)	0	50	1
T5	A(0) delay to IOA(0)	0	25	2
T6	A(0) delay to IOA(0)	0	25	2
T7	$\overline{BHE}$, M/$\overline{IO}$ delay to $\overline{SBHE}$, MM/$\overline{IO}$	0	25	1
T8	$\overline{BHE}$, M/$\overline{IO}$ delay to $\overline{SBHE}$, MM/$\overline{IO}$	0	25	1
T9	$\overline{UCHMSTR}$ on to A(21:23,1:19) tristate	0	15	1
T10	$\overline{UCHMSTR}$ off to PA(21:23,1:19) tristate	0	15	1
T11	$\overline{UCHMSTR}$ on to $\overline{SBHE}$, MM/$\overline{IO}$ tristate	0	15	1
T12	$\overline{UCHMSTR}$ off to $\overline{BHE}$, M/$\overline{IO}$ tristate	0	15	1
T13	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ setup to $\overline{ADRLE}$ on	10	—	1
T14	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ hold after $\overline{ADRLE}$ on	5	—	1
T15	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ setup to $\overline{CMDBUF}$ on	10	—	—
T16	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ hold after $\overline{CMDBUF}$ on	5	—	—
T17	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ setup to $\overline{CMDBUF}$ on	10	—	2
T18	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ hold after $\overline{CMDBUF}$ on	5	—	2
T19	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ setup to $\overline{MASLTCH}$ on	10	—	1
T20	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ hold after $\overline{MASLTCH}$ on	5	—	1
T21	A(21:23,1:19) delay to PA(23:21,1:19)	0	25	1
T22	A(21:23,1:19) delay to PA(23:21,1:19)	0	25	1
T23	$\overline{SBHE}$, MM/$\overline{IO}$ delay to $\overline{BHE}$, M/$\overline{IO}$	0	25	1
T24	$\overline{SBHE}$, MM/$\overline{IO}$ delay to $\overline{BHE}$, M/$\overline{IO}$	0	25	1

Table 3. Address Buffer Timing (in nsec)

Notes: 1. Refer to CPU/Channel Address Control Function Table for control states.
2. Refer to Channel/Peripheral Bus Address Control Function Table for control states.

		INPUT	OUTPUT
ADRLE	UCHMSTR	PA(1:23), M/IO, BHE	A(1:25), M/IO, SBHE
0	0	Storing	Tristate
0	1	Transparent	Current Inputs
1	0	Storing	Tristate
1	1	Storing	Previous Inputs
		INPUT	**OUTPUT**
MASLTCH	UCHMSTR	A(1:23), MM/IO, SBHE	PA(1:23), M/IO, BHE
0	0	Transparent	Current Inputs
0	1	Storing	Tristate
1	0	Storing	Previous Inputs
1	1	Storing	Tristate

Table 4. CPU/Channel Address Control Functions

	INPUT	OUTPUT
CMDBUF	A(0:23)	IOA(0:8)
0	X	Previous A(0:23)
1	—	A(0:23)

Table 5. Channel/Peripheral Bus Address Control Functions

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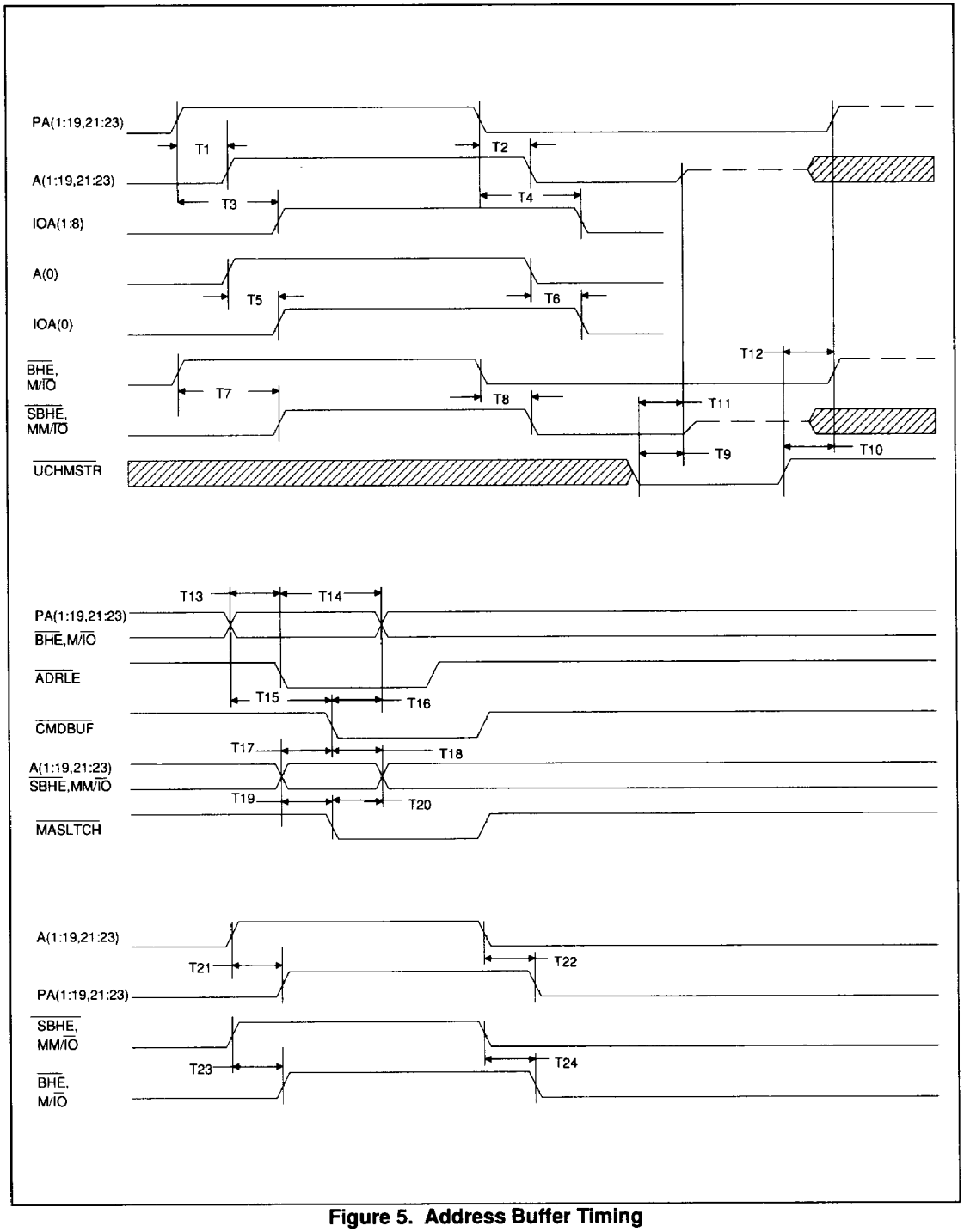

Figure 5. Address Buffer Timing

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	PD(0:15) delay to D(0:15)	0	25	1
T2	PD(0:15) delay to D(0:15)	0	25	1
T3	PD(0:7) delay to IOD(0:7)	0	50	—
T4	PD(0:7) delay to IOD(0:7)	0	50	—
T5	PD(8:15) delay to D(0:7)	0	25	1
T6	PD(8:15) delay to D(0:7)	0	25	1
T7	PD(8:15) delay to IOD(0:7)	0	50	—
T8	PD(8:15) delay to IOD(0:7)	0	50	—
T9	D(0:15) delay to PD(0:15)	0	25	1
T10	D(0:15) delay to PD(0:15)	0	25	1
T11	IOD(0:7) delay to PD(0:7)	0	50	—
T12	IOD(0:7) delay to PD(0:7)	0	50	—
T13	D(0:7) delay to PD(8:15)	0	25	1
T14	D(0:7) delay to PD(8:15)	0	25	1
T15	IOD(0:7) delay to PD(8:15)	0	25	—
T16	IOD(0:7) delay to PD(8:15)	0	25	—
T17	PD(0:15) setup to $\overline{\text{WRLE}}$ high	10	—	1
T18	PD(0:15) hold after $\overline{\text{WRLE}}$ high	5	—	1
T19	D(0:7) setup to $\overline{\text{RDLE}}$ high	10	—	1
T20	D(0:7) hold after $\overline{\text{RDLE}}$ high	5	—	1
T21	IOD(0:7) setup to $\overline{\text{RDLE}}$ high	10	—	—
T22	IOD(0:7) hold after $\overline{\text{RDLE}}$ high	5	—	—
T23	IOD(0:7) setup to IODCBA low	10	—	2
T24	IOD(0:7) hold after IODCBA low	5	—	2
T25	PD(0:7) tristate from $\overline{\text{ENADL}}$ or $\overline{\text{DTRAD}}$	0	15	1
T26	PD(8:15) tristate from $\overline{\text{ENADH}}$ or $\overline{\text{DTRAD}}$ high	0	15	1
T27	D(0:7) tristate from $\overline{\text{ENADL}}$ high	0	15	1
T28	PD(8:15) tristate from $\overline{\text{ENADH}}$ high	0	15	1
T29	D(0:15) tristate from $\overline{\text{DTRAD}}$ high	0	15	1
T30	IOD(0:7) tristate from $\overline{\text{IODDEN}}$ high	0	15	2
T31	IOD(0:7) tristate from $\overline{\text{IODTR}}$ low	0	15	2
T32	D(0:7) tristate from $\overline{\text{SWPAD}}$ or $\overline{\text{DTRAD}}$ high	0	15	1
T33	D(8:15) tristate from $\overline{\text{DTRAD}}$ low	0	15	1
T34	D(8:15) tristate from $\overline{\text{SWPAD}}$ high	0	15	1
T35	D(0:7) tristate from $\overline{\text{IODEN}}$ or $\overline{\text{IODTR}}$ high	0	15	2,3
T36	D(0:7) delay to IOD(0:7)	0	25	2
T37	D(0:7) delay to IOD(0:7)	0	25	2
T38	IOD(0:7) delay to D(0:7)	0	25	2
T39	IOD(0:7) delay to D(0:7)	0	25	2

Table 6. Data Buffer Timing (in nsec)

Notes:
1. Refer to CPU/Chhannel Data Control Function Table for control states.
2. Refer to Channel/Peripheral Bus Data Control Function Table for control status.
3. Data Sourced from IOD bus latch.

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RDLTCH	WRLE	DTRAD	ENADL	ENADH	SWPAD	PD (8:15)	PD (0:7)	D (8:15)	D (0:7)
0	X	0	0	0	1	D(8:15)	D(0:7)	—	—
0	X	0	0	0	0	D(0:7)	D(0:7)	—	—
1	X	0	0	0	1	D(1:15)	Pre-vious D(0:7)	—	—
1	X	0	1	1	1	Tristate	Tristate	—	—
X	0	1	0	0	1	—	—	PD(8:15)	PD(0:7)
X	0	1	0	0	0	—	—	PD(8:15)	PD(0:15)
X	1	1	0	0	1	—	—	Pre-vious D(15:8)	Pre-vious D(7:0)
X	1	1	1	1	1	—	—	Tristate	Tristate

Table 7. CPU/Channel Data Control Functions

IODTR	IODEN	IODCBA	D(0:7)	IOD(0:7)
0	0	0	IOD(0:7)	—
0	0	1	Previous IOD(0:7)	—
X	1	X	Tristate	—
1	0	X	—	D(0:7)
1	1	X	—	Tristate

Table 8. Channel/Peripheral Bus Data Control Functions

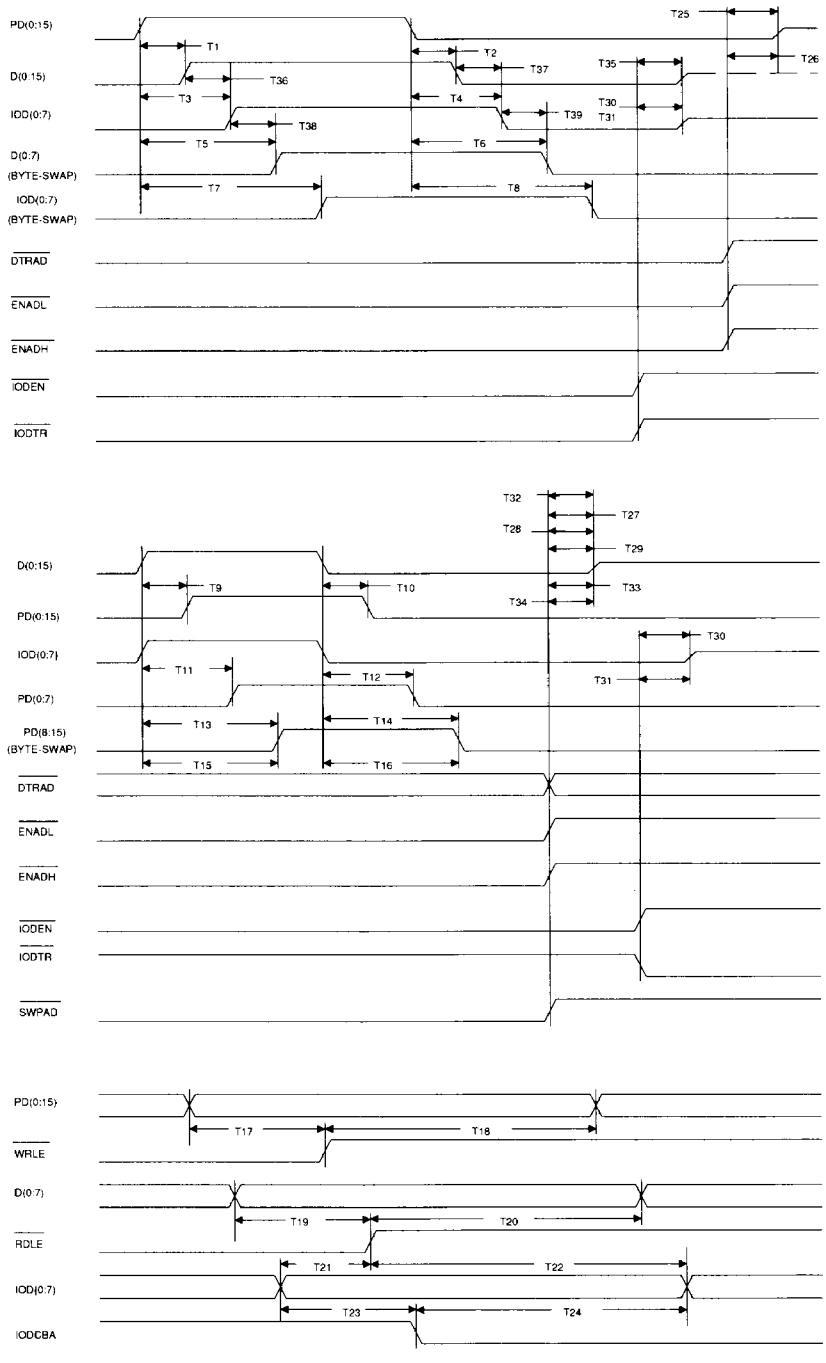

Figure 6. Data Buffer Timing

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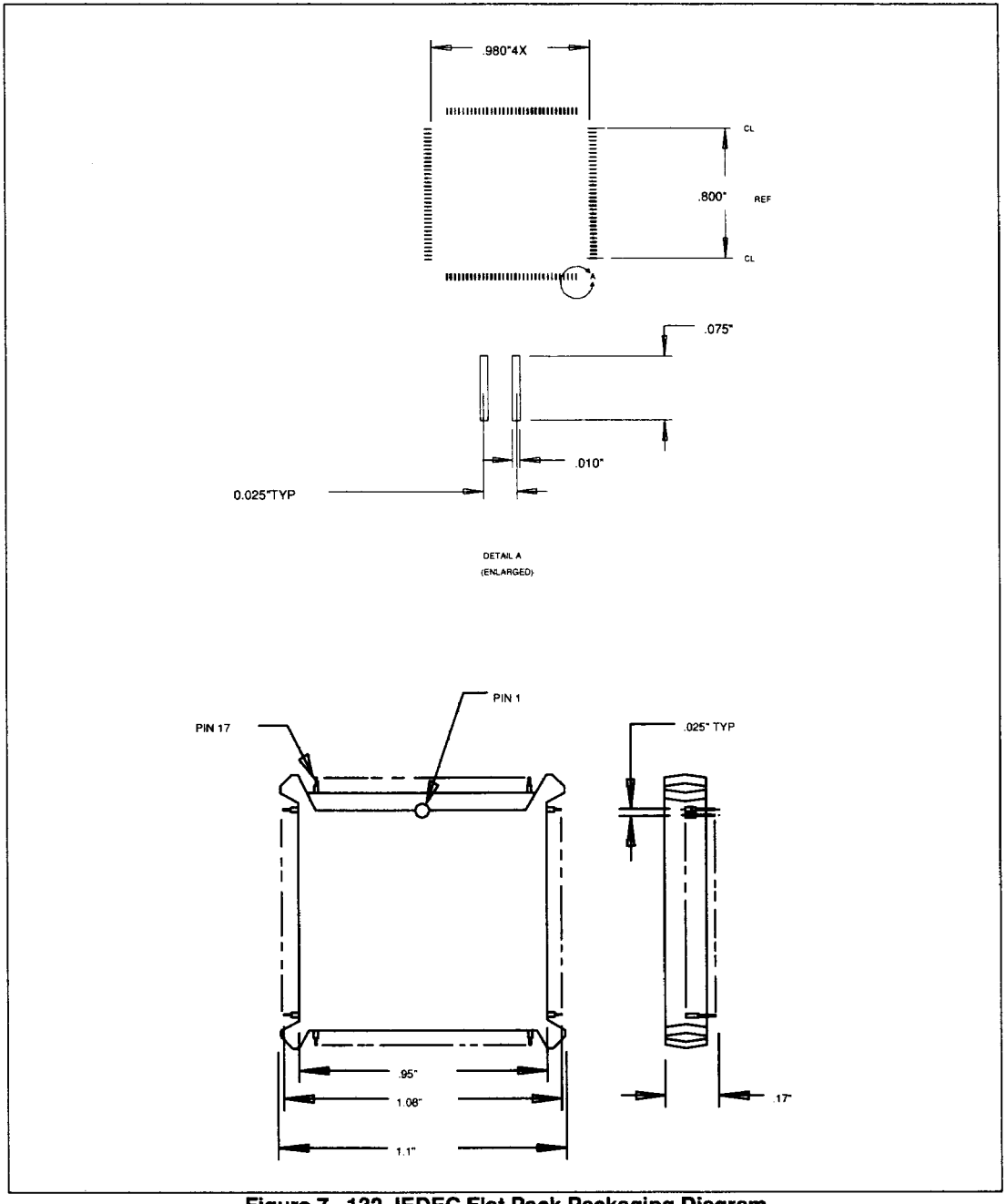
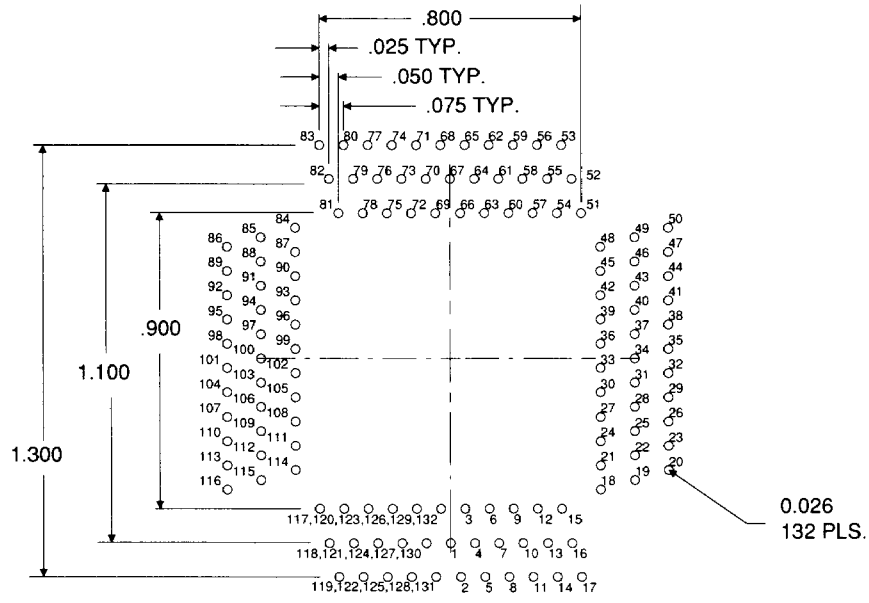


Figure 7. 132 JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-1

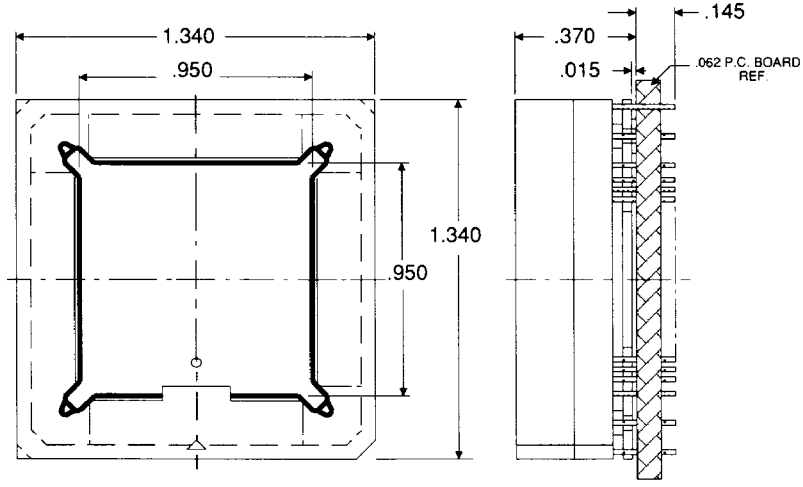


Figure 8. Socket Diagram

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