1.0 INTRODUCTION

1.1 DESCRIPTION

As part of the Western Digital® Micro Channel compatible chip sets (WD6500, WD6400SX, WD6400SX/LP), the WD6000 CPU and Peripheral Control Logic integrated circuit significantly facilitates the design and implementation of system boards compatible with IBM's Micro Channel architecture. It decreases the design complexity and saves space by combining the functions of many discrete arrays and components, while reducing system cost and increasing system reliability.

The Extended Setup Facility (ESF) is a fully compatible enhancement that allows designers to easily configure additional functionality such as a Winchester controller, LAN adapter, or an additional serial port on the system board. This facility can help reduce costs and provide system level product differentiation. Figure 1 shows a typical system diagram using Western Digital's Micro Channel compatible chip sets.

1.2 FEATURES

- Hardware (Register Level) and Software Compatible to the IBM Personal System/2 Micro Channel implementations
- Functionality equivalent to the following:
  - Two 8259 Interrupt Controllers
  - 8254 Timer
  - Watchdog Timer Logic
  - System Board I/O Decode Logic
  - Peripheral Bus Control Generator
  - NMI Generator
  - Error Control Logic
- Interfaces Directly to the Micro Channel
- Operates in an 80486, 80386DX or 80386SX System
- Math Coprocessor Support (80387/80387SX, Weitek 4167/3167 or compatible)
- Programmable Option Select (POS) Logic
- Clock Generation Logic for Math Coprocessor and Keyboard Controller
- Support for External CMOS RAM for storage of Configuration Data
- Extended Setup Facility™ (ESF™)
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

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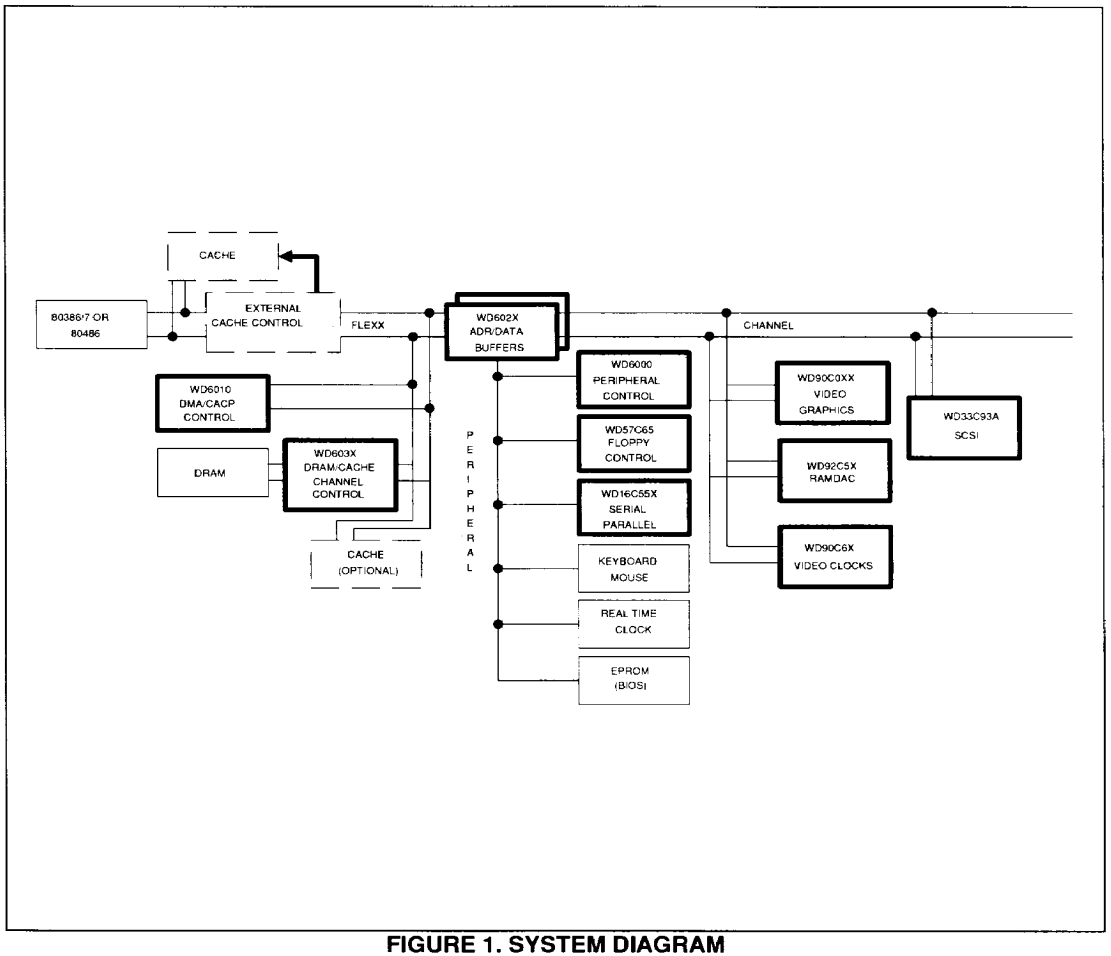

FIGURE 1. SYSTEM DIAGRAM

(DEVICES WITH BOLD OUTLINES AVAILABLE FROM WESTERN DIGITAL CORPORATION)

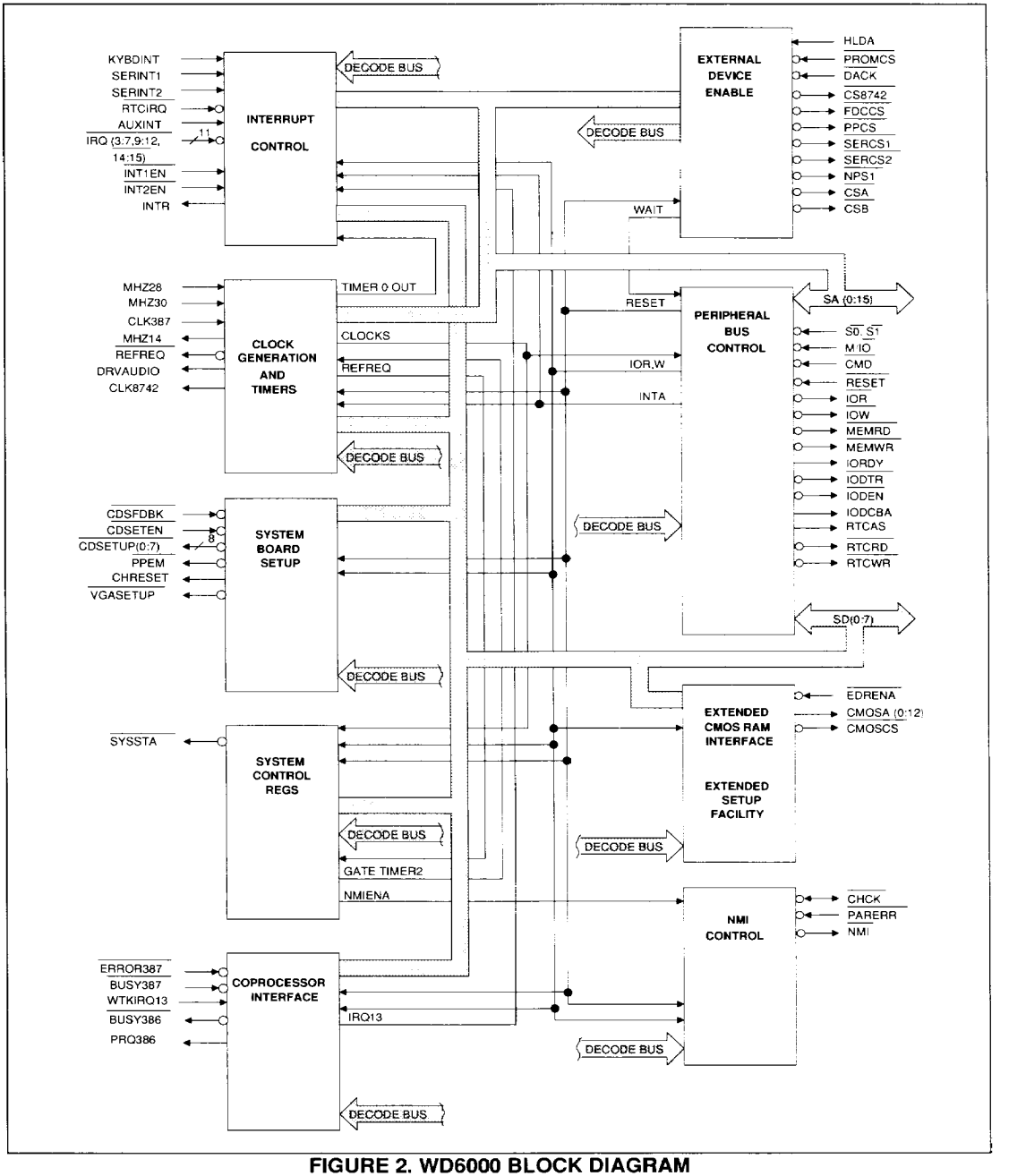

FIGURE 2. WD6000 BLOCK DIAGRAM

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2.0 PIN DESCRIPTION

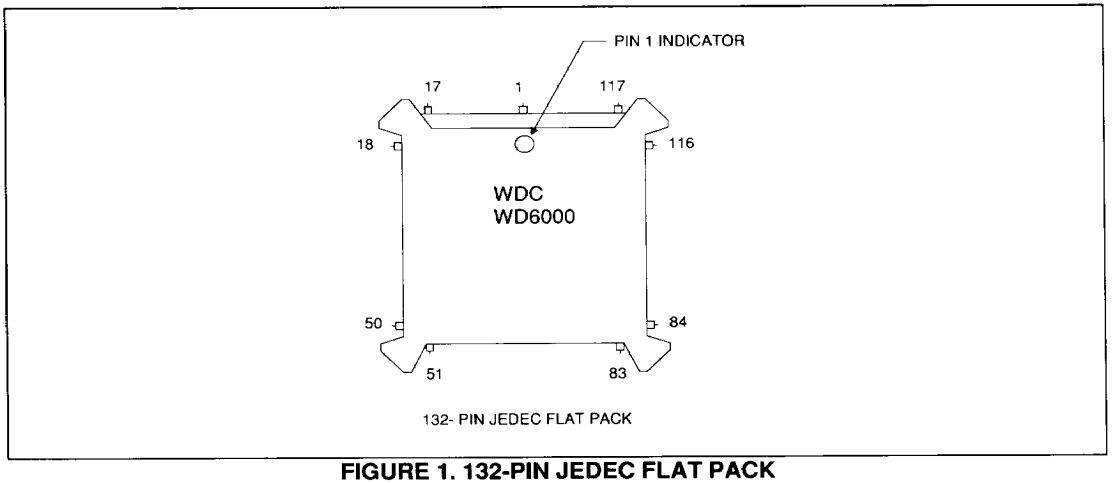

FIGURE 1. 132-PIN JEDEC FLAT PACK

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	SD6	34	SA14	67	TEST	100	RTCWR
2	V_{DD}	35	V_{DD}	68	V_{DD}	101	V_{SS}
3	SD5	36	SA13	69	CMOSA10	102	RTCRD
4	CLK387	37	SA12	70	CMOSA9	103	RTCAS
5	SD4	38	SA11	71	CMOSA8	104	IOW
6	SD3	39	SA10	72	CMOSA7	105	IOR
7	SD2	40	SA9	73	CMOSA6	106	MEMWR
8	WTKIRQ13	41	SA8	74	CMOSA5	107	MEMRD
9	SD1	42	SA7	75	CMOSA4	108	N/C
10	SD0	43	SA6	76	V_{SS}	109	CLK8742
11	V_{SS}	44	SA5	77	CMOSA3	110	IODCBA
12	CHCK	45	SA4	78	CMOSA2	111	IODEN
13	V_{SS}	46	SA3	79	CMOSA1	112	IODTR
14	BUSY387	47	SA2	80	CMOSA0	113	PRQ386
15	ERROR387	48	SA1	81	MHZ14	114	CMOSA12
16	RESET	49	SA0	82	NMI	115	V_{SS}
17	MHZ28	50	V_{SS}	83	DRVAUDIO	116	CMOSA11
18	PARERR	51	IRQ11	84	SYSSTA	117	BUSY386
19	CDSETEN	52	IRQ10	85	CMOSCS	118	CSA
20	MHZ30	53	IRQ9	86	V_{DD}	119	CSB
21	SERINT2	54	RTCIRQ	87	INTR	120	N/C
22	SERINT1	55	IRQ7	88	V_{SS}	121	CDSETUP0
23	INT2EN	56	IRQ6	89	NPS1	122	CDSETUP1
24	INT1EN	57	IRQ5	90	PPCS	123	V_{DD}
25	AUXINT	58	IRQ4	91	SERCS2	124	CDSETUP2
26	DACK	59	IRQ3	92	SERCS1	125	V_{SS}
27	PROMCS	60	KYBDINT	93	FDCCS	126	CDSETUP3
28	HLDA	61	M/IO	94	CS8742	127	CDSETUP4
29	IRQ15	62	CMD	95	PPEM	128	CDSETUP5
30	IRQ14	63	N/C	96	VGASETUP	129	CDSETUP6
31	EDRENA	64	S1	97	IORDY	130	CDSETUP7
32	IRQ12	65	S0	98	REFREQ	131	CHRESET
33	SA15	66	CDSFDBK	99	V_{DD}	132	SD7

PIN NO.	NAME	TYPE	FUNCTION
			INTERRUPT CONTROL
60	KYBDINT	I	KEYBOARD INTERRUPT - Driven by the system keyboard controller.
22	SERINT1	I	SERIAL INTERRUPT 1 - Internally switched with SERINT2 to share IRQ3 and IRQ4 under software control. The Program Control Register (PCR) and Setup Register 0102H are used to assign the serial interrupt signals.
21	SERINT2	I	SERIAL INTERRUPT 2 - Internally switched with SERINT1 to share IRQ3 and IRQ4 under software control. The Program Control Register (PCR) and Setup Register 0102H are used to assign the serial interrupt signals.
54	$\overline{\text{RTCIRQ}}$	I	$\overline{\text{REAL-TIME CLOCK INTERRUPT}}$ - Generated by the system Real-Time Clock module.
25	AUXINT	I	AUXILIARY INTERRUPT - Driven by the system keyboard controller.
59 58 57 56 55 53 52 51 32 30 29	$\overline{\text{IRQ3}}$ $\overline{\text{IRQ4}}$ $\overline{\text{IRQ5}}$ $\overline{\text{IRQ6}}$ $\overline{\text{IRQ7}}$ $\overline{\text{IRQ9}}$ $\overline{\text{IRQ10}}$ $\overline{\text{IRQ11}}$ $\overline{\text{IRQ12}}$ $\overline{\text{IRQ14}}$ $\overline{\text{IRQ15}}$	I	$\overline{\text{INTERRUPT REQUESTS}}$ - Asynchronous inputs that may be shared by other interrupting devices.
24	$\overline{\text{INT1EN}}$	I	$\overline{\text{SERIAL INTERRUPT 1 ENABLE}}$ - System generated programmable output that gates the interrupt signal SERINT1 from the associated serial device. This line must be grounded to enable the interrupt.
23	INT2EN	I	SERIAL INTERRUPT 2 ENABLE - System generated programmable output that gates the interrupt signal SERINT2 from the associated serial device. Line must be grounded to enable the interrupt.
87	INTR	O	INTERRUPT - Drives the system CPU interrupt pin.
			CLOCK GENERATION & TIMERS
17	MHZ28	I	28.636 MHz - Basic clock used for all WD6000 internal functions (timers, wait generator, bus interface logic.

O = Output, I = Inputy, I/O = Bi-directional

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PIN NO.	NAME	TYPE	FUNCTION
CLOCK GENERATION & TIMERS, Continued			
20	MHZ30 (optional)	I	30.0 MHz - Drives the coprocessor and keyboard clock outputs appropriately. See Pin 109 below.
81	MHZ14	O	14.318 MHz - This clock output drives the Channel OSC line.
98	$\overline{\text{REFREQ}}$	O	$\overline{\text{REFRESH REQUEST}}$ - Timer output used to request a refresh cycle by the CACP and DMA controller.
83	DRVAUDIO	O	DRIVE AUDIO - Drives the audio summing network shared by the Channel audio line and Timer 2 OUT gated by Control Port B (0061H) bit 0.
109	CLK8742	O	8742 CLOCK - Drives the keyboard controller. It is derived from the 30 MHz clock input divided by 3 if the MHZ30 clock input is present. If the MHZ30 clock input is connected to the MHZ28 clock, then the keyboard clock (CLK8742), is derived from the MHZ28 clock input divided by 3, and a math coprocessor will not be supported.
4	CLK387	I	For systems using an 80387 or 80387SX, this pin should be connected to the CLK phase of the coprocessor. It is used to synchronize the coprocessor logic to the coprocessor clock. For systems with non-Intel coprocessors, this pin should be left unconnected.
SYSTEM BOARD SETUP			
66	$\overline{\text{CDSFDBK}}$	I	$\overline{\text{CARD SELECTED FEEDBACK}}$ - This Channel signal indicates the addressed slave is present.
19	$\overline{\text{CDSETEN}}$	I	$\overline{\text{CARD SETUP ENABLE}}$ - Timing decode for the 0100H-0107H from the WD6010.
121 122 124 126 127 128 129 130	$\overline{\text{CDSETUP0}}$ $\overline{\text{CDSETUP1}}$ $\overline{\text{CDSETUP2}}$ $\overline{\text{CDSETUP3}}$ $\overline{\text{CDSETUP4}}$ $\overline{\text{CDSETUP5}}$ $\overline{\text{CDSETUP6}}$ $\overline{\text{CDSETUP7}}$	O	$\overline{\text{CARD SETUP}}$ - Each signal drives a Channel slot.
95	$\overline{\text{PPEM}}$	O	$\overline{\text{PARALLEL PORT EXTENDED MODE}}$ - When asserted, this signal puts the parallel port into Extended (bidirectional) Mode.
131	CHRESET	O	CHANNEL RESET - This software-generated signal resets all Channel resident adapters and system board I/O devices only. Located in register 0096H Bit 7.
96	$\overline{\text{VGASETUP}}$	O	$\overline{\text{VGA SETUP}}$ - Tells the VGA device to enter Setup Mode.

O = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
			SYSTEM CONTROL REGISTERS
84	$\overline{\text{SYSSTA}}$	O	$\overline{\text{SYSTEM STATUS}}$ - This signal is used to drive a hard disk active LED.
			COPROCESSOR INTERFACE
15	$\overline{\text{ERROR387}}$	I	$\overline{\text{ERROR 387}}$ - Driven by the coprocessor, this signal indicates the coprocessor has encountered an error condition which causes an interrupt (13H) to be issued and holds the $\overline{\text{BUSY386}}$ signal in the busy state. The busy and interrupt are cleared by issuing an 8-bit I/O write command to location 00F0H with data equal to 00H. For 80387/80387SX-based systems, this pin should be connected to the $\overline{\text{ERROR}}$ pin.
14	$\overline{\text{BUSY387}}$	I	$\overline{\text{BUSY 387}}$ - Driven by the coprocessor, this signal indicates the coprocessor is currently executing a command. This can also be used on 80386SX/80387SX-based systems.
117	$\overline{\text{BUSY386}}$	O	$\overline{\text{BUSY 386}}$ - Indicates the coprocessor is currently executing a command.
8	WTKIRQ13	I	For systems implementing a Weitek 4167/3167 (or compatible) math coprocessor, this pin should be connected to the IRQ13 pin of the EMC (Extended Math Coprocessor) socket. It is used to generate an interrupt 13 to the system when the Weitek coprocessor requires service.
			This pin has dual functions. At power up (trailing edge of RESET), the state of this pin is latched to determine whether the WD6000 will implement an 80386 or 80386SX-compatible math interface.
			For an 80386/80386SX/80486 system, this pin should be pulled down with a 100 ohm resistor.
			For an 80386/80386SX/80486 system which includes a Weitek (or compatible) coprocessor, this pin should be connected to the IRQ13 pin of the Weitek device.
113	PRQ386	O	The PRQ386 signal is OR'ed with the coprocessor request (PEREQ) to drive the PRQ386 signal to the CPU high to allow the coprocessor to complete any pending data transfers.
			EXTERNAL DEVICE ENABLE
28	HLDA	I	BUS HOLD ACKNOWLEDGE - This line indicates when the CPU has given the system local bus to another master (Channel bus master or DMA controller). It is used to prevent non-system CPU access to locations 0000-00FFH in the WD6000 during master cycles.

O = Output, I = Input, I/O = Bi-directional

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PIN NO.	NAME	TYPE	FUNCTION
			EXTERNAL DEVICE ENABLE, Continued
27	$\overline{\text{PROMCS}}$	I	$\overline{\text{PROM CHIP SELECT}}$ - This signal indicates an access to a PROM location and is activated on read accesses to the PROM address spaces E0000 - FFFFFH, FE0000 - FFFFFFH (80386SX systems), or FFFE0000 - FFFFFFFFH (80386 systems). This line is used by the Wait/Ready in the WD6030 logic to control the length of the channel cycle for PROM accesses.
26	$\overline{\text{DACK}}$	I	$\overline{\text{FLOPPY DMA ACKNOWLDGE}}$ - This pin is activated on a DMA Transfer to the floppy disk. It is used by the Wait/Ready logic in the WD6030 to control the length of the channel cycle for the floppy DMA.
94	$\overline{\text{CS8742}}$	O	$\overline{\text{CHIP SELECT 8742}}$ - This signal is the chip select to the keyboard/auxiliary device controller.
93	$\overline{\text{FDCCS}}$	O	$\overline{\text{FLOPPY DISK CONTROLLER CHIP SELECT}}$ - This signal is the chip select to the floppy disk controller.
90	$\overline{\text{PPCS}}$	O	$\overline{\text{PARALLEL PORT CHIP SELECT}}$ - This signal is the chip select to the parallel port controller.
92	$\overline{\text{SERCS1}}$	O	$\overline{\text{SERIAL CHIP SELECT 1}}$ - This signal is the chip select for the first serial port controller.
91	$\overline{\text{SERCS2}}$	O	$\overline{\text{SERIAL CHIP SELECT 2}}$ - This signal is the chip select for the second serial port controller.
89	$\overline{\text{NPS1}}$	O	$\overline{\text{NUMERIC PROCESSOR SELECT}}$ - This signal is the chip select for the math coprocessor.
118	$\overline{\text{CSA}}$	O	$\overline{\text{CHIP SELECT A}}$ - This signal is a software-programmable chip select.
119	$\overline{\text{CSB}}$	O	$\overline{\text{CHIP SELECT B}}$ - This signal is a software-programmable chip select.
			PERIPHERAL BUS CONTROL
10 9 7 6 5 3 1 132	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	I/O	SYSTEM DATA - Theses bi-directional lines are the low byte of data from the Channel data bus (buffered).

IO = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
			PERIPHERAL BUS CONTROL, Continued
49 48 47 46 45 44 43 42 41 40 39 38 37 36 34 33	SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15	I	SYSTEM ADDRESS - These 16 address lines are used to decode the appropriate locations of the system CPU 64K I/O space. These lines should be connected to the channel address bus (0...15).
65 64 61	$\overline{S0}$ $\overline{S1}$ M/$\overline{IO}$	I	$\overline{CHANNEL\ STATUS}$ and MEMORY $\overline{I/O}$ - These three lines encode information on the type of Channel bus cycle.
62	$\overline{CMD}$	I	$\overline{COMMAND}$ - This signal defines when data to or from the Channel is valid.
16	$\overline{RESET}$	I	$\overline{RESET}$ - This signal initializes all the internal logic to a power-on state.
105 104 107 106	$\overline{IOR}$ $\overline{IOW}$ $\overline{MEMRD}$ $\overline{MEMWR}$	O	$\overline{I/O\ READ}$, $\overline{I/O\ WRITE}$, $\overline{MEMORY\ READ}$ and $\overline{MEMORY\ WRITE}$ - These signals comprise the command information for peripheral bus cycles and track the Channel cycle.
97	IORDY	O	I/O READY - This signal indicates the WD6000 is finished with the current bus cycle. It is deactivated to extend the current Channel cycle.
112 111 110	$\overline{IODTR}$ $\overline{IODEN}$ IODCBA	O O O	$\overline{I/O\ DATA\ TRANSMIT/RECEIVE}$, $\overline{I/O\ DATA\ ENABLE}$, I/O DATA CLOCK (latches when clock is low) - These three lines control the address and data buffer latches for the peripheral bus. The I/O data transmit/receive signal controls the direction of the I/O data buffers inside the WD6022. If $\overline{IODTR}$ is low, the WD6022 drives data from IOD (0:15) to D (0:15), and if $\overline{IODTR}$ is high, the WD6022 drives data from D (0:15) to IOD (0:15). $\overline{IODEN}$ enables the I/O data buffers. When active, the WD6022 drives either the D (0:15) to $\overline{IOD}$ (0:15), depending on the direction set by $\overline{IODTR}$. The I/O data clock (IODCBA) is used to latch the data during reads from the Channel peripherals on the I/O bus.

IO = Output, I = Input, I/O = Bi-directional

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PIN NO.	NAME	TYPE	FUNCTION
			PERIPHERAL BUS CONTROL, Continued
103	RTCAS	O	REAL-TIME CLOCK ADDRESS SELECT - This signal latches the address into the Real-Time Clock module.
102 100	$\overline{\text{RTCRD}}$ $\overline{\text{RTCWR}}$	O	$\overline{\text{REAL-TIME CLOCK READ/WRITE}}$ - These two lines are the command lines to the Real-Time Clock module.
			EXTENDED CMOS RAM INTERFACE
31	$\overline{\text{EDRENA}}$	I	$\overline{\text{ESF DATA REGISTER PORT ENABLE}}$ - This signal from the WD6010 indicates that the ESF Data Register is being read or written to.
80 79 78 77 75 74 73 72 71 70 69 116 114	CMOSA0 CMOSA1 CMOSA2 CMOSA3 CMOSA4 CMOSA5 CMOSA6 CMOSA7 CMOSA8 CMOSA9 CMOSA10 CMOSA11 CMOSA12	O	CMOS ADDRESS - These 13 lines are used to address the Extended CMOS RAM.
85	$\overline{\text{CMOSCS}}$	O	$\overline{\text{CMOS CHIP SELECT}}$ - This line is used to select the Extended CMOS RAM.
			NMI CONTROL
12	$\overline{\text{CHCK}}$	I/O	$\overline{\text{CHANNEL CHECK}}$ - This signal is the channel error indication. It is driven by bus resident adapters. During a bus master DRAM cycle, the system board drives this line if a parity error occurs. When this signal is an output, it is an open collector output.
18	$\overline{\text{PARERR}}$	I	$\overline{\text{PARITY ERROR}}$ - This signal is the output of the DRAM controller parity generator.
82	$\overline{\text{NMI}}$	O	$\overline{\text{NON-MASKABLE INTERRUPT}}$ - When driven by the WD6010 to the CPU, $\overline{\text{NMI}}$ indicates the CACP has reached a bus timeout condition while monitoring the bus. When the signal is received by the WD6010 fromn the WD6000, it instructs the CACP in the WD6010 to initiate an arbitration cycle to remove any bus masters so the the CPU can service the interrupt.

IO = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
		MISCELLANEOUS	
2,35,68, 86,99,123	V_{DD}	I	+5 Power Supply
11,13,50, 76,88,101 115,125	V_{SS}	I	0 V Ground
63,108, 120	N/C	-	Not Connected
67	$\overline{TEST}$	I	$\overline{TEST}$ PIN - This is an active low pin that facilitates board-level testing. When low, this signal tri-states all outputs and bi-directional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bi-directional lines are enabled by the chip.

IO = Output, I = Input, I/O = Bi-directional

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The WD6500 and WD6400SX I/O map is shown in Table 1.

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	WD6010	DMA Controller, Channels 0-3 [1]
0018H	WD6010	Extended Function Register [1]
001AH	WD6010	Extended Function Execute [1]
0020 to 0021H	WD6000I	Interrupt Controller 1 (Master)
0040, 0042-0044, 0047H	WD6000	System Timers
0060H	WD6000	Keyboard Data Port
0061H	WD6000	System Control Port B
0064H	WD6000	RD=Kybd status, WR=Kybd command
0070H	WD6000	RTC/CMOS Addr. Register, NMI Mask
0071H	WD6000	RTC/CMOS Data Port
0074H	WD6000	EAR0 Extended CMOS RAM, ESF
0075H	WD6000	EAR1 Extended CMOS RAM
0076H	WD6000	Extended CMOS RAM data port
0081 to 0083, 0087H	WD6010	DMA Page Registers (0-3)[1]
0089 to 008B, 008FH	WD6010	DMA Page Registers (4-7)[1]
0090H	WD6010	Central Arbitration Control Point [1]
0091H	WD6000	Card Selected Feedback
0092H	WD6000	System Control Port A
0094H	WD6000	System Board Setup
0096, 0097H	WD6000	POS, Channel Connector Select
00A0 to 00A1H	WD6000	Interrupt Controller 2 (Slave)
00C0 to 00DFH	WD6010	DMA Controller (4 to 7)[1]
00F0H	WD6000	Coprocessor Clear Busy
00F1H	WD6000	Coprocessor Reset
00F8 to 00FFH	WD6000	Coprocessor
0100, 0101H	WD6000	System ID
0102 to 0107H	WD6000	System Board Configuration (POS)
0278 to 027BH	WD6000	Parallel Port 3
02F8 to 02FFH	WD6000	Alternate Serial Port
0378 to 037BH	WD6000	Parallel Port 2
03BC to 03BFH	WD6000	Parallel Port 1
03B4, 03B5, 03BA, 03C0-03C5H	VIDEO	Video Subsystem [2]
03CE, 03CF, 03D4, 03D5, 03DAH	VIDEO	Video Subsystem [2]
03C6 to 03C9H	VIDEO	Video DAC [2]
03F0 to 03F7H	WD6000	Diskette Drive Controller
03F8 to 03FFH	WD6000	Primary Serial Port
0700H	WD6010	ESF Data Register (Default)

[1] No Channel cycle is generated on these I/O addresses
[2] I/O location 03C3H (VGA Enable Register) is in WD6010.

TABLE 1. SYSTEM LEVEL I/O MAP

3.0 INTERRUPT CONTROLLER

The Interrupt Controller is functionally equivalent to two Intel 8259 controllers cascaded together. It operates in level-sensitive mode and controls sixteen levels of interrupts, five interna,l and eleven system interrupts. Interrupt Controller 1 is the master controller, located at I/O space 0020H and 0021H. Interrupt Controller 2 is the slave and is located at I/O space 00a0H and 00A1H. Interrupt Request 2 (IRQ2) from Interrupt Controller 1 is used to cascade the two controllers, as illustrated in Figure 4.

The edge trigger mode is not available. Any or all of the interrupts may be masked. The non-maskable interrupt may be masked by setting Register (0070H) Bit 7.

Interrupts may be shared by more than one hardware interrupt. Table 2 shows the interrupt assignments in a typical system environment.

The auxiliary and serial port interrupt signals are discussed below:

- AUXINT is the interrupt from the auxiliary device. It is an active high input that is ORed with IRQ12 from the Channel. It is treated exactly like an IRQ12 interrupt.
- SERINT1 is an active high interrupt from Serial Port 1 (SP1). SERINT1 is masked by $\overline{\text{INT1EN}}$, which must be low in order to detect SERINT1. SERINT1 is ORed with IRQ3 or IRQ4, depending on the programming. If SP1 is enabled (See Section 4.0), and it is programmed to Alternate Addresses 02F8 - 02FFH, SERINT 1 is treated as IRQ3. It is treated as IRQ4 when SP1 is programmed to Primary Addresses 03F8 - 03FFH.
- SERINT2 is an active high interrupt from Serial Port 2 (SP2). SERINT2 is masked by $\overline{\text{INT2EN}}$, which must be low in order to detect SERINT2. SERINT2 is ORed with IRQ3 or IRQ4, depending on the programming. If SP2 is enabled (See Section 9.2.3), and it is programmed to Primary Addresses 03F8 - 03FFH, SERINT2 is treated as IRQ4. It is treated as IRQ3 when SP2 is programmed to Alternate Addresses 02F8 - 02FFH.

3.1 INTERRUPT CONTROLLER OPERATION

Figure 5 contains a functional diagram of an interrupt controller in the WD6000, providing an operational representation of how each controller works. The various interrupt controller functions are described below.

3.1.1 Interrupt Request Register (IRR) and In-Service Register (ISR)

Interrupts are handled by the IRR and the ISR. The IRR stores all the interrupt levels that are being serviced.

3.1.2 Priority Resolver

This function decodes the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA cycle.

3.1.3 Interrupt Mask Register

The IMR stores the bits that mask selected interrupt lines. Masking a higher priority input does not affect lower priority interrupt request lines.

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3.1.4 Read/Write Control Logic

This function accepts commands from the CPU and allows the status of the Interrupt Controller to be read on the Data Bus. It contains the Initialization Command Word (ICW) and Operation Command Word (OCW) registers, that store the various control formats for device operation.

3.1.5 Cascade Buffer/Comparator

This function stores and compares the ID of the slave controller. In the WD6000 Interrupt Controller configuration, the CAS bus is an output from the master and an input to the slave. When a slave request line is activated and acknowledged, the master sends the ID of the slave, fixed at 2, to the CAS bus. This enables the slave to send its pre-programmed subroutine address to the data bus during the second INTA cycle. All handshaking is handled internally.

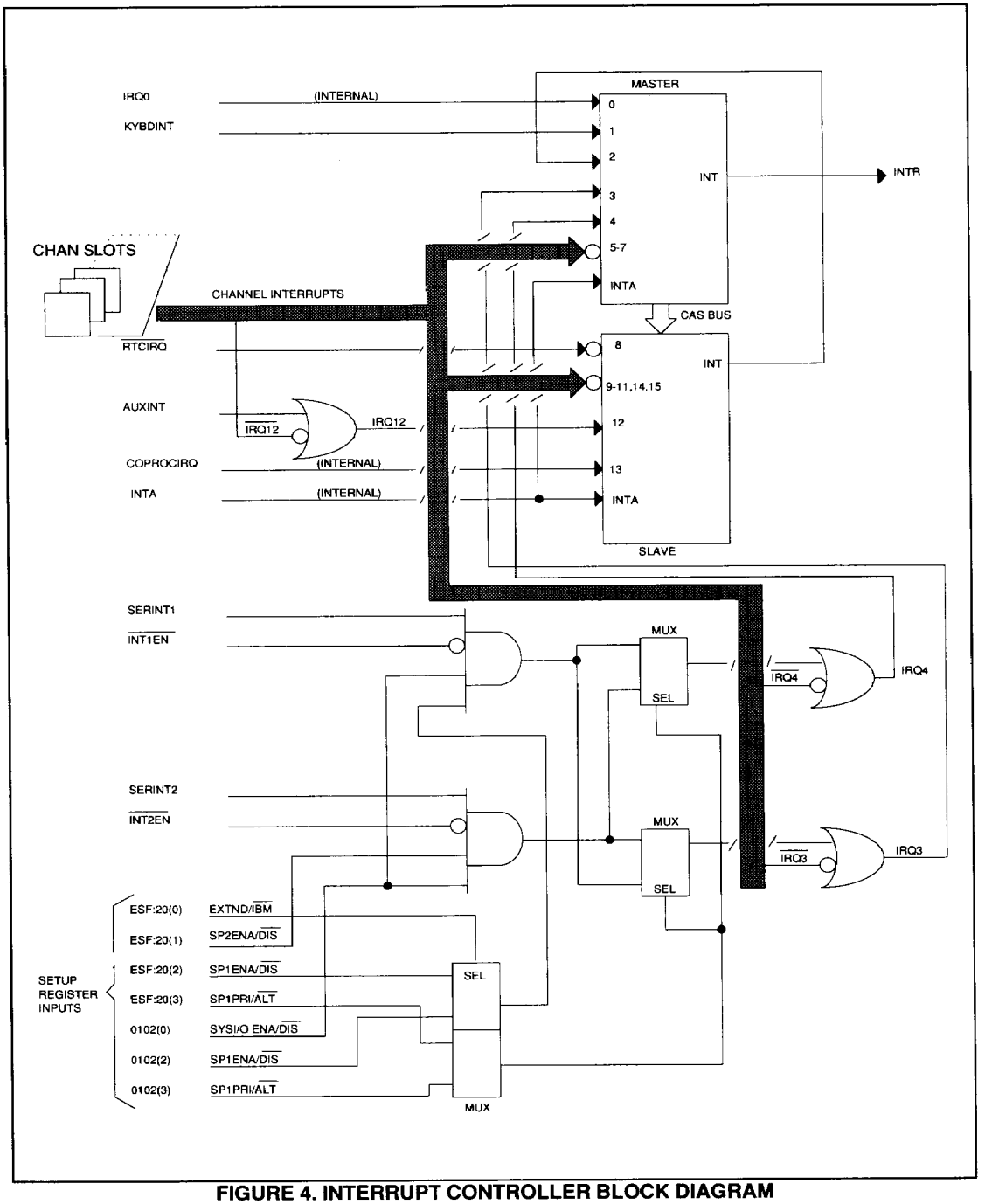


FIGURE 4. INTERRUPT CONTROLLER BLOCK DIAGRAM

SYSTEM SOURCE	CHANNEL	LEVEL
Timer	-	0 [1]
Keyboard Port	-	1
Cascade	-	2 [1]
Alternate Srial Port	IRQ3	3
Primary Serial Port	IRQ4	4
Reserved	IRQ5	5
Floppy Disk	IRQ6	6
Parallel Port	IRQ7	7
RTC	-	8
Cascade Redirectd	IRQ9	9
Reserved	IRQ10	10
Reserved	IRQ11	11
Mouse/Auxiliary	IRQ12	12
Coprocessor	-	13 [1]
Hard Disk	IRQ14	14
Reserved	IRQ15	15

[1] This interrupt is internally generated in the WD6000.

TABLE 2. INTERRUPT SHARING

3.2 INTERRUPT SEQUENCE

The sequence of events that make up an interrupt system environment are described below:

1. One or more interrupts arrive from a peripheral device which sets the corresponding bit(s) in the IRR.

2. The request is evaluated and if the interrupt has not been masked, it is passed to the priority circuit and the Interrupt Controller sends an interrupt (INTR) to the CPU.

3. The CPU responds to the interrupt with an INTA cycle.

4. When the INTA is received, the priority is frozen and the highest priority ISR bit is set. The Interrupt Controller does not drive the data bus during this cycle.

5. The CPU initiates another INTA cycle that causes the Interrupt Controller to send an 8-bit vector to the CPU. Either the master or slave may be programmed to send the byte of data. As long as the ISR bit is set, all interrupts at the same level or lower are inhibited. In Special Mask Mode (SMM), only interrupts at the same level are inhibited. If a higher priority interrupt occurs during an interrupt service routine, it is only acknowledged if the CPU internal interrupt enable has been re-enabled.

When the slave issues an interrupt, other interrupts from the slave are locked out. To preserve priority in the slave, that is, to allow higher interrupts to occur when a power interrupt is being serviced, Special Fully Nested Mode (SFNM) should be programmed in the master. See Section 2.9.4 for more details.

6. At the end of the second INTA cycle, one or two End-of-Interrupt (EOI) commands must be issued to complete the interrupt; one for the master and the other for the slave. This clears the appropriate bit in the ISR.

3.3 END OF INTERRUPT

There are three EOI commands: Specific, Non-Specific, and Automatic. When the Interrupt Controller is programmed to operate in modes that preserve fully nested interrupts, the CPU can determine which ISR bit to reset on EOI, since the

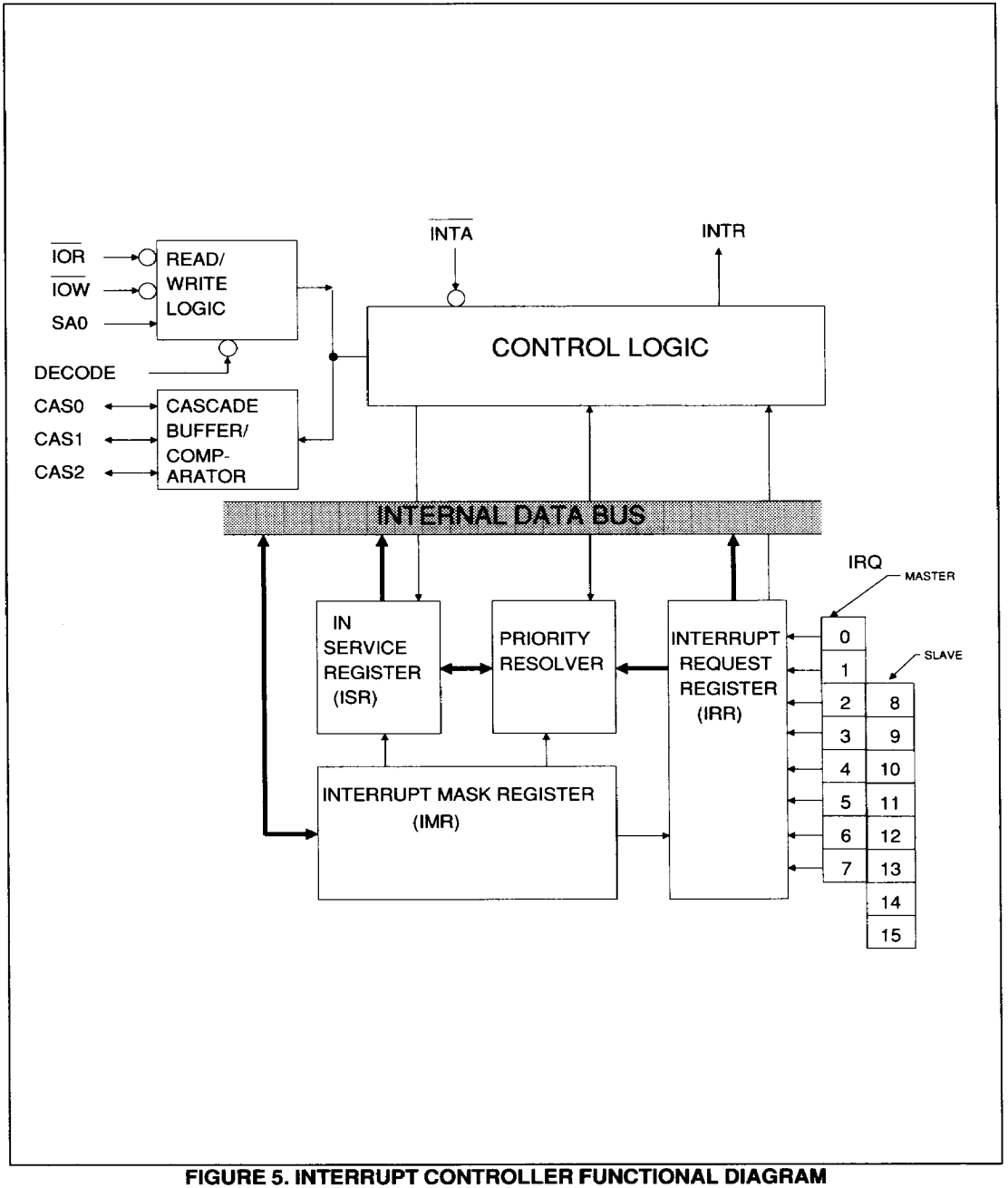


FIGURE 5. INTERRUPT CONTROLLER FUNCTIONAL DIAGRAM

(TYPICAL MASTER OR SLAVE)

current highest priority ISR bit is necessarily the last level acknowledged and serviced. In this case, a non-specific EOI can be issued. In Special Mask Mode, an ISR bit that is masked in the IMR is not cleared by a non-specific EOI.

When the fully nested structure is not preserved, a Specific EOI must be issued at the end of the interrupt service routine, which includes the ISR bit to reset. Both Specific and Non-Specific EOIs are issued with OCW2.

Automatic EOI (AEOI) automatically occurs on the trailing edge of the second INTA cycle. AEOI can only be used for the master, not the slave. AEOI is set with ICW4.

3.4 POLLED MODE

The Interrupt Controller may also be operated in Polled Mode. In this mode, interrupts should be masked by the CPU. An interrupt is detected when the software issues a poll command, setting P = 1 in OCW3. This results in an equivalent INTA cycle during the next read operation to the Interrupt Controller (i.e., IOR = 0, DECODE = 0) which sets the IS bit, if a request was made, and allows the priority level to be read. See Figure 6. The IRR remains frozen until the read cycle is complete. At the end of the process, Polled Mode is reset to zero.

D7	D6	D5	D4	D3	D2	D1	D0
I	-	-	-	-	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to "1" if there is an interrupt.

FIGURE 6. INTERRUPT PRIORITY LEVEL USING THE POLL COMMAND

3.5 INTERRUPT PRIORITY

There are three types of interrupt priority:

- Fixed Priority
- Automatic Rotation
- Specific Rotation

3.5.1 Fixed Priority

In this mode, the interrupts are fully nested; IRQ0 is assigned the highest priority, and IRQ7 the lowest priority. Fixed priority is the default condition, unless Automatic or Specific Rotation is programmed with OCW3.

3.5.2 Automatic Rotation

Automatic Rotation is useful for applications where a number of interrupting devices have equal priority, as the priority is rotated between them. In this mode, the last interrupt serviced has the lowest priority. Figures 7 and 8 show the status of the ISR before and after Automatic Rotation. Once the interrupt with the highest priority (IRQ4 in Figure 7) has been serviced, its status changes from the highest to the lowest priority, as illustrated in Figure 7.

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
0	1	0	1	0	0	0	0
IRQ STATUS							
Lowest Priority							Highest Priority
3	2	1	0	7	6	5	4
PRIORITY STATUS							

FIGURE 7. INTERRUPT PRIORITY BEFORE AUTOMATIC ROTATION

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
0	1	0	0	0	0	0	0
IRQ STATUS							
Lowest Priority							Highest Priority
4	3	2	1	0	7	6	5
PRIORITY STATUS							

FIGURE 8. INTERRUPT PRIORITY AFTER AUTOMATIC ROTATION

3.5.3 Specific Rotation

Specific Rotation fixes the priorities by assigning one interrupt the lowest priority, and thus changing the priorities of the rest. For example, if IRQ4 is programmed to have the lowest priority, then the new order of priority is 5, 6, 7, 0, 1, 2, 3, and 4, with IRQ5 having the highest priority and IRQ4 the lowest priority.

Specific Rotation is programmed with OCW2 in two ways, Rotate on Specific EOI, and Set Priority. Note that priority changes can only be made during an EOI command by using Rotate on Specific EOI.

3.6 SPECIAL MASK MODE

Special Mask Mode (SMM) allows the interrupt priority structure to be dynamically changed. In SMM, when a bit is masked in OCW1, interrupts are inhibited at that level; all other levels, lower or higher, that are not masked are enabled. This selectively enables interrupts by changing the IMR. SMM is programmed with OCW3.

3.7 READING REGISTER STATUS

The status of the IRR and ISR can be read at Address 020H (master) and 0A0H (slave). Prior to the read status operation, indicate the register to be read with OCW3. The contents of the selected register can be read again, unless Polled Mode is selected, that is, there is no need to write another OCW3 to read the same register.

The IMR can be read at Addresses 021H and 0A1H.

3.8 INTERRUPT TRIGGERING

An interrupt request is recognized by a low level on the $\overline{IRQ}$ input. The interrupt request must be removed before the EOI is issued or before the CPU internal interrupt enable has been re-enabled. Otherwise, a second interrupt is detected.

The $\overline{IRQ}$ inputs must remain low until after the falling edge of the first $\overline{INTA}$ as generated from interrupt acknowledge cycles from the CPU. See Figure 9. If the $\overline{IRQ}$ goes high before this time, the Interrupt Controller issues an Interrupt Level 7 vector during the second INTA cycle, thus ignoring the false interrupt. This allows false interrupts caused by spurious noise glitches on the interrupt inputs to be detected.

If IRQ7 is needed for another purpose, a false IRQ7 can still be detected by reading the ISR. A normal IRQ7 sets the corresponding ISR bit; a false IRQ7 does not, except when a false IRQ7 occurs during a normal IRQ7. In this case, it is necessary to keep track of IRQ7 occurrences to determine default occurrences that may follow.

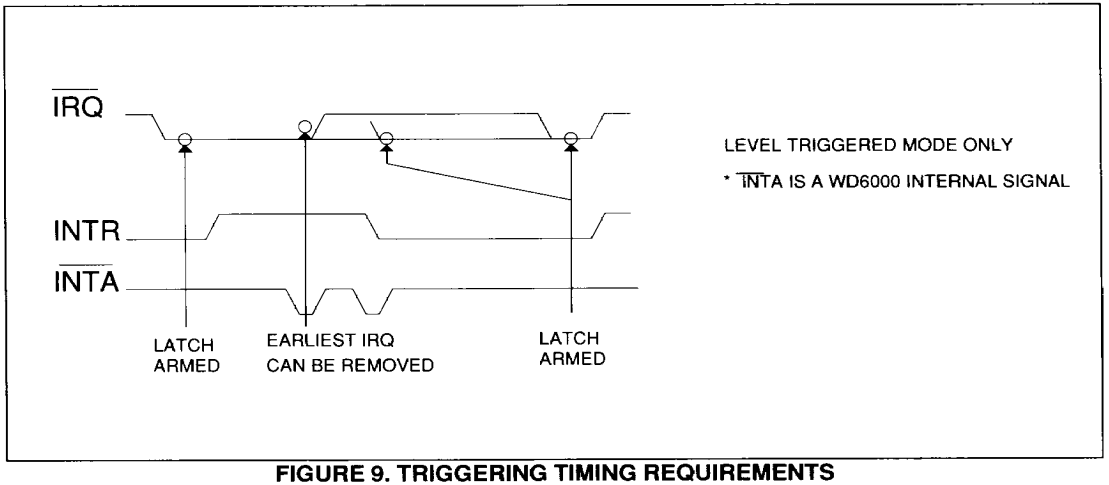


FIGURE 9. TRIGGERING TIMING REQUIREMENTS

(NOTE: I/O ADDRESS 20/21H APPLIES TO MASTER, A0/A1H APPLIES TO SLAVE)

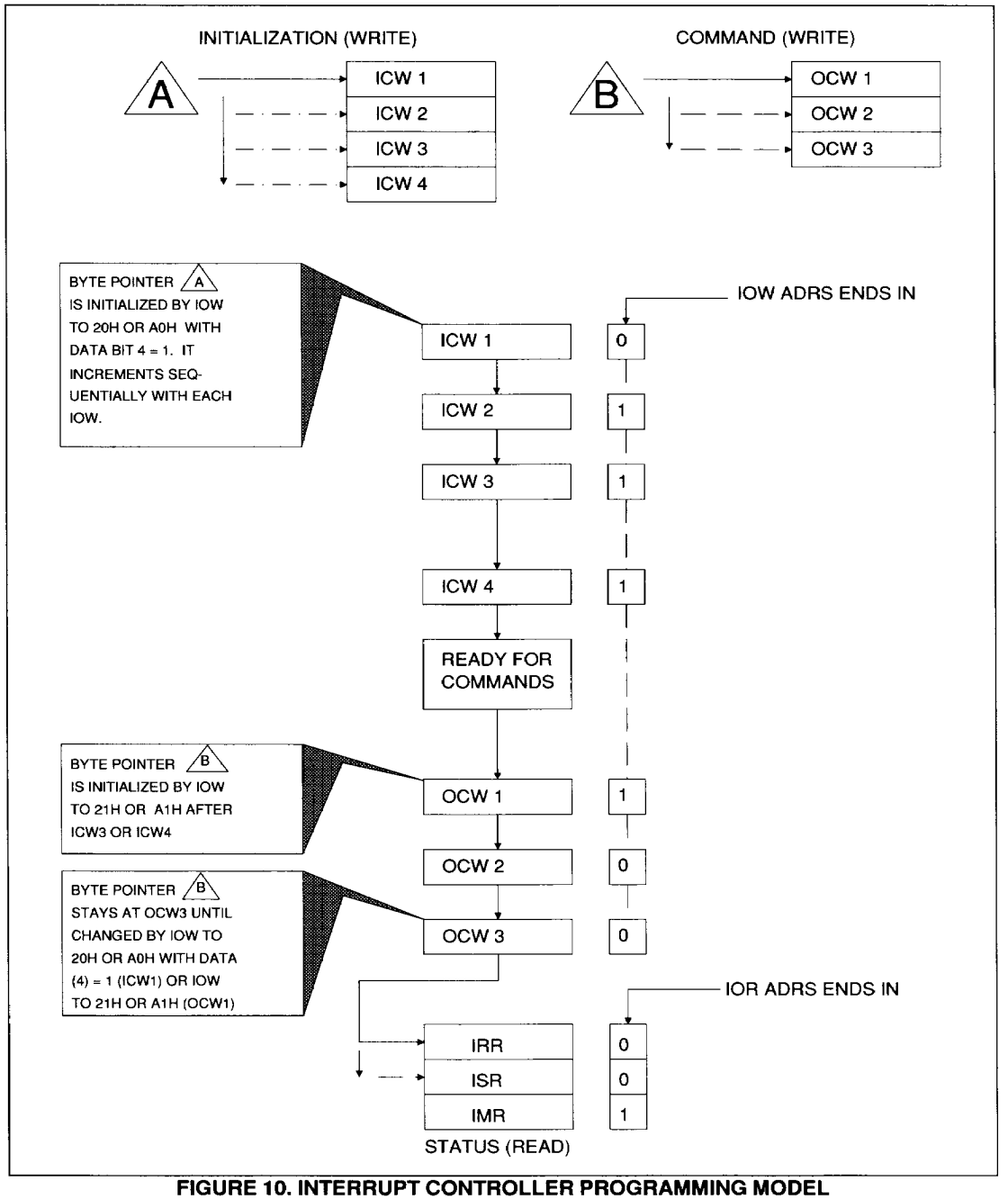


FIGURE 10. INTERRUPT CONTROLLER PROGRAMMING MODEL

(NOTE: I/O ADDRESS 20/21H APPLIES TO MASTER, A0/A1H APPLIES TO SLAVE)

3.9 PROGRAMMING

The Interrupt Controller is initialized by writing a series of Initialization Command Words (ICWs) to each controller, whether master or slave. See Figure 10 for more information. After initialization, the controllers are ready to accept interrupt requests. Operation Control Words (OCWs) can then be used to change operating modes and command the controllers for various functions. The master and slave can be programmed to work in different modes.

Table 3 indicates each read/write function and its corresponding address for Interrupt Controllers 1 and 2, master and slave respectively.

INTERRUPT CONTROLLER	ADDRESS	FUNCTION	READ/WRITE
1	020	ICW1	Fixed
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	IMR	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	IMR	Read

TABLE 3. INTERRUPT CONTROLLER FUNCTION MAP

3.9.1 Initialization Command Word 1 (ICW1)

The initialization sequence is started by writing ICW1 to Address 020H or 0A0H. ICW1 has a fixed format, illustrated in Figure 11. Initialization accomplishes the following:

1. The Interrupt Mask Register is cleared.
2. Fixed Priority Mode is selected.
3. The Slave Mode address is set to 2.
4. Special Mask Mode is cleared.
5. IRR is set for Status Read.

The next three commands to Addresses 021H or 0A1H load ICW2 through ICW4.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
-	-	-	-	LVL TRIG MODE	-	CASCADE MODE	ICW4 NEEDED
0	0	0	1	1	0	0	1

FIGURE 11. ICW1

▒▒ = Nonprogrammable

3.9.2 Initializaation Command Word 2 (ICW2)

Bits 3-7 are the five most significant bits of the interrupt vector (T3-T7); they are programmable by the CPU. Bits 0-2 are generated by the Priority Resolver during the INTA cycle, according to the interrupt level. Refer to Table 2. Figure 12 shows the format for ICW2.

11

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
INTERRUPT LEVEL HAS SLAVE							
YES NO	YES NO	YES No	YES NO	YES NO	YES NO	YES NO	YES NO
0	0	0	0	0	0	1	0

			LEVEL	
D2	D1	D0	MASTER	SLAVE
0	0	0	0	8
0	0	1	1	9
0	1	0	2	10
0	1	1	3	11
1	0	0	4	12
1	0	1	5	13
1	1	0	6	14
1	1	1	7	15

FIGURE 12. ICW2 FORMATS

3.9.3 Initialization Command Word 3 (ICW3)

ICW3 initializes the master and slave. For the master, ICW3 sets a 1 for each IRQ input used to cascade a slave. For the slave, bits 0-2 of ICW3 provide the Slave Mode address. Figure 13 shows the format for ICW3 for master and slave. The formats are fixed and must be written as shown in order to function.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
INTERRUPT LEVEL HAS SLAVE							
YES NO	YES NO	YES No	YES NO	YES NO	YES NO	YES NO	YES NO
0	0	0	0	0	0	1	0

D2	D1	D0	SLAVE ID = 2
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FIGURE 13. ICW3 FORMATS

3.9.4 Initialization Command Word 4 (ICW4)

ICW4 is used to program Special Fully Nested Mode (SFNM) and Automatic End of Interrupt (AEOI). See Figure 14 for details.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
-	-	-	SPECFULLY NESTMODE	-	-	AUTO EOI	-
0	0	0	YES NO	0	0	AUTO NOR	

FIGURE 14. ICW4

= Non-programmable

3.9.5 Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the IMR. See Figure 15. M0-M7 represent the eight mask bits, where M0 controls IRQ0, M1 controls IRQ1, and so on. Programming a 1 indicates that the interrupt is masked.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
M7/S15		M6/S14		M5/S13		M4/S12		M3/S11		M2/S10		M1/S9		M0/S8	
YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO

Mn = Master Mask Bit
Sn = Slave Mask Bit

FIGURE 15. OCW1 (MAS REG)

3.9.6 Operation Control Word 2 (OCW2)

Bits 5-7 (EOI, SL and R) of COW2 control the EOI and Rotate modes and combinations of the two. See Figure 16. Bits 0-2 (L0-L2) of OCW2 determine which interrupt is affected when Bit 6 is active.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R		SL		EOI		-		-		IRQ LEVEL					
-		-		-		0		0		L2		L1		L0	

D2	D1	D0	FUNCTION
0	0	0	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate Non-specific EOI command
1	0	0	Rotate In Automatic EOI Mode (set)
0	0	0	Rorate in Automatic EOI Mode (Clr)
1	1	1	*Rotate on Specific EOI Command
1	1	0	*Set Priority Command
0	1	0	No Operation

*L0-L2 ARE USED

L2	L1	L0	IRQ LEVEL MASTER	IRQ LEVEL SLAVE
0	0	0	0	8
0	0	1	1	9
0	1	0	2	10
0	1	1	3	11
1	0	0	4	12
1	0	1	5	13
1	1	0	6	14
1	1	1	7	15

= Non-programmable

FIGURE 16. OCW2

3.9.7 Operation Control Word 3 (OCW3)

Bits 5 and 6 program Speciao Mask Mode (SMM). Sets Bits 5 (SMM) and 6 (ESMM) to 1 to program SMM. Refer to Figure 17. If SMM is set to zero, it resets the controller to Normal Mask Mode. Polled Mode is enabled when Bit 2 is set to 1.

Set Bit 1 (RR) and Bit 0 (RIS) to 0 to read the status of the ISR on SD0-SD7 at Address 020H or 0A0H. Set Bit 1 to 1 and Bit 0 to 0 to read the status of the IRR on SD0-SD7 at Address 020H or 0A0H.

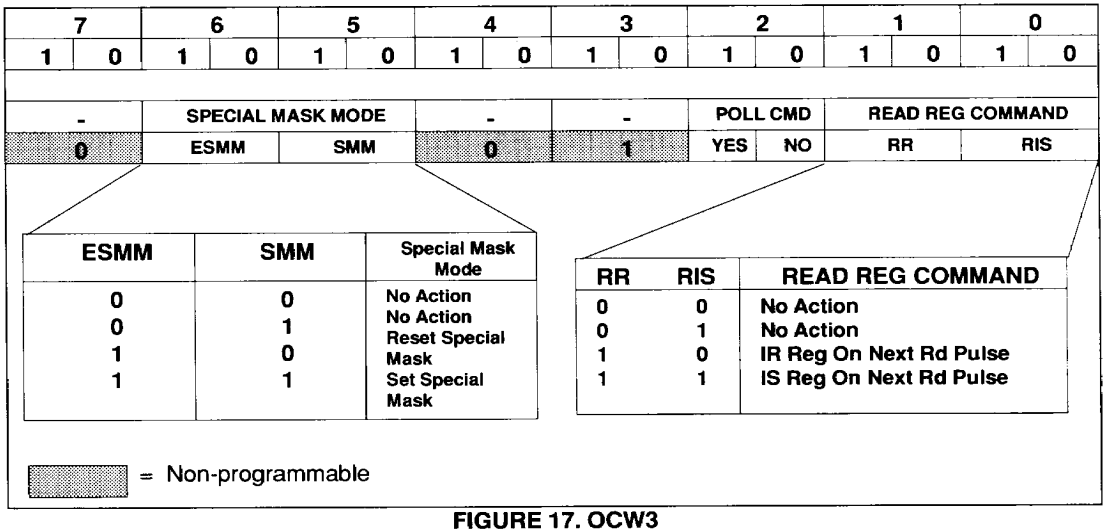


FIGURE 17. OCW3

4.0 TIMERS AND CLOCK GENERATION

The WD6000 has four counters of timers designated Timers 0, 1, 2 and 3. See Figure 18.

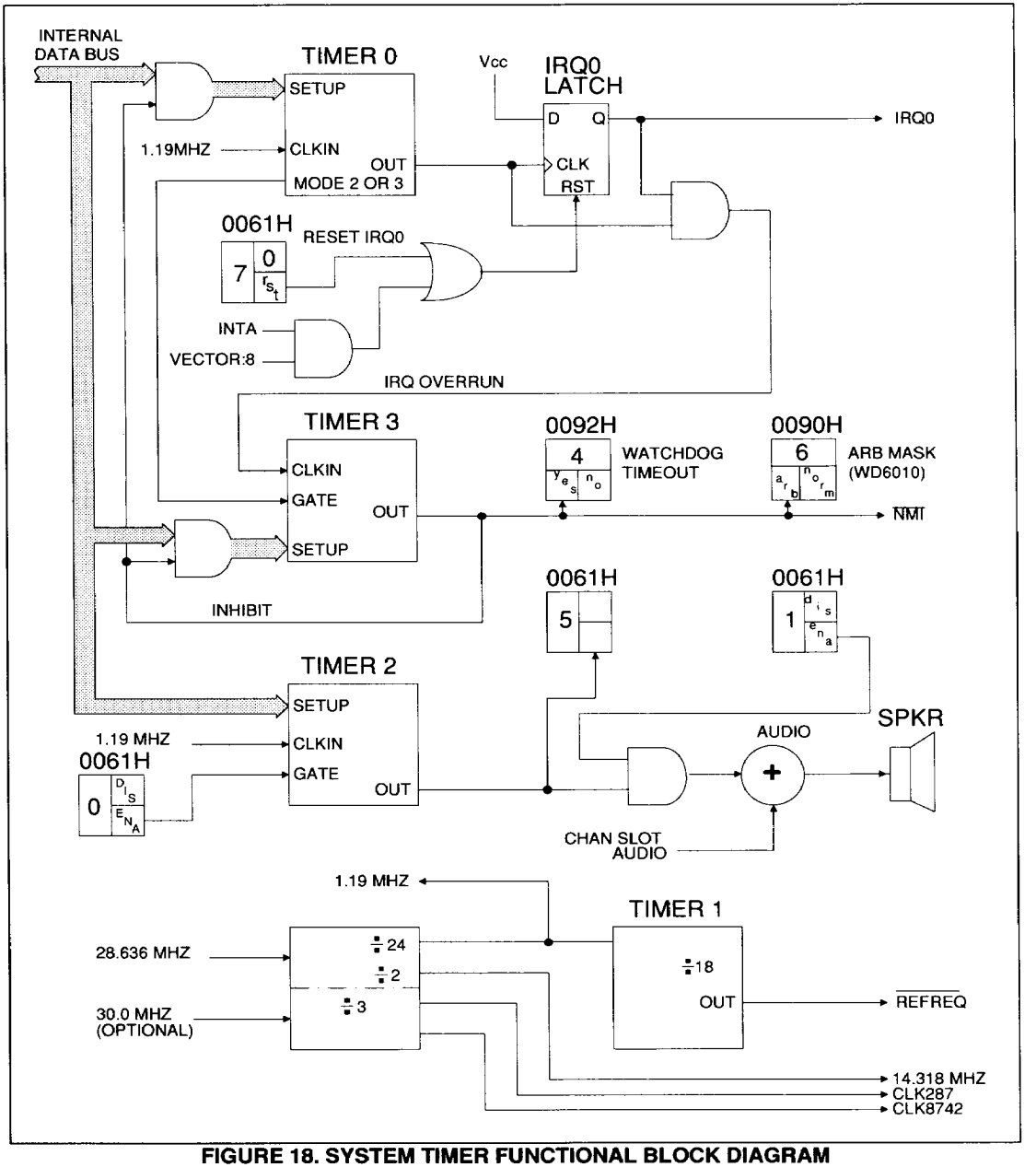


FIGURE 18. SYSTEM TIMER FUNCTIONAL BLOCK DIAGRAM

4.1 TIMERS

Timer 1 generates Refresh requests, and is not programmable. REFREQ is generated based on a 1.19 MHz clock divided by 18 (28.636 MHz divided by 24).

Timer 1 also generates the clocks to the 80387/80387SX and 8742 devices. The MHZ30 clock input is optional, making a lower cost implementation possible. If a MHZ30 clock input is connected to a 30.0 MHz clock, the output clock is 10 MHz. If not, this pin will be connected to a MHZ28 pin, in which case the output to the 8742 device will be 9.54 MHz.

Timers 0 and 2 are 16-bit, programmable binary or BCD down counters. Timer 3 is an 8-bit binary down counter which can be preset. All three timers are fully independent and can be programmed, except as noted, to operate in the modes shown in Table 4. Addresses 0040H, 0042H, and 0044H are the data ports for Timers 0, 2, and 3, respectively. Timers 0 and 2 are 16-bit, programmable, binary or BCD 16-bit synchronous down counters that can be preset.

MODE	DESCRIPTION
0	Interrupt on Terminal Count
1	Hardware Retriggerable One Shot (Timer 2 only)
2	Rate Generator
3	Square Wave
4	Software Retriggerable Strobe

TABLE 4. COUNTER OPERATING MODES

ADDRESS	FUNCTION
040H	Timer 0 Read/Write
042H	Timer 2 Read/Write
044H	Timer 3 Read/Write
043H	Control Word Reg. (Timer 0 or 3) Write Only
047H	Control Word Reg. (Timer 3) Write Only

TABLE 5. COUNTER/TIMER ADDRESS MAP

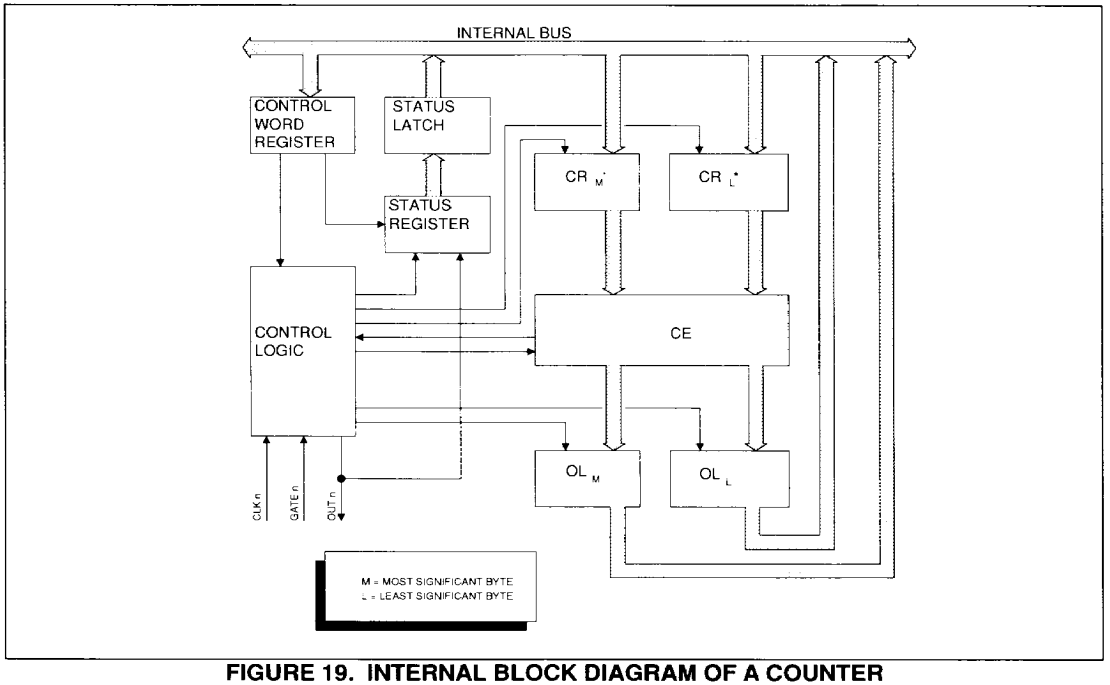


FIGURE 19. INTERNAL BLOCK DIAGRAM OF A COUNTER

4.2 PROGRAMMING

At power-up the counter mode, count value, and output of all counters and registers is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word to the Control Word Register followed by an initial count. The Control Word indicates the counter being programmed and the format of the initial count (e.g. most significant only). Figure 20 shows the format for the Control Word for Timers 0 and 2 and 3 at their respective addresses.

4.2.1 Write Operations

When writing to each counter, the Control Word must be written before the initial count is written and the initial count must follow the format specified in the Control Word. As long as the conventions in the Control Word formats are followed, no particular programming sequence is required.

A new initial count may be written to a counter at any time without affecting the programmed mode of the counter, provided the programmed format is followed. Counting is affected as described in the mode definitions.

---------- Important ----------

When writing two-byte counts, do not transfer control to another routine that writes into the same counter between the first and second bytes. If you do so, the counter is loaded with an incorrect count.

4.2.2 Read Operations

The counters can be read in three ways: a read operation, the Counter Latch Command, and the Read-Back Command. A simple read operation to a counter requires that the CLK input of the selected counter be inhibited by using the GATE input. If it is not inhibited, a false reading could result because the counter may change during the read.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0

SELECT COUNTER		READ/WRITE MODE		PROGRAM MODE			COUNT MODE	
SC1	SC0	RW1	RW0	M2	M1	M0	BCD	BNY

SC1	SC0	SELECT COUNTER
0	0	Select Counter 0
0	1	Reserved
1	0	Select Counter 2
1	1	Read-back Command (See Read Operations)

RW1	RW0	READ/WRITE MODE
0	0	Counter Latch Command (see Read Operations)
0	1	Read/ Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

M2	M1	M0	PROGRAM MODE
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

(Register 0043H W/O)

SELECT COUNTER		SETUP MODE		RESERVED
SC1	SC0	RW1	RW0	0

SC1	SC0	SELECT COUNTER
0	0	Select Counter 3
0	1	Reserved
1	0	Reserved
1	1	Reserved

(Register 0047H W/O)

RW1	RW0	SETUP MODE
0	0	Counter 0 Latch Command
0	1	Read/Write least significant byte only
1	0	Reserved
1	1	Reserved

= Nonprogrammable

FIGURE 20. CONTROL WORD FORMATS

7	6	5	4	3	2	1	0
-	-	STATUS/COUNTER SELECT		COUNTER SELECTED			-
1	1	- CNT	- STS	COUNTER2	COUNTER1	COUNTER0	0

FIGURE 21. READ-BACK COMMAND

Important

When reading two-byte counts, do not transfer control to another routine that reads from the same counter between the first and second byte. This could result in an incorrect count being read.

Counter Latch Command—When a Counter Latch Command is issued in a Control Word (see Figure 20), the output latches OLs of the selected counter latch, the current count of the CE. The count remains latched until read by the CPU or until the counter is reprogrammed. A subsequent counter latch command for the same counter is ignored if issued before the latches are read. A Counter Latch Command may be issued to more than one counter. It does affect the programmed mode of the counter.

Read-Back Command—When a Read-Back Command is issued in a Control Word (see Figure 21), the count, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter(s) can be checked. The Read-Back Command can be used to latch multiple counter output latches OLs by setting D5 = 0 and by selecting the desired counter(s). This command is equivalent to several counter latch commands; one for each counter latched. As with the counter latch command, counts are held until read by the CPU or until the counter is reprogrammed.

OUTPUT	COUNT		READ/WRITE MODE		PROGRAM MODE			COUNT MODE	
STATE	NULL	AVAIL	RW1	RW0	M2	M1	M0	BCD	BNRY

Counter 0, 2 Status Byte

RW1	RW0	READ/WRITE MODE
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

M2	M1	M0	PROGRAM MODE
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

OUTPUT	COUNT		READ/WRITE MODE		RESERVED
STATE	NULL	AVAIL	RW1	RW0	0

Counter 3 Status Byte

RW1	RW0	READ/WRITE MODE
0	0	Counter 0 Latch Command
0	1	Read/Write least signif. byte only
1	0	Reserved
1	1	Reserved

FIGURE 22. COUNTER STATUS BYTES

COMMAND								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status-Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count-Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read bacvk count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Cntr 1

FIGURE 23. READ-BACK COMMAND EXAMPLES

Status information of the selected counter(s) can be latched by the Read-Back Command by setting status bit D4 = 0. The status is latched until read by the CPU with a read operation to the counter or until the counter is reprogrammed. Figure 21 shows the format for the counter status. Bits 0–5 indicate the programmed status of the counter as written into the Control Word Register.

D7 (Figure 22) allows the counter output to be monitored. The Null Count (NC) flag indicates the condition of the CE. NC = 1 during a write operation to the Control Word Register or the counter. NC = 0 when a new count is loaded from the CRs to the CE. If the counter is programmed for two-byte counts, NC = 1 when the second byte is written.

Both the count and status of the selected counter(s) may be latched simultaneously by setting D4 and D5 to 0. This command is equivalent to two read-back commands.

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

Note: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 24. MINIMUM AND MAXIMUM INITIAL COUNTS

If both the count and the status are latched with a read-back command, the first read operation to the selected counter(s) returns the status. The next read, or two reads if the counter is programmed for two-byte counts, returns the latched count. Subsequent reads return unlatched counts.

4.3 COUNTER OPERATION

Each counter may be set in one of five modes by writing a Control Word. When a Control Word is written to a counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulse is required.

New counts are loaded and counters are decremented on the falling edge of CLK. The maximum possible initial count is 0-equivalent to 65536 in binary operation or 10000 in BCD. The counter does not stop when it reaches 0. In Modes 0, 1, 4, and 5 it wraps around to the highest count (FFFF in binary operation or 9999 in BCD). In Modes 2 and 3, the counter is reloaded with the initial count and continues counting. Figure 24 shows minimum and maximum initial counts for each mode.

The GATE input is level-sensitive in Modes 0, 2, 3, and 4 and is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. A rising edge (trigger) sets an internal flip-flop whose output is sampled on the next rising edge of CLK. The flip-flop resets immediately after it is sampled. Note that in Modes 2 and 3, the GATE input is both edge-and-level-sensitive.

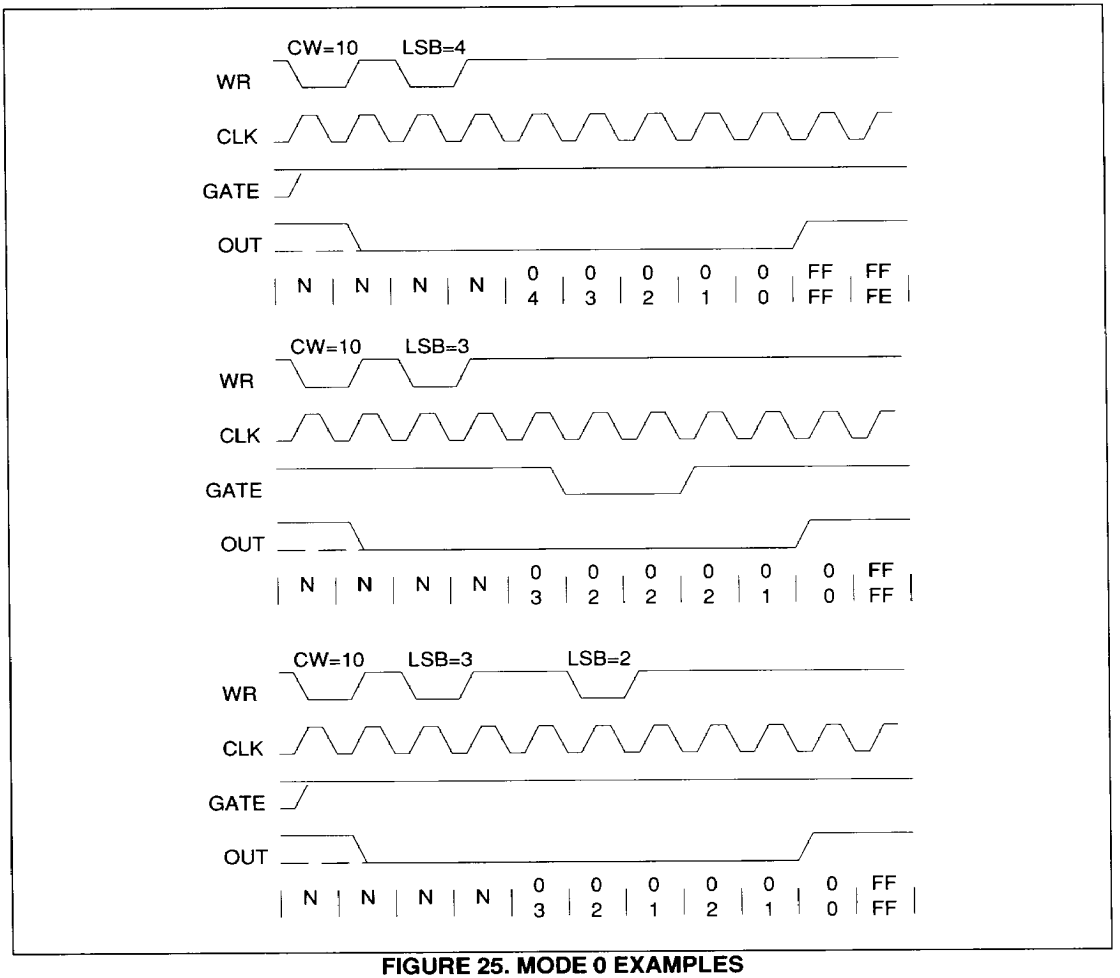


FIGURE 25. MODE 0 EXAMPLES

4.3.1 Mode 0—Interrupt on Terminal Count

Mode 0 is typically used for event counting. Writing the Control Word causes OUT to go low and remain low until the counter reaches 0. At this time OUT goes high and remains high. The counter continues to run until a new count or Control Word is written. Counting is enabled when GATE = 1. Disabling the count (GATE = 0) has no effect on OUT.

The initial count is loaded into the CE on the next CLK pulse after the Control Word and initial count are written. For an initial count of N, OUT goes high N+1 CLK pulses later. Writing a new count reloads the counter (CE) on the next CLK pulse and counting continues from the new count.

When writing a two-byte count, the first byte disables counting and OUT is set low. After writing the second byte, the new count is loaded on the next CLK pulse. This allows the counting sequence to be synchronized by the software.

If an initial count is written when GATE = 0, it is still loaded on the next CLK pulse. When GATE = 1, counting begins and OUT goes high N CLK pulses later. Figure 25 shows examples of Mode 0 operation.

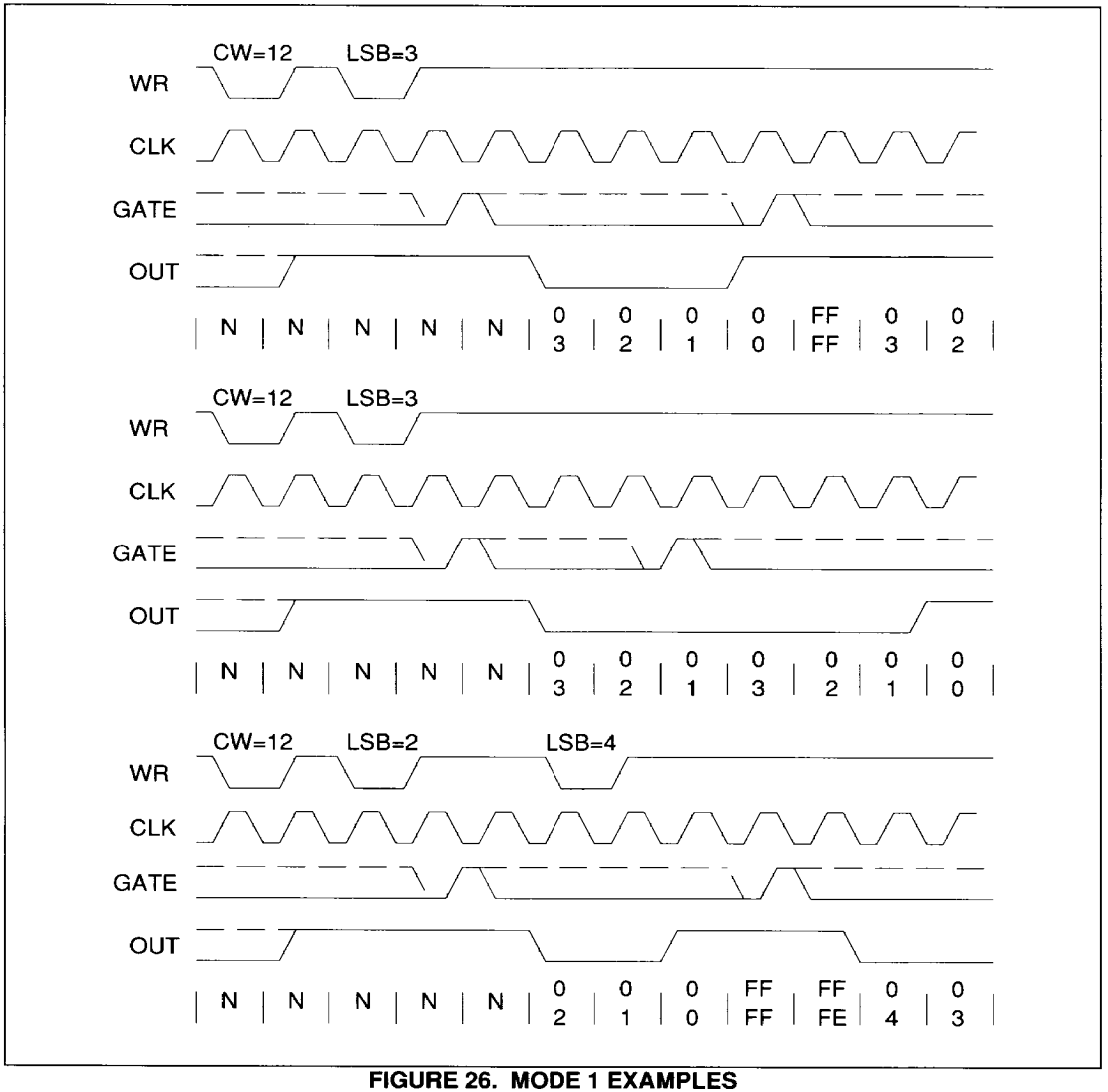


FIGURE 26. MODE 1 EXAMPLES

4.3.2 Mode 1—Hardware Retriggerable One-Shot

Writing the Control Word causes OUT to go high. A trigger (i.e., GATE = 1) causes OUT to go low on the next CLK pulse and remain low until the counter reaches 0; this creates a one-shot pulse. At this time, OUT goes high and remains high until the next trigger. An initial count of N results in a one-shot pulse N CLK cycles long.

Since the one-shot is retriggerable, if another trigger occurs during a one-shot pulse, OUT remains low to extend the pulse for N CLK cycles. Writing a new count during a one-shot pulse has no effect unless the counter is retriggered, in which case the pulse extends from the new count. GATE has no effect on OUT. Figure 26 shows examples of Mode 1 operation. Mode 1 is valid for Counter 2 only.

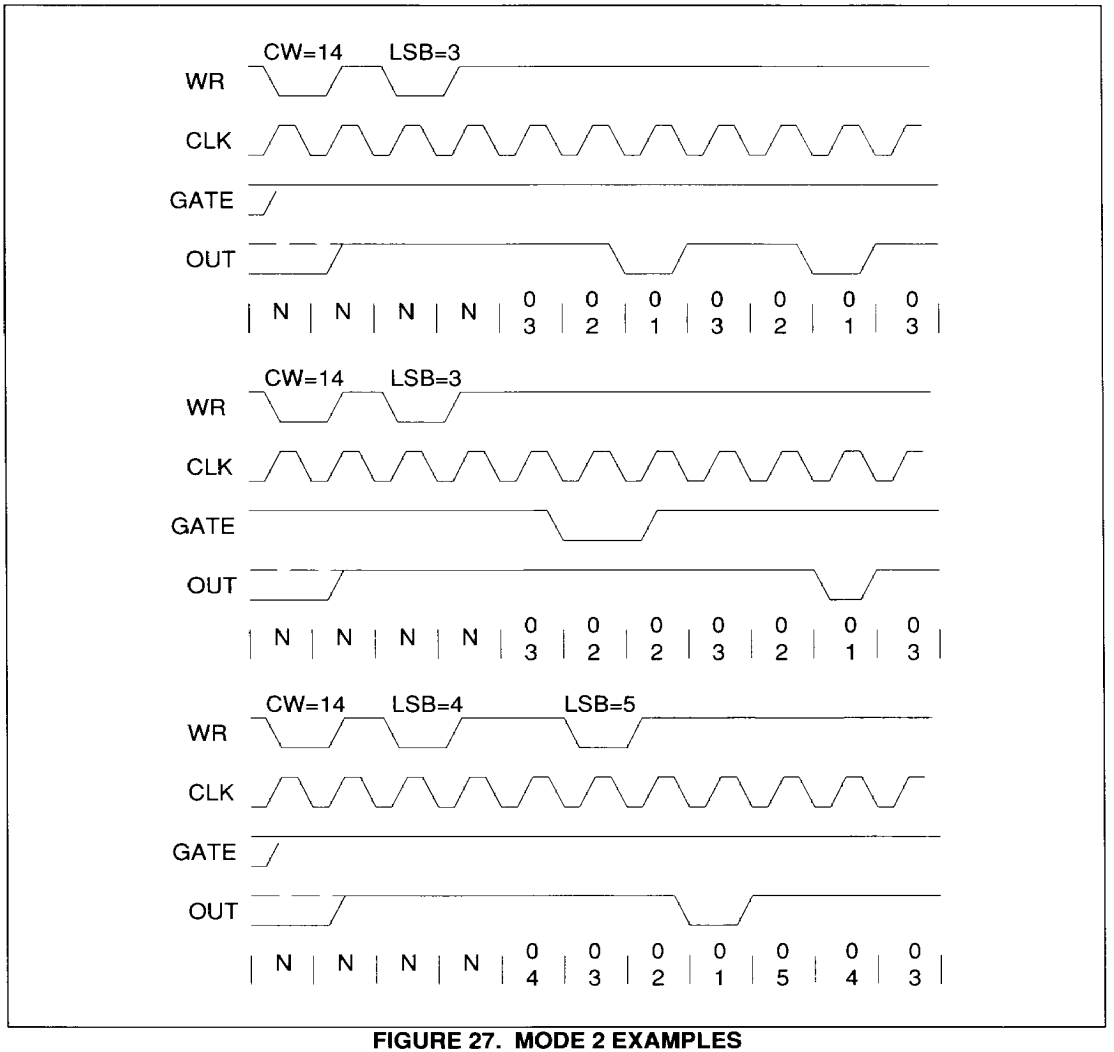


FIGURE 27. MODE 2 EXAMPLES

4.3.3 Mode 2—Rate Generator

Mode 2 functions as a divide-by-N counter. It is typically used to generate a real-time clock interrupt. Writing the Control Word causes OUT to go high. When the initial count reaches 1, OUT goes low for one CLK pulse. When OUT becomes high, the counter reloads the initial count and the process is repeated. For an initial count of N, the sequence repeats every N CLK cycles. Note that a count of one is illegal in Mode 2.

Counting is enabled when GATE = 1. GATE = 0 disables counting and forces OUT to high. A trigger reloads the counter with the initial count on the next CLK pulse. Using the GATE input allows counting to be synchronized with external events.

Writing a new count during a counting sequence has no effect unless the counter is triggered. If triggered, the count is extended by the new count on the next CLK pulse. If not, the new count is loaded at the end of the current counting cycle. Figure 27 shows examples of Mode 2 operation.

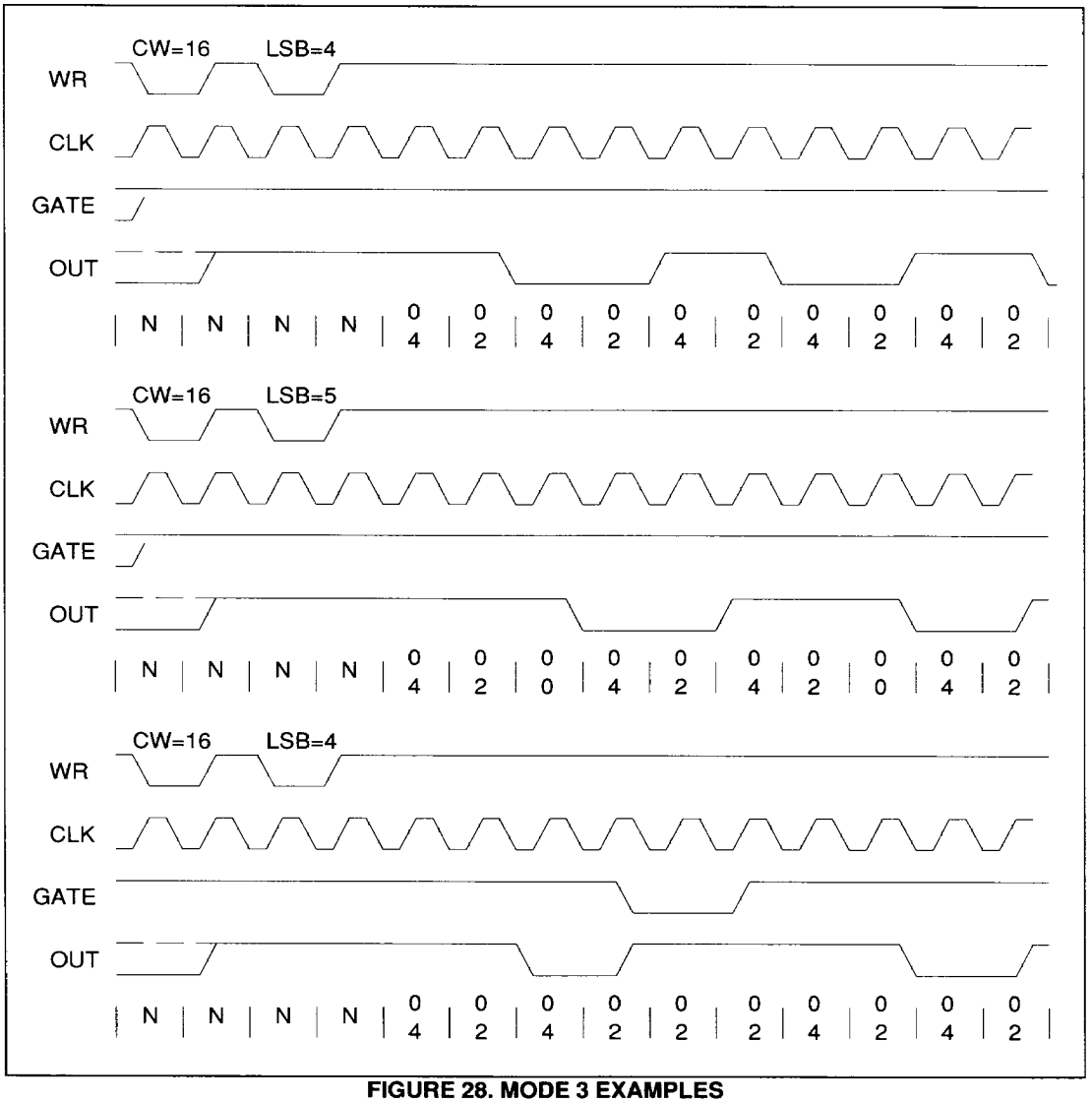


FIGURE 28. MODE 3 EXAMPLES

4.3.4 Mode 3—Square Wave Generator

Mode 3 is typically used for Baud rate generation. This mode is identical to Mode 2 except for the OUT duty cycle. Writing to the Control Word causes OUT to become high and remain high for the first half of the count. Then OUT becomes low and remains low for the remainder of the count. The cycle is repeated, creating a square wave with a period of N CLK cycles when the initial count is N.

If the counter is loaded with an even count, the OUT duty cycle is 50% (i.e., high = low = N2). For odd count values, OUT is high for one CLK cycle longer than it is low (i.e., high = (N+1)/2 and low = (N-1)/2). Figure 28 shows examples of Mode 3 operation.

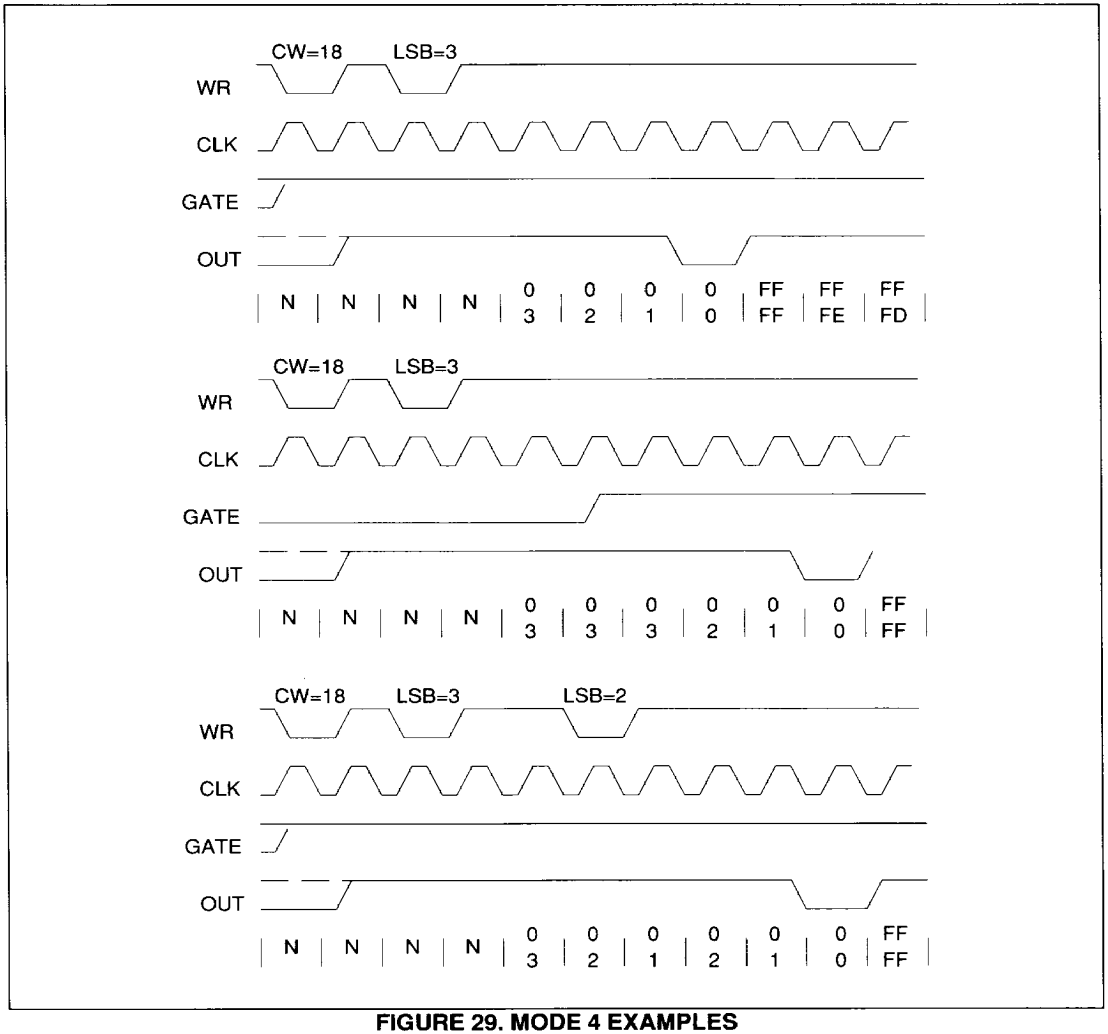


FIGURE 29. MODE 4 EXAMPLES

4.3.5 Mode 4—Software Triggered Strobe

Writing the Control Word causes OUT to go high. When the initial count expires, OUT goes low for one CLK cycle. The sequence is started by writing the initial count. Counting is enabled when GATE = 1. Disabling the count (GATE = 0) has no effect on OUT.

The initial count is loaded on the next CLK pulse after the Control Word and initial count are written. For an initial count of N, OUT goes low for one CLK cycle N+1 CLK cycles later.

If a new count is written during a counting sequence, it is loaded into the CE on the next CLK pulse and counting continues from the new count. When writing a two-byte count, the first byte has no effect on counting. After writing the second byte, the new count is loaded on the next CLK pulse. This allows the counting sequence to be retriggered by the software. Figure 29 shows examples of Mode 4 operation.

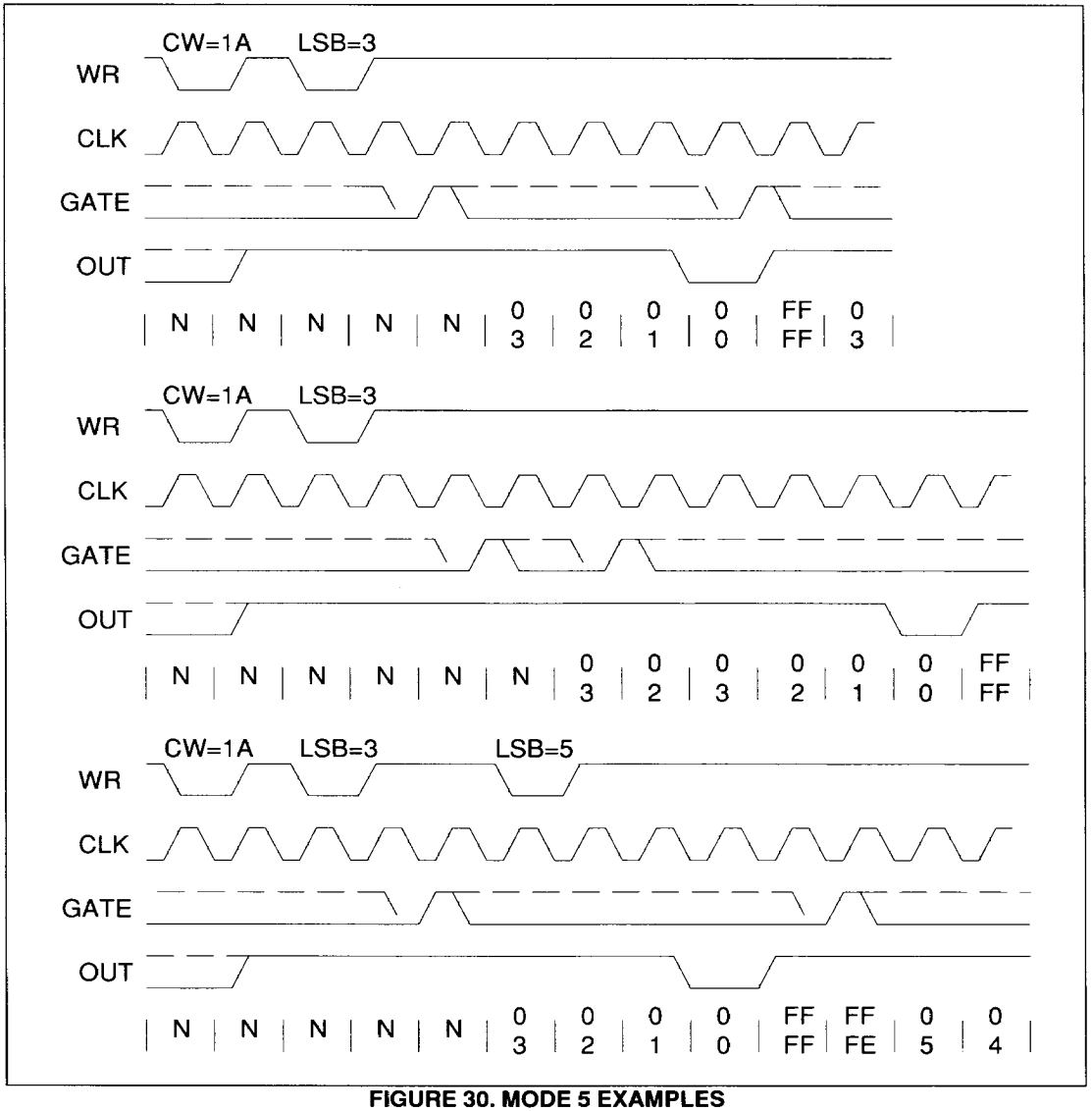


FIGURE 30. MODE 5 EXAMPLES

4.3.6 Mode 5—Hardware Triggered Strobe

Writing the Control Word causes OUT to go high. Count-ing is started by a trigger (i.e., rising edge of GATE) which loads the CE on the next CLK pulse. When the initial count N expires, N CLK cycles later, OUT goes low for one CLK cycle. GATE = 0 disables the counting.

Writing a new count during a counting sequence has no effect unless the counter is triggered. If triggered, the count is extended by the new count on the next CLK pulse. If not, the new count is loaded at the end of the current counting cycle. Figure 30 shows examples of Mode 5 operation. Mode 5 is valid only for Counter 2.

4.4 WATCHDOG TIMER OPERATION

The watchdog timer is set up by writing the control word for Timer 3 to Location 0047H and the count value to Location 0044H. Timer 3 is enabled to count on the first CLK pulse after the count is loaded to the CE. The CLK pulse for the watchdog timer is the output of Timer 0 and occurs every 55.05 ms.

The watchdog timer, Timer 3, can be enabled to monitor the IRQ0 service routine. When Timer 3 is loaded with a count of one and latched IRQ0 is pending for more than one CLK cycle, Timer 3 decrements to zero, generating a watchdog timeout and NMI. Write access to Timer 0 and 3 is not permitted when a watchdog time-out occurs.

The watchdog timer implementation assumes that the NMI vector in low memory has not been corrupted. System recovery may be invoked by the NMI service routine.

The IRQ0 Latch is reset by any of the following:

1. System Reset
2. IOW to 0061H D7 = 1
3. INTA (Interrupt Ack) with vector (D7:0)=8

Timer 3 is disabled by resetting the IRQ0 Latch and then performing the steps described for the watchdog set up.

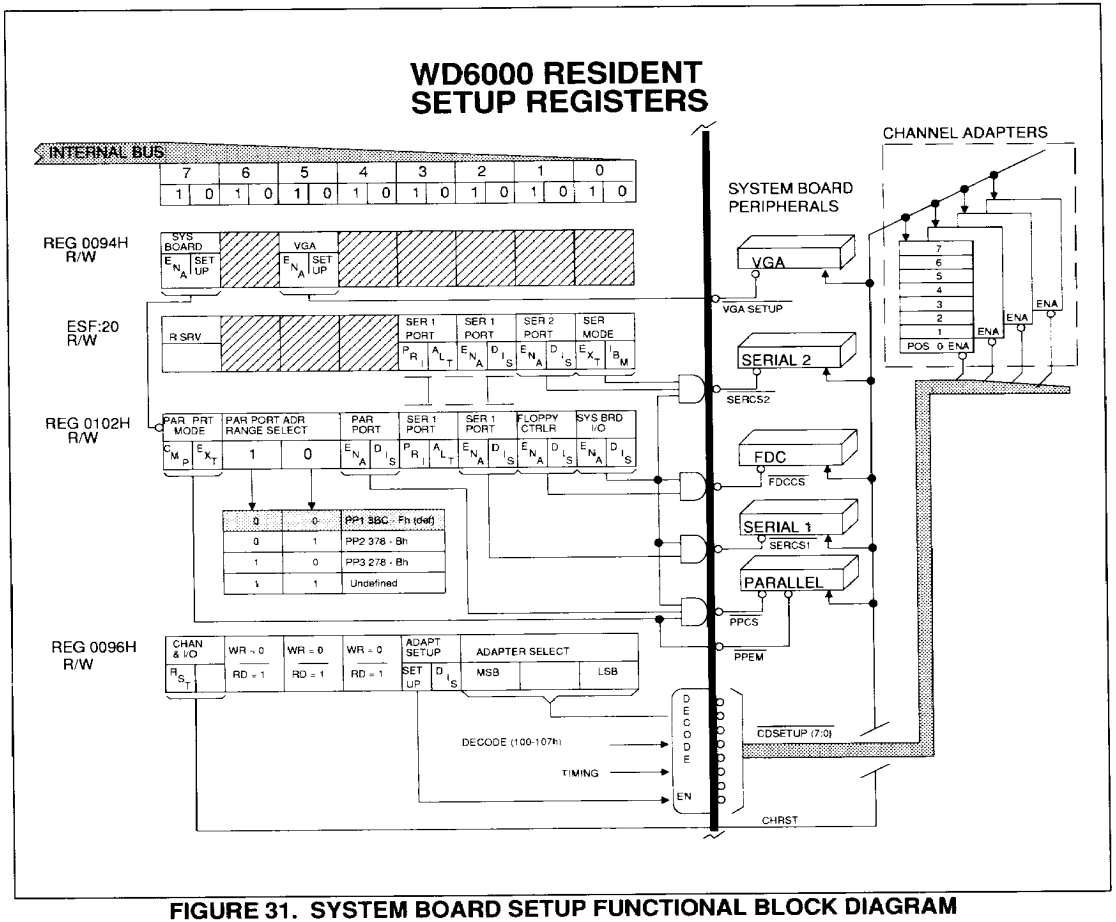


FIGURE 31. SYSTEM BOARD SETUP FUNCTIONAL BLOCK DIAGRAM

5.0 SYSTEM BOARD SETUP

The Programmable Option Select (POS) is implemented by I/O Registers 0091H, 0094H, 0096H, 0100H, 0101H, 0102H, and 0103H. For details, see Figure 31. POS eliminates switches from the system board and Channel adapters by incorporating programmable registers. The programmed configuration data and adapter ID numbers are then stored in battery-backed CMOS RAM. This permits the Power-On Self-Test (POST) to automatically reconfigure the system whenever the system is powered on.

- **System ID Setup**

POS Registers 0100H and 0101H contain the system ID code. These registers are read-only, but can be written once to store the appropriate ID.

- **Parallel Port Setup**

Figure 32 defines the bits in POS Registers 0102H and 0103H. Bit 0 of Register 0102H allows Bits 1, 2, and 4 to enable and disable their respective devices. In Compatible Mode (Bit 7 = 1), the parallel port is compatible with the PC/AT printer port. In Extended Mode, it operates in bi-directional mode, compatible with PS/2 MCA machines. This port is configured by POS Register 0102H, Bits 4–7.

- **Serial Ports Setup**

The configuration of on-board serial ports is controlled by either POS Register 0102H or the Peripheral Control Register (PCR). The PCR is part of the Extended Setup Facility (ESF). The physical ports are identified as SP1 and SP2. There are two logical ports identified as the primary serial port at Locations 03F8–03FFH (IRQ4) and the alternate serial port at Locations 02F8–02FFH (IRQ3). SP1 is configured by POS Register 0102H, Bits 2 and 3. Note that Bits 2 and 3 are overridden in Extended Mode. For more information, see Section 9.0, Extended Setup Facility.

- **Micro Channel Setup**

Figure 33 defines the bits for POS Registers 0091H, 0094H, and 0096H. POS Register 0091H, a read-only register, is used to determine if the PVGA, the system board, or a Channel adapter is present in the systems board peripherals. The Card Select Feedback $\overline{\text{CDSFDBK}}$ is set to zero when the address space of the adapter is accessed. Bit 0 of 0091H is set to one whenever $\overline{\text{CDSFDBK}}$ is asserted or when the system board I/O functions are accessed by an I/O cycle.

- **Video Setup**

The Video Graphics device, system board peripherals and Channel adapters are configured or enabled by specific bit settings in Registers 0094H and 0096H. Bits 5 and 7 of Register 0094H configures Setup Mode and System Board Setup Mode, respectively. Bit 3 of Register 0096H enables Adapter Setup Mode.

Important

Only one category of device can be in Setup Mode at a time. If more than one is in Setup Mode, bus conflicts occur.

11

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PARALLEL PORT MODE		PARALLEL PORT SETUP		PARALLEL PORT		SERIAL PORT SEL		SERIAL PORT (SP1)		FLOPPY CONTROL		SYSTEM BOARD IO	
PC/AT COMP	EXT	-	-	ENA	DIS	SP1= PRIM	SP1= ALT	ENA	DIS	ENA	DIS	ENA	DIS

0102H

6	5	PARALLEL PORT SETUP
0	0	PP1 3BC-Fh
0	1	PP2 378-Bh
1	0	PP3 278-Bh
1	1	Undefined

RESERVED	DET2	DET1	RESERVED	SYS BD MEM	
1	0	1	1	ENA	DIS

0103H

= Nonprogrammable

FIGURE 32. POS REGISTER FORMATS (0102H and 0103H)

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED	CARD SEL FEEDBACK	
-	YES	NO

0091H Read Only

SYS BOARD		RESERVED		VGA ENABLE		RESERVED									
ENA (NMI)	Setup Mode	-	-	ENA (NMI)	Setup Mode	-	-	-	-	-	-	-	-	-	-

0094H Read/Write

RESET CHANNEL		RESERVED						ADAPTER SETUP		CARD SELECT		
RSET	-							ENA	DIS	-	-	-

0096H Read/Write

2	1	0	CARD SELECT SLOT
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

= Default

FIGURE 33. POS REGISTER FORMATS (0091H, 0094H, and 0096H)

6.0 SYSTEM CONTROL REGISTERS

The WD6000 has two IBM MC-conmpatible system control registers at 0061H (Control Port B) and 0092H (Control Port A). These ports are defined in Figures 34 and 35.

See Section 10.0 for details of other control registers.

7.0 COPROCESSOR INTERFACE

The coprocessor support function supplies error and control signals between the CPU and coprocessor, if any. An error signal from the coprocessor generates Interrupt IRQ13 in the WD6000. This causes the busy signal to the CPU to be held in the busy state. The interrupt and busy signals are cleared by writing 00H to the Coprocessor Clear Busy register, 00F0H. This interface also holds $\overline{BUSY386}$ low during power on reset to initiate self test on the 80386 processor.

For further information, refer to the Pin Table. For an interface to the Weitek 3167 and competition, also refer to the Pin Table.

8.0 EXTERNAL DEVICE ENABLE

The WD6000 enables the following external devices:

Keyboard/Auxiliary Controller (8742)

- Floppy Disk Controller
- Parallel Port
- Serial Ports
- VGA Video
- Real-time Clock/CMOS RAM
- Coprocessor
- Port A/B decodes (programmable decodes)

In general, an $\overline{IOR}$ or $\overline{IOW}$ to the address ranges shown in the I/O map in Table 1 activates the various chip select lines. The WD6000 control interface is shared by the Channel. The System Board Setup Functional Block Diagram in Figure 32 indicates the selection of the floppy disk controller $\overline{FDCCS}$, the parallel port controller $\overline{PPCS}$, and Serial Ports 1 $\overline{SERCS1}$ and 2 $\overline{SERCS2}$, by enabling the appropriate POS registers.

The keyoard/auxiliary controller is selected through $\overline{CS8742}$ when the keyboard data port is accessed at location 0060H, or when a read or write to the keyboard command/status port is executed at location 0064H. The coprocessor is selected through $\overline{NPS1}$ when the coprocessor ports are addressed at Locations 00F8–00FFH. $\overline{CSA}$ and $\overline{CSB}$ are configurable select lines controlled by Ports A and B. See Section 9.0 for a description of the other control registers.

11

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PARITY CHECK		CHAN CHECK		TIMER2 STATE		REFERSH TOGGLE		CHAN CHECK		PARITY CHECK		SPKR		TIMER2 GATE	
ERR	OK	ERR	OK	-		-		DIS	ENA	DIS	ENA	ENA	DIS	DIS	ENA

READ

RESET IRQ0		RESERVED	CHAN CHECK		PARITY CHECK		SPKR		TIMER2 GATE	
RSET	ENA	-	DIS	ENA	DIS	ENA	ENA	DIS	ENA	DIS

WRITE

FIGURE 34. SYSTEM CONTROL REGISTER FORMATS (0061H)

SYSTEM STATUS (SYSSTA)		RESERVED	WATCHDOG TIMEOUT		PASSWORD SEC LOCK		RESERVED	ALTERNATE A20		ALTERNATE HOT RST	
-		-	YES	NO	YES	NO	-	YES	NO	RST	NO

7	6	SYSTEM STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

GATE A20 A20=0

Note: Read/Write in WD6000
Write-Only in WD6010.

= DEFAULT

FIGURE 35. SYSTEM CONTROL REGISTER FORMATS(0092H READ/WRITE)

9.0 PERIPHERAL BUS CONTROL

The Peripheral Bus Control generates control signals that interface with the peripheral devices, and are enabled by the External Device Enable function to the CPU complex. $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ encode the information on the type of Channel bus cycle, as shown in Table 6.

M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	BUS CYCLE TYPE
0	0	0	Interrupt Acknowledge
0	0	1	IO Read
0	1	0	IO Write
0	1	1	No Cycle
1	0	0	System CPU Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	No Cycle

TABLE 6. CHANNEL COMMAND ENCODING

10.0 EXTENDED CMOS RAM INTERFACE AND EXTENDED SETUP FACILITY

The WD6000 provides external signals that are related to the Extended CMOS RAM (ECR) and the Extended Setup Facility (ESF). The WD6000 shares the implementation of the ECR and ESF with the WD6010. Figure 36 is a block diagram of the ECR and ESF, indicating how functions are divided between the WD6000 and the WD6010.

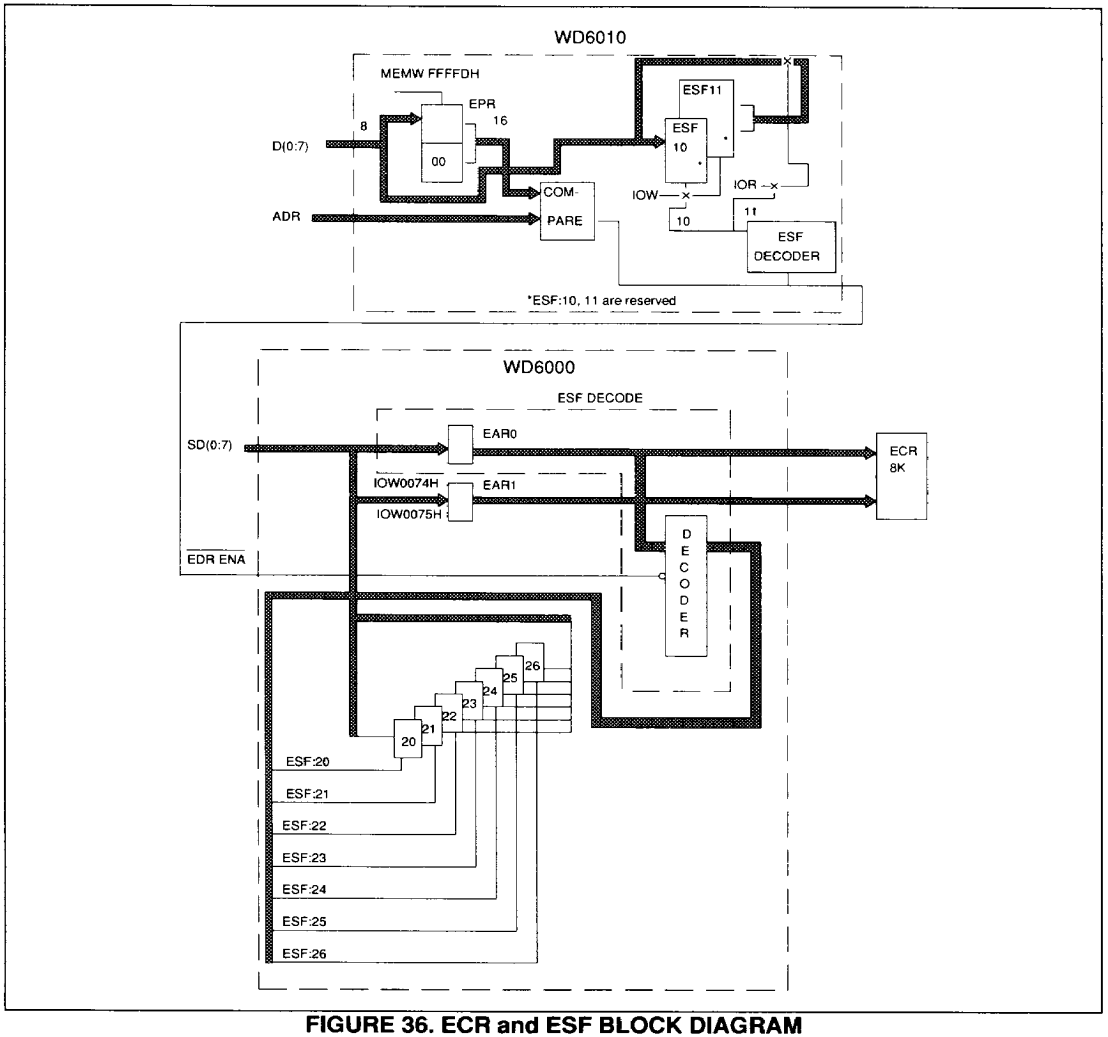


FIGURE 36. ECR and ESF BLOCK DIAGRAM

10.1 EXTENDED CMOS RAM (ECR) INTERFACE

The ECR supports Real-Time Clock (RTC) access and additional storage for POS and the ESF parameters needed for large systems. The RTC function is accessed through I/O Ports 0070H and 0071H. Port 0070H is used to point to the internal register or RAM location. Refer to Figure 37. Port 0071H is the read/write data port. Refer to the IBM Technical Reference for the byte definitions of the CMOS RAM.

The ECR interface allows an additional 8K bytes for storage of POS and/or additional system parameters. This function is accessed through Ports 0074H, 0075H, and 0076H when the RTC CMOS address port (0070H) is set to 8DH. Ports 0074H (EAR0) and 0075H (EAR1) are used to set the desired RAM address. The ECR address bus (CMOSA), consists of EAR0 (the LSB of the ECR address), and bits 0–4 of EAR1 (the MSB of the ECR address). Port 0076H is the data port.

10.2 EXTENDED SETUP FACILITY (ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable ($\overline{\text{EDRENA}}$) output from the WD6010 to the WD6000. It is designed to extend the configuration architecture established with the POS features. See Figure 38 for an ESF overview.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
NMI		RESERVED		RT/CMOS ADDRESS											
DIS	ENA	-		MSB		-		-		-		-		LSB	

= DEFAULT

FIGURE 37. RTC/CMOS ADDRESS PORT REGISTER (0070H)

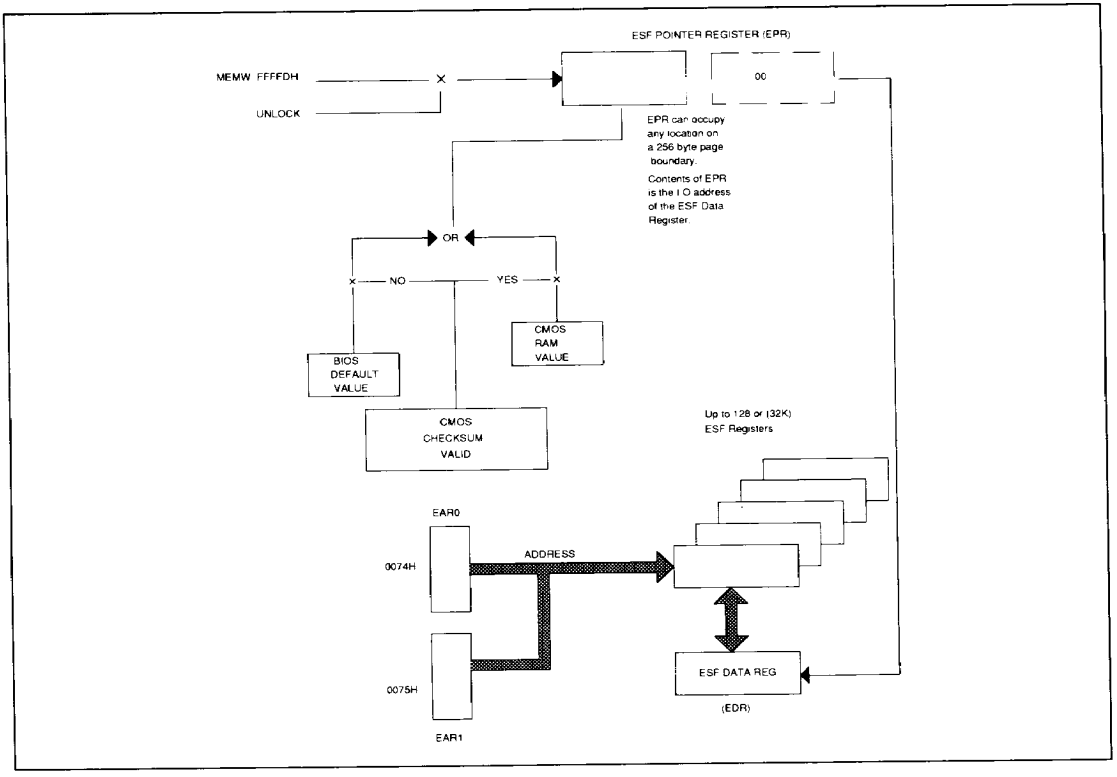


FIGURE 38. EXTENDED SETUP FACILITY OVERVIEW

ESF supports:

- Memory Map Control Registers
- Additional physical serial port
- Programmable Port Enables A and B
- External DRAM control configuration
- Customer specified enhancements that could include:
  System Identification
  System Version
  Miscellaneous system board features

10.2.1 ESF Access

ESF is based on an "alternate I/O space" concept similar to how IBM has implemented their Extended CMOS RAM feature. ESF space (128 locations expandable to 32K) is accessed through a single "real I/O space" window called the ESF Data Register (EDR). ESF space may be implemented as either word or byte-wide at the discretion of the designer.

The EDR is pointed to by the software configurable (write only) ESF Pointer Register (EPR) located in the WD6010. The EPR is loaded by writing to memory location FFFFDH or FFFFFDH (normally a PROM). The power-on default location for the EDR is located at IO address 0700H.

The following procedure is recommended for modifying the EPR:

1. Set the value 8DH in Port 0070H to disable $\overline{\text{NMI}}$.
2. Read the System Control Port B at 0061H and test for a change in the state of Bit 4 (Refresh Toggle) to synchronize with the refresh circuitry.
3. Read EAR0 at 0074H (normally write-only) to unlock the EPR.
4. Write the new value into the EPR (FFFFDH). This locks the EPR again.
5. Enable $\overline{\text{NMI}}$ if required.

Note that the EPR is locked when written or on the next refresh cycle, whichever occurs first.

The value in the EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K IO space of the CPU from 0400H to FF00H.

To address the ESF I/O space:

1. Write the value 8DH to port 0070H to disable $\overline{\text{NMI}}$.
2. Write the address value to EAR0 at 0074H (and EAR1 if expanded ESF is being used).
3. Issue an I/O Read or Write command to EDR Address.

The selected ESF register is determined by decoding the EAR0 (and EAR1) address value.

10.2.2 ESF Address Maps

The lower 64 bytes (EAR0 = 00H–3FH) are reserved for Western Digital functions and features. The upper 64 bytes (EARO = 40H–7FH) are for customer use (see Table 7). All functions using ESF must include Bit 7 in the decode. Bit 7 of EAR0 must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 locations, set EAR0 Bit 7 to 1 and write the second ESF address byte to EAR1.

ESF ADDRESS	FUNCTION
00H-0FH	System Reserved
10H-1FH	System board core functions
20H-3FH	System board peripheral functions

TABLE 7. ESF GENERAL USAGE MAP

The ESF address map in a WD6500 and WD6400SX(LP) system environment is shown in Table 8.

ESF ADDRESS	FUNCTION	R/W	WD6500 DEVICE	WD6400SX(/LP) DEVICE
0-001FH	Reserved	-	-	-
20H	Peripheral Configuration	R/W	WD6000	WD6000
21,24H	Port A, B Control	R/W	WD6000	WD6000
22,25H	Port A, B Address (LSB)	R/W	WD6000	WD6000
23,26H	Port A, B Address (MSB)	R/W	WD6000	WD6000
30-3FH	Reserved	-	-	-
40-7FH	Customer-specified	-	-	-
0180H	Memory Configuration	R/W	WD6030	WD6036SX (/LP)
0181H	Memory Size Register	R/W	WD6030	WD6036SX (/LP)
0182H	Bank Enable Register	R/W	WD6030	WD6036SX (/LP)
0183H	Split Address Extension	R/W	WD6030	N/A
0184H	Memory Window Bank 0	R/W	WD6030	WD6036SX (/LP)
0185H	Memory Window Bank 1	R/W	WD6030	WD6036SX (/LP)
0186H	Memory Window Bank 2	R/W	WD6030	WD6036SX (/LP)
0187H	Memory Window Bank 3	R/W	WD6030	WD6036SX (/LP)
0188H	CAS Pulse Width	R/W	WD6030	WD6036SX (/LP)
0189H	RAS Pre-Charge Delay	R/W	WD6030	WD6036SX (/LP)
018AH	RAS Pulse Width[1] - RAS to CAS Delay [2]	R/W	WD6030	WD6036SX (/LP)
018BH	RAS Access Time[1] -PSRAM Chip Select[2]	R/W	WD6030	WD6036SX (/LP)
018CH	Enhanced Addressing	R/W	WD6010	N/A
018DH	Reserved	-	-	-
018EH	Reserved	-	-	-
018FH	System Control Register[1] System Configuration[2]	R/W ***	WD6030	WD6036SX (LP)

Notes:
1. WD6500 implementation only.
2. WD6400SX(/LP) implementation only.

*** Dependent on the state of the UCHMSTER and A20GTX signals at reset.

TABLE 8. ESF ADDRESS MAP IN A WD6500 or WD6400SX (LP) SYSTEM ENVIRONMENT

10.2.3 Peripheral Configuration Register (PCR)

The PCR is assigned to ESF location 20H. It allows the additional serial port, SP2, to be configured. When PCR Bit 0 = 1 (Extended Mode enabled), Bits 2 and 3 in the System Board Setup register (0102H) are overridden. Figure 39 shows the PCR format.

10.2.4 Port A/B Decodes

Ports A and B are identical device-enable ports that are configurable by software. The 16-bit starting I/O address, port depth (up to 128 bytes), programmable wait state logic, and enable/disable control are provided by Ports A and B. The starting address must be on an even binary multiple of the port depth. Figure 40 shows the ESF format for Port A and B Control Registers.

11.0 NMI CONTROL

The NMI Control logic generates an $\overline{NMI}$ signal when any of the following events occur:

1. Channel $\overline{CHCK}$ line asserted (Bit 3 = 0 of Control Port B at 0061H).
2. DRAM parity error (Bit 2 = 0 of Control Port B).
3. Watchdog Timer time-out (Enabled by programming the Timer).
4. System channel time-out.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
TIMER		RESERVED				SP1		SP1		SP2		MODE			
TEST	NORM	-		-		-		PRI	ALT	ENA	DIS	ENA	DIS	EXTD	IBM

= DEFAULT

FIGURE 39. PERIPHERAL CONFIGURATION REGISTER FORMAT (ESF:20 READ/WRITE)

PORT		COMMAND WIDTH SELECT			RESERVED	I/O SPACE DEPTH		
ENA	DIS	2	1	0	-	2	1	0

6	5	4	WIDTH (NS) [1]
0	0	0	70
0	0	1	140
0	1	0	280
0	1	1	420
1	0	0	560
1	0	1	700
1	1	0	840
1	1	1	980

[1] Any I/O device may extend the cycle beyond these times given by driving CDCHRDY inactive.

2	1	0	BYTES
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	Reserved

FIGURE 40. PORT A OR B CONTROL REGISTER (ESF:21, ESF:24 READ/WRITE - TYPICAL)

12.0 TECHNICAL SPECIFICATIONS

12.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for the device are listed below. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}-V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}-0.3	V_{DD}+0.3	V
Bias on output pin	V_{OABS}	V_{SS}-0.3	V_{DD}+0.3	V
Storage Temperature	T_S	-40	125	°C

12.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Power Dissipation	P_W	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

12.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input capacitance @ f_c=1 MHz	C_I	-	5	pF
*I/O capacitance	C_{IO}	-	10	pF
Logic high input voltage	V_{IH}	2.0	-	V
Logic low input voltage	V_{IL}	-	0.8	V
*Input leakage	I_{IL}	-	±10	µA
*Tri-state output leakage	I_{LO}	-	±30	µA
*I/O pin leakage	I_{IOL}	-	±40	µA
OUTPUTS MHZ14 AND $\overline{CHCK}$				
*Source current @ V_{OH}=2.4 V	I_{OH}	4	-	mA
*Sink current @ V_{OL}=0.4 V	I_{OL}	24	-	mA
OUTPUTS $\overline{CDSETUP}$ [0:07]				
Source current @ V_{OH}=2.4 V	I_{OH}	1	-	mA
Sink current @ V_{OL}=0.4 V	I_{OL}	6	-	mA
ALL OTHER OUTPUTS				
*Source current @ V_{OH}=2.4 V	I_{OH}	1	-	mA
*Sink current @ V_{OL}=0.4 V	I_{OL}	4	-	mA

***Notes:**

Pins $\overline{INT1EN}$ and $\overline{INT2EN}$ have internal pulldowns of 10 K ohms nominal value. Measurement of input capacitance and input leakage values on these pins will be affected by these resistances.

11

$\overline{CHCK}$ is an open drain output. An external pullup is required. Only the sink current value applies.

$\overline{NMI}$ is an open drain output. An external pullup is required. Only the sink current value applies.

13.0 TIMING

See following tables.

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	$\overline{S0}$, $\overline{S1}$(0:1) hold from $\overline{CMD}$ on	30	-	-
T2	SA(0:15) setup to $\overline{CMD}$ on	60	-	-
T3	SD(0:7) setup to $\overline{CMD}$ on	-	25	1
T4	SA(0:15) hold from $\overline{CMD}$ off	0	-	-
T5	SD(0:7) hold from $\overline{CMD}$ off	0	-	-
T6	$\overline{CDSETEN}$ hold from $\overline{CMD}$ on	30	-	-
T7	$\overline{PROMCSL/H}$ setup to $\overline{CMD}$ on	25	-	-
T8	$\overline{PROMCSL/H}$ hold from $\overline{CMD}$ off	0	-	-
T9	M/$\overline{IO}$ hold from $\overline{CMD}$ on	30	-	-
T10	$\overline{CDSFDBK}$ setup to $\overline{CMD}$ on	10	-	-
T11	$\overline{EDRENA}$ setup to $\overline{CMD}$ on	25	-	-
T12	$\overline{EDRENA}$ hold from $\overline{CMD}$ on	0	-	-
T13	$\overline{IOR/W}$, $\overline{MEMRD/WR}$ delay from $\overline{CMD}$ on	40	-	-
T14	$\overline{MEMRD/WR}$ pulse width	-	-	2
T14	$\overline{IOR/W}$, $\overline{CS8742}$	160	-	-
T14	$\overline{IOR/W}$, $\overline{FDCCS}$	90	-	-
T14	$\overline{IOR/W}$, $\overline{SERCS1}$, $\overline{SERCS2}$	125	-	-
T14	$\overline{IOR/W}$, $\overline{PPCS}$	125	-	-
T14	$\overline{IOR/W}$, $\overline{NPS1}$	90	-	-
T14	$\overline{IOR/W}$, $\overline{CSA}$, $\overline{CSB}$	70	980	-
T15	$\overline{IOR/W}$, $\overline{MEMRD/WR}$ off to $\overline{CMD}$ off	60	-	-
T16	$\overline{IODTR}$ setup to $\overline{IODEN}$ on	5	-	-
T17	$\overline{IODTR}$ hold from $\overline{IODEN}$ off	5	-	-
T18	$\overline{IODEN}$ on from $\overline{CMD}$ on	5	-	-
T19	$\overline{IODEN}$ hold from $\overline{CMD}$ off	5	-	-
T20	IODCBA on from $\overline{CMD}$ on	40	-	-
T21	IODCBA off to $\overline{IOW/R}$, $\overline{MEMRD/WR}$ off	5	-	-
T22	$\overline{S0}$(1:0) on to IORDY off	-	20	-
T23	IORDY on to $\overline{CMD}$ off	60	-	-
T24	SD(0:7) read access from $\overline{IOR}$ on	25	-	-
T25	SD(0:7) read hold from $\overline{IOR}$ off	5	-	-
T26	CS (ext.dev) setup to $\overline{IOR/R}$, $\overline{MEMRD/WR}$ on	70	-	-
T27	CS (ext.dev) hold from $\overline{IOR/W}$, $\overline{MEMRD/WR}$ on	25	-	-
T28	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ delay from $\overline{CMD}$ on	40	-	-
T29	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ off to $\overline{CMD}$ off	60	-	-
T30	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ pulse width	325	-	-
T30A	CMOSA(0:12) on from $\overline{CMD}$ on	40	-	-
T31	CDSETUP(0:7) hold from $\overline{CMD}$ on	30	-	-

NOTES: 1. THE WD6000 allows SD bus valid to be later than CMD active.
2. T21 for $\overline{MEMRD/WR}$ follows $\overline{CMD}$ input.

TABLE 9. PERIPHERAL BUS CYCLE (IN NSEC)

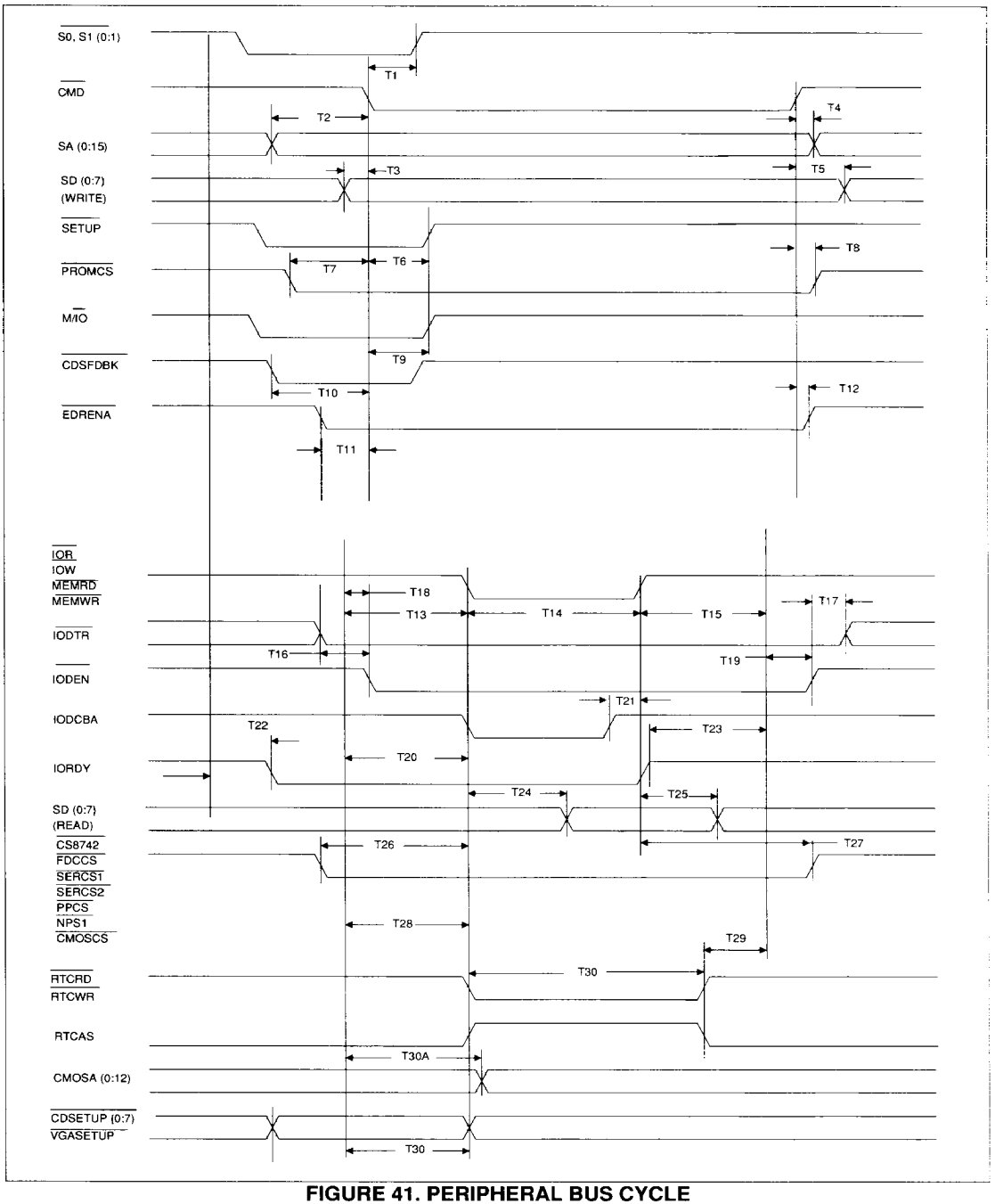


FIGURE 41. PERIPHERAL BUS CYCLE

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	MHZ28 period	35	-	-
T2	MHZ28 low time	17	-	-
T3	MHZ28 high time	16	-	-
T4	MHZ30 period	33	-	-
T5	MHZ30	18	-	-
T6	MHZ30 high time	15	-	-
T7	MHZ14 period	70	-	-
T8	MHZ14 high time	20	-	-
T9	MHZ14 low time	20	-	-
T10	CLK387 period	105/100	-	1
T10F	CLK387 rise time	-	10	3
T10R	CLK387 fall time	-	10	3
T11	CLK387 high time	28	-	4
T12	CLK387 low time	62	-	4
T13	CLK8742 period	105/100	-	1
T14	CLK8742 low time	33	-	-
T15	CLK8742 high time	33	-	-
T16	$\overline{\text{REFREQ}}$ period	15 µs	-	2

NOTES: 1. Clock derived from 28.636 MHz, unless optional 30 MHz is used.
2. 50% duty cycle .
3. Rise and fall times are measured between 0.8 V and 2.0 V.
4. Clock low time measured at 1.0 V, clock high time measured at 3.6 V.

TABLE 10. CLOCK CYCLE TIMES (IN NSEC EXCEPT WHERE NOTED)

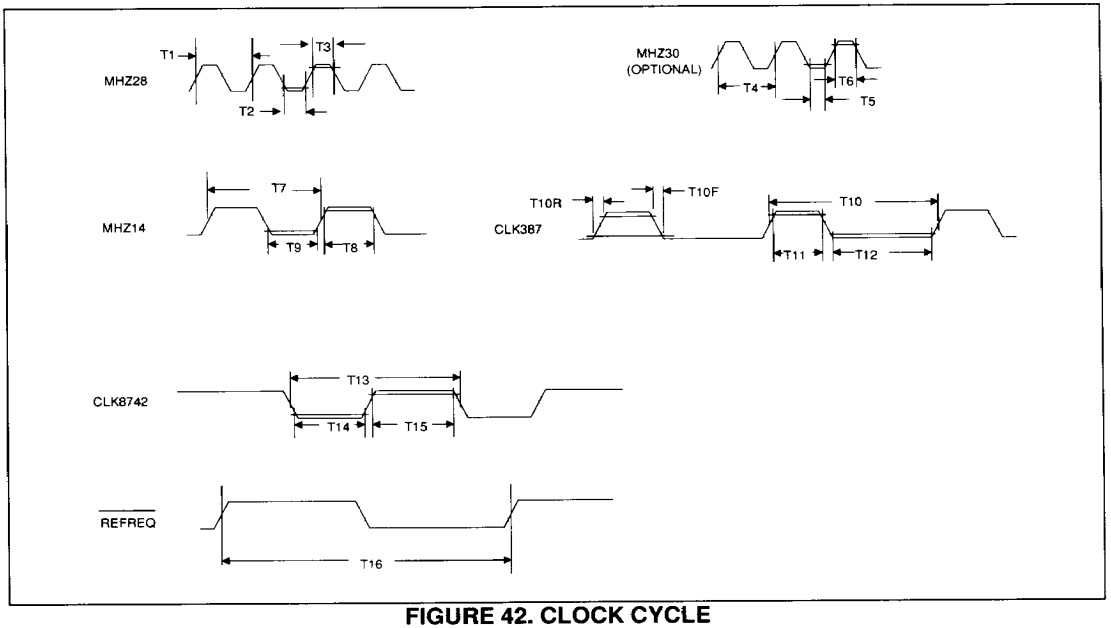


FIGURE 42. CLOCK CYCLE

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	INTR output delay	-	100	-
T2	INTR hold from INTACK on	10	32	1

NOTES: 1. Interrupt inputs must be held until the first Interrupt Acknowledge cycle begins.

TABLE 11. INTERRUPT CYCLE (IN NSEC)

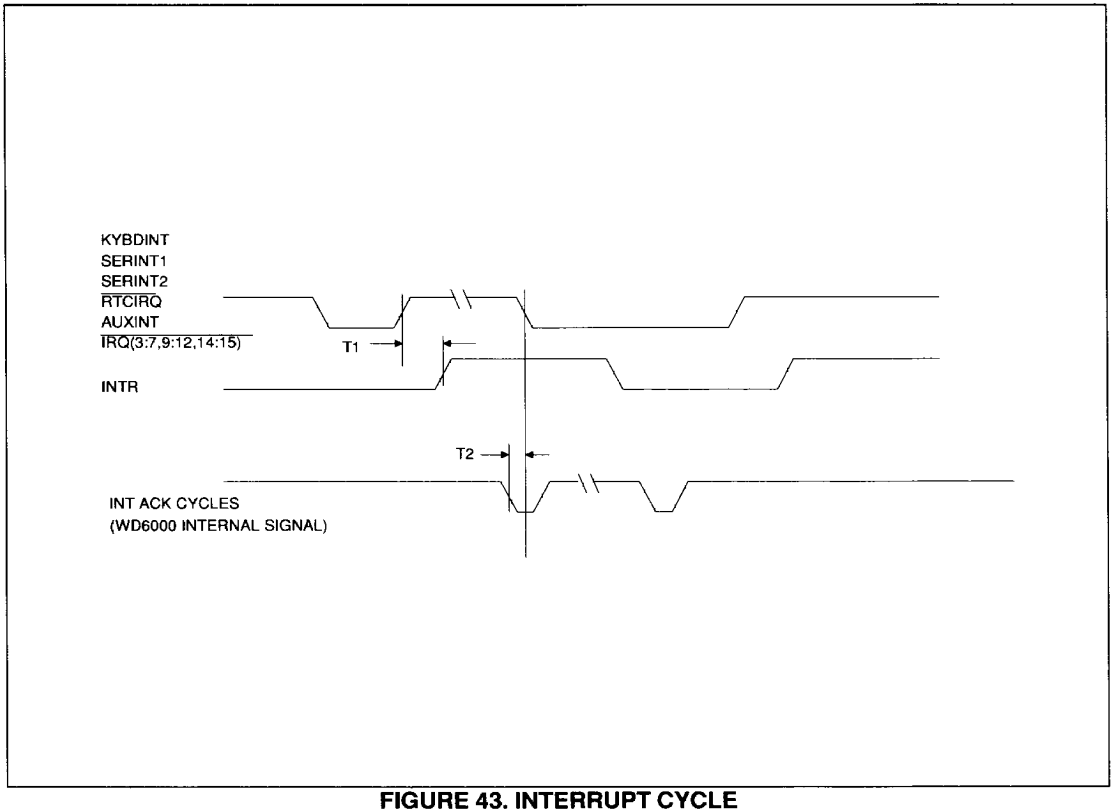


FIGURE 43. INTERRUPT CYCLE

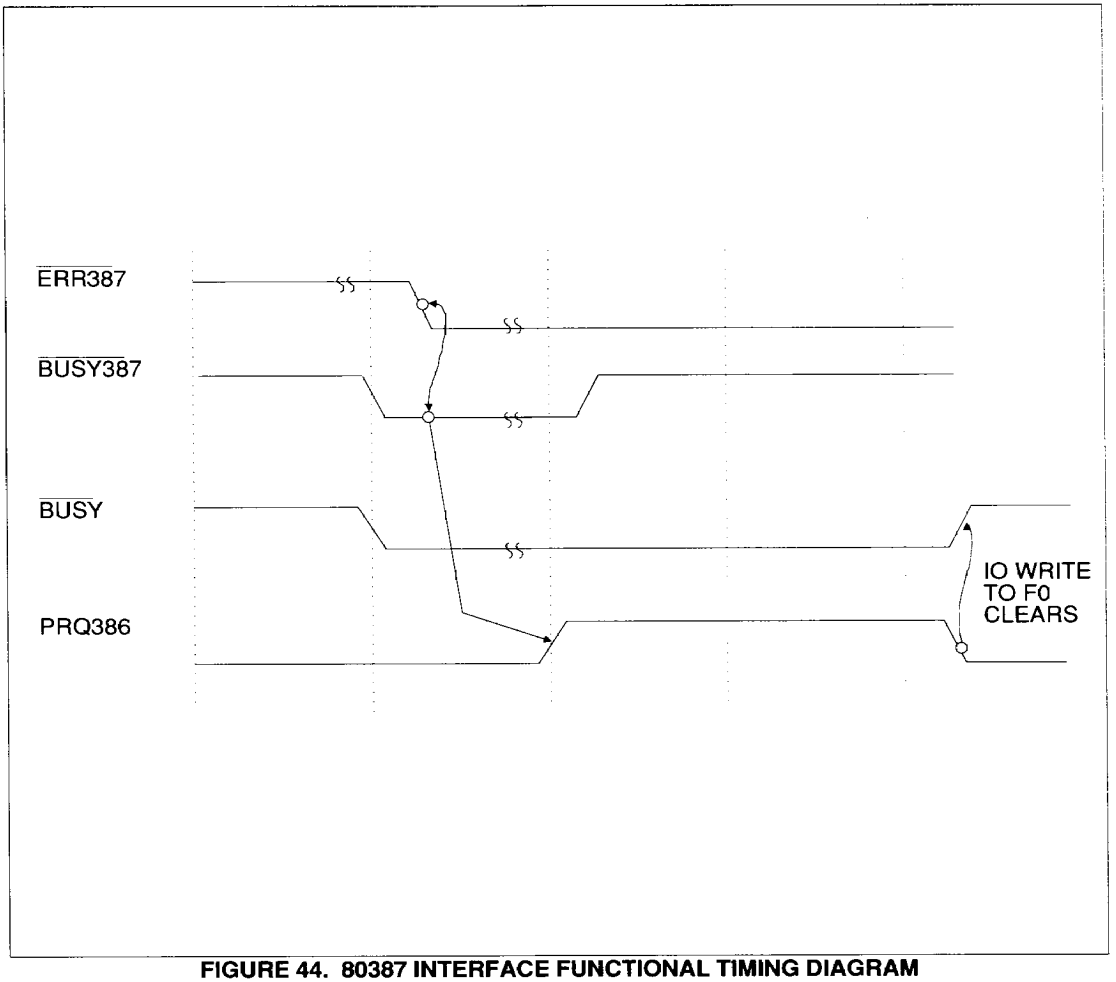
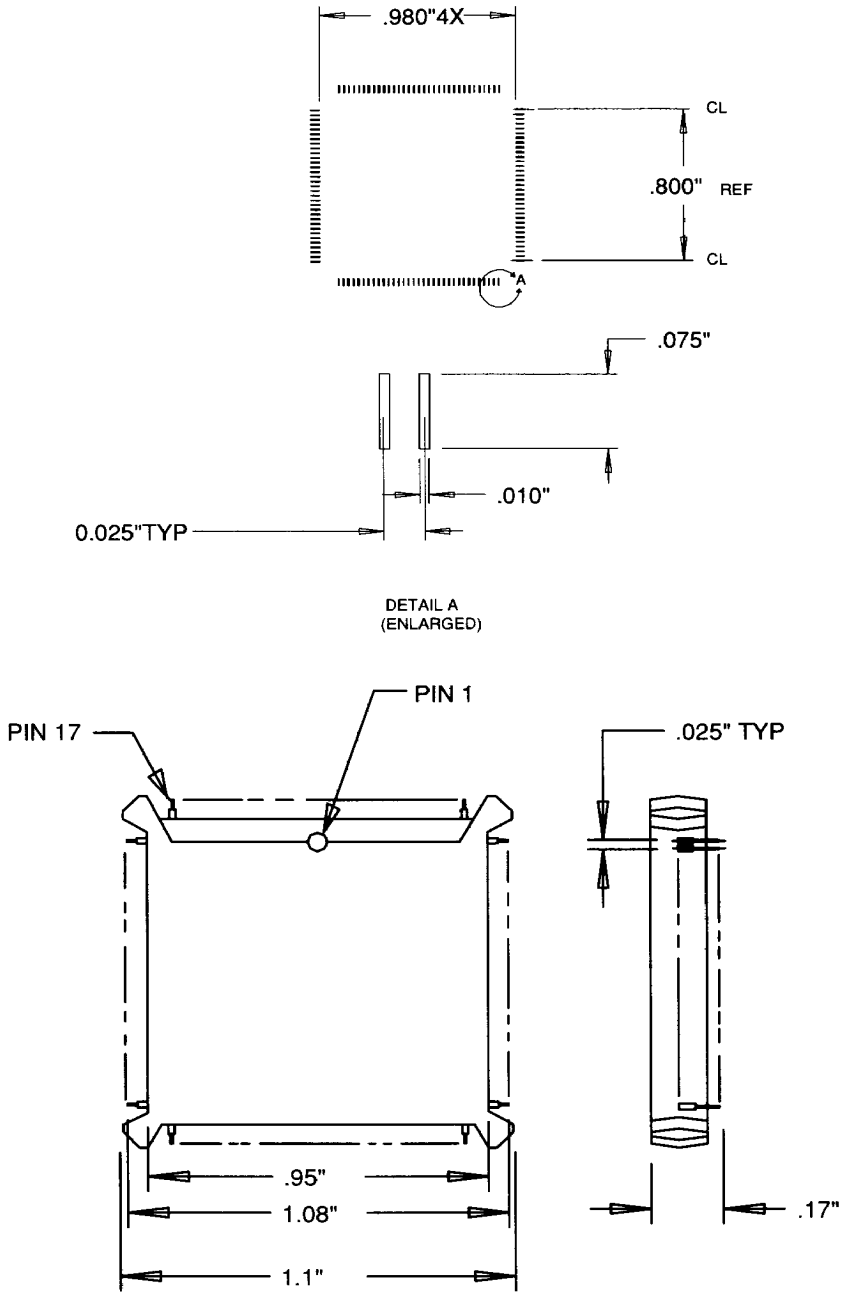
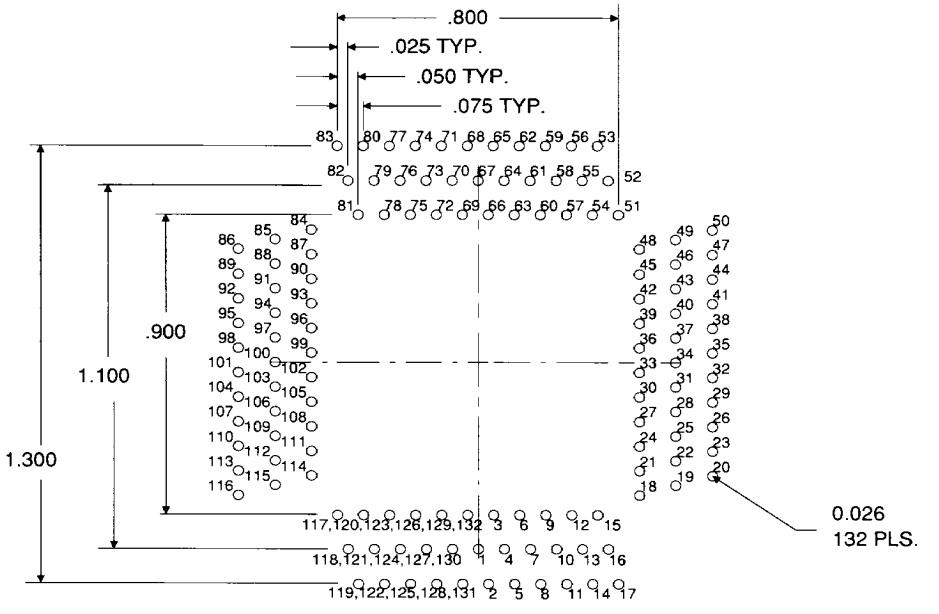


FIGURE 44. 80387 INTERFACE FUNCTIONAL TIMING DIAGRAM



FIFUEW 45. 132-PIN JEDEC FLAT PACK PACKAGING DIAGRAM



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

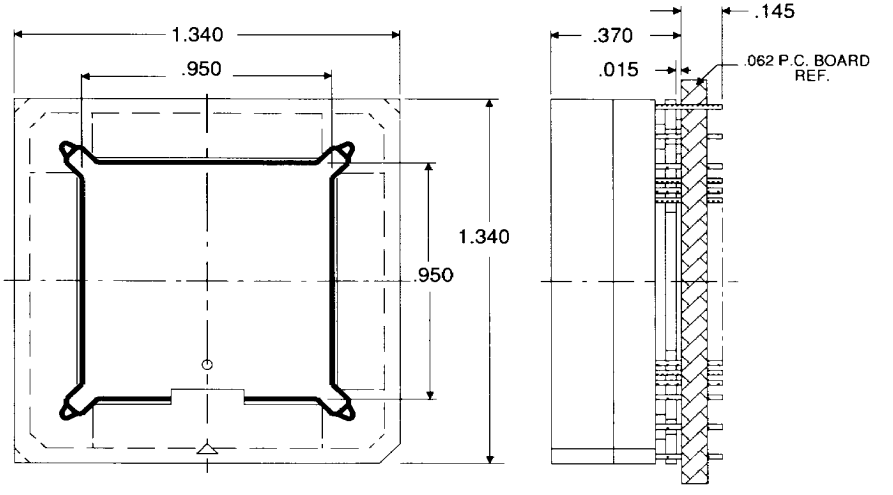


FIGURE 46. SOCKET DIAGRAM

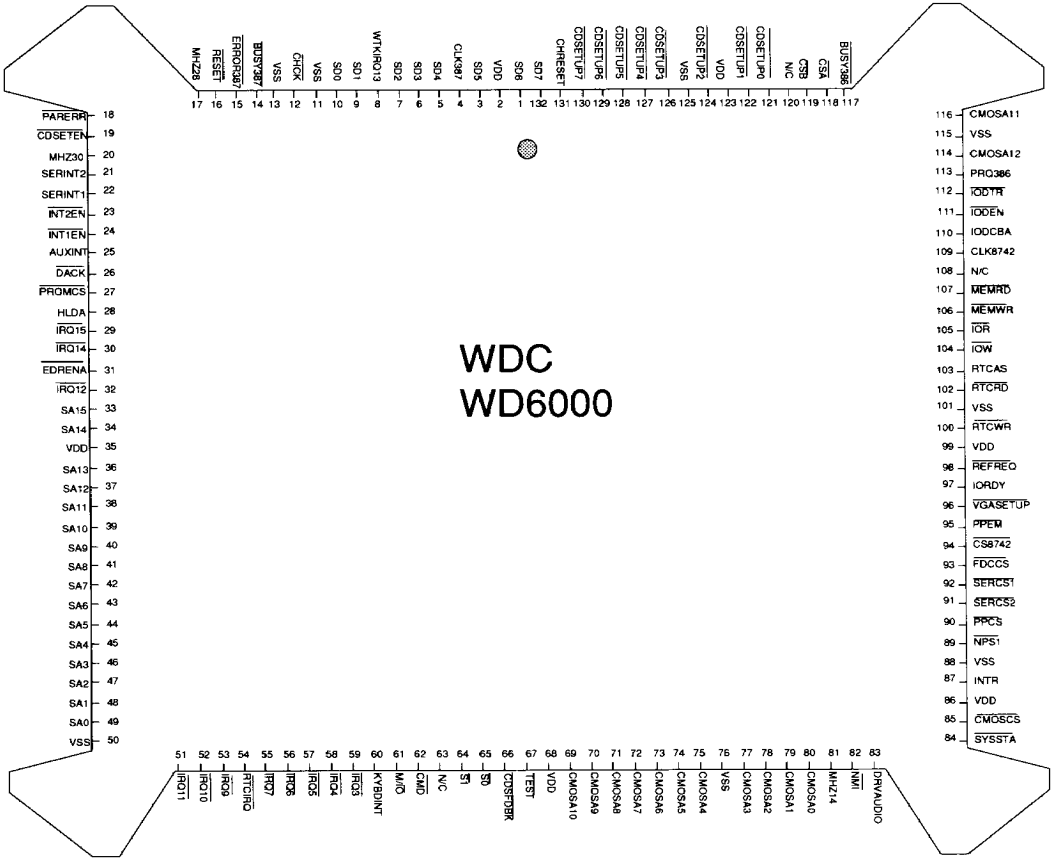


FIGURE 47. PIN LAYOUT DIAGRAM - TOP VIEW