FE6022
Address And Data Buffer Devices

- Provides Address and Data Buffers that interface to the Micro Channel *
- Meets Micro Channel AC/DC Specifications
- Contains Peripheral Bus Address and Data Buffers
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

The FE6022 devices form part of Western Digital's ® innovative FE6500 chip set, which facilitates the design and implementation of Model 70/80-compatible system boards. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, also reducing system cost and increasing system reliability.

The chip set contains two FE6022 devices, one configured as an Address Buffer device, and the other as a Data Buffer Device. Configuration is determined by a Mode pin. When this is zero, the device is configured as an address buffer; when it is one, the device is configured as a data buffer. The block diagram in Figure 1 illustrates a typical system using the FE6500 chip set, and shows the two FE6022 devices. Devices with bold outlines are available from Western Digital Corporation.

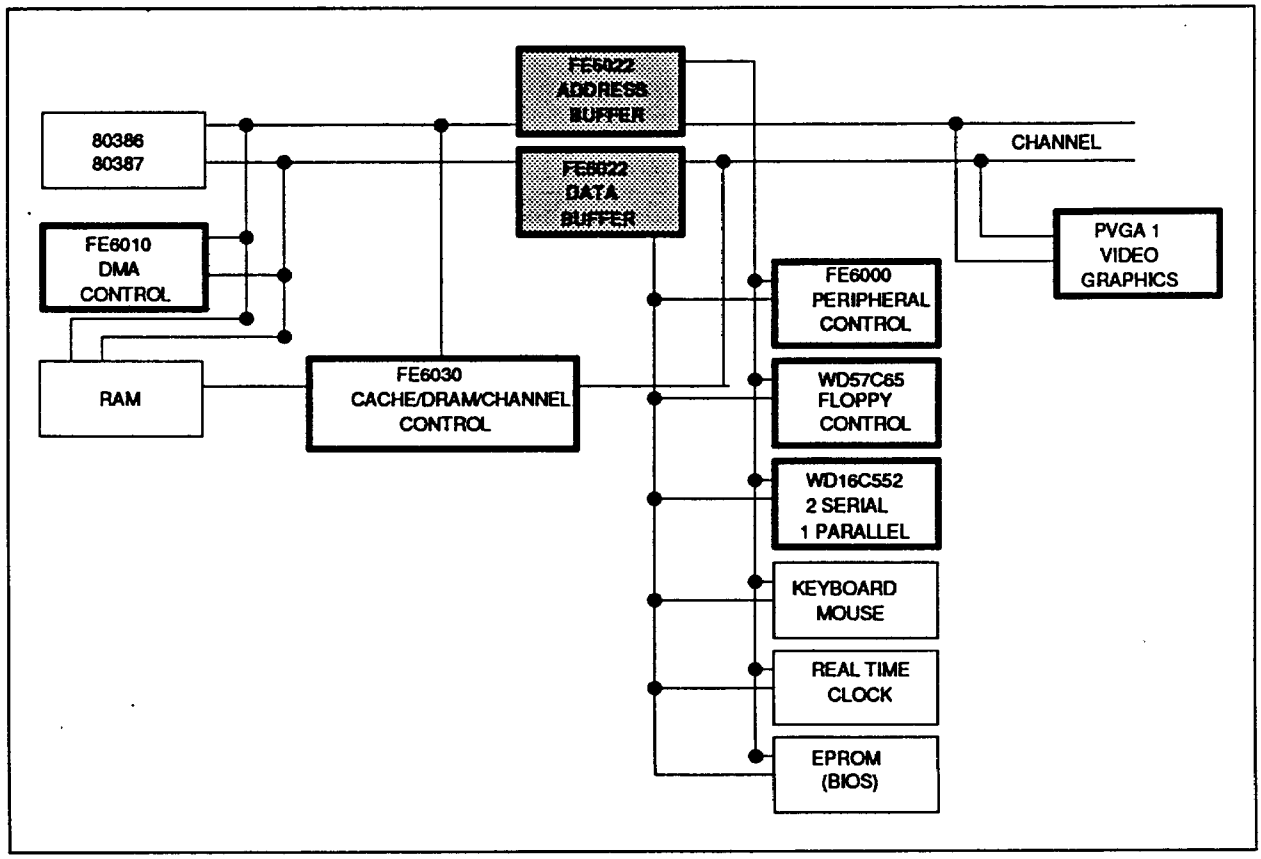

Figure 1. System Block Diagram

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WESTERN DIGITAL

Additional References

IBM PS/2 Model 70 Technical Reference Manual
IBM PS/2 Model 80 Technical Reference Manual
Intel* Microprocessor and Peripheral Handbook

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1.0 PIN DESCRIPTION

The signals assigned to the different pins are grouped according to their function, and discussed in more detail in Table 1.

1.1 Address Buffers

To configure the FE6022 as an address buffer, the Mode pin is tied to GND. In this mode, the FE6022 buffers the processor address signals from the Channel address bus. It also generates MADE24 signals, and PROM Chip Selects. In addition, the Address Buffer mode implements the Central Translator function for the Channel.

1.2 Data Buffers

To configure the FE6022 as data buffers, the Mode pin is tied to V_{DD}. The data buffers buffer the processor data bus from the Channel data bus. In this mode, the FE6022 performs Micro Channel Data Steering, and data swaps for 80386 and DMA operations.

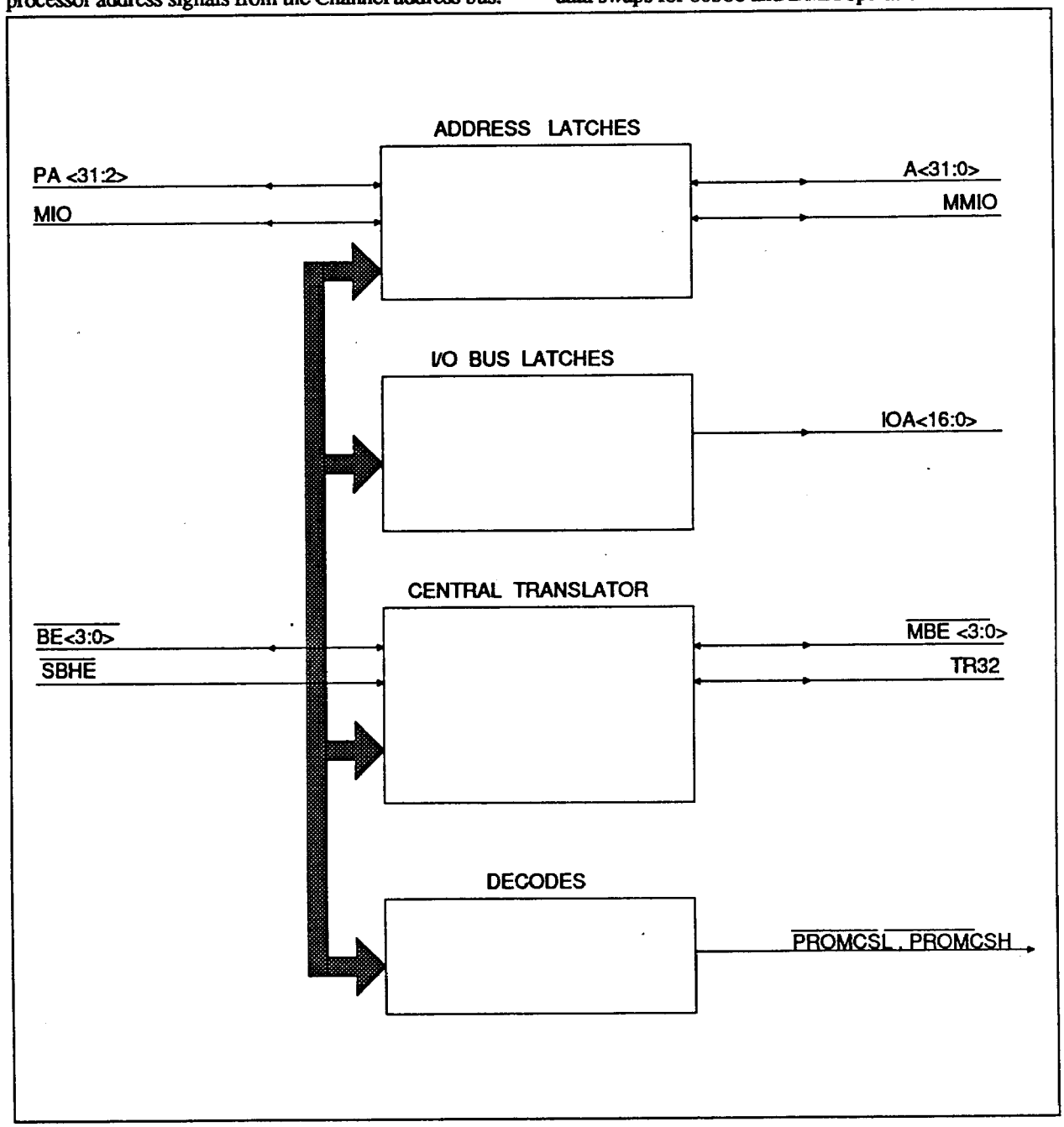


Figure 2 Address Buffer Mode Functional Block Diagram

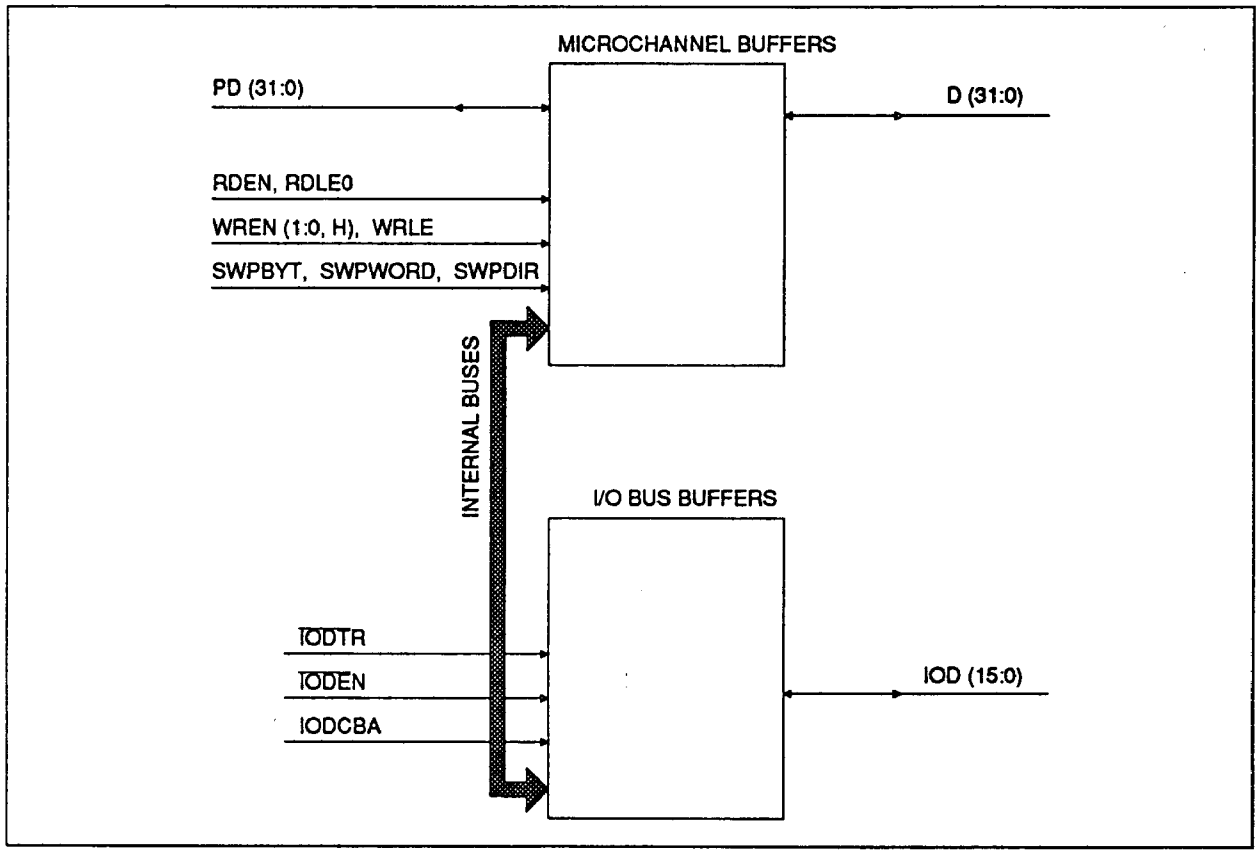


Figure 3 Data Buffer Mode Functional Block Diagram

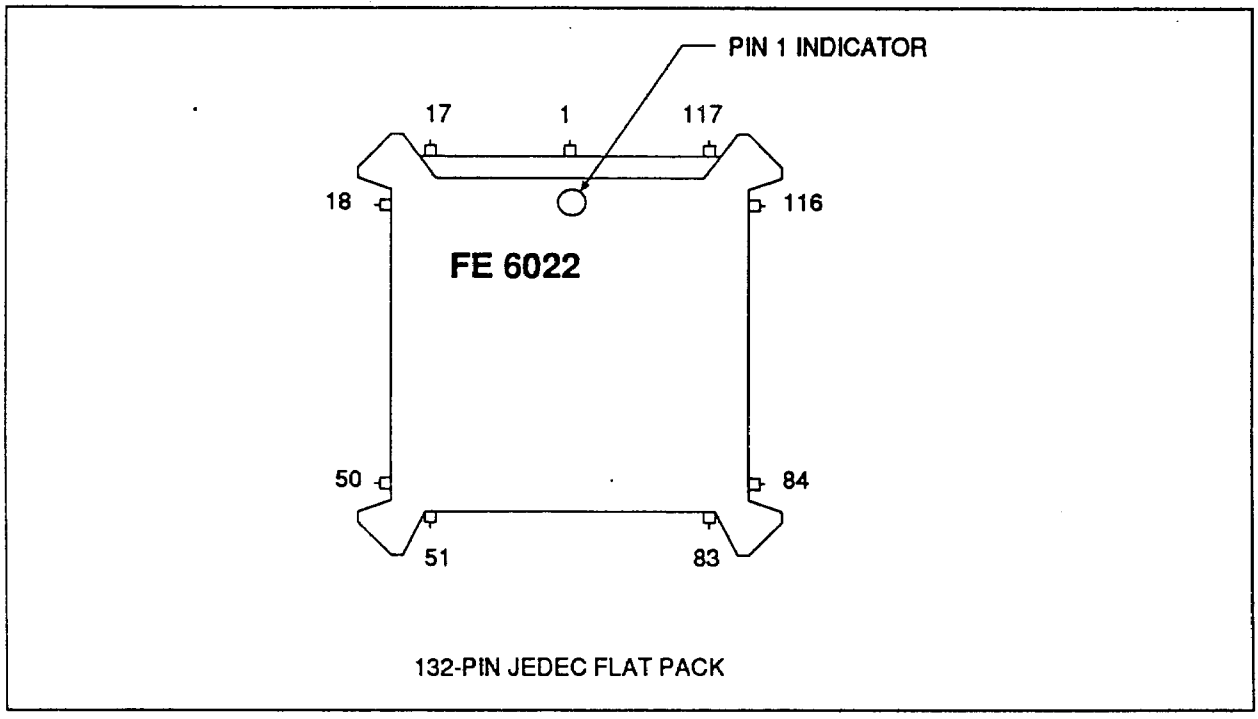


Figure 4. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	IOA9	34	A9	67	$\overline{TEST}$	100	V_{DD}
2	IOA8	35	V_{DD}	68	MMIO	101	PA20
3	V_{DD}	36	A10	69	UCHCMD	102	PA19
4	IOA7	37	A11	70	EOT	103	PA18
5	IOA6	38	V_{SS}	71	$\overline{PROMCSL}$	104	PA17
6	IOA5	39	A12	72	$\overline{PROMCSH}$	105	PA16
7	IOA4	40	A13	73	$\overline{MMC}$	106	PA15
8	IOA3	41	A14	74	$\overline{BE2}$	107	PA14
9	IOA2	42	A15	75	$\overline{BE3}$	108	PA13
10	IOA1	43	V_{SS}	76	V_{SS}	109	V_{SS}
11	IOA0	44	A16	77	$\overline{MBE0}$	110	PA12
12	MADE24	45	A17	78	$\overline{MBE1}$	111	PA11
13	TR32	46	V_{DD}	79	$\overline{MBE2}$	112	PA10
14	$\overline{CMDBUF}$	47	A18	80	$\overline{MBE3}$	113	PA9
15	A20GTX	48	A19	81	MIO	114	PA8
16	$\overline{S1}$	49	A20	82	BIAS	115	PA7
17	V_{SS}	50	V_{SS}	83	V_{DD}	116	V_{DD}
18	V_{SS}	51	V_{SS}	84	HLDA	117	V_{SS}
19	$\overline{S0}$	52	A21	85	$\overline{MMCMD}$	118	PA6
20	$\overline{CMD}$	53	A22	86	$\overline{SBHE}$	119	PA5
21	UCHMSTR	54	A23	87	V_{SS}	120	PA4
22	A0	55	A24	88	PA31	121	PA3
23	A1	56	A25	89	PA30	122	PA2
24	V_{DD}	57	V_{DD}	90	PA29	123	$\overline{BE1}$
25	A2	58	A26	91	PA28	124	$\overline{BE0}$
26	A3	59	A27	92	PA27	125	IOA16
27	V_{SS}	60	V_{SS}	93	PA26	126	IOA15
28	A4	61	A28	94	PA25	127	IOA14
29	A5	62	A29	95	PA24	128	IOA13
30	A6	63	A30	96	PA23	129	IOA12
31	A7	64	A31	97	PA22	130	IOA11
32	V_{SS}	65	V_{SS}	98	V_{SS}	131	IOA10
33	A8	66	MODE	99	PA21	132	V_{SS}

Table 1. Address Buffer Mode (Mode = 0) Pinout

PIN	–	NAME	PIN	–	NAME	PIN	–	NAME	PIN	–	NAME
1	–	IOD9	34	–	D9	67	–	$\overline{\text{TEST}}$	100	–	V_{DD}
2	–	IOD8	35	–	V_{DD}	68	–	RESERVED	101	–	PD20
3	–	V_{DD}	36	–	D10	69	–	RESERVED	102	–	PD19
4	–	IOD7	37	–	D11	70	–	RESERVED	103	–	PD18
5	–	IOD6	38	–	V_{SS}	71	–	RESERVED	104	–	PD17
6	–	IOD5	39	–	D12	72	–	RESERVED	105	–	PD16
7	–	IOD4	40	–	D13	73	–	RESERVED	106	–	PD15
8	–	IOD3	41	–	D14	74	–	RESERVED	107	–	PD14
9	–	IOD2	42	–	D15	75	–	RESERVED	108	–	PD13
10	–	IOD1	43	–	V_{SS}	76	–	V_{SS}	109	–	V_{SS}
11	–	IOD0	44	–	D16	77	–	RESERVED	110	–	PD12
12	–	$\overline{\text{IODEN}}$	45	–	D17	78	–	RESERVED	111	–	PD11
13	–	$\overline{\text{IODTR}}$	46	–	V_{DD}	79	–	RESERVED	112	–	PD10
14	–	$\overline{\text{WRLE}}$	47	–	D18	80	–	RESERVED	113	–	PD9
15	–	$\overline{\text{WRENH}}$	48	–	D19	81	–	RESERVED	114	–	PD8
16	–	$\overline{\text{WREN1}}$	49	–	D20	82	–	BIAS	115	–	PD7
17	–	V_{SS}	50	–	V_{SS}	83	–	V_{DD}	116	–	V_{DD}
18	–	V_{SS}	51	–	V_{SS}	84	–	SWPDIR	117	–	V_{SS}
19	–	$\overline{\text{WREN0}}$	52	–	D21	85	–	$\overline{\text{SWPWORD}}$	118	–	PD6
20	–	$\overline{\text{RDLE0}}$	53	–	D22	86	–	$\overline{\text{SWPBYT}}$	119	–	PD5
21	–	$\overline{\text{RDEN}}$	54	–	D23	87	–	V_{SS}	120	–	PD4
22	–	D0	55	–	D24	88	–	PD31	121	–	PD3
23	–	D1	56	–	D25	89	–	PD30	122	–	PD2
24	–	V_{DD}	57	–	V_{DD}	90	–	PD29	123	–	PD1
25	–	D2	58	–	D26	91	–	PD28	124	–	PD0
26	–	D3	59	–	D27	92	–	PD27	125	–	IODCBA
27	–	V_{SS}	60	–	V_{SS}	93	–	PD26	126	–	IOD15
28	–	D4	61	–	D28	94	–	PD25	127	–	IOD14
29	–	D5	62	–	D29	95	–	PD24	128	–	IOD13
30	–	D6	63	–	D30	96	–	PD23	129	–	IOD12
31	–	D7	64	–	D31	97	–	PD22	130	–	IOD11
32	–	V_{SS}	65	–	V_{SS}	98	–	V_{SS}	131	–	IOD10
33	–	D8	66	–	MODE	99	–	PD21	132	–	V_{SS}

Table 2. Data Buffer Mode (Mode=1) Pinout

2.0 PIN SIGNALS

PIN NO.	NAME	TYPE	FUNCTION
			FE6022 ADDRESS BUFFER MODE
16	A20GTX	I	ADDRESS BIT 20 GATE SIGNAL A20GTX gates Address Bit 20 of PA 20 from the processor. The signal is generated by the FE6010, and has no effect on the address when the DMA or Micro Channel master is generating the addresses. It is encoded in the following manner:
			HLDA **UCHMSTR** **A20GTX** **A20** **SOURCE DEVICE** 0 0 0 0 80386 0 0 1 PA20 80386 1 0 x PA20 DMA 1 1 x PA20 Micro Channel Master
20	UCHMSTR	I	CHANNEL MASTER This signal is generated by the CACP in the FE6010. When active, it indicates that a Channel master has control of the bus. It is used to control the direction of the address buffers.
84	HLDA	I	HOLD ACKNOWLEDGE The 80386 generates this signal in response to a HOLD signal from the DMA controller. When active, it indicates that the 80386 has relinquished control of the local bus.
19	$\overline{\text{CMD}}$	I	$\overline{\text{CHANNEL COMMAND}}$ This Channel Command signal generates the latch signal that latches the Channel addresses when a Channel master has the bus.
88	PA31	I/O	PROCESSOR ADDRESS BUS This is the local processor address bus on the motherboard, and interfaces directly with the 80386 address bus. It is an input for 80386/DMA cycles and output for master cycles.
89	PA30		
90	PA29		
91	PA28		
92	PA27		
93	PA26		
94	PA25		
95	PA24		
96	PA23		
97	PA22		
99	PA21		
101	PA20		
102	PA19		
103	PA18		
104	PA17		
105	PA16		
106	PA15		
107	PA14		
108	PA13		
110	PA12		
111	PA11		
112	PA10		
113	PA9		
114	PA8		
115	PA7		
118	PA6		
119	PA5		
120	PA4		
121	PA3		

PIN NO.	NAME	TYPE	FUNCTION
122 123 124	PA2 PA1 PA0	I/O	PROCESSOR ADDRESS BUS (CONT)
64 63 62 61 59 58 56 55 54 53 52 49 48 47 45 44 42 41 40 39 37 36 34 33 31 30 29 28 26 25 23 22	A31 A30 A29 A28 A27 A26 A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I/O I	CHANNEL ADDRESS BUS This Channel address bus interfaces directly to the Channel. It is an input during 80386/DMA cycles. Note that A0 is always an input, and is generated by the FE6030 during 80386/DMA cycles.
75 74 123 124	$\overline{BE3}$ $\overline{BE2}$ $\overline{BE1}$ $\overline{BE0}$	I/O	$\overline{BYTE\ ENABLES}$ These byte enables on the local bus interface directly with the 80386 byte enables. When the address flow is from the processor address bus to the Channel address bus, these signals generate Address Bit 1 (A1). A0 is generated in the FE6030. When the address flow is from the Channel address bus to the processor address bus, these signals are generated by a 32-bit master on the Channel or the central translator for a 16-bit master.
80 79 78 77	$\overline{MBE3}$ $\overline{MBE2}$ $\overline{MBE1}$ $\overline{MBE0}$	I/O	$\overline{CHANNEL\ BYTE\ ENABLES}$ These Channel byte enable signals interface directly to the $\overline{BE\ (3:0)}$ on the Micro Channel. During an 80386/DMA cycle, these signals are outputs. For a master cycle they are input signals.
14	TR32	I/O	TRANSLATE 32 The Translate 32 signal on the Channel is used in the central translator logic. When it is active, the central translator translates A0, A1, and $\overline{SBHE}$ to $\overline{BE\ (3:0)}$. TR32 is used for a 16-bit master communi-cating with a 32-bit slave.

PIN NO.	NAME	TYPE	FUNCTION
86	$\overline{SBHE}$	I	$\overline{SYSTEM\ BYTE\ HIGH\ ENABLE}$ The System Byte High Enable signal on the Channel interfaces directly to $\overline{SBHE}$ on the Channel. When the address flow is from the processor bus to the Channel bus, the FE6030 generates this signal as a decode of $\overline{BE\ (3:0)}$. When the address flow goes from the Channel bus to the processor bus, this signal is used in the central translator function.
82	MIO	I/O	LOCAL BUS MIO The MIO signal is on the local bus, and interfaces directly with the M/IO# signal on the 80386. When a Channel master accesses the system board DRAM, this signal is a latched version of the MMIO signal.
68	MMIO	I/O	CHANNEL MIO This signal interfaces directly with the Channel MIO signal, a delayed version of the $\overline{CMD}$ signal generated by the FE6000. When the 80386 or the DMA accesses the Channel, this signal is the same as MIO.
14	$\overline{CMDBUF}$	I	$\overline{CHANNEL\ BUFFER}$ This signal latches the Channel addresses for the IOA (16:0) address bus. It is generated by the FE6000, and is a delayed version of the $\overline{CMD}$ signal.
125 126 127 128 129 130 131 1 2 4 5 6 7 8 9 10 11	IOA16 IOA15 IOA14 IOA13 IOA12 IOA11 IOA10 IOA9 IOA8 IOA7 IOA6 IOA5 IOA4 IOA3 IOA2 IOA1 IOA0	O	I/O ADDRESS BUS This is the I/O address bus on the system board. It is the latched version of the addresses on the Channel. The I/O address bus supplies the addresses to all the Channel peripherals on the system board, such as the video, floppy, serial port, parallel port, timer and interrupt controllers, and EPROM.
16 19	$\overline{S1}$ $\overline{S0}$	I	$\overline{CHANNEL\ CONTROL\ SIGNALS}$ These two signals interface directly to the Channel $\overline{S(1:0)}$ signals. Together with MADE24, MMIO, and the Channel address, it generates the PROM chip selects.
13	MADE24	I/O	CHANNEL MADE24 SIGNAL This signal directly interfaces with the Channel MADE24 signal. In combination with $\overline{S(1:0)}$ and MMIO, it generates the PROM chip selects. During 80386/DMA cycles, this signal is an output signal. **ADDRESSES** — **MADE24** 0-16 MBytes — 1 >16 MBytes — 0
85	$\overline{MMCMD}$	I	$\overline{CHANNEL\ MATCHED\ MEMORY\ COMMAND}$ This is the Matched Memory Command signal on the Channel. Together with $\overline{CMD}$, it generates the UCHCMD signal.
19	$\overline{CMD}$	I	$\overline{CHANNEL\ COMMAND}$ This is the Command signal on the Channel, which, together with $\overline{MMCMD}$, generates the UCHCMD signal.

PIN NO.	NAME	TYPE	FUNCTION
71 72	$\overline{\text{PROMCSL}}$ $\overline{\text{PROMCSH}}$	O O	$\overline{\text{PROM CHIP SELECT (Low)}}$ $\overline{\text{PROM CHIP SELECT (High)}}$ These signals select the two 64K x 8 (27512) PROMs which together form the 128K of PROM on the system board. The two PROMs are organized into even and odd banks, providing a 16-bit wide interface. $\overline{\text{PROMCSL}}$ selects the even banks and $\overline{\text{PROMCSH}}$ selects the odd banks. Configurations with 8-bit wide, 1 M bit PROMs (27010) are also possible. In such a case, PROM Chip Select is generated by executing a logical OR of $\overline{\text{PROMCSL}}$ and $\overline{\text{PROMCSH}}$. To get the BIOS to execute faster, the PROM can be mapped to the DRAM and executed from there. The PROMs are located at 000E0000H - 000FFFFFH and at FFFE0000 - FFFFFFFFH. An access to either of these locations generates the chip selects for the PROM. However, a Channel cycle to access the PROM will only be run if an access is made to FFFE0000 - FFFFFFFFH, or if a read access is made to E0000 -FFFFF, and the PROM is not mapped to RAM. Writes to these addresses are ignored.
69	UCHCMD	O	COMMAND INDICATION This signal is the logical OR of the $\overline{\text{CMD}}$ and $\overline{\text{MMCMD}}$ signals, and indicates that a command is present on the Channel. It is used in the FE6010 diagnostic interface.
70	EOT	O	END-OF-CYCLE This signal is activated when $\overline{\text{CMD}}$ and $\overline{\text{S(1:0)}}$ are inactive. The CACP controller inside the FE6010 uses this signal and $\overline{\text{BURST}}$ to detect an End-of-cycle condition.
67	TEST	I	$\overline{\text{TEST PIN}}$ This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines so that an ATE tester can drive these signals instead.
82	BIAS	I	BIAS PIN This pin controls the biasing of the internal buffers, and should be pulled low with a 1.25K ±1% resistor.
66	MODE	I	MODE PIN This pin determines the mode of operation for the FE6022 device. When tied to V_{DD}, it puts the FE6022 into the data buffer mode; when it is tied to ground, it puts it into the address buffer mode.
3, 24, 35, 46,57, 83, 100, 116	V_{DD}	I	+5 V Power Supply
17, 18, 27, 32, 38, 43, 50, 51, 60, 65, 76, 87, 98, 109, 117, 132	V_{SS}	I	0 V Ground

PIN NO.	NAME	TYPE	FUNCTION
			FE6022 DATA BUFFER MODE
		I/O	PROCESSOR BUS LINES These processor data bus signal lines connect directly to the 80386 data bus.

CYCLE	PD(31:0) SIGNAL DRIVER	D(31:0) SIGNAL DRIVER
80386/DMA Writes to the Channel	80386/DMA	FE6022
Master reads from system board DRAM	DRAM Data Buffers	FE6022
80386/DMA Reads from Channel	FE6022	Channel Slave
Master Writes to system board DRAM	FE6022	Channel Master

88	PD31	I/O	CHANNEL BUS LINES These Channel data bus signal lines connect directly to the Channel data bus.
89	PD30		
90	PD29		
91	PD28		
92	PD27		
93	PD26		
94	PD25		
95	PD24		
96	PD23		
97	PD22		
99	PD21		
101	PD20		
102	PD19		
103	PD18		
104	PD17		
105	PD16		
106	PD15		
107	PD14		
108	PD13		
110	PD12		
111	PD11		
112	PD10		
113	PD9		
114	PD8		
115	PD7		
118	PD6		
119	PD5		
120	PD4		
121	PD3		
122	PD2		
123	PD1		
124	PD0		

PIN NO.	NAME	TYPE	FUNCTION
20	$\overline{\text{RDEN}}$	I	$\overline{\text{READ ENABLE}}$ This read-enable signal enables Bits PD(31:0) in the buffer during data flow from the Channel data processor data bus. The signals are active when the 80386 or the DMA performs a read from the Channel, or when the Channel master writes to the system board RAM.
19	$\overline{\text{RDLE0}}$	I	$\overline{\text{READ LATCH ENABLE 0}}$ This signal is the latch enable signal for Byte 0 (7:0). When the 80386 or the DMA performs a cycle to an 8-bit device on the Channel, the cycle is split in two. This signal latches the data during the first cycle.
15 17 19	$\overline{\text{WRENH}}$ $\overline{\text{WREN1}}$ $\overline{\text{WREN0}}$	I	$\overline{\text{WRITE ENABLE (HIGH, 1:0)}}$ This signal enables the buffer during a data flow from the processor data bus to the Channel data bus D (31:0). The signals control Bytes 0 (7:0) ($\overline{\text{WREN0}}$), 1 (15:8) ($\overline{\text{WREN1}}$), and the upper word (31:16) ($\overline{\text{WRENH}}$). They are valid when the 80386 or the DMA performs a write operation to the Channel or when a Channel master performs a read from the motherboard RAM.
14	$\overline{\text{WRLE}}$	I	$\overline{\text{WRITE LATCH ENABLE}}$ This write latch enable signal latches the write data during an 80386 or DMA write operation to the Channel. It also provides the write-data-hold time required by the Channel during these operations. This signal also latches the data when the 80386 or the DMA writes to an 8-bit port and the cycle has to be split in two.
86	$\overline{\text{SWPBYT}}$	I	$\overline{\text{BYTE SWAP}}$ When the 80386 or the DMA accesses an 8-bit port, this signal is used to swap the data to the correct byte: Bits 7-0 are swapped to Bits 15-8 for a Read operation; Bits 15-8 are swapped to Bits 7-0 for a Write operation.
85	$\overline{\text{SWPWORD}}$	I	$\overline{\text{WORD SWAP}}$ This signal swaps words when a 16-bit Channel master communicates with a 32-bit slave. This function on the Channel is called Data Steering.
84	SWPDIR ($\overline{\text{COPRES}}$)	I	SWAP DIRECTION At power-up, the state of this signal is latched by the FE6030 to determine the presence of the numeric coprocessor. In normal operation, this signal determines the direction of the byte-swap or word-swap buffers. **SWPDIR** — **DIRECTION OF TRANSFER**: **BYTE SWAP** / **WORD SWAP** 0 — (7:0) to (15:8) / (15:8) to (31:16) 1 — (15:8) to (7:0) / (31:16) to (15:0)
11, 9-3, 1, 132, 130-125	IOD (15:0) to IOD (0:0)	I/O	16-BIT I/O DATA BUS This is the 16-bit I/O data bus, which provides support for devices eight bits or sixteen bits wide.
14	$\overline{\text{IODTR}}$	I	$\overline{\text{I/O DATA TRANSMIT/RECEIVE}}$ The I/O Data Transmit/Receive signal controls the direction of the I/O data buffers inside the FE6022. The signal itself is generated by the FE6000 device. **IODTR** — **DIRECTION** 1 — D(15:0) to IOD(15:0) 0 — IOD(15:0) to D(15:0)

PIN NO.	NAME	TYPE	FUNCTION
13	$\overline{\text{IODEN}}$	I	$\overline{\text{I/O DATA ENABLE}}$ The I/O Data Enable signal enables the I/O data buffers and is generated by the FE6000. When it is active, the FE6022 drives either D(15:0) or IOD(15:0), depending on the direction set by the $\overline{\text{IODR}}$ signal.
12	IODCBA	I	I/O DATA CLOCK The I/O Data Clock signal is used to latch the data during reads from the Channel peripherals on the I/O bus. The MEMRD, MEMWR, IORD, and IOWR commands to the peripherals are shorter than the Channel $\overline{\text{CMD}}$ signal. This signal ensures that the data being read meets the timings to the Channel $\overline{\text{CMD}}$ signal.
67	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines so that an ATE tester can drive these signals instead.
66	MODE	I	MODE PIN This pin determines the mode of operation for the FE6022 device. When tied to V_{DD}, it puts the FE6022 into the data buffer mode; when it is tied to ground, it puts it into the address buffer mode.
82	BIAS	I	BIAS PIN This pin controls the biasing of the internal buffers, and should be pulled low with a 1.25K ±1% resistor.
3, 24, 35, 46,57, 83, 100, 116	V_{DD}	I	+5 V Power Supply
17, 18, 27, 32, 38, 43, 50, 51, 60, 65, 76, 87, 98, 109, 117, 132	V_{SS}	I	0 V Ground
68, 69, 70, 71, 72, 73, 74, 75, 77, 78, 79, 80, 81	Reserved	-	RESERVED PINS These pins should not be connected.

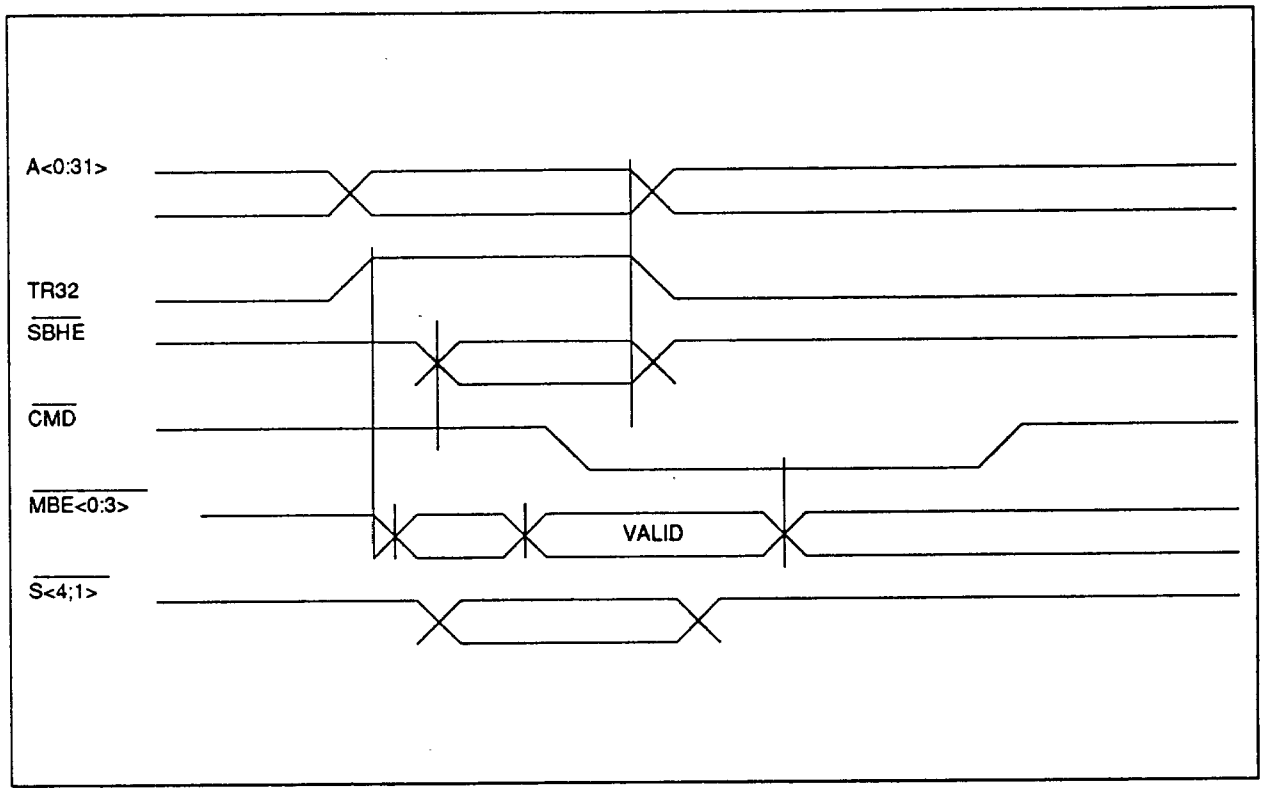


Figure 5. Address Chnl Master Accesses Translate Function

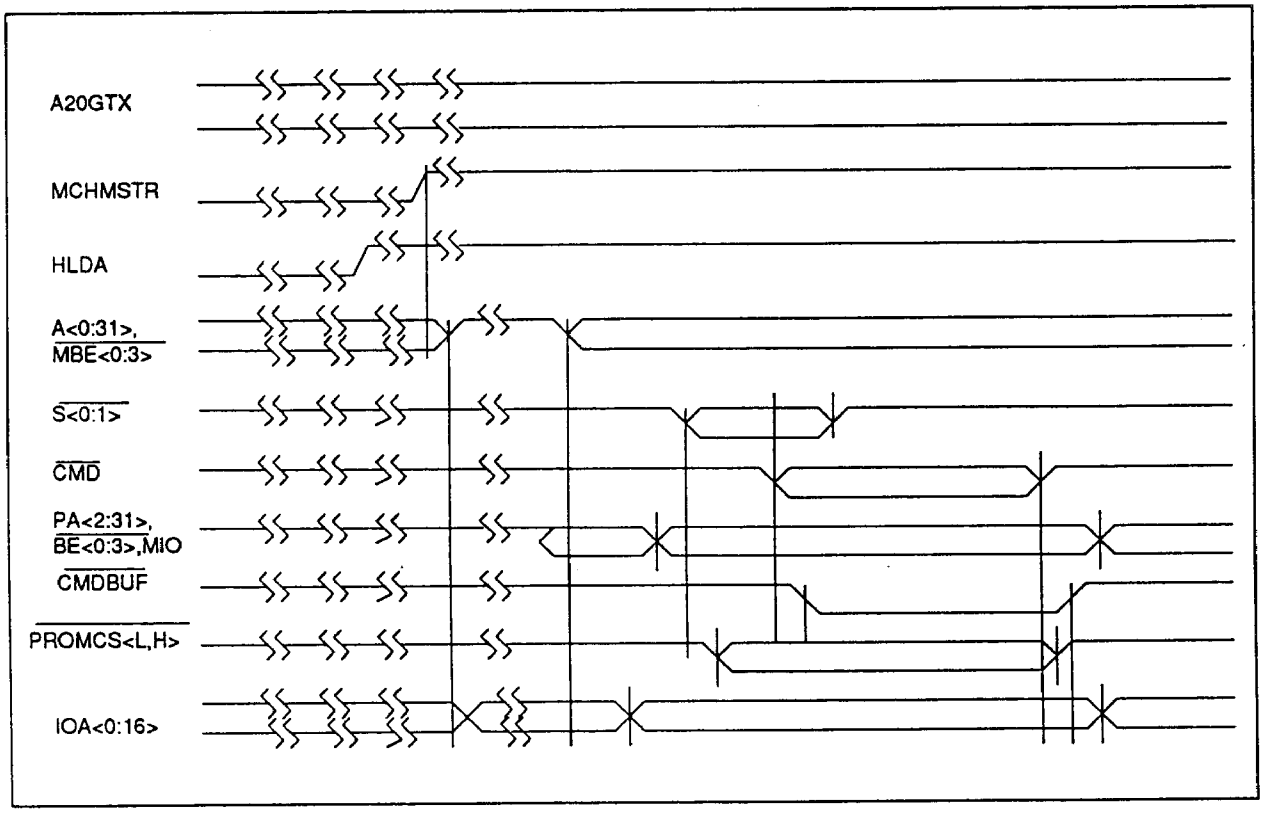


Figure 6. Address Mode Channel Master Accesses

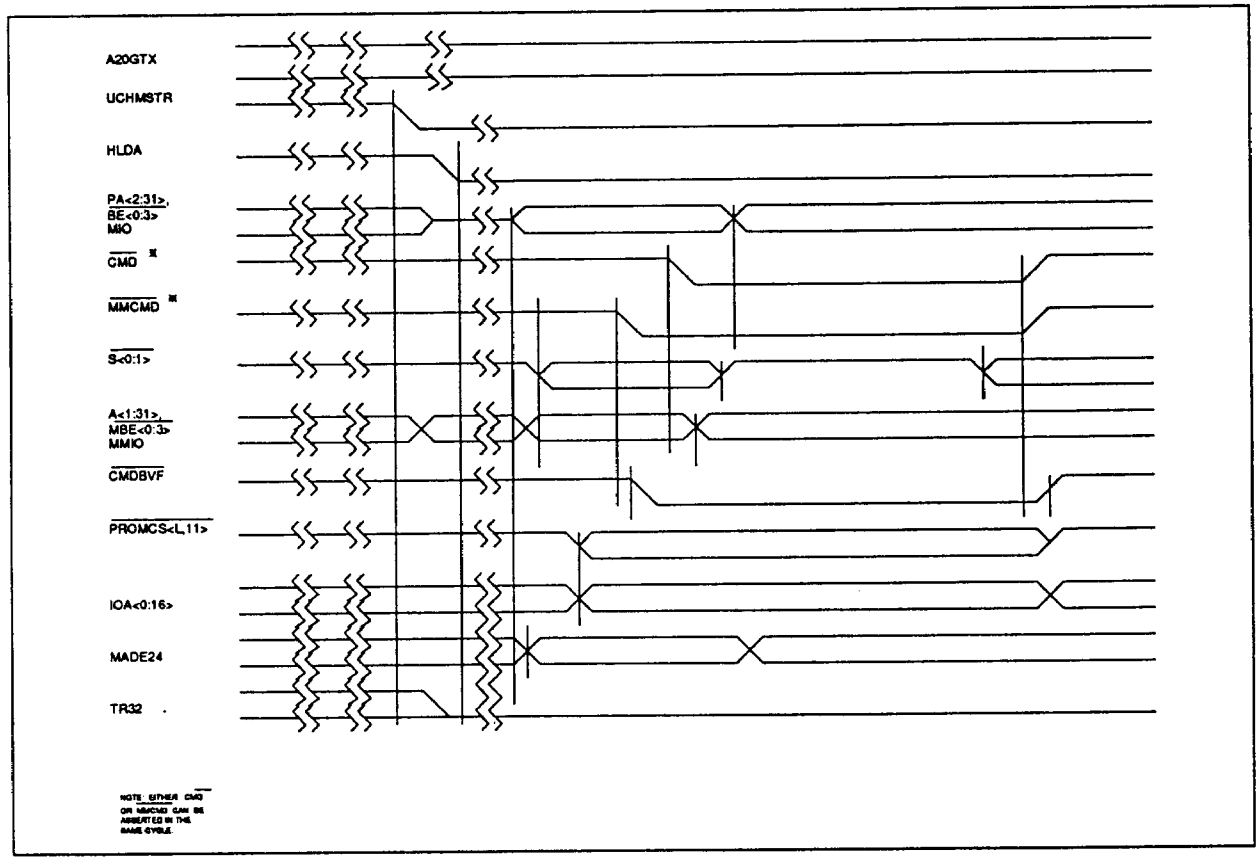


Figure 7. Address Mode: 80386/DMA Channel Accesses

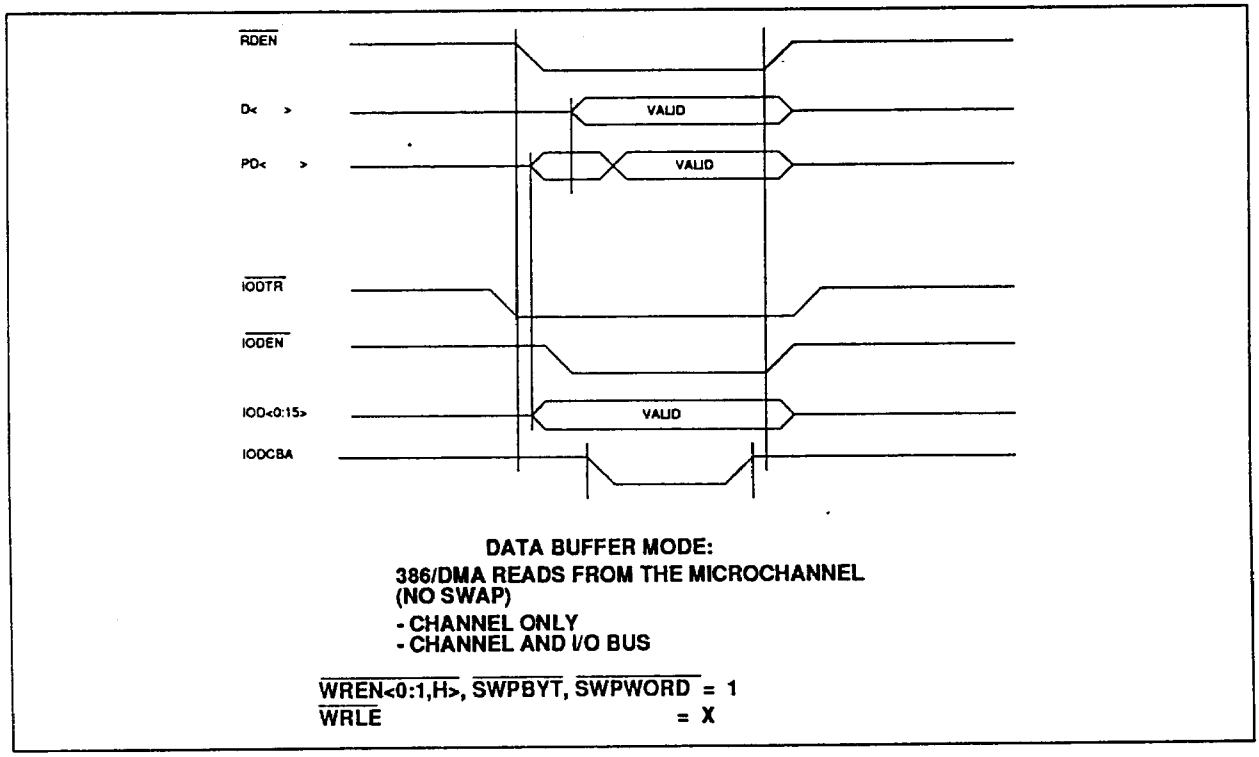
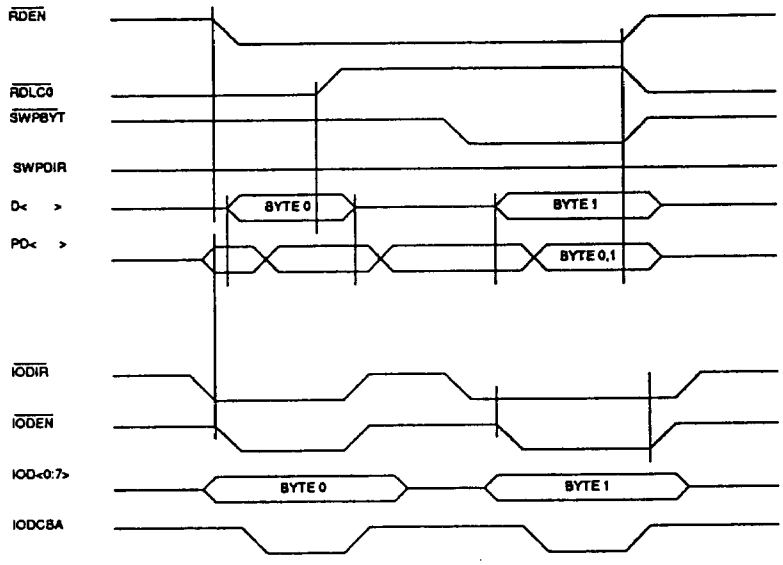


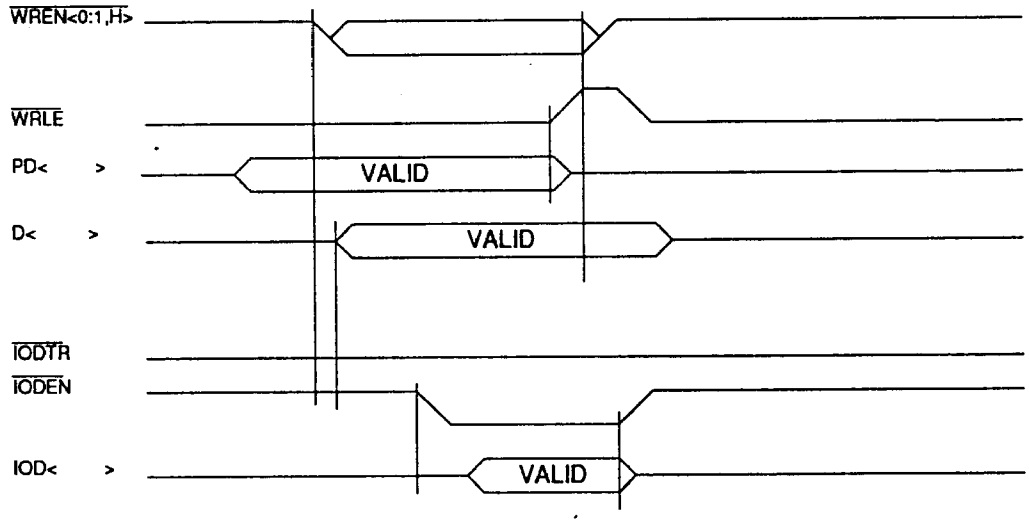
Figure 8. Data Mode: 80386/DMA Reads from the Channel



FE6021: 386/DMA READS FROM THE MICROCHANNEL
(WITH SWAP)
- CHANNEL ONLY
- CHANNEL AND I/O BUS

WREN<0:1,H>, SWPWORD = 1
WRLE = X

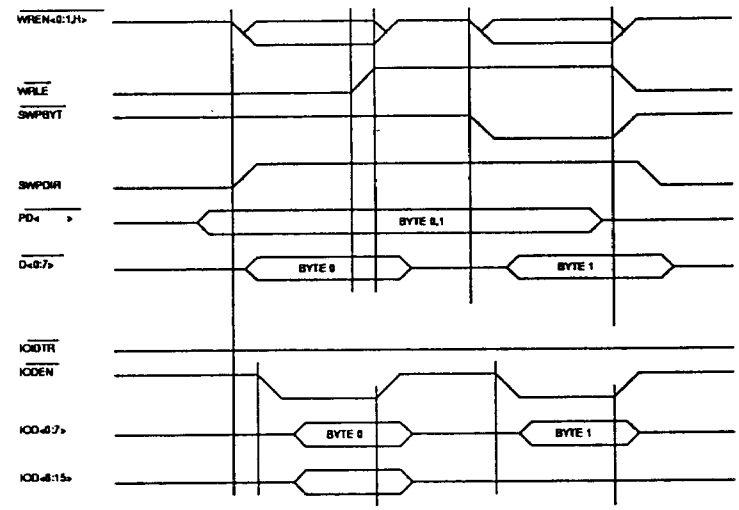
Figure 9. Data: 80386/DMA Reads from the Chnl with Swap



FE6021: 386/DMA - WRITES TO THE MICROCHANNEL
(NO SWAP)
- CHANNEL ONLY
- CHANNEL AND I/O BUS

RDEN, SWPBYT, SWPWORD = 1
RDLE0, SWPDIR, IODCBA = X

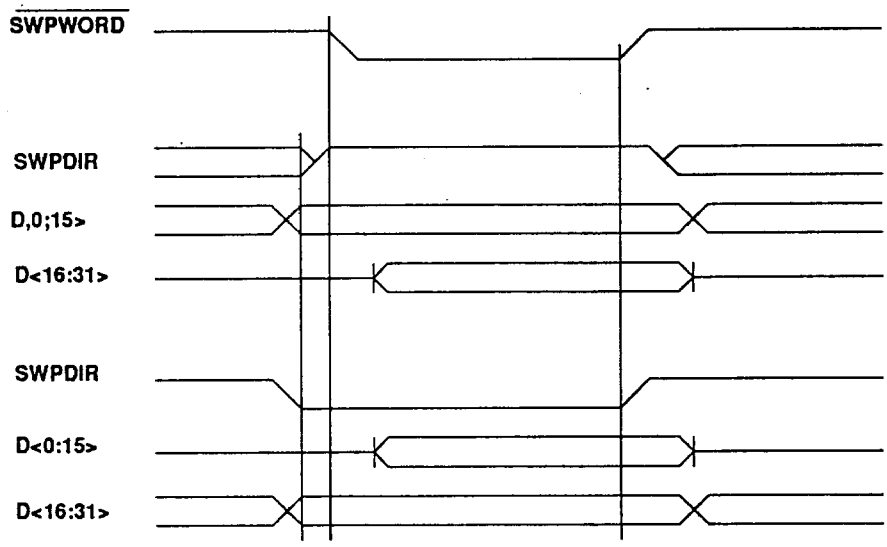
Figure 10. Data: 80386/DMA Writes to the Channel



FE6021: 386/DMA WRITE TO THE MICROCHANNEL
(WITH SWAP)
- MICROCHANNEL ONLY.
- MICROCHANNEL AND I/O BUS.

$\overline{RDEN}$, $\overline{SWPWORD}$ = 1
$\overline{RDLE0}$, $\overline{IODCBA}$ = X

Figure 11. Data: 80386/DMA Writes to the Chnl with Swap



FE6021: MICROCHANNEL MASTER - WORD SWAP

$\overline{SWPBYT}$, $\overline{NWRLE}$, $\overline{NRDLE0}$ = 1
$\overline{CODTR}$, $\overline{NIODEN}$, $\overline{NRDEN}$ = X
$\overline{WREN<0:1,H>}$

Figure 12. Data Mode: Channel Master Word Swap

3.0 TECHNICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for the FE6022 devices are tabulated below. Permanent damage to the devices could result from exposing it to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD} - V_{SS}	0	7	V
Input Voltage	V_{IABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Bias on Output Pin	V_{OABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	T_S	-40	125	°C

3.2 NORMAL OPERATING CONDITIONS

Exposing the FE6022 to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

V_{SS} = 0 V

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD} + 0.3	V
Power Dissipation	P_W	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

3.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ fc = 1 MHz	C_I	-	5	pF
I/O Capacitance	C_{IO}	-	10	pF
Logic High Input Voltage	V_{IH}	2.0	-	V
Logic Low Input Voltage	V_{IL}	-	0.8	V
Input Leakage	I_{IL}	-	+-10	µA
Tristate Output Leakage	I_{OL}	-	+-30	µA
I/O Pin Leakage	I_{IOL}	-	+-40	µA
FE6022 ADDRESS BUFFER MODE (MODE = 0)				
OUTPUTS $\overline{\text{PROMCSL}}$, $\overline{\text{PROMCSH}}$, EOT, UCHCMD, PA(2:31)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	-	mA
OUTPUTS $\overline{\text{BE}}$(3:0), MIO*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	-	mA
OUTPUT IOA(16:0)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	8	-	mA
ALL OTHER OUTPUTS*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	24	-	mA

PARAMETER	SYMBOL	MIN	MAX	UNITS
FE6022 DATA BUFFER MODE (MODE = 1)				
OUTPUTS PD(31:0)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	-	mA
OUTPUTS IOD(15:0)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	-	mA
OUTPUT D(31:0)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	8	-	mA

*The following signals are bi-directional: PA(31:2), $\overline{BE(3:0)}$, MIO, MADE24, TR32, MMIO, $\overline{MBE(3:0)}$, A(31:1), $\overline{SBHE}$, PD(31:0), IOD(15:0), and D(31:0).

NOTE

1.The input pin "BIAS" is connected externally to ground through a 1% 1.25 K ohm resistor, and is part of an internal biasing circuit. Capicitance, leakage, and threshold measurements on this pin do not apply.

2.The following signals have internal pullups of 20K: $\overline{BE(3:2)}$, $\overline{MBE(3:0)}$, MMIO, MIO.

3.When $\overline{TEST}$ = 0, all outputs and bi-directional signal lines are tristated.

3.4 A.C. LOAD SPECIFICATIONS

SIGNAL	SYMBOL	MIN	MAX	UNITS
FE6022 ADDRESS BUFFER MODE (MODE = 0)				
$\overline{PROMCSL}$, $\overline{PROMCSH}$, EOT, UCHCMD	CL	50	-	pF
$\overline{BE(3:0)}$, MIO*	CL	120	-	pF
PA(31:2), IOA(16:0)*	CL	120	-	pF
MADE24, TR32, MMIO, $\overline{MMC}$, $\overline{MBE(3:0)}$, A(31:1), $\overline{SBHE}$*	CL	240	-	pF
FE6022 DATA BUFFER MODE (MODE = 1)				
PD(31:0), IOD(15:0)*	CL	120	-	pF
D(31:0)*	CL	240	-	pF

*The following signals are bi-directional: PA(31:2), $\overline{BE(3:0)}$, MIO, MADE24, TR32, MMIO, $\overline{MBE(3:0)}$, A(31:1), $\overline{SBHE}$, PD(31:0), IOD(15:0), and D(31:0).

NOTE

1.The following signals have internal pullups of 20K: $\overline{BE(3:2)}$, $\overline{MBE(3:0)}$, MMIO, MIO.

4.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	UNITS
T1	Propagation Delay			ns
	A1, $\overline{SBHE}$, $\overline{MBE(3:0)}$ to $\overline{BE(3:0)}$		28	ns
	PA(31:2), to A(31:2)		26	ns
	A(31:0) to PA(31:2), $\overline{BE(3:0)}$	26	28	ns
	A20GTX to A20		26	ns
	MIO to MMIO		25	ns
	MMIO to MIO		25	ns
	TR32, A(1:0), $\overline{SBHE}$ to $\overline{MBE(3:0)}$ or		28	ns
	$\overline{BE(3:0)}$	-	28	ns
T2	$\overline{CMD}$, $\overline{MMCMD}$, to UCHCMD	-	20	ns
T3	$\overline{S(1:0)}$, $\overline{CMD}$ to EOT	-	25	ns

Table 3 Address Buffer Mode Timings (ns)

PARAM	DESCRIPTION	MIN	MAX	UNITS
T4A	MIO, S(1:0), MADE24, A(0, 31:17)	-	27	ns
	SBHE to PROMCSL, PROMCSH	-	27	ns
T4B	PA(17:13), A20GTX, HLDA, UCHMSTR to	-	54	ns
	PROMCSL, PROMCSH	-	54	ns
T5A	A(16:0), to IOA(16:0)	-	25	ns
T5B	PA(16:2), BE(3:0) to IOA(16:0)	-	50	ns
T6	HLDA to MMC or MADE24	-	25	ns
T7A	Setup to Falling Edge of CMD, MADE24, 5432, MIO,	10	-	ns
	MMIO, PA(31:2), BE(3:0), A(31:0), MBE(3:0),	10	-	ns
	SBHE, S(1:0)	10	-	ns
T7B	Setup to Falling Edge of CMD	40	-	ns
	A20GTX, UCHMSTR, HLDA	40		ns
T8A	Hold from Falling Edge of MCMD, MADE24, TR32,	10	-	ns
	MIO, MMIO, PA(31:2), BE(3:0), A(31:0),	10	-	ns
	MBE(3:0), SBHE, S(1:0)	10	-	ns
T8B	Hold from Falling Edge of CMD	15	-	ns
	A20GTX, UCHMSTR, HLDA	15	-	ns
T9	CMD Inactive Pulse Width	30	-	ns
T10A	Setup to Rising Edge of CMDBUF	10	-	ns
	PA(31:2), BE(3:0), A(15:0)	10	-	ns
T10B	Setup to Rising Edge of CMD	5	-	ns
T11	Hold from Rising Edge of CMDBUF	5	-	ns
	PA (31:2), BE(3:0), A(15:0)	5	-	ns
T12	CMDBUF Inactive Pulse Width	30	-	ns
T13A	Disable - from UCHMSTR	21	-	ns
	A(31:1), MBE(3:0), MMIO, MADE24,	21	-	ns
	TR32, SBHE, PA(31:2), BE(3:0), MIO	21	-	ns
T13B	Enable - from UCHMSTR	26	-	ns
	A(31:1), MBE(3:0), MMIO, MADE24,	26	-	ns
	TR32, SBHE, PA(31:2), BE(3:0), MIO	26	-	ns

Table 3 (Cont) Address Buffer Mode Timings (ns)

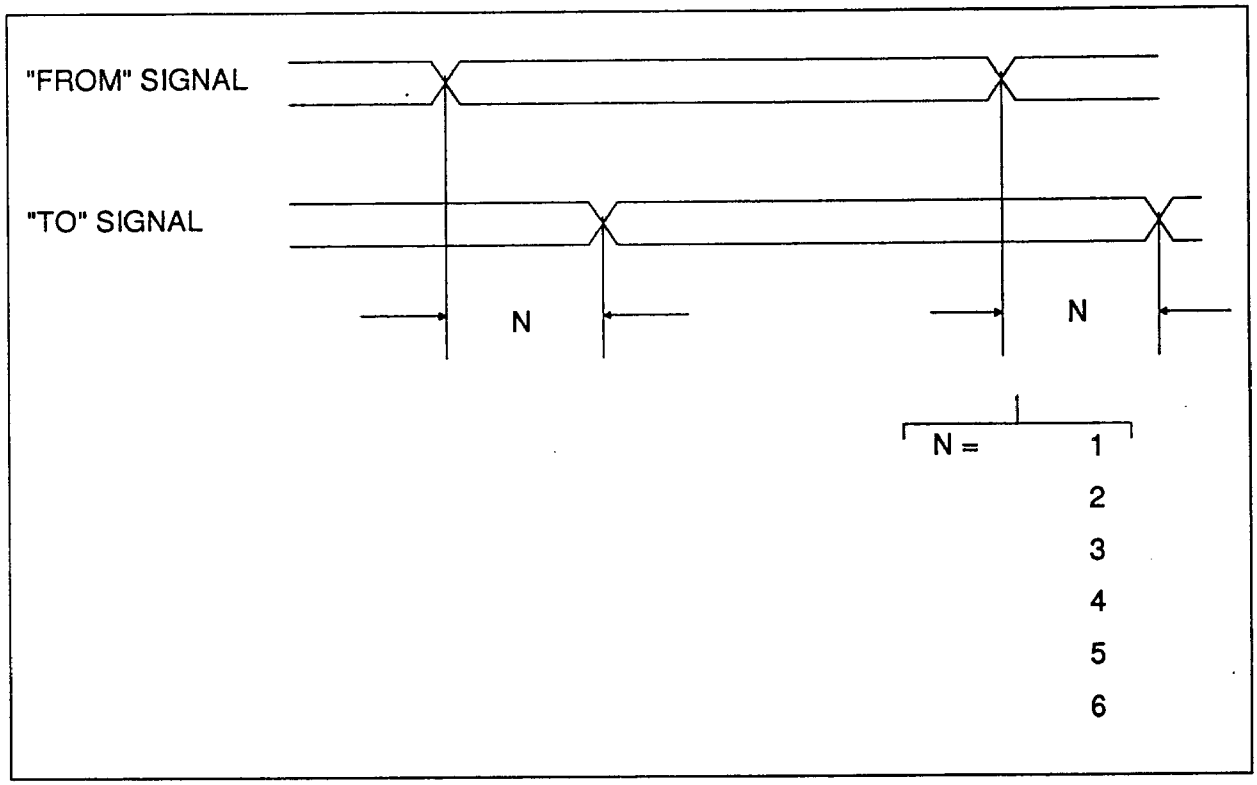


Figure 13. Address Buffer Mode: Propagation Delay Timings

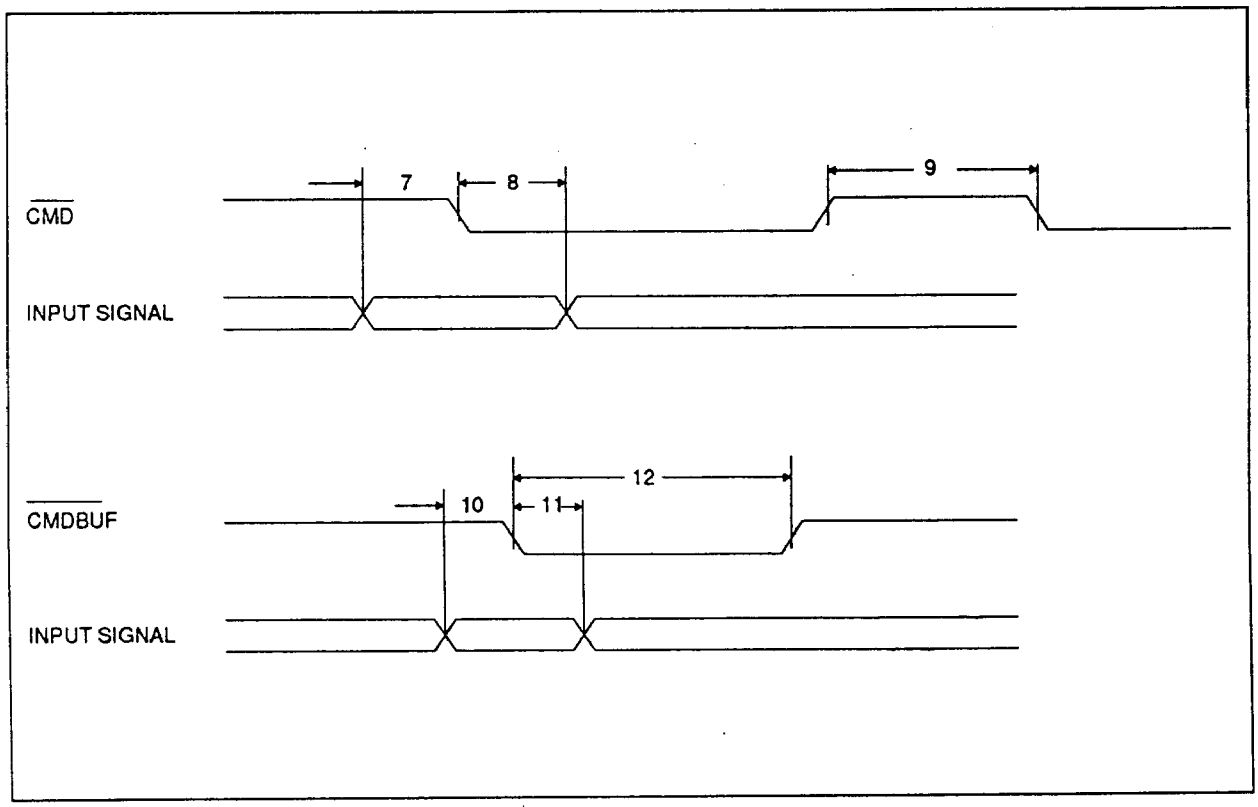


Figure 14. Address Buffer Mode: Latch Timings

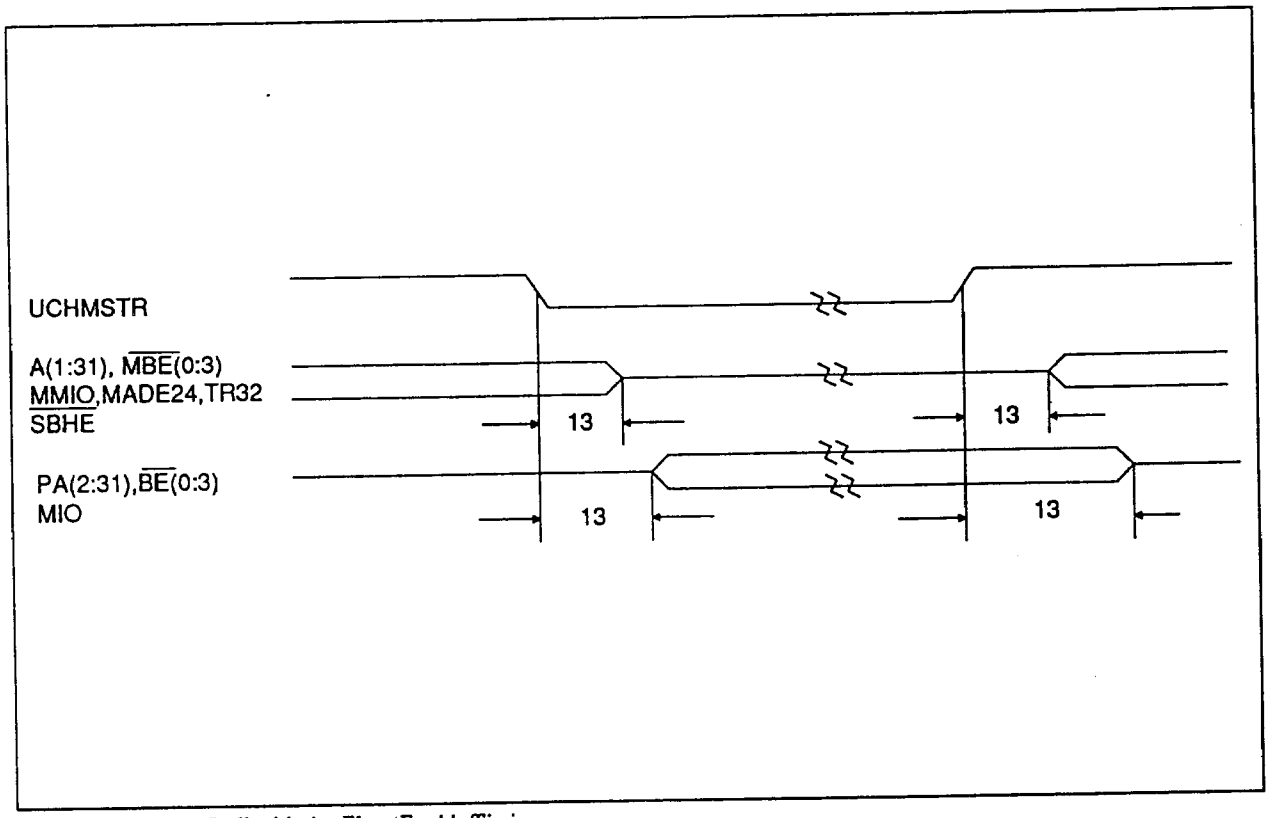


Figure 15. Address Buffer Mode: Float/Enable Timings

PARAM	DESCRIPTION	MIN	MAX	UNITS
T1	Output Enable/Disable	-	-	ns
	$\overline{WREN0}$ to D(7:0)	-	26	ns
	$\overline{WREN1}$ to D(15:8)	-	26	ns
	$\overline{WRENH}$ to D(31:16)	-	26	ns
	$\overline{RDEN}$ to PD(31:0)	-	28	ns
	$\overline{IODEN}$ or $\overline{IODTR}$ to D(15:0) or IOD(15:0)	-	25	ns
T2	Propagation Delay in Transparent Mode	-	-	ns
	PD(31:0) to D(31:0)	-	26	ns
	D(31:0) to PD(31:0)	-	26	ns
T3	Latch Enable to Data	-	-	ns
	$\overline{WRLE}$ to D(31:0) ($\overline{WRENx}$ active)	-	15	ns
	$\overline{RDLE0}$ to PD(7:0) ($\overline{RDENL}$ active)	-	15	ns
T4A	Data Setup to Latch Enable	-	-	ns
	D(7:0) to $\overline{RDLE0}$	10	-	ns
	IOD(15:0) to IODCBA	10	-	ns
T4B	Data Setup to Latch Enable	20	-	ns
	PD(31:0) to $\overline{WRLE}$	20	-	ns
T5	Data Hold from Latch Enable	5	-	ns
	D(7:0) from $\overline{RDLE0}$	5	-	ns
	IOD(15:0) from IODCBA	5	-	ns
	PD(31:0) from $\overline{WRLE}$	5	-	ns
T6A	Latch Enable Active Pulse Width	15	-	ns
	$\overline{WRLE}$, $\overline{RDLE0}$, IODCBA	15	-	ns
T6B	Latch Enable Active Pulse Width	30	-	ns
	$\overline{WRLE}$, $\overline{RDLE0}$, IODCBA	30	-	ns
T7	Propagation Delay	-	-	ns
	SWPDIR to D( ) or PD( )	28	30	ns
	$\overline{SWPBYT}$ to D( ) or PD( )	28	28	ns
	$\overline{SWPWORD}$ to D( ) or PD( )	28	28	ns

Table 4. Data Buffer Mode Timings (ns)

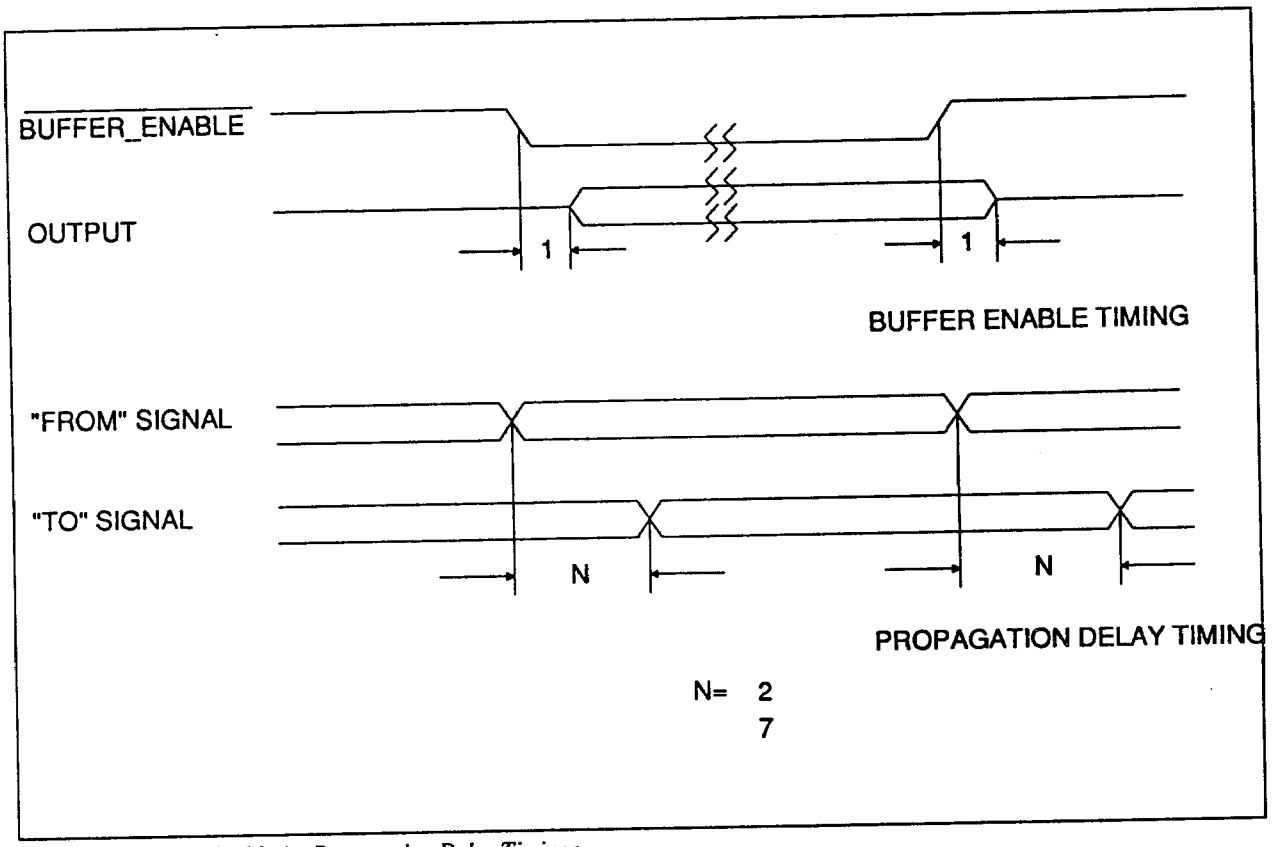


Figure 16. Data Buffer Mode: Propagation Delay Timings

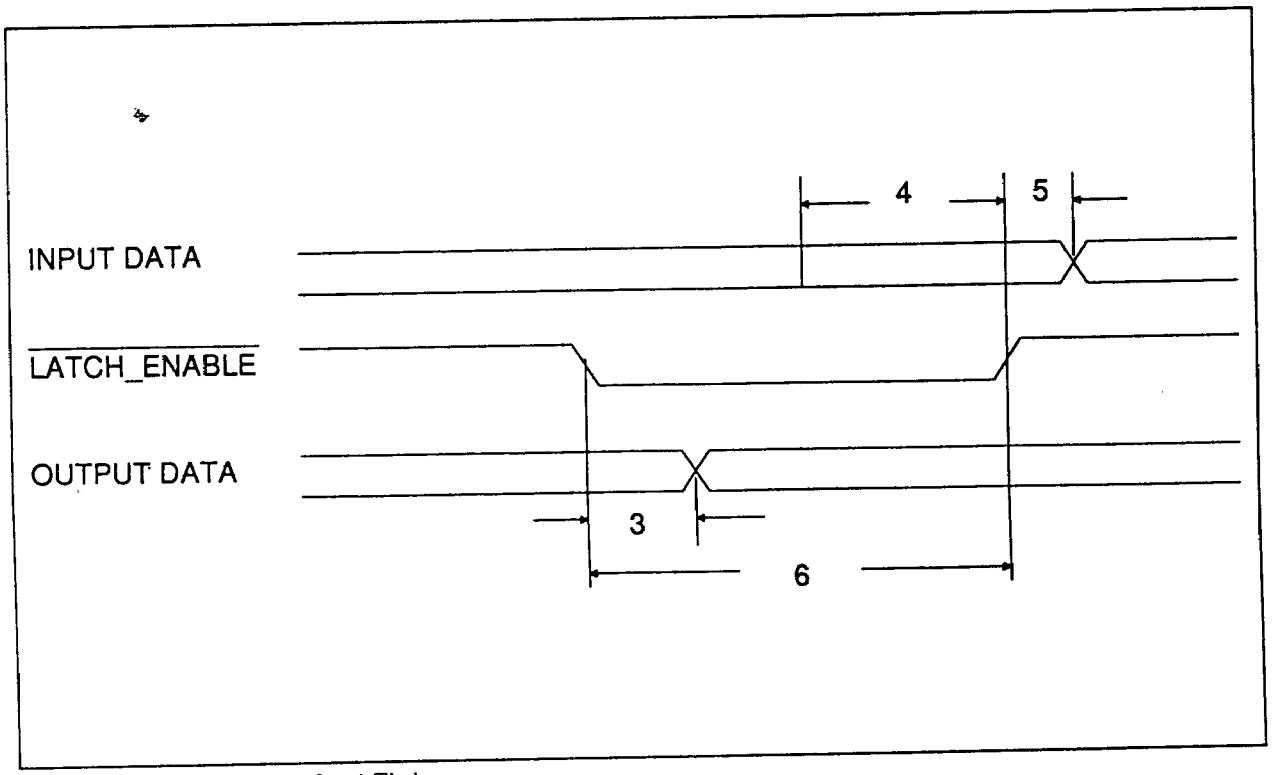


Figure 17. Data Buffer Mode: Latch Timings

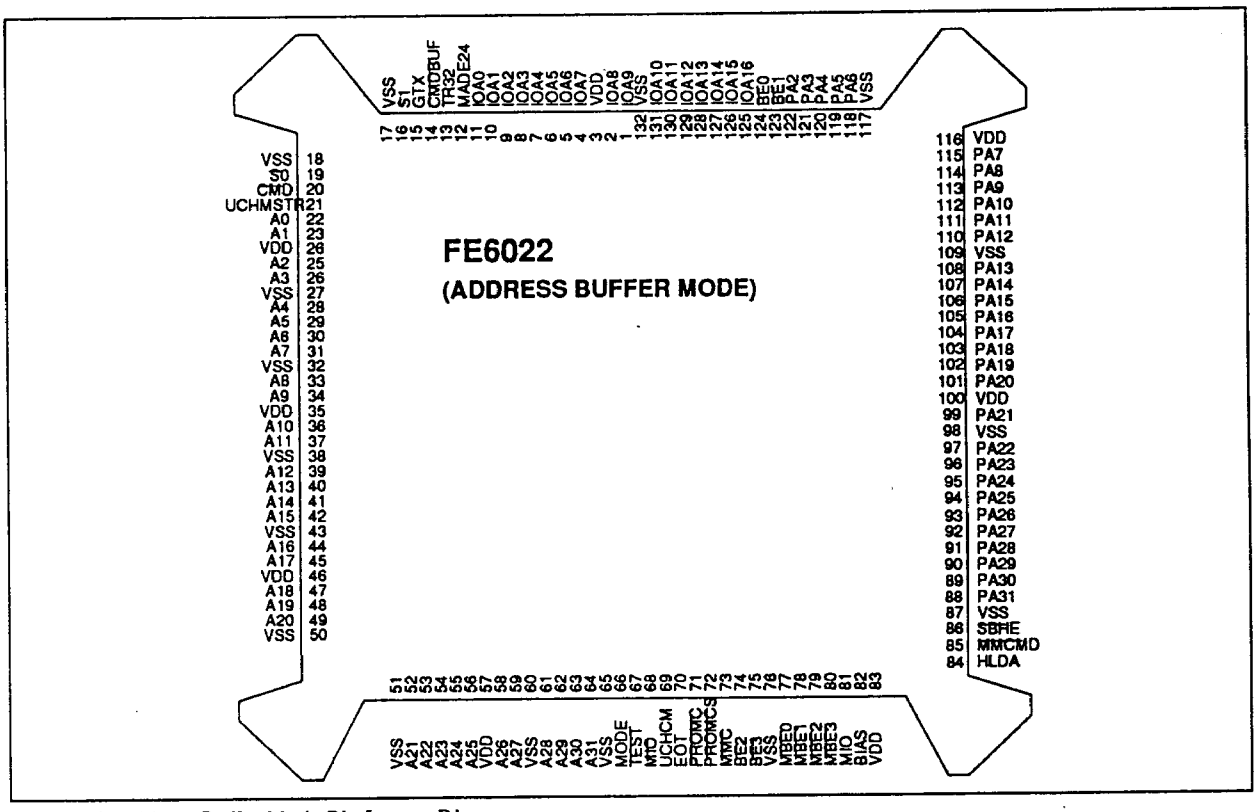


Figure 18. Address Buffer Mode Pin Layout Diagram

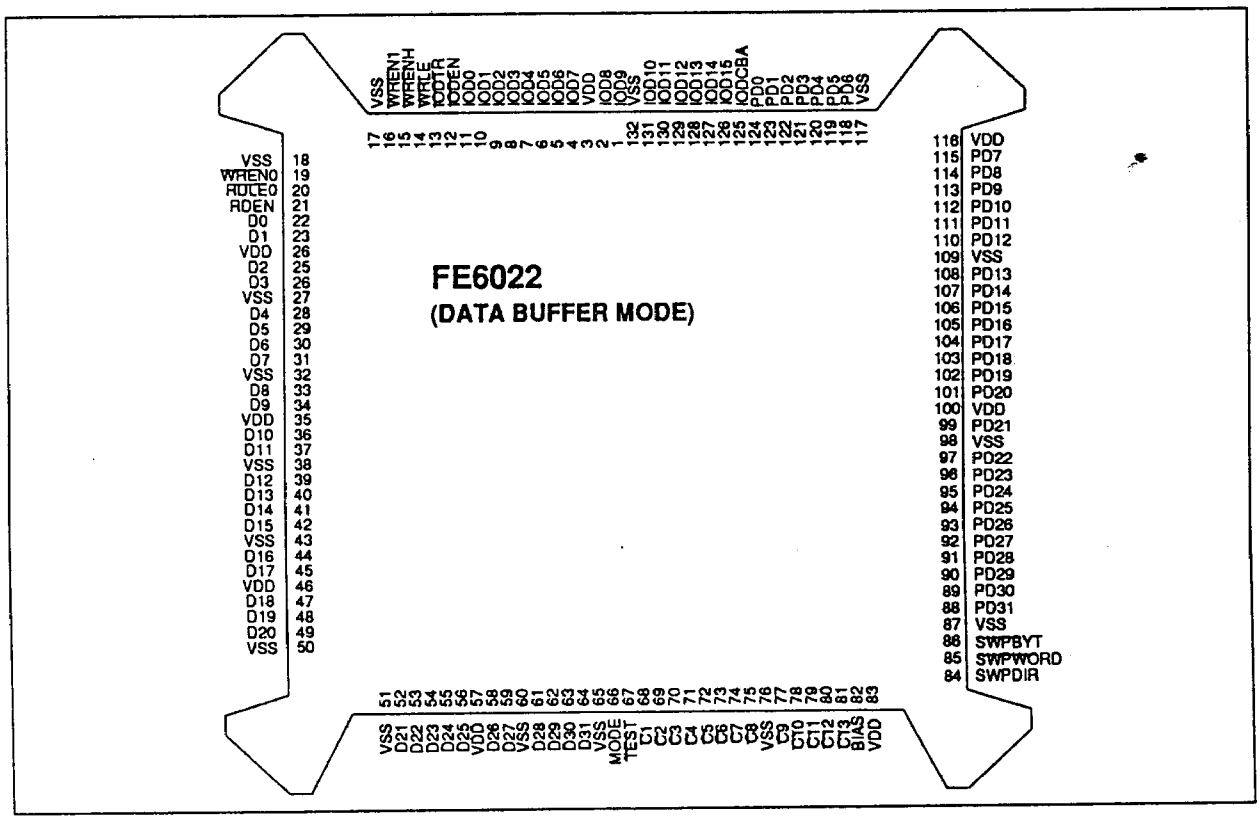


Figure 19. Data Buffer Mode Pin Layout Diagram

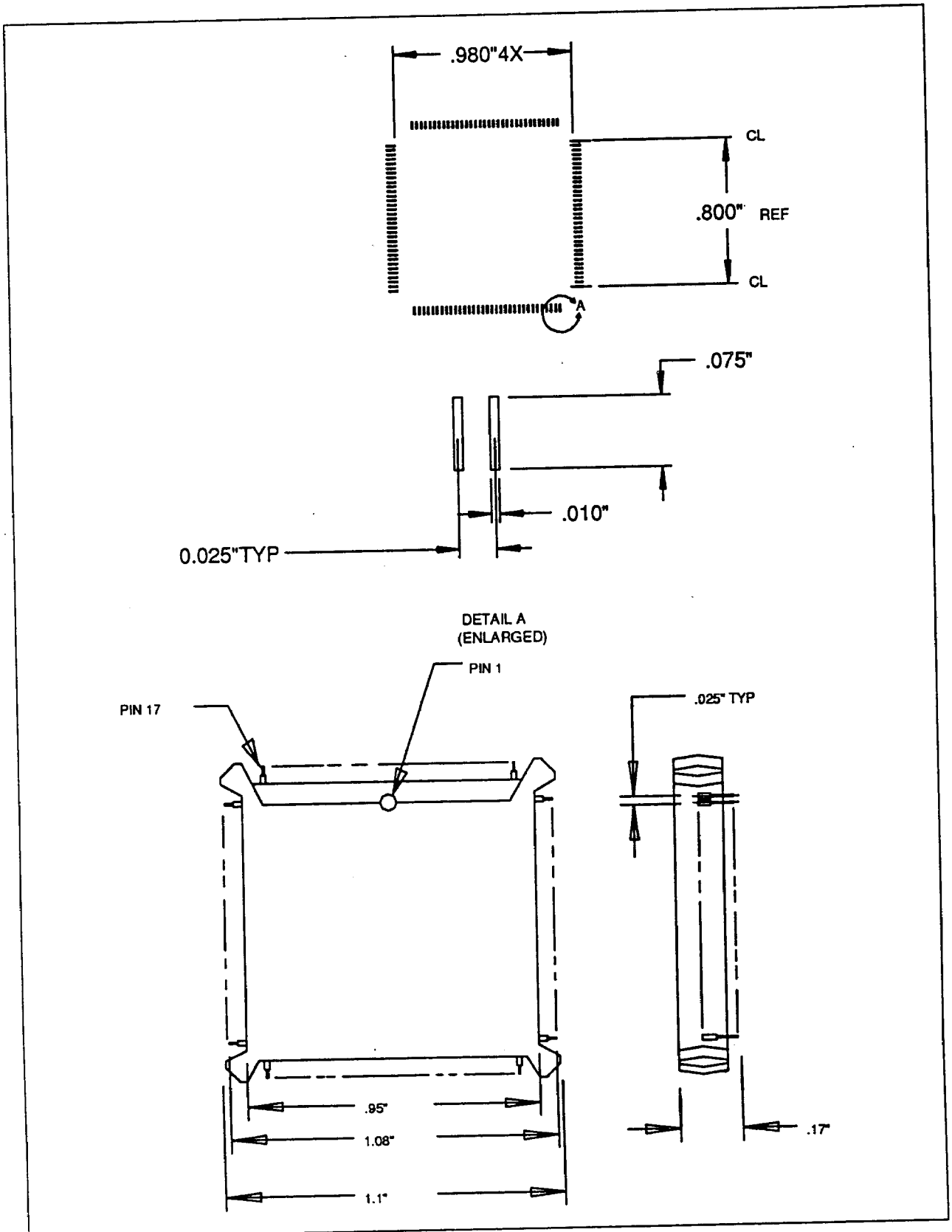
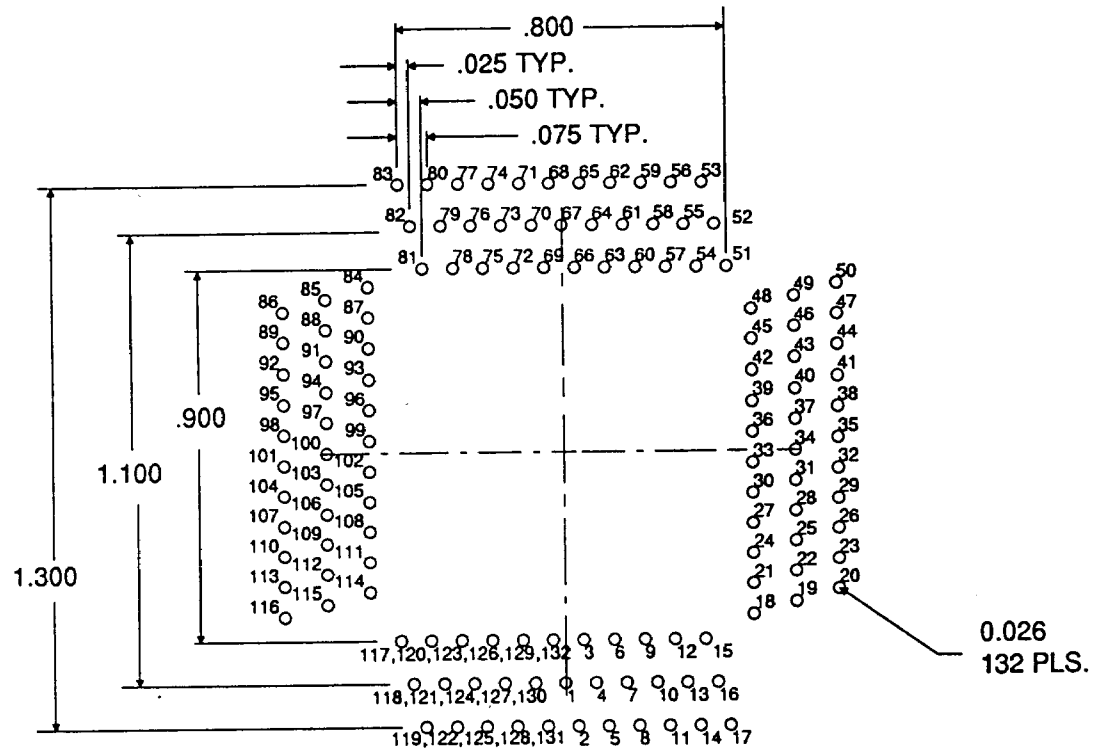


Figure 20. 132-Pin JEDEC Flat Pack Packaging Diagram



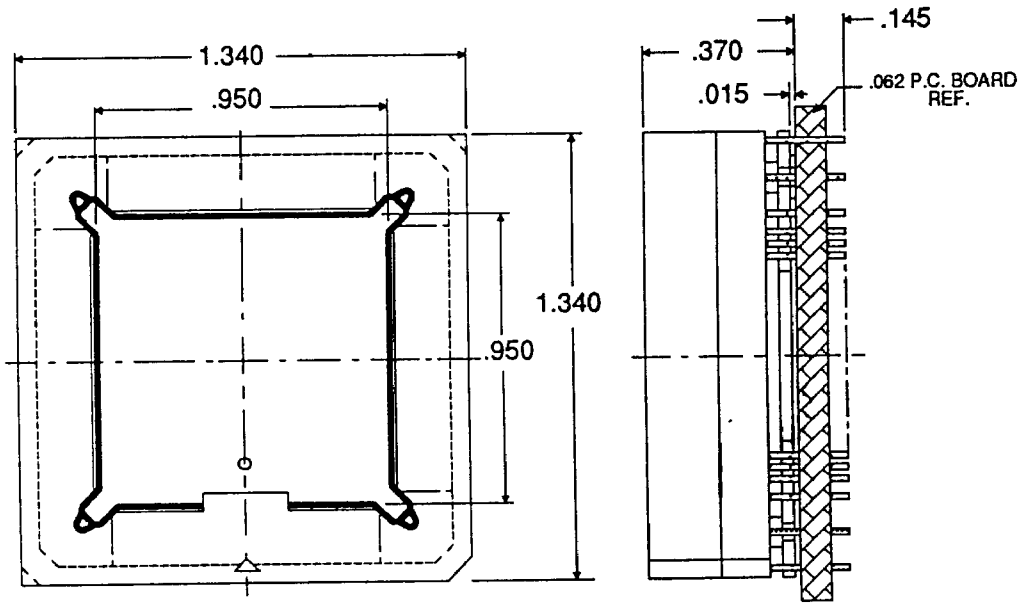


Figure 21. Socket Diagram