Advance Information

FE6010

DMA and Channel Control Logic

- Completely compatible with the IBM Personal System/2* Models 70 and 80
- Configurable for systems based on the 80386 (FE6500) or the 80386SX
- 16, 20, and 25 MHz Clock Speeds to Maximize Flexibility and Performance
- Half-speed 80387/80387SX Operation
- 4-Gigabyte Enhanced Addressing
- Micro Channel* Arbitration Control Logic
- Functionality equivalent to two 8237 DMA controllers with Extended Mode Support
- Clock, Resets, and Parity Latch Control
- Extended Setup FacilityTM (ESF)TM
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

The FE6010 integrated circuit forms part of Western Digital's innovative FE6500 chip set, facilitating the design and implementation of boards equivalent to the Model 70 and 80 system boards. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, while reducing system cost and increasing system reliability.

The Extended Setup Facility is a Western Digital enhancement, designed to allow more functionality such as a Winchester Controller, LAN Adapter or additional serial port to be added on to the system board. It provides product differentiation at the system level and helps hold down costs. The general block diagram in Figure 1 illustrates a typical system using the FE6500 chip set. Devices with bold outlines are available from Western Digital Corporation.

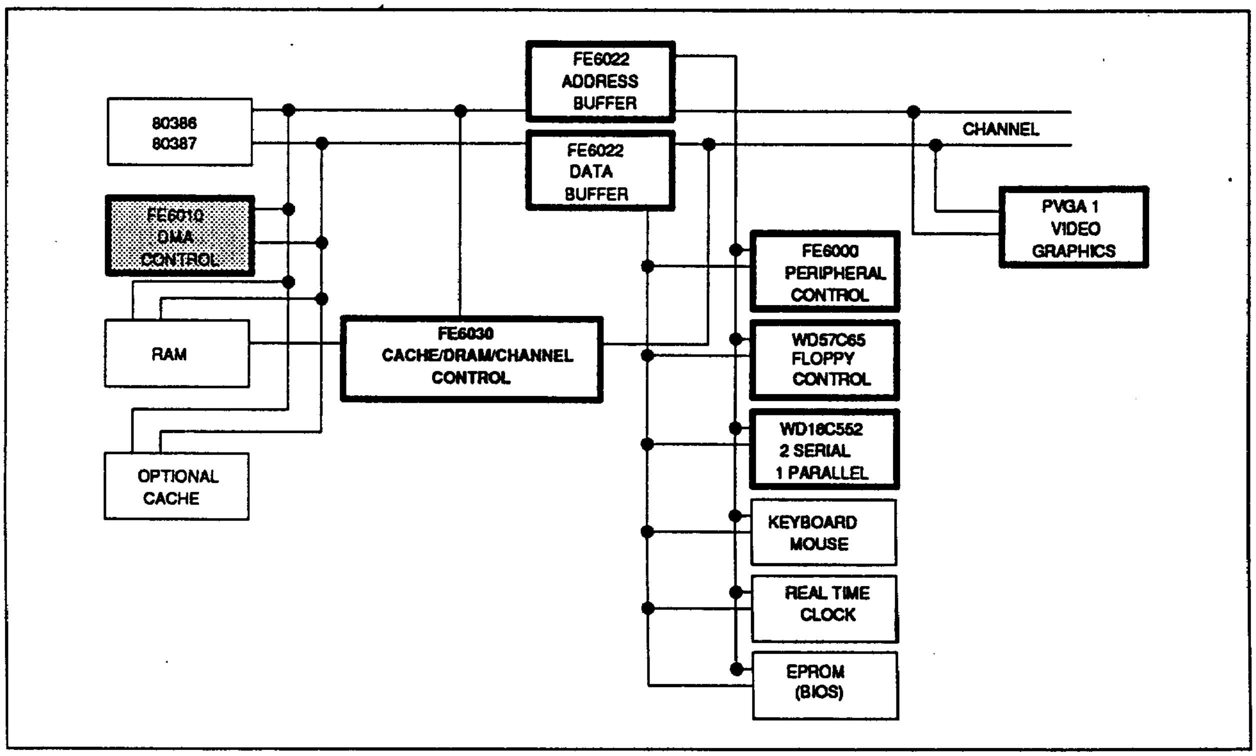

Figure 1. System Block Diagram

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WESTERN DIGITAL

Additional References

IBM PS/2 Model 70 Technical Reference Manual
IBM PS/2 Model 80 Technical Reference Manual
Intel Microprocessor and Peripheral Handbook*

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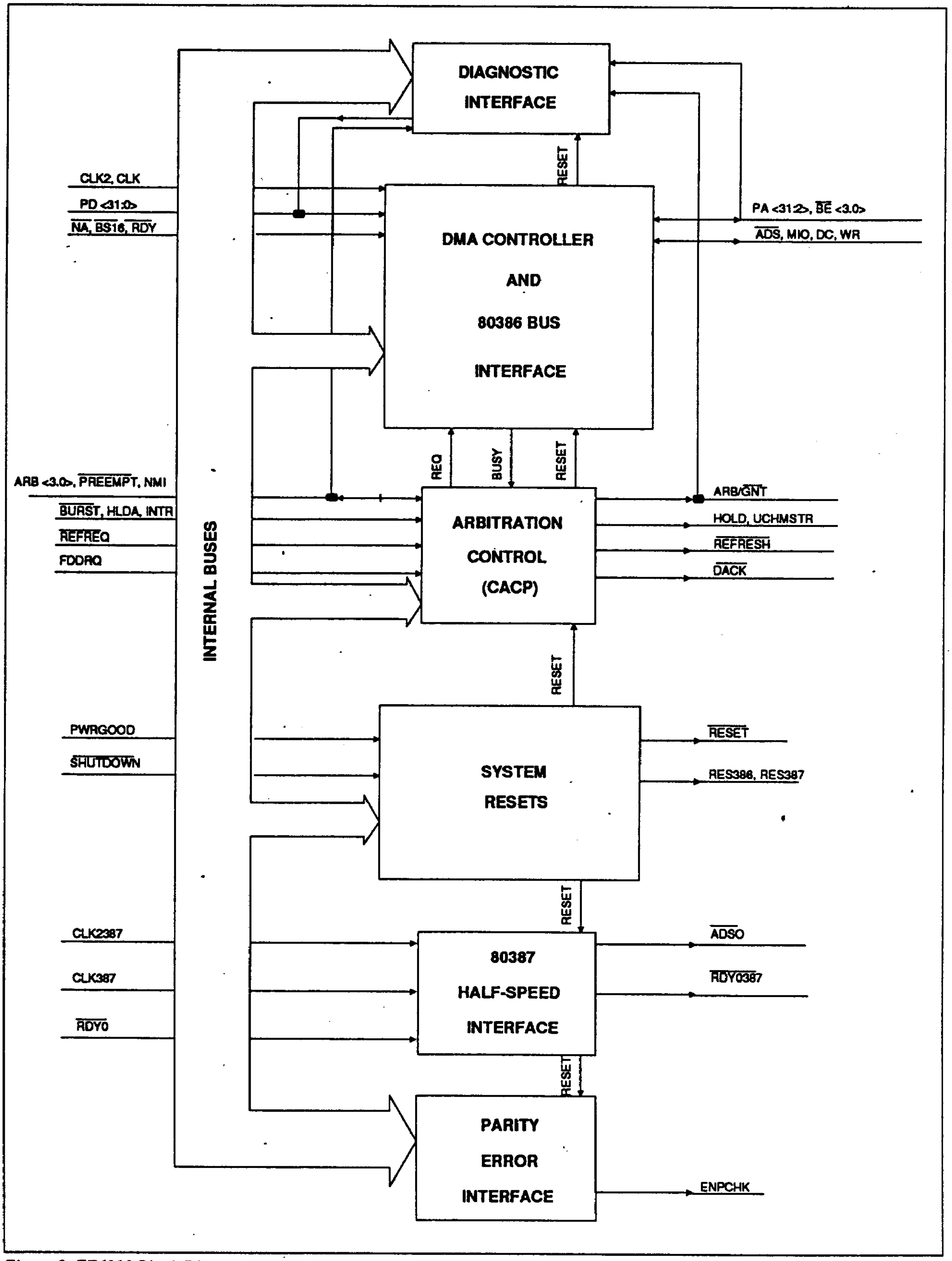
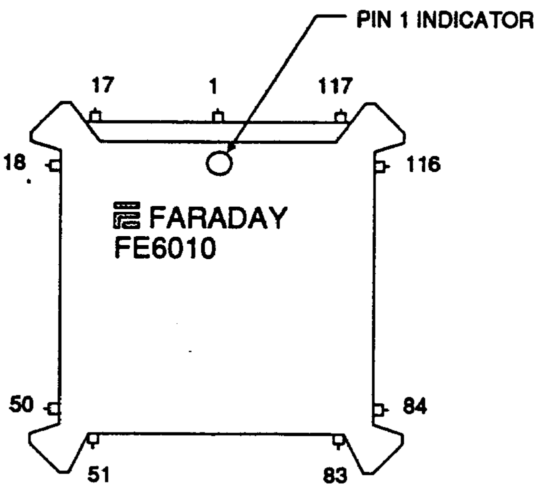


Figure 2. FE6010 Block Diagram



132 -PIN JEDEC FLAT PACK

Figure 3. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	CLK2	34	PD7	67	$\overline{REFRESH}$	100	V_{DD}
2	V_{SS}	35	V_{SS}	68	$\overline{BE0}$	101	PA17
3	CLK	36	PD8	69	$\overline{BE1}$	102	PA16
4	CLK2387	37	PD9	70	$\overline{BE2}$	103	PA15
5	V_{DD}	38	PD10	71	$\overline{BE3}$	104	PA14
6	CLK387	39	PD11	72	V_{SS}	105	PA13
7	EOT	40	PD12	73	$\overline{ADS}$	106	PA12
8	$\overline{REFREQ}$	41	PD13	74	MIO	107	PA11
9	UCHCMD	42	PD14	75	DC	108	V_{SS}
10	A20GATE	43	V_{SS}	76	WR	109	PA10
11	No Connect	44	PD15	77	$\overline{RESET}$	110	PA9
12	INTR	45	PD16	78	RES386	111	PA8
13	PWRGOOD	46	PD17	79	RES387	112	PA7
14	$\overline{SHUTDOWN}$	47	PD18	80	$\overline{CDSETEN}$	113	PA6
15	$\overline{BURST}$	48	PD19	81	VGAEN	114	PA5
16	$\overline{TEST}$	49	PD20	82	$\overline{EDRENA}$	115	PA4
17	V_{SS}	50	V_{SS}	83	V_{DD}	116	V_{DD}
18	$\overline{PREEMPT}$	51	PD21	84	PA31	117	PA3
19	ARB0	52	PD22	85	PA30	118	PA2
20	ARB1	53	PD23	86	PA29	119	$\overline{NMI}$
21	ARB2	54	PD24	87	V_{SS}	120	ENPCHK
22	ARB3	55	V_{DD}	88	PA28	121	$\overline{DACK}$
23	V_{SS}	56	PD25	89	PA27	122	$\overline{ADSO}$
24	CHRESET	57	PD26	90	PA26	123	$\overline{RDY0387}$
25	$\overline{CHCK}$	58	PD27	91	PA25	124	$\overline{RDY0}$
26	PD0	59	PD28	92	PA24	125	FDDRQ
27	PD1	60	PD29	93	PA23	126	UCHMSTR
28	PD2	61	PD30	94	PA22	127	A20GTX
29	PD3	62	PD31	95	V_{SS}	128	V_{SS}
30	V_{DD}	63	HOLD	96	PA21	129	HLDA
31	PD4	64	V_{SS}	97	PA20	130	$\overline{BS16}$
32	PD5	65	ARB/$\overline{GNT}$	98	PA19	131	$\overline{NA}$
33	PD6	66	$\overline{TC}$	99	PA18	132	$\overline{RDY}$

1.0 PIN DESCRIPTION

The signals assigned to the different pins are grouped according to their function, and discussed individually in Table 1.

- **RESET CONTROLS**

  The Reset Control block in the FE6010 generates three levels of resets, compatible with the Model 70/80.

  — A system reset, $\overline{\text{RESET}}$, which resets all the devices in the system.

  — An 80386 reset, RES386, which only resets the 80386 microprocessor. The synchronization of this signal to the 80386 clock, CLK2, must be done externally.

  — An 80387 reset, RES387, which only resets the 80387 numeric coprocessor. Synchronizing this signal to the 80387 clock, CLK2387, must be executed externally.

> NOTE
>
> The FE6010 is compatible with both the 80386 and the 80386SX microprocessors. In the following description, any references to the system microprocessor refer to both the 80386 and the 80386SX, unless specifically stated otherwise. Similarly, any references to the NPX (Numeric coprocessor extension) refer to the both the 80387 and the 80387SX, unless explicitly stated otherwise. Section 9.0 describes the differences in implementation on an 80386 system versus an 80386SX system.

- **ARBITRATION CONTROL**

  The Arbitration Control block in the FE6010 arbitrates between different masters requesting use of the bus at the same time. The Central Arbitration Control Point (CACP) controls the arbitration timing in accordance with Channel specifications.

- **DMA CONTROLLER SIGNALS**

  The DMA Controller on the FE6010 is fully compatible with the Model 70/80 in the basic mode. In addition, the Faraday FE6010 provides an enhanced addressing mode, the 4Gig Mode, to enhance the DMA addressing capability.

> NOTE
>
> The registers implemented on the FE6010 can only be accessed by the system microprocessor.

- **NUMERIC COPROCESSOR EXTENSION (NPX) HALF-SPEED INTERFACE**

  The NPX half-speed interface allows the NPX to be operated at half the speed of the CPU. A half-speed NPX interface is useful in systems where the cost-performance requirements dictate an inexpensive coprocessor. In an 80386 system, the coprocessor used is an 80387; on an 80386SX system it is an 80387SX.

- **DECODES**

  This interface is used to diagnose errors in the system. This block implements the decodes for system-wide functions.

- **DIAGNOSTICS**

  The diagnostic signals recover the state of the bus after an error condition. For more details, see Section 7.6.

- **PARITY LATCH CONTROL**

  This signal interfaces with external parity latches and provides the capability to latch parity errors.

- **MISCELLANEOUS**

  The V_{DD} signals indicate the +5V power supply, and the V_{SS} signals indicate the 0V ground.

PIN NO.	NAME	TYPE	FUNCTION
CLOCK RESET CONTROL			
14	$\overline{\text{SHUTDOWN}}$	I	$\overline{\text{SHUT DOWN}}$ – This signal initiates a system MPU reset, and is generated by the 8X42 keyboard controller, as commanded by the system MPU.
13	PWRGOOD	I	POWER SUPPLY VOLTAGE STATUS – This signal originates in the power supply and indicates the state of the power supply voltages. Power-on Reset (POR) is derived from the state of this line.
77	$\overline{\text{RESET}}$	O	$\overline{\text{SYSTEM RESET}}$ – This system signal, generated from PWRGOOD and synchronized with CLK2, resets all the components in the system. While it is active, no memory refreshes take place.
78	RES386	O	80386 RESET – This signal is generated on System Reset, Alternate Hot Reset, Keyboard Shutdown, or Processor Shutdown cycles, and is an unsynchronized reset for the processor. It must be externally synchronized with the processor timing before being sent to the processor. On an Alternate Hot Reset or Processor Shutdown cycle, RES386 is guaranteed to stay valid for at least sixteen CLK2 periods. The pulse width of the signal is determined by the 8742 when a keyboard shutdown occurs, and by the power supply logic in case of a system reset.
79	RES387	O	80387 RESET – This reset signal is generated on a system reset or an NPX soft reset, and is an unsynchronized reset for the NPX. It must be externally synchronized before being sent to the NPX. On a system reset, the pulse width of the signal is determined by the power supply logic. On an NPX soft reset (an I/O write to Port 00F1), this signal has a pulse width of at least 256 CLK2s. When the NPX is operating at half the frequency of the 80386, the pulse width is 128 CLK2387 periods (CLK2387 period = 2*CLK2 period). The table that follows shows the sources of the resets and the signals that are asserted in response to the sources in a system containing the FE6010.

RESET SOURCE	$\overline{\text{RESET}}$	$\overline{\text{RES386}}$	$\overline{\text{RES387}}$	$\overline{\text{CHRESET}}$
Power-On	x	x	x	x
Alternate Hot Reset (Port 92, Bit 0)	—	x	—	—
Soft Channel Reset	—	—	—	x
Keyboard Shutdown	—	x	—	—
Processor Shutdown	—	x	—	—
NPX Soft Reset (Port F1)	—	—	x	—

PIN NO.	NAME	TYPE	FUNCTION
ARBITRATION CONTROL			
22 21 20 19	ARB3 ARB2 ARB1 ARB0	I/O	ARBITRATION BUS – These four open collector lines contain the state of all the Channel local arbiters after an arbitration cycle. When the ARB/$\overline{\text{GNT}}$ line goes to the Grant state, the master or the slave adapter owning that arbitration level is given ownership of the Channel bus. When the floppy controller requests the bus through FDDRQ, these lines are driven by the FE6010.
12	INTR	I	INTERRUPT – If Bit 4 of the CACP register (0090H) is set, and a bus master other than the system CPU is using the bus, this interrupt signal is used to initiate an arbitration cycle. This allows the system CPU to service the interrupt during bus master cycles.

0 = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
18	PREEMPT	I/O	PREEMPT – This open collector line signals that a Channel adapter wants to use the bus, and the CACP initiates an arbitration cycle when the line is asserted. A floppy controller request, a refresh cycle request, or receipt of an NMI causes the line to be driven by the CACP.
15	BURST	I	BURST – This signals that the current Channel bus owner will continue to hold the bus for more than one transfer. For DMA transfers, BURST is removed during the last I/O bus cycle of the transfer or during TC if the terminal count is reached. To prevent more transfers from taking place, BURST must be de-asserted in accordance with Channel timings.
7	EOT	I	END-OF-TRANSFER SIGNAL – This signal from the FE6022 (Address Buffer Mode) indicates an End-of-Transfer condition. It is activated when both CMD and S(1:0) are inactive on the Channel. Internally, it is ORed with BURST to show an End of Cycle condition. This information is used by the CACP.
8	REFREQ	I	REFRESH REQUEST – This signal is generated by the FE6000 to request a refresh cycle. The FE6010 responds by driving the PREEMPT signal. The CACP enters the ARB state and requests the local CPU bus. The refresh cycle is executed and the bus returned to the GNT state. If the CACP is already in the ARB state, the refresh request extends the period by one bus cycle. Depending on the FREF bit in the Memory Control Register, the FE6000 generates Fast Refreshes (every 0.8 us, FREF = 0) or normal refreshes (every 15.1 us, FREF = 1).
125	FDDRQ	I	FLOPPY DISK REQUEST – This signal indicates that the floppy disk controller requires the DMA transfer services. The CACP translates this request into Arbitration Level 2 and competes on the Channel.
121	DACK	I/O	DMA REQUEST ACKNOWLEDGE – This pin has two functions. Normally it is an output signal to the floppy controller, which, when active, initiates a single I/O read or write transfer. Multiple transfers are only initiated if BURST is also active. At power-on, it is an input signal. The state of this pin is sampled on the trailing edge of RESET and is used to determine whether the FE6010 will operate in an 80386-compatible or 80386SX-compatible mode.
65	ARB/GNT	O	ARBITRATION/GRANT – This signal indicates the state of the system arbiter. In the ARB state (high), all local arbiters and adapters must remove their drivers from the bus. Local arbiters may compete for Channel ownership by comparing their arbitration levels on a bit-for-bit basis. At the end of the ARB time (a minimum of 300 ns), the Channel is given to the owner of the winning arbitration level, and the change is signified by the change in the polarity of the line to GNT (low). 129
129	HLDA	I	HOLD ACKNOWLEDGE – The CPU assesses HLDA in response to a HOLD signal and indicates that it has relinquished the local bus.
63	HOLD	O	HOLD – This signal is synchronous with CLK2. When asserted, it requests the 80386 to relinquish the local bus for a Refresh, DMA, or Channel master transfer.
119	NMI	I/O	NON-MASKABLE INTERRUPT – When driven by the FE6010 to the system MPU, NMI indicates that the CACP has reached a bus time-out condition while monitoring the Channel bus. When the signal is received from the FE6000, it tells the CACP to initiate an arbitration cycle to remove any bus masters so that the system MPU can service the NMI.

O = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
67	$\overline{\text{REFRESH}}$	O	$\overline{\text{REFRESH}}$ – This Channel signal indicates that the memory read operation on the bus is a refresh cycle. The PA address lines (10:2) and $\overline{\text{BE}}$ (3:0) hold the state of the refresh address counter in the DMA controller. The upper address lines are driven to zero. In response, the FE6030 performs a memory read operation on the Channel and a RAS-only refresh for the mother board DRAM. On the Channel, any slave can choose to extend the cycle by de-asserting CHRDY.
126	UCHMSTR	I/O	CHANNEL MASTER – The Channel Master signal becomes active when a Micro Channel master other than the 80386 or the motherboard DMA controller gets control of the bus. At power-up, this pin functions differently. The state of the signal is latched on the trailing edge of $\overline{\text{RESET}}$, and is used in conjunction with F0 (A20GTX) to determine the frequency at which the system will operate. FREQUENCY / UCHMSTR (F1) / A20GTX (F0) 16 MHz / 0 / 0 20 MHz / 0 / 1 25 MHz / 1 / 1
DMA CONTROL			
3 1	CLK CLK2	I	CLOCK SIGNALS – Both signals are CMOS-level clock signals. CLK2 has a frequency twice that of the processor clock frequency, and the FE6010 shares this signal with the CPU. CLK has the same frequency as the processor. At system reset, it has the same phase relationship with CLK2 as the internal CLK of the CPU.
71 70 69 68	$\overline{\text{BE3}}$ $\overline{\text{BE2}}$ $\overline{\text{BE1}}$ $\overline{\text{BE0}}$	I/O	$\overline{\text{BYTE ENABLE}}$ – These byte enable signals indicate the byte to which the data is transferred. During a DMA operation they are output signals. When the system CPU accesses the FE6010 registers, they are input signals. The definition of these signals changes to match the type of microprocessor (80386 or 80386SX), as configured by $\overline{\text{DACK}}$ at power-up. SIGNAL / 80386 SYSTEM / 80386SX SYSTEM $\overline{\text{BE3}}$ / $\overline{\text{BE3}}$ / Not connected $\overline{\text{BE2}}$ / $\overline{\text{BE2}}$ / PA1 $\overline{\text{BE1}}$ / $\overline{\text{BE1}}$ / $\overline{\text{BEH}}$ $\overline{\text{BE0}}$ / $\overline{\text{BE0}}$ / $\overline{\text{BEL}}$
84 85 86 88 89 90 91 92 93 94 96	PA31 PA30 PA29 PA28 PA27 PA26 PA25 PA24 PA23 PA22 PA21	I/O	CPU ADDRESS BUS – This is a bi-directional address bus between the processor and the DMA. During CPU accesses to FE6010 registers, these are input signals, and during DMA transfers they are output signals. During DMA transfers in the IBM compatibility mode, which is the power-on default, the FE6010 drives PA (23:2) according to the programmed addresses. Bits (31:24) are always driven to zero. In Enhanced Addressing Mode all the bits are driven according to the programmed addresses. When the FE6010 is used in a 80386SX system, Address Bits (31:24) should be left unconnected.

O = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
97	PA20	I/O	CPU ADDRESS BUS – (Cont'd)
98	PA19		
99	PA18		
101	PA17		
102	PA16		
103	PA15		
104	PA14		
105	PA13		
106	PA12		
107	PA11		
109	PA10		
110	PA9		
111	PA8		
112	PA7		
113	PA6		
114	PA5		
115	PA4		
117	PA3		
118	PA2		
	PD (31:0)	I/O	CPU DATA BUS – This bi-directional data bus between the CPU and the FE6010 is used to transfer data during DMA and CPU accesses of FE6010 registers. The FE6010 has a 32-bit data bus interface compatible with the 80386. However, DMA transfers are always in 8-bit or 16-bit blocks. The FE6010 performs internal swaps and asserts the correct byte enables to put the data in the right word. It handles misaligned transfers by generating the multiple cycles needed to complete the transfer. The FE6010 performs dynamic bus sizing to accomodate 16-bit and 32-bit devices on a cycle-by-cycle basis, accomplishing this by sampling the BS16 output. The combinations of byte enables asserted for different transfers are tabulated below.
62	PD31		
61	PD30		
60	PD29		
59	PD28		
58	PD27		
57	PD26		
56	PD25		
54	PD24		
53	PD23		
52	PD22		
51	PD21		
49	PD20		
48	PD19		
47	PD18		
46	PD17		
45	PD16		
44	PD15		
42	PD14		
41	PD13		
40	PD12		
39	PD11		
38	PD10		
37	PD9		
36	PD8		
34	PD7		
33	PD6		
32	PD5		
31	PD4		
30	PD3		
29	PD2		

VALID DATA BUS SIGNALS	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	BYTE/WORD
PD (7:0)	1	1	1	0	Byte 0
PD (15:8)	1	1	0	1	Byte 1
PD (23:16)	1	0	1	1	Byte 2
PD (31:24)	0	1	1	1	Byte 3
PD (15:0)	1	1	0	0	Word 0
PD (23:8)	1	0	0	1	Word 1
PD (31:16)	0	0	1	1	Word 2

The next table shows the way in which the FE6010 splits misaligned transfers into multiple bus cycles. In each cycle, it samples BS16 and adjusts the transfer accordingly.

	DATA TRANSFER SIZE (In Bytes)				
	1	2			
Physical Address (PA Bus)	xx	00	01	10	11
Transfer Cycles over PD Bus	B	W	LB HB	W	LB* HB

O = Output, I = Input, I/O = Bi-directional

<table>
<tr><th>PIN NO.</th><th>NAME</th><th>TYPE</th><th>FUNCTION</th></tr>
<tr><td>27
26</td><td>PD1
PD0</td><td>I/O</td><td>Legend:
Transfers in bold letters indicate that $\overline{BS16}$ was active when sampled.
B – Byte
W – Word
HB – High Order Byte
LB – Low Order Byte
* – The 80386 will first transfer the HB, and then the LB.

If the $\overline{BS16}$ output is tied low permanently, the FE6010 data bus interface generates a 16-bit interface compatible with the 80386SX. In this mode, data bits PD (31:16) should not be connected as they have a weak internal pull-up. The combinations of byte enables asserted in an 80386SX system are tabulated below.

<table>
<tr><th>VALID DATABUS SIGNAL</th><th>$\overline{BE3}$</th><th>$\overline{BE2}$ (PA1)</th><th>$\overline{BE1}$ (NBEH)</th><th>$\overline{BE0}$ (NBEL)</th><th>BYTE/WORD</th></tr>
<tr><td>PD (7:0)</td><td>x</td><td>0</td><td>1</td><td>0</td><td>Byte 0</td></tr>
<tr><td>PD (15:8)</td><td>x</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>PD (15:0)</td><td>x</td><td>0</td><td>0</td><td>0</td><td>Word 0</td></tr>
<tr><td>PD (7:0)</td><td>x</td><td>1</td><td>1</td><td>0</td><td>Byte 2</td></tr>
<tr><td>PD (15:8)</td><td>x</td><td>1</td><td>0</td><td>1</td><td>Byte 3</td></tr>
<tr><td>PD (15:0)</td><td>x</td><td>1</td><td>0</td><td>0</td><td>Word 1</td></tr>
</table></td></tr>
<tr><td>132</td><td>$\overline{RDY}$</td><td>I</td><td>80386 READY SIGNAL – This signal is the same as the Ready signal to the CPU, and is used to track the bus cycles on the CPU local bus. It is synchronized with the system clock.</td></tr>
<tr><td>73</td><td>$\overline{ADS}$</td><td>I/O</td><td>80386 ADDRESS STROBE SIGNAL – When the CPU is in control of the bus, the CPU Address Strobe signal is an input used to track bus cycles. When the DMA controller is in control of the bus, this signal is output. Its timings are identical to those of the CPU, and the signal supports pipelined and non-pipelined cycles.</td></tr>
<tr><td>131</td><td>$\overline{NA}$</td><td>I</td><td>80386 NEXT ADDRESS – The Next Address signal is typically generated by the FE6030 in an 80386 system. It is shared with the CPU and asserted whenever a pipelined cycle is required by the system. When this signal is asserted and the FE6010 has an internal request pending, the FE6010 goes into pipelined mode. On the FE6010, this is an input-only signal, that is only applicable during DMA transfers. Figure 4 illustrates a non-pipelined transfer and Figure 5 illustrates a typical pipelined transfer.</td></tr>
<tr><td>130</td><td>$\overline{BS16}$</td><td>I</td><td>BUS SIZE 16 – This system-driven signal is generated by the FE6030 in an 80386 system, and is the same as the $\overline{BS16}$ input to the 80386. It indicates whether the current access is to a 16-bit port. When $\overline{BS16}$ is found asserted during DMA transfers, the FE6010 adjusts its bus transfers as shown in the table on splitting misaligned transfers in the description of the PD signals.

On an 80386SX-based system this signal should always be tied low, as such a system has a 16-bit data path.</td></tr>
<tr><td>74</td><td>MIO</td><td>I/O</td><td>MIO SIGNAL – The MIO signal is tied to the CPU MIO signal, acting as input when the 80386 has control of the bus. When the DMA controller controls the bus, this signal is output, with timings identical to those of the CPU, including in pipelined and non-pipelined modes.</td></tr>
</table>

O = Output, I = Input, I/O = Bi-directional

<table>
<tr><th>PIN NO.</th><th>NAME</th><th>TYPE</th><th>FUNCTION</th></tr>
<tr><td>75
76</td><td>DC
WR</td><td>I/O</td><td>DC AND WR SIGNALS - These signals are tied to the CPU DC and WR signals respectively. Together with MIO, they identify the type of bus cycle being executed on the CPU bus. They are input when the CPU has bus control, and output when the FE6010 has control of the bus. The following table shows the encoding of the control signals and their compatibility with the 80386 signals.
<table>
<tr><th>MIO</th><th>DC</th><th>WR</th><th>FE6010 OPERATION</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Does not occur</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>I/O Write</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Does not occur</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory Read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Memory Write</td></tr>
</table></td></tr>
<tr><td>66</td><td>$\overline{TC}$</td><td>O</td><td>$\overline{\text{TERMINAL COUNT}}$ – The Terminal Count signal, generated duing the last I/O bus cycle of a DMA transfer, indicates that the DMA channel currently servicing the Channel has reached a terminal count condition. The timing on this signal is compatible with that required by the Channel.</td></tr>
<tr><td>4</td><td>CLK2387</td><td>I</td><td>CLOCK CONTROL – This CMOS-level clock signal generated by external circuitry corresponds to CLK2 in normal operation. In the half-speed mode, it operates at half the speed of the primary system clock, CLK2. This pin should be connected to V_{DD} when the NPX is used in Normal (Full Speed) Mode.</td></tr>
<tr><td>6</td><td>CLK387</td><td>I</td><td>CLOCK CONTROL – This CMOS-level clock signal is generated by the external circuitry, and corresponds to the CLK signal in normal mode. In the half-speed mode, it operates at half the speed of the system phase clock CLK. The clock is high in Phase 2 of the NPX and low in Phase 1. RES387 should be synchronized to CLK2387 to meet the Reset timings for the 80387. This pin should be connected to V_{DD} when the NPX is used in Full Speed Mode.</td></tr>
<tr><td>122</td><td>$\overline{ADSO}$</td><td>O</td><td>$\overline{\text{ADDRESS STROBE}}$ – This signal contains the address strobe output for the NPX. When used in Half-Speed Mode, this pin should be connected to the ADS input of the NPX. In the Full-Speed mode, this pin is a N.C.</td></tr>
<tr><td>124</td><td>$\overline{RDYO}$</td><td>I</td><td>$\overline{\text{READY}}$ – This line is the ready output from the NPX. When used in Half-Speed Mode, it allows the FE6010 to track bus cycles to the NPX. It should be connected to the $\overline{\text{READYO}}$ output of the NPX.

When used in Full Speed Mode, this pin should be conncected to V_{DD}. In this case, the $\overline{RDYO}$ output from the 80387 is used to generate $\overline{RDY}$ to the processor.</td></tr>
<tr><td>123</td><td>$\overline{RDYO387}$</td><td>O</td><td>$\overline{\text{READY}}$ – When the NPX is used in the Half-Speed Mode, this signal provides the Ready signal for the CPU, and should be connected to the logic generating $\overline{RDY}$ for the CPU. When the NPX is used in Full Speed Mode, this is left unconnected, and the $\overline{RDYO}$ output from the NPX is directly connected to the logic for $\overline{RDY}$.</td></tr>
</table>

O = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
DECODES			
81	VGAEN	O	VIDEO GRAPHICS ADAPTER ENABLE – When enabled by the Video Subsystem Enable Register (03C3), Bit 0, this signal decodes the upper address bits 31-20 for the System Board Video RAM area, 000A0000 to 000BFFFFH.
82	EDRENA	O	EXTENDED DATA REGISTER ENABLE – When active, EDRENA enables the selected ESF register to read or write. It is generated by comparing the CPU I/O address to the value stored in the ESF Pointer Register.
80	CDSETEN	O	CARD SETUP ENABLE – This timing signal decodes I/ O Addresses 0100H to 0107H with the appropriate timing for the FE6000 for channel setup cycles in the system.
DIAGNOSTICS			
24	CHRESET	I	CHANNEL RESET – A Channel Reset signal on the Micro Channel enables the latching of the bus.
25	CHCK	I	CHANNEL CHECK – Assertion of this signal disables further latching of the bus state.
9	UCHCMD	I	CHANNEL COMMAND – This signal indicates a Micro Channel command, and is a logical OR of the CMD and MMCMD signals. If enabled, the channel state is latched at the leading edge of this signal. For an 80386SX system, CMD should be inverted and tied to UCHCMD.
10	A20GATE	I	ADDRESS GATE – Whenever the 80386 generates the address, this signal gates the PA20 address bit. The signal is generated by the 8742 micro-controller.
127	A20GTX	I/O	GATE SIGNAL – A20GTX performs two functions. At power-on, it is an input signal, latched with the trailing edge of RESET. This determines the speed at which the system will operate. In normal operation, it is an output signal, acting as a gate for the Address Bit PA20. The signal is activated whenever A20GATE is active or whenever the Alternate Gate A20 bit (Port 92, Bit 1) is asserted and the CPU has the bus.
PARITY LATCH CONTROL			
120	ENPCHK	O	ENABLE PARITY CHECK – This signal is a duplication of Bit 0 of Memory Encoding Register 1 (00E1H) on the FE6030. It is used to enable/disable parity checking. The signal interfaces with the external parity latches. See the FE6030 Data Sheet for more information.
MISCELLANEOUS			
16	TEST	I	TEST PIN – This is an active low pin that facilitates board-level testing. When low, this signal tristates all outputs and bi-directional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bi-directional lines are enabled by the chip.
5 30 55 83, 100 116	V_{DD}	I	+5V POWER SUPPLY

O = Output, I = Input, I/O = Bi-directional

2 17 23 35 43 50 64 72 87 95 108 128	Vss	I	0V GROUND

Table 1. Pin Signals

Figure 4 illustrates a typical non-pipelined bus cycle for the FE6010, and shows that the bus interface for the FE6010 is identical to the 80386.

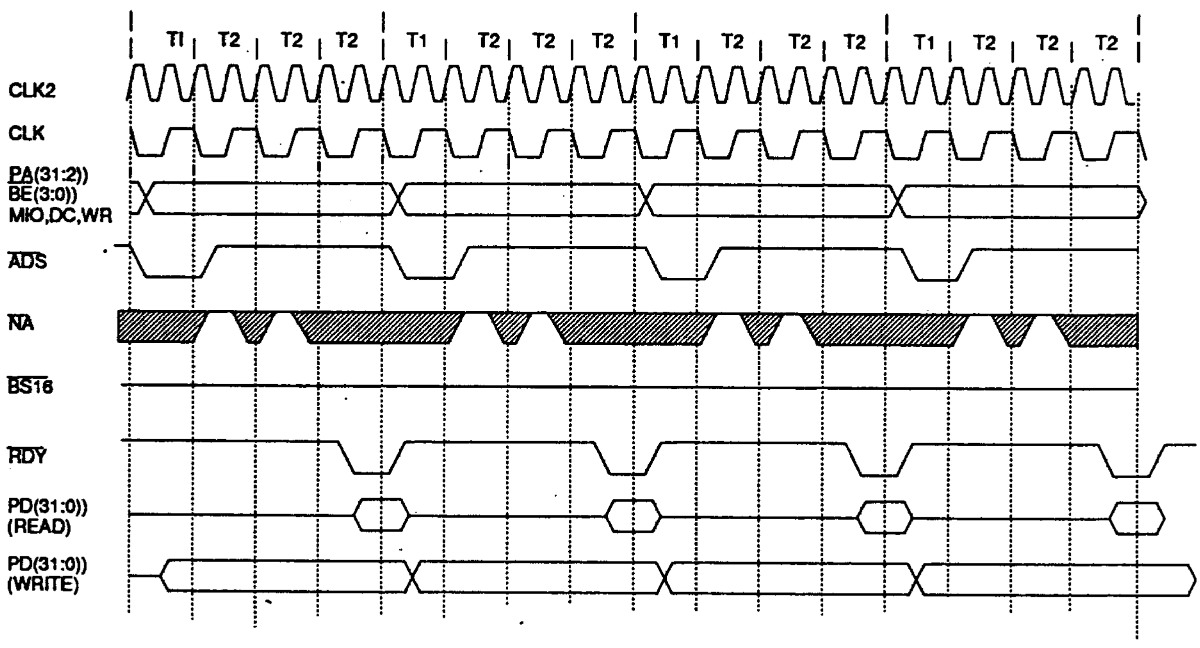


Figure 4. Non-Pipelined Mode Timing Diagram

Figure 5 illustrates a typicl Pipelined bus cycle for the FE6010. The FE6010 generates bus cycles which are identical to the 80386 bus cycles.

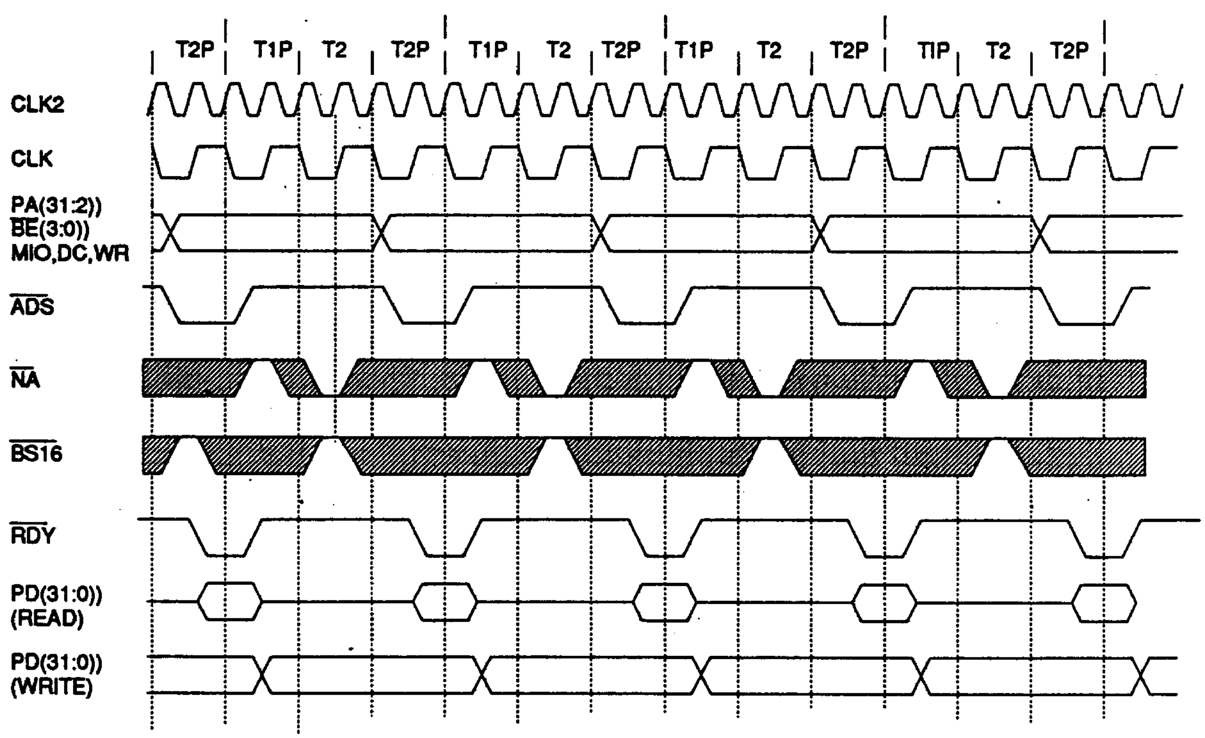


Figure 5. Pipelined Mode Timing Diagram

Table 2 shows the I/O map for the FE6500.

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	FE6010	DMA Controller Chs 0-3*
0018H	FE6010	Extended Function Reg.*
001AH	FE6010	Extended Function Execute*
0020 to 0021H	FE6000	Interrupt Controller 1
0040, 0040-0044, 0047H	FE6000	System Timers
0060H	FE6000	Keyboard Data Port
0061H	FE6000	System Control Port B
0064H	FE6000	Rd - Keyboard Status, Wr – Keyboard Command
0070H	FE6000	RTC/CMOS Address Register, NMI Mask
0071H	FE6000	RTC/CMOS Data Port
0074H	FE6000	EAR0 Extended CMOS RAM, ESF
0075H	FE6000	EAR1 Extended CMOS RAM
0076H	FE6000	Extended CMOS RAM Data Port
0081 to 0083, 0087H	FE6010	DMA Page Registers 0-3*
0089 to 008B, 009FH	FE6010	DMA Page Registers 4-7*
0090H	FE6010	CACP Register*
0091H	FE6000	Card Selected Feedback
0092H	FE6000	System Control Port A
0094H	FE6000	System Board Setup
0096, 0097H	FE6000	POS, Channel Connector Select
00A0, 00A1H	FE6000	Interrupt Controller 2
00C0 to 00DFH	FE6000	DMA Controller (even only)*
00E0 to 00E1	FE6010	Memory Control Registers
00E2 to 00E7	FE6010	Diagnostic Registers
00F0H	FE6000	Coprocessor Clear Busy
00F1H	FE6000	Coprocessor Reset
00F8 to 00FFH	NPX	80387/80387SX Coprocessor*
0100, 0101H	FE6000	System ID
0102 to 0107H	FE6000	Board Configuration (POS)
0278 to 027BH	FE6000	Parallel Port 3
02F8 to 02FFH	FE6000	Alternate Serial Port
0378 to 037BH	FE6000	Parallel Port 2
03BC to 03BFH	FE6000	Parallel Port 1
03B4, 03B5, 03BA, 03C0-03C5H	PVGA1	Video Subsystem**
03CE, 03CF, 03D4, 03D5, 03DAH	PVGA1	Video Subsystem
03C6 to 03C9H	PVGA1	Video DAC**
03F0 to 03F7H	FE6000	Diskette Drive Controller
03F8 to 03FFH	FE6000	Primary Serial Port
0700H	FE6010	ESF Data Register (Default)

* No Channel cycle generated on these addresses.
**The PVGA Enable Register (03C3H) is in the FE6010.

Table 2. System Level I/O Map

2.0 DMA CONTROLLER

The DMA Controller is a serial transfer device compatible with the Intel* 8237, and includes the IBM extended controller interface and functions. Its logic supports eight independent channels, six of which are assigned fixed priorities. The remaining two have programmable priorities.

The FE6010 takes two bus cycles to transfer a word or byte between memory and I/O. Each bus cycle needs two or more CPU clock cycles. Channel and bus arbitration functions are resolved externally.

2.1 DMA INTERFACE

The DMA Controller interfaces to the system on the CPU local bus. As the table in the description of the PD signals shows, it generates and encodes the same control signals as the 80386. The controller may be programmed at any time that Hold Acknowledge (HLDA) from the CPU is inactive. The programming may only be done by the system CPU.

Each of the two transfer bus cycles requires two or more CPU clock cycles. The time taken by the I/O portion of the cycle depends on the response from the system interface: whether it is a local cycle or a Channel cyle. All Channel cycles take at least 200 ns. The time taken by the memory portion of the cycle depends on the response from the system interface, that is, if it is a local cycle versus a Channel cycle, cache hit versus a cache miss, page hit versus a page miss, and so on.

A Channel transfer is established by the CPU setup and initiated from an external slave source through arbitration control in the form of DMAREQ input. The requesting DMA channel is specified on the ARB bus input.

2.2 INTERNAL ARCHITECTURE

The internal architecture of the DMA Controller in the FE6010 is based on the six basic modules described in the subsections that follow.

2.2.1 Address Translator

This module converts address and data information from the CPU interface that is in PC/AT Compatibility Mode format into the Extended Mode format. This information is then stored for run-time use.

2.2.2 RAM Registers

These RAM locations store the 32-bit base address, the 32-bit current address, the 16-bit base count, the 16-bit current count, and the 16-bit current I/O address, for each channel. The current values are read/write and are written by the CPU at the same time as the base registers. An additional register, the Transfer Holding Register, temporarily stores data between bus cycles of a transfer. This register can not be accessed by the system CPU.

The RAM array is 112 bits x 8 locations, with one location allocated to each channel. The Channel 0 and 4 implement the Virtual DMA feature of the Micro Channel system.

Base Memory Register

This 32-bit register is initialized by the system CPU through byte-wide accesses. This is a read/write register and can not be read by the system CPU. In Compatibility Mode, three writes are executed to program twenty-four address bits, and four writes are executed in Enhanced Addressing Mode to program thirty-two address bits.

Current Memory Register

The CPU initializes this 32-bit read/write register by byte-wide accesses at the same time that it initializes the Base Register. This register can also be read in byte-wide accesses.

During DMA transfers, this register is incremented or decremented after each memory bus cycle. Enabling Auto-Initialize reloads this register at the end of a transfer with the value stored in the Base Register. This state is reached when the DMA controller reaches a terminal count condition and the $\overline{TC}$ signal has been generated. Figure 6 illustrates a read cycle with Auto-Initialize, followed by another transfer.

Base Transfer Count Register

The system CPU initializes this 16-bit register in byte-wide accesses. The number of transfers is the value in the register + 1. The FE6010 does a single transfer when this register is programmed to 0000H.

Current Transfer Count Register

The CPU initializes this 16-bit read/write register by byte-wide accesses at the same time that it initializes the Base Register. This system CPU can read it in byte-wide accesses.

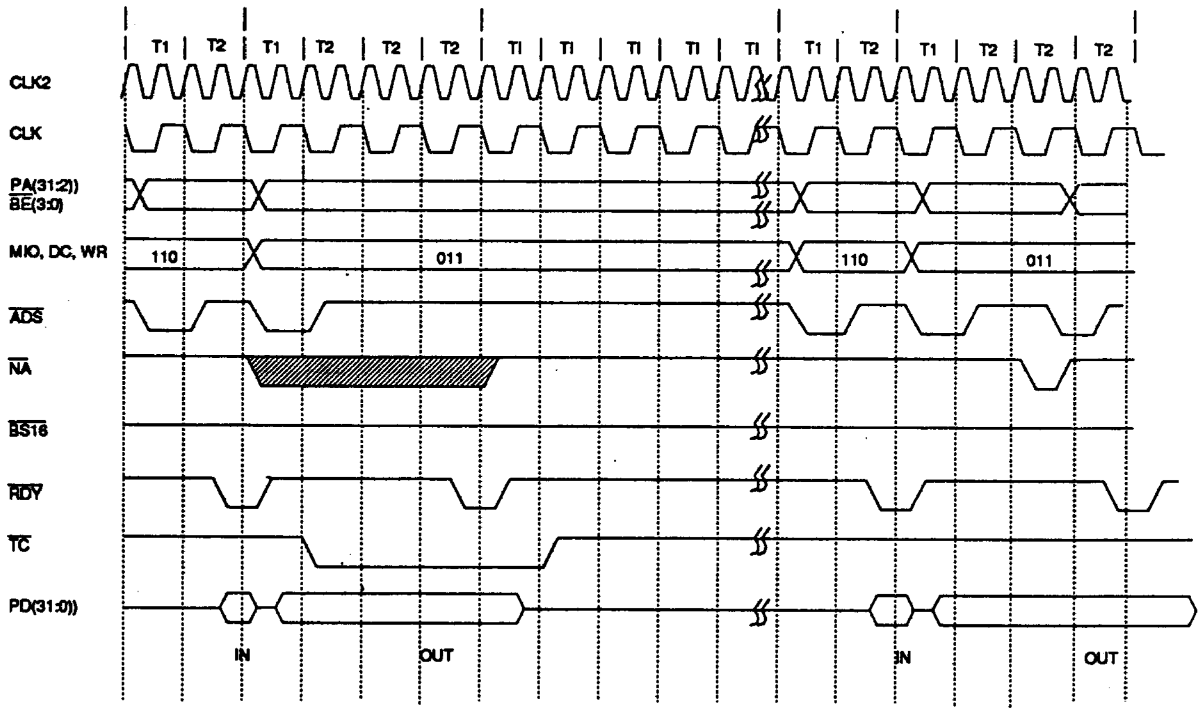


Figure 6. Read Cycle With Auto-Initialize

During DMA transfers, this register is decremented after each memory bus cycle. Enabling Auto-Initialize reloads this register at the End-of-Transfer (EOT) with the value FFFFH from the Base Register.

Current I/O Address Register

This register is initialized by the system CPU in Extended Mode only. The value gated to the bus during the I/O bus cycle depends on the state of Bit 0 in the Extended Mode Register. If Programmed I/O Address Mode is set, then the value in the register is used; if not, 0000H is used.

Temporary Holding Register

This register temporarily stores data between bus cycles of a transfer. The system CPU can not access this register.

2.2.3 DMA Registers

The DMA registers consist of the Mask, Mode, Arbus, and Status registers. Table 3 shows the allocation of these registers.

REGISTER	SIZE	QTY	ALLOCATION
MASK	4 bits	2	1 for Chs 0-3 1 for Chs 4-7
MODE	8 bits	8	1 per channel
ARBUS	4 bits	2	1 for Ch 0, 1 for Ch 4
STATUS	8 bits	2	1 for Chs 0-3

Table 3. DMA Register Allocation

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Figure 7 shows the format for the Mask register, and Figure 8 shows the format for the Mode Register. See Section 2.3 for a description of the various modes and transfer types set in the Mode Register.

RESERVED	MASK BIT		CHANNEL SELECT	
0	DIS	ENA	–	–

Set/Clear Interface

1	0	Channel
0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

RESERVED	CH 3 OR 7		CH 2 OR 6		CH 1 OR 5		CH 0 OR 4	
0	DIS	ENA	DIS	ENA	DIS	ENA	DIS	ENA

Set/Reset Interface

Figure 7. Mask Register Format

(shaded) = **Default**

MODE SELECT		COUNT DIR		AUTOINITIAL		TRANSFER TYPE		CHANNEL SELECT	
—	—	DEC	INC	ENA	DIS	—	—	—	—

7	6	Mode Select
0	0	Demand
0	1	Single (NU)
1	0	Block (NU)
1	1	Cascade (NU)

3	2	Transfer Type
0	0	Verify
0	1	Write Mem
1	0	Read Mem
1	1	Reserved

1	0	Channel
0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

PC/AT Compatible Mode

Extended Mode

RESERVED	WIDTH		RESERVED	COUNT DIR		TRANSFER		TRANSFER		AUTOINITIAL		IO ADR	
0	8 BIT XFER	16 BIT XFER	0	DEC	INC	WRITE MEM	READ MEM	DATA	VERIF	ON	OFF	PROG VALU	0000H

Figure 8. Mode Register Format

RESERVED				ARBITRATION LEVEL			
—	—	—	—	—	—	—	—

3	2	1	0	Level
0	0	0	0	0 Available
0	0	0	1	1 See Warning
0	0	1	0	2 See Warning
0	0	1	1	3 See Warning
0	1	0	0	4 Available
0	1	0	1	5 See Warning
0	1	1	0	6 See Warning
0	1	1	1	7 See Warning
1	0	0	0	8 Available
1	0	0	1	9 Available
1	0	1	0	A Available
1	0	1	1	B Available
1	1	0	0	C Available
1	1	0	1	D Available
1	1	1	0	E Available
1	1	1	1	F Reserved—System MPU

WARNING:
These levels are assigned to DMA channels 1—3, 5—7. If channel 0 or 4 is assigned to one of these levels, the user must insure that no conflict occurs.

Figure 9. Arbus Register Format

REQUEST STATUS								TERMINAL COUNT STATUS							
CHAN 3 OR 7		CHAN 2 OR 6		CHAN 1 OR 5		CHAN 0 OR 4		CHAN 3 OR 7		CHAN 2 OR 6		CHAN 1 OR 5		CHAN 0 OR 4	
YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO

Figure 10. Status Register Format

(shaded) = Default

The two Arbus registers, one each for DMA Channels 0 and 4, implement the "virtual DMA" feature. The software can use these registers to dynamically re-assign the arbitration level to which these channels respond during a DMA operation. This allows Channels 0 and 4 to service devices at any arbitration level. Normally, Channels 0 and 4 are assigned levels 08H to 0EH only, Levels 01-03H and 05-07H are assigned to DMA Channels 1-3 and 5-7. If Channels 0 or 4 are assigned one of these levels, it is up to the user to ensure that there are no conflicts. Figure 9 illustrates the Arbus register format.

In Extended Mode, a status read provides the status of Channels 0-3, and a second read gives the status of Channels 4-7. The byte pointer is initialized when the command is given. Figure 10 shows the format of the Status Register.

2.2.4 Transfer Control

This module provides the interface for the CPU bus. The signals and timings are equivalent to those of the CPU, and are generated from the same CPU clock source.

2.2.5 Register Control

This control function co-ordinates the various modules during a DMA transfer cycle.

2.2.6 Work Registers

These registers are used for the temporary storage of data and parameters during and between DMA transfer bus cycles.

2.3 SYSTEM CPU ACCESS MODES

The system CPU can access the DMA controller in two modes: PC/AT Compatibility Mode, and PS/2 Extended Mode. At run-time, the mode through which the transfer was set up is not retained.

The FE6010 does not support the Compatibility Mode command, and request and rotating priority functions. The Mode register is only supported to the extent detailed in the following subsections.

2.3.1 Compatibility Mode

Table 4 provides an I/O map of this mode.

I/O ADRS	DESCRIPTION	BIT WIDTH	BYTE PTR
0000H	Ch 0 Memory Adrs. Reg. (R/W)	15-00	yes*
0001H	Ch 0 Transfer Count Reg. (R/W)	15-00	yes*
0002H	Ch 1 Memory Adrs. Reg. (R/W)	15-00	yes*
0003H	Ch 1 Transfer Count Reg. (R/W)	15-00	yes*
0004H	Ch 2 Memory Adrs. Reg. (R/W)	15-00	yes*
0005H	Ch 2 Transfer Count Reg. (R/W)	15-00	yes*
0006H	Ch 3 Memory Adrs. Reg. (R/W)	15-00	yes*
0007H	Ch 3 Transfer Count Reg. (R/W)	15-00	yes*
0008H	Chs 0-3 Status Register	07-00	–
000AH	Chs 0-3 Mask Reg.(Set/Rst)(W)	02-00	–
000BH	Chs 0-3 Mode Register (W)	07-00	–
000CH	Chs 0-3 Clear Byte Pointer (W)	N/A	–
000DH	Chs 0-3 Master Clear (W)	N/A	–
000EH	Chs 0-3 Clear Mask Register (W)	N/A	–
000FH	Chs 0-3 Write Mask Register (W)	03-00	–
0081H	Ch 2 Page Register (R/W)	07-00	–
0082H	Ch 3 Page Register (R/W)	07-00	–
0083H	Ch 1 Page Register (R/W)	07-00	–
0087H	Ch 0 Page Register (R/W)	07-00	–
0089H	Ch 6 Page Register (R/W)	07-00	–
008AH	Ch 7 Page Register (R/W)	07-00	–
008BH	Ch 5 Page Register (R/W)	07-00	–
008FH	Ch 4 Page Register (R/W)	07-00	–
00C0H	Ch 4 Memory Adrs. Reg. (R/W)	15-00	yes*
00C2H	Ch 4 Transfer Count Reg. (R/W)	15-00	yes*
00C4H	Ch 5 Memory Adrs. Reg. (R/W)	15-00	yes*
00C6H	Ch 5 Transfer Count Reg. (R/W)	15-00	yes*
00C8H	Ch 6 Memory Adrs. Reg. (R/W)	15-00	yes*
00CAH	Ch 6 Transfer Count Reg. (R/W)	15-00	yes*
00CCH	Ch 7 Memory Adrs. Reg. (R/W)	15-00	yes*
00CEH	Ch 7 Transfer Count Reg. (R/W)	15-00	yes*
00D0H	Chs 4-7 Status Register	07-00	–
00D4H	Chs 4-7 Mask Reg.(Set/RST)(W)	02-00	–
00D6H	Chs 4-7 Mode Reg. (W)	07-00	–
00D8H	Chs 4-7 Clear Byte Pointer (W)	N/A	–
00DAH	Chs 4-7 Master Clear (W)	N/A	–
00DCH	Chs 4-7 Clear Mask Reg. (W)	N/A	–
00DEH	Chs 4-7 Write Mask Reg. (W)	03-00	–

* Both Memory Address and Transfer Count Registers are loaded on a write operation; only the Current register is readable.

Table 4. Compatibility Mode I/O Map

2.3.2. Extended Mode

This mode is accessed through four locations in the I/O space, as Table 5 shows. The format for the Extended Function Register (EFR), 0018H, is shown in Figure 11.

The protocol for Extended Mode is as follows:

1.Write to the EFR (0018H) to set the channel selection and function command. This resets the internal byte pointer to point to least significant byte (LSB). Direct commands only require an I/O write to the EFR. If it is not a direct command, go on to Step 2.

2.Write or read the appropriate number of times to execute the function from the EFE port. The byte pointer increments automatically.

Direct commands written to the EFR include Mask Register Set Bit, Mask Register Reset Bit, and Master Clear. The Mask Register Set Bit command masks or disables all the channels in the Mask Register. The Mask Register Reset Bit command unmasks or enables all the channels in the Mask Register. The Master Clear can be generated by the CPU or by a bus time-out condition. If a Master Clear command is given, the DMA controller must be re-initialized. The Master Clear masks all the channels in the Mask Register, that is, it sets all the bits to one. It also resets the Status Register by setting all the bits to zero.

I/O ADDRESS	DESCRIPTION
0018H	Extended Function Register (EFR) (W)
0019H	Reserved
001AH	Extended Function Execute (EFE) (W)
001BH	Reserved

Table 5. Extended Mode I/O Addresses

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PROGRAMMED COMMAND (1AH)								RESERVED				CHANNEL SELECTION			
BIT 7		BIT 6		BIT 5		BIT 4		0		BIT 2		BIT 1		BIT 0	

7	6	5	4	Command	Bit Width	Byte Ptr
0	0	0	0	0 IO Adr Reg (R/W)	00–15	yes
0	0	0	1	1 Reserved	—	—
0	0	1	0	2 Mem Adr Reg (R/W)	00–23	yes
0	0	1	1	3 Mem Adr Reg Read	00–23	yes
0	1	0	0	4 Xfer Cnt Reg (R/W)	00–15	yes
0	1	0	1	5 Xfer Cnt Reg Read	00–15	yes
0	1	1	0	6 Status Reg Read	00–07	yes
0	1	1	1	7 Mode Reg (R/W)	00–07	—
1	0	0	0	8 Arbus Reg (R/W)	00–07	—
1	0	0	1	9 Mask Reg Set Bit	Direct	—
1	0	1	0	A Mask Reg Reset Bit	Direct	—
1	0	1	1	B IBM Test DRQ (NU)	—	[1]
1	1	0	0	C IBM Test Clear (NU)	—	[1]
1	1	0	1	D Master Clear	Direct	—
1	1	1	0	E Reserved	—	—
1	1	1	1	F Reserved	—	—

[1] These functions are not implemented

2	1	0	Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 11. Extended Function Register (EFR) (0018H)

2.3.3 Enhanced Mode

The DMA Controller Enhanced Mode is a Western Digital innovation implemented on the FE6010 which extends the DMA address space up to 4 Gbytes. A DMA operation can now take place in Memory Addresses 0000,0000 to FFFF,FFFFH.

The FE6010 powers up in a mode compatible with the Model 80, which allows DMA operation in Compatibility Mode or Extended Mode. The memory address space in which a DMA operation can take place extends from 00,0000 to FF,FFFFH. If the addresses exceed FF,FFFF, they roll over to 000000. Address Bits 23 to 31 are always zero in this mode.

Setting the Mode4 Gig bit in the Enhanced Addressing Register (ESF:018CH) puts the FE6010 in Enhanced Mode. In this mode, the addresses roll over to 0000,0000 if they exceed FFFF,FFFFH, instead of FF,FFFFH.

When in this mode, all the channels generate 32-bit addresses. To program the memory addresses for thirty-two bits, four writes to the Memory Address Register should be executed in Extended Mode. To read back the memory addresses, four reads are executed to the same locations. Internally, the bytes are organized as Bytes 0,1,2, and 3. If the upper-most byte is not programmed, the old value is used. Therefore, care must be taken to program all the bytes with their proper values. Figure 12 shows the bit assignment for Register ESF:18CH.

2.4 DMA OPERATION

The state of the HLDA signal from the CPU distinguishes the operaion of the DMA controller. If HLDA is inactive, the operating mode of the DMA controller can be programmed. See Section 5, Arbitration Control, for more information. If HLDA is active, the DMA can only execute transfer cycles that have been set up previously.

To terminate a transfer, the DMA controller examines the state of the $\overline{BURST}$ signal. As long as this signal is active and the terminal count (TC) has not been reached, transfers continue to be executed. If $\overline{BURST}$ is inactive at the beginning of a transfer, a single transfer is executed. After it has been asserted, $\overline{BURST}$ always deasserts during the I/O cycle.

2.4.1 Single Transfer Mode

This mode consists of one I/O bus cycle and one memory bus cycle, in either order. A single transfer is executed when $\overline{BURST}$ is found to be inactive at the beginning of a cycle.

2.4.2 Demand Transfer Mode

Demand transfers are continous transfers carried out as long ast the $\overline{BURST}$ signal remains active. They may be either slave-terminated or controller-terminated.

A slave-terminated transfer ends under either of two conditions. The transfer ends when the slave has transferred one byte or word and has not asserted the $\overline{BURST}$ signal, or when the slave has completed a partial transfer and releases $\overline{BURST}$ during the last I/O cycle.

A controller-terminated transfer can only end when the TC has been reached for that channel. At EOT, the channel is masked from further operation until the system CPU interacts with it. Figures 13 to 15 provide timing diagrams of typical DMA operations in Demand Transfer Mode.

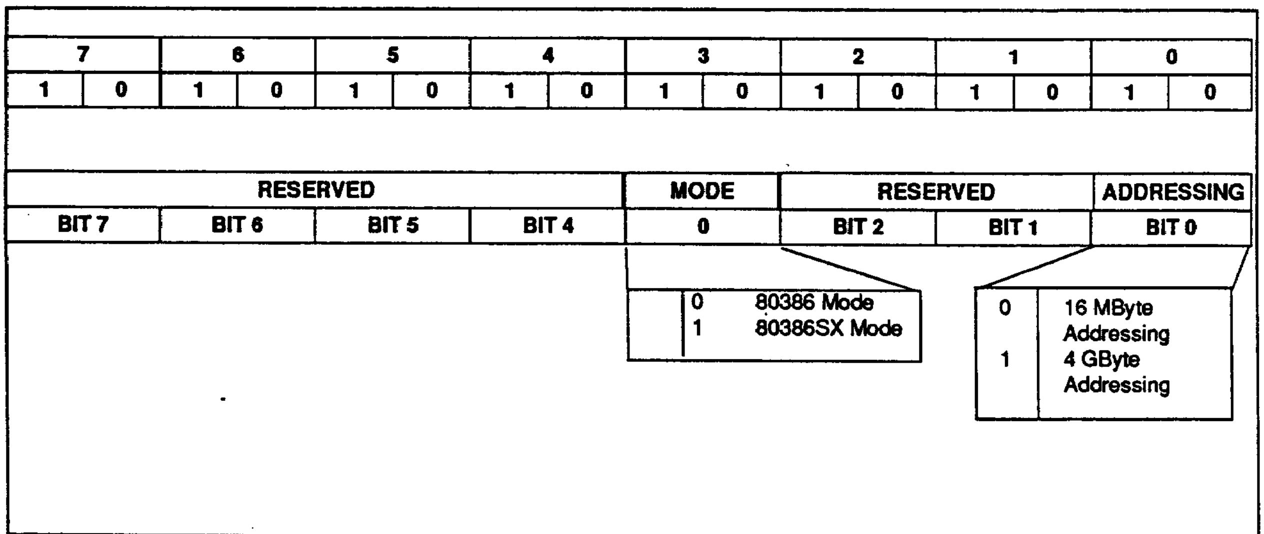


Figure 12. Enhanced Addressing Register ESF:018CH

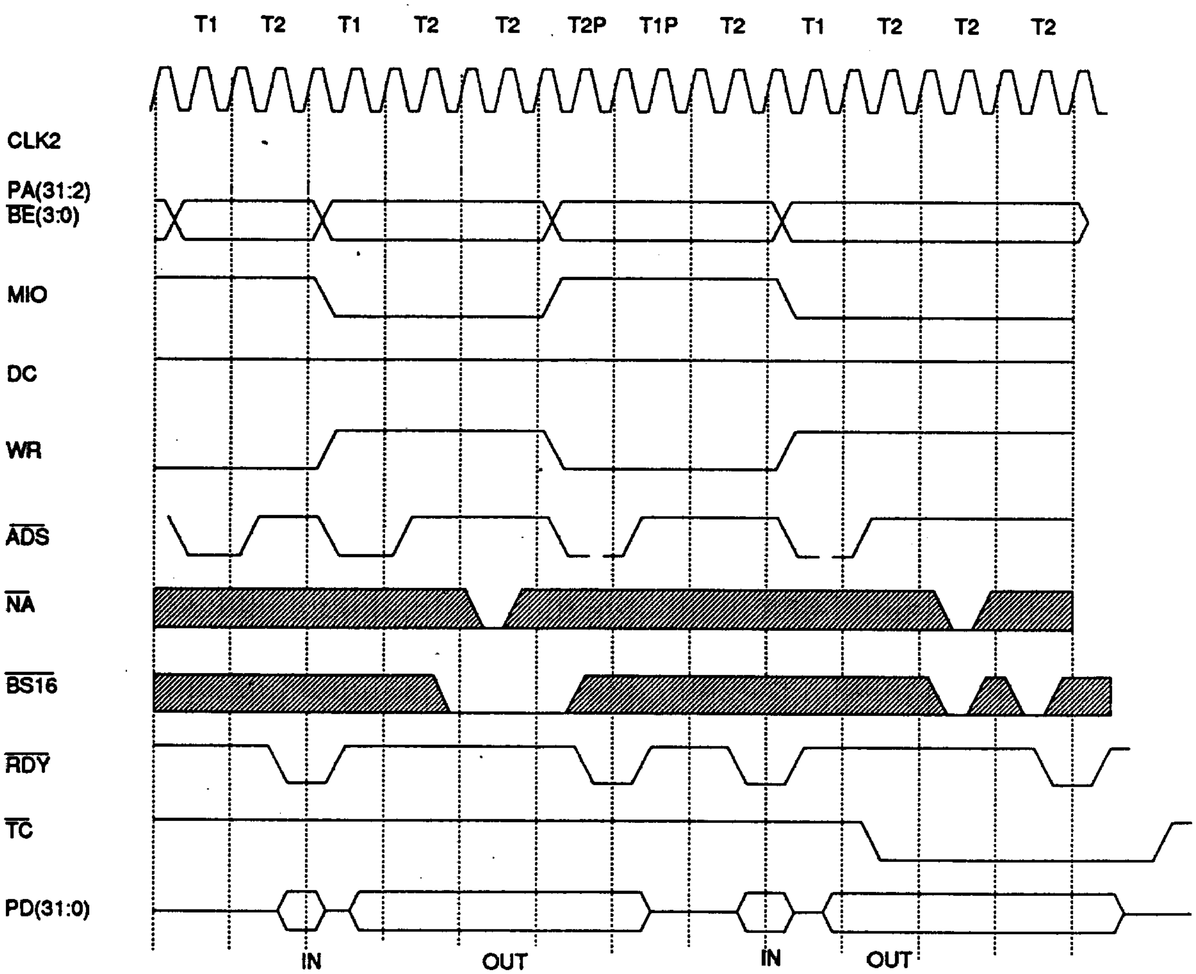


Figure 13. 16-Bit Read Transfer With Transfer Count Expiration

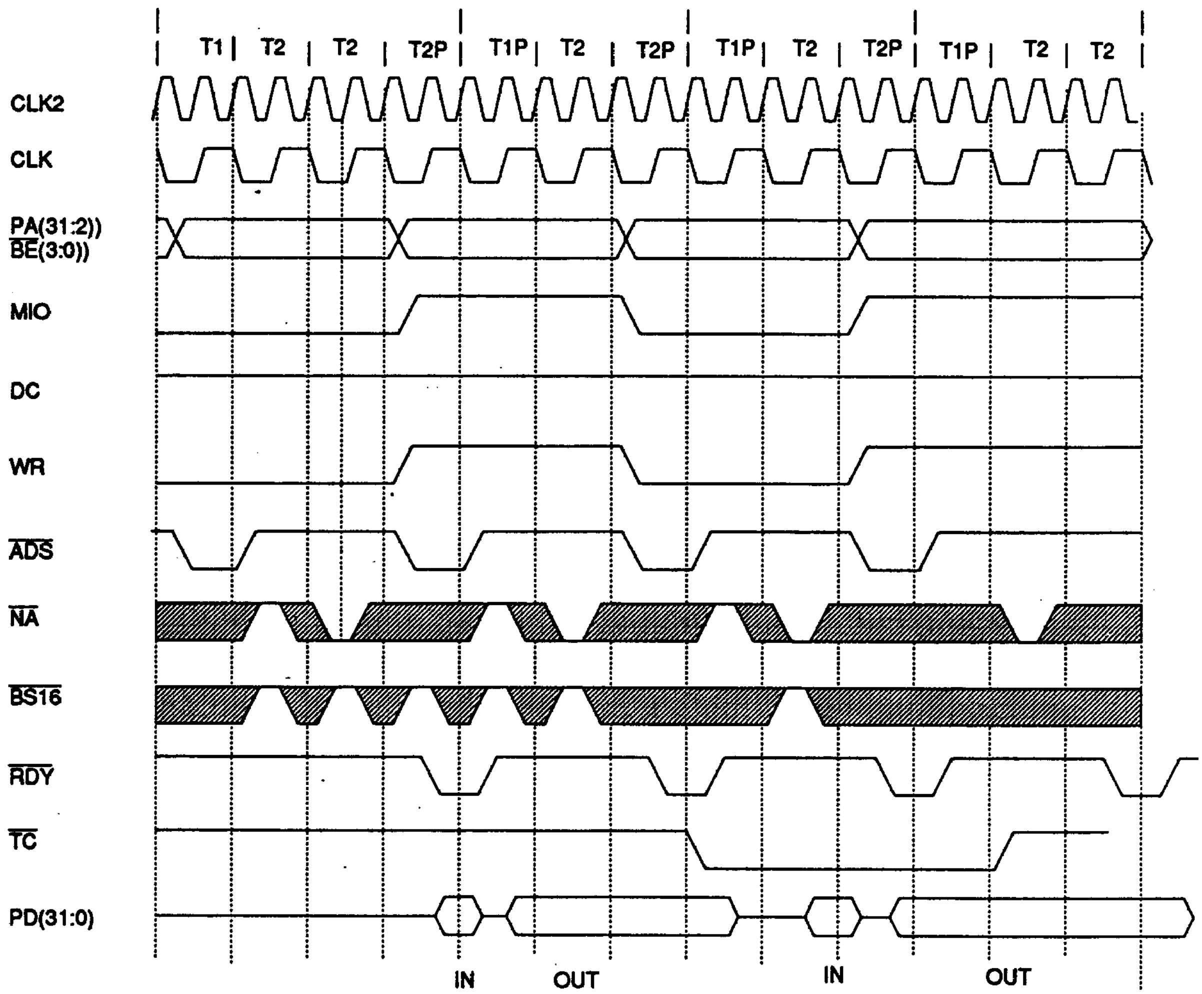


Figure 14. 16-Bit Write Transfer with Transfer CountExpiration

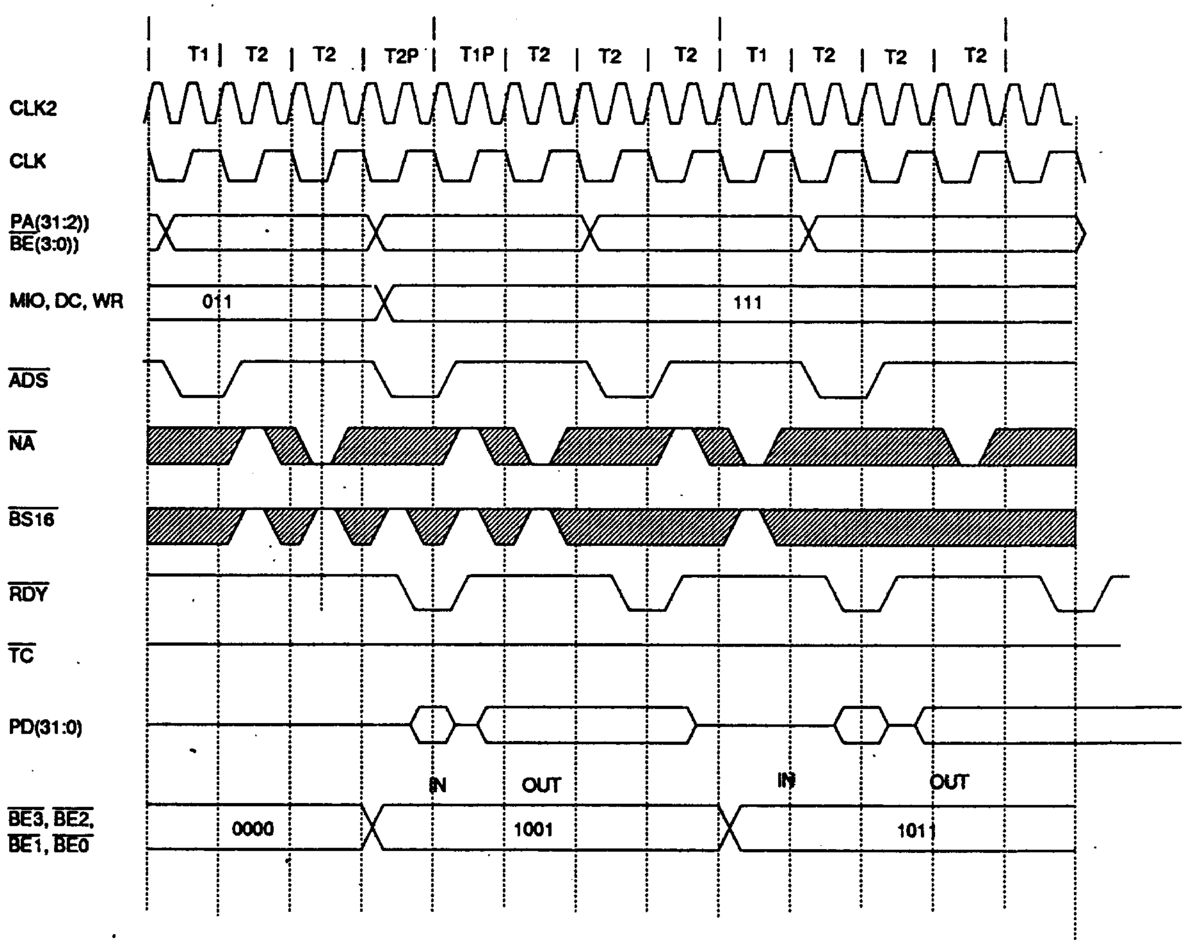


Figure 15. Write Cycle At Address N + 1 To 16-Bit Memory, Illustrated with 2 Wait States

2.4.3 Verify Mode

This mode performs address and TC generation as in normal transfers, but only initiates memory read commands on the bus. Figures 16 and 17 illustrate this mode through timing diagrams.

2.4.4 Submodes

Auto-initialize Mode allows a channel to operate continuously without interaction from the CPU. At EOT, the values in the base registers are loaded into the current registers; the channel remains unmasked.

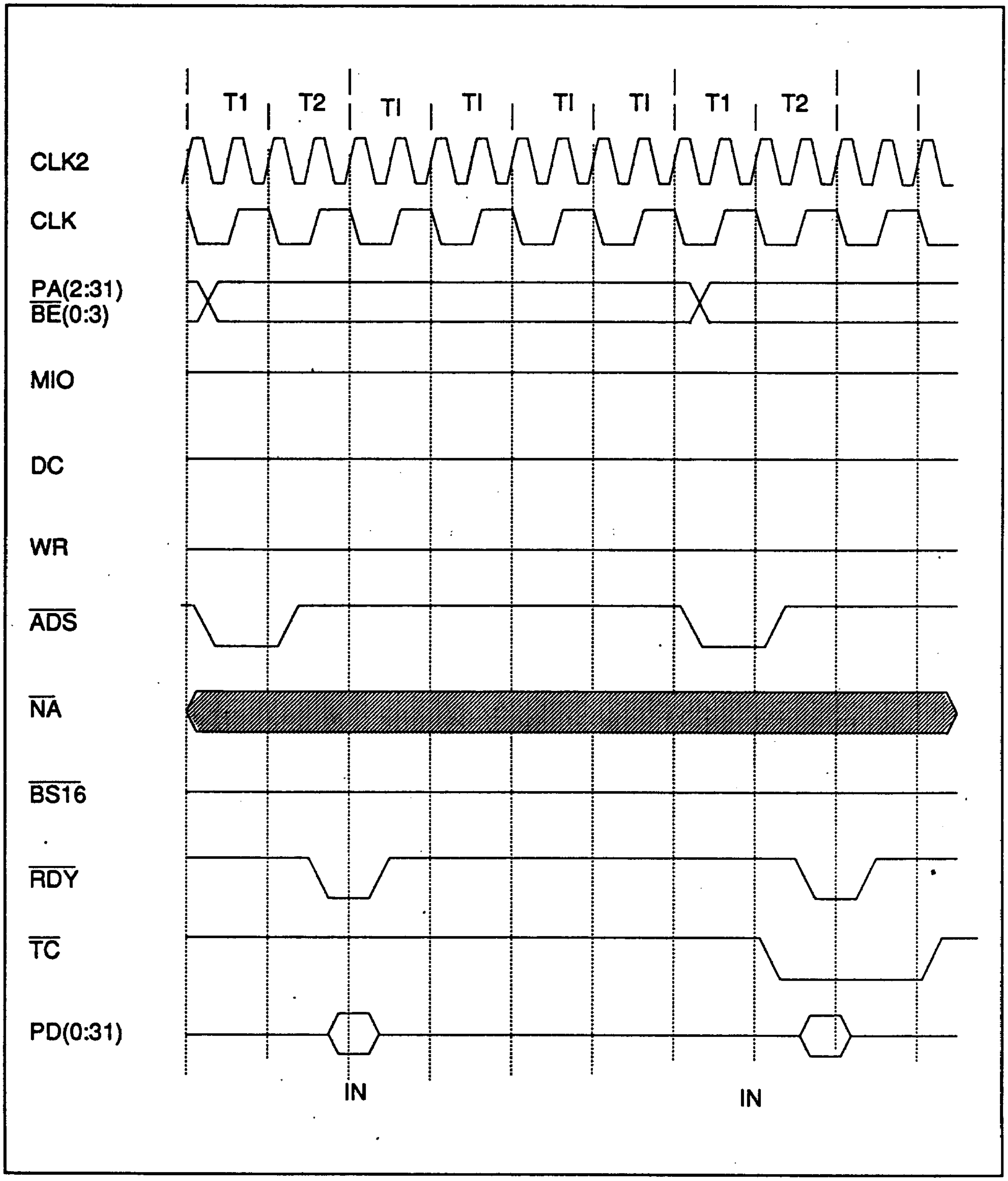


Figure 16. Verify Transfer With Transfer Count Expiration

The Increment/Decrement submode can set each channel Memory Address Register to increment or decrement.

2.4.5 Boundary And End Conditions

When the Memory Address Register reaches the end of a 64 Kbyte segment of memory, it carries into the upper byte of the counter without indicating this to the system CPU.

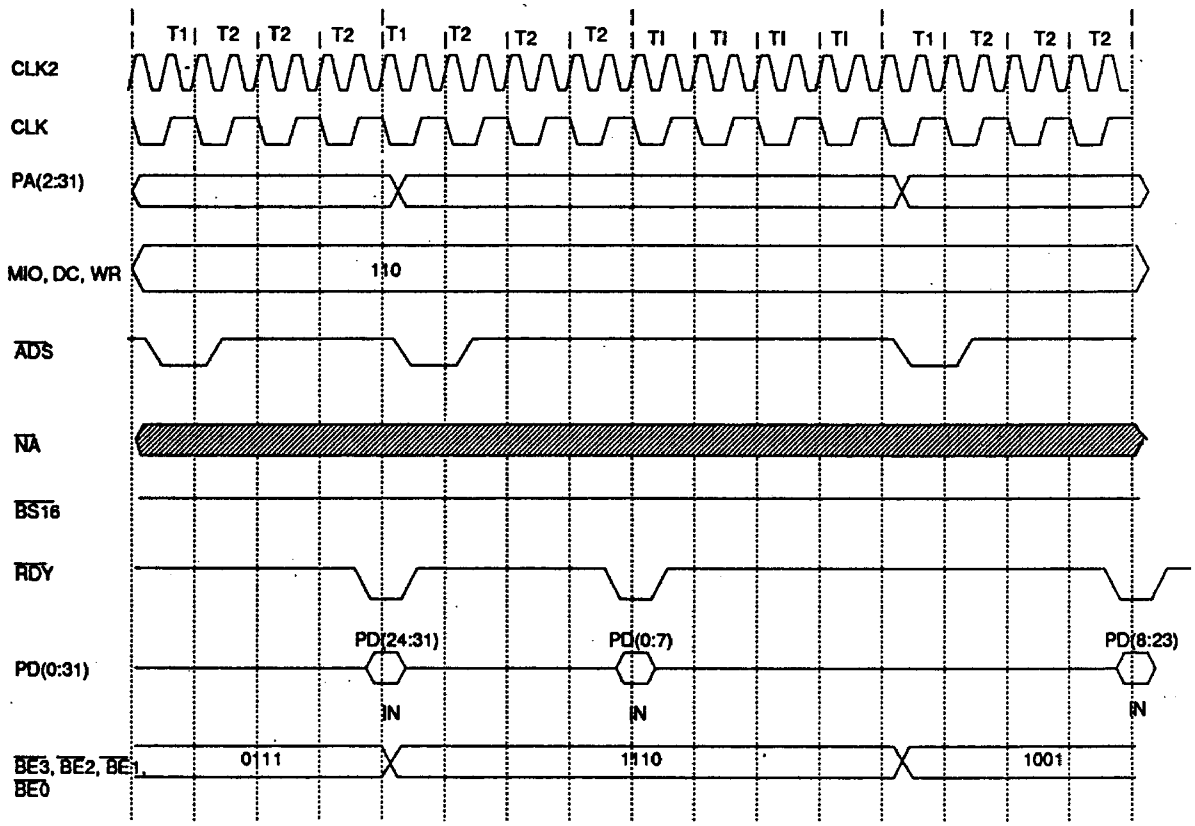


Figure 17. Verify Cycle At Address N + 3

With a 16M or 4 GByte physical memory limit, if the Transfer Count Register has a valid count remaining and the DMA slave continues to request service, the Memory Address Register rolls over to Address 0 and continues. If the transfer is a memory write, no warning is given of the alteration to low memory.

At TC, the Transfer Count Register decrements to FFFFH and stops. If the register was initially set to FFFFH, the counter decrements until it encounters FFFFH again.

At EOT, the mask register bit is not set if Auto-Initialize was selected for that channel, as this would disable the channel.

2.4.6 Direct Commands

The Clear Byte Pointer command initializes the internal byte pointer to point to the least significant byte.

The Master Clear command sets the Mask Register to mask or disable all channels. It also resets all status bytes to zeros.

The Clear Mask Register command unmasks or enables all the channels.

The Write All Register Mask Bits command masks or disables all the channels.

2.4.7 Enhanced Mode

All the DMA operations described in this section are valid when the system is operating in Enhanced Mode. However, it must be remembered that all channels generate 32-bit addresses when in this mode, necessitating four read or write operations to program the memory addresses. See Section 2.3.3 for more information.

3.0 RESET CONTROL

The clock and reset control functions on the FE6010 include the generation of CPU resets, coprocessor resets, and general system resets.

The Alternate Hot Reset Function specified by Control Port A (0092H, Bit 0) is write-only in the FE6010 and read/write on the FE6000. Figure 19 shows the Clock and Reset control function in an FE6010-based system. The block diagram shows an FE6500 system; however, the same architecture applies to any system based on the FE6010.

FREQUENCY	UCHMSTR	A20GTX
16 MHz	0	0
20 MHz	0	1
25 MHz	1	1
33 MHz	1	0

Table 6. Clock Rate Definitions

The generation of different resets is described in the Pin Description Table.

The clock rates and the signal pins are shown in Table 6. The state of three signal pins at power-on reset (POR) determines the clock rates. After POR, the pins revert to their normal functions.

4.0 ARBITRATION CONTROL (AC)

Arbitration Control controls and monitors the Channel and local bus arbitration functions. The AC functions are controlled by the bit settings in the Arbitration Register at 0090H. Figure 10 shows the format for the Arbitration Register.

4.1 ARBITRATION REGISTER

The Arbitration Register (0090H) controls the different functional parameters of the CACP. Figure 19 shows the bit assignments for this register for read and write operations.

4.2 ARBITRATION CONTROL FUNCTIONS

The Central Arbitration Control Point (CACP) functions are discussed in more detail in the subsections that follow.

	7		6		5		4		3		2		1		0	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Read	CPU CYCLES		NMI OCCURRED		BUS TIMEOUT		IRQ MASTER PREEMPT		ARBITRATION LEVEL							
	ENA	DIS	YES	NO	YES	NO	ENA	DIS	0 = LSB							
Write	CPU CYCLES		ARB STATE		ARB CYCLE		IRQ MASTER PREEMPT		RESERVED							
	ENA	DIS	ARB	GNT	EXTD	NORM	ENA	DIS	—		—		—		—	

Figure 18. Arbitration Register Format (0090H)

Shaded (DIS, NO, NO, DIS; DIS, ARB, NORM, DIS) = Default

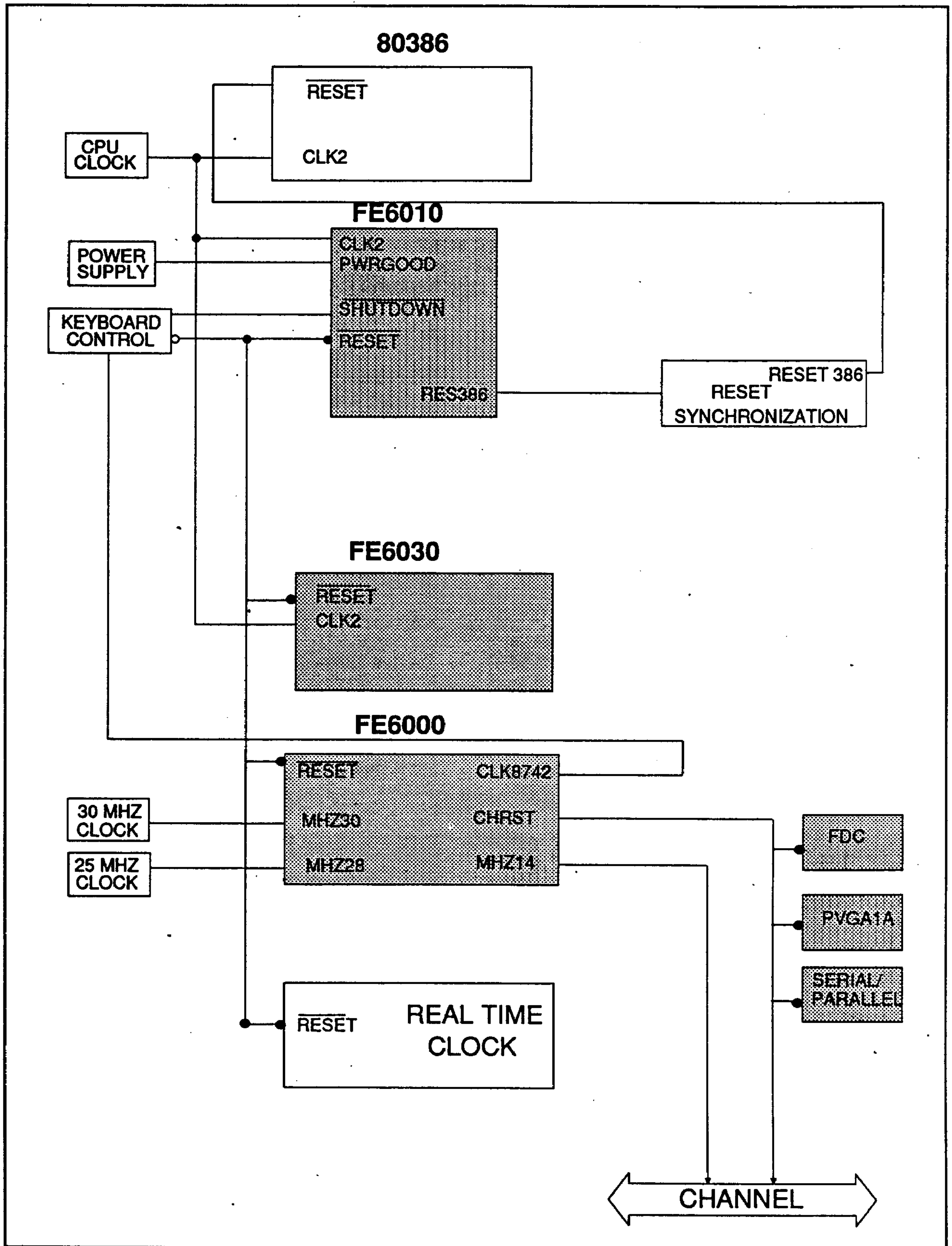


Figure 19. System Clock and Reset Control

4.2.1 Execute Arbitration Cycles

An arbitration cycle is defined as a transition of the ARB/$\overline{GNT}$ signal from low to high to low, Grant to ARB to Grant. When it is high (ARB), all competing local arbiters may drive Arb (3:0) to determine the new bus owner. Refresh cycles are executed when ARB is high and extend the arbitration cycle by that amount. An arbitration cycle can be initiated by these external requests:

- Refresh Request
- Bus Time-out
- Competing Bus Master
- Competing DMA Slave
- NMI
- Bus Idle
- Interrupt, When 0090H, Bit 4 is 1

The bus is said to be idle when a Bus Master or DMA slave has been granted the bus, and there are no bus control signals such as $\overline{S0}$, $\overline{S1}$, $\overline{CMD}$, and $\overline{BURST}$ present. It indicates a condition when DMA slave or Bus Master transfers have been executed.

4.2.2 Arbitrate the Local CPU Bus

Bus cycles originating from the DMA slave, Channel bus master, or refresh requests require the system MPU to give up the local bus. This arbitration request function is performed by the CACP.

4.2.3 Regulate Arbitration Cycle Duration

- CPU-Programmable

When Bit 5 of the Arbitration Register (0090H) equals one, the default arbitration cycle is extended from a minimum of 300 ns to a maximum of 750 ns, depending on the CPU clock rate. Table 7 defines this relationship.

CPU CLOCK	AC REGISTER BIT 5 = 0	BIT 5 = 1
16 MHz	312.5 ns	750 ns
20 MHz	300 ns	750 ns
25 MHz	320 ns	720 ns

Table 7. Extending The Default Arbitration Cycle

- Arb = 0000 Special Case

If the Arbus goes to 0000B during an arbitration cycle, the arbitration can be shortened to a minimum of 100 ns.

- Dynamic Extension of Arbitration Time

Arbitration time can be extended by an NMI or Refresh cycle. The NMI sets Bit 6 of the Arbitration Register to one, which forces the ARB/$\overline{GNT}$ signal to ARB until the CPU clears the bit to zero.

4.2.4 Arbitration Monitor

Since the Channel arbitration mechanism is distributed between the system board and the Micro Channel-based peripherals, a central monitoring point is needed to allow for recovery from malfunctions. The CACP monitors the Channel bus, and when a bus master does not release the bus as requested by an asserted $\overline{PREEMPT}$ signal, it hands system control to the MPU, so that it can initiate error recovery.

When a bus time-out occurs, the CACP captures the arbitration level of the device and generates an NMI. The DMA controller, is also initialized to allow the MPU to attempt error recovery.

The time-out mechanism is based on the refresh timer which cycles approximately every fifteen microseconds. The time-out is armed when a refresh request is pending and when the arbiter is in any state except Refresh. If the request is not honored before the next refresh request, a bus time-out condition is said to exist.

The bus time-out and the resulting NMI are held asserted until cleared by a write from the CPU which sets Bit 6 of the Arbitration Register to zero.

4.2.5 Floppy Disk Controller DMA Interface

On behalf of the floppy disk controller, this function competes for ownership of the system bus by converting DMA requests such as DRQ and $\overline{DACK}$ into the appropriate signals for the CACP.

4.3 $\overline{PREEEMPT}$ GENERATOR

The FE6010 generates the $\overline{PREEMPT}$ signal in certain situations, which are described below.

4.3.1 Floppy Controller DMA Request

The CACP generates a $\overline{PREMPT}$ signal on behalf of the floppy controller when the floppy controller issues a FDDRQ, and Floppy DMA Controller Channel 2 is not masked. This signal is cleared when a DMA Master Clear command is received or when the bus has been won by Floppy Disk DMA Channel 2 after a bus arbitration cycle.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
RESERVED														VGA SUBSYSTEM	
—		—		—		—		—		—		—		ENA	DIS

Figure 20. PVGA Register Format

4.3.2 Refresh Request

A refresh request made when the ARB/GNT line is in the GNT state will cause a PREEMPT signal to be asserted.

4.3.3 Arbitration Register Bit 6 Set

A PREEMPT is asserted when the ARB/GNT line is in the GNT state and Arbitration Register Bit 6 is set with any ARB value but a system board value, that is, other than 0FH.

4.3.4 Interrupt Request

A PREEMPT signal is asserted when the ARB/GNT line is in the GNT state, the ARBUS value is other than a system board value (0FH), Arbitration Register Bit 4 is set and an interrupt request to the CPU is active.

5.0 SYSTEM FUNCTIONS

The addresses used by the system control functions are listed below.

1. The ESF Pointer Register (EPR), located at 0FFFFDH or FFFF, FFFDH, is used to decode the ESF Data Register (EDR).
2. Setup Mode Timing Strobe (CDSETEN)
3. The VGA Enable Register (03C3H)
4. Refresh Address Generator (11 bits)

The PVGA Enable Register (03C3H) format is defined in Figure 20. When Bit 1 is set to one, an access to an address space below 1 MByte asserts VGAEN, which indicates that the video subsytem is enabled.

6.0 HALF-SPEED INTERFACE

This interface runs the 80387 at half the speed of the 80386, permitting the designer to utilize a slower numeric processor interface to implement a more cost-effective version. It could also be used if the 80387 were unavailable for any reason. For example, when the 80386 is running at 25 MHz, it allows the 80387 to operate at 12.5 MHz. When used in half-speed mode, the clock input to the 80387 has the same frequency as the CLK signal on the FE6010. The reset signal for the 80387 (RES387) must be synchronized to the 80387 primary clock (CLK2387) with the proper setup and hold times so that CLK387 has the same phase relationship as the internal CLK of the 80387. The phase relationship and clock frequency are set up at power up, and once set, can not be changed.

Figure 21 shows a block diagram of the 80387 half-speed interface, and Figure 22 contains a timing diagram of this interface.

7.0 DIAGNOSTICS

This logic allows the state of the Micro Channel bus to be latched on a Channel Check condition and is useful to diagnose faults in the system. The error recovery interface is compatible with the Model 80-071.

On a Channel Reset, the latching of the channel state is enabled. At the leading edge of each CMD or MMCMD, the channel state is latched. When a Channel check takes place, the latching is disabled, and the last channel state is retained. The current channel state can be read by the system CPU at I/O Locations 00E2H - 00E6H. An I/O Read at 00E7H returns the state of local bus DC pin (Bit 0), and enables the latching again.

The diagnostic signals are described in Table 1. The six read-only diagnostic registers are described here:

- PA (24:31) - 00E2H
- PA (16:23) - 00E3H
- PA (8:15) - 00E4H
- ARB/GNT, MMIO, PA (2:7) - 00E5H
- BE (0:3), ARB (0:3) - 00E6H
- DC, RESERVED - 00E7H

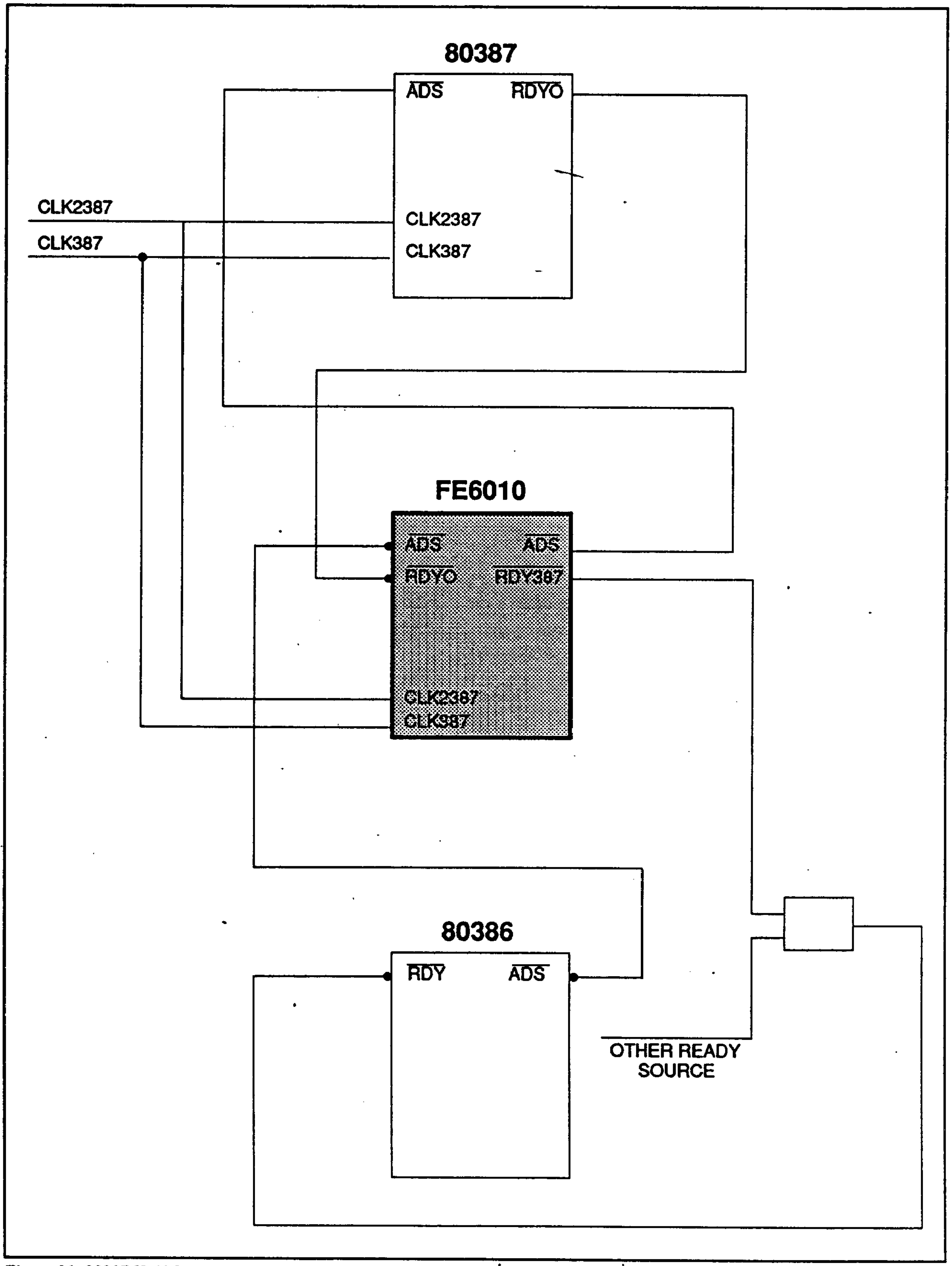


Figure 21. 80387 Half-Speed Interface

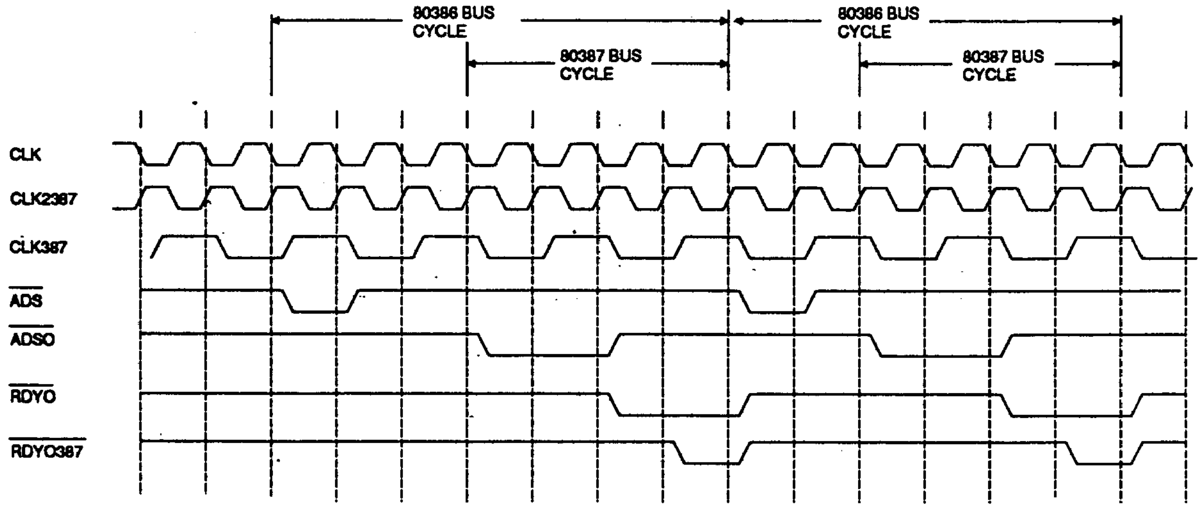


Figure 22. 80387 Half-Speed Interface Timing Diagram

7.1 DIAGNOSTIC REGISTER 1

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PA31	PA30	PA29	PA28	PA27	PA26	PA25	PA24

A Read at this location, 00E2H, gives the last latched state of the bus.

7.2 DIAGNOSTIC REGISTER 2

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PA23	PA22	PA21	PA20	PA19	PA18	PA17	PA16

A Read at this location, 00E3H, gives the last latched state of the bus.

7.3 DIAGNOSTIC REGISTER 3

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PA15	PA14	PA13	PA12	PA11	PA10	PA09	PA08

A Read at this location, 00E4H, gives the last latched state of the bus.

7.4 DIAGNOSTIC REGISTER 4

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PA15	PA14	PA13	PA12	PA11	PA10	PA09	PA08

A Read at this location, 00E5H, gives the last latched state of the bus.

7.5 DIAGNOSTIC REGISTER 5

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

ARB3	$\overline{ARB2}$	ARB1	ARB0	BE3	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$

A Read at this location 00E6H, gives the last latched state of the bus.

7.6 DIAGNOSTIC REGISTER 6

A Read at this location, 00E7H, gives the last latched state of the bus. It also enables the relatching of the state of

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	9	1	0	1	0	1	0

Reserved (bits 7–1)	DC

8.0 EXTENDED SETUP FACILITY (ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (EDRENA) output from the FE6010 to the FE6000. ESF is designed to extend the configuration architecture established with POS features. See Figures 23 and 24 for an overview of the ESF function. ESF supports

- Memory Map Control Registers
- Additional Physical Serial Port (SP2)
- Programmable Port Enables A and B
- EMS Control Registers
- External DRAM Control Configuration
- System Board LAN Configuration
- Customer-specified Enhancements that include
- System Identification
- System Version

8.1 ESF ACCESS

ESF is based on an "alternate I/O space" concept similar to the way in which the Extended CMOS RAM feature was implemented by IBM. ESF space, which consists of 128 locations expandable to 32K, is accessed through a single "real I/O space" window called the ESF Data Register (EDR). ESF space may be implemented as word-wide or byte-wide, at the discretion of the designer.

The write-only ESF Pointer Register (EPR), configurable by the software, points to the EDR. It is loaded by writing to memory location FFFFDH or FFFF, FFFDH, a PROM location. The power-on default location for the EDR is at I/O Address 0700H.

1. Set Port 0700H to 8DH to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4, Refresh Toggle, to synchronize it with the refresh circuitry.

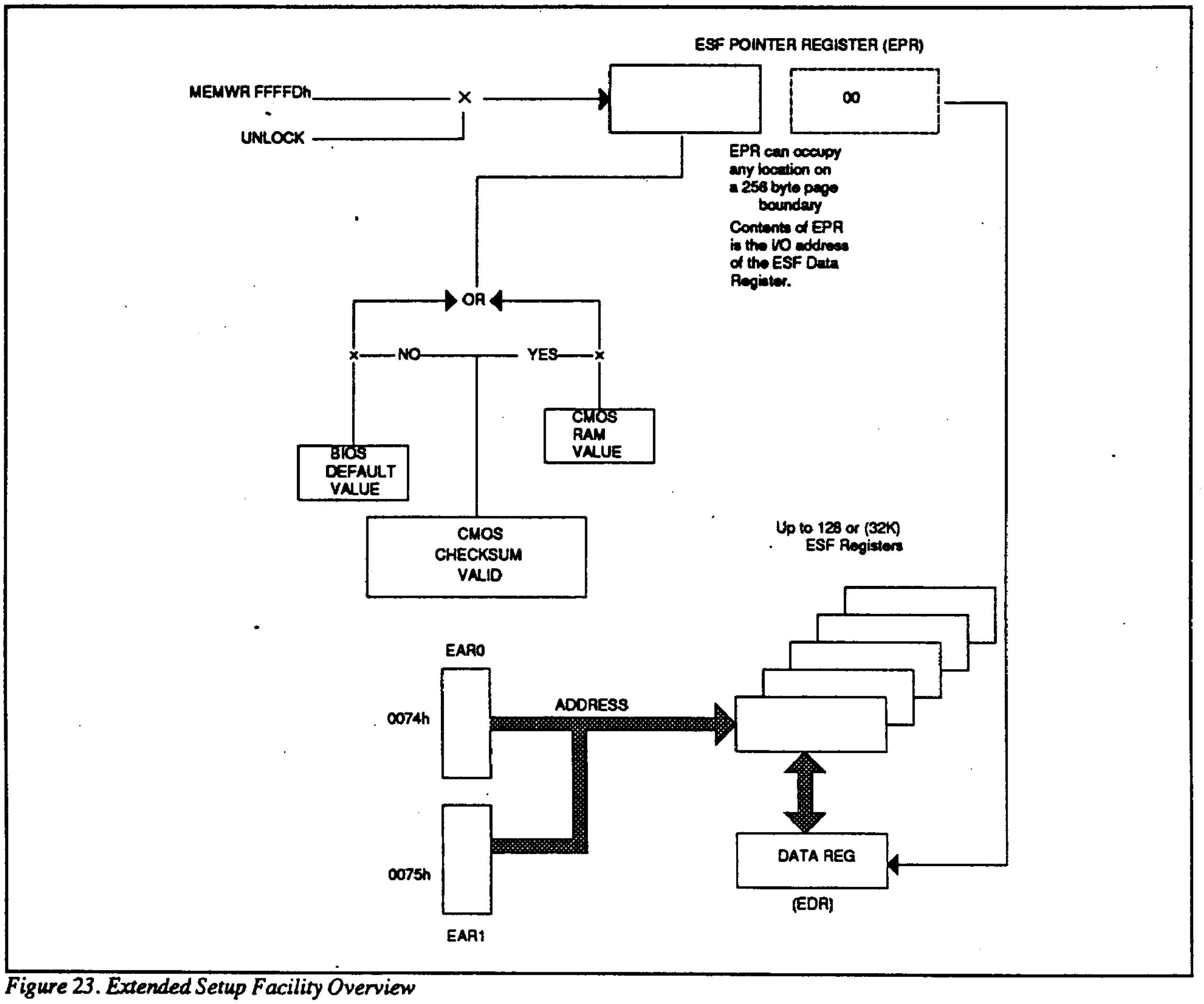


Figure 23. Extended Setup Facility Overview

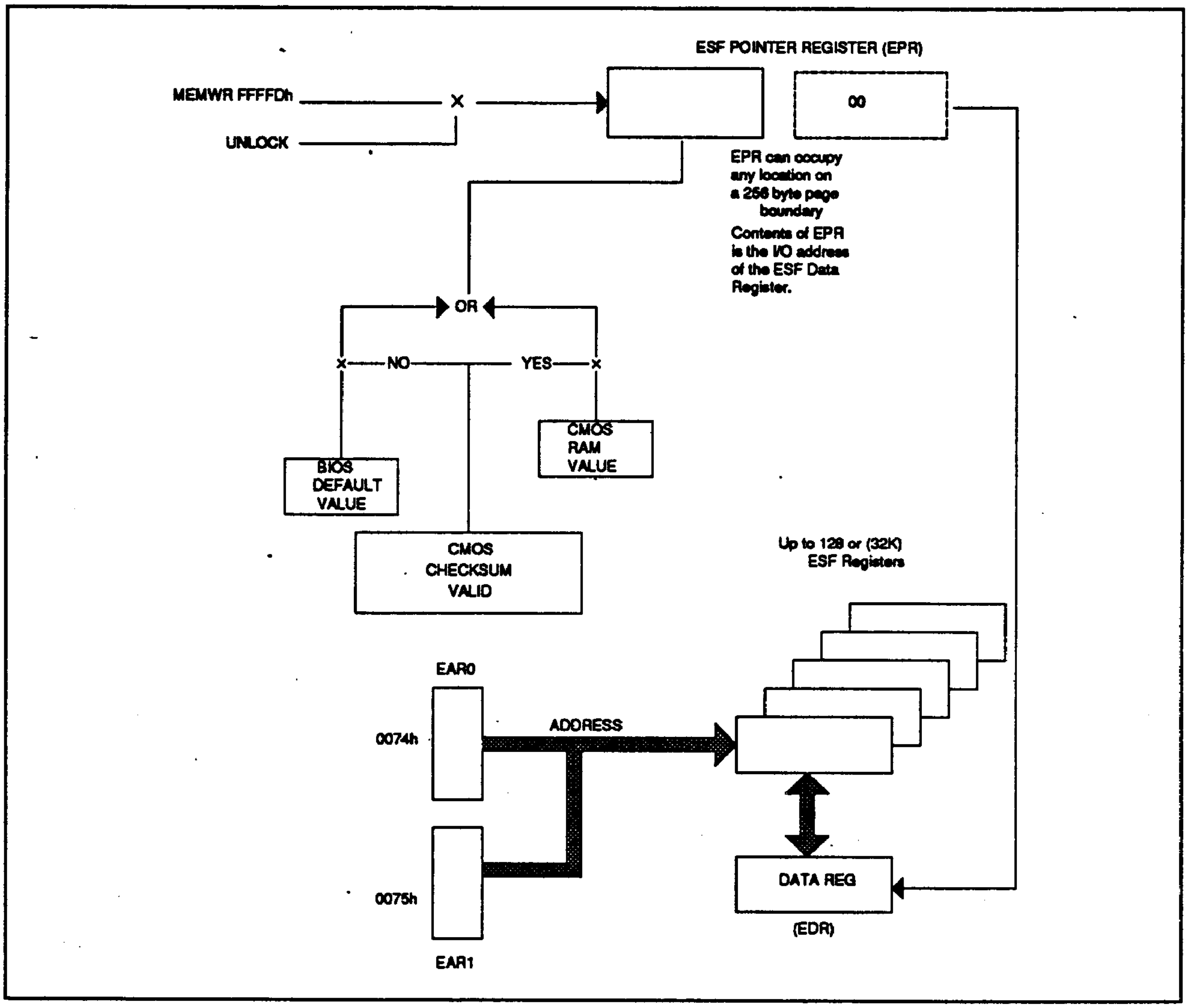


Figure 24. Extended Setup Facility Overview

3. To unlock the EPR, read EAR0 at 0074H, normally a write-only address.

4. Write the new value into the EPR at FFFFDH. This locks the EPR once again.

5. Enable NMI if required. Note that the EPR is locked when written, or on the next refresh cycle, whichever occurs first. The value in EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space:

1. Write 8DH to Port 0070H to disable NMI.

2. Write the address value to EAR0 at 0074H. If Expanded ESF is being used, also write the value to EAR1.

3. Issue an I/O Read or Write command to the EDR address.

The selected ESF register is determined by decoding the EAR0 address value.

8.2 ESF ADDRESS MAPS

The lower sixty-four bytes (EAR0 = 00H - 3FH) are reserved for Western Digital functions and features. The upper sixty-four bytes (40H -7FH) can be used by the customer. See Table 8 for details. All functions using ESF must include Bit 7 of EAR0 in the decode. This bit must be zero when addressing only 128 ESF registers. To expand the ESF to 32,768 location, set EAR0 Bit 7 to one and write the second ESF address byte to EAR1.

ESF ADDRESS	FUNCTION	R/W	DEVICE
0 - 001FH	Reserved	-	-
20H	Peripheral Configuration	R/W	FE6000
21, 24H	Port A,B Control	R/W	FE6000
2, 25H	Port A,B Address (LSB)	R/W	FE6000
30 - 3FH	Reserved	-	-
40 - 7FH	Customer-specified	-	-
0180H	Memory Configuration	R/W	FE6030
0181H	Memory Size Register	R/W	FE6030
0182H	Bank Enable Register	R/W	FE6030
0183H	Split Address Extension	R/W	FE6030
0184H	Memory Window Bank 0	R/W	FE6030
0185H	Memory Window Bank 1	R/W	FE6030
0186H	Memory Window Bank 2	R/W	FE6030
0187H	Memory Window Bank 3	R/W	FE6030
0188H	CAS Pulse Width	R/W	FE6030
0189H	RAS PreCharge Delay	R/W	FE6030
018AH	RAS Pulse Width	R/W	FE6030
018BH	RAS Access Time	R/W	FE6030
018CH	Enhanced Addressing	R/W	FE6010
018DH	Reserved	-	-

Table 8. ESF Registers for an FE6500 System

9.0 THE FE6010 IN 80386 AND 80386SX ENVIRONMENTS

As described before, the FE6010 can be configured to be used in either an 80386-based system or an 80386SX-based system. The differences in usage in these two environments is summarized in this section.
Certain signals, listed below, have been provided with weak internal pull-ups to ease system design:

- PD (31:16) 20K internal pull-up
- DACK 20K internal pull-up

When using an 80386-based system, the following points should be noted:

- PD (31:0) connect to the 80386 data lines (31:0)
- PA (31:2) connect to the 80386 address lines (31:2)
- BE (1:0) connect to the 80386SX byte enables BEH and BEL respectively. BE2 connects to 80386SX Address Line 1. BE3 should be left open on the FE6010.
- The FE6010 BS16 input should be tied to GND.

10.0 TECHNICAL SPECIFICATIONS

10.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for the FE6010 device are tabulated below. Permanent damage to the device could result from exposing it to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD} - V_{SS}	0	7	V
Input Voltage	V_{IABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Bias on Output Pin	V_{OABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	TS	-40	125	°C

10.2 NORMAL OPERATING CONDITIONS

Exposing the FE6010 to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.5	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD} + 0.3	V
Power Dissipation	PW	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

10.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input Capacitance @ fc = 1 MHz	CI	–	5	pF
*I/O Capacitance	C_{IO}	–	10	pF
Logic High Input Voltage	V_{IH}	2.0	–	V
Logic Low Input Voltage	V_{IL}	–	0.8	V
*Input Leakage	I_{IL}	–	±10	µA
*Tri-state Output Leakage	I_{OL}	–	±30	µA
*I/O Pin Leakage	I_{IOL}	–	±40	µA
OUTPUTS $\overline{BE(3:0)}$, $\overline{MIO}$, $\overline{DC}$, $\overline{WR}$, $\overline{ADS}$				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	24	µA
OUTPUTS TC, ARB (3:0), PREEMPT, ARB/GNT, REFRESH				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	24	µA
ALL OTHER OUTPUTS				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	4	µA

NOTE Underlined signals are open collector outputs.

NOTE Signals PA (31:24), BE3, PD(31:16), and DACK have internal pullups of 20K

NOTE When TEST = 0, all outputs and bi-directional signal lines are tristated.

*Pins ARB [3:0] and PREEMPT are open collector outputs. Source current value does not apply. External pullups are required on these outputs.

10.4 A.C TEST LOADS

OUTPUTS	SYMBOL	MIN	MAX	UNITS
BE(3:0), WR, MIO, DC, ADS*	CL	-	50	pF
PA(31:2), PD(31:0)*	CL	-	120	pF
ARB(3:0), PREEMPT	CL	-	200	pF
TC, ARB/GNT, REFRESH	CL	-	240	pF
ALL OTHER OUTPUTS	CL	-	50	pF

*These signals are tested at 50 pF for the 25 MHz frequency.

NOTE

1.PA(31:2), BE(3:0), PD(31:0), ADS, MIO, DC, WR, ARB(3:0), PREEMPT, and NMI are bi-directional signals.
2.UCHMSTR, A20GTX, and DACK are inputs only at power-up; they are outputs the rest of the time.
3.TC is a tristate output signal.
4.ARB(3:0), PREEMPT, and NMI are open collector signals and require external pullups.

11.0 TIMING

The following inputs are asynchronous to CLK2: A20GATE, PREEMPT, BURST, EOT, FDDRQ, REFREQ, CHCK, CHRESET, UCHCMD, NMI, INTR, SHUTDOWN, PWRGOOD, and ARB(3:0).

The following outputs are asynchronous to CLK2: ARB/GNT, ARB(3:0), DACK, REFRESH, UCHMSTR, A20GTX, RES386, RES387, RESET, and ENPCHK.

The timings in the following table are in nanoseconds.

PARAMETER	DESCRIPTION	MIN	MAX	NOTE
T1A	PREEMPT on to EOT	0	7.8 µs	–
T2A	ARB/GNT high from EOT	30	–	1
T3A	PREEMPT off from ARB/GNT	0	50	low
T4A	on from ARB/GNT low	–	50	–
T5A	ARB/GNT high	300	–	–
T6A	Driver turn-on delay from ARB/GNT high	0	50	–
T7A	Driver turn-off delay from ARB/GNT high	0	50	–
T8A	Driver turn-on delay from higher priority line	0	50	–
T9A	ARB [3:0] stable before ARB/GNT low	10	–	–
T10A	Tristate drivers from ARB/GNT high	–	50	–

1 EOT signifies the End of Transfer on the Channel with CHS [1:0], BURST, and CMD off.
2,3 To be clarified

Table 9. Arbitration Cycles (In ns)

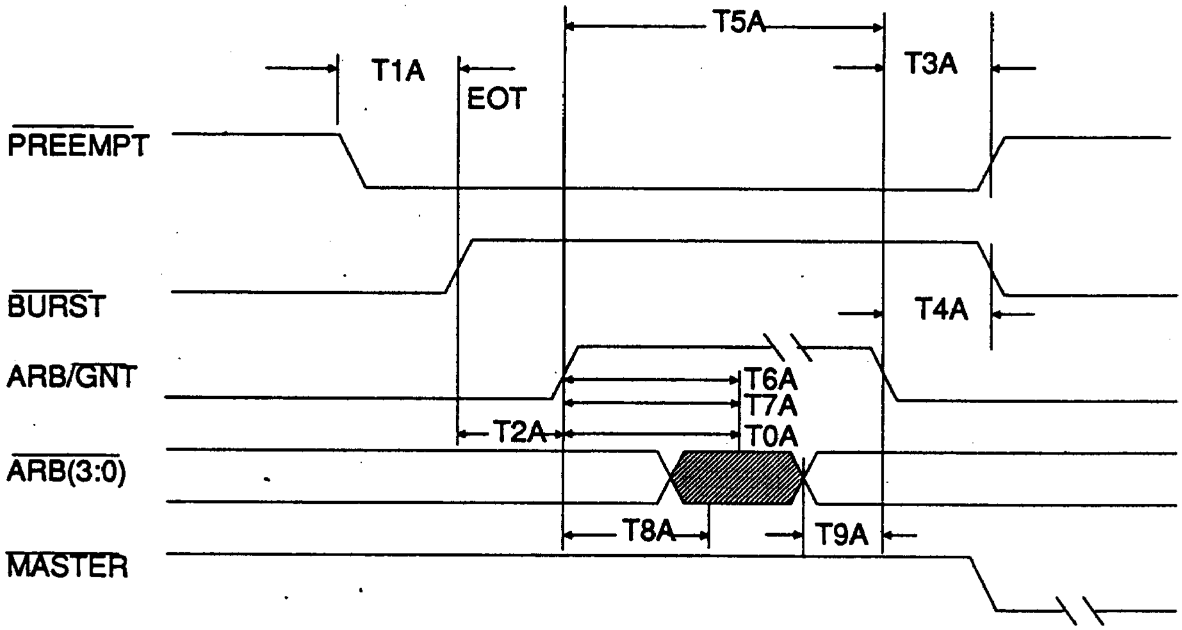


Figure 25. Arbitration Timing

PARAM	DESCRIPTION	16 MHZ MIN	16 MHZ MAX	20 MHZ MIN	20 MHZ MAX	25 MHZ MIN	25 MHZ MAX
T1B	FDDRQ on to $\overline{\text{PREEMPT}}$ on	25	–	20	–	15.6	–
T2B	ARB/$\overline{\text{GNT}}$ high to $\overline{\text{DACK}}$ off	0	–	0	–	0	–
T3B	ARB/$\overline{\text{GNT}}$ high to HOLD on	0	–	0	–	0	–
T4B	ARB/$\overline{\text{GNT}}$ high to HOLD off	0	–	0	–	0	–
T5B	HLDA to ARB/$\overline{\text{GNT}}$ low	25	–	20	–	15.6	–

Table 10. Floppy Request Cycles (In ns)

Figure 26 shows an arbitration timing diagram, and Table 10 tabulates the arbitration cycles in nanoseconds.

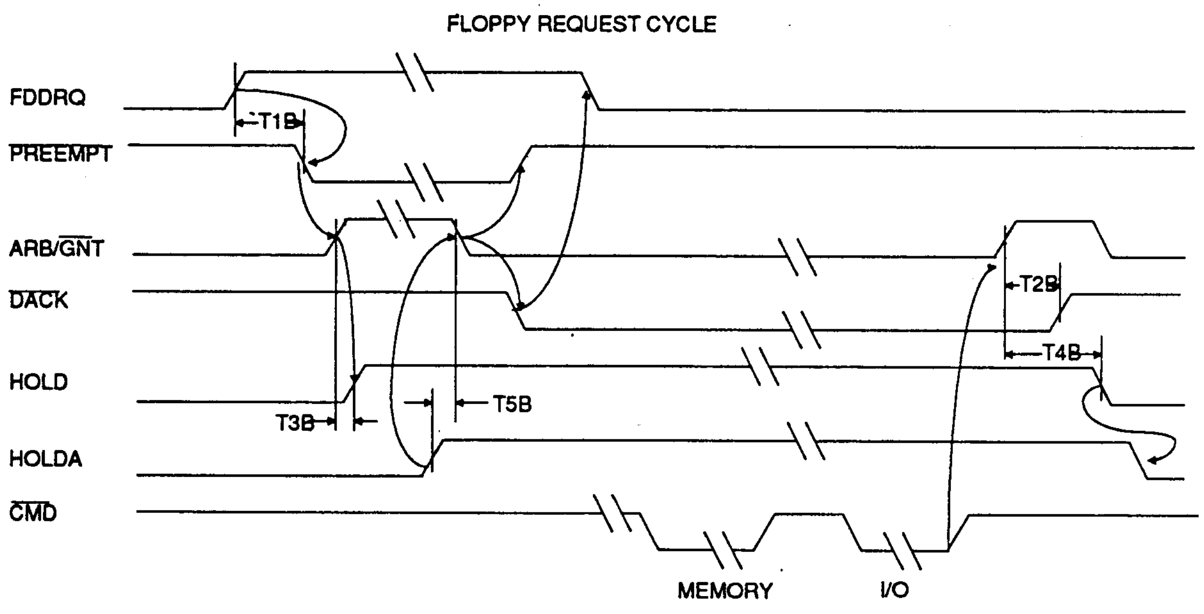


Figure 26. Floppy Request Cycle

PARAM	DESCRIPTION	16 MHz MIN	16 MHz MAX	20 MHz MIN	20 MHz MAX	25 MHZ MIN	25 MHZ MAX	NOTES
	Operating Frequency	4	16	4	20	4	25	MHz
	CLOCKS							
T1C	CLK2 Period	31.25	125	25	125	20	125	@ 2V
T2AC	CLK2 High Time	5	–	5	–	4	–	@ (V_{DD}-0.8V)
T2BC	CLK2 High Time	9	–	8	–	7	–	@ 2V
T3AC	CLK2 Low Time	7	–	6	–	4	–	@0.8V
T3BC	CLK2 Low Time	9	–	8	–	7	–	–
T4C	CLK Period	62.5	250	50	250	40	250	–
T5C	CLK High Time	20	–	14	–	17	–	–
T6C	CLK Low Time	15	–	12	–	17	–	–
T7C	CLK2387 Period	31.25	250	25	250	20	125	–
T8C	CLK2387 High Time	–	–	–	–	7	–	–
T9C	CLK2387 Low Time	–	–	–	–	7	–	–
T10C	CLK387 Period	62.5	500	50	500	40	500	–
T11C	CLK387 High Time	–	–	–	–	17	–	–
T12C	CLK387 Low Time	–	–	–	–	17	–	–

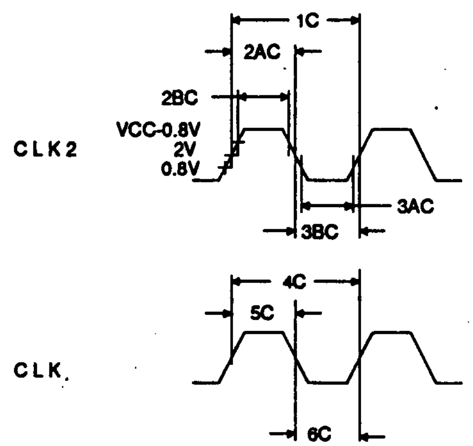


Figure 27. Input Clock Specifications

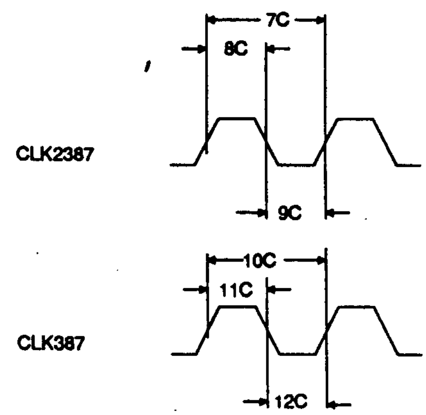


Figure 28. Input Clock Specifications II

DMA OPERATION								
PARAM	DESCRIPTION	16 MHz MIN	16 MHz MAX	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	NOTES
T1D	PA(31:2), $\overline{BE}$(3:0) Valid	2	38	2	32	2	24	1
T2D	Disable/Enable MIO, DC, WR, $\overline{ADS}$	2	38	2	32	2	30	1
T3D	Valid	4	35	4	30	2	24	2
T4D	Disable/Enable FE6010 REGISTER READ	4	35	4	30	4	30	2
T5D	PD(31:0) Valid	2	50	2	40	2	31	1
T6D	PD(31:0) Disable DMA WRITE CYCLE	2	35	2	27	2	22	1
T7D	PD(31:0) Valid	2	50	2	40	2	31	1
T8D	PD(31:0) Disable	2	35	2	27	2	22	1
T9D	HOLD Valid	4	35	4	30	5	24	–
T10D	HOLD Disable	4	35	4	30	5	24	–
T11D	$\overline{TC}$ Valid	4	25	4	25	4	25	–
T12D	$\overline{TC}$ Disable	4	25	4	25	4	25	–
T13D	$\overline{RDY}$ Setup Time	20	–	11	–	9	–	–
T14D	$\overline{RDY}$ Hold Time	3	–	3	–	3	–	–
T15D	HLDA Setup Time	25	–	18	–	16	–	–
T16D	HLDA Hold Time	3	–	3	–	3	–	–
T17D	Setup Time	22	–	20	–	16	–	–
T18D	Hold Time MIO, DC, WR, $\overline{ADS}$	2	–	2	–	2	–	–
T19D	Setup Time	22	–	20	–	16	–	–
T20D	Hold Time FE6010 REGISTER WRITE	2	–	2	–	2	–	–
T21D	PD(31:0) Setup	30	–	25	–	20	–	–
T22D	PD(31:0) Hold DMA READ CYCLE	15	–	15	–	15	–	–
T23D	PD(31:0) Setup	10	–	10	–	7	–	–
T24D	PD(31:0) Hold $\overline{NA}$, $\overline{BS16}$	5	–	5	–	5	–	–
T25D	Setup Time	10	–	8	–	7	–	–
T26D	Hold Time $\overline{MI}$, INTR*	20	–	20	–	3	–	–
T27D	Setup Time	15	–	15	–	15	–	–
T28D	Hold Time	15	–	15	–	5	–	–

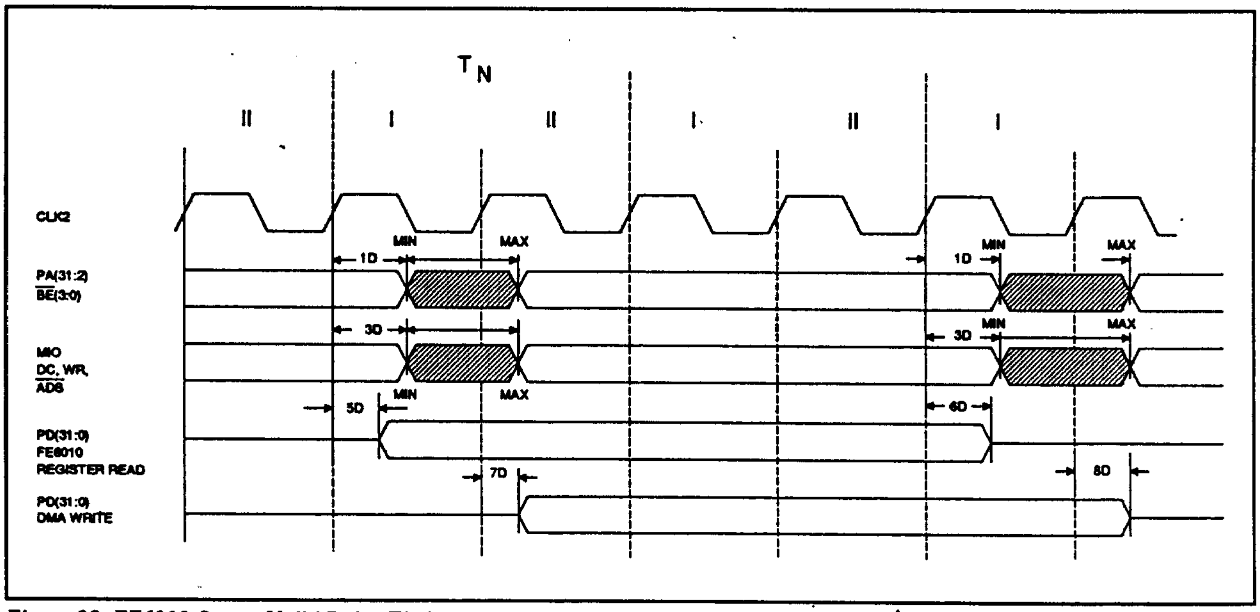


Figure 29. FE6010 Output Valid Delay Timing

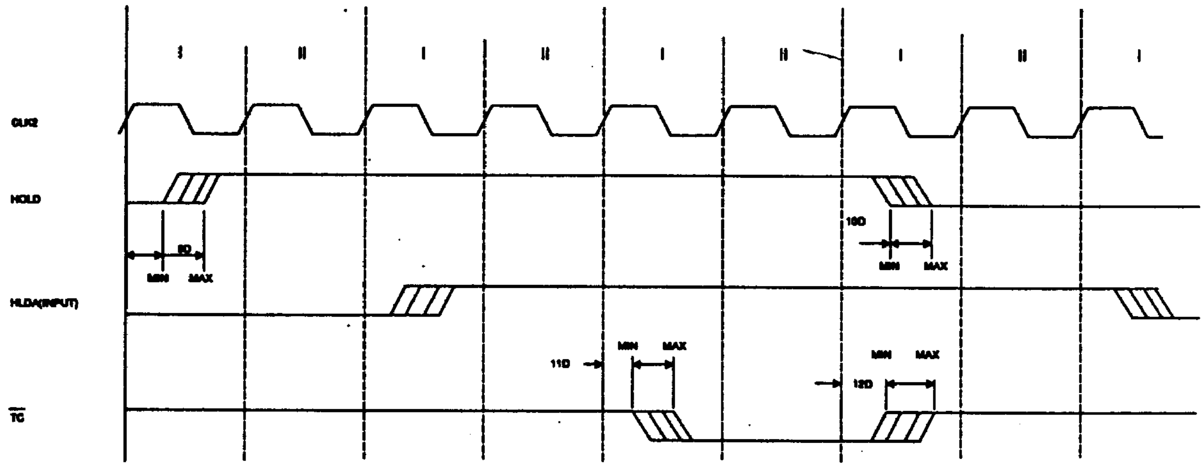


Figure 30. FE6010 Output Valid Delay Timing II

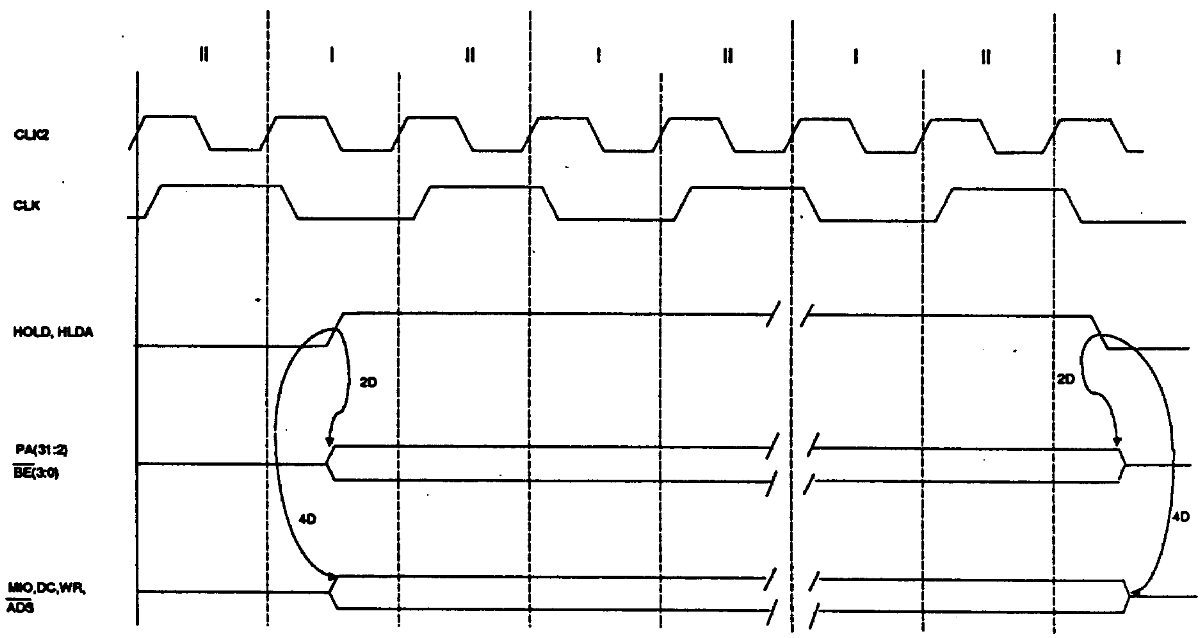


Figure 31. Bus Tristate Timings

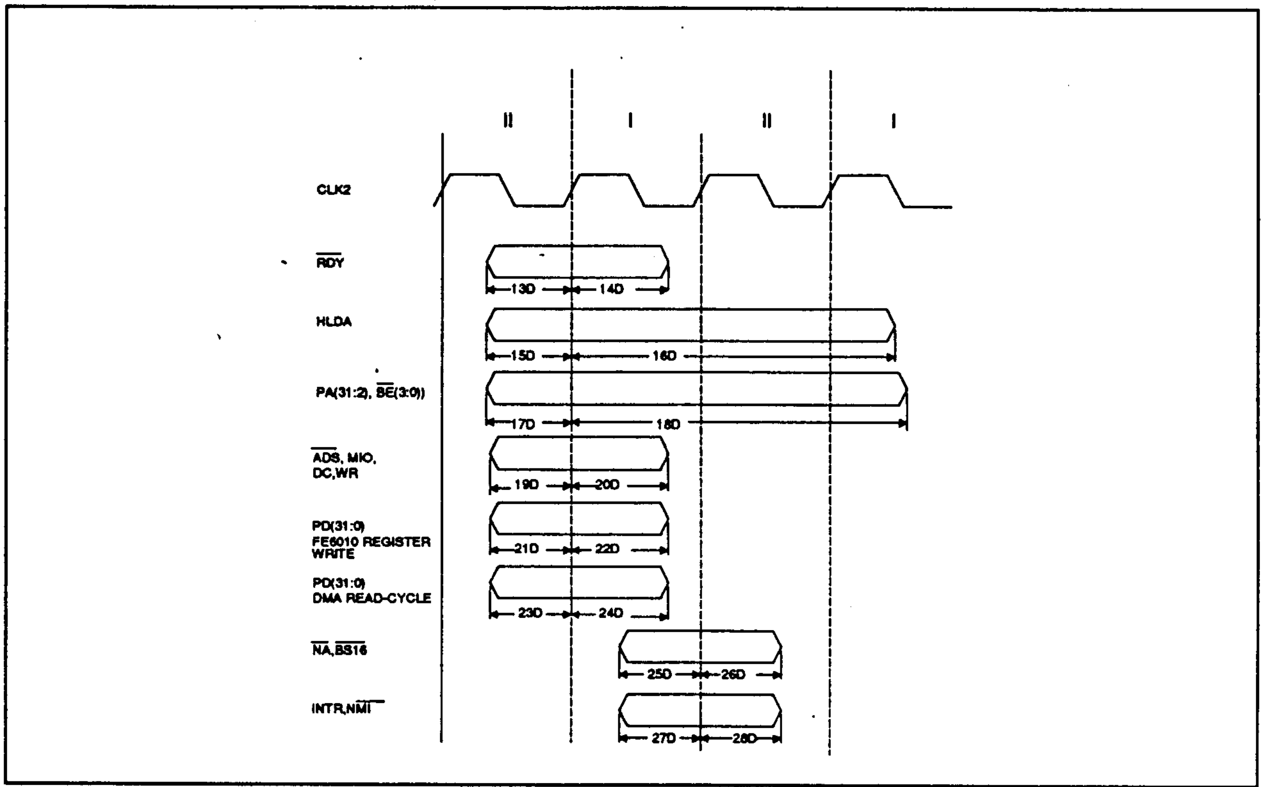


Figure 32. Input Setup and Hold Timings

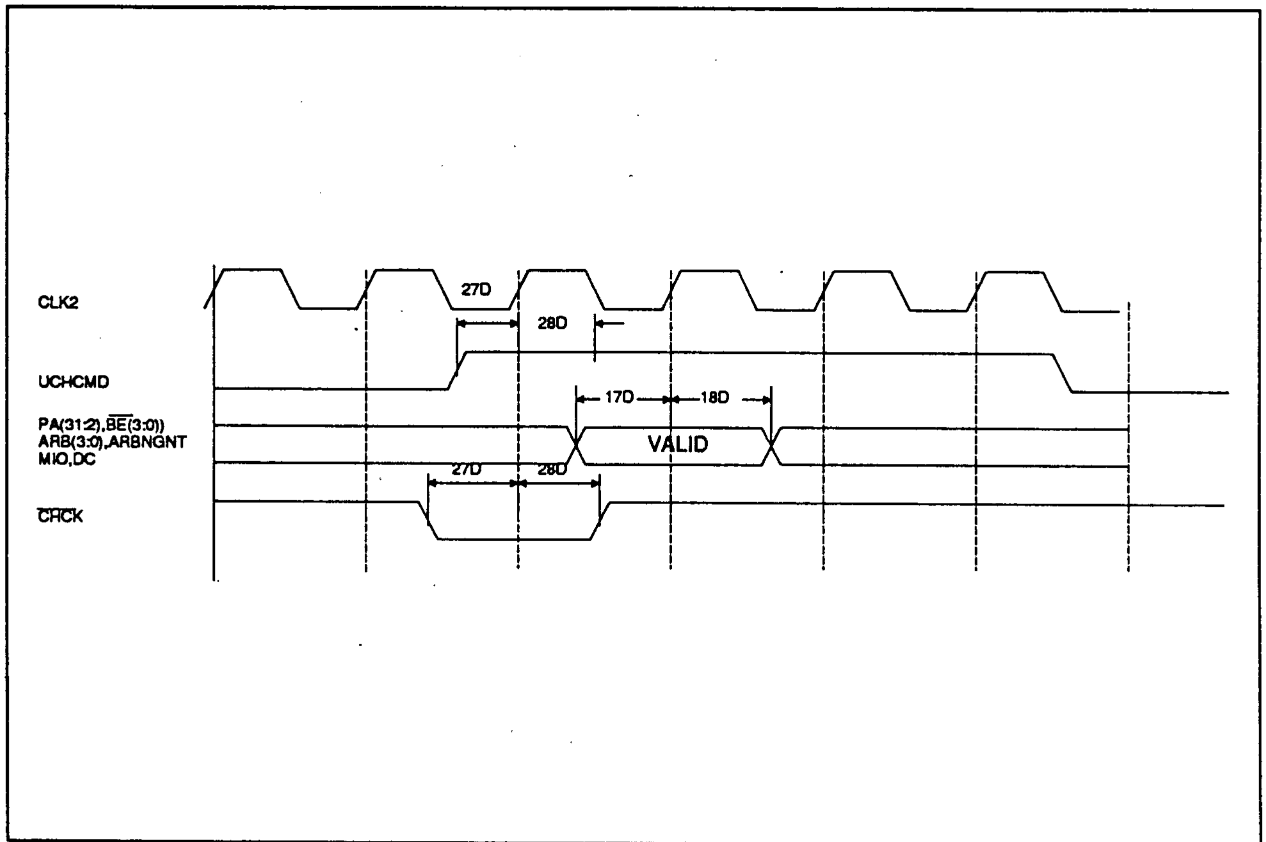


Figure 33. Diagnostic Interface Timing

80387 HALF-SPEED INTERFACE								
T1H	ADS0 Valid from CLK2387 RDY0	6	34	6	28	3	24	–
T2H	Setup Time to CLK2 rising edge	20	–	11	–	9	–	–
T3H	Hold Time from CLK2 rising edge NRDY0387	4	–	4	–	3	–	–
T4H	Valid from CLK2	2	25	2	25	2	19	–
DEVICE ENABLE TIMINGS								
T1E	CDSETEN, VGAEN, EDRENA	Valid from address		–	20	–	20	–

1CL = 120 pF for 16 MHz and 20 MHz; CL = 50 pF for 25 MHz.
2CL = 75 pF for 16 MHz and 20 MHz; CL = 50 pF for 25 MHz.
*These inputs can be asynchronous to CLK2.

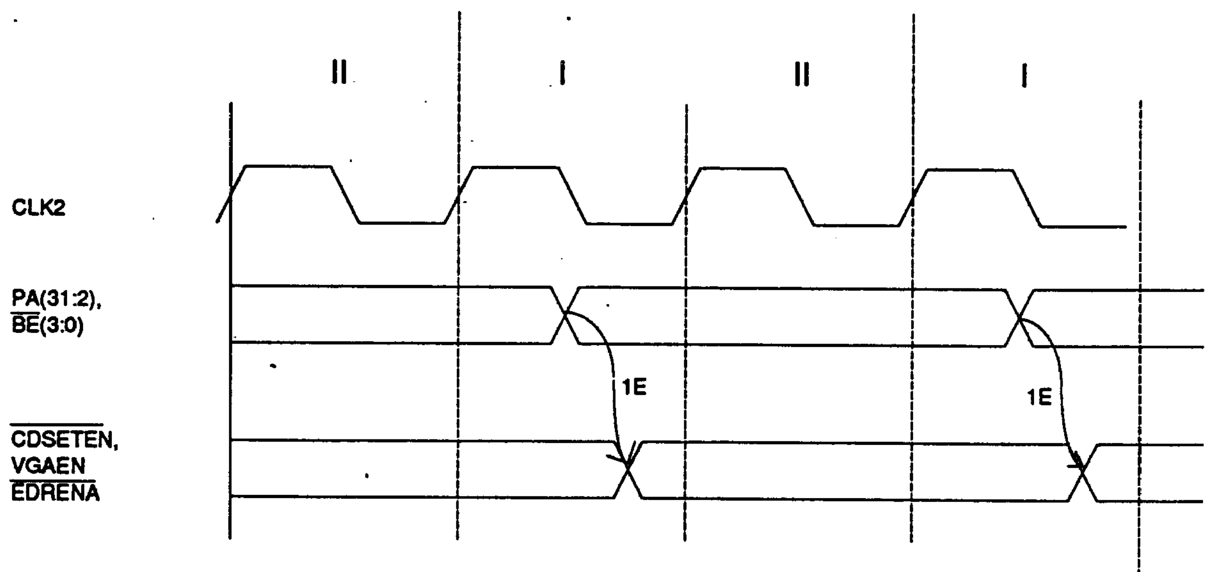


Figure 34. Device Enable Timings

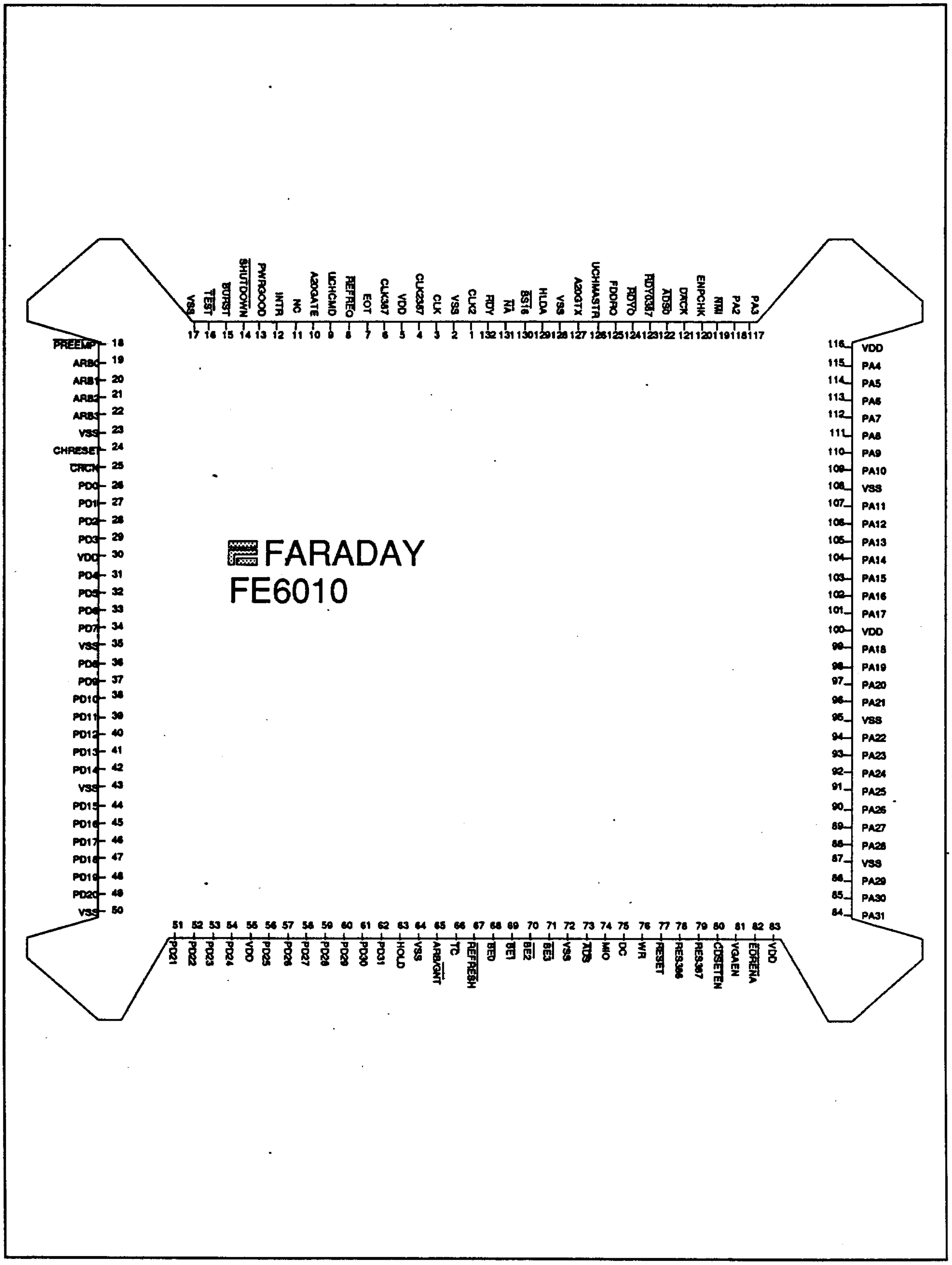


Figure 35. Pin Layout Diagram- Top View

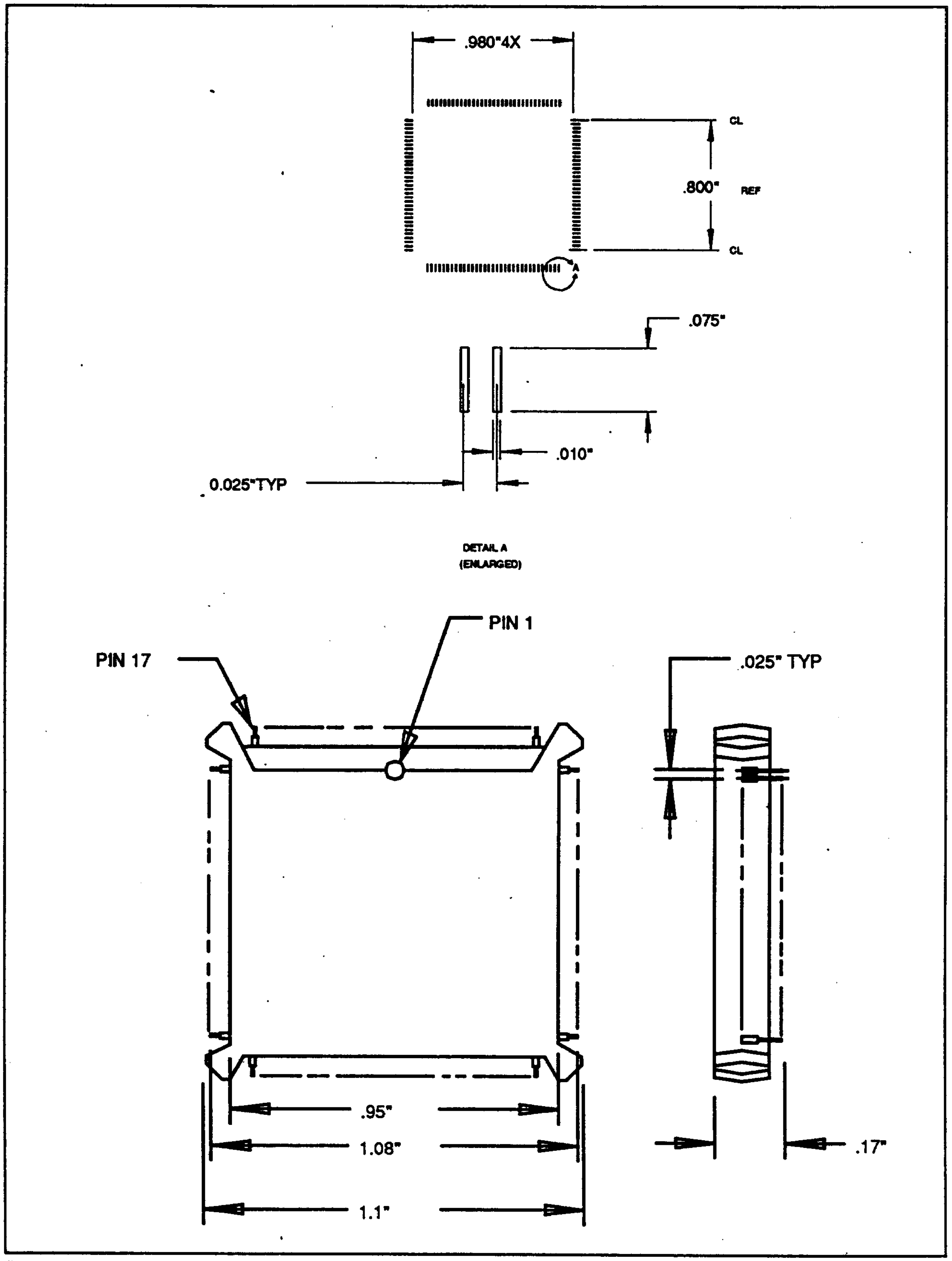


Figure 36. 132-Pin JEDEC Flat Pack Packaging Diagram

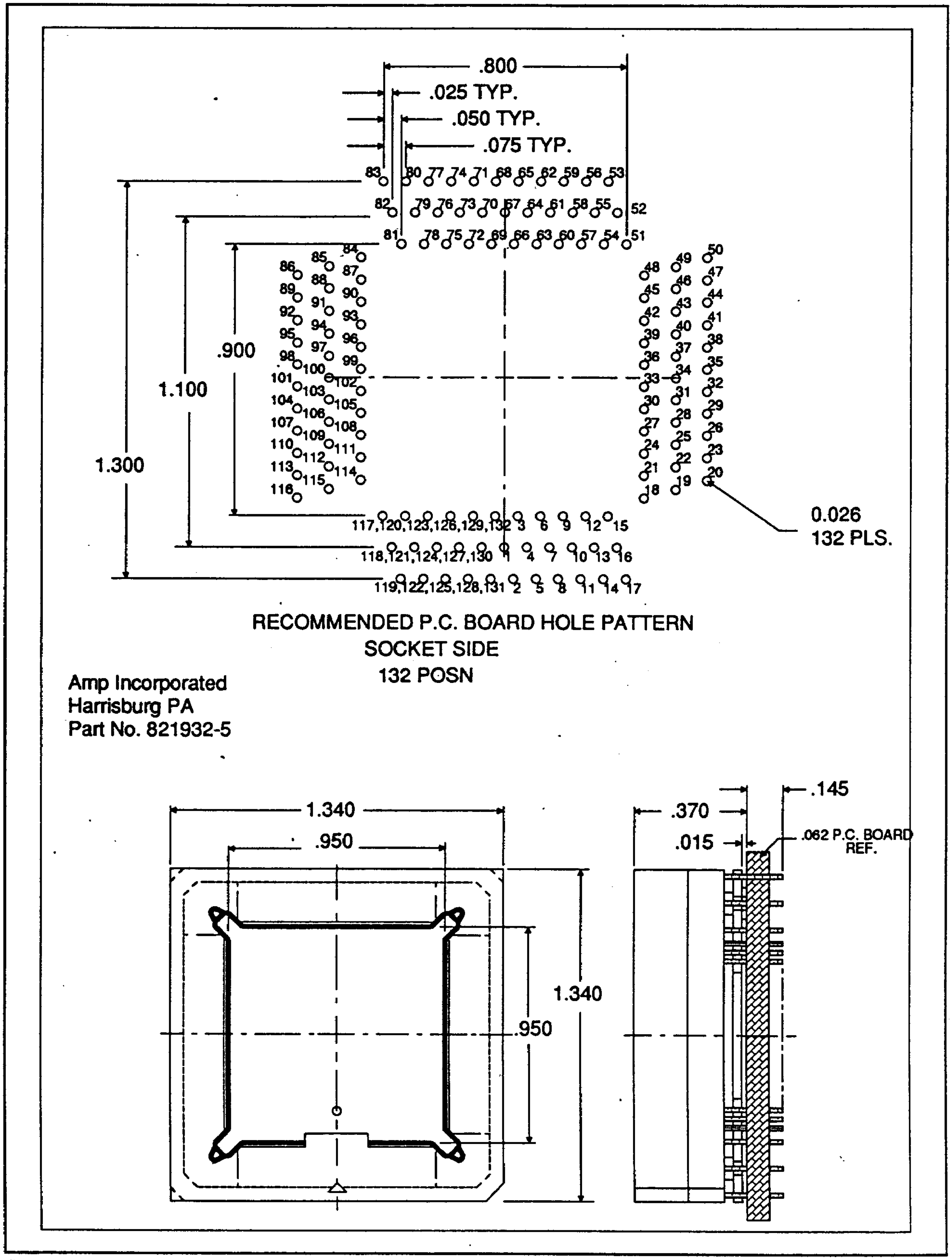


Figure 37. Socket Diagram

Advance Information