CPU Core Logic for Model 50/60 Compatibles

T-49-17-01

FE5400

Features

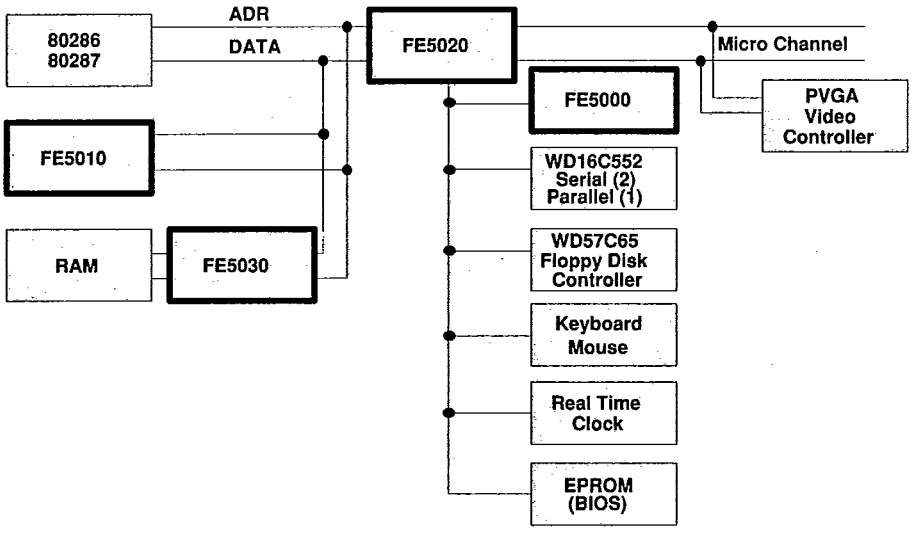
- Four-chip core logic implementation for 80286-based IBM® PS/2™ Model 50 or 60 compatible computers
- Operates at high performance 20 MHz CPU clock rate
- 100% hardware (register level) and software compatible with PS/2 Models 50 and 60
- Model 50/60 Peripheral and Control Logic:
  - Two 8259A compatible interrupt controllers
  - 8254 compatible timer
  - Watchdog timer
  - Programmable option select logic
  - NMI, coprocessor interface, audio logic
  - System board I/O decoder
  - Extended Setup Facility™ (ESF™)
- Model 50/60 DMA and Micro Channel™ Control:
  - Two 8237 compatible DMA controllers with extensions
  - Central arbitration control point logic
  - Micro Channel bus controls
  - Clock generation
  - Basic DRAM control
- Address and data buffers interface directly to Micro Channel with 24 mA drivers
- Integrated Memory Controller:
  - Version 4.0 EMS (LIM) support
  - Page, static column and interleave modes
  - 256K, 1M and 4M DRAM support
- 132-pin JEDEC Standard low power CMOS and BiCMOS packages

Description

The FE5400 chip set provides all necessary core logic to build a totally integrated IBM Personal System/2™ Model 50 or 60 compatible motherboard using the 16-bit Intel® 80286 Central Processing Unit (CPU).

The FE5400 chip set is 100% hardware (register level) and software compatible with the PS/2™ Models 50 and 60. It includes the components needed to build a PS/2 compatible motherboard including IBM's Micro Channel Architecture™.

The FE5400 chip set consists of four devices: FE5000, FE5010, FE5020 and FE5030. They operate at CPU clock rates of up to 20 MHz or twice as fast as the PS/2 Model 50/60's clock rate resulting in significantly higher performance and a natural migra-



Model 50/60 Compatible System

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CPU Core Logic for Model 50/60 Compatibles

tion/differentiation path for PS/2 compatible manufacturers.

This highly integrated chip set significantly facilitates design and implementation of Model 50 and 60 compatible system boards that are smaller, less noisy, consume less power and have higher performance.

Components

The FE5000 Peripheral and Control and the FE5010 DMA and Micro Channel Control logic devices contain the equivalent functions of two Intel 8259 interrupt controllers (16 channels), a 3-channel 8254 timer and two 8237 DMA controllers with IBM compatible extensions. They hold the central arbitration control point logic.

In addition, the FE5000 and FE5010 include logic for the watchdog timer, programmable option select, coprocessor interface, system board I/O decode, buffer controls, clock generation and Micro Channel bus controls.

A basic memory controller is included and an Extended Setup Facility is provided to facilitate special configurations. The FE5000 and FE5010 are manufactured using CMOS technology.

The FE5020 Address and Data Buffer logic device contains the address and data buffers that are used to directly interface the device to the Micro Channel bus without external drivers. The buffers have a 24mA drive capability.

A local bus buffer is provided that makes it easy to integrate other peripheral controllers such as a floppy controller, serial ports, hard disk and display controllers.

The FE5030 Memory Controller contains the logic necessary to manage the system's dynamic memory (DRAM). It includes a RAS/CAS DRAM address multiplexer and a data buffer with parity checking that interfaces CPU and DRAM. RAS/CAS control circuitry is also included.

Memory configuration is programmable offering the designer maximum flexibility. The chip includes extended memory support (the Lotus, Intel and Microsoft implementation of EMS). It supports page, static column and interleave modes. It also allows usage of 256K, 1M and 4M DRAM devices.

Both FE5020 and FE5030 are manufactured using BiCMOS technology for its high speed and high drive capability.

Micro Channel and DMA

The FE5400 chip set directly interfaces to the bus and meets all Micro Channel bus timing specifications.

Micro Channel bus timing is, however, decoupled and independent of the CPU clock rate. This allows the processor to run at its maximum rate and still maintain compatibility on the bus.

Arbitration logic controls and monitors the Micro Channel and local bus arbitration functions.

A Cost Effective Design

The FE5400 chip set is cost effective because it replaces three gate arrays plus approximately 100 additional devices. The direct result is a smaller motherboard with lower power consumption.

Packaging

The FE5400 chip set devices are manufactured in surface mountable 132-pin JEDEC Standard packages.

This type of packaging allows for a higher level of logic integration resulting in an extremely reliable device that takes up less space.

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