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T-52-33-19

Advance Information

FE5010

DMA and Channel Control Logic

- 100% Hardware (Register Level) and Software Compatible to the IBM* Personal System/2* Models 50 and 60
- 10, 12.5, 16, and 20 MHz Clock Speeds to Maximize Flexibility and Performance
- Meets Micro Channel* Bus Timings
- Arbitration Control Logic
- Equivalent Functionality of two 8237 DMA Controllers with Extended Mode Support
- Provides System Board Bus, Clock/Reset, and Wait/Ready Control
- Faraday® Extended Setup Facility™ (ESF™)
- Low Power 1.25 Micron CMOS Technology
- 132 Lead JEDEC Plastic Quad Flat Pack

As part of the Faraday FE5400 Chip Set, the FE5010 DMA and Channel Control Logic integrated circuit significantly facilitates the design and implementation of IBM PS/2* Model 50 and 60 compatible system boards. By combining functionality normally implemented in 2 gate arrays and 33 discrete components, the FE5010 decreases design complexity, saves space, reduces system cost, and increases system reliability.

The Extended Setup Facility (ESF) is a fully compatible enhancement that allows designers to provide additional functionality (e.g., Winchester Controller, LAN Adapter, Additional Serial Port) on the system board. This facility can help reduce costs and provide system level product differentiation. Figure 1 shows a typical system diagram using the FE5400 Chip Set.

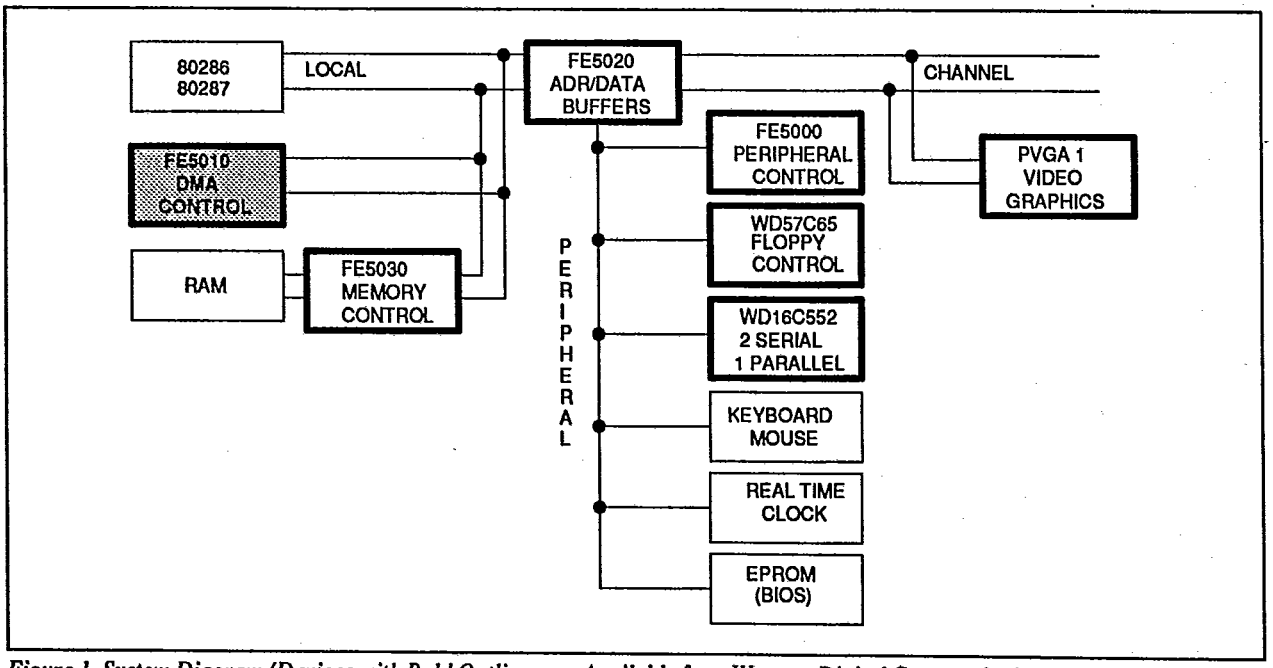

Figure 1. System Diagram (Devices with Bold Outlines are Available from Western Digital Corporation)

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Release 1.0

January 31, 1988

Additional References

IBM PS/2 Model 50/60 Technical Reference Manual
Intel Microprocessor and Peripheral Handbook*

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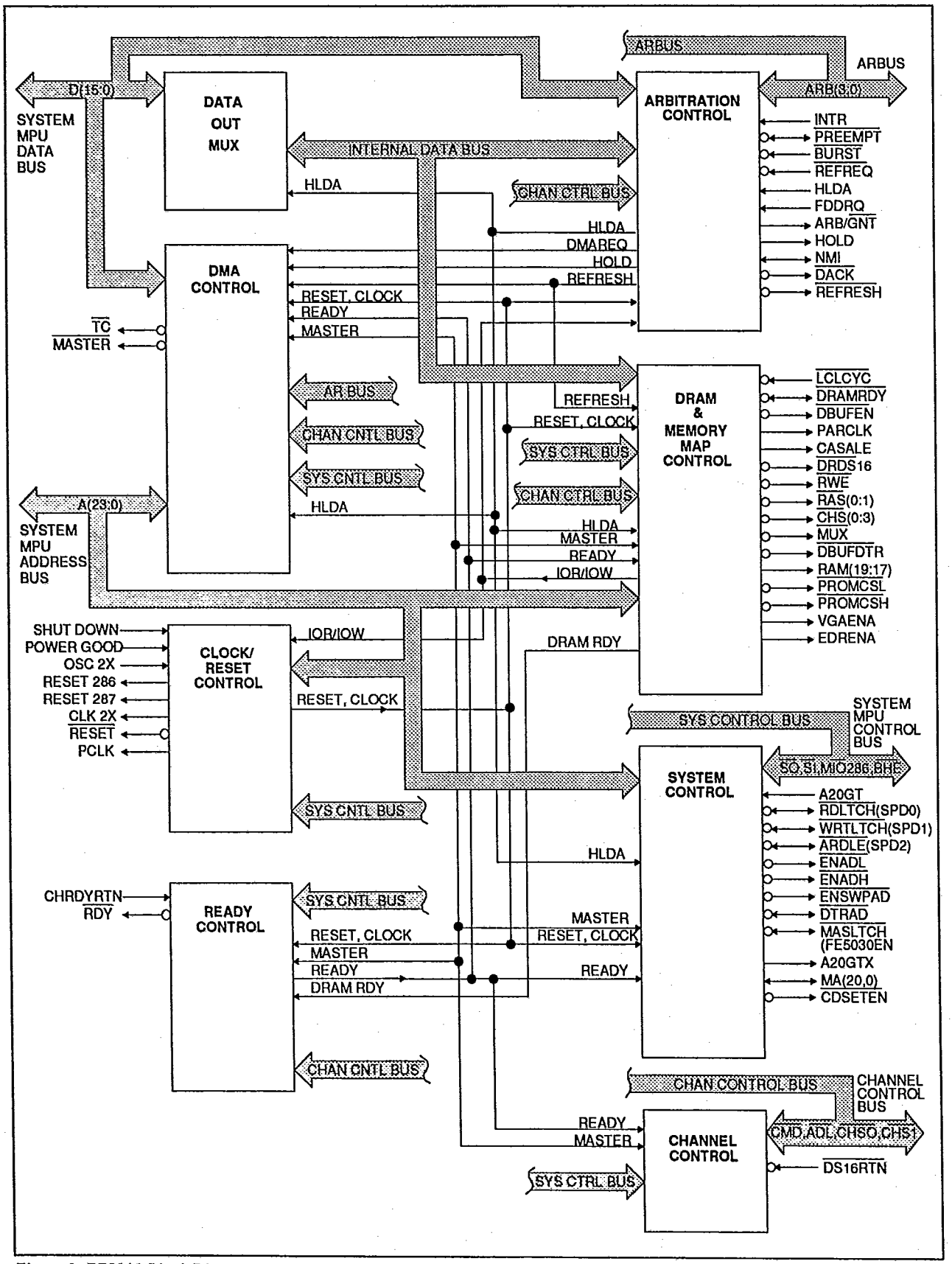


Figure 2. FE5010 Block Diagram

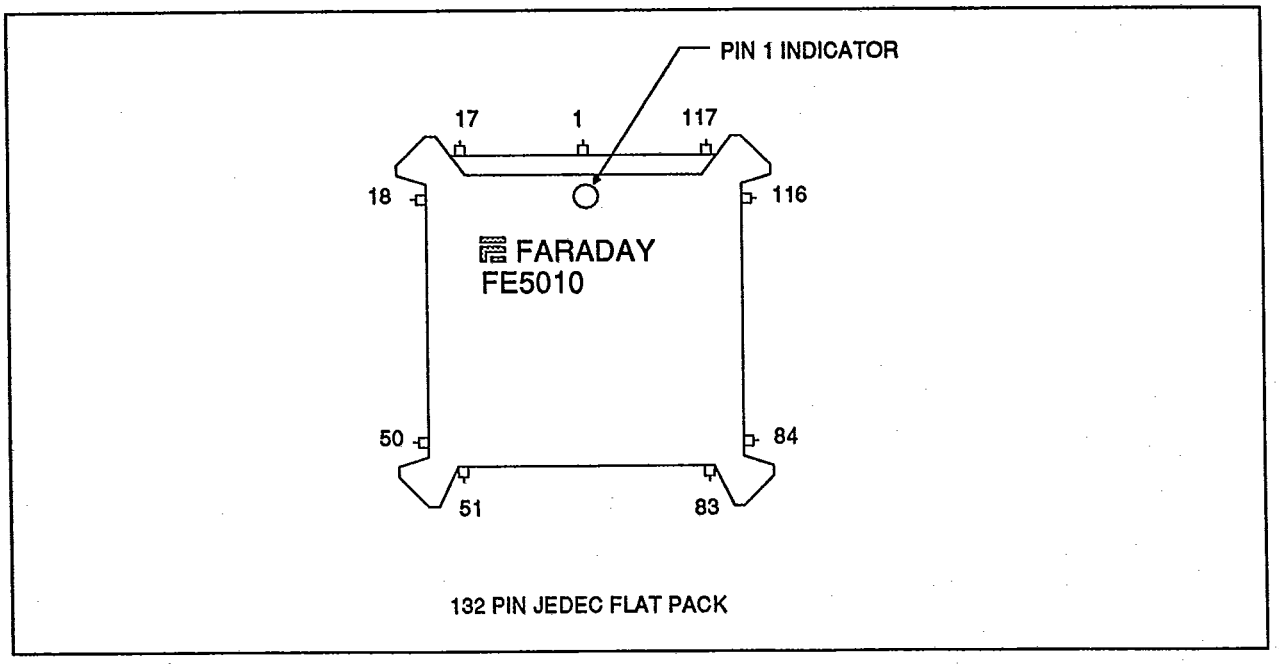


Figure 3. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	D13	34	CLK2X	67	ENSWPAD	100	A14
2	Vss	35	Vss	68	Vss	101	Vcc
3	D12	36	RESET286	69	DRDS16	102	A13
4	D11	37	HOLD	70	EDRENA	103	A12
5	D10	38	DBUFDTR	71	CDSETEN	104	A11
6	D9	39	RAM17	72	ARB/GNT	105	A10
7	D8	40	RAM18	73	PROMCSH	106	A9
8	Vcc	41	RAM19	74	VGAENA	107	A8
9	D7	42	MUX	75	DACK	108	A7
10	D6	43	Vcc	76	Vcc	109	A6
11	D5	44	RWE	77	PREEMPT	110	Vss
12	D4	45	CASALE	78	ARB0	111	A5
13	D3	46	PARCLK	79	Vss	112	A4
14	D2	47	Vss	80	ARB1	113	A3
15	D1	48	PROMCSL	81	ARB2	114	A2
16	D0	49	MASTER	82	ARB3	115	A1
17	Vss	50	ENADL	83	Vcc	116	A0
18	LCLCYC	51	REFRESH	84	NMI	117	Vss
19	SHUTDOWN	52	RESET	85	BHE	118	MIO286
20	Vcc	53	RESET287	86	Vss	119	CMD
21	CHRDYRTN	54	RDY	87	S0	120	ADL
22	FDDRQ	55	A20GTX	88	S1	121	CHS0
23	A20GT	56	RAS0	89	DRAMRDY	122	CHS1
24	HLDA	57	RAS1	90	A23	123	Vcc
25	Vss	58	Vss	91	A22	124	MA20
26	INTR	59	CAS0	92	A21	125	MA0
27	DS16RTN	60	CAS1	93	A20	126	RDLTCH(SPD0)
28	POWERGOOD	61	CAS2	94	A19	127	WRTLTCH(SPD1)
29	BURST	62	CAS3	95	A18	128	ADRLE(SPD2)
30	REFREQ	63	Vcc	96	Vss	129	MASLTCH
31	OSC2X	64	DBUFEN	97	A17	130	Vss
32	TC	65	DTRAD	98	A16	131	D15
33	PCLK	66	ENADH	99	A15	132	D14

1.0 PIN DESCRIPTION

PIN NO.	NAME	TYPE	FUNCTION
			DMA CONTROL
116 115 114 113 112 111 109 108 107 106 105 104 103 102 100 99 98 97 95 94 93 92 91 90	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23	IO	ADDRESS—Bi-directional address bus between the 80286 and FE5010. During CPU transfers this bus is input only. During DMA transfers the bus is output only from the FE5010. During a Channel bus master cycle to system memory, with the exception of A0 and A20 which are outputs, the bus is input only to the FE5010.
16 15 14 13 12 11 10 9 7 6 5 4 3 1 132 131	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	IO	DATA—Bi-directional data bus between the 80286 and FE5010. These data lines are bi-directional between the CPU and FE5010 for CPU transfers, DMA transfers, and Channel bus master transfers.
32	$\overline{TC}$	O	$\overline{TERMINAL\ COUNT}$—The TC line signals that a terminal count condition has been reached by the DMA channel currently servicing the Channel. TC is generated during the last IO bus cycle of the DMA transfer.
49	$\overline{MASTER}$	O	$\overline{MASTER}$—This line steers the address bus. When not asserted the system MPU address and DMA controller address is gated to the Channel. When $\overline{MASTER}$ is asserted addresses from a Channel master are gated to the local CPU bus.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
18	$\overline{\text{LCLCYC}}$	I	$\overline{\text{LOCAL CYCLE}}$—This signal is driven by any device that gates data onto the local bus from IO or memory space which the FE5010 does not recognize as being on the local bus. This signal is used to degate the Channel bus cycle which would occur otherwise.
			CLOCK RESET CONTROL
19	SHUTDOWN	I	SHUTDOWN—This signal is generated by the system 8742 keyboard controller, as commanded by the system CPU, to initiate a system CPU reset.
28	POWERGOOD	I	POWERGOOD—This signal comes from the power supply and indicates the status of the power supply voltages. Power-on-reset (POR) is derived from the state of this line.
31	OSC2X	I	OSCILLATOR 2X—This signal is the clock signal from which all the timings of the FE5010 are generated.
53	RESET287	O	COPROCESSOR RESET—This signal is a reset to the 80287 generated by a POR or IOW to address 00F1H with data = 0.
36	RESET286	O	CPU RESET—This signal is an OR of SHUTDOWN, internally generated ALT HOT RST, and POR. It is synchronized to the 2X CPU CLOCK for the 80286.
34	CLK2X	O	CLOCK 2X—This clock signal is driven to the 80286. It is the same frequency as OSC2X.
52	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$—This signal is the general system Power on Reset (POR).
33	PCLK	O.	PHASED CLOCK—This clock is phase synchronized and half the frequency of the OSC2X. The phase relationship is negative edge to negative edge. This clock is presented as a utility output and has no designated use.
			READY CONTROL
21	CHRDYRTN	I	CHANNEL READY RETURN—This signal is an AND of all the ready inputs from the system; it allows a slave to extend the current bus cycle. The sources for this signal are the Channel slots, PVGA, FE5000 (IORDY) and DRAM control.
54	$\overline{\text{RDY}}$	O	$\overline{\text{READY}}$—This signal to the system CPU is synchronized with the system clock.
89	DRAMRDY	I	DRAM READY—If an external DRAM Controller is being used, (as configured by the state of the FE5030EN line at reset), this signal is an input that provides the bus controller end of cycle information for memory operations.
			ARBITRATION CONTROL
78 80 81 82	ARB0 ARB1 ARB2 ARB3	IO (open collector)	ARBITRATION BUS—These four lines contain the state of all the Channel local arbiters after an arbitration cycle. The master or slave adapter that "owns" this arbitration level, is given ownership of the Channel when the ARB/GNT line goes to the GNT state. When the floppy controller is requesting the bus, these lines may be driven.
26	INTR	I	INTERRUPT—If AC register (0090H) bit 4 is set, and a bus master other than the system CPU is using the buses, this interrupt signal is used to initiate an arbitration cycle. This allows the system CPU to service the interrupt.
77	$\overline{\text{PREEMPT}}$	IO (open collector)	$\overline{\text{PREEMPT}}$—This input initiates an arbitration cycle when asserted by indicating that a Channel adapter wants to use the bus. This line is driven by the AC when the floppy controller requests the bus, a refresh cycle is required, an NMI is received, or when interrupt request is pending (see INTR).
29	$\overline{\text{BURST}}$	I	$\overline{\text{BURST}}$—This input indicates that the current Channel bus owner will continue to hold the bus for more than one transfer. In the case of DMA transfers, BURST is removed during the last IO bus cycle of the transfer or during TC if the terminal count is reached.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
30	$\overline{\text{REFREQ}}$	I	$\overline{\text{REFRESH REQUEST}}$—In the GNT state, this signal indicates that the PREEMPT being serviced by the AC is being driven by the refresh timer in the FE5000. The AC enters the ARB state and requests the local CPU bus. The refresh cycle is executed before returning the bus to the GNT state. If the AC is already in the ARB state, the refresh request extends this per. .d by one bus cycle.
24	HLDA	I	HOLD ACKNOWLEDGE—This signal from the system CPU acknowledges a previous hold request from the AC to gain ownership of the local CPU bus for the DMA Controller or other Channel master.
22	FDDRQ	I	FLOPPY DISK REQUEST—This signal indicates that DMA transfer services are required by the Floppy Disk Controller. The AC translates this request into arbitration level 2.
72	ARB/$\overline{\text{GNT}}$	O	ARBITRATION/$\overline{\text{GRANT}}$—This signal indicates the state of the system arbiter. In the ARB state (high), all local arbiters and adapters must remove their drivers from the bus. During the ARB time, all local arbiters may compete for ownership of the Channel by comparing their arbitration level with other competing arbiters on a bit for bit basis. At the end of the ARB time the Channel is given to the owner of the "winning" arbitration level. This change is signaled by a change of polarity of the line to GNT (low).
37	HOLD	O	HOLD—This signal requests that the system CPU relinquish the local bus for a Refresh, DMA transfer, or Channel master transfer.
84	NMI	IO	NONMASKABLE INTERRUPT—This bi-directional signal when driven by the FE5010 to the system CPU indicates that the AC has reached a timeout condition while monitoring the Channel. When the signal is received from the FE5000, it tells the AC to initiate an arbitration cycle to remove any bus masters so the system CPU can service the NMI.
75	$\overline{\text{DACK}}$	O	$\overline{\text{DMA REQUEST ACKNOWLEDGE}}$—This line signals the floppy disk controller that the current bus cycle from the DMA Controller is for it. The DMA Controller initiates a single transfer (IO read, IO write) while this signal is active.
51	$\overline{\text{REFRESH}}$	O	$\overline{\text{REFRESH}}$—This Channel signal indicates that the memory read operation on the bus is a refresh cycle. The address lines (A0- A10) hold the state of the refresh address counter in the DMA Controller.
			SYSTEM CONTROL
87 88 118	$\overline{\text{S0}}$ $\overline{\text{S1}}$ M$\overline{\text{IO}}$286	IO	$\overline{\text{CPU STATUS}}$ and MEMORY/$\overline{\text{IO}}$—These three lines from the system CPU encode the bus cycle type information. These are inputs during CPU cycles and outputs during DMA and Channel master transfers to memory. See section 6.0 for decodes.
85 116	$\overline{\text{BHE}}$ A0	IO	$\overline{\text{BYTE HIGH ENABLE}}$ and CPU ADDRESS 0—These signals indicate which byte(s) of data are being asserted on the data bus. These are inputs during CPU cycles and outputs during DMA and Channel master transfers to memory. See section 6.0 for decodes.
23	A20GT	I	ADDRESS 20 GATE—This signal is driven from the keyboard controller. When asserted it allows the A20 address line to be gated to the system.
126 127	$\overline{\text{RDLTCH}}$(SPD0) $\overline{\text{WRTLTCH}}$(SPD1)	O	$\overline{\text{READ/WRITE LATCH}}$—During a CPU 16-bit read on an even address to and 8-bit device on the Channel, $\overline{\text{RDLTCH}}$ latches the low data byte. During CPU write operations, $\overline{\text{WRTLTCH}}$ maintains the data on the Channel to satisfy data hold timing to CMD inactive. These signals are asserted to make the data latches transparent during Channel master bus cycles. During system reset, they provide configuration inputs (SPD0, SPD1) to select the system clock rate. See also $\overline{\text{ADRLE}}$ (SPD2) and section 3.0.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
128 129	ADRLE (SPD2) MASLTCH (FE5030EN)	IO	ADDRESS LATCH ENABLE/MASTER LATCH—These two lines latch the address bus. ADRLE latches addresses generated by the system CPU and DMA Controller. MASLTCH latches addresses from a Channel master. During POR these lines are configuration inputs to the FE5010. SPD2 is used in the clock rate selection (see SPD0, SPD1 above and section 3.0). During a reset, FE5030EN is held low to enable the FE5030 for system DRAM control.
50 66	ENADL ENADH	O	ENABLE DATA LOW/HIGH—These two lines enable data from the CPU local bus tri-state buffer to drive the Channel.
67 65	ENSWPAD DTRAD	O	ENABLE SWAP ADDRESS and DATA TRANSFER DIRECTION—These two lines control the 8-bit buffer between the high (Hi) and low (Lo) data buses. Hi/Lo transfers are required when an 8-bit slave is being addressed by a 16-bit master.
55	A20GTX	O	ADDRESS 20 GATED EXTERNAL—This signal is used by an external DRAM/Cache controller to gate the A20 address line from the system CPU.
			DECODES
74	VGAENA	O	VIDEO GRAPHICS ADAPTER ENABLE—This output signal indicates the state of the Video Subsystem Enable Register (03C3H) bit 0.
70	EDRENA	O	EXTENDED DATA REGISTER ENABLE—This output signal is generated by comparing the CPU IO address to the value stored in the ESF pointer register. When active this signal enables the selected ESF register to read or write.
71	CDSETEN	O	CARD SETUP ENABLE—This timing signal decodes IO addresses 0100H to 0107H with the appropriate timing for the FE5000.
125	MA0	IO	CHANNEL A0—This Channel signal together with CBHE from the FE5020 indicates which byte(s) of data are being asserted on the data bus. MA0 is an output when the system CPU or the DMA Controller is the bus master and an input when a Channel adapter is the bus master.
124	MA20	IO	CHANNEL A20—This Channel signal is part of the 24-bit address bus and is controlled by the state of the A20GT and ALT GATE A20 (0092H bit 1) generated internally.
48 73	PROMCSL PROMCSH	O	PROM CHIP SELECT LOW/HIGH—If the system PROM is in a byte wide implementation. CSL is asserted if the address is in the range E0000H to EFFFFH. CSH is asserted if the address is in the range F0000H to FFFFFH. These lines are used by the FE5000 Wait/Ready logic to control the bus cycle length for PROM access. These lines are not used if the EPROM is connected to the FE5030 which would assert LCLCYC.
			CHANNEL CONTROL
119	CMD	IO	COMMAND—This Channel signal defines when data (read or write) is valid on the Channel bus. This signal is an output when the system CPU or the DMA Controller is the bus master. This signal is an input when a Channel adapter is bus master.
120	ADL	IO	ADDRESS DECODE LATCH—This Channel signal is available to an adapter to latch valid address and status. This signal is an output when the system CPU or the DMA Controller is the bus master. This signal is an input when a Channel adapter is bus master.
121 122	CHS0 CHS1	IO	CHANNEL STATUS (0:1)—These two lines and MIO from the FE5020 encode the Channel bus cycle type information. These are outputs during CPU and DMA transfers and inputs during Channel bus master transfers to memory.
27	DS16RTN	I	DATA SIZE 16 RETURN—This signal indicates the selected Channel slave is capable of transferring data in 16-bit units. All the CD DS 16n signals from the system (including signals from each individual Channel slot) must be externally OR'd to generate this signal.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
			DRAM CONTROL
64	$\overline{\text{DBUFEN}}$	O	$\overline{\text{DATA BUFFER ENABLE}}$—This signal enables the DRAM buffers.
46	PARCLK	O	PARITY CLOCK—This signal clocks the parity error latch.
45	CASALE	O	CAS ADDRESS LATCH ENABLE—This signal latches the column addresses so that the DRAMs are guaranteed sufficient hold time.
69	$\overline{\text{DRDS16}}$	O	$\overline{\text{DRAM DATA SIZE 16}}$—This signal generates the DS16RTN signal to the Channel Bus Master.
44	$\overline{\text{RWE}}$	O	$\overline{\text{RAM WRITE ENABLE}}$—This signal is a general write command connecting all the DRAM modules.
56 57	$\overline{\text{RAS0}}$ $\overline{\text{RAS1}}$	O	$\overline{\text{REAL ADDRESS SELECT}}$—These signals latch the raw address into the appropriate DRAM module.
59 60 61 62	$\overline{\text{CAS0}}$ $\overline{\text{CAS1}}$ $\overline{\text{CAS2}}$ $\overline{\text{CAS3}}$	O	$\overline{\text{COLUMN ADDRESS SELECT}}$—These signals latch the column address into the appropriate DRAM module.
42	$\overline{\text{MUX}}$	O	$\overline{\text{MULTIPLEXER SWITCHER}}$—This signal switches the external address multiplexer between row and column addresses.
38	$\overline{\text{DBUFDTR}}$	O	$\overline{\text{DATA BUFFER TRANSMIT/RECEIVE}}$—This signal controls the direction of the data drivers from/to the system DRAM.
39 40 41	RAM17 RAM18 RAM19	O	DRAM ADDRESS—These addresses are generated after the address translation in memory map control.
			MISCELLANEOUS
8,20,43, 63,76,83, 101,123	V_{DD}	I	+5V power supply
2,17,25, 35,47,58, 68,79,86, 96,110, 117,130	V_{SS}	I	0V ground

O = Output, I = Input, IO = Bidirectional

The FE5400 chip set IO map is shown in Table 1.

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	FE5010	DMA Controller chan 0-3 [1]
0018H	FE5010	Extended Function Register [1]
001AH	FE5010	Extended Function Execute [1]
0020 to 0021H	FE5000	Interrupt Controller 1
0040,0042-0044,0047H	FE5000	System Timers
0060H	FE5000	Keyboard Data Port
0061H	FE5000	System Control Port B
0064H	FE5000	RD=Kybd status, WR=Kybd command
0070H	FE5000	RTC/CMOS address register, NMI Mask
0071H	FE5000	RTC/CMOS data port
0074H	FE5000	EAR0 Extended CMOS RAM, ESF
0075H	FE5000	EAR1 Extended CMOS RAM
0076H	FE5000	Extended CMOS RAM data port
0081 to 0083, 0087H	FE5010	DMA Page Registers (0-3) [1]
0089 to 008B, 008FH	FE5010	DMA Page Registers (4-7) [1]
0090H	FE5010	AC [1]
0091H	FE5000	Card Selected Feedback
0092H	FE5000	System Control Port A
0094H	FE5000	System Board Setup
0096,0097H	FE5000	POS, Channel Connector Select
00A0 to 00A1H	FE5000	Interrupt Controller 2
00C0 to 00DFH	FE5000	DMA Controller (even only) [1]
00F0H	FE5000	Coprocessor clear busy
00F1H	FE5000	Coprocessor reset
00F8 to 00FFH	FE5000	Coprocessor
0100, 0101H	FE5000	System ID
0102 to 0107H	FE5000	System Board Configuration (POS)
0278 to 027BH	FE5000	Parallel Port 3
02F8 to 02FFH	FE5000	Alternate Serial Port
0378 to 037BH	FE5000	Parallel Port 2
03BC to 03BFH	FE5000	Parallel Port 1
03B4,03B5,03BA,03C0-03C5H	PVGA1	Video Subsystem [2]
03CE,03CF,03D4,03D5,03DAH	PVGA1	Video Subsystem [2]
03C6 to 03C9H	PVGA1	Video DAC [2]
03F0 to 03F7H	FE5000	Diskette Drive Controller
03F8 to 03FFH	FE5000	Primary Serial Port
0700H	FE5010	ESF Data Register (Default)
[1] No Channel cycle is generated on these IO addresses.		[2] IO location 03C3H (PVGA Enable Register) is in FE5010.

Table 1. System Level I/O Map

2.0 DMA CONTROLLER

The DMA Controller is compatible with the Intel 8237 and includes the IBM extended DMA Controller interface and functions. It has logic to support 8 independent channels. Six of the channels are assigned fixed priorities; two have programmable priorities.

The DMA Controller is a serial transfer device requiring two bus cycles to transfer a word or byte between memory and IO. Each transfer bus cycle takes 200ns or more and requires 2 or more CPU clock cycles. Channel priority and bus arbitration functions are resolved externally.

2.1 INTERFACE

The DMA Controller interfaces to the system on the CPU local bus. It generates and encodes the same control signals as the 80286 as shown in Table 2. DMA Controller programming may be done anytime Hold Acknowledge (HLDA) from the CPU is inactive.

M/$\overline{IO}$	$\overline{S0}$	$\overline{S1}$	DMA OPERATION
0	0	0	Reserved
0	0	1	IO Write
0	1	0	IO Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved

Table 2. DMA Control Signal Encoding

A channel transfer is established by CPU setup and initiated from an external slave source via the arbitration control. The requesting DMA channel is specified on the Arbus input.

2.2 INTERNAL ARCHITECTURE

The internal architecture of the DMA Controller is based on six basic modules described below.

2.2.1 Address Translator

This module converts the CPU interface information (address and data), that may be in PC/AT Compatibility Mode format, into the Extended Mode format which is then stored for run-time use.

2.2.2 RAM Registers

These RAM locations store the base address (24 bits), current address (24 bits), base count (16 bits), current count (16 bits) and current IO address (16 bits) information for each channel. The base register values are write only. The current values are read/write and are written by the CPU at the same time as the Base registers. An additional register, the Transfer Holding Register, is used as temporary storage of the data between bus cycles of a transfer. This register is not available to the system CPU.

Base Memory Address Register—This register is 24 bits and is initialized by the system CPU by byte-wide accesses. This register is not readable by the system CPU.

Current Memory Address Register—This register is 24 bits and is initialized by the system CPU by byte-wide accesses at the same time as the Base register. The system CPU may read this register in byte-wide accesses.

During DMA transfers, this register is incremented or decremented after each memory bus cycle. If Auto-initialize is enabled (see DMA Registers), this register is reloaded at end-of-process (EOP) with the value stored in the Base register. EOP which is internal is generated when the DMA Controller reaches a terminal count condition. This condition creates the $\overline{TC}$ signal from the DMA Controller.

Base Transfer Count Register—This register is 16 bits and is initialized by the system CPU by byte-wide accesses. This register is not readable by the system CPU. The number of transfers is the value in the register +1.

Current Transfer Count Register—This register is 16 bits and is initialized by the system CPU by byte-wide accesses at the same time as the Base register. The system CPU may read this register in byte-wide accesses.

During DMA transfers, the register is decremented after each Memory bus cycle. If Auto-initialize is enabled, this register is reloaded at EOP from the value stored in the Base register. The value of this register at EOP is FFFFH.

Current IO Address Register—This register is initialized by the system CPU in Extended Mode only. The value gated to the bus during the IO bus cycle depends on the state of bit 0 in the Extended Mode Register. If programmed IO address mode is set, then the value in this register is used, otherwise 0000H is used.

2.2.3 DMA Registers

The DMA registers consist of the Mask, Mode, Arbus, and Status registers. The DMA register allocation is shown in Table 3.

REGISTER	SIZE	QTY	ALLOCATION
MASK	4 BITS	2	1 for chan 0–3, 1 for chan 4–7
MODE	8 BITS	8	1 per chan
ARBUS	4 BITS	2	1 for chan 0, 1 for chan 4
STATUS	8 BITS	2	1 for chan 0–3, 1 for chan 4–7

Table 3. DMA Register Allocation

The Mask Register format is shown in Figure 4.

The Mode Register format is shown in Figure 5. See Modes of Operation for descriptions of the various modes and transfer types set in the Mode Register.

There are two Arbus registers, one for DMA channel 0 and one for DMA channel 4. These registers allow an arbitration level to be assigned by software. Normally DMA channels 0 and 4 are assigned levels 08H to 0EH only. Levels 01–03H and 05–07H are assigned to DMA channels 1–3, 5–7. If channel 0 or 4 is assigned to one of these levels, the user must insure that no conflict occurs. Figure 6 shows the format for the Arbus Register.

In Extended Mode, a status read (see Extended Mode) provides the status of channels 0–3. A second read provides the status of channels 4–7. The byte pointer is initialized when the command is given. Figure 7 shows the Status Register format.

2.2.4 Transfer Control

This module interfaces to the 80286 bus. The signals and timing are equivalent to the 80286 and are generated from the same CPU clock source.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED	MASK BIT		CHANNEL SELECT	
0	DIS	ENA	—	—

Set/Clear Interface

1	0	Channel
0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

RESERVED	CH 3 OR 7		CH 2 OR 6		CH 1 OR 5		CH 0 OR 4	
0	DIS	ENA	DIS	ENA	DIS	ENA	DIS	ENA

Set/Reset Interface

Figure 4. Mask Register Format

= Default

MODE SELECT		COUNT DIR		AUTOINITIAL		TRANSFER TYPE		CHANNEL SELECT	
—	—	DEC	INC	ENA	DIS	—	—	—	—

7	6	Mode Select
0	0	Demand
0	1	Single (NU)
1	0	Block (NU)
1	1	Cascade (NU)

PC/AT Compatible Mode

3	2	Transfer Type
0	0	Verify
0	1	Write Mem
1	0	Read Mem
1	1	Reserved

1	0	Channel
0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

RESERVED	WIDTH		RESERVED	COUNT DIR		TRANSFER		TRANSFER		AUTOINITIAL		IO ADR	
0	8 BIT XFER	16 BIT XFER	0	DEC	INC	WRITE MEM	READ MEM	DATA	VERIF	ON	OFF	PROG VALU	0000H

Extended Mode

Figure 5. Mode Register Format

2.3 SYSTEM CPU ACCESS MODES

The DMA Controller can be accessed by the system CPU in two modes: Compatibility Mode and Extended Mode. At run-time the mode by which a transfer was setup is not retained.

The Compatibility Mode command, and the Request and Rotating Priority functions are not supported. The Mode register is only partially supported as detailed in the following sections.

2.3.1 Extended Mode

Extended Mode is accessed through four locations in the IO space as shown in Table 4.

IO ADRS	DESCRIPTION
0018H	Extended Function Register (EFR)(W)
0019H	Reserved
001AH	Extended Function Execute (EFE)(W)
001BH	Reserved

Table 4. Extended Mode IO Addresses

2.3.2 Compatibility Mode

The Compatibility Mode IO Map is described in Table 5.

The format for the Extended Function Register (EFR) at location 0018H is shown in Figure 8.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED				ARBITRATION LEVEL			
—	—	—	—	—	—	—	—

3	2	1	0	Level
0	0	0	0	0 Available
0	0	0	1	1 See Warning
0	0	1	0	2 See Warning
0	0	1	1	3 See Warning
0	1	0	0	4 Available
0	1	0	1	5 See Warning
0	1	1	0	6 See Warning
0	1	1	1	7 See Warning
1	0	0	0	8 Available
1	0	0	1	9 Available
1	0	1	0	A Available
1	0	1	1	B Available
1	1	0	0	C Available
1	1	0	1	D Available
1	1	1	0	E Available
1	1	1	1	F Reserved—System MPU

WARNING:
These levels are assigned to DMA channels 1—3, 5—7. If channel 0 or 4 is assigned to one of these levels, the user must insure that no conflict occurs.

Figure 6. Arbus Register Format

REQUEST STATUS								TC STATUS							
CHAN 3 OR 7		CHAN 2 OR 6		CHAN 1 OR 5		CHAN 0 OR 4		CHAN 3 OR 7		CHAN 2 OR 6		CHAN 1 OR 5		CHAN 0 OR 4	
YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO

Figure 7. Status Register Format

= Default

IO ADRS	DESCRIPTION	BIT WIDTH	BYTE PTR
0000H	Ch 0 Memory Addrs Register (R/W)	00–15	yes [1]
0001H	Ch 0 Transfer Count Register (R/W)	00–15	yes [1]
0002H	Ch 1 Memory Addrs Register (R/W)	00–15	yes [1]
0003H	Ch 1 Transfer Count Register (R/W)	00–15	yes [1]
0004H	Ch 2 Memory Addrs Register (R/W)	00–15	yes [1]
0005H	Ch 2 Transfer Count Register (R/W)	00–15	yes [1]
0006H	Ch 3 Memory Addrs Register (R/W)	00–15	yes [1]
0007H	Ch 3 Transfer Count Register (R/W)	00–15	yes [1]
0008H	Ch 0–3 Status Register	00–07	—
000AH	Ch 0–3 Mask Register (Set/Rst)(W)	00–02	—
000BH	Ch 0–3 Mode Register (W)	00–07	—
000CH	Ch 0–3 Clear Byte Pointer (W)	don't care	—
000DH	Ch 0–3 Master Clear (W)	don't care	—
000EH	Ch 0–3 Clear Mask Register (W)	don't care	—
000FH	Ch 0–3 Write Mask Register (W)	00–03	—
0081H	Ch 2 Page Register (R/W)	00–07	—
0082H	Ch 3 Page Register (R/W)	00–07	—
0083H	Ch 1 Page Register (R/W)	00–07	—
0087H	Ch 0 Page Register (R/W)	00–07	—
0089H	Ch 6 Page Register (R/W)	00–07	—
008AH	Ch 7 Page Register (R/W)	00–07	—
008BH	Ch 5 Page Register (R/W)	00–07	—
008FH	Ch 4 Page Register (R/W)	00–07	—
00C0H	Ch 4 Memory Addrs Register (R/W)	00–15	yes [1]
00C2H	Ch 4 Transfer Count Register (R/W)	00–15	yes [1]
00C4H	Ch 5 Memory Addrs Register (R/W)	00–15	yes [1]
00C6H	Ch 5 Transfer Count Register (R/W)	00–15	yes [1]
00C8H	Ch 6 Memory Addrs Register (R/W)	00–15	yes [1]
00CAH	Ch 6 Transfer Count Register (R/W)	00–15	yes [1]
00CCH	Ch 7 Memory Addrs Register (R/W)	00–15	yes [1]
00CEH	Ch 7 Transfer Count Register (R/W)	00–15	yes [1]
00D0H	Ch 4–7 Status Register	00–07	—
00D4H	Ch 4-7 Mask Register (Set/Rst)(W)	00–02	—
00D6H	Ch 4–7 Mode Register (W)	00–07	—
00D8H	Ch 4–7 Clear Byte Pointer (W)	don't care	—
00DAH	Ch 4–7 Master Clear (W)	don't care	—
00DCH	Ch 4–7 Clear Mask Register (W)	don't care	—
00DEH	Ch 4–7 Write Mask Register (W)	00–03	—

[1] Both Base and Current Memory Address and Transfer Count Registers are loaded on a write operation. Only the Current register is readable.

Table 5. Compatibility Mode IO Map

The Extended Mode protocol is as follows:

1. Write to the EFR (0018H) to set the channel selection and function command. This operation always resets the internal byte pointer to point to the least significant byte (LSB).

Direct Commands require an IO Write to the EFR only, otherwise:

2. Write to or Read from the EFE port the appropriate number of times to execute the function. The byte pointer increments automatically.

Direct Commands written to the EFR include Mask Register Set Bit, Mask Register Reset Bit, and Master Clear. The Mask Register Set Bit command masks (i.e., disables) all channels in the Mask Register. The Mask Register Reset Bit command unmasks (i.e., enables) all the channels in the Mask Register. The Master Clear command does the following:

1. Masks all channels in the Mask Register (i.e., sets all bits to 1).

2. Resets the Status Register (i.e., sets all bits to 0). In addition to the CPU generated Master Clear command, a bus time-out condition generates a Master Clear. If a Master Clear occurs, the DMA Controller must be reinitialized.

2.4 MODES OF OPERATION

Programming the operating mode of the DMA Controller can be done anytime HLDA (see section 5, Arbitration Control) from the CPU is inactive. When HLDA is active the DMA Controller can execute transfer cycles, if previously setup.

The normal operating mode of the DMA Controller is Demand Mode. Once initialized in Demand Mode, transfer modes are determined by the state of the $\overline{\text{BURST}}$ signal (see section 5, Arbitration Control). If in-

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PROGRAMMED COMMAND (1AH)				RESERVED	CHANNEL SELECTION		
BIT 7	BIT 6	BIT 5	BIT 4	0	BIT 2	BIT 1	BIT 0

7	6	5	4	Command	Bit Width	Byte Ptr
0	0	0	0	0 IO Adr Reg (R/W)	00–15	yes
0	0	0	1	1 Reserved	—	—
0	0	1	0	2 Mem Adr Reg (R/W)	00–23	yes
0	0	1	1	3 Mem Adr Reg Read	00–23	yes
0	1	0	0	4 Xfer Cnt Reg (R/W)	00–15	yes
0	1	0	1	5 Xfer Cnt Reg Read	00–15	yes
0	1	1	0	6 Status Reg Read	00–07	yes
0	1	1	1	7 Mode Reg (R/W)	00–07	—
1	0	0	0	8 Arbus Reg (R/W)	00–07	—
1	0	0	1	9 Mask Reg Set Bit	Direct	—
1	0	1	0	A Mask Reg Reset Bit	Direct	—
1	0	1	1	B IBM Test DRQ (NU)	—	[1]
1	1	0	0	C IBM Test Clear (NU)	—	[1]
1	1	0	1	D Master Clear	Direct	—
1	1	1	0	E Reserved	—	—
1	1	1	1	F Reserved	—	—

[1] These functions are not implemented

2	1	0	Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 8. Extended Function Register (EFR) (0018H)

active a Single Transfer is indicated; if active a Demand Transfer is indicated.

2.4.1 Single Transfer Mode

Single Transfer Mode consists of one IO bus cycle and one memory bus cycle in either order.

2.4.2 Demand Transfer Mode

Demand Transfers are characterized as continuous transfers while the $\overline{\text{BURST}}$ signal is active. These transfers may be slave terminated or controller terminated.

Slave Terminated—A slave terminated transfer ends under two conditions:

1. When the slave has transferred one byte or word and has not asserted the $\overline{\text{BURST}}$ signal.

2. When the slave has completed a partial transfer and releases the $\overline{\text{BURST}}$ signal during the *last* $\overline{\text{CMD}}$ active time of the transfer.

DMA Controller Terminated—The DMA Controller may terminate transfers only when a terminal count (TC) has been reached for that channel. At EOP the channel is masked from further operation until interaction by the system CPU.

2.4.3 Verify Mode

Verify Mode performs address and TC generation as in normal transfers. However, only memory read commands are initiated.

2.4.4 Sub-Modes

Auto-initialize Mode allows a channel to operate in a continuous fashion without the interaction of the system CPU. At EOP the value in the Base registers are loaded into the Current registers and the channel remains unmasked.

Each channel Memory Address Register may be set to increment or decrement.

2.4.5 Boundary and End Conditions

When the Memory Address Register reaches the end of a 64K byte segment of memory, it carries into the upper byte of the counter without any indication to the system CPU.

The Memory Address Register rolls over to address 0 and continues if the Transfer Count Register has a valid count remaining and the DMA slave continues to request service. If the transfer is a memory write, no warning is given that low memory is being altered.

The Transfer Count Register decrements to FFFFH and stops. If the register is set to FFFFH initially, the counter decrements until FFFFH is encountered again.

If Auto-initialize is selected for a channel, the associated mask register bit is not set at EOP. Otherwise, EOP causes the channel to be masked (disabled).

3.0 CLOCK/RESET CONTROL

The clock and reset control functions of the FE5010 include:

1. Synchronization of CPU reset with the CPU clock

2. Coprocessor reset

3. General system reset

The Alternate Hot Reset function specified by Control Port A 0092H bit 0 (see Extended Setup Facility, Section 6.2) is write only in the FE5010 and read/write in the FE5000. Figure 9 shows the clock and reset control function of the core logic.

The clock rates supported are shown in Table 6; they are defined during power-on reset (POR) by the state of 3 signal pins. After POR, the pins revert to their normal function. Table 6 also indicates the signal pins for the clock definition.

	CLOCK DEFINITION		
CLOCK RATE	SPD0 $\overline{\text{RDLTCH}}$	SPD1 $\overline{\text{WRTLTCH}}$	SPD2 $\overline{\text{ADRLE}}$
10 MHZ	0	0	0
12.5 MHZ	0	0	1
16 MHZ	0	1	0
20 MHZ	0	1	1

Table 6. Clock Rate Definition

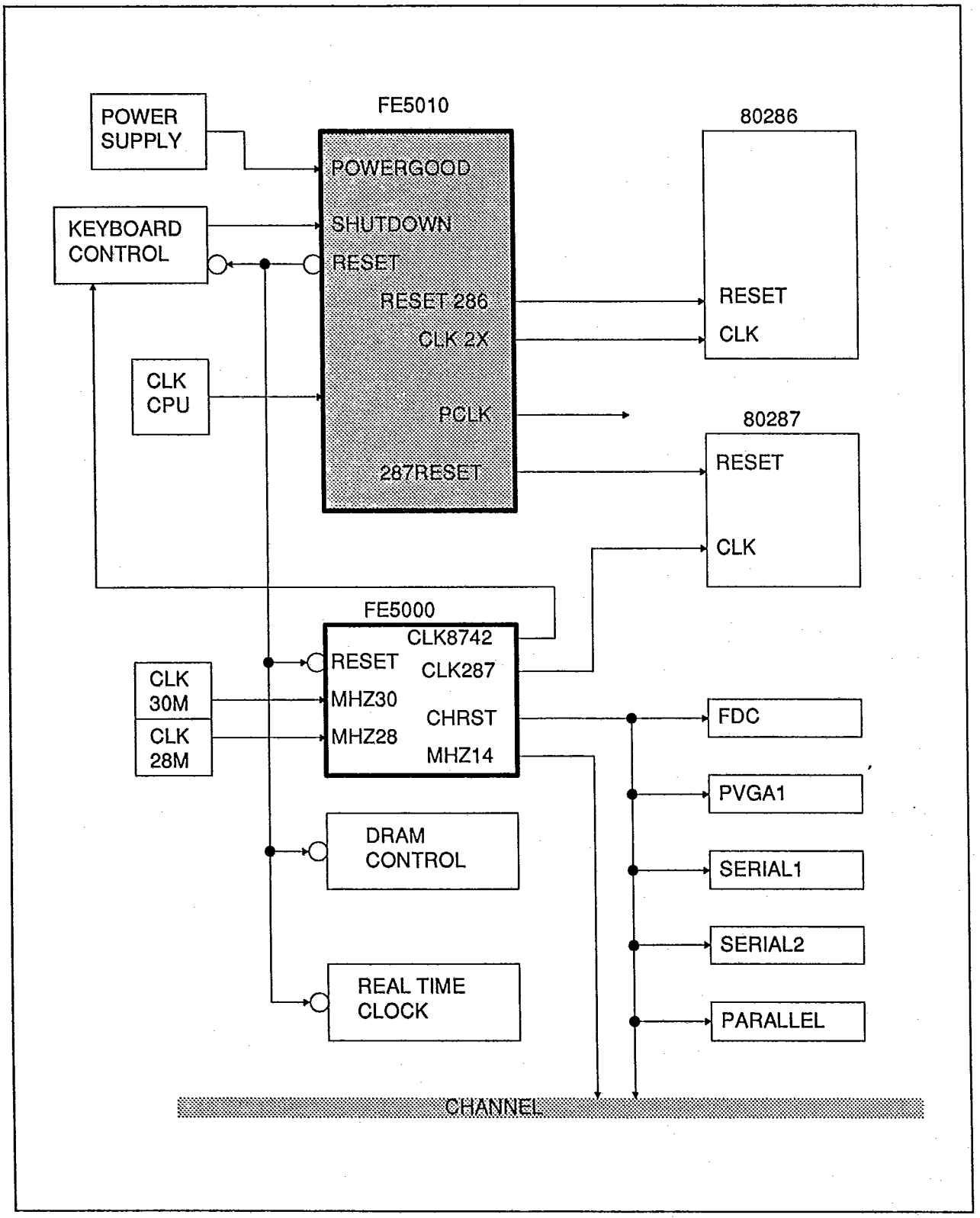


Figure 9. System Clock and Reset Control

4.0 WAIT/READY CONTROL

The FE5010 provides a "normally ready" interface to the system CPU. If an external device requires a longer bus cycle, it must deactivate one of the ready inputs to the FE5010.

This function receives system and Channel wait/ready signals and synchronizes them properly to the CPU.

5.0 ARBITRATION CONTROL (AC)

The AC controls and monitors the Channel and CPU local bus arbitration functions. The functions of the AC are controlled by the bit settings in the Arbitration-Register at location 0090H. Figure 10 shows the format for the Arbitration Register.

5.1 AC FUNCTIONS

5.1.1 Execute Arbitration Cycles

An arbitration cycle is defined as a transition of the ARB/$\overline{GNT}$ signal from a low to high to low (Grant to ARB to Grant). During the ARB time, all competing local arbiters may drive the Arbus to determine the new bus owner. Refresh cycles are executed during the ARB high time and extend the arbitration cycle.

An arbitration cycle can be initiated by the following external events:

- Refresh Request
- Bus Timeout
- Competing Bus Master
- Competing DMA Slave
- NMI
- Bus Idle
- Interrupt (0090H bit 4 = 1)

The Bus Idle condition exists when a Bus Master or DMA slave has been granted the bus and no bus control signals (S0, S1, CMD, BURST) are present (i.e., after DMA slave or Bus Master transfers are done).

5.1.2 Arbitrate the Local CPU Bus

Bus cycles originating from a DMA slave, a Channel bus master, or refresh requests require the system CPU to give up the local bus. The AC performs this arbitration request function.

5.1.3 Regulate Arbitration Cycle Duration

CPU Programmable—When bit 5 of the Arbitration Register equals 1, the default arbitration cycle is extended depending on the CPU clock rate. Table 7 specifies the actual times by the CPU clock rate.

	AC REGISTER (0090H)	
CPU CLOCK	BIT 5 = 0	BIT 5 = 1
10 MHZ	300ns	700ns
12.5 MHZ	320ns	720ns
16 MHZ	312ns	750ns
20 MHZ	300ns	750ns

Table 7. Extending the Default Arbitration Cycle

Arbus = 0000 Special Case—If the Arbus goes to 0000B during an arbitration cycle the arbitration can be truncated to 100ns minimum.

Dynamic Extension of Arbitration Time—The arbitration time can be extended by a NMI or Refresh cycle. A nonmaskable interrupt sets bit 6 in the

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
CPU CYCLES		NMI OCCURRED		BUS TIMEOUT		IRQ MASTER PREEMPT		ARBITRATION LEVEL							
ENA	DIS	YES	NO	YES	NO	ENA	DIS	0 = LSB							
Read															
CPU CYCLES		ARB STATE		ARB CYCLE		IRQ MASTER PREEMPT		RESERVED							
ENA	DIS	ARB	GNT	EXTD	NORM	ENA	DIS	—		—		—		—	
Write															

Figure 10. Arbitration Register Format (0090H)

= Default

Arbitration Register to 1. The CPU must clear the bit to 0 to allow arbitration to resume. A refresh cycle extends the arbitration time by the duration of the memory refresh cycle.

5.1.4 Arbitration Monitor

Because the arbitration mechanism is distributed between the system board and Channel based peripherals, a central monitoring point is necessary to allow for recovery from malfunctions. The AC monitors the Channel bus for conditions where a bus master does not release the bus when requested by an asserted $\overline{\text{PREEMPT}}$ signal. If this condition occurs, the AC allows the system CPU to initiate error recovery.

When a bus time-out occurs, the AC captures the arbitration level of the device and generates a NMI. Additionally, the DMA Controller, Channel control logic and Ready logic are initialized to allow the system CPU to attempt error recovery. All DMA registers must be reprogrammed after bus time-out.

The time-out mechanism is based on the refresh timer that cycles approximately every 15 microseconds. The time-out is armed when a refresh request is pending and the arbiter is in any state except Refresh. If the request is not honored (cleared) before the next refresh request, a bus time-out condition exists.

The Bus Timeout and resulting NMI are held asserted until cleared by a CPU IOW which sets the Arbitration Register bit 6 to 0.

5.1.5 Floppy Disk Controller DMA Interface

This function competes on behalf of the Floppy Disk Controller for ownership of the system bus by converting DMA requests (FDDRQ) into the appropriate signals for the AC. If successful, this interface generates DACK to the FDC.

5.2 ARBITRATION STATES

The arbitration control mechanism has six major states with two primary outputs: the ARB/$\overline{\text{GNT}}$ and CPU HOLD signals. Table 8 shows the relationships between these two signals and the arbitration states.

STATE	ARB/$\overline{\text{GNT}}$	HOLD
SYSTEM	ARB	OFF
CPU	$\overline{\text{GNT}}$	OFF
ARB	ARB	HOLD
REFRESH	ARB	HOLD
GRANT	$\overline{\text{GNT}}$	HOLD
WAIT	$\overline{\text{GNT}}$	HOLD

Table 8. Arbitration States

5.2.1 System/Dispatcher State

The system CPU may execute error recovery programs, diagnostics or other "system" level programs when the arbiter is in this state. In general, normal applications do not execute while the arbiter is in this state.

5.2.2 CPU State

Normal application programs may execute when the arbiter is in this state. Error recovery or supervisory programs may execute when the arbiter is in this state.

5.2.3 ARB State

This is a transition state where the CPU has been requested to yield the bus to a higher priority bus user. When the CPU releases the bus, a refresh cycle or bus master can use the bus.

5.2.4 Refresh State

This is a transition state where a single refresh cycle is generated. When the cycle is finished this state is relinquished.

5.2.5 Grant State

A bus master or DMA slave has won the bus in this state.

5.2.6 Wait State

This is a transition state that allows the DMA Controller to finish both bus cycles of a transfer before relinquishing the bus.

5.3 $\overline{\text{PREEMPT}}$ GENERATOR

The FE5010 generates the $\overline{\text{PREEMPT}}$ signal under the following conditions.

5.3.1 Floppy Controller DMA Request

When the Floppy Disk Controller issues a DRQ and the floppy DMA Controller channel 2 is not masked, the AC generates a $\overline{\text{PREEMPT}}$ on behalf of the Floppy Disk Controller. The $\overline{\text{PREEMPT}}$ for this case is cleared when a DMA Master Clear command is received, or the bus is won by another device.

5.3.2 Refresh Request

When the ARB/$\overline{\text{GNT}}$ line is in the GNT state, a Refresh Request causes a $\overline{\text{PREEMPT}}$.

5.3.3 Arbitration Register Bit 6 Set

When the ARB/$\overline{GNT}$ line is in the GNT state, an Arbus value other than 0FH (not system board) and NMI sets bit 6 in the Arbitration Register which causes a $\overline{PREEMPT}$.

5.3.4 Interrupt Request

When the ARB/$\overline{GNT}$ line is in the GNT state, an Arbus value other than 0FH (not system board), bit 4 set in the Arbitration Register, and an active interrupt request to the CPU generates a $\overline{PREEMPT}$.

6.0 SYSTEM CONTROL

The System Control function interfaces to the system board buffers and latches and provides other miscellaneous interface functions. The system control bus signals $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO286}$ encode the CPU bus cycle type information as shown in Table 9.

Signals $\overline{BHE}$ and A0 indicate which byte(s) of data are being transferred on the data bus (see Table 10).

$\overline{ENSWPAD}$ enables byte transfer direction to be swapped between the high and low data bus. $\overline{DTRAD}$ enables the direction of the transfer (i.e., low byte first or high byte first). Table 11 shows the encoding for this function.

6.1. MISCELLANEOUS FUNCTIONS

The System Control function includes the following addresses.

1. The ESF Pointer Register (EPR) at location 0FFFFDH or FFFFFDH which is used to decode the ESF Data Register (EDR).

2. Setup Mode timing strobe ($\overline{CDSETEN}$)

3. The VGA Enable Register (03C3H)

4. Refresh Address Generator (11 bits)

The PVGA Enable Register (03C3H) format is defined in Figure 11. The output VGAENA reflects the status of this register; when set to 1, VGAENA indicates that the video subsystem is enabled.

CPU BUS CYCLE			
M/$\overline{IO286}$	$\overline{S1}$	$\overline{S0}$	TYPE
0	0	0	Interrupt Acknowledge
0	0	1	IO Read
0	1	0	IO Write
0	1	1	None
1	0	0	If CPU ADR 1 = 1 then Halt, else shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None

Table 9. CPU Bus Cycle Type

$\overline{BHE}$	A0	FUNCTION
0	0	Word transfer
0	1	Byte transfer on upper byte (8:15)
1	0	Byte transfer on lower byte (0:7)
1	1	Will not occur

Table 10. Data Bus Transfer Type

$\overline{DTRAD}$	$\overline{ENSWPAD}$	FUNCTION
0	0	Enable Lo to Hi
X	1	Disable Swap
1	0	Enable Hi to Lo
X	1	Disable Swap

Table 11. Byte Transfer Configuration

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED							VGA SUBSYSTEM	
—	—	—	—	—	—	—	ENA	DIS

Figure 11. PVGA Register Format

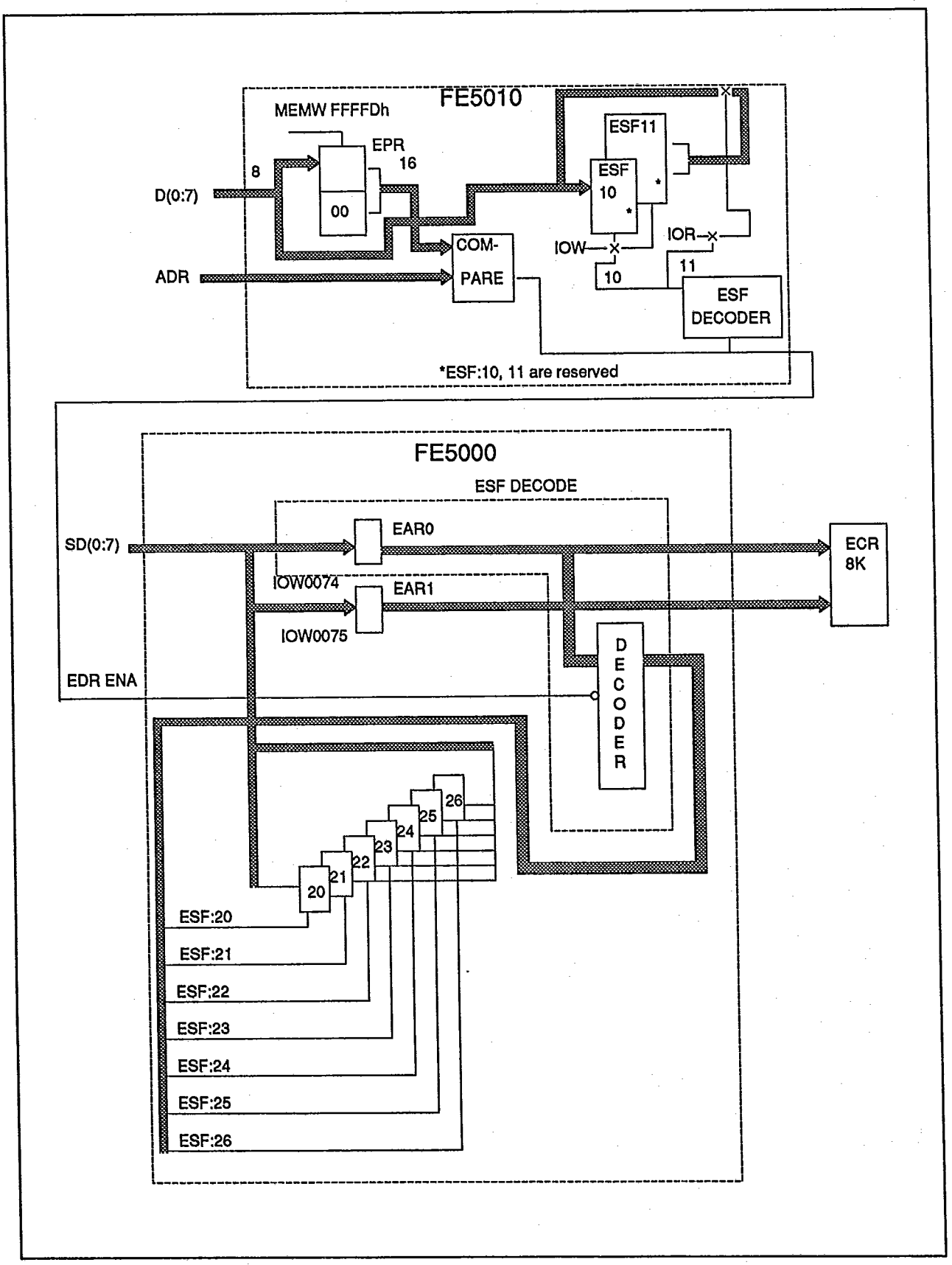


Figure 12. ECR and ESF Block Diagram

6.2 EXTENDED SETUP FACILITY (ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable ($\overline{EDRENA}$) output from the FE5010 to the FE5000. ESF is designed to extend the configuration architecture established with the POS features. See Figures 12 and 13 for an overview of the ESF function. ESF supports:

- Memory Map Control Registers
- Additional physical serial port (SP2)
- Programmable Port Enables A and B
- EMS control registers
- External DRAM control configuration
- System board LAN configuration
- Customer specified enhancements that could include:
  - System Identification
  - System Version

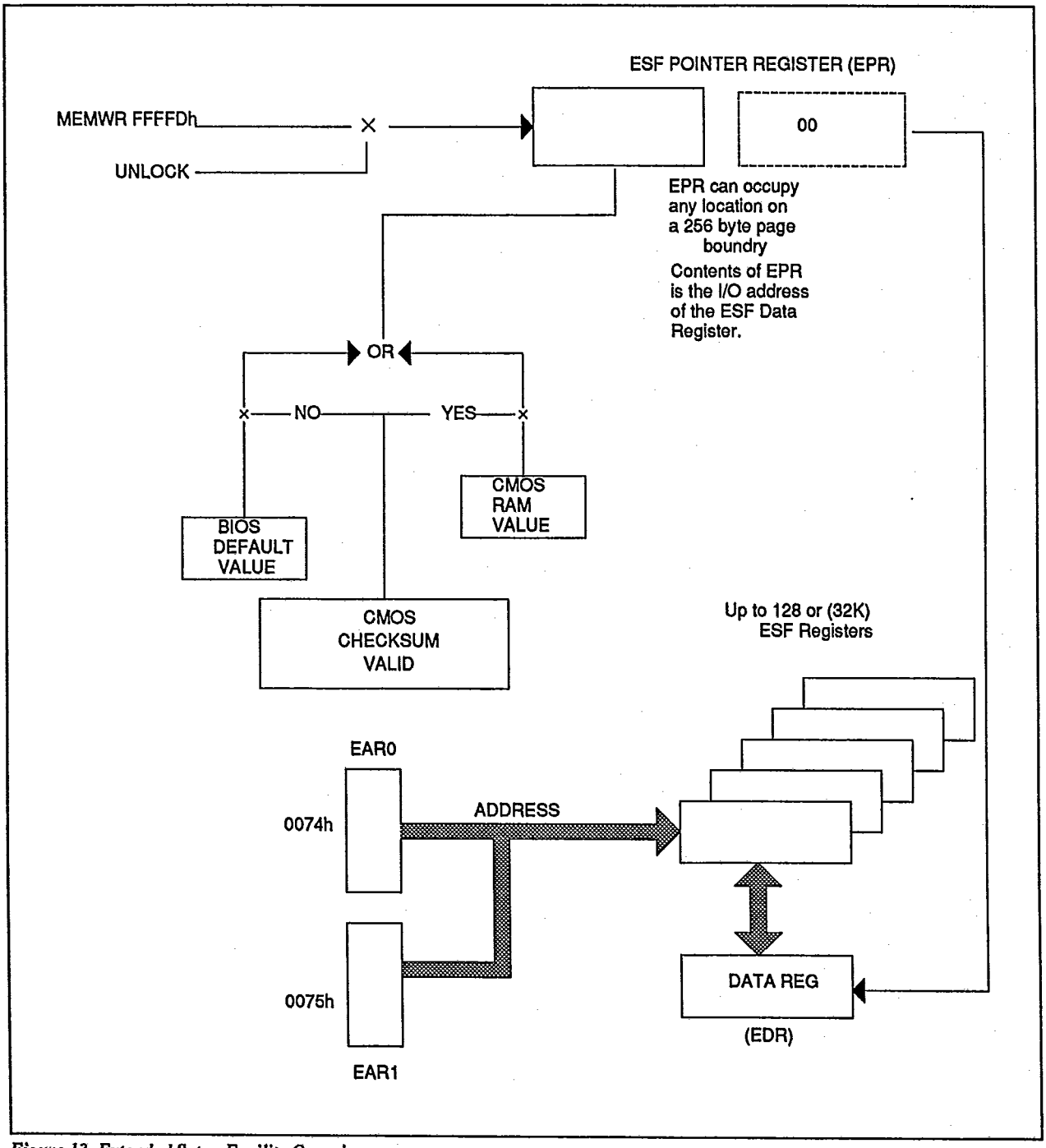


Figure 13. Extended Setup Facility Overview

6.2.1 ESF Access

ESF is based on an "alternate IO space" concept similar to how IBM has implemented their Extended CMOS RAM feature. ESF space (128 locations expandable to 32K) is accessed through a single "real IO space" window called the ESF Data Register (EDR). ESF space may be implemented as either word or byte-wide at the discretion of the designer.

The EDR is pointed to by the software configurable (write only) ESF Pointer Register (EPR) located in the FE5010. The EPR is loaded by writing to memory location FFFFDH or FFFFFDH (normally a PROM). The power-on default location for the EDR is located at IO address 0700H.

The following procedure is recommended for modifying the EPR:

1. Set the value 8DH in port 0070H to disable NMI.

2. Read the System Control Port B at 0061H and test for a change in the state of bit 4 (Refresh Toggle) to synchronize to the refresh circuitry.

3. Read EAR0 at 0074H (normally write only) to unlock the EPR.

4. Write the new value into the EPR (FFFFDH). This locks the EPR again.

5. Enable NMI if required. Note that the EPR is locked when written or on the next refresh cycle, whichever occurs first.

The value in the EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K IO space of the CPU from 0400H to FF00H.

To address the ESF IO space:

1. Write the value 8DH to port 0070H to disable NMI.

2. Write the address value to EAR0 at 0074H (and EAR1 if expanded ESF is being used).

3. Issue an IO Read or Write command to EDR Address.

The selected ESF register is determined by decoding the EAR0 address value.

6.2.2 ESF Address Maps

The lower 64 bytes (EAR0 = 00H–3FH) are reserved for Faraday functions and features. The top 64 bytes (EARO =40H–7FH) are for customer use (see Table 12). All functions using ESF must include bit 7 in the decode. Bit 7 of EAR0 must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 locations, set EAR0 bit 7 to 1 and write the second ESF address byte to EAR1.

ESF ADDRESS	DEFINITION
00H–0FH	System Reserved
10H–1FH	System board core functions
20H–3FH	System board peripheral functions
40H–7FH	Customer Specified
0080H–FFFFH	Expansion (EAR0 bit 7 must be 1)

Table 12. ESF General Usage Map

The ESF address map in a system environment is shown in Table 13. It includes the FE5030 usage.

ESF ADDRESS	DEFINITION
ESF:10	DRAM Control Register (DCR)
ESF:11	System RAM Boundary Reg (SRBR)
ESF:16	RAM Control (FE5030)
ESF:17	Bank 0 Boundary (FE5030)
ESF:18	Bank 1 Boundary (FE5030)
ESF:19	Bank 2 Boundary (FE5030)
ESF:1A	Bank 3 Boundary (FE5030)
ESF:1B	Split Memory Address (FE5030)
ESF:1C	SRBR (FE5030)
ESF:1D	Timing Control (FE5030)
ESF:1E	EMS Control (FE5030)
ESF:1F	Cache Control (FE5030)
ESF:20	Peripheral Configuration Reg (PCR)
ESF:21,24	Port A, B Control Registers
ESF:22,25	Port A, B Address Register (LSB)
ESF:23,26	Port A, B Address Register (MSB)
ESF:80–FF	EMS Page Registers (FE5030)

Table 13. ESF System Address Map

7.0 CHANNEL CONTROL

The Channel Bus Control interfaces to the Channel directly. This function translates the system CPU signals from/to the equivalent Channel signals. The ALT GATE A20 function of Control Port A (0092H) bit 1 in FE5000 is duplicated as a write only function in this block.

The Channel control bus signals $\overline{\text{CHS0}}$, and $\overline{\text{CHS1}}$ are used with $\overline{\text{MIO}}$ from the FE5020 to encode the Channel cycle type information (see Table 14).

M/IO	CHS1	CHS0	BUS CYCLE TYPE
0	0	0	Interrupt Acknowledge
0	0	1	IO Read
0	1	0	IO Write
0	1	1	No Cycle
1	0	0	Halt / Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	No Cycle

Table 14. Channel Bus Cycle Type

Channel signal MA0 and CHBHE (from the FE5020) indicates which byte(s) of data are being asserted on the data bus (see Table 15).

CHBHE	MA0	FUNCTION
0	0	Word transfer
0	1	Byte transfer on upper byte (8:15)
1	0	Byte transfer on lower byte (0:7)
1	1	Will not occur

Table 15. Channel Bus Transfer Type

Table 16 shows the relationship between CPU clock frequency and Channel cycle time.

CLOCK RATE	CHANNEL CYCLE
10 MHZ	300 ns (1–WS)
12.5 MHZ	320 ns (2–WS)
16 MHZ	312 ns (3–WS)
20 MHZ	300 ns (4–WS)

Table 16. Clock Rates vs. Cycle Times

8.0 MEMORY CONTROL

Memory control functions on the FE5010 are discussed under the following headings.

8.1 SYSTEM BOARD DRAM

The FE5010 DRAM Controller handles two banks of DRAM memory. The banks can be disabled and/or swapped in the memory map, thus allowing a fault in either bank to be bypassed by the system. The FE5010 supports RAS-only refresh and simple RAS/CAS DRAM controls.

Table 17 illustrates the relationship between CPU clock frequency and memory cycle times.

CLOCK RATE	MEMORY CYCLE	DRAM ACCESS
10 MHz	200 ns (0-WS)	100 ns
12.5 MHz	240 ns (1-WS)	100 ns
16 MHz	250 ns (2-WS)	100 ns
20 MHz	200 ns (2-WS)	100 ns

Table 17. CPU Clock Frequency and Memory Cycle Times

8.2 MEMORY MAPPING

Memory can be mapped in the configurations tabulated below (Table 18, Memory Maps 1–4). Any memory accesses above the SRBR value are directed to the channel. All DRAM locations are word-wide; all PROM and EPR locations are byte-wide. Internal map control can be disabled in favor of external map control. All maps include the EPR write-only location FFFFDH or FFFFFDH. Where 1MB DRAMs are used, a special feature allows Maps 5 and 6 to be selected if one of the two banks is found defective. This allows the system to work with a decreased memory size.

MEMORY MAP 1	
ADDRESS RANGE	1MB SYSTEM DRAM AND PROM
00000–9FFFFH	640K System Board DRAM
A0000–BFFFFH	128K System Board Video RAM
C0000–DFFFFH	128K Channel ROM
E0000–FFFFFH	128K System Board PROM (BIOS)
100000–15FFFFH	384K System Board DRAM
FE0000–FFFFFFH	128K System Board PROM (BIOS)
MEMORY MAP 2	
ADDRESS RANGE	1MB SYSTEM DRAM ONLY
00000–9FFFFH	640K System Board DRAM
A0000–BFFFFH	128K System Board Video RAM
C0000–DFFFFH	128K Channel ROM
E0000–FFFFFH	128K System Board DRAM (BIOS)
100000–13FFFFH	256K System Board DRAM
FE0000–FFFFFFH	128K System Board DRAM (BIOS)
MEMORY MAP 3	
ADDRESS RANGE	4MB SYSTEM DRAM AND PROM
00000–9FFFFH	640K System Board DRAM
A0000–BFFFFH	128K System Board Video RAM
C0000–DFFFFH	128K Channel ROM
E0000–FFFFFH	128K System Board PROM (BIOS)
100000–3FFFFFH	3MB System Board DRAM
400000–45FFFFH	384K System Board DRAM
FE0000–FFFFFFH	128K System Board PROM (BIOS)

MEMORY MAP 4	
ADDRESS RANGE	**4MB SYSTEM DRAM ONLY**
00000–9FFFFH	640K System Board DRAM
A0000–BFFFFH	128K System Board Video RAM
C0000–DFFFFH	128K Channel ROM
E0000–FFFFFH	128K System Board DRAM (BIOS)
100000–3FFFFFH	3MB System Board DRAM
400000–43FFFFH	256K System Board DRAM
FE0000–FFFFFFH	128K System Board DRAM (BIOS)
MEMORY MAP 5	
ADDRESS RANGE	**2MB SYSTEM DRAM AND PROM**
00000–9FFFFH	640K System Board DRAM
A00000–BFFFFH	128K System Board Video RAM
C0000–DFFFFH	128K Channel ROM
E0000–FFFFFH	128K System Board PROM (BIOS)
100000–1FFFFFH	1MB System Board DRAM
200000–25FFFFH	384K System Board DRAM
FE0000–FFFFFFH	128K System Board PROM (BIOS)
MEMORY MAP 6	
ADDRESS RANGE	**2MB SYSTEM DRAM ONLY**
00000–9FFFFH	640K System Board DRAM
A00000–BFFFFH	128K System Board Video RAM
C0000–DFFFFH	128K Channel ROM
E0000–FFFFFH	128K System Board DRAM (BIOS)
100000–1FFFFFH	1MB System Board DRAM
200000–23FFFFH	256K System Board DRAM
FE0000–FFFFFFH	128K System Board PROM (BIOS)

Table 18. Memory Map Configurations

8.3 DRAM AND MEMORY MAP CONTROL

The FE5010 DRAM control and mapper can handle one or two banks of DRAM memory and reconfigures the addresses needed to implement the memory maps. To do this, the system board must have at least 1MB of DRAM.

The System RAM Boundary Register (SRBR) is an 8-bit read/write register (ESF 11) that specifies the upper boundary address of the on-board system DRAM in 128Kb increments. See Figure 14 for details. Addresses beyond this boundary may be added through a plug-in Channel adapter. The POR default value of the SRBR is 0AH. When using the internal DRAM controller, the value of the SRBR is restricted to those values shown in Table 19. Table 19 defines the SRBR values and the memory maps supported by the FE5010 internal memory control and mapper.

DESCRIPTION	SRBR VALUE
Memory Map 1	0AH [1]
Memory Map 2	09H
Memory Map 3	22H
Memory Map 4	21H
Memory Map 5	12H
Memory Map 6	11H
	[1] POR Default Value

Table 19. SRBR Values and Memory Maps

The DRAM Control Register (DCR) allows the system MPU to modify the operation and set up of memory map control. Bit A24, which allows an extra 384K bytes to be mapped above the 16MB boundary, must be programmed to allow the system MPU to access this DRAM. (See Figure 15.)

The first megabyte of system memory space contains 384K of non-DRAM functions which is physically mapped on to the system board DRAM space as illustrated in Figure 16. The upper 128K (Seg C in Figure 16) maps EPROM. BIOS should be copied to this section of RAM whenever a map specifies DRAM in lieu of PROM. Write Enable to that address range must be inhibited by setting ESF10:7=1, and the SRBR must be modified to reflect the new reduced system RAM boundary.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

MAP ADDRESS							
ADR 24	**ADR 23**	**ADR 22**	**ADR 21**	**ADR 20**	**ADR 19**	**ADR 18**	**ADR 17**

Figure 14. System RAM Boundary Register (SRBR) ESF 11

Where there is an external DRAM controller (FE5030), the internal controls must be disabled (ESF10:5=0). This bit is configured at POR according to the state of the $\overline{\text{MASLTCH}}$ (FE5030EN) pin during POR. With either controller, the SRBR must be active; it will be write-only in the case of an external controller.

7		6		5		4		3		2		1		0	
1	0		0	1	0	1	0	1	0	1	0	1	0	1	0

WRITE PROTECT		RESERVED	INTERNAL DRAM CTRL		BANK 2		BANK 1		RESERVED	RESERVED	SRBR A24 ENABLE	
ENA	WP	—	ENA	DIS	ENA	DIS	ENA	DIS	—	—	DIS	ENA

Write Protect for Maps 2, 4, 6, 8

Gated with FE5030EN

Figure 15. System DRAM Control Register (DCR) ESF 10

= Default

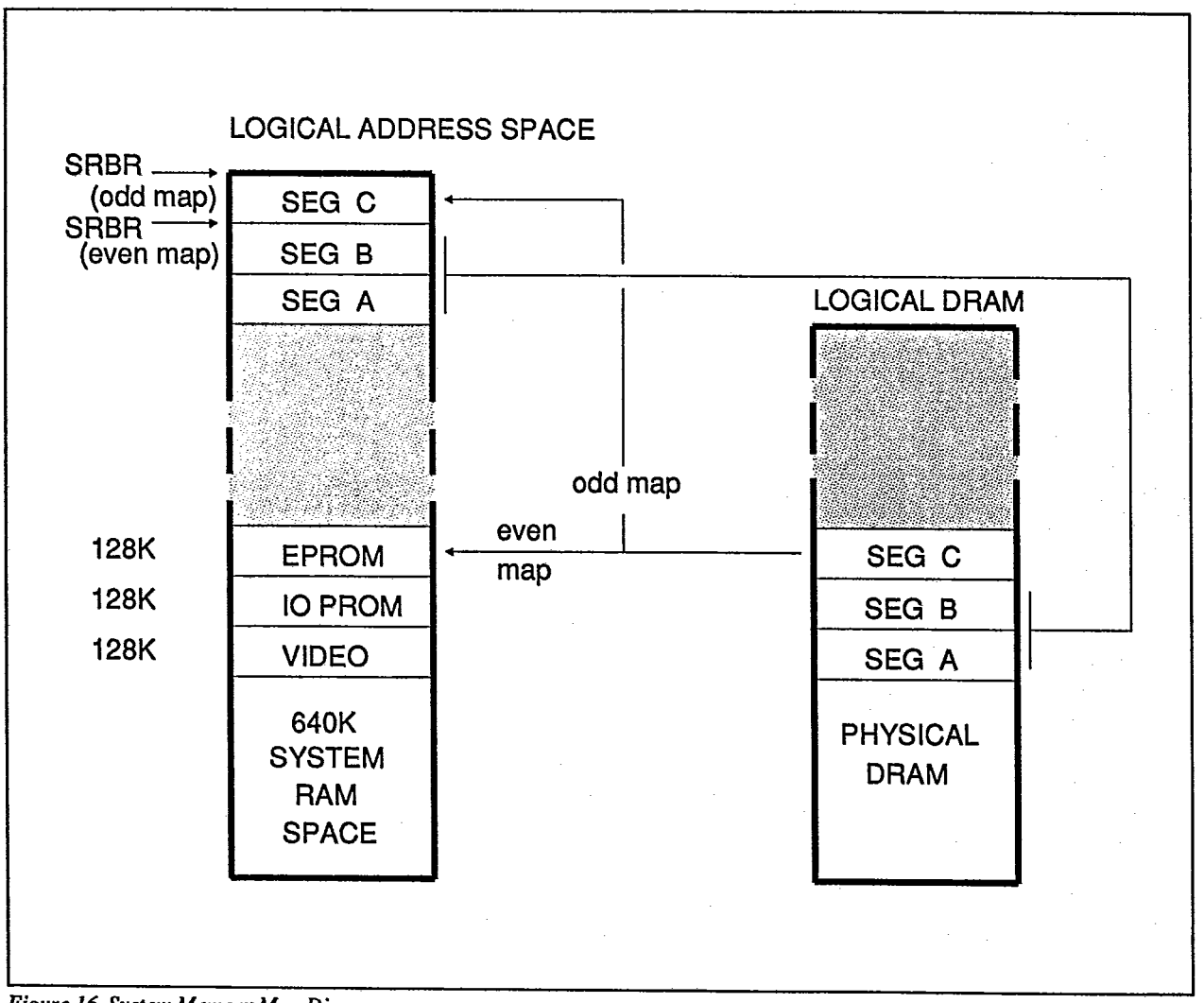


Figure 16. System Memory Map Diagram

9.0 TECHNICAL SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

These are absolute maximum stress ratings for the device. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}–V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}–0.3	V_{DD}+0.3	V
Bias on output pin	V_{OABS}	V_{SS}–0.3	V_{DD}+0.3	V
Storage Temperature	T_S	–40	125	°C

9.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

(V_{SS} = 0 V)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.5	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	–0.3	V_{DD}+0.3	V
Power Dissipation	P_W	—	TBD	mW
Supply Current	I_{DD}	—	TBD	mA

9.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input capacitance @ f_C= 1 MHz	C_I	—	10	pF
*I/O Capacitance	C_{IO}	—	15	pF
Logic high input voltage	V_{IH}	2.0	—	V
Logic low input voltage	V_{IL}	—	0.8	V
*Input leakage	I_{IL}	—	±10	uA
*Tri-state output leakage	I_{OL}	—	±30	uA
*I/O Pin Leakage	I_{IOL}	—	±40	uA
OUTPUTS $\overline{\text{PREEMPT}}$, $\overline{\text{ARB}}$ [3:0], MA0, MA20, $\overline{\text{CHS}}$ [1:0], $\overline{\text{ADL}}$, $\overline{\text{CMD}}$, $\overline{\text{TC}}$, $\overline{\text{REFRESH}}$, $\overline{\text{ARBGNT}}$				
Source current @ V_{OH}= 2.4 V	I_{OH}	4	—	mA
Sink current @ V_{OL}= 0.4 V	I_{OL}	24	—	mA
ALL OTHER OUTPUTS				
Source current @ V_{OH}= 2.4 V	I_{OH}	1	—	mA
Sink current @ V_{OL}= 0.4 V	I_{OL}	4	—	mA

***Notes:**
Pins D [15:0] and $\overline{\text{LCLCYC}}$ have internal pullups of 8 K ohms nominal value. Measurements of output current, input capacitance, leakage current values will be affected by these resistances.

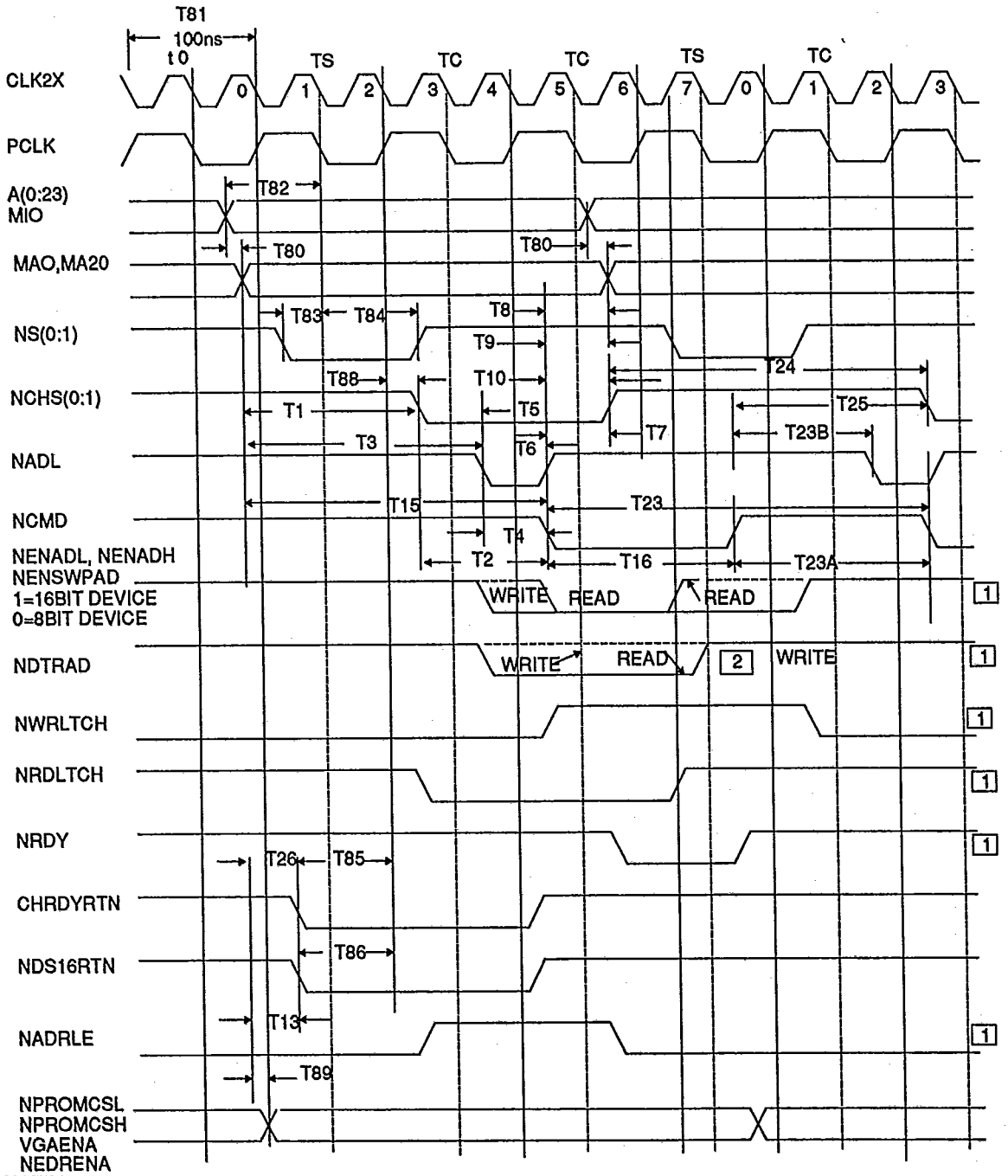
Pins ARB [3:0] and $\overline{\text{PREEMPT}}$ are open collector outputs. Source current value does not apply. External pullups are required on these outputs.

10.0 TIMING

PARAM	DESCRIPTION	10 MHZ MIN	10 MHZ MAX	12.5 MHZ MIN	12.5 MHZ MAX	16 MHZ MIN	16 MHZ MAX	20 MHZ MIN	20 MHZ MAX	NOTE
T1	MA(20,0) valid to $\overline{CHS}$(1:0) valid	95	171	68	141	45	115	31	96	—
T2	$\overline{CHS}$(1:0) valid to $\overline{CMD}$ on	100	100	80	80	63	63	75	75	2
T3	MA(20,0) valid to $\overline{ADL}$ on	145	221	108	181	60	130	56	121	—
T4	$\overline{ADL}$ on to $\overline{CMD}$ on	50	50	40	40	47	47	50	50	2
T5	$\overline{CHS}$(1:0) valid to $\overline{ADL}$ on	50	50	40	40	16	16	25	25	2
T6	$\overline{ADL}$ pulse width	50	50	40	40	63	63	50	50	2
T7	$\overline{CHS}$(1:0) hold after $\overline{ADL}$ off	50	50	80	80	109	109	75	75	2
T8	MA(20,0) hold after $\overline{ADL}$ off	29	105	99	172	120	190	129	194	—
T9	MA(20,0) hold after NCMD on	29	105	99	172	135	205	129	194	—
T10	$\overline{CHS}$(1:0) hold after $\overline{CMD}$ on	50	50	80	80	125	125	75	75	2
T13	MA(20,0) valid to $\overline{DS16RTN}$ on	—	55	—	55	—	55	—	55	1
T15	MA(20,0) valid to $\overline{CMD}$ on	195	271	148	221	107	177	106	171	—
T16	$\overline{CMD}$ pulse width	150	150	120	120	156	156	150	150	2
T23	$\overline{CMD}$ on to next $\overline{CMD}$ on	300	300	320	320	313	313	300	300	2
T23A	$\overline{CMD}$ off to next $\overline{CMD}$ on	150	150	200	200	156	156	150	150	2
T23B	$\overline{CMD}$ off to next $\overline{ADL}$ on	100	100	160	160	109	109	100	100	2
T24	$\overline{CHS(1:0)}$ off to next $\overline{CHS(1:0)}$ on	150	150	160	160	125	125	150	150	2
T25	$\overline{CHS(1:0)}$ valid to last $\overline{CMD}$ off	-50	-50	-120	-120	-94	-94	-75	-75	2
T26	MA(20,0) valid to CHRDYRTN off	—	60	—	60	—	60	—	60	1
T80	A(20,0) to MA(20,0) path delay	10	30	10	30	10	30	10	30	—
T81	CLK2X period	50	50	40	40	31	31	25	25	2
T82	A(23:0) setup to CLK2X	65	—	68	—	34	—	26	—	—
T83	$\overline{S(1:0)}$ setup to CLK2X	28	—	22	—	13	—	11	—	—
T84	$\overline{S(1:0)}$ hold after CLK2X	1	30	3	20	1	20	1	16	—
T85	CHRDYRTN setup to CLK2X	85	—	55	—	29	—	20	—	—
T86	$\overline{DS16RTN}$ setup to CLK2X	90	—	60	—	34	—	25	—	—
T87	MA0 hold after $\overline{CMD}$ on	100	100	80	80	63	63	50	50	4
T88	CLK2X to output delay (typ)	10	32	10	32	10	32	10	32	—
T89	$\overline{PROMCS}$,VGAENA,$\overline{EDRENA}$ delay	10	30	10	30	10	30	10	30	—

Table 20. CPU to Channel Cycles (in nsec)

Notes:
1. Timing parameters associated with adapter performance.
2. These min/max timings should be considered typical values only and are based on multiples of the CLK2X frequency (T81).
3. This table applies to Figures 14–21.
4. T87—Refer to Figures 18–21.



NOTES:

1 EDGE TRANSITIONS ON THESE SIGNALS OCCUR T88 FROM NEAREST NEGATIVE EDGE TRANSITION OF CLK2X.

2 THIS EDGE GENERATED FROM POSITIVE EDGE OF CLK2X.

Figure 17. 10 MHZ CPU Cycle to Channel

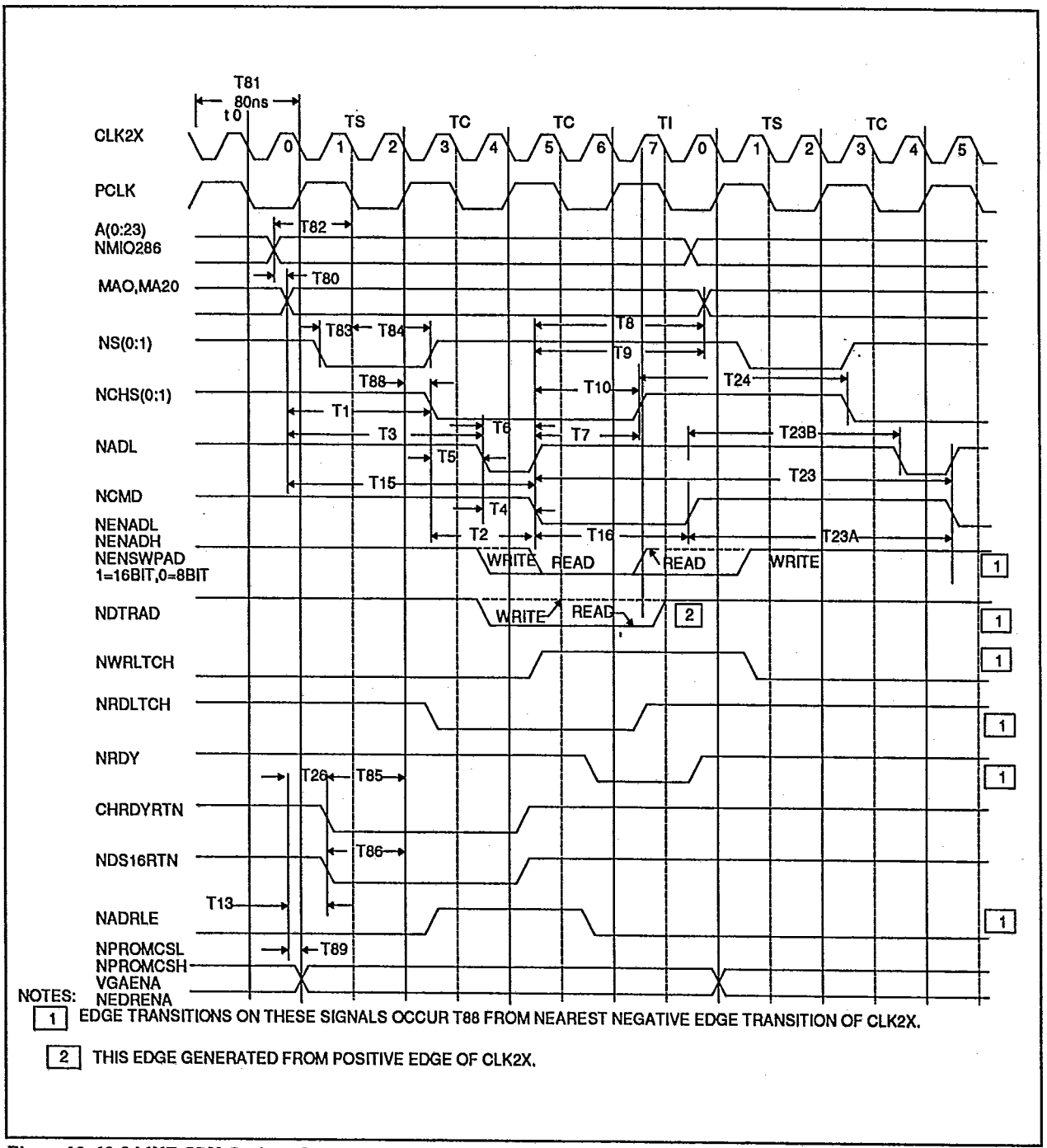


Figure 18. 12.5 MHZ CPU Cycle to Channel

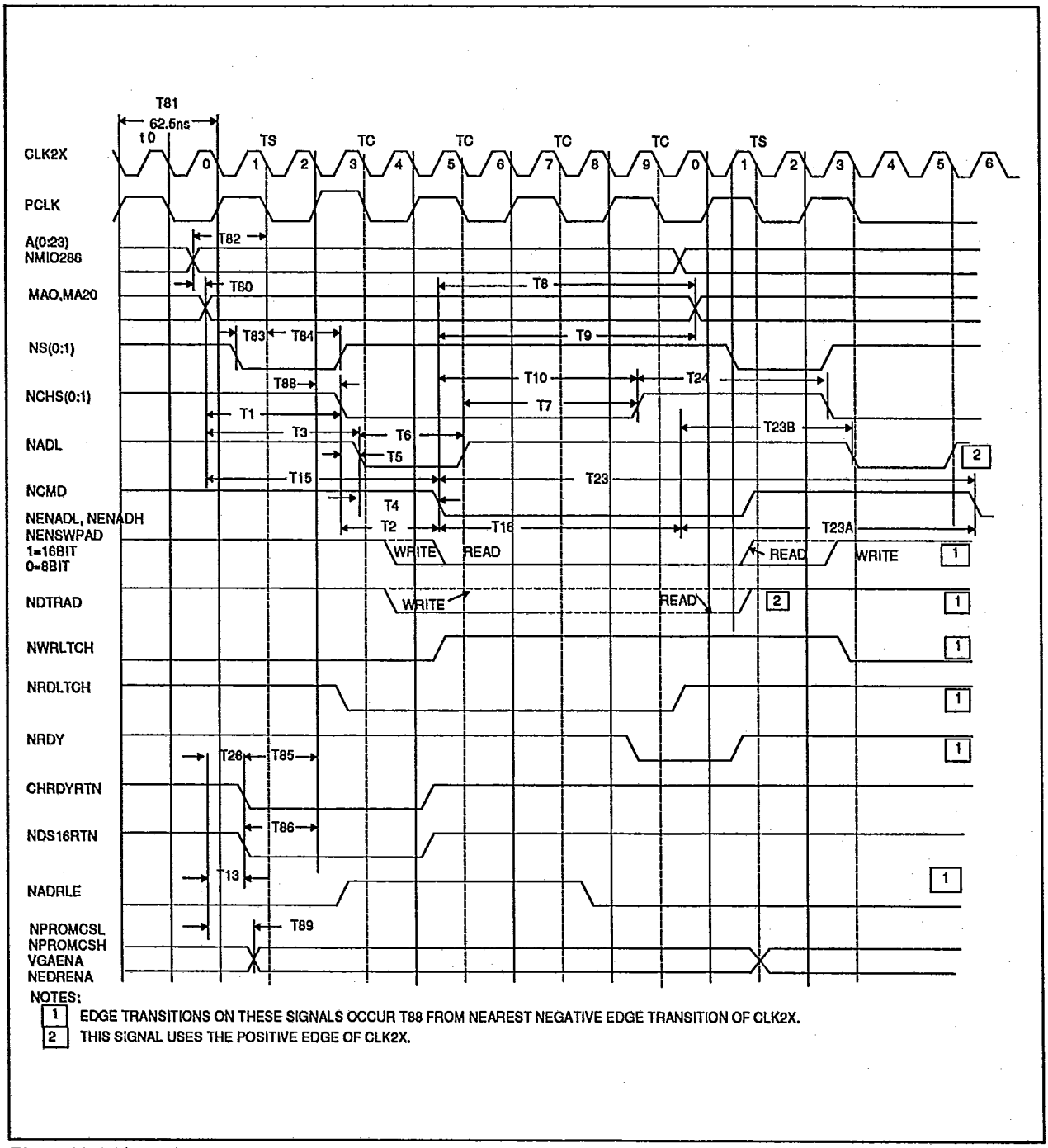


Figure 19. 16 MHZ CPU Cycle to Channel

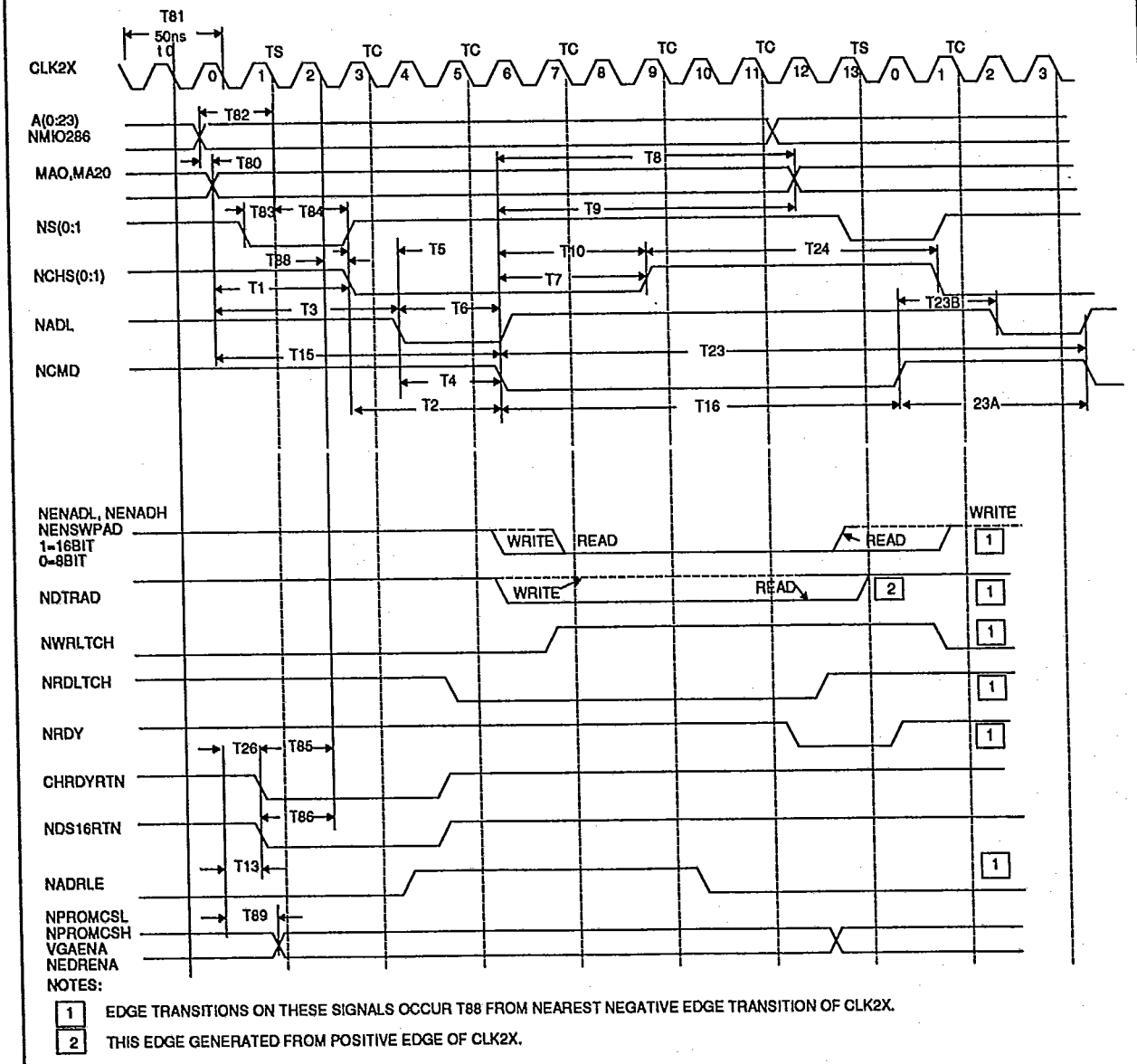


Figure 20. 20 MHZ CPU Cycle to Channel

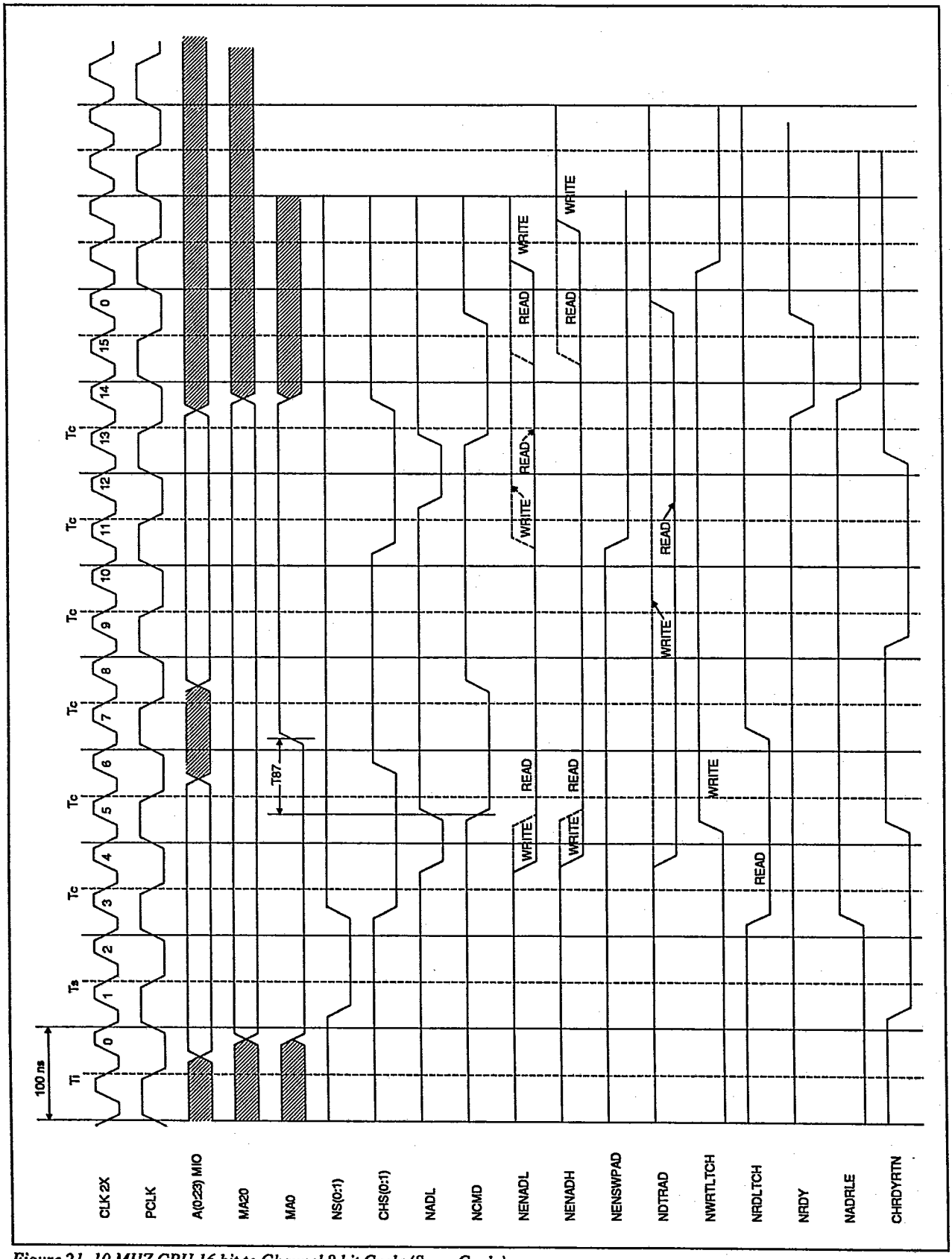


Figure 21. 10 MHZ CPU 16 bit to Channel 8 bit Cycle (Swap Cyale)

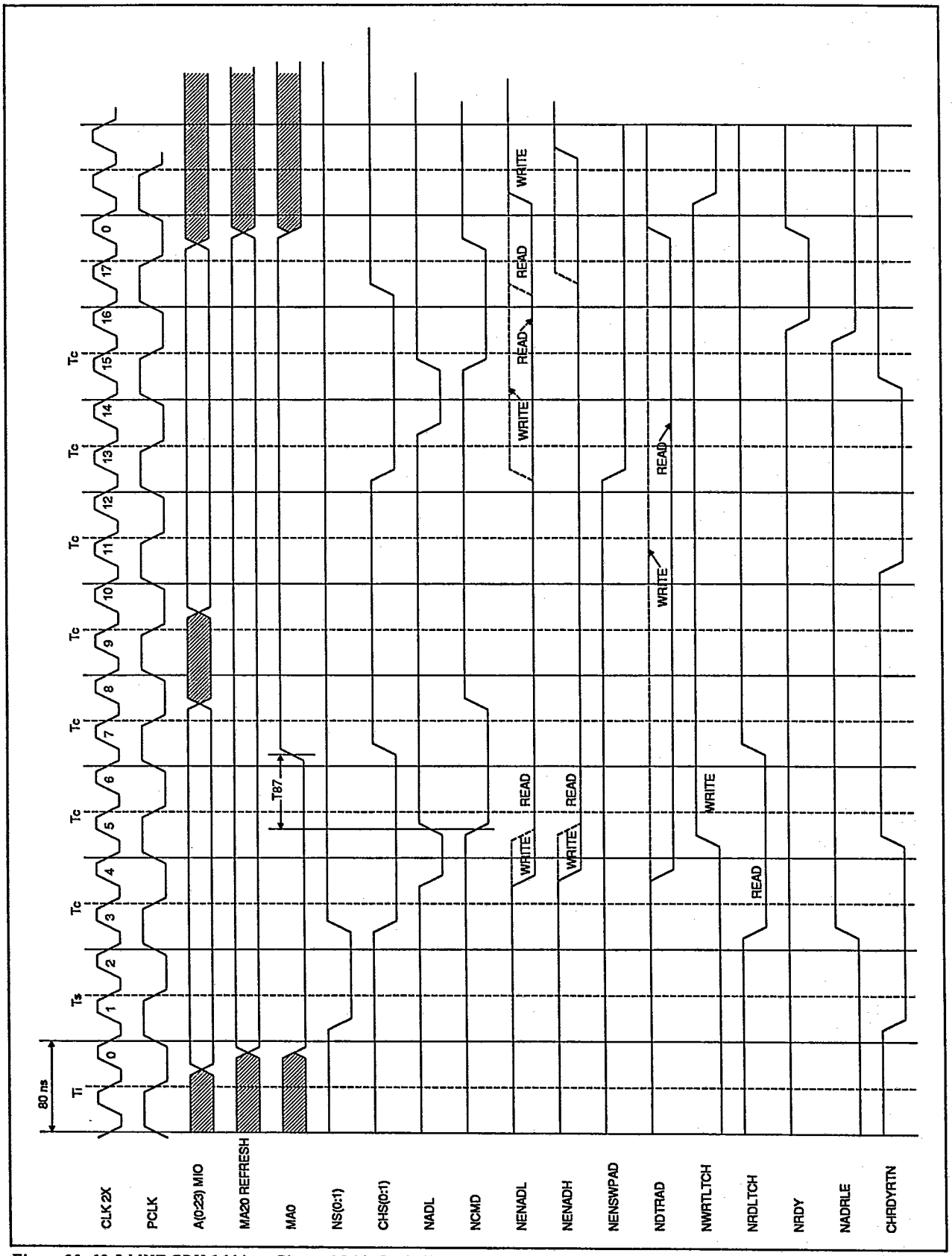


Figure 22. 12.5 MHZ CPU 16 bit to Channel 8 bit Cycle (Swap Cycle)

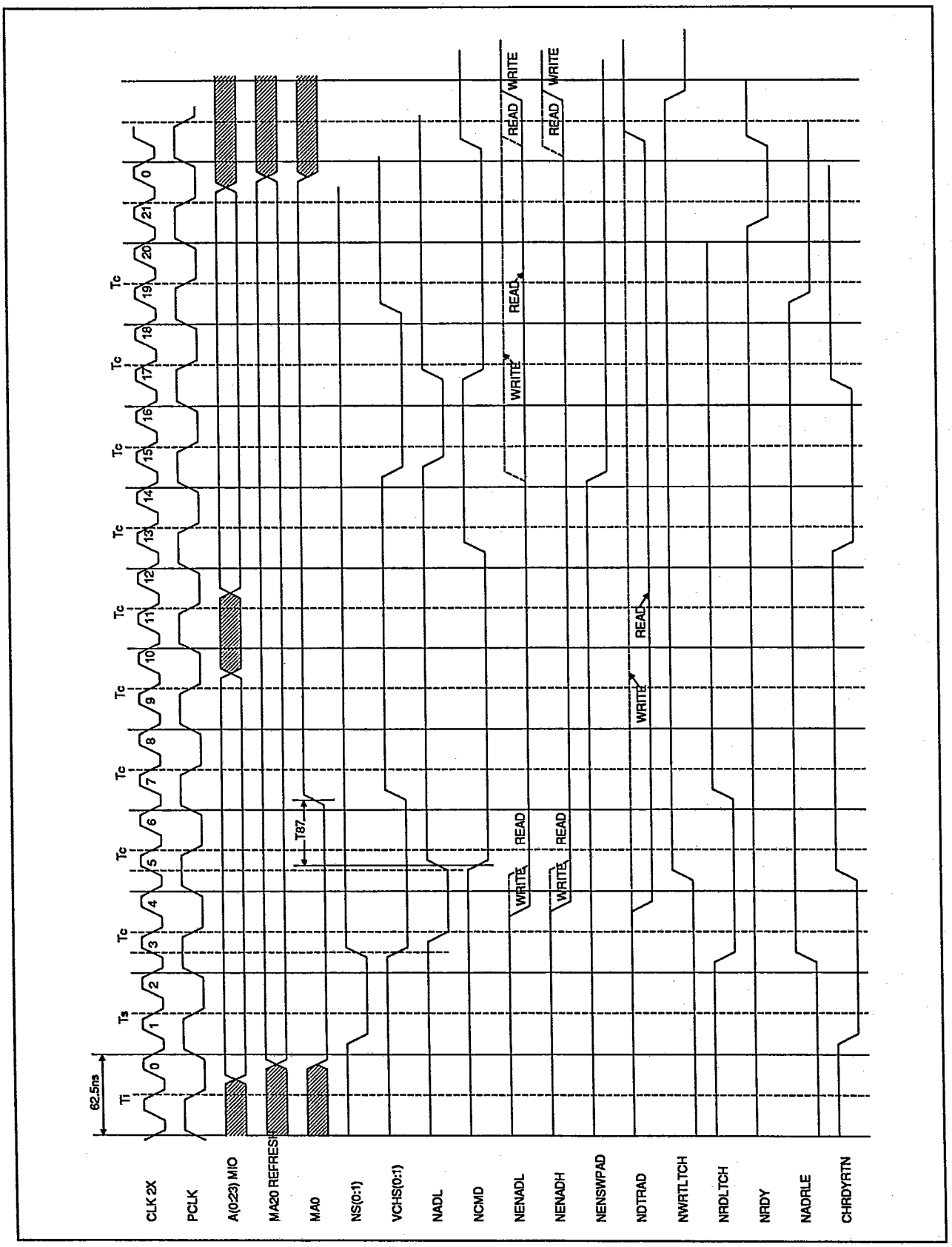


Figure 23. 16 MHZ CPU 16 bit to Channel 8 bit Cycle (Swap Cycle)

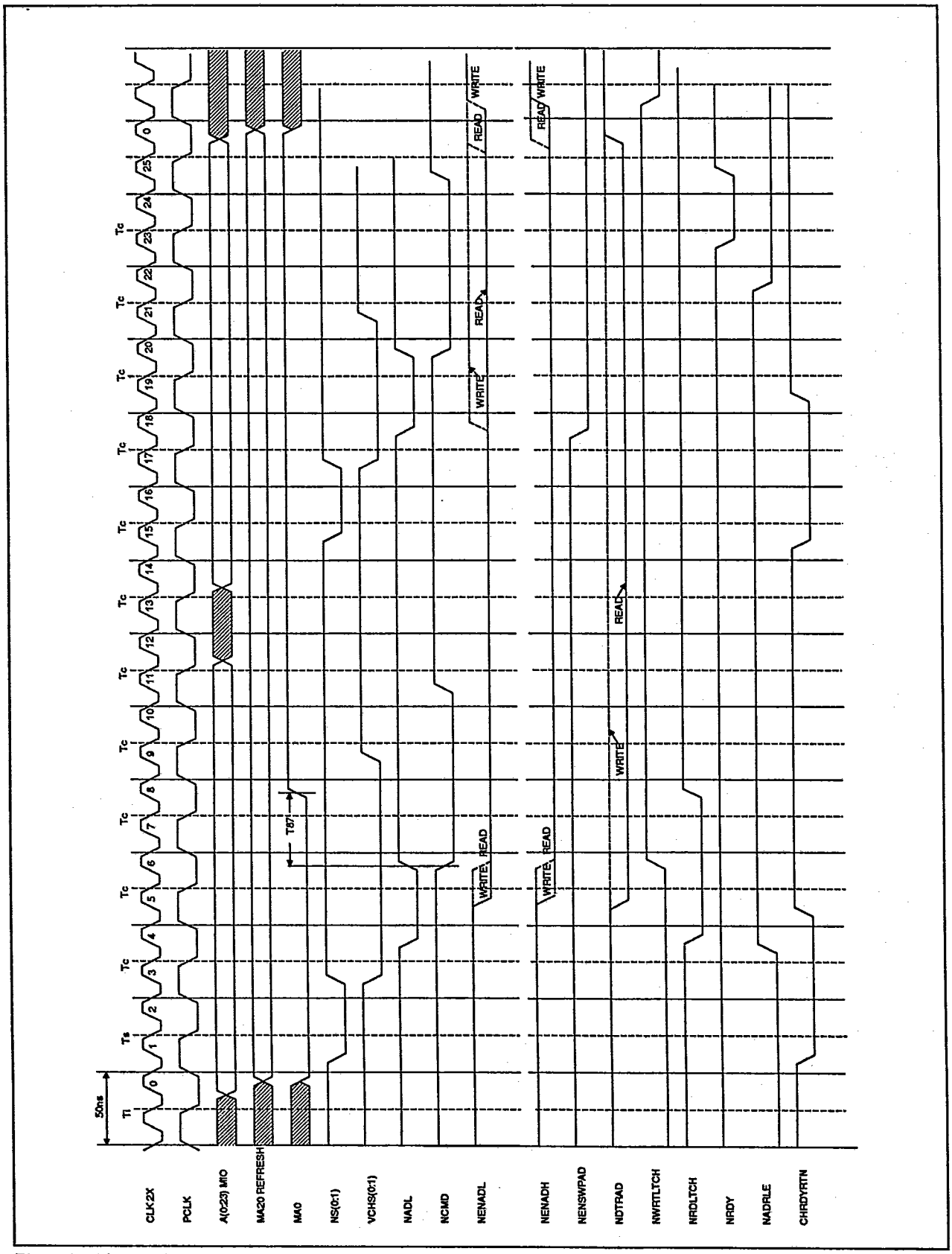


Figure 24. 20 MHZ CPU 16 bit to Channel 8 bit Cycle (Swap Cycle)

PARAM	DESCRIPTION	10 MHZ		12.5 MHZ		16 MHZ		20 MHZ		NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T1	A(23:0) output delay from CLK2X	1	35	1	32	1	29	1	24	—
T2	$\overline{S(1:0)}$ output delay from CLK2X	1	22	3	18	1	18	1	14	—
T3	$\overline{BHE}$ output delay from CLK2X	1	35	1	32	1	29	1	24	—
T4	Write D(15:0) delay from CLK2X	0	30	0	30	0	22	0	18	—
T5	Write D(15:0) hold from CLK2X	0	47	0	32	0	29	0	24	—
T6	Read D(15:0) setup to CLK2X	8	—	5	—	3	—	4	—	—
T7	Read D(15:0) hold from CLK2X	8	—	6	—	5	—	4	—	—

Table 21. DMA Cycles (in nsec)

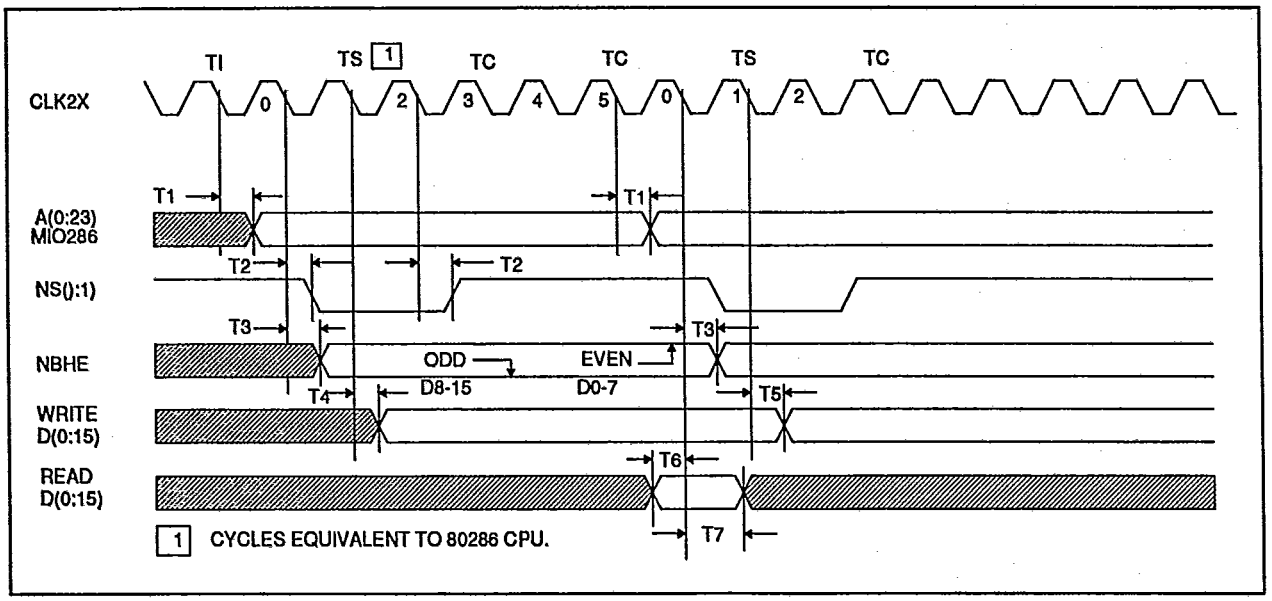


Figure 25. 10 MHZ DMA Cycle

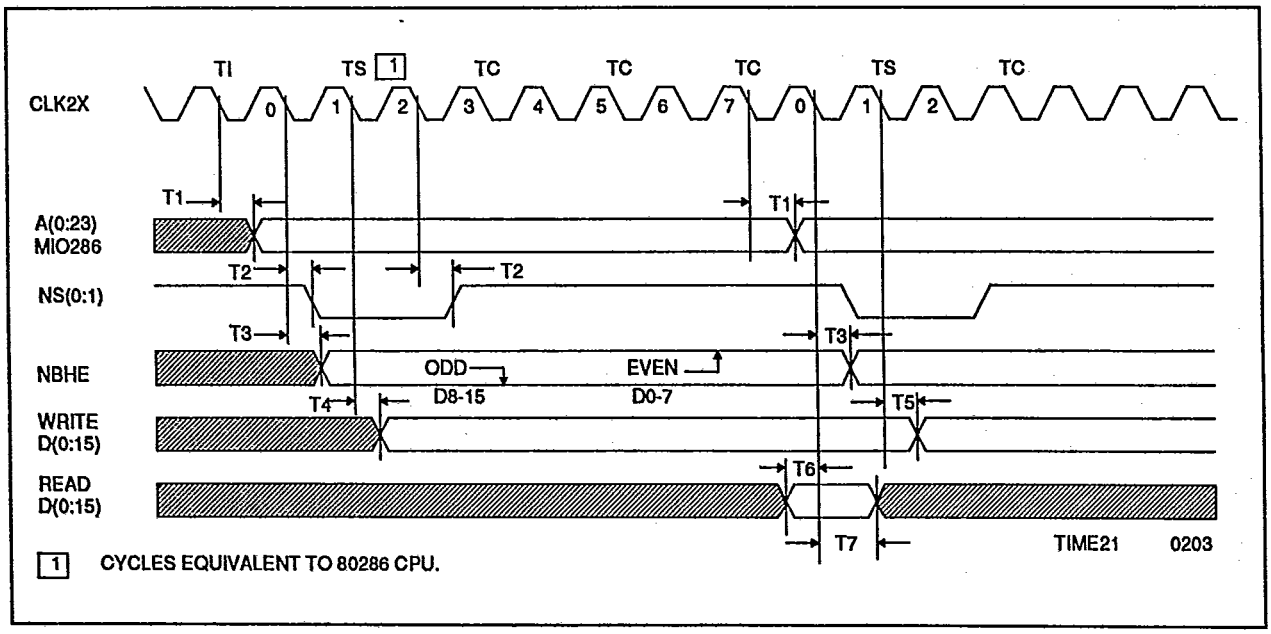


Figure 26. 12.5 MHZ DMA Cycle

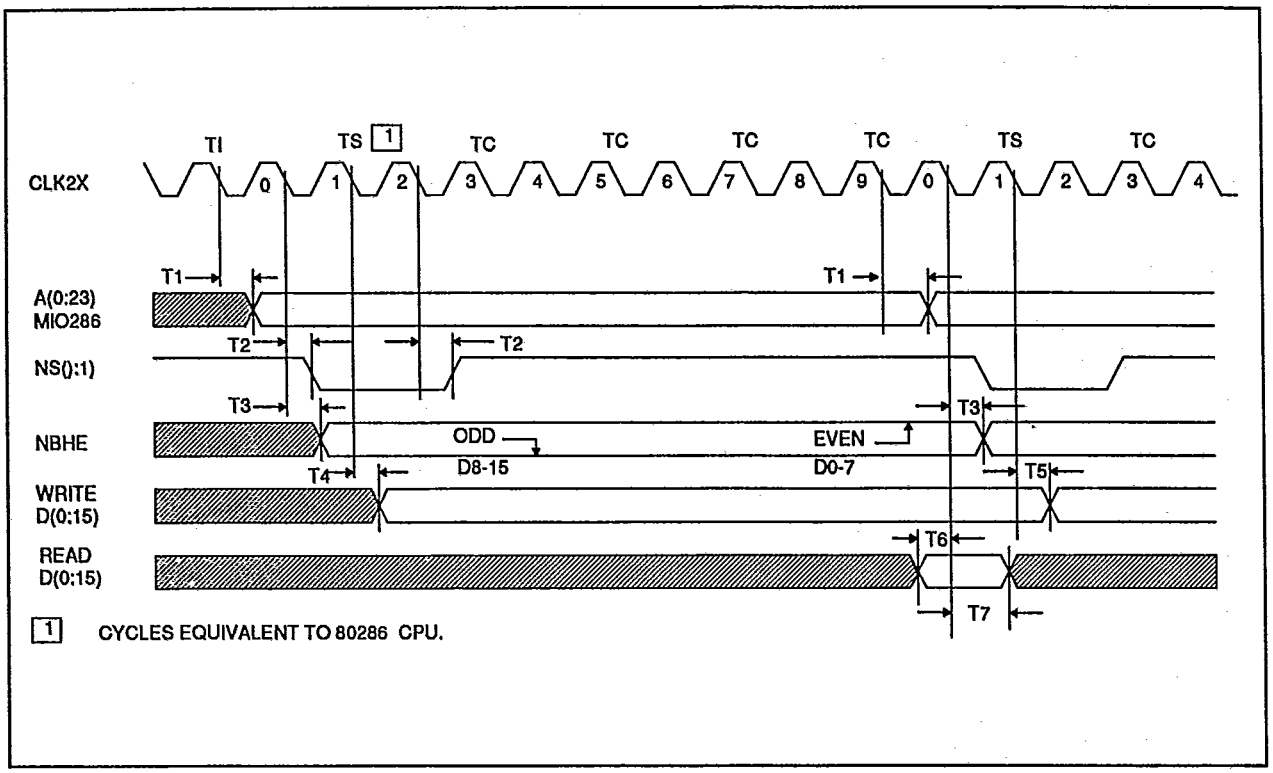


Figure 27. 16 MHZ DMA Cycle

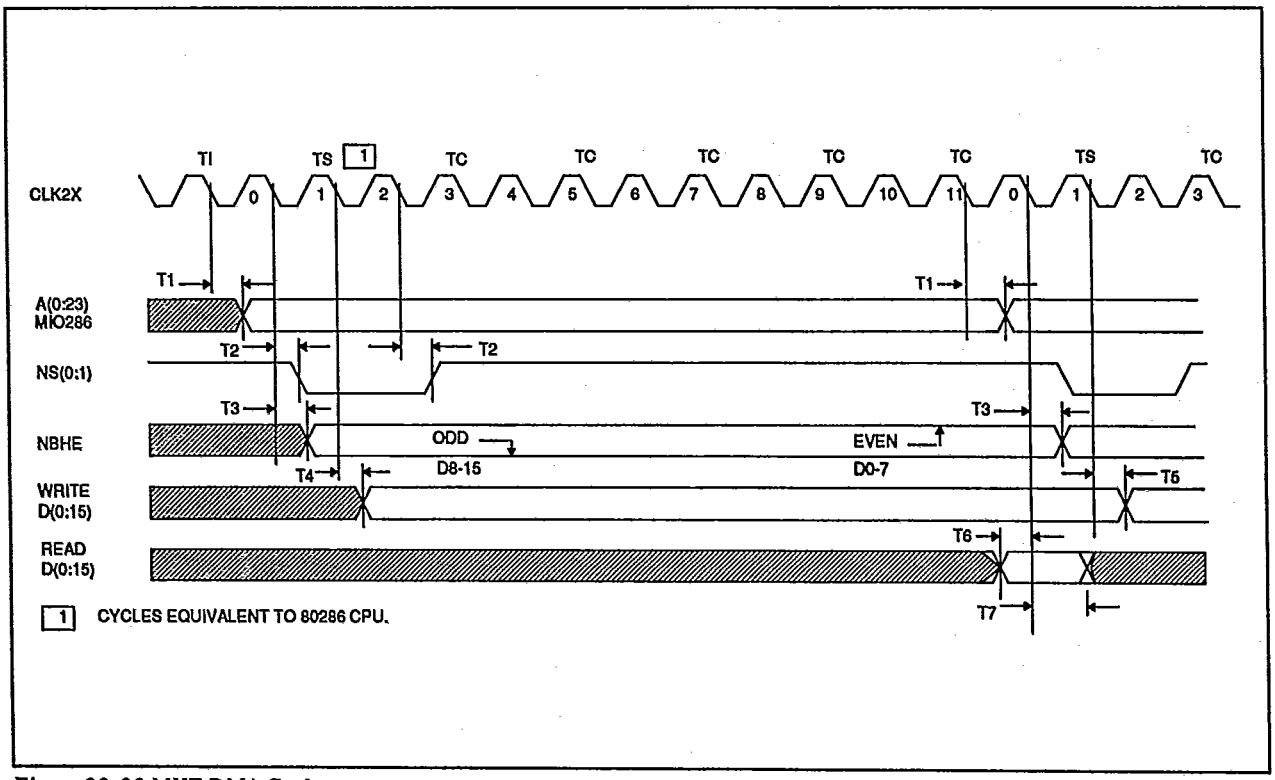


Figure 28. 20 MHZ DMA Cycle

PARAM	DESCRIPTION	10 MHZ		12.5 MHZ		16 MHZ		20 MHZ		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	NOTE
T1	CLK2X period	50	250	40	250	31.2	250	25	250	—
T2	CLK2X low	12	232	11	237	9	239	8	241	—
T3	CLK2X high	16	239	13	239	11	243	9	242	—
Tr	CLK2X rise time	—	8	—	8	—	8	—	8	—
Tf	CLK2X fall time	—	8	—	8	—	8	—	8	—
T4	PCLK delay from CLK2X	3	25	3	20	3	12	3	10	—
T5	RESET286 on/off setup to CLK2X	23	—	18	—	14	—	12	—	—
T6	RESET286 on/off hold to CLK2X	5	—	5	—	3	—	3	—	—
T7	Min 16 CLK2X cycles									

Table 22. Clock/Reset Cycles (in nsec)

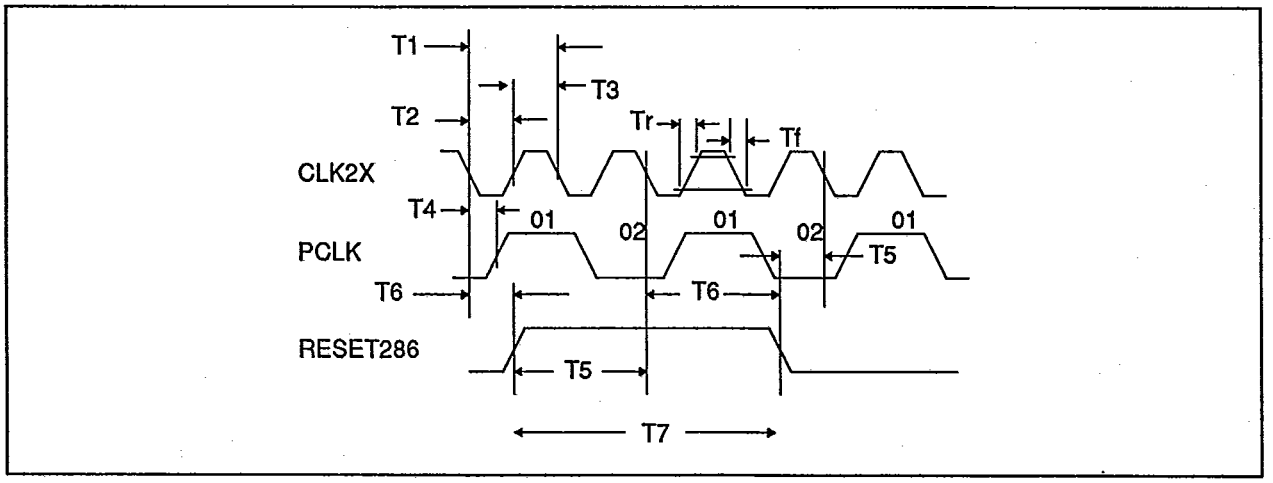


Figure 29. Clock/Reset Timing

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	CHRDYRTN on to $\overline{RDY}$ on	60	—	1

Table 23. Ready Cycle (in nsec)

Notes:
1. Applicable only to cycles extended beyond the standard cycle duration.

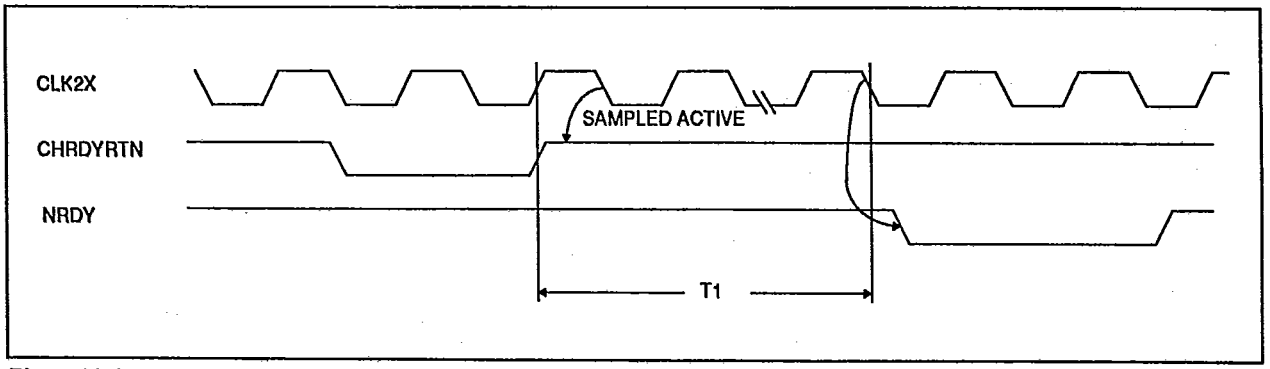


Figure 30. Ready Timing

PARAM	DESCRIPTION	MIN	MAX	NOTE
T40	$\overline{\text{PREEMPT}}$ on to EOT	0	7.8us	
T41	ARB/NGNT high from EOT	30	—	1
T42	$\overline{\text{PREEMPT}}$ off from ARB/$\overline{\text{GNT}}$ low	0	50	—
T43	$\overline{\text{BURST}}$ on from ARB/$\overline{\text{GNT}}$ low	—	50	—
T44	ARB/$\overline{\text{GNT}}$ high	300	—	—
T45	Driver turn-on delay from ARB/$\overline{\text{GNT}}$ high	0	50	—
T46	Driver turn-off delay from ARB/$\overline{\text{GNT}}$ high	0	50	—
T47	Driver turn-on delay from higher prority line	0	50	—
T48	ARB(3:0) stable before ARB/$\overline{\text{GNT}}$ low	10	—	—
T49	Tristate drivers from ARB/$\overline{\text{GNT}}$ high	—	50	—

Table 24. Arbitration Cycles (in nsec)

Notes:
1. EOT means End Of Transfer on the channel ($\overline{\text{CHS}}$(1:0), $\overline{\text{BURST}}$, $\overline{\text{CMD}}$ all off).

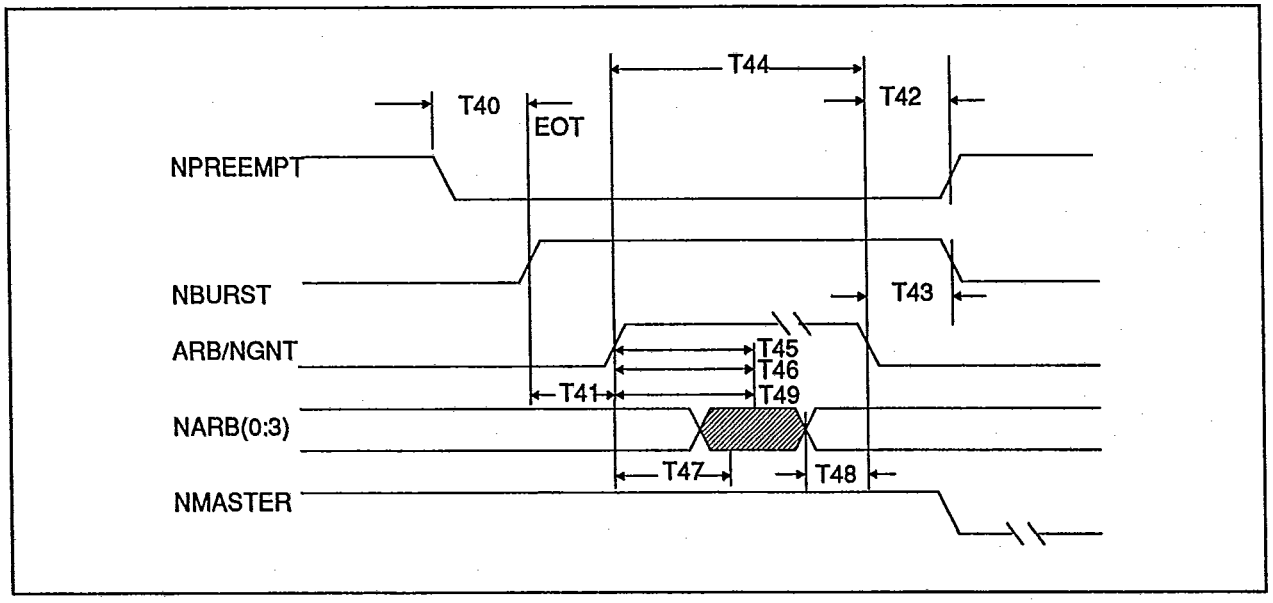


Figure 31. Arbitration Timing

PARAM	DESCRIPTION	10 MHZ MIN	10 MHZ MAX	12.5 MHZ MIN	12.5 MHZ MAX	16 MHZ MIN	16 MHZ MAX	20 MHZ MIN	20 MHZ MAX	NOTE
T1	$\overline{\text{LCLCYC}}$ setup to CLK2X	10	—	10	—	10	—	8	—	—
T2	$\overline{\text{LCLCYC}}$ hold from CLK2X	5	—	5	—	5	—	5	—	—
T3	$\overline{\text{DRAMRDY}}$ setup to CLK2X	55	—	52	—	45	—	40	—	—
T4	NDRAMRDY hold from CLK2X	5	—	5	—	5	—	5	—	—

Table 25. Local Cycles (in nsec)

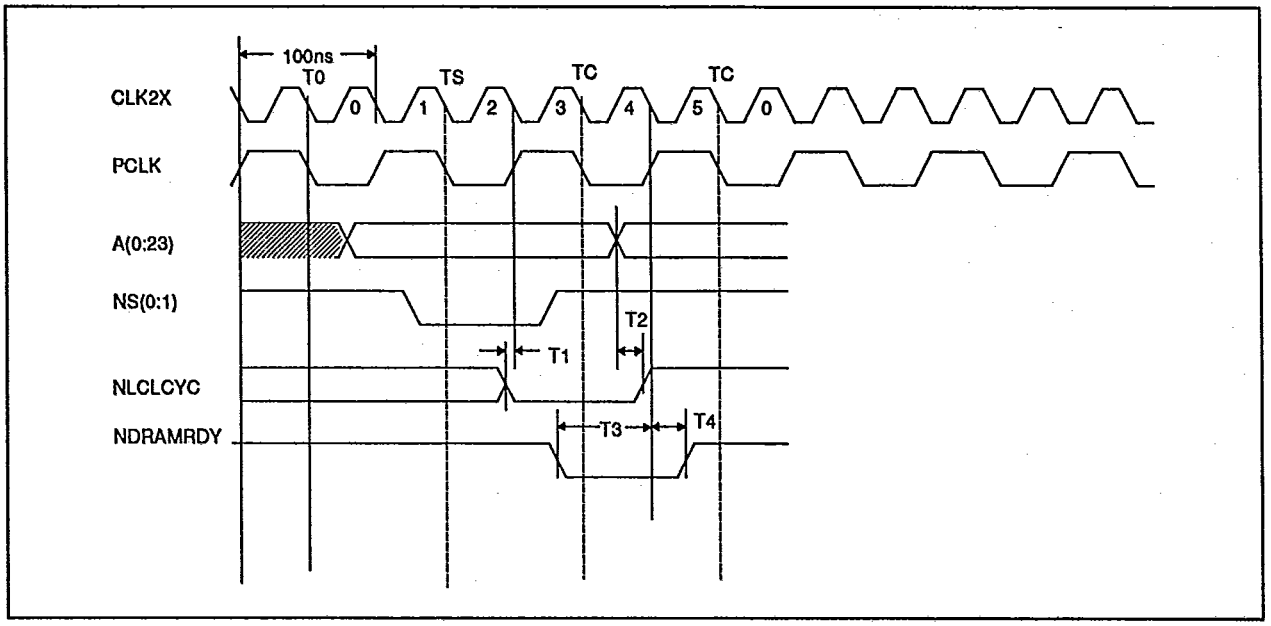


Figure 32. 10 MHZ Local Cycle

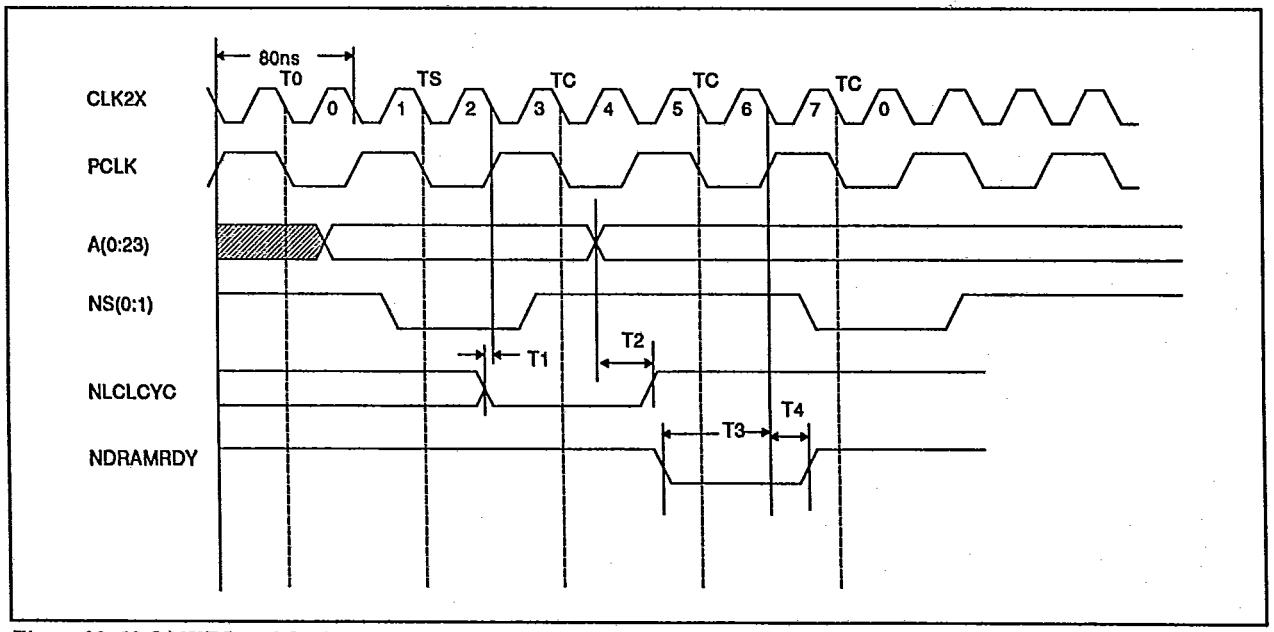


Figure 33. 12.5 MHZ Local Cycle

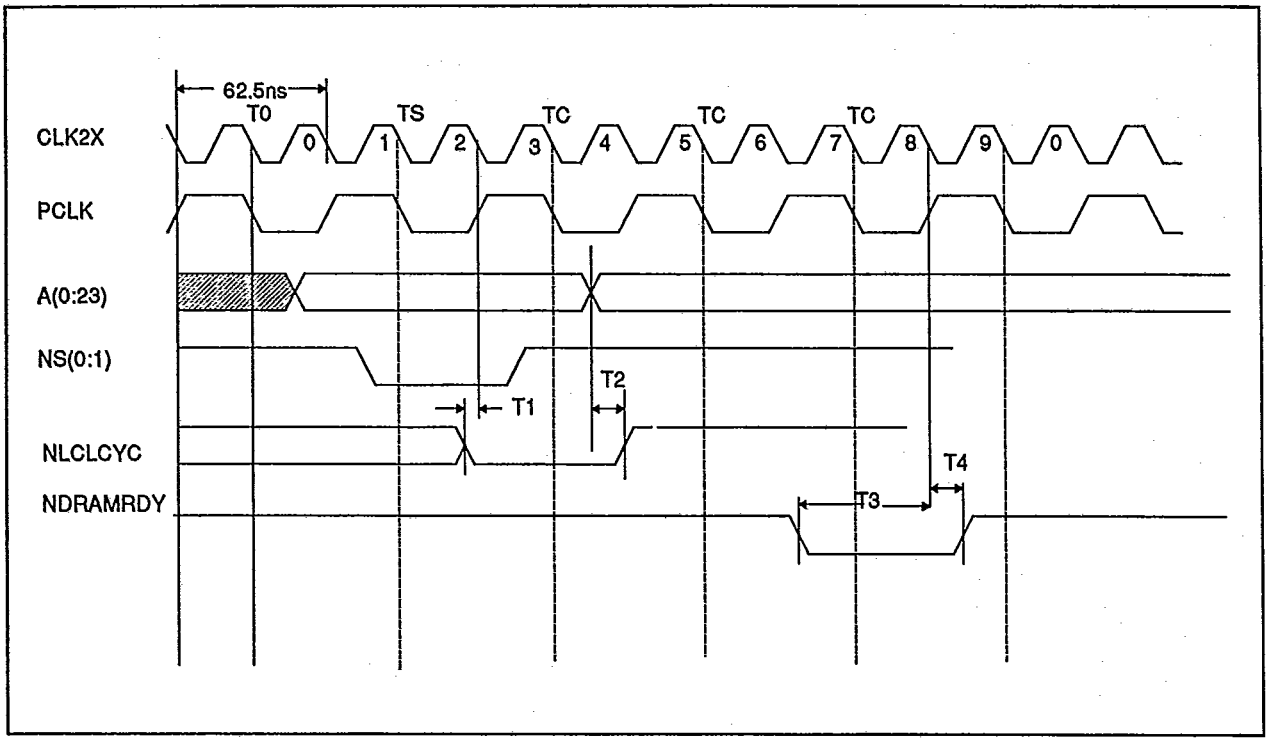


Figure 34. 16 MHZ Local Cycle

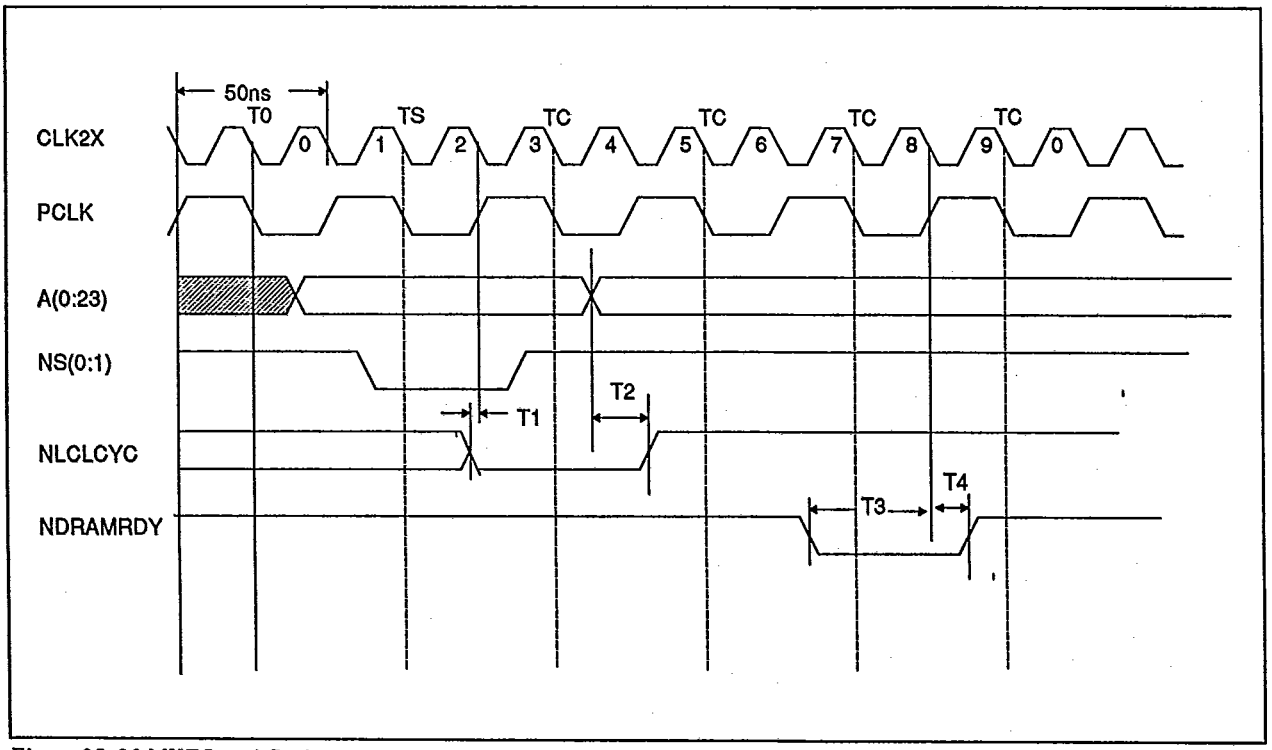


Figure 35. 20 MHZ Local Cycle

PARAM	DESCRIPTION	MIN	MAX	NOTE
T61	$\overline{\text{CDSETEN}}$ setup to $\overline{\text{ADL}}$ on	15	—	—
T62	$\overline{\text{CDSETEN}}$ hold from $\overline{\text{ADL}}$ off	25	—	—
T63	$\overline{\text{CDSETEN}}$ hold from $\overline{\text{CMD}}$ on	30	—	—
T65	CHRDYRTN off from $\overline{\text{CDSETN}}$ on	—	100	—

Table 26. Configuration Timing Cycles (in nsec)

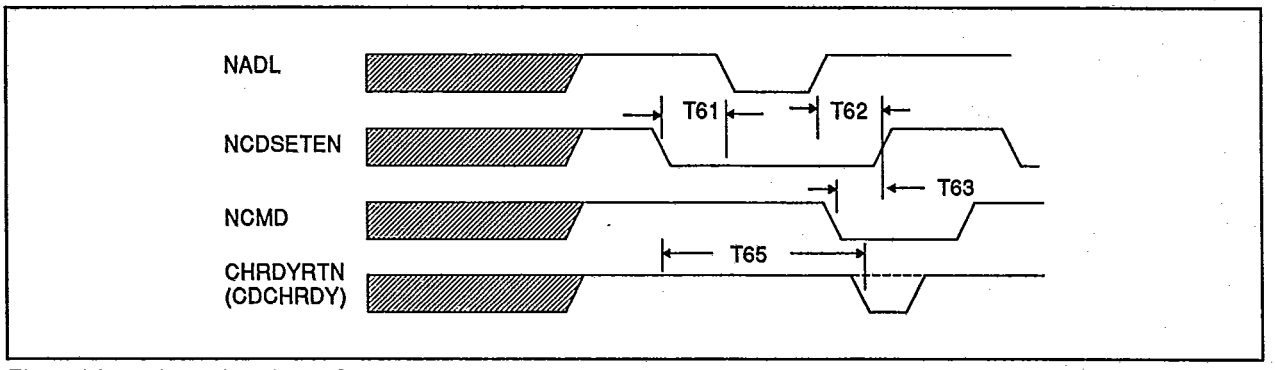


Figure 36. Configuration Timing Cycle

PARAM	DESCRIPTION	10 MHZ MIN	10 MHZ MAX	12.5 MHZ MIN	12.5 MHZ MAX	16 MHZ MIN	16 MHZ MAX	20 MHZ MIN	20 MHZ MAX	NOTE
T1	FDDRQ on to $\overline{\text{PREEMPT}}$ on	25	—	20	—	15.6	—	12.5	—	—
T2	ARB/$\overline{\text{GNT}}$ high to $\overline{\text{DACK}}$ off	0	—	0	—	0	—	0	—	—
T3	ARB/$\overline{\text{GNT}}$ high to HOLD on	0	—	0	—	0	—	0	—	—
T4	ARB/$\overline{\text{GNT}}$ high to HOLD off	0	—	0	—	0	—	0	—	—
T5	HOLDA on to ARB/$\overline{\text{GNT}}$ low	25	—	20	—	15.6	—	12.5	—	—

Table 27. Floppy Request Cycles (in nsec)

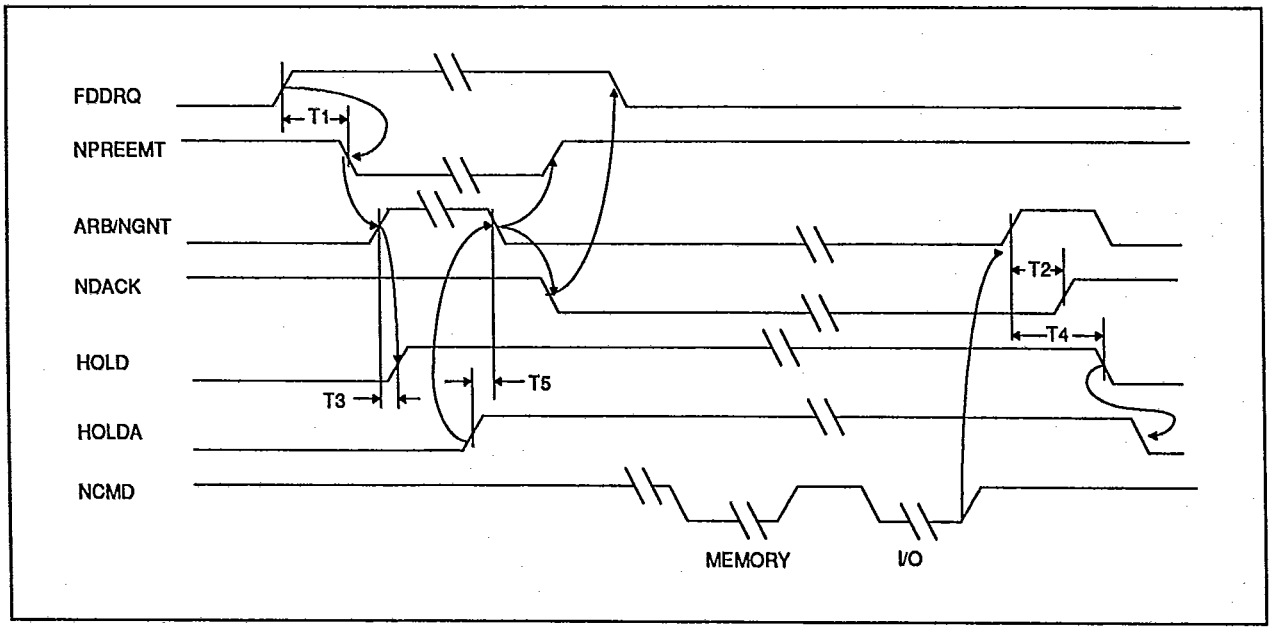


Figure 37. Floppy Request Cycle

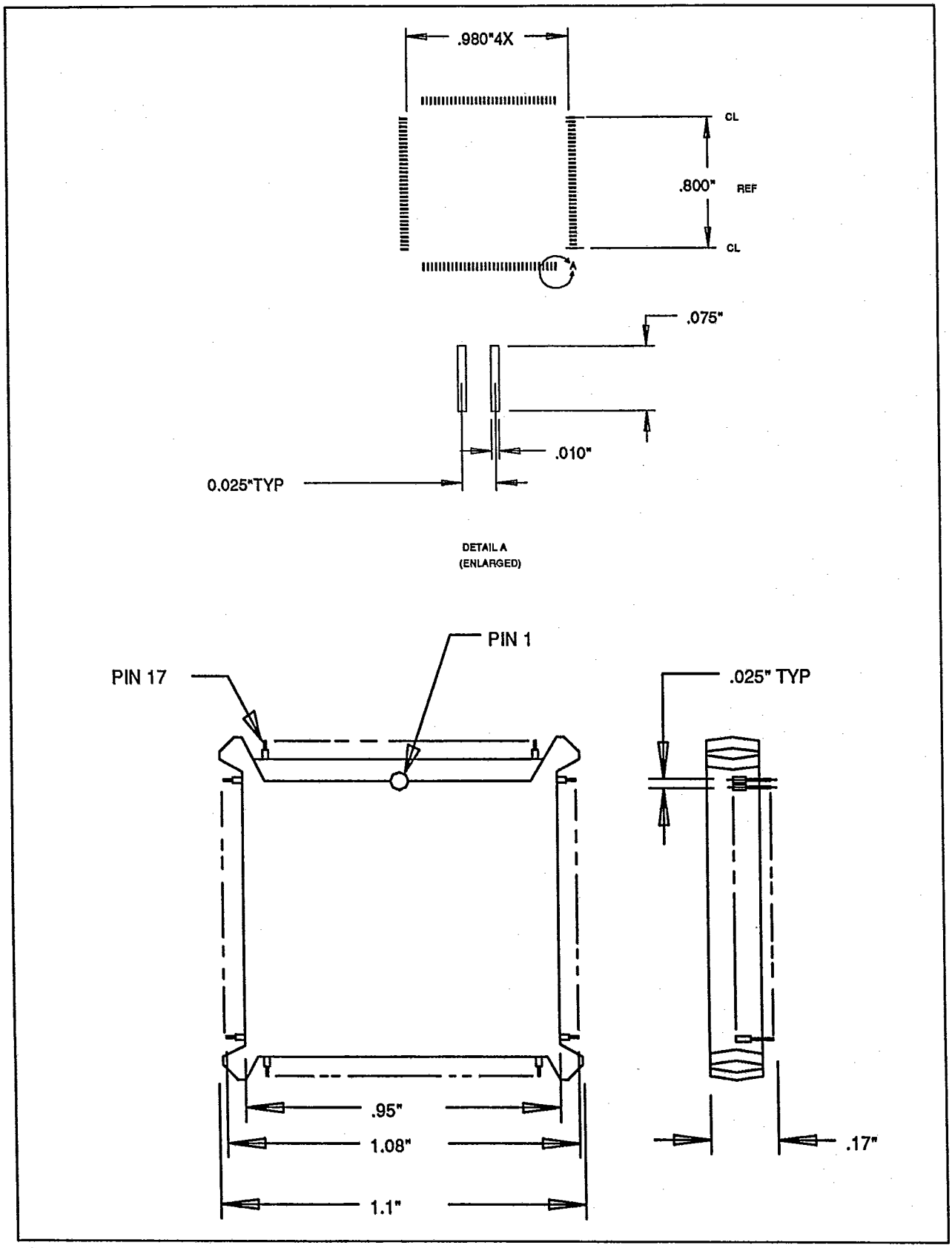
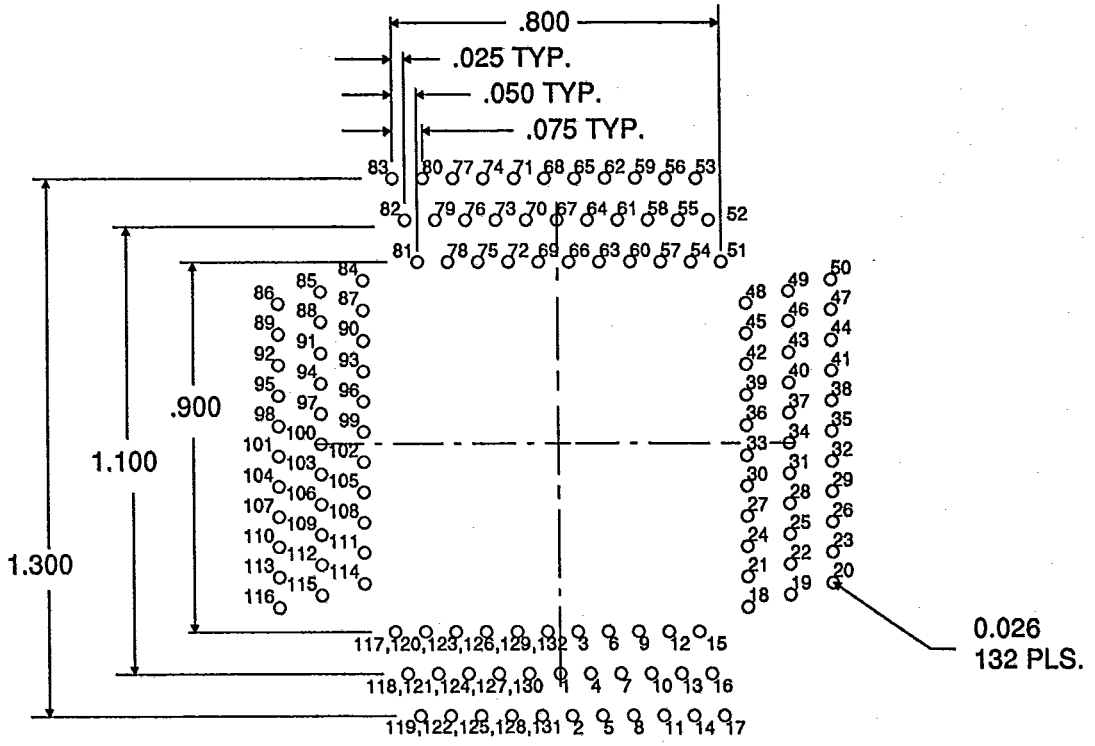


Figure 38. 132 JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-1

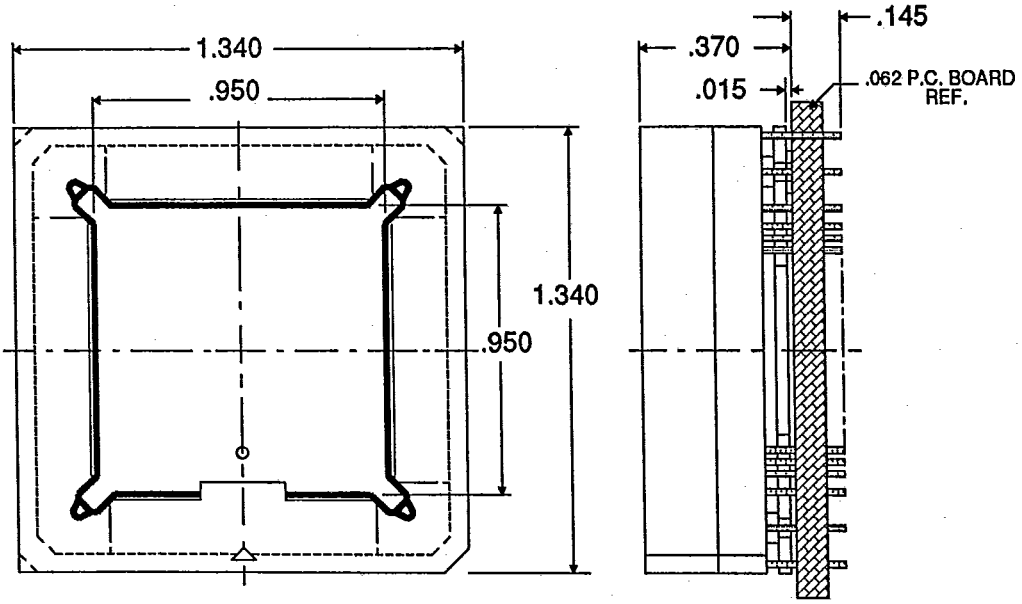


Figure 39. Socket Diagram