PRELIMINARY ENGINEERING SPECIFICATION

I/O MANAGER DEVICE

FE3040

			R. Chung	7/21/87
REV	ECO	DESCRIPTION	APPR	DATE

SIGNATURES	DATE	TITLE	WESTERN DIGITAL CORPORATION		
			CLASS CODE 96	BASE NUMBER 000610	REV X2.3
			SCALE:	SHEET 1 OF 32	

FE3040 DEVICE FEATURES

- generates chip selects for hard disk, floppy, 8042, 80287, and NMI
- generates programmable chip selects for four additional devices
- individually programmable wait state generation for I/O ports and system board memory
- maps main and EGA BIOS into one physical PROM
- generates fast IOCS16 for 16 bit I/O ports
- glitchless clock switching circuitry for processor and DMA
- bus-compatibility clock switching for I/O card accesses
- "Hot" reset generation for quick 80286 switch from protected to real mode
- Alternate Gate A20 generation
- 68 pin PLCC package

The FE3040 device is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with other Western Digital peripheral chips on a PC-AT compatible system board.

Chip count is reduced by integrating appropriate random logic and logic formerly implemented with PALs. Flexibility is retained by making the PAL type logic software programmable, so that characteristics may be changed by different versions of BIOS ROMs or through a BIOS ROM set-up program. Programmability also greatly reduces the number of jumpers on the system board.

A major function of the FE3040 is to generate chip select decodes for peripheral chips on the system board, for instance, the floppy controller, hard disk controller, serial, and parallel port chips. System operating speed may be optimized by tailoring the number of processor wait states to each individual peripheral device. An early generation of the IOCS16 signal is also provided, since this signal is in a critical timing path in high speed AT compatibles.

To reduce chip count and improve performance, particularly when an EGA graphics controller is placed on the system board, seperate blocks of ROM may be mapped into a single physical ROM. For instance, the EGA BIOS and standard BIOS may be placed into the same pair of ROM chips or into a single 16 bit wide ROM. Besides reducing chip count, EGA operating speed will be improved, since EGA BIOS will be accessed 16 bits at a time. To improve BIOS performance, ROM code may be copied into excess RAM, and the BIOS ROM mapped out and replaced by RAM 16K bytes at a time. (Excess RAM is the 384K left over after the lower 640K out of a 1 MB RAM is used).

Clock switching circuitry is included, which provides glitch free switching between two unrelated clocks under BIOS control. In addition, the processor clock output frequency may be programmed to be divided by two. The clocks will typically be at a frequency of 12 MHz to 24 MHz. In addition, the clock may be programmed to automatically divide by 2 when expansion cards are accessed, to provide compatibility with slow expansion cards while allowing full speed execution when accessing system board RAM, ROM, and I/O.

UPDATE HISTORY

REV X2.3: Added Alternate Gate A20 function to chip select C, enabled by control register FFF07.

Added RAM control register FFF58, providing ability to deselect on-board RAM between 256K-640K or 512K-640K.

Changed default wait states for on-board ROM from 2 wait states to 1 wait state; register FFF50.

Pin 33 has been renamed IORDY from IORDY-. It's function has not been redefined.

The CSFP-, CSF, CSHD-, CSPRGA-, CSPRGB-, CSPRGC-, CSPRGD-, CS8042-, CS287-, CSNMI-, GTCK-, and D3-D0 pins will have a 2 mA drive capability rather than 4 mA.

REV X2.2: Changed output drive specification from 4 mA to 2 mA for certain output pins. See sheet 29, DC Operating Characteristics.

Changed timing parameters T4-T7, T14, T16, T20, T24, T26. Changed T8 and T9 reference from PCLK to PROCLK. Added timing parameter T10. See sheet 30, AC Operating Characteristics.

Redefined SEL field in the Processor Clock Select Register, FFF62.

REV X2.1: The EPROM/RAM swap control registers FFF53-FFF56 bit definitions have changed. The function specified by control bit 0 has been swapped with control bit 3, and bit 2 swapped with bit 1.

REV X2.0: Added bus cycle clock switching, controlled by register FFF62.

Added "Hot" reset function to chip select D. Added control register at FFF07.

The port control registers FFF08, FFF10, FFF18, and FFF20 will generate up to 6 wait states rather than 8. The zero wait state line will no longer be asserted for the 1 or 2 wait state case.

The CSFP0- and CSFPC- floppy controller select pins have been combined into a single pin, CSF.

REV X2.0: (continued)
Pin 29 was spare, now is A0.
Pin 2 was ADDR0, now is MI0.
Pin 48 was SYSCLK, now is S1-.
Pin 46 was DMACLK, now is PROCLK.
Pin 54 was CSPRGD-, now is SYSCLK.
Pin 58 was CSFPC-, now is CSPRGD-.

REV X1.3: External RAM and I/O Wait State Control register FFF61 deleted. The External RAM and I/O Wait State Control has been simplified and integrated into register FFF50.

Address pin A0, pin 29, has been deleted and is now a spare pin.

The default DMA clock rate has been changed from the selected clock divided by 8 to the selected clock divided by 2.

REV X1.2: Floppy and hard disk chip selects are now fixed in function. The three floppy and one hard disk chip select pins had alternate functions as programmable chip selects E, F, G, and H.

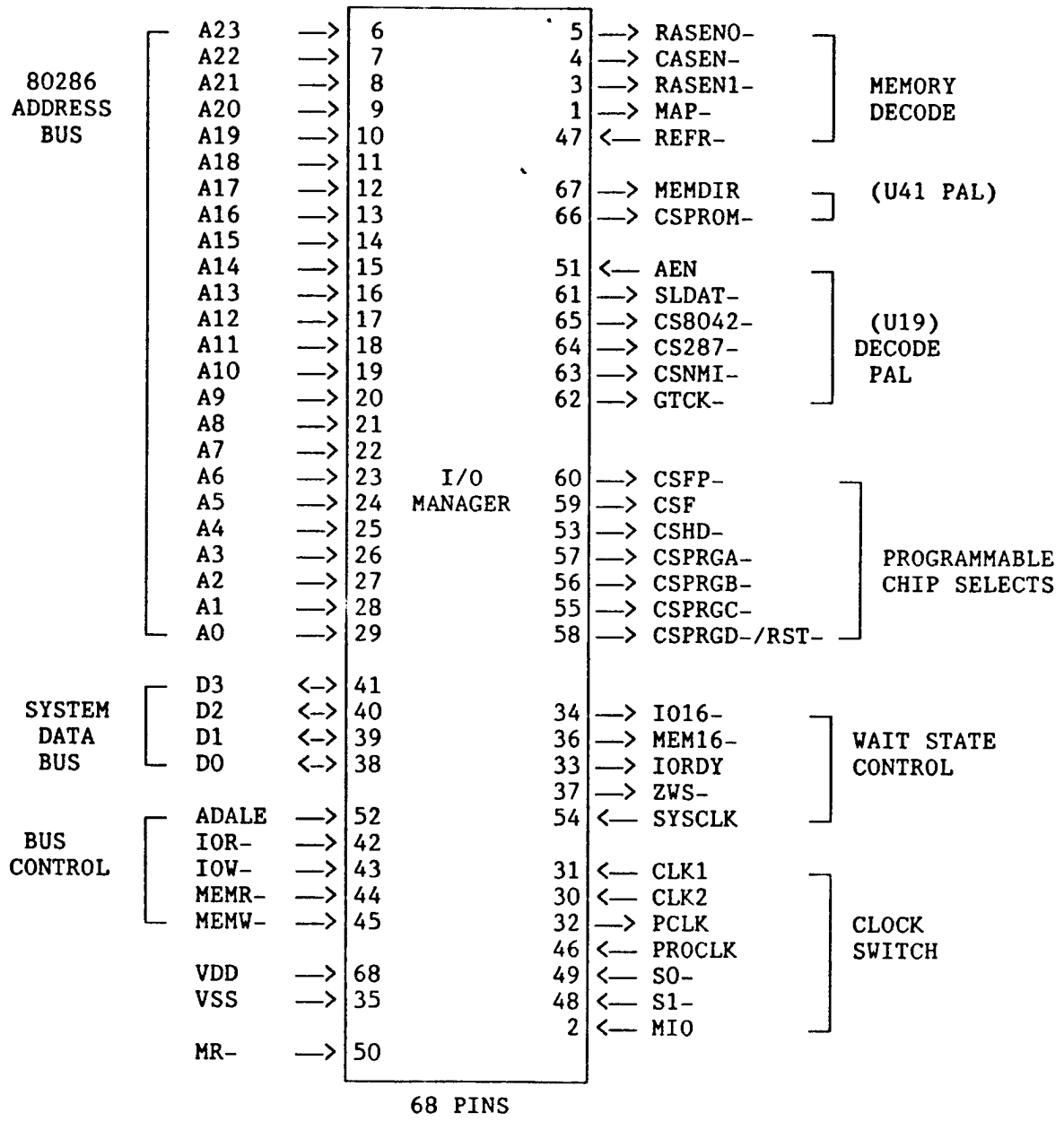
Programmable ports A, B, C, and D now have four address range choices, rather than eight. Also, the A8 address bit may be masked, rather than the A9 address bit. The Port I/O Address registers are reset to all zeroes by master reset, rather than preset to all ones.

The External I/O Wait State Control register (FFF48) has been deleted. The external I/O wait state control has been simplified and is now coded in register FFF61, the External RAM Wait State Control register.

The Clock1/Clock2 SELect bit in the DMA Clock Select register (FFF63) has been moved from bit 0 to bit 1.

REV X1.1: Added version number register (FFF01).

PINOUT



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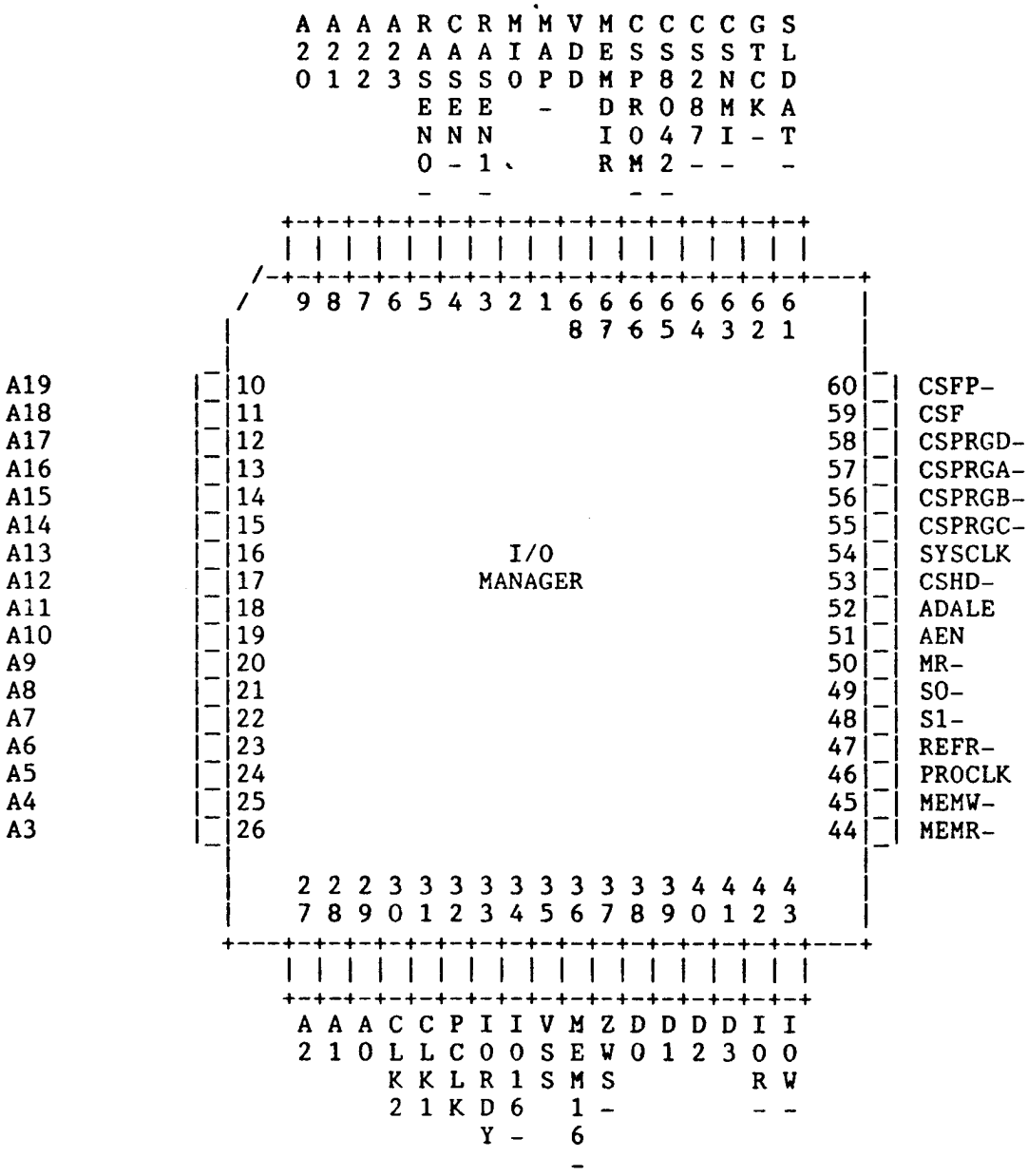

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80286 INTERFACE

This interface port connects with the 80286 address lines and the 80286 bus status lines. By connecting directly to the 80286 and by duplicating a portion of the 82288 bus controller logic, early determination of memory or I/O accesses may be made, as well as whether the access will be 8 bits or 16 bits.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
6	A23	I	80286 ADDRESS LINE
7	A22	I	. . .
8	A21	I	. . .
9	A20	I	. . .
10	A19	I	. . .
11	A18	I	. . .
12	A17	I	. . .
13	A16	I	. . .
14	A15	I	. . .
15	A14	I	. . .
16	A13	I	. . .
17	A12	I	. . .
18	A11	I	. . .
19	A10	I	. . .
20	A9	I	. . .
21	A8	I	. . .
22	A7	I	. . .
23	A6	I	. . .
24	A5	I	. . .
25	A4	I	. . .
26	A3	I	. . .
27	A2	I	. . .
28	A1	I	. . .
29	A0	I	80286 ADDRESS LINE

DATA BUS INTERFACE AND BUS CONTROL

The data bus port is 4 bits wide, which should connect to the EDATA data bus. The upper 4 bits should be ignored when reading the control registers.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
41	D3	I/O	CONTROL REGISTER DATA LINE
40	D2	I/O	...
39	D1	I/O	...
38	D0	I/O	CONTROL REGISTER DATA LINE
42	IOR-	I	SYSTEM I/O READ COMMAND SIGNAL
43	IOW-	I	SYSTEM I/O WRITE COMMAND SIGNAL
44	MEMR-	I	SYSTEM MEMORY READ COMMAND SIGNAL
45	MEMW-	I	SYSTEM MEMORY WRITE COMMAND SIGNAL
52	ADALE	I	SYSTEM ADDRESS LATCH ENABLE SIGNAL 'OR'ED WITH ADSTB
54	SYSCLK	I	SYSTEM CLOCK (PROCESSOR CLOCK DIVIDED BY TWO)

I/O CHIP SELECT CONTROL

This logic section generates chip selects for standard system board functions such as the 8042 keyboard controller, 80287 math coprocessor, floppy controller, and hard disk controller. It also generates chip selects for up to 4 additional I/O ports which may have programmable addresses and wait state characteristics.

PIN NUMBER	PIN NAME	I/O	FUNCTION
57	CSPRGA-	O	PROGRAMMABLE CHIP SELECT A
56	CSPRGB-	O	PROGRAMMABLE CHIP SELECT B
55	CSPRGC-	O	PROGRAMMABLE CHIP SELECT C
58	CSPRGD-	O	PROGRAMMABLE CHIP SELECT D OR HOT RESET OUTPUT
59	CSF	O	FLOPPY DISK CONTROLLER OPERATION OR CONFIGURATION REGISTER SELECT
60	CSFP-	O	FLOPPY DISK CHIP SELECT
53	CSHD-	O	HARD DISK CONTROLLER CHIP SELECT
65	CS8042-	O	8042 KEYBOARD CONTROLLER SELECT
64	CS287-	O	80287 ARITHMETIC COPROCESSOR SELECT
63	CSNMI-	O	NMI LOGIC
62	GTCK-	O	ENABLE MEMORY PARITY AND I/O CHECK. GATED EXTERNALLY WITH I/O READ AND I/O WRITE.
34	IO16-	O	EARLY IOCS16 SIGNAL FOR SYSTEM BOARD I/O PORTS
33	IORDY	O	PROGRAMMABLE WAIT STATE LINE FOR SYSTEM BOARD I/O PORTS
37	ZWS-	O	ZERO WAIT STATE LINE
36	MEM16-	O	16 BIT MEMORY SIGNAL
61	SLDAT-	O	DIRECTION OF DATA TRANCEIVER - DATA TO EDATA BUS
51	AEN	I	SYSTEM AEN SIGNAL

The IORDY pin will normally be at a high state. It will go low when generating wait states. This pin should be AND'ed with the bus signal IOCHRDY.

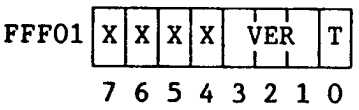
The following table lists the data work size, I/O addresses, and chip selects generated for each variable port type.

The Port A, B, C, and D addresses are fully programmable, with the choice of either using nine I/O addresses for decode, or masking the A8 address bit (for instance, for decoding dual serial ports). The LSB (A0) address is always ignored. The lower 2, 3, or 4 bits of the address may also be ignored so that 2, 4, 8, or 16 bytes may be allocated for the port.

All FE3040 control registers are accessed by first writing eight times to address FFF00 (in an area allocated for ROM BIOS). Any memory access outside of the ROM BIOS address space, either data access or instruction fetch, will abort the unlocking process. Once unlocked, memory accesses outside of the ROM BIOS area may be made without affecting the unlocked state. When unlocked, the address space from FFF01 to FFFFE becomes register controls for the FE3040 device. The controls are locked again by reading location FFFFF.

A Version Number register provides information on the version of the I/O Manager chip. It also contains a bit which toggles between '0' and '1' which provides indication that the register set has been unlocked.

VERSION NUMBER



T : toggles between 0 and 1 with every read access
of the Version Number register.

V : 001 when T=0
: 001 when T=1

System board devices may be located on the EDATA bus rather than on the I/O expansion slot DATA bus. The SLDAT- signal which controls the DATA to EDATA bus direction is affected by the two port location registers. This option is available for peripheral devices which cannot directly drive the high current I/O slot DATA bus. Note, however, that DMA transfers cannot be made to devices on the EDATA bus.

The SLDAT- signal is active (low) when IOR- is active and address bits A8 and A9 are low, or the PORTS ABCD location register indicates that an addressed port is on the EDATA bus.

PORTS ABCD LOCATION REGISTER

	7	6	5	4	3	2	1	0
FFF06	X	X	X	X	A	B	C	D

IF A=0 THEN THE PORT A DEVICE IS ON THE DATA BUS.
IF A=1 THEN THE PORT A DEVICE IS ON THE EDATA BUS.
THE SAME CODING IS USED FOR PORTS B,C, AND D.

THE PORT LOCATION REGISTER IS CLEARED BY A MASTER RESET.

The CSPRGC- pin (Port C) may be redefined to provide an alternate gate A20 function which is generated faster than the gate A20 signal provided by the 8042 keyboard controller. When defined as an alternate gate A20 signal, writing a '1' to bit 1 of I/O port 092 will cause the CSPRGC- pin to go to a low state.

The CSPRGD- pin (Port D) may be redefined to provide a "hot" reset function, to provide a fast switch from protected mode to real mode, by setting the "H" bit of the System Control Port register. Writing a '1' to bit 0 of I/O port 092 will generate an active low reset pulse 32 PCLKs wide, 128 PCLKs after writing to port 092. A reset pulse will be generated only when the bit is changed from a 0 to a 1.

SYSTEM CONTROL PORT SELECT

	7	6	5	4	3	2	1	0
FFF07	X	X	X	X	0	0	A	H

IF A=1 THEN THE CSPRGC- PIN BECOMES THE ALTERNATE GATE A20 FUNCTION.
IF H=1 THEN THE CSPRGD- PIN BECOMES THE HOT RESET FUNCTION.
THIS REGISTER IS CLEARED BY A MASTER RESET.

PORT CONTROL REGISTERS

X	X	X	X	WS		P	BW
7	6	5	4	3	2	1	0

WS	BW=0 8 BIT PORT	BW=1 16 BIT PORT
00	2 W.S.	1 W.S.
01	4 W.S.	1 W.S.
10	6 W.S.	2 W.S.
11	6 W.S.	2 W.S.

PORT	PORT CONTROL REGISTER ADDRESS
A	FFF08
B	FFF10
C	FFF18
D	FFF20

FOR PORTS A, B, C, AND D, IF P=0
THEN THE OUTPUT IS DISABLED (ALWAYS HIGH).

THE PORT CONTROL REGISTERS ARE CLEARED BY A MASTER RESET.

The A, B, C, and D port chip selects are enabled with the P bit. If the P bit is 0, then the port chip select bit will always be at an inactive (high) state. These ports are disabled after master reset.

PORT ADDRESS MASK REGISTERS

X	X	X	X	0	U	LMASK	
7	6	5	4	3	2	1	0

LMASK	ADDRESS BITS COMPARED
00	A9 A8 A7 A6 A5 A4 A3 A2 A1 X
01	A9 A8 A7 A6 A5 A4 A3 A2 X X
10	A9 A8 A7 A6 A5 A4 A3 X X X
11	A9 A8 A7 A6 A5 A4 X X X X

U = 0 : INCLUDE A8 IN ADDRESS COMPARISON

LMASK	ADDRESS BITS COMPARED
00	A9 X A7 A6 A5 A4 A3 A2 A1 X
01	A9 X A7 A6 A5 A4 A3 A2 X X
10	A9 X A7 A6 A5 A4 A3 X X X
11	A9 X A7 A6 A5 A4 X X X X

U = 1 : IGNORE A8 IN ADDRESS COMPARISON

THE PORT ADDRESS MASK REGISTER IS CLEARED BY A MASTER RESET.

PORT	PORT CONTROL REGISTER ADDRESS
A	FFF09
B	FFF11
C	FFF19
D	FFF21

PORT ADDR - LOWER MSB

7	6	5	4	3	2	1	0
X	X	X	X	X	X	A9	A8

PORT ADDR - UPPER LSB

7	6	5	4	3	2	1	0
X	X	X	X	A7	A6	A5	A4

PORT ADDR - LOWER LSB

7	6	5	4	3	2	1	0
X	X	X	X	A3	A2	A1	0

PORT	PORT I/O ADDRESS REGISTERS A9-A8	A7-A4	A3-A0
A	FFF0A	FFF0B	FFF0C
B	FFF12	FFF13	FFF14
C	FFF1A	FFF1B	FFF1C
D	FFF22	FFF23	FFF24

The four Port A I/O Address registers are set to all zeroes by a master reset.

The following table lists the I/O addresses and chip selects generated for each fixed port type. The number of wait states for the fixed ports is set by the External I/O Wait State Control register. The IOCS16- signal is generated only on accesses to the hard disk controller data port. The chip selects are not gated with IOR- or IOW-. The floppy controller operations register select and configuration register select may be generated from the CSF and CSHD- pins. The operations register is being accessed when CSF is active (high) and CSHD- is inactive (high). The configuration register is being accessed when both CSF and CSHD- are active.

PORT	BIT SIZE	I/O ADDRESS	ACTIVE PIN	FUNCTION
FLOPPY	8	3F2 372	CSF	FDC OPERATION SELECT. 3F2 IS PRIMARY ADDRESS, 372 IS SECONDARY ADDRESS.
	8	3F4-3F5 374-375	CSFP-	3F4-3F5 ARE PRIMARY ADDRESSES, 374-375 ARE SECONDARY.
	8	3F6 376	CSHD-	HARD DISK CONTROLLER CHIP SELECT. 3F6 IS PRIMARY ADDRESS, 376 IS SECONDARY.
	8	3F7 377	CSF CSHD-	CSHD- AND CSF PINS WILL BE ASSERTED. 3F7 IS PRIMARY ADDRESS, 377 IS SECONDARY.
80287	8	0E0-0FF	CS287-	80287 CHIP SELECT.
8042	8	060-06E (EVEN)	CS8042-	8042 CHIP SELECT.
NMI LOGIC	8	070-07E (EVEN)	CSNMI-	NMI LOGIC SELECT.
PARITY CK	8	061-06F (ODD)	GTCK-	PARITY CHECK SELECT AND PORT B CLOCK. EXTERNAL LOGIC MUST SEPERATE THE SIGNALS.
HARD DISK	16	1F0 170	CSHD-	HDC CHIP SELECT - DATA PORT ACCESS. 1F0 IS PRIMARY ADDRESS, 170 IS SECONDARY.
	8	1F1-1F7 171-177	CSHD-	HDC CHIP SELECT - TASK FILE. 1F1-1F7 ARE PRIMARY ADDRESSES, 171-177 SECONDARY.

PRIMARY/SECONDARY PORT FUNCTION SELECT

FFF49

X	X	X	X	DH	DF	H	F
7	6	5	4	3	2	1	0

DH=0 : Enable CSHD- output
DH=1 : Disable CSHD- output (always high)

DF=0 : Enable CSFP- and CSF outputs
DF=1 : Disable CSFP- and CSF outputs (always high)

H=0 : Primary hard disk port address
H=1 : Secondary hard disk port address

F=0 : Primary floppy disk port address
F=1 : Secondary floppy disk port address

DH, DF, H, and F are cleared to '0' by master reset

MEMORY DECODE CONTROL

TWo RAS enable pins are available for controlling two 16 bit wide banks of system board RAM. A single CAS enable is provided; external circuitry must gate CASEN- with A0 to enable the low or high bytes of memory. During a refresh cycle, both RAS enables will be active (ignoring the RAM configuration register FFF57) and CASEN will stay inactive. The MEMDIR signal is a logic '1' only when MEMR- is active and RASEN0-, RASEN1-, or CSPROM- is active.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
5	RASEN0-	O	RAS ENABLE FOR DRAM MEMORY BANK 0
3	RASEN1-	O	RAS ENABLE FOR DRAM MEMORY BANK 1
4	CASEN-	O	CAS ENABLE FOR DRAM MEMORY BANKS 0 AND 1
1	MAP-	O	RAM MAP SIGNAL
47	REFR-	I	MEMORY REFRESH SIGNAL
67	MEMDIR	O	CONTROLS DIRECTION PIN OF 245 MEMORY LATCH, HIGH WHEN READING ON-BOARD RAM OR ROM.
66	CSPROM-	O	BIOS PROM SELECT

PORT	BIT SIZE	MEMORY ADDRESS	ACTIVE PIN	FUNCTION
BIOS PROM	16	0F0000-0FFFFF	CSPROM-	BIOS PROM ALSO SELECTED WHEN ADDRESS IS FF0Q00 TO FFFFFF.
	16	0C0000-0C3FFF OR 0C0000-0C7FFF	CSPROM-MAP	IF EGA BIOS MAPPING IS ENABLED, THEN BOTH CSPROM AND MAP PINS WILL BE ACTIVE WHEN 0C0000-0C3FFF, THE EGA BIOS AREA, OR 0C0000-0C7FFF, AN EXTENDED EGA BIOS AREA, IS ADDRESSED.

SYSTEM BOARD PROM AND EXTERNAL WAIT STATE CONTROL REGISTER

FFF50	X	X	X	X	RWS	0	XWS
	7	6	5	4	3	2	1	0

RWS	
00*	1 W.S.
01	2 W.S.
10	4 W.S.
11	6 W.S.

* : DEFAULT AFTER MASTER RESET

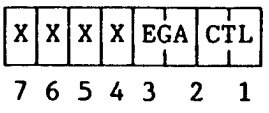
XWS=0* : 1 W.S FOR 16 BIT I/O, 4 W.S. FOR 8 BIT I/O
1 : 6 W.S. FOR 8 OR 16 BIT I/O

The system BIOS address space is from F0000 to FFFFF. If the EGA BIOS is to be mapped, then the BIOS ROM chip select is also active when the region from C0000 to C3FFF is addressed, along with the MAP signal pin. The BIOS PROM size and number of wait states will then apply to both regions F0000-FFFFF and C0000-C3FFF.

The ROM memory is assumed to be 16 bits wide. If the ROM memory is actually implemented with 8 bit wide ROM chips, then the MEMCS16 output must be externally gated with the CSPROM signal. The RWS field specifies the number of wait states for the system ROM.

The XWS bit is used to program the minimum number of wait states for external RAM and external I/O. The FE3000 wait state generator will generate 1 wait state for 16 bit devices and 4 wait states for 8 bit devices. If the XWS bit is '0', then the FE3000 will generate the wait states. If the XWS bit is '1', then the FE3040 will extend the wait states to six for both 8 bit and 16 bit external devices.

EPROM/RAM MAP CONTROL REGISTER



EGA = 00 : PROM chip select will be active when address is 0F0000-0FFFFF or FF0000-FFFFFF. Default case after master reset.

01 : Map 0C0000-0C3FFF (16K EGA ROM area) to 0F8000-0FBFFF so both can be placed in same physical rom. When 0C0000-0C3FFF is addressed then both PROM Chip Select and MAP pins will be active.

10 : Map 0C0000-0C7FFF (32K EGA ROM area) to 0F8000-0FFFFF so both can be placed in same physical rom. When 0C0000-0C7FFF is addressed then both PROM Chip Select and MAP pins will be active.

CTL = 00 : No EPROM/RAM swapping, Main BIOS and EGA BIOS are in seperate ROMs. Default case after master reset.

01 : Swap RAM for EPROM in C0000-FFFFF, in 16K pages (requires minimum 1 MByte RAM). Ram swapping will override EGA mapping.

10 : No EPROM/RAM swapping, map 384K (A0000-FFFFF) of RAM to extended memory. This mode is supported for three memory configurations: 1) bank 0 = 256K by 16, bank 1 = 256K by 16
2) bank 0 = 256K by 16, bank 1 = 1M by 16
3) bank 0 = 1M by 1, no bank 1

11 : Swap RAM for EPROM in E0000-FFFFF, enableable in 16K pages (requires minimum 1 Mbyte RAM). Map 256K (A0000-DFFFF) of RAM to extended memory. This mode is supported for three memory configurations: 1) bank 0 = 256K by 16, bank 1 = 256K by 16
2) bank 0 = 256K by 16, bank 1 = 1M by 16
3) bank 0 = 1M by 1, no bank 1

Write protection is accomplished by not asserting CASEN when MEMW is active.

EPROM/RAM MAP WRITE CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF52	X	X	X	X	WPF	WPE	WPD	WPC

WPF=1 : WRITE PROTECT FFFFF-F0000
WPE=1 : WRITE PROTECT EFFFF-E0000
WPD=1 : WRITE PROTECT DFFFF-D0000
WPC=1 : WRITE PROTECT CFFFF-C0000

EPROM/RAM SWAP CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF53	X	X	X	X	ENF0	ENF4	ENF8	ENFC

ENFC = 1 : SWAP FC000-FFFFF
ENF8 = 1 : SWAP F8000-FBFFF
ENF4 = 1 : SWAP F4000-F7FFF
ENF0 = 1 : SWAP F0000-F3FFF

EPROM/RAM SWAP CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF54	X	X	X	X	ENE0	ENE4	ENE8	ENEC

ENEC = 1 : SWAP EC000-EFFFF
ENE8 = 1 : SWAP E8000-EBFFF
ENE4 = 1 : SWAP E4000-E7FFF
ENE0 = 1 : SWAP E0000-E3FFF

EPROM/RAM SWAP CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF55	X	X	X	X	END0	END4	END8	ENDC

ENDC = 1 : SWAP DC000-DFFFF
END8 = 1 : SWAP D8000-DBFFF
END4 = 1 : SWAP D4000-D7FFF
END0 = 1 : SWAP D0000-D3FFF

EPROM/RAM SWAP CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF56	X	X	X	X	ENC0	ENC4	ENC8	ENCC

ENCC = 1 : SWAP CC000-CFFFF
ENC8 = 1 : SWAP C8000-CBFFF
ENC4 = 1 : SWAP C4000-C7FFF
ENC0 = 1 : SWAP C0000-C3FFF

THESE REGISTERS ARE CLEARED BY MASTER RESET.

RAM CONFIGURATIQN REG

FFF57

X	X	X	X	BNK 1 SZ	BNK 0 SZ

BANK 0 SZ=00 : NO RAM PRESENT
SZ=01 : RESERVED
SZ=10 : 256K DRAM
SZ=11 : 1MBIT DRAM

BANK 1 SZ=00 : NO RAM PRESENT
SZ=01 : 64K DRAM
SZ=10 : 256K DRAM
SZ=11 : 1MBIT DRAM

AFTER MASTER RESET, BANK1 SZ=00, BANK0 SZ=10
NOTE: 64K DRAM IS SUPPORTED ONLY IN BANK 1 AND ONLY WHEN BANK 0 SZ=10.

RAM CONTROL REG

FFF58

X	X	X	X	SD	XC	UL	EE

SD=1: DISABLE MEM FROM 512K TO 640K
XC=1: EXCHANGE RASENO AND RASEN1
UL=1: MEMORY CONTROL SIGNALS UNLATCHED
EE=1: DISABLE MEM FROM 256K TO 640K

* REGISTER CLEARED BY MASTER RESET.

When the SD bit is set, on-board memory will be disabled when addressed between 512K and 640K, to support certain SDLC controller cards. When the EE bit is set, on-board memory will be disabled when addressed between 256K and 640K, to support EEMS expanded memory boards. When the XC bit is set, RASEN0 and RASEN1 signals are exchanged, to simplify the determination of RAM type in bank 1 at boot-up time. When the UL bit is set, the RASENO-, RASEN1-, CASEN-, MEM16-, MEMDIR-, CSPROM-, and MAP- pins are unlatched, rather than being latched by ADALE.

ON-BOARD RAM
WAIT STATE CONTROL REG

FFF60

X	X	X	X	BNK 1 WS	BNK 0 WS

BANK 0 WS = 00 : 0 WAIT STATES
= 01 : 1 WAIT STATE *
= 10 : 2 WAIT STATES
= 11 : 3 WAIT STATES

BANK 1 WS = 00 : 0 WAIT STATES
= 01 : 1 WAIT STATE *
= 10 : 2 WAIT STATES
= 11 : 3 WAIT STATES

* : DEFAULT AFTER MASTER RESET

CLOCK SWITCH CONTROL

This logic section provides glitchless clock switching between two clocks under CPU control. CLK1 is immediately selected for the processor clock, without glitch suppression, when the reset pin is asserted. CLK1 divided by 2 is immediately selected for the DMA clock, without glitch suppression, when the reset pin is asserted.

If CLK2 has not gone high since master reset, clock switching from CLK1 to CLK2 is inhibited. If the CLK2 pin is not used, it should be tied to ground.

Two bus compatibility clock switch modes are available when the SEL field is 01 or 11. In both modes, on board memory is accessed at the full clock speed, while DMA transfers are made at half speed. In the medium speed mode, external I/O devices (devices on the I/O bus) are accessed at half the clock rate, while on board I/O devices are accessed at full speed. External memory is also accessed at full speed.
In the slowest speed mode, all external memory and all I/O, both on board and external, is accessed at half speed.

For board test purposes, the PCLK pin may be tristated. Refer to the next section for a description of the test mode.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
50	MR-	I	MASTER RESET
31	CLK1	I	INPUT CLOCK 1
30	CLK2	I	INPUT CLOCK 2
32	PCLK	O	PROCESSOR CLOCK, SWITCHED BETWEEN CLK1 AND CLK2

PROCESSOR CLOCK SELECT REGISTER

FFF62

VAR = 00*: NORMAL CLOCK
01 : MEDIUM SPEED BUS COMPATIBLE CLOCK SWITCH MODE
10 : SLOWEST SPEED BUS COMPATIBLE CLOCK SWITCH MODE
11 : RESERVED

SEL = 00*: SELECT CLK1 DIVIDED BY 2 FOR PCLK
= 10 : SELECT CLK1 FOR PCLK
= 01 : SELECT CLK2 DIVIDED BY 2 FOR PCLK
= 11 : SELECT CLK2 FOR PCLK

* : DEFAULT AFTER MASTER RESET

CLASS CODE	BASE NUMBER	REV
96	000610	X2.3
	SHEET 24 OF 32	

TEST MODE

All output pins will become tristated if MEMR- and MEMW- are active simultaneously while MR- is active. The outputs will remain tristated if MR- is brought inactive while MEMR- and MEMW- are both active. The outputs will become active drivers again when MR- is brought low without both MEMR- and MEMW- active. This "all output tristate" mode allows an in-circuit board tester to drive the FE3040 output pins.

The PCLK pin will become tristated if IOR- and MEMW- are active simultaneously while MR- is active. The PCLK pin will remain tristated if MR- is brought inactive while IOR- and MEMW- are both active. The PCLK pin will become an active driver again when MR- is brought low without both IOR- and MEMW- active.

REGISTER MAP

	3	2	1	0	
FFF00	X	X	X	X	UNLOCK REGISTER
FFF01	VER			T	VERSION NUMBER
FFF06	A	B	C	D	PORTS ABCD LOCATION
FFF07	0	0	0	H	SYSTEM CONTROL PORT SELECT
FFF08	WS		P	BW	PORT A CONTROL
FFF09	0	U	LMASK		PORT A ADDRESS MASK
FFF0A	X	X	A9	A8	PORT A ADDR - LOWER MSB
FFF0B	A7	A6	A5	A4	PORT A ADDR - UPPER LSB
FFF0C	A3	A2	A1	0	PORT A ADDR - LOWER LSB
FFF10	WS		P	BW	PORT B CONTROL
FFF11	0	U	LMASK		PORT B ADDRESS MASK
FFF12	X	X	A9	A8	PORT B ADDR - LOWER MSB
FFF13	A7	A6	A5	A4	PORT B ADDR - UPPER LSB
FFF14	A3	A2	A1	0	PORT B ADDR - LOWER LSB

FFF18	WS | P | BW	PORT C CONTROL
FFF19	O | U | LMASK	PORT C ADDRESS MASK
FFF1A	X | X | A9 | A8	PORT C ADDR - LOWER MSB
FFF1B	A7 | A6 | A5 | A4	PORT C ADDR - UPPER LSB
FFF1C	A3 | A2 | A1 | A0	PORT C ADDR - LOWER LSB
FFF20	WS | P | BW	PORT D CONTROL
FFF21	O | U | LMASK	PORT D ADDRESS MASK
FFF22	X | X | A9 | A8	PORT D ADDR - LOWER MSB
FFF23	A7 | A6 | A5 | A4	PORT D ADDR - UPPER LSB
FFF24	A3 | A2 | A1 | A0	PORT D ADDR - LOWER LSB
FFF49	DH | DF | H | F	PRIMARY/SECONDARY PORT FUNCTION SELECT
FFF50	RWS | 0 | XWS	SYSTEM BOARD PROM AND EXTERNAL WAIT STATE CONTROL
FFF51	EGA | CTL	EPROM/RAM MAP CONTROL
FFF52	WPF | WPE | WPD | WPC	EPROM/RAM MAP WRITE CONTROL

FFF53	ENFC	ENF8	ENF4	ENF0	EPROM/RAM SWAP CONTROL
FFF54	ENEC	ENE8	ENE4	ENE0	EPROM/RAM SWAP CONTROL
FFF55	ENDC	END8	END4	END0	EPROM/RAM SWAP CONTROL
FFF56	ENCC	ENC8	ENC4	ENC0	EPROM/RAM SWAP CONTROL

FFF57	BNK 1 SZ	BNK 0 SZ	RAM CONFIGURATION

FFF58	X	X	X	X	SD	XC	UL	EE	RAM CONTROL REG

FFF60	BNK 1 WS	BNK 0 WS	ON-BOARD RAM WAIT STATE CONTROL

FFF62	VAR	SEL	PROCESSOR CLOCK SELECT

FFFFF	X	X	X	X	LOCK REGISTER

DC OPERATING CHARACTERISTICS
Ta = 0 to 70 deg C Vcc = 5V +-.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	INPUT LEAKAGE		+-10	UA	VIN=.4 TO VCC
IOZ	TRISTATE AND OPEN DRAIN OUTPUT LEAKAGE		+-10	UA	VOUT=.4 TO VCC
VIH	INPUT HIGH VOLTAGE	2.0		V	
VIL	INPUT LOW VOLTAGE		.8	V	
ICC	SUPPLY CURRENT		50	MA	ALL OUTPUTS OPEN, INPUTS AT 2.0V, CLKOUT=SYSCLK=12 MHZ

FOR OUTPUTS CSFP-, CSF, CSHD-, CSPRGA-, CSPRGB-, CSPRGC-, CSPRGD-/RST-, CS8042-, CS287-, CSNMI-, GTCK-, AND D3-D0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IOUT=-2 MA
VOL	OUTPUT LOW VOLTAGE		.4	V	IOUT=2 MA

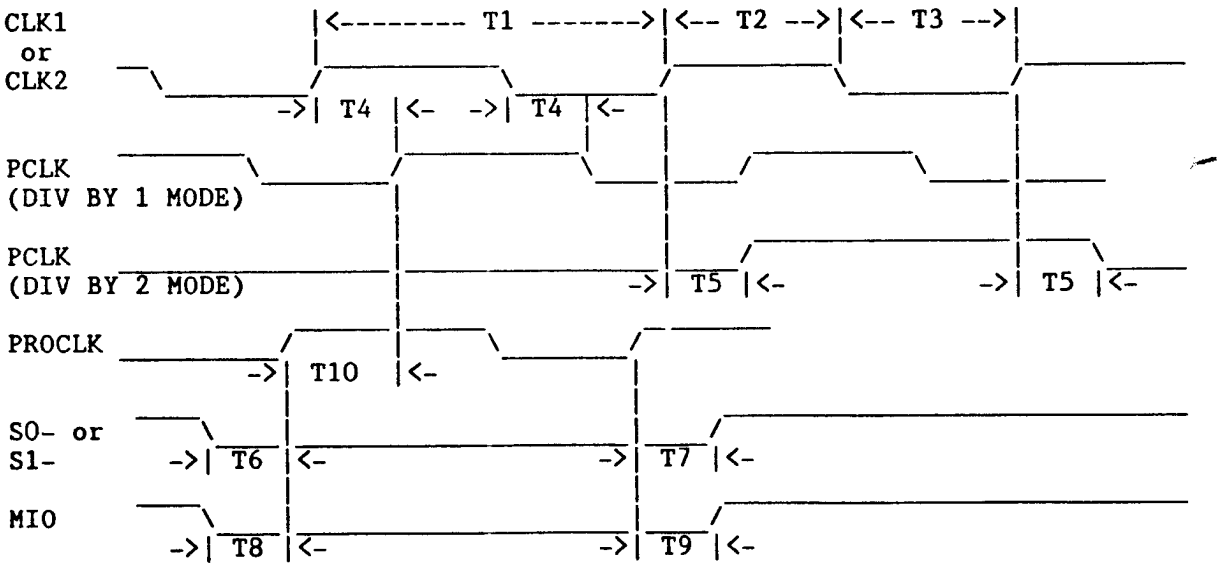
FOR OUTPUTS RASENO-, CASEN-, RASEN1-, MAP-, MEMDIR, CSPROM-, SLDAT-, IO16-, EMM16-, IORDY, ZWS-, PCLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IOUT=-4 MA
VOL	OUTPUT LOW VOLTAGE		.4	V	IOUT=4 MA

AC TIMING CHARACTERISTICS
load capacitance=50 pF each output

CLOCK TIMING FE3040

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T1	CLK1, CLK2 CYCLE	40		NS	
T2	CLK1, CLK2 HIGH PULSE WIDTH	16		NS	
T3	CLK1, CLK2 LOW PULSE WIDTH	16		NS	
T4	CLK1, CLK2 TO PCLK		38	NS	DIV BY 1 MODE
T5	CLK1, CLK2 TO PCLK		38	NS	DIV BY 2 MODE
T6	SO-,S1- SETUP TO PROCLK	-4		NS	
T7	SO-,S1- HOLD FROM PROCLK		20	NS	
T8	MIO SETUP TO PROCLK	10		NS	
T9	MIO HOLD FROM PROCLK		10	NS	
T10	PCLK SETUP TO PROCLK	5	28	NS	



WESTERN DIGITAL
CORPORATION

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