CPU Core Logic for PS/2™ Model 30 Compatible

T-52-33-05

FE2011

Features

- 100% hardware (register level) and software compatible with IBM® PS/2™ Model 30
- Supports 8086, 80C86 and V30 processors
- High performance 10 MHz, zero wait state operation
- One chip includes all CPU core logic for compatible IBM PS/2 Model 30 designs:
  - 8237A compatible DMA controller
  - 8259A compatible interrupt controller with all PS/2 Model 30 extensions
  - 8253 compatible timer
  - 8255 compatible PIO port
  - Bus control logic
  - Clock generation logic
  - DRAM control logic
  - Address and data buffers
- True Model 30 compatible bidirectional keyboard and mouse ports
- Software selectable CPU clock and DMA wait state
- System board I/O decoder
- Integrated EMS (LIM) support for version 4.0 EMS specification
- Variable RAM configurations: 64K, 256K, 1M DRAM
- Typical Model 30 CPU would consist of FE2011, 8086, 2 crystals, 2 TTL devices and memory
- 132-pin JEDEC Standard package
- Low power CMOS

Description

The FE2011 is a single chip implementation of all core logic needed to support the 16-bit Intel® 8086 Central Processing Unit (CPU) in the creation of a high performance IBM® Personal System/2™ Model 30 compatible computer. It replaces nearly 100 components used in prior 8086-based designs.

The FE2011 is 100% hardware, register level, and software compatible with the PS/2™ Model 30. Operating with a 10 MHz clock rate, the FE2011 improves PS/2 Model 30 performance by up to 25%.

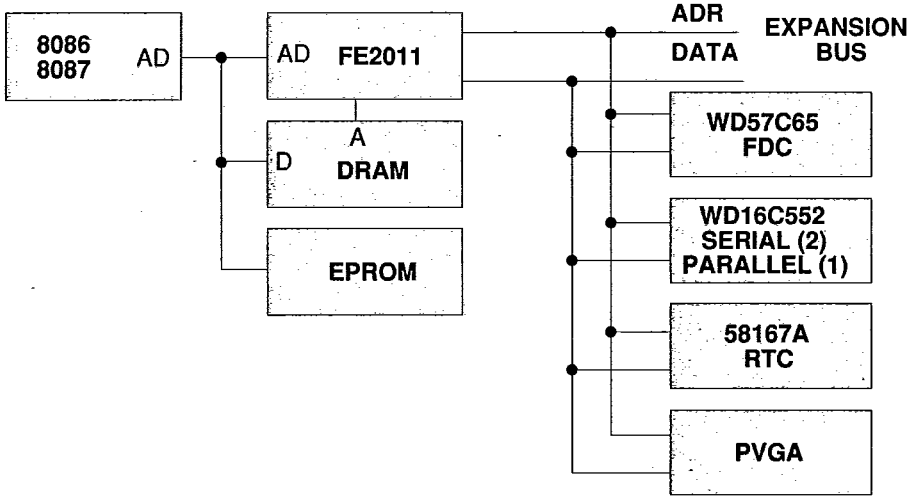
Highly Integrated Functional Capabilities

The FE2011 contains all processor and peripheral support logic. It includes an 8237A compatible Direct Memory Access (DMA) controller, an 8259A interrupt controller with interrupt extension that handles shared interrupts, an 8253 compatible timer, and 8255 compatible peripheral I/O port.

It also includes logic for bus control, DRAM control, clock generation, and the bidirectional keyboard/mouse port.

The FE2011 contains address and data buffers which enable the user to drive an expansion bus without external drivers. A memory data buffer and DRAM address multiplexer make it easy to interface directly to memory.

The FE2011 has built-in extended memory support (the Lotus, Intel and Microsoft im-



Model 30 Compatible System

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CPU Core Logic for PS/2 Model 30 Compatibles

plementation of EMS) that allows access to up to 2.5 Mbytes of memory through use of four page registers.

A system board I/O decoder provides chip select signals for on-board peripherals: parallel port, serial port, floppy disk controller, hard disk controller and display adapter.

Implementation Flexibility

The FE2011 supports a flexible memory architecture. It allows usage of 64K, 256K and 1M DRAM in five different configurations.

With the EMS feature, the FE2011 supports a total of 2.5 Mbytes of memory consisting of 640K of conventional memory and 1920K of expanded memory. Operation at 10 MHz requires the use of 100 ns DRAM.

The FE2011 is designed for performance flexibility. It operates at software selectable CPU clock rates of 7.15 or 9.54 MHz that are derived from a single 28.636 MHz crystal. The FE2011 can be optionally driven at 8 or 10 MHz using external crystal/oscillators. In addition, the FE2011 supports software selectable DMA wait states of zero or one.

Packaging

Manufactured in low-power CMOS, the FE2011 is available in a surface mount 132-pin JEDEC Standard package.

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