FE2010

PC BUS CPU & PERIPHERAL CONTROLLER IC

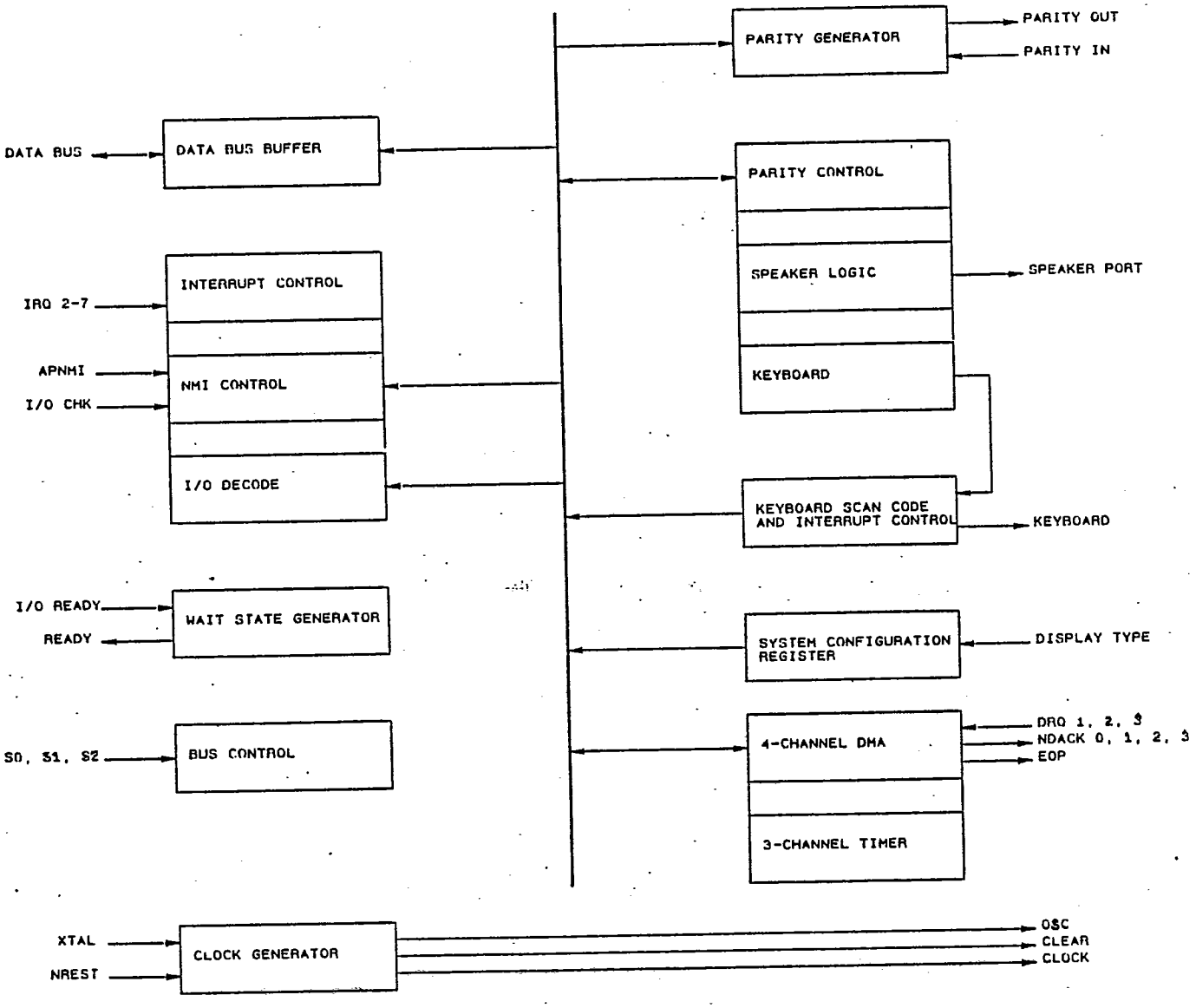
* 100% Hardware & Software compatible to the IBM-PC
* 8284 Clock Generator
* 8288 Bus Controller
* 4 DMA Channels
* 8 Interrupt Channels
* 3 timer Channels
* 84 Pin J-Type Leaded Surface Mount Plastic Chip Carrier
* Keyboard Port
* Complete CPU control logic
* System configuration register eliminating external switches
* 256K & 64K RAM support
* HCMOS Technology
* TTL Compatible

The Faraday XT CPU controller integrated Circuit (FE2010) is a highly integrated chip that allows designers to easily build a IBM compatible PC or XT single board computer.

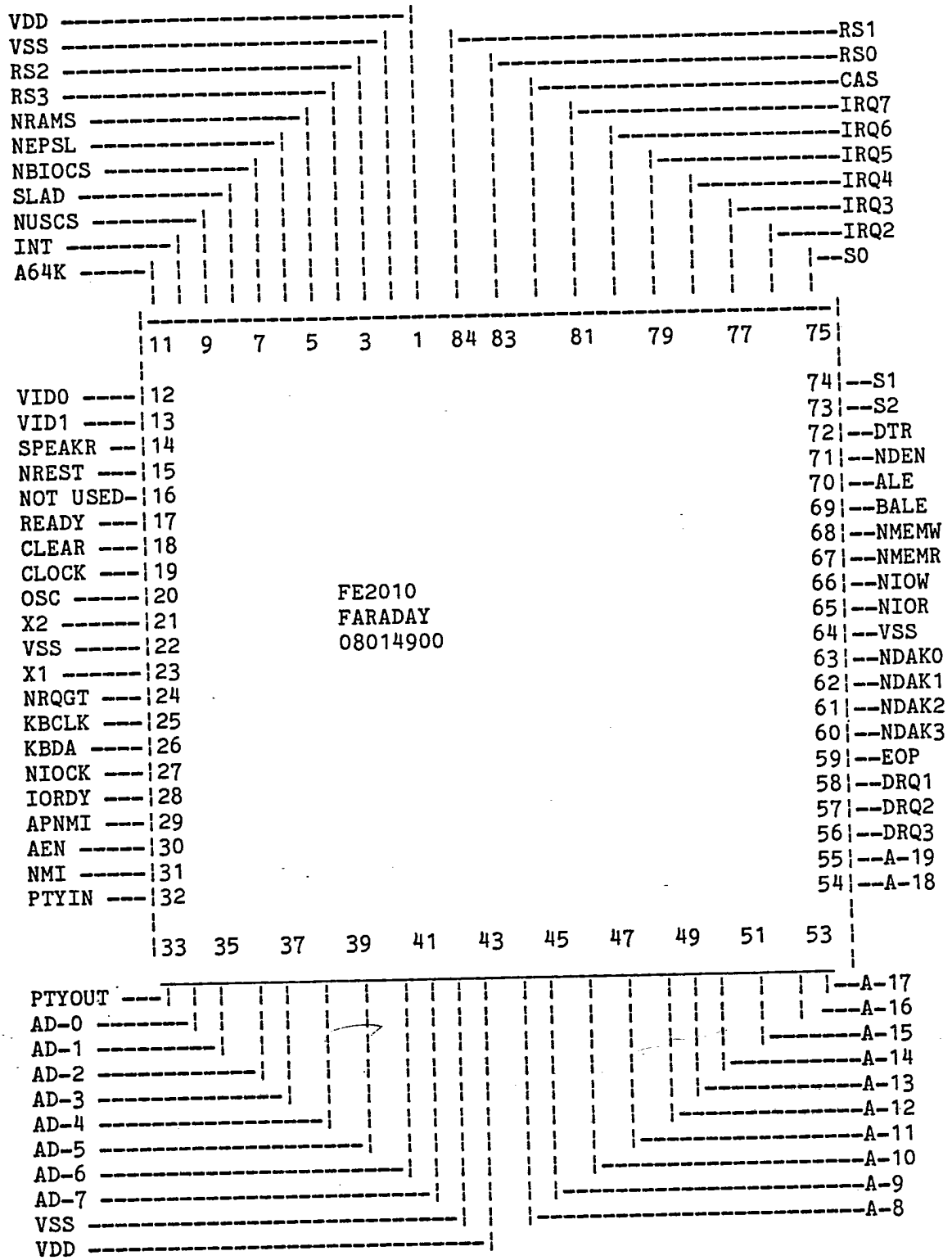
The FE2010 has been designed for OEMs who would like to reduce cost, lower power requirments, increase reliability, and reduce board size over that of a functionally equivalent IBM PC or XT motherboard. The FE2010 replaces a total of 71 components, while reducing the size of a typical PC/XT motherboard by 77% (Appendix A).

The FE2010 replaces functionally five Intel peripheral controller I C's in a motherboard(8284 Clock Generator, 8288 Bus Controller, 8259A Interrupt controller, 8237A DMA controller & 8253 Timer). In addition, it supports both 64K and 256K memory types and has an internal configuration register to replace external switches in the board design.

The FE2010 is a 2 micron CMOS gate-array packaged in an 84 Pin J-type Leaded Surface Mount Plastic Chip Carrier (mating socket Burndy part number Q1LE84P10).



FE2010 BLOCK DIAGRAM



FE2010 PIN DIAGRAM

PIN DESCRIPTION:

PIN	TYPE	SYMBOL	FUNCTION
1	-	VDD	POWER: +5 volts supply
2	-	VSS	GROUND
3	O	RS2	RAS 2 Active high RAS signal for RAM bank 2
4	O	RS3	RAS 3 Active high RAS signal for RAM bank 3
5	O	NRAMS	RAM DECODE Active low Decode for on board RAM RAM size can be: 4 banks of 64K RAMS (256K total memory) 4 banks of 256K RAMS (640K total memory) 1 bank of 256K RAMS (256K total memory)
6	O	NEPSL	PROM DECODE Active low Top 64K decode (F0000 to FFFFF)
7	O	NBIOCS	BIOS ROM chip enable Active low Top 8K decode (FE000 to FFFFF)
8	O	SLAD	ADDRESS SELECT Active high Select signal for dynamic RAM address muxtiplexer Low = lower address bits High = higher address bits
9	O	NUSCS	USER PROM SELECT Active low F0000 to F5FFF
10	O	INT	INTERRUPT TO CPU (8088) Active high
11	I	A64K	RAM TYPE SELECT Jumper for RAM type

Low = 256K RAMS
High = 64K RAMS

12	I	VID0	VIDEO TYPE 0 Video type jumper 0
13	I	VID1	VIDEO TYPE 1 Video type jumper 1

VID1	VID0	Video type
0	0	None
0	1	40 X 25 Color
1	0	80 X 25 Color
1	1	Monochrome or Monochrome and Color

14	O	SPEAKR	DATA TO SPEAKER
15	I	NREST	RESET IN Active low External reset in to generate reset to system
16	I	---	UNUSED Should be left open
17	O	READY	READY TO CPU (8088) Active high
18	O	CLEAR	RESET TO CPU (8088) AND EXPANSION BUS Active high
19	O	CLOCK	CLOCK TO CPU (8088) AND EXPANSION BUS 4.77 Mhz clock
20	O	OSC	OSC TO EXPANSION BUS 14.31818 Mhz clock
21	O	X2	CRYSTAL OUTPUT
22	-	VSS	GROUND
23	I	X1	CRYSTAL INPUT
24	I/O	NRQGT	REQUEST/GRANT TO CPU (8088) FOR BUS Active low
25	I/O	KBCLK	KEYBOARD CLOCK Clock to and from keyboard
26	I/O	KBDA	KEYBOARD DATA Active high Data to and from keyboard

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27	I	NIOCK	ERROR FROM EXPANSION BUS Active low
28	I	IORDY	READY FROM EXPANSION BUS Active high
29	I	APNMI	NMI FROM CO-PROCESSOR (8087) Active high
30	O	AEN	DMA CYCLE Active high Signal to indiate that the current bus cycle is a DMA cycle
31	O	NMI	NON MASKABLE INTERRUPT TO CPU (8088) Active high NMI generated by 8087, memory parity error, or error from bus (NIOCK)
32	I	PTYIN	PARITY BIT FROM PARITY RAM
33	O	PTYOUT	PARITY BIT TO PARITY RAM
34	I/O	AD-0	ADDRESS DATA BUS BIT 0
35	I/O	AD-1	1
36	I/O	AD-2	2
37	I/O	AD-3	3
38	I/O	AD-4	4
39	I/O	AD-5	5
40	I/O	AD-6	6
41	I/O	AD-7	7
42	-	VSS	GROUND
43	-	VDD	POWER: + 5 volts supply
44	I/O	A-8	ADDRESS BUS BIT 8
45	I/O	A-9	9
46	I	A-10	10
47	I	A-11	11
48	I	A-12	12
49	I/O	A-13	13

50	I/O	A-14	14
51	I/O	A-15	15
52	I/O	A-16	16
53	I/O	A-17	17
54	I/O	A-18	18
55	I/O	A-19	19
56	I	DRQ3	DMA REQUEST LINE 3 Active high
57	I	DRQ2	DMA REQUEST LINE 2 Active high
58	I	DRQ1	DMA REQUEST LINE 1 Active high
59	O	EOP	END OF PROCESS INDICATOR FOR DMA Active high
60	O	NDAK3	DMA ACKNOWLEDGE FOR CHANNEL 3 Active low
61	O	NDAK2	DMA ACKNOWLEDGE FOR CHANNEL 2 Active low
62	O	NDAK1	DMA ACKNOWLEDGE FOR CHANNEL 1 Active low
63	O	NDAK0	DMA ACKNOWLEDGE FOR CHANNEL 0 Active low Indicates a refresh cycle
64	-	VSS	GROUND
65	O	NIOR	I/O READ COMMAND Active low
66	O	NIOW	I/O WRITE COMMAND Active low
67	O	NMEMR	MEMORY READ COMMAND Active low
68	O	NMEMW	MEMORY WRITE COMMAND Active low
69	O	BALE	ADDRESS LATCH ENABLE Active high Address latch signal to expansion bus

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70	O	ALE	ADDRESS LATCH ENABLE Active high Address latch signal to address latches
71	O	NDEN	DATA ENABLE TO TRANSCEIVERS FOR LOCAL OR SYSTEM BUS Active low Signal to enable data transceiver
72	O	DTR	DATA TRANSMIT OR RECEIVE Active high Signal to data transceiver to indidate a write cycle
73	I	S2	CPU (8088) STATUS BIT S2
74	I	S1	CPU (8088) STATUS BIT S1
75	I	S0	CPU (8088) STATUS BIT S0
76	I	IRQ2	INTERRUPT REQUEST INPUT 2 Active high
77	I	IRQ3	INTERRUPT REQUEST INPUT 3 Active high
78	I	IRQ4	INTERRUPT REQUEST INPUT 4 Active high
79	I	IRQ5	INTERRUPT REQUEST INPUT 5 Active high
80	I	IRQ6	INTERRUPT REQUEST INPUT 6 Active high
81	I	IRQ7	INTERRUPT REQUEST INPUT 7 Active high
82	O	CAS	RAM CAS Active high CAS signal for RAM memory
83	O	RS0	RAS 0 Active high RAS signal for RAM bank 0
84	O	RS1	RAS 1 Active high RAS signal for RAM bank 1

FUNCTIONAL DESCRIPTION - FE2010

INTERRUPT CONTROLER

The interrupt controller is the equivalent of an 8259A interrupt controller. Interrupt 0 is tied to the keyboard port and interrupt 1 is tied to timer 0.

WAIT STATE GENERATOR

The wait state generator generates 1 wait state on all CPU I/O and DMA operations. It also synchronizes the external ready that may be used to generate wait states.

BUS CONTROL

The bus controller is the equivalent of an 8288 for CPU bus operations, and generates the bus controls for DMA operations. Memory decodes including RAS, CAS generation are provided by this block.

CLOCK GENERATOR

The clock generator is the equivalent of a 8284A clock generator. It also generates the clock for the timer.

PARITY GENERATOR

The parity generator checks and generates parity for RAM memory.

KEYBOARD PORT

The keyboard port connects to an IBM compaitble keyboard.

DMA

The DMA is the equivalent of an 8237 DMA controller. Channel 0 is reserved for the refresh of RAM memory.

TIMER

The timer is the equivalent of a 8253 timer. Channel 0 is tied to interrupt 0, channel 1 is used to generate refresh, and channel 2 is used for the speaker port.

PIO

The PIO is used to for system configuration, to control the keyboard and speaker ports, and to enable error checks.

FE2010 TIMING & A/C SPECIFICATIONS

T-52-33-15

1.CLOCK HIGH PERIOD	83 NS
2.CLOCK LOW PERIOD	127 NS
3.CLOCK RISE TIME	< 10 NS
4.CLOCK FALL TIME	< 10 NS
5.OSC RISE TIME	< 10 NS
6.OSC FALL TIME	< 10 NS
7.CLOCK _ CLEAR _	22 NS
8.CLOCK _/ READY _	81 NS
9.CLOCK _/ READY _/	67 NS
10.READY _/ CLOCK _/	143 NS
11.OSC _ CLOCK _/	15 NS
12.OSC _ CLOCK _	28 NS
13.AD(7:0) >< PTYOUT ><	64 NS
14.NIOR _ AD(7:0) >< INVALID	454 NS
15.NIOR _/ AD(7:0) >< INVALID	40 NS
16.CLOCK _ NIOR,NIOW,NMEMR,NMEMW _/ (AEN=0)	24 NS
17.CLOCK _ NIOR,NIOW,NMEMR,NMEMW _ (AEN=0)	32 NS
18.CLOCK _ NDAK0,NDAK1,NDAK2,NDAK3 _/	42 NS
19.CLOCK _ NDAK0,NDAK1,NDAK2,NDAK3 _	59 NS
20.CLOCK _/ EOP _/	136 NS
21.CLOCK _/ EOP _	145 NS
22.CLOCK _/ BALE _	26 NS
23.RAS0,1,2,3 _/ SLAD _/	31 NS
24.ALE _ AD(7:0) >< INVALID (AEN=1)	24 NS
25.BALE _ ALE _	7 NS
26.CLOCK _/ DTR _/	17 NS
27.CLOCK _/ NDEN _/ (READ)	21 NS
28.CLOCK _/ NDEN _/ (WRITE)	99 NS
29.X1 _/ CLOCK _/	47 NS

Absolute Maximum Ratings

TA=+25 C

Power supply voltage, VDD	-0.5 V to +7.0 V
Power dissipation, PDMAX	
Input voltage, VI	-0.5 V to VDD +0.3 V
Output voltage, VO	-0.5 V to VDD +0.3 V
Operating temperature, TOPT	
Storage temperature, TSTG	-65 C to +150 C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

TA=+25 C, VDD=0 V

Parameter	Limits Symbol	Min	Max	Unit	Test Conditions
					fc = 1 MHz
Input capacitance	CI		15	pF	Unmeasured pins
I/O capacitance	CIO		15	pF	returned to 0 V

DC Characteristics

TA = 0 C to 70 C, VCC = 5 V $\pm$ 5%

PARAMETER	CONDITION	MIN	MAX	PINS
VIL	VDD=5V+/-5%	VSS	0.8	029=APNMI,011=A64K, 058=DRQ1,057=DRQ2, 056=DRQ3,028=IORDY, 076=IRQ2,077=IRQ3, 078=IRQ4,079=IRQ5, 080=IRQ6,081=IRQ7, 027=NIOCK, 016=NTSTCR, 032=PTYIN,075=S-0, 074=S-1,073=S-2, 012=VID0,013=VID1
VIL	VDD=5V+/-5%	VSS	0.8	034=AD-0,035=AD-1, 036=AD-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AH-0,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1,024=NRQGT
VIL	VDD=5v+/-5%	VSS	0.3*VDD	023=X1
VIL	VDD=5V+/-5%	VSS		015=NREST
VIL	VDD=5V+/-5%	VSS	1.0	025=KBCLK,026=KBDA
VIH	VDD=5V+/-5%	2.0V	VDD	029=APNMI,011=64K, 058=DRQ1,057=DRQ2, 056=DRQ3,028=IORDY, 076=IRQ2,077=IRQ3, 078=IRQ4,079=IRQ5, 080=IRQ6,081=IRQ7, 027=NIOCK, 016=NTSTCR, 032=PTYIN,075=S-0, 074=S-1,073=S-2, 012=VID0,013=VID1
VIH	VDD=5V+/-5%	2.0V	VDD	034=AD-0,035=AD-1, 036=AD-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AH-0,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1,024=NRQGT
VIH	VDD=5V+/-5%	0.7*VDD	VDD	023=X1
VIH	VDD=5V+/-5%		VDD	015=NREST

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PARAMETER	CONDITION	MIN	MAX	PINS
VIH	VDD=5V+/-5%	4.0	VDD	025=KBCLK,026=KBDA
IIL	VIN=0.0V	-10UA	-300UA	029=APNMI,011=A64K 058=DRQ1,057=DRQ2, 056=DRQ3,028=IORDY, 076=IRQ2,077=IRQ3, 078=IRQ4,079=IRQ5, 080=IRQ6,081=IRQ7, 027=NIOCK, 016=NTSTCR, 032=PTYIN,075=S-0, 074=S-1,073=S-2, 012=VID0,013=VID1
IIL	VIN=0.0V		-10UA	034=AD-0,035=AD-1, 036=AD-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AH-1,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1,024=NRQGT
IIL	VIN=0.0V		-10UA	023=X1
IIL	VIN=0.0V		-10UA	025=KBCLK,026=KBDA
IIH	VIN=VDD		40UA	029=APNMI,011=A64K, 058=DRQ1,057=DRQ2, 056=DRQ3,028=IORDY, 076=IRQ2,077=IRQ3, 078=IRQ4,079=IRQ5, 080=IRQ6,081=IRQ7, 027=NIOCK, 016=NTSTCR, 032=PTYIN,075=S-0, 074=S-1,073=S-2, 012=VID0,013=VID1
IIH	VIN=VDD		10UA	034=AD-0,035=AD-1 036=AD-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AD-0,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1,024=NRQGT
IIH	VIN=VDD		10UA	023=X1
IIH	VIN=VDD		10UA	025=KBCLK,026=KBDA

PARAMETER	CONDITION	MIN	MAX	PINS
VOL	IOL=2.0MA		0.4V	030=AEN,070=ALE, 069=BALE,018=CLEAR, 072=DTR,059=EOP, 010=INT,007=NBIOCS, 063=NDAK0, 062=NDAK1, 061=NDAK2, 060=NDAK3,071=NDEN, 006=NEPSL,065=NIOR, 066=NIOW,067=NMEMR, 068=NMEMW,031=NM1, 005=NRAMS, 009=NUSCS, 033=PTYOUT, 017=READY
VOL	IOL=4.0MA		0.4V	082=CAS,019=CLOCK, 020=OSC,083=RSO, 084=RS1,003=RS2, 004=RS3,008=SLAD, 014=SPEAKR
VOL	IOL=4.0MA		0.4V	046=AM-0,047=AM-1, 048-AM-2
VOL	IOL=4.0MA		0.4V	025=KBCLK,026=KBDA, 024=NRQGT
VOL	IOL=8.0MA		0.4V	021=X2
VOL	IOL=4.0MA		0.4V	034=AD-0,035=AD-1, 036=13-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AH-0,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1
VOH	IOH=-2.0MA	2.4V		030=AEN,070=ALE, 069=BALE,018=CLEAR, 072=DTR,059=EOP, 010=INT,007=NBIOCS, 063=NDAK0, 062=NDAK1, 061=NDAK2, 060=NDAK3,071=NDEN, 006=NEPSL,065=NIOR, 066=NIOW,067=NMEMR, 068=NMEMW,031=NMI, 005=NRAMS, 009=NUSCS, 033=PTYOUT, 017=READY

PARAMETER	CONDITION	MIN	MAX	PINS
VOH	IOH=-4.0MA	2.4V		082=CAS,019=CLOCK, 020=OSC,083=RS0, 084=RSI,003=RS2, 004=RS3,008=SLAD, 014=SPEAKR
VOH	IOH=-4.0MA	2.4V		046=AM-0,047=AM-1, 048=AM-2
VOH	N/A	N/A		025=KBCLK,026=KBDA, 024=NRQGT
VOH	IOH=-8.0MA	2.4V		021=X2
VOH	IOH=-12.MA	2.4V		034=AD-0,035=AD-1, 036=AD-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AH-0,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1
IOZ	OV<VOUT<VDD	-10.0UA	10.0UA	045=AM-0,047=AM-1, 048=AM-2,025=KBCLK, 026=KBDA,024=NRQGT
IOZ	OV<VOUT<VDD	-90.0UA	-1.0UA	034=AD-0,035=AD-1, 036=AD-2,037=AD-3, 038=AD-4,039=AD-5, 040=AD-6,041=AD-7, 049=AH-0,050=AH-1, 051=AH-2,052=AH-3, 053=AH-4,054=AH-5, 055=AH-6,044=AL-0, 045=AL-1
IDD	VDD=5.25V			

PROGRAMMING

The FE2010 accepts I/O read write commands from the CPU.

I/O Address Map

Address	Use
000-00F	DMA controller
020-021	Interrupt controller
040-043	Timer
060-063	PIO
081-083	DMA page registers
0A0	NMI mask register
100-1FF	Reserved

The timer is programmed the same as the 8253 timer, the DMA controller is programmed the same as the 8237 DMA controller, and the interrupt controller is programmed the same as the 8259 interrupt controller.

PIO

The PIO is the equivalent of the 8255 PIO, but it is configured in a fixed way for system configuration, controlling the speaker port, and as a keyboard port.

Address	Use
060 (read)	Keyboard Data Register
061	Control Register
062	Switch Register
063 (write)	Configuration Register

Keyboard Data Register

The Keyboard Data Register is a read only register that is used to read data from the keyboard. When a character is in the register, interrupt 1 will be sent to the interrupt controller. The register may be cleared by setting bit 7 of the control register.

Control Register (061)

Data Bit	Use
0	Gate speaker timer channel
1	Gate speaker data
2	Switch register select
3	Not used
4	Disable parity check
5	Disable I/O check
6	Enable keyboard clock
7	Clear Keyboard Data Register

Switch Register (Write) (062)

The switch register is used for system configuration. Bits 0-3, 6 and 7 are read write. Bits 4 and 5 are the VID0 and VID1 pin.

Data Bit	Use
0	Not used
1	8087 installed
2-3	System memory
4-5	Video type
6-7	# of floppies

Switch Register (Read) (062)

When the switch register is read the data is multiplexed on bits 0-3 of the data bus. The muxtiplexing is controlled by bit 2 of the Control Register.

Control register bit 2	Switch Register Mux
0	Bits 4-7
1	Bits 0-3

Data Bit	Control Register bit 2 = 1	Control Register bit 2 = 0
0	Switch Register bit 0	Switch Register bit 4
1	Switch Register bit 1	Switch Register bit 5
2	Switch Register bit 2	Switch Register bit 6
3	Switch Register bit 3	Switch Register bit 7
4	Timer 2 Output	Timer 2 Output
5	Timer 2 Output	Timer 2 Output
6	I/O Check	I/O Check
7	Parity check	Parity Error

Configuration Register (063)

The configuration register is a write only register that is used for configuartion. If bit 3 is written, this register and the switch register are locked in that they may not be written to. This lock is removed by a system reset.

Data Bit	Use
0	Enable parity
1	8087 present (enable 8087 NMI)
2	256K RAMS
3	Lock register
4-7	Not used

Page Registers (081-083)

The page registers are write only registers used to generate address bits 16-19 during a DMA transfer.

Address	Page Register
81	DMA Channel 2
82	3
83	1

Data Bits	Use
0	DMA Address 16
1	17
2	18
3	19

NMI Mask Register (0A0)

The NMI Mask Register is used to enable the NMI to the CPU (8088).

Data Bit	Use
0-6	Not used
7	Enable NMI

APPENDIX A

Chip Replacement Chart
FE2010

8288	74LS175(2)	74LS74(4)
8259A	74LS138(3)	74LS30(2)
8284A	74LS244(2)	74LS00(1)
8237A(5)	74LS670	74LS08(3)
8253(5)	74LS322	74LS158(2)
8255A(5)	74LS125(2)	74LS139
DELAY-LINE(1)	74LS10	74LS32
74S280	74LS11	74S08
74LS373(2)	74LS04(4)	74LS14
74LS245(3)	74LS02(1)	SWITCHES(2)
		RESISTORS(10)

No. of chips replaced = 71

APPLICATION NOTE

SBC DESIGN BASED ON FE2010

This application note describes an 8088 based PC BUS Single Board computer design. This SBC is one of Faraday's board level product called MICRO PC and utilizes the FE2010 I.C.

Configuration:

* one bank of 256K onboard RAM
* 8K ROM using Intel 2764 type EPROM
* design allowed for Intel 8087 support
* three external ports: speaker port, reset port and NMI port
* the entire board is designed to consume about 430 ma at 5 volts(without the 8087)

The block diagram of the SBC is shown in Fig AP-1 while Fig AP-2 shows the schematics of the board design.

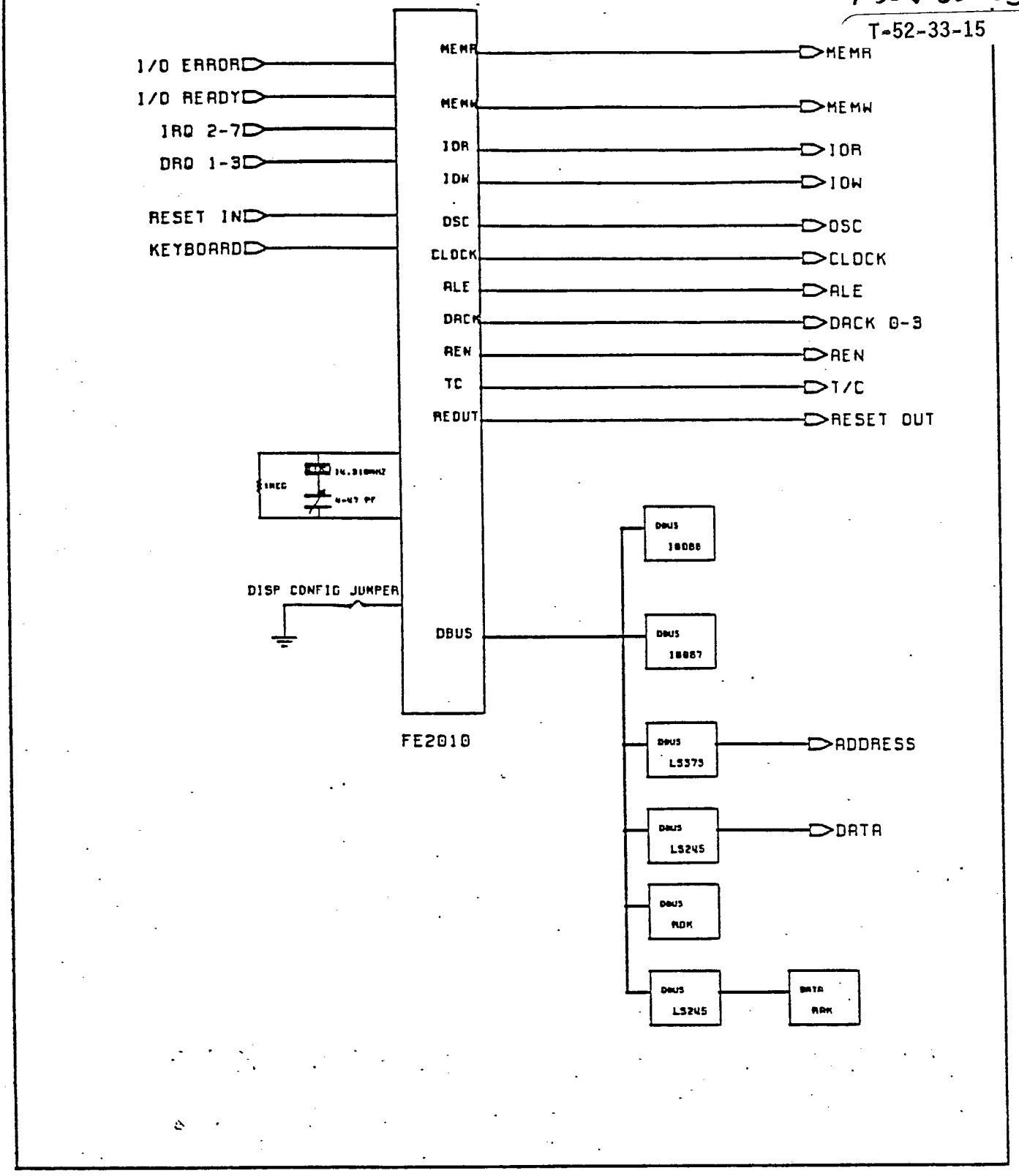


FIG AP-1 BLOCK DIAGRAM OF PC BUS SBC DESIGN

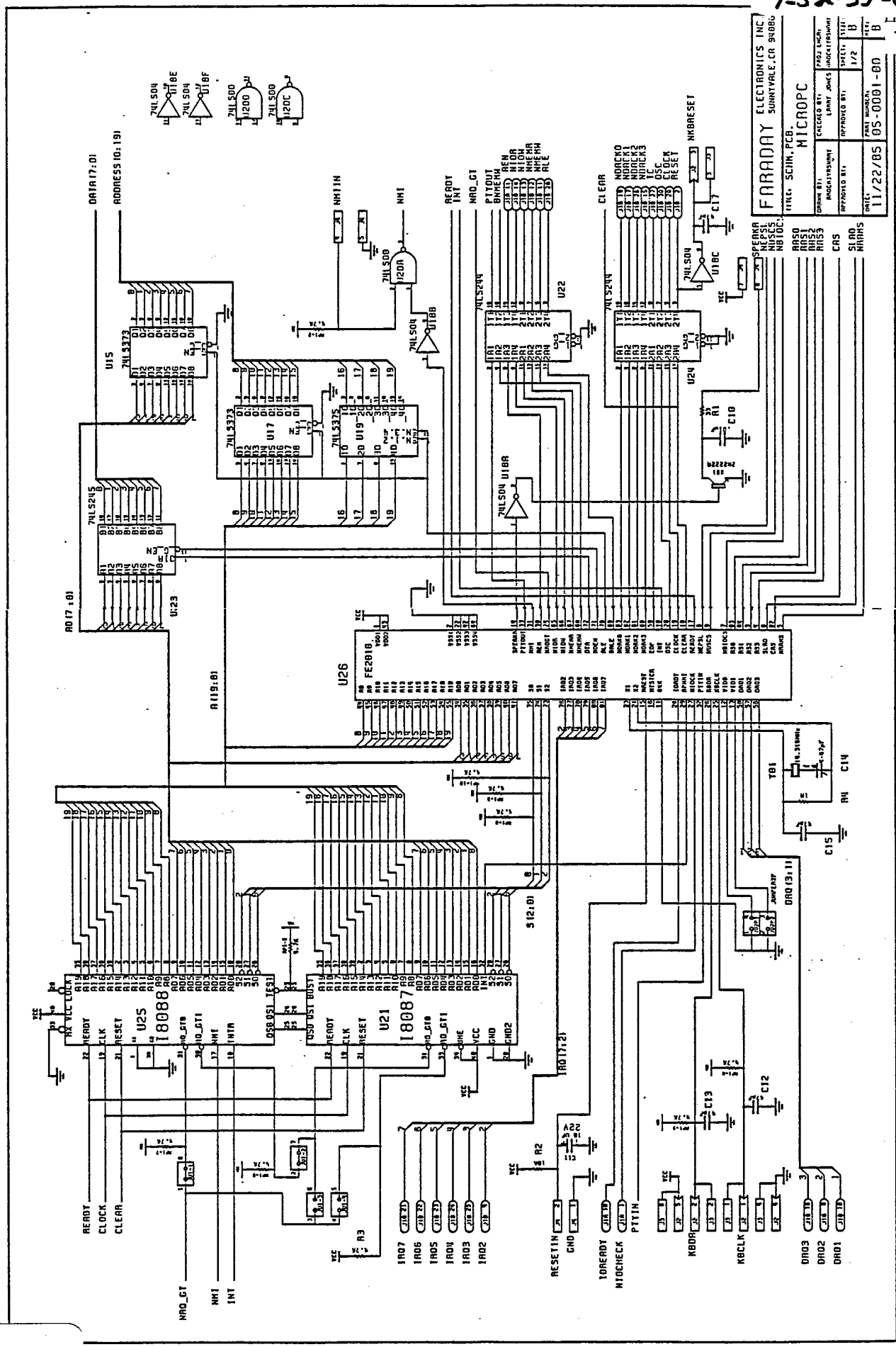
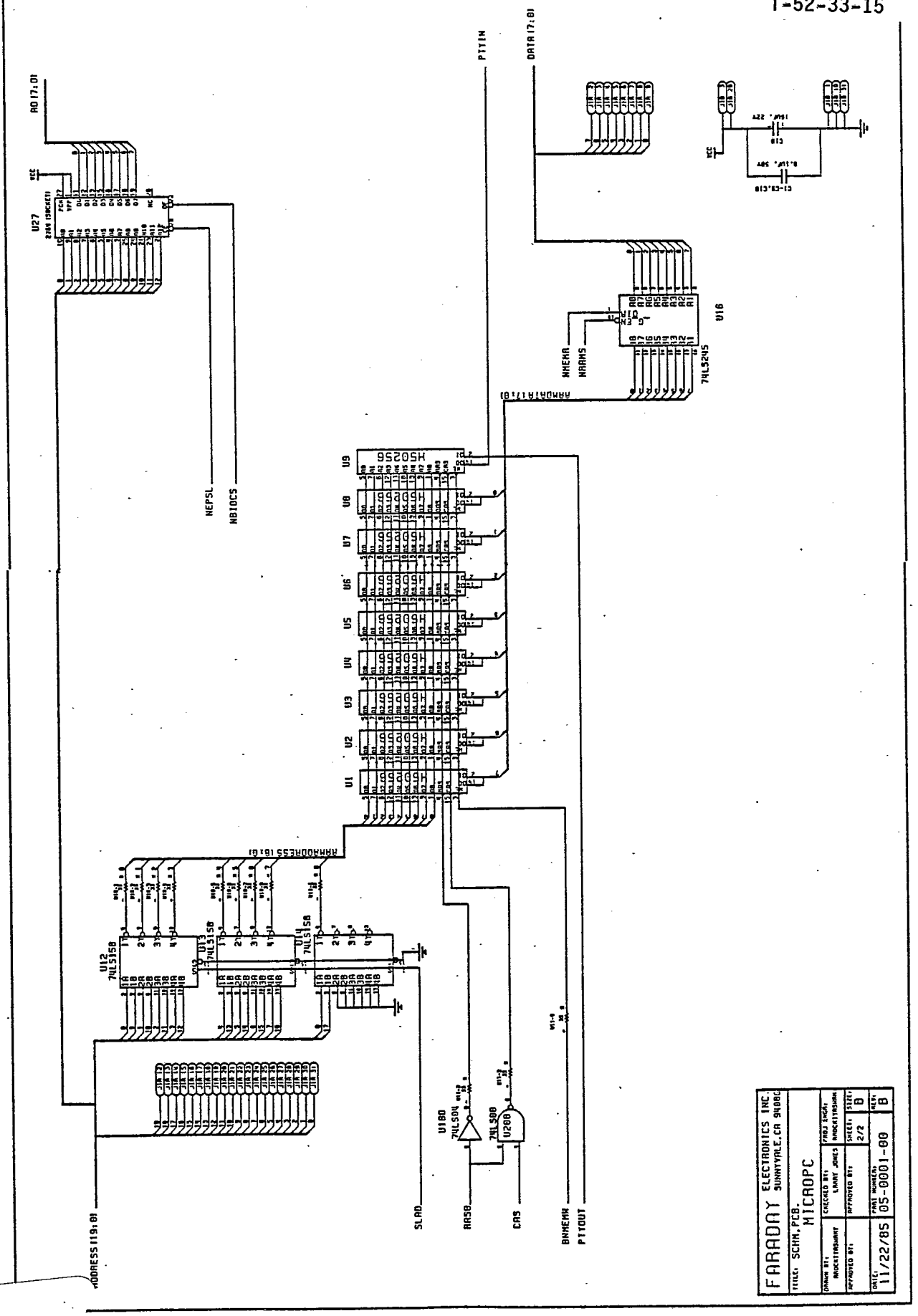


FIG AP-2

T-52-33-03

T-52-33-15



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