VLSI TECHNOLOGY, INC.

PRODUCT SPECIFICATION

VL82C002

INPUT SCANNER

FEATURES

- 16-bit shift register
- Selectable modes of operation:
  - Standard Shift Register Mode
  - Sample and Hold Mode
- In Sample and Hold mode, D_IN[15:0] inputs which pulse low for more than one clock period are held until the shift register is loaded
- 1.0-micron CMOS
- 28-lead Plastic Leaded Chip Carrier (PLCC)

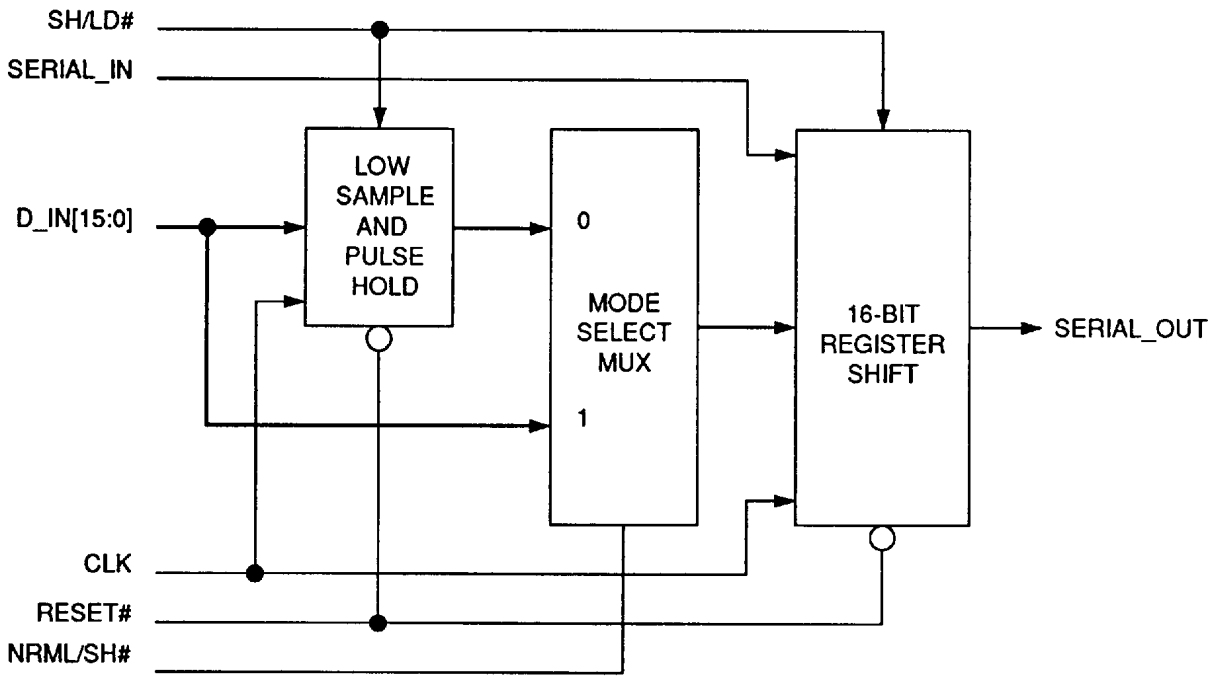
OVERVIEW

The VL82C002 Input Scanner chip implements the serial scanning of the ISA bus compatible interrupt signals. The VL82C002 operates in two modes: Sample and Hold Mode and Standard Shift Register Mode (a non-sampling type of mode).

In the Sample and Hold Mode, the VL82C002 guarantees that any of the D_IN[15:0] inputs which pulse low for more than one period of the input clock will be held until it has been loaded into the shift register.

In the Standard Shift Register Mode, the VL82C002 operates as a 16-bit shift register with the D_IN[15:0] inputs being sampled only when the shift register is instructed to load. Below is a block diagram of the VL82C002.

BLOCK DIAGRAM

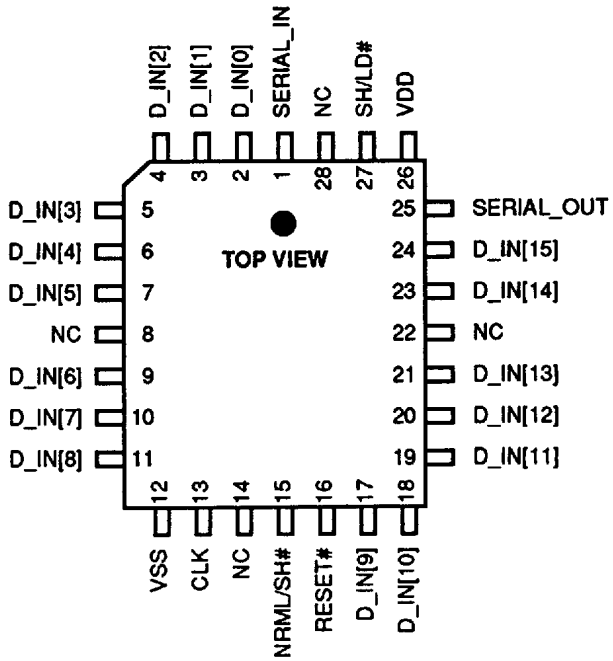


ORDER INFORMATION

Part Number	Package
VL82C002-QC	Plastic Leaded Chip Carrier

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM



PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
1	SERIAL_IN	I	TTL		15	NRML/SH#	I(1)	TTL	
2	D_IN[0]	I	TTL		16	RESET#	I	TTL	
3	D_IN[1]	I	TTL		17	D_IN[9]	I	TTL	
4	D_IN[2]	I	TTL		18	D_IN[10]	I	TTL	
5	D_IN[3]	I	TTL		19	D_IN[11]	I	TTL	
6	D_IN[4]	I	TTL		20	D_IN[12]	I	TTL	
7	D_IN[5]	I	TTL		21	D_IN[13]	I	TTL	
8	NC				22	NC			
9	D_IN[6]	I	TTL		23	D_IN[14]	I	TTL	
10	D_IN[7]	I	TTL		24	D_IN[15]	I	TTL	
11	D_IN[8]	I	TTL		25	SERIAL_OUT	O	TTL	12
12	VSS	GND			26	VDD	PWR		
13	CLK	I	TTL		27	SH/LD#	I	TTL	
14	NC				28	NC			

Notes: (1) Indicates an internal 30K ohm pull-up resistor on pin.

Legend:

I	Input pin
GND	Ground pin
O	Output pin
PWR	Power supply pin
TTL	TTL-compatible input pin

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CLK	13,	I-TTL	Clock - This is the input clock signal. The rising edge of this signal is used to sample inputs or shift out data.
D_IN[15:0]	24, 23, 21:17, 11:9, 7:2	I-TTL	Data In - These 16 inputs are the parallel inputs to the shift register. In the Sample and Hold Mode they are sampled on every rising edge of the input clock, CLK. In this mode, when a low is sampled, it is held until is has been loaded into the shift register. In the Standard Shift Register Mode, these inputs are sampled only on the rising edge of the input clock when SH/LD# is low.
NRML/SH#	15	I-TTL(1)	Normal Shift Register Mode / Sample and Hold Mode - This input controls whether the device operates as a standard shift register, NRML/SH# high, or whether the sample and hold logic is enabled, NRML/SH# low.
RESET#	16	I-TTL	Reset - This active low signal is an asynchronous reset to both the sample and hold logic and the shift register.
SERIAL_IN	1	I-TTL	Serial Input - This input is the serial input to the shift register. It allows multiple VL82C002s to be connected together to form wider shift registers. This input is sampled on the rising edge of the input clock, CLK, when SH/LD# is high.
SERIAL_OUT	25	O-TTL	Serial Out - This is the output of the shift register. After a parallel load, SERIAL_OUT is equal to the value on the D_IN[0] pin (or the value stored in the sample and hold circuit). D_IN[15] is the last of the parallel inputs to be shifted out.
SH/LD#	27	I-TTL	Serial Shift / Parallel Load - This input controls whether the device is in Serial Shift Mode or Parallel Load Mode. When high, the device is in Serial Shift Mode. When low, the device is in Parallel Load Mode. In this mode, the D_IN inputs or the outputs of the sample and hold logic are loaded into the shift register.
NC	8, 14, 22, 28		No Connect.

Note: Refer to the Notes and Legend on page 2 for details on the Signal Type.

AC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tPWL	CLK pulse width low	6		ns	
tPWH	CLK pulse width high	6		ns	
tPRD	CLK period	14		ns	
tD1	CLK rising to SERIAL_OUT		9	ns	30 pF load
tD2	RESET# falling to SERIAL_OUT		10	ns	30 pF load
tSU	SH/LD# Setup to CLK rising	5		ns	
tH	SH/LD# Hold to CLK rising	2		ns	
tSU	SERIAL_IN Setup to CLK rising	5		ns	
tH	SERIAL_IN Hold to CLK rising	2		ns	

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C
Storage Temperature –65°C to +150°C
Supply Voltage to Ground Potential –0.5 V to VDD + 0.3 V
Applied Output Voltage –0.5 V to VDD + 0.3 V
Applied Input Voltage –0.5 V to + 7.0 V
Power Dissipation 100 mW

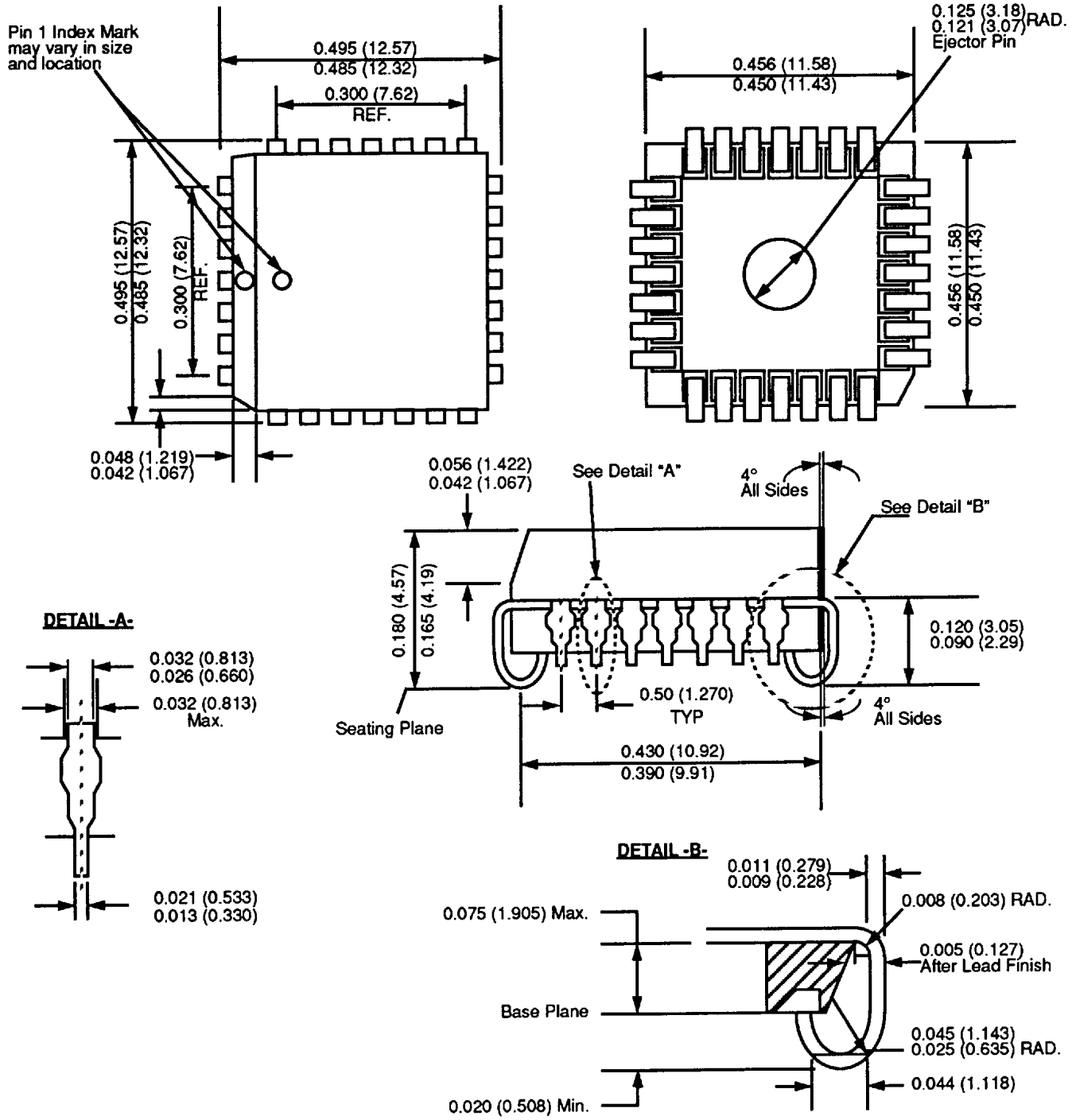
Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs, All Inputs
VOL	Output Low Voltage		0.4	V	IOL = 12.0 mA, SERIAL_OUT
VOH	Output High Voltage	2.4		V	IOH = 1.2 mA, SERIAL_OUT
IIH	Input High Current		10	µA	VIN = VDD, All Inputs
IIL	Input Low Current	–10		µA	VIN = VSS + 0.2 V, All Inputs
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
IDD	Operating Supply Current		40	mA	
IDDQ	Static Supply Current		5.0	mA	

MECHANICAL PACKAGE OUTLINE

28 Lead Plastic Leaded Chip Carrier (PLCC, Dwg No. 25-60001, *B)



Notes:
1. Lead Finish: Matte tin plate or solder plated.
2. Leadframe material: Copper.
3. Tolerance to be ± 0.005 (0.127).
4. Dimensions are in inches and (metric).
5. Molded plastic dim. does not include end flash burr which is 0.010 (0.254) max. all four sides.
6. Spacing to be maintained between formed lead and molded plastic along full length of lead.
7. Maximum co-planarity not to eceed 0.006 inch.

SYSTEM APPLICATION

APPLICATION NOTE:
USING THE VL82C002 WITH THE VL82C480 OR VL82C481

The following shows a typical application using the VL82C002 in a design based on the VL82C480 or the VL82C481 System Controller. It is assumed that the VL82C002 is in the Sample and Hold Mode of operation. In this configuration, the CLK input can be connected to the ISA bus common 14.318 MHz clock. All IRQx references are to the standard ISA interrupts.

TABLE 1. PIN INTERFACE WITH VL82C480 OR VL82C481

VL82C002 Pin #	Name	Connection
1	SERIAL_IN	GND
2	D[0]	IOCHK#
3	D[1]	IRQ[1]
4	D[2]	IRQ[8]#
5	D[3]	IRQ[9]
6	D[4]	IRQ[10]
7	D[5]	IRQ[11]
8	NC	NC
9	D[6]	IRQ[12]
10	D[7]	GND
11	D[8]	IRQ[14]
12	VSS	GND
13	CLK	CLOCK (> 10 MHz)
14	NC	NC
15	NRML/SH#	1= Normal, 0= Sample/Hold
16	RESET#	Active Low
17	D[9]	IRQ[15]
18	D[10]	IRQ[3]
19	D[11]	IRQ[4]
20	D[12]	IRQ[5]
21	D[13]	IRQ[6]
22	NC	NC
23	D[14]	IRQ[7]
24	D[15]	TURBO
25	SERIAL_OUT	480/481 Pin 153
26	VDD	+5
27	SH/LD#	480/481 Pin 150
28	NC	NC