SYSTEM CONTROLLER

DESCRIPTION

The VL82C330 System Controller is highly configurable via software. No hardware jumpers are required. Defaults on reset for the configuration registers allow the system to boot at the CPU's rated speed. However, operational capabilities are reduced until the configuration registers are set to mirror the true system configuration.

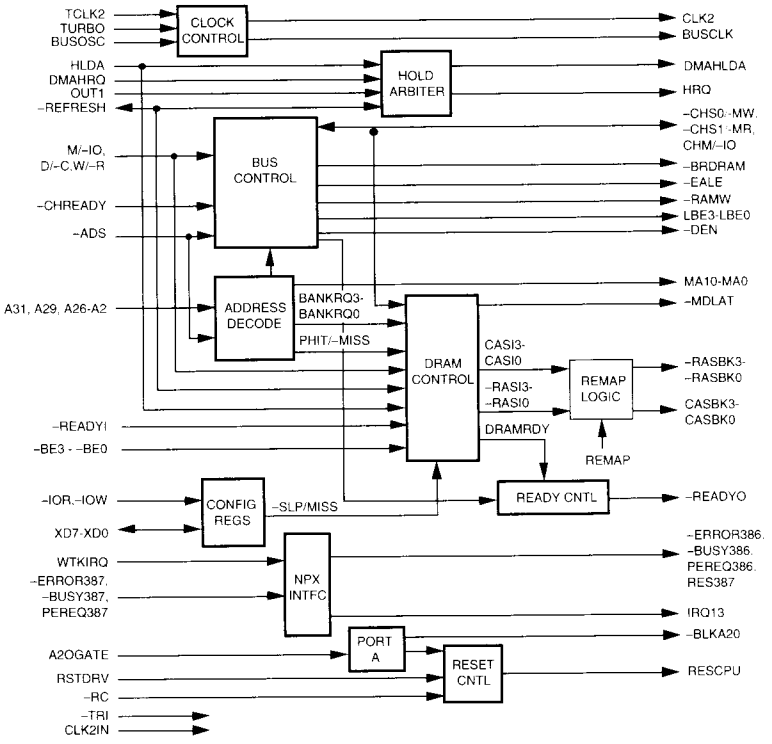
The VL82C330 is designed to perform in 386DX systems running up to 33 MHz. Built-in page mode operation, two- or four-way interleaving and fully programmable memory timing allow the PC designer to maximize system performance using commodity DRAMs. Programmable memory timing allows the system to be setup to match the requirements of the chosen DRAMs; standard or custom.

The VL82C330 handles system board refresh directly and also controls the timing of slot bus refresh which is actually performed by the ISA Bus Controller. Refresh may be performed in coupled or decoupled mode. The former method is the standard PC/AT®-compatible mode where on- and off-board refreshes are performed synchronously. In decoupled mode, the timing of on- and off-board refreshes are independent. Both may be programmed for independent, slower than normal rates. This allows use of low-power, slow refresh DRAMs. The VL82C330 controls all timing in both modes. In all cases, refreshes are staggered to minimize power supply loading and attendant noise on the VDD and ground pins.

The physical banks of DRAM can be logically reordered through one of the indexed configuration registers. This DRAM remap option is useful in order to map out bad DRAM banks allowing continued use of a system until repairs are possible. It also allows DRAM bank combinations not in the supported memory maps to be logically moved into a supported configuration without physically moving memory components. This unique, programmable function performs this task by switching the internal –RASI and CASI signals between the external –RASBK and CASBK pins. This allows internal strobes generated for DRAM bank 0, for example, to be routed to any one of the four on-board DRAM banks.

4

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C330-FC	Plastic Quad Flatpack

Note: Operating temperature range is 0°C to +70°C.

PC/AT is a registered trademark of IBM Corporation.

Active low –RASBK signals are generated to directly drive DRAM banks. Active high CASBK and LBE signals are externally decoded with NAND gates to provide 16 active low CASBK signals. This scheme provides extra timing margin and lower cost since NAND gates are cheaper and faster than equivalent OR gates.

Both the Intel 387™ DX and Weitek 3167 numeric coprocessors are supported and may be used individually or in combination. Support is for both 8-bit wide and 16-bit wide system BIOS ROM.

Full EEMS support is provided in hardware for the complete full LIM EMS 4.0® standard. Seventy-two mapping registers provide a standard and an alternate set of 36 registers each. The system allows backfill to 256K for EEMS support and provides 24 mapping registers covering this space. Twelve of the 36 are page registers which cover the EMS space from C0000h to EFFFFh. These twelve registers can alternatively be mapped in the A0000-BFFFFh and D0000h-DFFFFh range by changing a configuration bit in the VL82C330. All registers are capable of translating over the complete 64 Mbyte range of on-board DRAM. Users preferring an alternate plug-in EMS solution can disable the on-board EMS system as well as system board DRAM, as required, down to 256K.

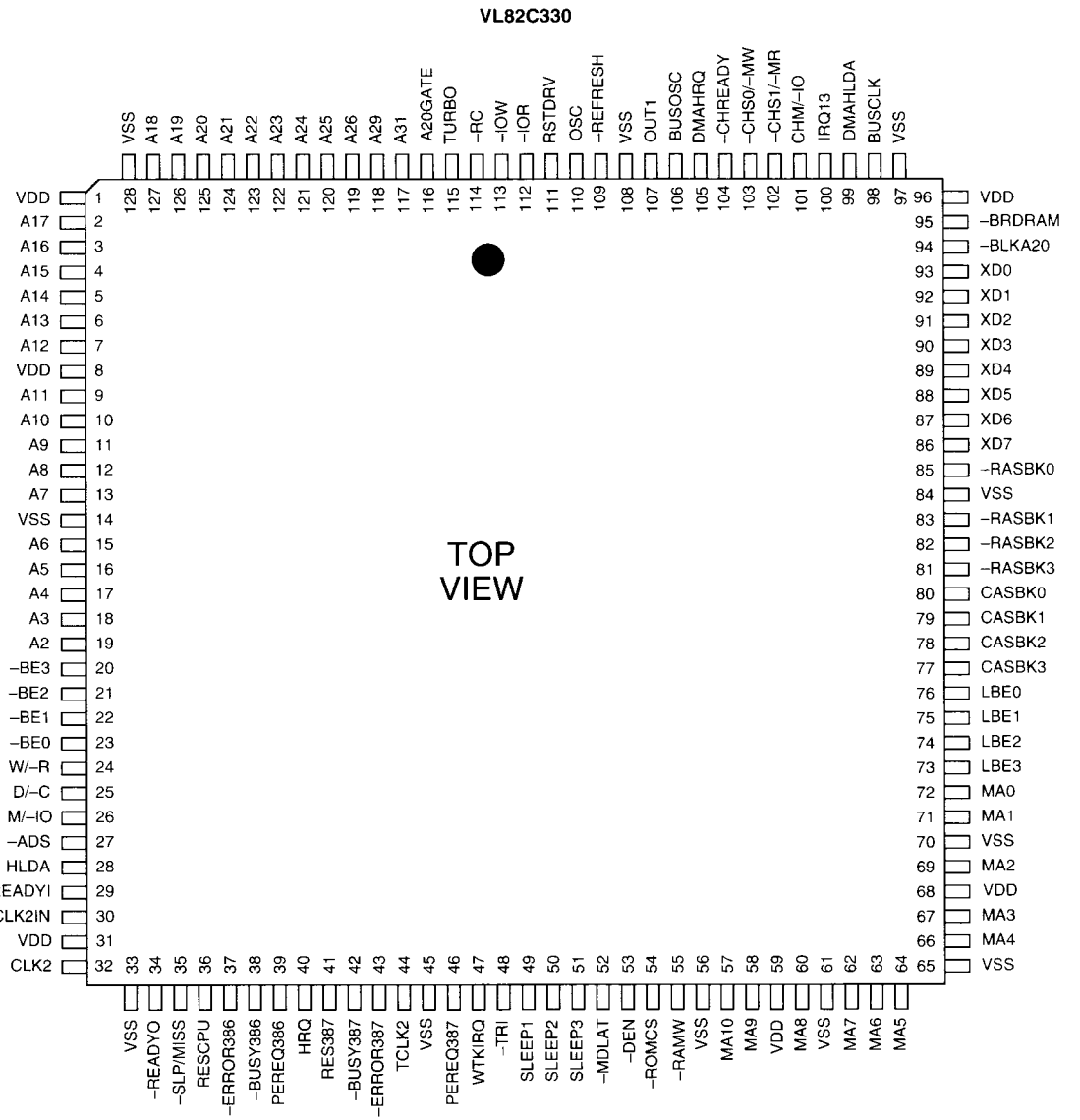
Shadowing features are supported on all 16K boundaries between 640K and 1M. EMS use, shadowed ROM, and direct system board access is possible in non-overlapping fashion throughout this memory space. Control over four access options is provided. These controls are overridden by EMS in segments for which it is enabled.

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

The VL82C330 is used to program the desired operational mode of the AT bus. Based on this programming, it provides the bus clock and signalling interface to the Bus Controller, which actually interfaces with the bus. The bus clock may be derived from the TCLK2 or bus OSC inputs. A programmable divider conditions the selected BUSCLK source providing divide by 1, 2, 3, or 4.

LIM EMS 4.0® is a registered trademark of Lotus Development Corp., Intel Corp., and Microsoft Corp.

PIN DIAGRAM


VL82C330
TOP VIEW
1 VDD
2 A17
3 A16
4 A15
5 A14
6 A13
7 A12
8 VDD
9 A11
10 A10
11 A9
12 A8
13 A7
14 VSS
15 A6
16 A5
17 A4
18 A3
19 A2
20 -BE3
21 -BE2
22 -BE1
23 -BE0
24 W/-R
25 D/-C
26 M/-IO
27 -ADS
28 HLDA
29 -READYI
30 CLK2IN
31 VDD
32 CLK2
33 VSS
34 -READYO
35 -SLP/MISS
36 RESCPU
37 -ERROR386
38 -BUSY386
39 PEREQ386
40 HRQ
41 RES387
42 -BUSY387
43 -ERROR387
44 TCLK2
45 VSS
46 PEREQ387
47 WTKIRQ
48 -TRI
49 SLEEP1
50 SLEEP2
51 SLEEP3
52 -MDLAT
53 -DEN
54 -ROMCS
55 -RAMW
56 VSS
57 MA10
58 MA9
59 VDD
60 MA8
61 VSS
62 MA7
63 MA6
64 MA5
65 VSS
66 MA4
67 MA3
68 VDD
69 MA2
70 VSS
71 MA1
72 MA0
73 LBE3
74 LBE2
75 LBE1
76 LBE0
77 CASBK3
78 CASBK2
79 CASBK1
80 CASBK0
81 -RASBK3
82 -RASBK2
83 -RASBK1
84 VSS
85 -RASBK0
86 XD7
87 XD6
88 XD5
89 XD4
90 XD3
91 XD2
92 XD1
93 XD0
94 -BLKA20
95 -BRDRAM
96 VDD
97 VSS
98 BUSCLK
99 DMAHLDA
100 IRQ13
101 CHM/-IO
102 -CHS1/-MR
103 -CHS0/-MW
104 -CHREADY
105 DMAHRQ
106 BUSOSC
107 OUT1
108 VSS
109 -REFRESH
110 OSC
111 RSTDRV
112 -IOR
113 -IOW
114 -RC
115 TURBO
116 A20GATE
117 A31
118 A29
119 A26
120 A25
121 A24
122 A23
123 A22
124 A21
125 A20
126 A19
127 A18
128 VSS

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A31, A29, A26	117-119	I-TPU	A26 is used to prevent aliasing above 64 Mbyte. A31 and A29 are used to differentiate upper BIOS accesses, Weitek 3167 accesses, and 387DX accesses. When HLDA is active, these signals are held low internally. This is required in order to prevent errant Bus Master and DMA accesses to on-board memory.
A25-A2	120-127, 2-7, 9-13, 15-19	I-TTL	Address Bits - These bits allow direct access of up to 64 Mbytes of memory.
–BE3 - –BE0	20-23	I-TTL	Byte Enables 3 through 0, active low - These signals allow 8-bit resolution during read/write accesses.
W/–R	24	I-TPU	Write or active low Read - W/–R is decoded with the remaining control signals to indicate the type of bus cycle requested.
D/–C	25	I-TPU	Data or active low Code - D/–C is decoded with the remaining control signals to indicate the type of bus cycle requested.
M/–IO	26	I-TPU	Memory or active low I/O - M/–IO is decoded with the remaining control signals to indicate the type of bus cycle requested.
–ADS	27	I-TPU	Address Strobe, active low - Indicates that the address and control signals are valid. This signal is used internally to indicate that the address and command are valid and to determine the beginning of a bus cycle.
CLK2IN	30	I-CMOS	This is the main clock input to the VL82C330 and is connected to the CLK2 signal that is output by the VL82C330. This signal is used internally to clock the VL82C330's logic.
TCLK2	44	I-CMOS	This input is connected to a crystal oscillator whose frequency is equal to two times the system frequency. The CMOS level is used to generate CLK2 output and optionally, bus clock.
CLK2	32	O	This output signal is a CMOS level converted TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
–SLP/MISS	35	IO-OD	As a "power on reset" default, this signal is an output that is equal to bit 7 of the –SLEEP register. When configuration register bit 0 of CTRL = 1, this pin becomes a MISS input for use with a future VLSI product.
–READYO	34	O	Ready Out, active low - This signal is an indication that the current cycle is complete. It is generated from the internal DRAM Controller or the synchronized version of –CHREADY for slot bus accesses. The culmination of these ORed READY signals is sent to the CPU and is also connected to the VL82C330's –READYI input. This signal may be combined externally with other READY sources.
–READYI	29	I-TTL	Ready Input, active low - This signal indicates the current bus cycle is complete.
HLDA	28	I-TTL	Hold Acknowledge, active high - This signal is issued in response to the HRQ driven by the VL82C330. When HLDA is active, the memory control is generated from –CHS1/–MR and –CHS0/–MW.
HRQ	40	O	Hold Request, active high - Driven by the VL82C330 to the CPU, this output indicates that a Bus Master, such as a DMA or AT Channel Master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a coupled refresh cycle. It is synchronized to CLK2.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
RESCPU	36	O	Reset CPU, active high - This signal is sent to the CPU by the VL82C330. It is issued in response to the control bit for software reset located in the Port A register or a read to I/O port EFh. It is also issued in response to signals on the RSTDRV or RC inputs and in response to VL82C330 detection of a shutdown command. In all cases, it is synchronized to CLK2.
–ERROR386	37	O	Error 386, active low - On any CPU reset it is pulled low to set the 386DX to 32-bit coprocessor interface mode.
–BUSY386	38	O	Busy 386, active low - The state of –BUSY387 is always passed through to –BUSY386 indicating that the 387 is processing a command. On occurrence of an –ERROR387 signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RSTDRV.
PEREQ386	39	O	Processor Extension Request 386, active high - An output signal generated in response to a PEREQ387, which is issued by the coprocessor to the VL82C330. PEREQ386 is asserted on occurrence of –ERROR387 after –BUSY387 has gone inactive. A write to F0h returns control of the PEREQ386 signal to directly follow the PEREQ387 input.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
–RAMW	55	O-TTL	RAM Write, active low - This signal is active during memory write cycles and is high at all other times.
MA10-MA0	57, 58, 60, 62-64, 66, 67, 69, 71, 72	O-TTL	Memory Addresses 10 through 0 - These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the bus master addresses.
–RASBK3 - –RASBK0	81-83, 85	O	Row Address Strobe Bank 0 through 3, active low - These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles. The active period for this signal is completely programmable.
CASBK3 - CASBK0	77-80	O-TTL	Column Address Strobe Bank 0 through 3 - These signals are the respective column address strobes for each of the banks. These signals are externally gated (NAND) with the LBE signals to generate the CASBK strobes for each byte of a DRAM memory bank.
LBE3-LBE0	73-76	O	Latched Byte Enable 0 through 3, active high - These signals are the latched version of the CPU's –BE3 - –BE0 signals when the CPU is Bus Master or is the latched version of SA1, SA0, and –BHE when the Master or DMA is in control.
–REFRESH	109	IC-OD	Refresh signal, active low - This output is used by the VL82C330 to initiate an off-board DRAM refresh operation in coupled refresh mode. In decoupled mode, the Bus Controller drives refresh active to indicate to the VL82C330 that it has decoded a refresh request command and is initiating an off-board refresh cycle.
–ROMCS	54	O	ROM Chip Select - This is the on-board system BIOS ROM chip select.
COPROCESSOR SIGNALS			
PEREQ387	46	I-TPD	Coprocessor Extension Request 387, active high - This input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT-compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQ386 during 387 interrupts.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ERROR387	43	I-TPU	Error 387, active low - An input signal from the coprocessor indicating that an error has occurred in the previous instruction. This signal is internally gated and latched with –BUSY387 to produce IRQ13.
–BUSY387	42	I-TPU	Busy 387, active low - An input signal that is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQ386.
RES387	41	O	Reset 387, active high - This output is connected to the 387DX reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. A write to port F1h only resets the coprocessor. A software FINIT signal must occur after an F1h generated reset before the coprocessor is reset to the same internal state that a 287 is put into by a hardware reset alone. Optionally, the F1h reset may be disabled by setting bit 6 of MISCSET to 1.
WTKIRQ	47	I-TPD	Weitek 3167 Interrupt Request, active high.
IRQ13	100	O	Interrupt Request 13, active high - This signal is driven to the Bus Controller to indicate that an error has occurred within the coprocessor. This signal is a decode of the –BUSY387 and –ERROR387 inputs ORed with the WTKIRQ input.
BUS CONTROL SIGNALS			
–CHREADY	104	I-CMOS	Channel Ready, active low - This signal is issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with ready signals from the coprocessor and DRAM controller to form the final version of –READYO which is sent to the CPU.
–CHS0/–MW	103	IO-CMOS	Channel Select 0/Memory Write, active low - This signal is a decode of the 386DX's bus control signals and is sent to the Bus Controller. When combined with –CHS1 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMW signal for DMA or Bus Master access to system memory.
–CHS1/–MR	102	IO-CMOS	Channel Select 1/Memory Read, active low - This signal is a decode of the 386DX's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMR signal for DMA or Bus Master access to system memory.
CHM/–IO	101	O	Channel Memory I/O - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and –CHS1 and decoded, the bus cycle type is defined for the Bus Controller.
–BLKA20	94	O	Block A20, active low - An output driven to the Bus Controller to deactivate address bit 20. It is a decode of the A20GATE signal and Port A bit 1 indicating the dividing line of the 1 Mbyte memory boundary. Port A bit 1 may be directly written or set by a read of I/O port EEh.
BUSOSC	106	I–TTL	Bus Oscillator - This signal is supplied from an external oscillator. It is supplied to the Bus Controller when the VL82C330's internal configuration registers are set for asynchronous slot bus mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUSCLK	98	O-TTL	Bus Clock - This is the source clock used by the Bus Controller to drive the slot bus. It is two times the AT bus clock (SYSCLK). It is a programmable division TCLK2 or BUSOSC.
DMAHRQ	105	I-CMOS	DMA Hold Request, active high - This signal is an input sent by the Bus Controller. It is internally synchronized by the VL82C330 before used to generate HRQ.
DMAHLDA	99	O	DMA Hold Acknowledge - An output sent to the Bus Controller that indicates that the current hold acknowledge is in response to DMAHRQ.
–BRDRAM	95	O	Board DRAM, active low - An output to indicate that on-board DRAM is being addressed.
OUT1	107	I-CMOS	Indicates a refresh request.
PERIPHERAL INTERFACE SIGNALS			
A20GATE	116	I-TTL	Address Bit 20 Enable - An input that is used internally along with Port A bit 1 to determine if A20 is passed through or forced low. It also determines the state of –BLKA20.
TURBO	115	I-TTL	Turbo, active high - This input to the VL82C330 determines the speed at which the system board operates. It is internally ANDed with a software settable latch. When high, operation is at full speed. When low, CLK2 is divided by the value coded in configuration register MISCSET. Turbo mode is active only when all TURBO requests are active.
–RC	114	I-TTL	Reset Control, active low - The rising edge of this signal causes a RESCPU signal.
SLEEP1	49	O-OD	Sleep Signal 1, active high - This pin is the logical OR of bits 7 and 1 of the SLEEP register. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive.
SLEEP2	50	O-OD	Sleep Signal 2, active high - This pin is the logical OR of bits 7 and 2 of the SLEEP register. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive.
SLEEP3	51	O-OD	Sleep Signal 3, active high - This pin is the logical OR of bits 7 and 3 of the SLEEP register. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive.
BUS INTERFACE SIGNALS			
XD7-XD0	86-93	IO-TTL	Peripheral Data Bus - This bus is connected to the Bus Controller and the VL82C330. It is used to transfer data to/from on-board 8-bit peripherals.
–DEN	53	O	Data Enable, active low - This signal is an output to the Data Buffer to enable data transfers on the local bus.
–IOR	112	I-TTL	I/O Read, active low - Indicates that an I/O read cycle is occurring on the bus.
–IOW	113	I-TTL	I/O Write, active low - Indicates that an I/O write cycle is occurring on the bus.
RSTDRV	111	I-CMOS	Reset Drive, active high - This signal is used to reset internal logic and to derive the RES386, and RES387.
–MDLAT	52	O	Memory Data Bus Latch - This is an output signal to the Data Buffer. On the rising edge, the Data Buffer latches the memory data bus. –MDLAT is low anytime one of the CASBK signals is high. When low, the Data Buffer latches are transparent.
OSC	110	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
TEST MODE PIN			
–TRI	48	I-TPU	Three-state - This pin is used to drive all outputs to a high impedance state. When –TRI is low, all outputs and bidirectional pins are high impedance.
POWER AND GROUND PINS			
VDD	1, 8, 31, 59, 68, 96	PWR	Power Connections, nominally +5 volts - These pins should each have 0.1 µF bypass capacitors.
VSS	14, 33, 45, 56, 61, 65, 70, 84, 97, 108, 128	GND	Ground Connection - 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type	Signal Code	Signal Type
I-TTL	TTL level input	O	CMOS and TTL level compatible output
I-TPD	Input with 30k ohm pull-down resistor	O-OD	Open drain, output
I-TPU	Input with 30k ohm pull-up resistor	O-TTL	TTL level output
I-CMOS	CMOS level input	IO-CMOS	CMOS level input/output
IO-TTL	TTL level input/ouput	GND	Ground
IC-OD	Open drain, output or CMOS input	PWR	Power

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATIONS

The sections that follow cover detailed operational information for the various logical groupings of VL82C330 subsystems. In most of these sections, the effect of configurable elements that can be controlled via internal I/O registers is discussed at length. Operation of the indexed I/O registers is repeated in summary form in the "Functional Summary of Indexed Registers" section. However, some lesser configurable functions are described only in that section. Do not assume that the information in that section is discussed elsewhere.

CPU INTERFACE

The VL82C330 handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the 386DX's bus status and address signals, and decodes the bus access. It then decides whether to handle the bus request itself, or send it off to the ISA Bus Controller.

Local Bus Accesses

The VL82C330 decodes the CPU bus signals and addresses. If the decode points to on-board memory, a bank request is issued to the on-chip DRAM Controller. The DRAM Controller then delivers the appropriate signals to on-board memory and returns a –READYO signal. –READYO may be combined with READY signals from the coprocessor or other external devices on the D bus to form the final –READY signal driven to the CPU.

If the system includes a cache controller, the VL82C330 allows the Cache Controller to perform posted write cycles to on-board memory. This allows the CPU to continue with local bus cache read hits after posting a cache write through to memory. The Data Buffer latches the write data via the Cache Controller's posted cache write clock. The Cache Controller then drives the CPU control signals to the VL82C330 notifying the DRAM Controller to write the data to memory.

Slot Bus Accesses

The CPU makes slot bus accesses when the VL82C330 decodes the CPU's control signals as either an I/O cycle, INTA cycle, or an off-board memory access (the latter includes ROM accesses). In this case, the VL82C330 latches and decodes the CPU's control signals and sends out bus cycle status signals to the Bus Controller. The Bus Controller handles control of the slot transfer. The CPU is prevented from executing another cycle until the slot cycle is completed. During a slot cycle, the –READY signal returned to the CPU from the VL82C330 is delayed until the Bus Controller notifies the VL82C330 that it has completed the data transfer via –CHREADY.

Other CPU Interface

Bus arbitration is handled with the VL82C330's DMAHRQ, DMAHLDA, OUT1, HRQ, and HLDA signals. When the VL82C330 receives an active DMAHRQ (DMA hold request) from the Bus Controller, it synchronizes the HRQ (hold request) signal with the CPU clock and relays it to the CPU. The CPU responds with HLDA (hold acknowledge) to the VL82C330 which then delivers DMAHLDA to the Bus Controller. When the system memory refresh timer expires, HRQ is sent to the CPU and HLDA is returned to indicate the CPU has given up the bus for refresh cycles.

Sixteen-bit transfers are handled by the Bus Controller. There is no –BS16 signal in the CPU interface. The Bus Controller decodes the –BE3- –BE0 and CPU control signals. If it detects a 32-bit read bus access to 16-bit I/O or memory, it starts an internal state machine. The state machine latches the necessary information and provides the consecutive bus cycle controls necessary to complete the 32-bit transfer. When four bytes have been delivered to the CPU's data bus, the Bus Controller notifies the VL82C330 via –CHREADY. The VL82C330 signals the CPU, which then reads its bus. For 32-bit slot bus write cycles, the Bus Controller returns –CHREADY only upon cycle completion. In this case, the CPU sees one bus cycle where there are normally two or more.

Reset control is supplied by the VL82C330. The VL82C330 contains the PS/2-compatible Port A. It contains a bit that can be set to cause a CPU reset. A second I/O address is provided to perform the same function. The latter option is supplied for Special Features compatibility. These two controls are combined with an RC (reset control) input and a RSTDRV (reset drive) hard reset to produce the synchronized RESCPU (CPU reset) delivered to the CPU. (Refer to the section "System Reset Options" for details.)

Coprocessor interface is also supplied by the VL82C330. If the system contains a coprocessor, the interface signals (–ERROR387, –BUSY387 and PEREQ387) are sent from the coprocessor to the VL82C330 and decoded to produce the proper interface signals for the CPU. This interface provides PC/AT-compatibility for use with the 387DX. This interface also supports the Weitek 3167.

BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION CHANNEL

The asynchronous interface to the ISA Bus Controller is handled by a group of signals from the VL82C330. –CHS0, –CHS1, and CHM/–IO define which type of cycle is to be excuted as in the table below.

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

ISA Bus Clock Control

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider	**Bus Clock Divider**	**Bus Mode**

The VL82C386 chip set is capable of supporting AT slot bus operation asynchronous with respect to the CPU clock. Though the ISA Bus Controller actually drives the slot bus, the VL82C330 is programmed for the specified mode and sources the required clock to the ISA Bus Controller. Whether synchronous or asynchronous modes, the VL82C330 synchronizes the command interface between itself and the ISA Bus Controller to BUSCLK.

BUSCLK is the AT bus clock provided to the ISA Bus Controller by the VL82C330. It runs at twice the final AT slot bus frequency. MISCSET, shown above, is one of the indexed configuration registers. The lower three bits control sourcing of BUSCLK to the ISA Bus Controller. Bit 0 sets synchronous or asynchronous mode. When set to 1, asynchronous mode is selected and the BUSOSC input is routed to the programmable divider. When set to 0, TCLK2 is output to the driver. Bits 1 and 2 of MISCSET provide for a programmable BUSCLK divider. Values of bit 1 and 2 provide for division from one to four, respectively. The programmable BUSCLK divider must be set to provide a BUSCLK of 2X the desired bus frequency. When a 16 MHz external oscillator is used, a ÷1 results in 8 MHz bus operation. Power-on reset defaults to ÷4, synchronous mode. See the section "Functional Summary of Indexed Registers" for more details.

Further programmability of bus timing is afforded by the ISA Bus Controller.

DRAM SUBSYSTEM DESCRIPTION

The VL82C330 supports up to 64 Mbyte of DRAM on the system board in four 32-bit banks. Each byte contains its own parity bit for a total of 36 bits per bank. A single bank can consist of 256K, 1M or 4M DRAMs.

The parts used in multiple banks can consist of all one DRAM type or mixtures of any two types. It is not possible to use all three types in a single system simultaneously and not all combinations of any two types are supported. The section "Page Mode/ Interleave Subsystem Overview" shows the valid options.

The VL82C330 supports four banks by providing four –RASBK signals, four CASBK signals, and four LBE lines. By applying the latter eight signals to four 74F00's, the 16 CAS lines required to drive four banks are generated.

Several configuration registers internal to the VL82C330 are used to control the memory map, DRAM timing and page mode. These features are discussed in the following sections. Since interleaving requires pairs of banks, various controls described next act on memory in bank pairs. The short hand notation Bank A is used when describing something that affects DRAM banks 0 and 1 as a set. Similarly, Bank B is used to describe DRAM banks 2 and 3 as a set.

Memory Maps

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (3)	ROMSLOT	1	1	**DRAM Memory Map Code**				

The VL82C330 supports 24 memory maps and two special cases. These maps are shown in Table 1. The table shows the DRAM combinations that are addressable in each of four 32-bit memory banks. The memory column shows the total system memory available in each memory map. The RAMMAP (4-0) column indicates the hex value written in bits 0 through 4 of the RAMMAP indexed configuration register in order to select each map. It should be noted that banks 0 through 3 in Table 1 refer to the "logical" banks as internally addressed by the VL82C330. The actual system board memory banks accessed by the internal signals may differ depending on the value stored in indexed configuration register RAMMOV. See the section "DRAM Remap Options" for more details.

TABLE 1. DRAM MEMORY MAPS SUPPORTED

Bank 0	Bank 1	Bank 2	Bank 3	Memory MB	RAMMAP (4-0)
256K				(1.38) 1.00	(1F*) 0
256K	256K			(2.30) 2.00	(1E*) 1
256K	256K	256K		3.00	2
256K	256K	256K	256K	4.00	3
1M				4.00	4
256K	1M			5.00	5
256K	256K	1M		6.00	6
1M	1M			8.00	7
1M	1M	256K		9.00	8
256K	256K	1M	1M	10.00	9
1M	1M	1M		12.00	A
1M	1M	1M	1M	16.00	B
4M				16.00	C
256K	4M			17.00	D
256K	256K	4M		18.00	E
1M	4M			20.00	F
1M	1M	4M		24.00	10
4M	4M			32.00	11
4M	4M	256K		33.00	12
256K	256K	4M	4M	34.00	13
4M	4M	1M		36.00	14
1M	1M	4M	4M	40.00	15
4M	4M	4M		48.00	16
4M	4M	4M	4M	64.00	17

*1Eh and 1Fh are special case memory maps. The 384K of DRAM above 640K are accessed as extended memory. EMS and shadow RAM are unavailable in this mode. Memory map 0h allows EMS and shadowing, but no extended memory. All other memory maps can support EMS, extended, and expanded memory as desired.

DRAM Remap Options

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMOV (04)	1	1	1	1	RAS - CAS Swap Code			

The RAMMAP register described in the previous section shows 26 distinct memory maps that are available in a TOPCAT-based system. Those are actually logical memory maps. The addition of the RAMMOV function provides 16 different ways to map the logical maps into the four possible physical DRAM banks. The combination of these two register functions provides a large number of unique ways to create a valid TOPCAT memory map. This capability provides two key features for the end user.

Easier DRAM Memory Upgrades

The physical DRAM banks need not be populated in the same order as would normally be dictated by the RAMMAP options alone. One example of when this is useful is the case where a system with one bank of 1M DRAMs is upgraded by adding a second bank of 256K DRAMs. Without the RAMMOV feature, it would be necessary to remove the 1M DRAM bank and move it to physical bank 1 then put the 256K DRAMs in physical bank 0. Using RAMMOV allows the 1M DRAMs to be left in place. The 256K DRAMs may be placed in any of the three available physical DRAM banks remaining. The proper RAMMOV code is then programmed so that the logical memory map (RAMMAP = 5h) is correctly routed to the proper physical DRAM devices.

DRAM Error Recovery

In case of a partial or total DRAM bank failure, the remaining functional DRAMs can be switched into an alternate, valid logical memory map by reprogramming RAMMOV and RAMMAP together.

Table 2 shows the 16 logical to physical mappings that are available. In the top row of this chart, the numbers 3, 2, 1, and 0 directly under "DRAM BANK MAPPING" refer to the four physical DRAM memory banks. In the 16 rows beneath, the code that must be programmed into the RAMMOV register bits 4-0 is shown on the left side of the chart. On the right side is shown the logical bank that is mapped to the corresponding physical bank shown in the top row.

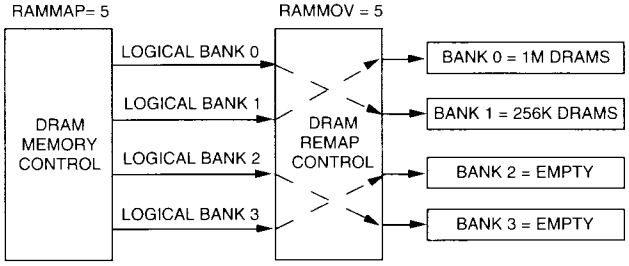
As an example, consider RAMMOV code 0001b shown in Table 2. Accesses to logical bank 3 are directed to physical bank 3. Accesses to logical bank 0 are directed to physical bank 2. Accesses to logical bank 2 are directed to physical bank 1. Accesses to logical bank 1 are directed to physical bank 0.

Note that when RAMMOV = 0000b, the default condition, the logical banks are directed to the same physical bank numbers.

TABLE 2. REMAP CONFIGURATION REGISTER CODE

RAMMOV Code				DRAM Bank Mapping				
D3	D2	D1	D0	3	2	1	0	Physical DRAM Banks
0	0	0	0	3	2	1	0	
0	0	0	1	3	0	2	1	
0	0	1	0	3	1	2	0	
0	0	1	1	3	0	1	2	
0	1	0	0	3	1	0	2	
0	1	0	1	2	3	0	1	
0	1	1	0	2	1	0	3	
0	1	1	1	2	0	1	3	Logical DRAM Banks
1	0	0	0	1	3	2	0	
1	0	0	1	1	2	3	0	
1	0	1	0	1	0	2	3	
1	0	1	1	0	3	2	1	
1	1	0	0	0	2	3	1	
1	1	0	1	0	2	1	3	
1	1	1	0	0	1	3	2	
1	1	1	1	0	1	2	3	

EXAMPLE: UPGRADING FROM ONE 1M DRAM BANK TO ONE 1M AND ONE 256K BANK



Page Mode/Interleave Subsystem Overview

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (05)	DRAM Drive		ESTART	RASDRV	Page Mode A	Page Mode B	Bank A Int	Bank B Int

In order to raise performance and decrease system cost, both page mode and interleave operation are available on the system board DRAM. Options are selected by programming of RAMSET and RAMMAP configuration registers. Page mode is enabled or disabled for each pair of DRAM banks independently. When on, it is active on all memory maps for the enabled bank pairs. Interleaving requires pairs of banks. Detailed operation of each is given in the following sections.

Interleave Operation

Two-way interleaving is automatically enabled whenever both banks of a pair are populated with like DRAM types. If all four banks are populated with like DRAMs, four-way interleaving automatically occurs if both bank pairs are programmed to interleave on the same bit. If not, two-way interleaving occurs. If the four banks are not populated with like DRAMs, two-way interleaving occurs on pairs that are of the same type. In a machine with three banks populated, the first two banks two-way interleave if they are of the same type. The third does not interleave. Table 3 shows the automatic interleaving options that occur versus the number of populated banks. All combinations not shown are unsupported. Table 3 also shows that 0, 1, 2, and 3 are the designations for each of the four DRAM banks. In the columns below these designators, "Yes" or "No", indicate whether the bank is populated. There is no configuration register programmability for enabling the interleave mode. All interleaving options (none, two-way, or four-way) occur automatically as the result of the memory map programmed into RAMMAP.

While the use of interleave is automatic and not programmable via the configuration registers, it is possible to select which bit is used for interleaving. Configuration register RAMSET bit 1 programs the Bank A interleave and bit 0 programs the Bank B interleave.

TABLE 3. AUTOMATIC INTERLEAVE VS MEMORY MAP

Bank 0	Bank 1	A Bank Address Mode	Bank 2	Bank 3	B Bank Address Mode
Yes	No	Linear	No	No	N/A
Yes	Yes	Two-Way Interleave	No	No	N/A
Yes	Yes	Two-Way Interleave	Yes	No	Linear
Yes	Yes	Two-Way Interleave 0 and 1*	Yes	Yes	2-Way Interleave 2 and 3*

*This is for the case where Banks A and B contain different types of DRAMs. For memory maps 03h, 0Bh, and 17h, all four banks contain the same DRAM type and four-way interleaving is used if both bank pairs interleave on the same bit.

When set to 0, interleave occurs on bit 2. This is called "word interleaving". When set to 1, interleave occurs on bit 11 regardless of DRAM types used. This is called "block interleaving". When all four DRAM banks are populated with like part types and bit 0 and bit 1 are set differently, two-way interleaving occurs. When they are the same, four-way interleaving occurs.

Tables 4, 5, and 6 show how the CPU address lines are used to accomplish the interleave options possible with the three supported DRAM types. The top portion of each table shows the CPU address lines that are strobed onto MA0-MA10 by CASBK, the column address strobe. The middle portion of each table shows the CPU address lines strobed onto MA0-MA10 by –RASBK, the row address strobe. The bank select box shows the CPU address bit(s) used for interleaving. The bank enable decodes further qualify whether the CPU address is in the range of current memory map.

Page Mode Operation

Interleaving operates independently of page mode. Once the desired interleave bits are set, the remaining interleave modes are automatically selected by the programmed memory map. Page mode control is given by two configuration register bits in the RAMSET register. Bit 3 = 1 enables page mode operation on DRAM banks 0 and 1. Bit 2 = 1 enables page mode operation on banks 2 and 3.

When activated for a bank pair, page mode is active whether one bank or both are populated. When four-way interleaving is active it is possible to have page mode active on either, neither, or both DRAM bank pairs. This does not impact the automatic interleaving, though it impacts performance.

When pairs of banks are installed, interleaving is automatically enabled. The combination of page mode with interleaving results in the best possible combination of fast system memory operation using the most cost-effective DRAMs. When accesses interleaved between banks occur, CASBK precharging of the next bank to be accessed occurs while CASBK is active on the current bank. This has the effect of multiplying the effective page size by the number of banks being interleaved, thus increasing the odds of page hit cycles.

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TABLE 4. 256K DRAM INTERLEAVE MAPPING

	No Interleave	Two-Way Block	Two-Way Word	Four-Way Block	Four-Way Word	Memory Address
Column Address	4	4	4	4	4	0
	5	5	5	5	5	1
	6	6	6	6	6	2
	7	7	7	7	7	3
	8	8	8	8	8	4
	9	9	9	9	9	5
	10	10	10	10	10	6
	2	2	11	2	11	7
	3	3	3	3	12	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Row Address	19	19	19	19	19	0
	18	18	18	18	18	1
	17	17	17	17	17	2
	16	16	16	16	16	3
	15	15	15	15	15	4
	14	14	14	14	14	5
	13	13	13	13	13	6
	12	12	12	21	21	7
	11	20	20	20	20	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Interleave Bits	–	11	2	11	2	
	–	–	–	12	3	
Bank Enable Decodes	20	–	–	–	–	
	21	21	21	–	–	
	22	22	22	22	22	
	23	23	23	23	23	
	24	24	24	24	24	
	25	25	25	25	25	

Note: For the 256K options: Bit 10 of the CA register = A13 for RAMMAP = 13; A12 for all others.
Bit 9 of the CA register = A11 for RAMMAP = 9, 13; A10 for all others.
Bit 10 of theRA register = A24 for RAMMAP = D, E; A23 for all others.
Bit 9 of theRA register = A22 for RAMMAP = 5, 6; A21 for all others.

TABLE 5. 1M DRAM INTERLEAVE MAPPING

	No Interleave	Two-Way Block	Two-Way Word	Four-Way Block	Four-Way Word	Memory Address
Column Address	4	4	4	4	4	0
	5	5	5	5	5	1
	6	6	6	6	6	2
	7	7	7	7	7	3
	8	8	8	8	8	4
	9	9	9	9	9	5
	10	10	10	10	10	6
	2	2	11	2	11	7
	3	3	3	3	12	8
	11	12	12	13	13	9
	–	–	–	–	–	10
Row Address	19	19	19	19	19	0
	18	18	18	18	18	1
	17	17	17	17	17	2
	16	16	16	16	16	3
	15	15	15	15	15	4
	14	14	14	14	14	5
	13	13	13	23	23	6
	12	21	21	21	21	7
	20	20	20	20	20	8
	21	22	22	22	22	9
	–	–	–	–	–	10
Interleave Bits	–	11	2	11	2	
	–	–	–	12	3	
Bank Enable Decodes	22	–	–	–	–	
	23	23	23	–	–	
	24	24	24	24	24	
	25	25	25	25	25	

Note: For 1 Megabyte options: Bit 10 of the CA register = A13 for RAMMAP = 15; A112 for all others.
Bit 10 of the RA register = A24 for RAMMAP = F, 10; A23 for all others.

TABLE 6. 4M DRAM INTERLEAVE MAPPING

	No Interleave	Two-Way Block	Two-Way Word	Four-Way Block	Four-Way Word	Memory Address
Column Address	4	4	4	4	4	0
	5	5	5	5	5	1
	6	6	6	6	6	2
	7	7	7	7	7	3
	8	8	8	8	8	4
	9	9	9	9	9	5
	10	10	10	10	10	6
	2	2	11	2	11	7
	3	3	3	3	12	8
	11	12	12	13	13	9
	12	13	13	14	14	10
Row Address	19	19	19	19	19	0
	18	18	18	18	18	1
	17	17	17	17	17	2
	16	16	16	16	16	3
	15	15	15	15	15	4
	14	14	14	25	25	5
	13	23	23	23	23	6
	21	21	21	21	21	7
	20	20	20	20	20	8
	22	22	22	22	22	9
	23	24	24	24	24	10
Interleave Bits	–	11	2	11	2	
	–	–	–	12	3	
Bank Enable Decodes	24	–	–	–	–	
	25	25	25	–	–	

Programmable Memory Timing

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RASTMA (07)	RAS ADDSEL	tRCD	tRP			tRAS		
CASTMA (08)	tCASW		tCST	tCP		tCASR		
RASTMB (09)	RAS ADDSEL	tRCD	tRP			tRAS		
CASTMB (0A)	tCASW		tCST	tCP		tCASR		

System board memory timing for this chip set is not specified in wait states. Instead, each of the critical DRAM timing parameters is specified as a number of programmable clock cycles. This allows virtually unlimited flexibility in matching DRAM specs to system CPU speed. The number of wait states for the system is whatever falls out of the programmed parameters. Banks A and B are programmed separately. This allows a user who later adds memory to maximize the speed advantage of faster parts when these chips are accessed. Conversely, a user can add slower parts for a cost savings without slowing down accesses to the entire memory system.

Four configurations registers are used to program the DRAM timing parameters. RASTMA allows programming of RAS ADDSEL delay, tRCD, tRP, and tRAS parameters for banks 0 and 1. RASTMB performs the same functions for banks 2 and 3.

FIGURE 2. –RASBK/CASBK TIMING MODEL

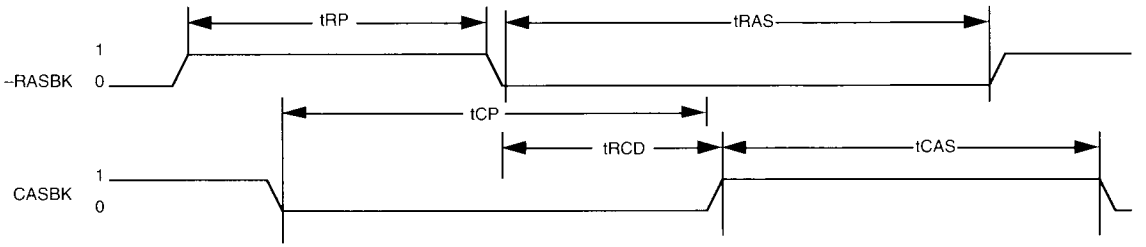
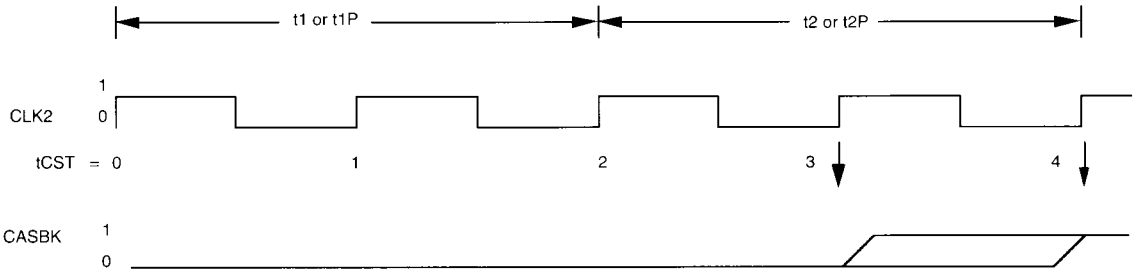
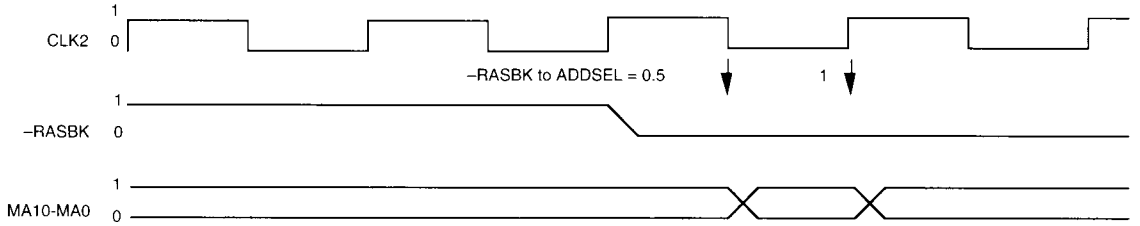


FIGURE 3. CASBK START TIME (tCST) TIMING MODEL



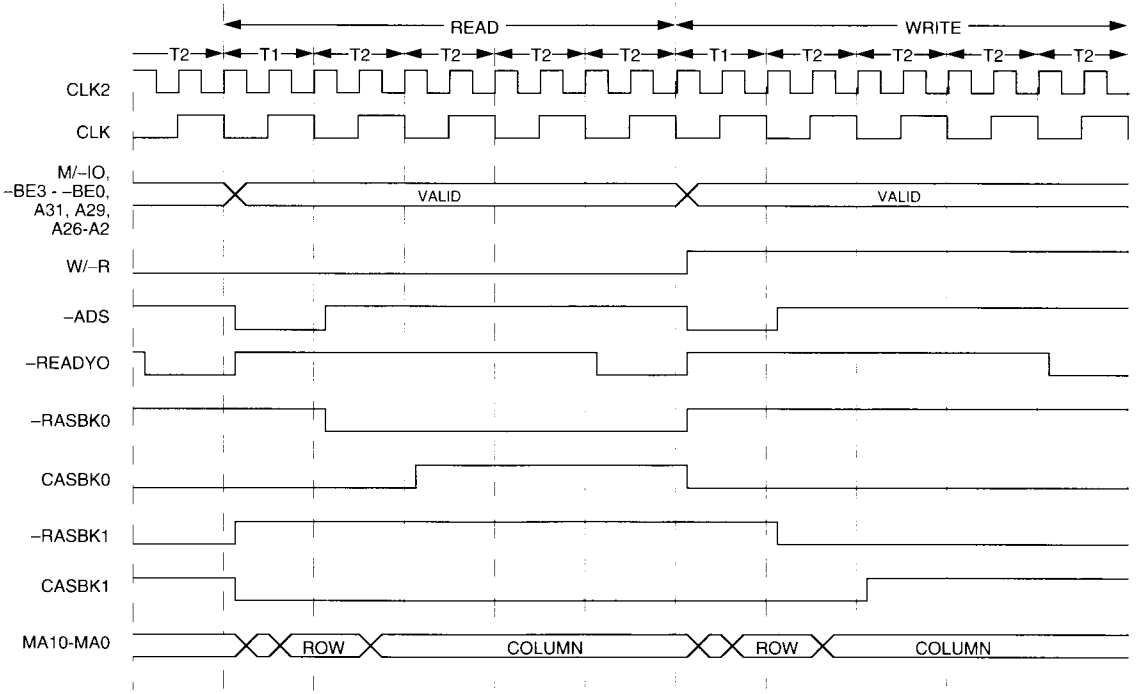
Note: tCST applies to write cycles only and always equals 3, or 4. During pipelined read cycles CASBK start time defaults to zero CLK2s if RAMSET bit 5 (ESTART) is programmed active (0) or one CLK2 if ESTART = 1. During non-pipelined read cycles, CASBK start time occurs at 2 or 3 depending on the state of the ESTART bit. These are the earliest times CASBK can start. Actual CASBK start time may be delayed due to CASBK pre-charge time or RAS to CAS delay time not yet met.

FIGURE 4. –RASBK TO ADDRESS SELECT TIMING MODEL



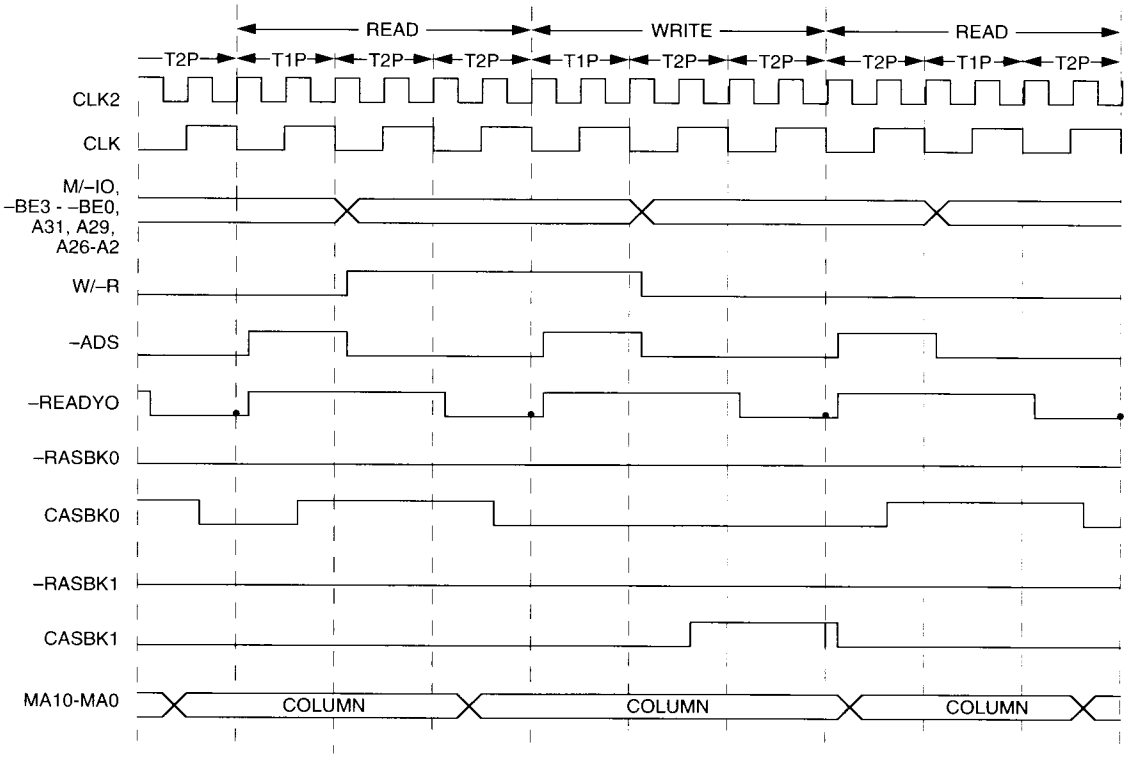
Note: Address Select can be programmed to switch MA lines 1/2 CLK2 or one CLK2 cycle after –RASBK.

FIGURE 5. NON-PAGE MODE, TWO-WAY INTERLEAVE, NON-PIPELINED



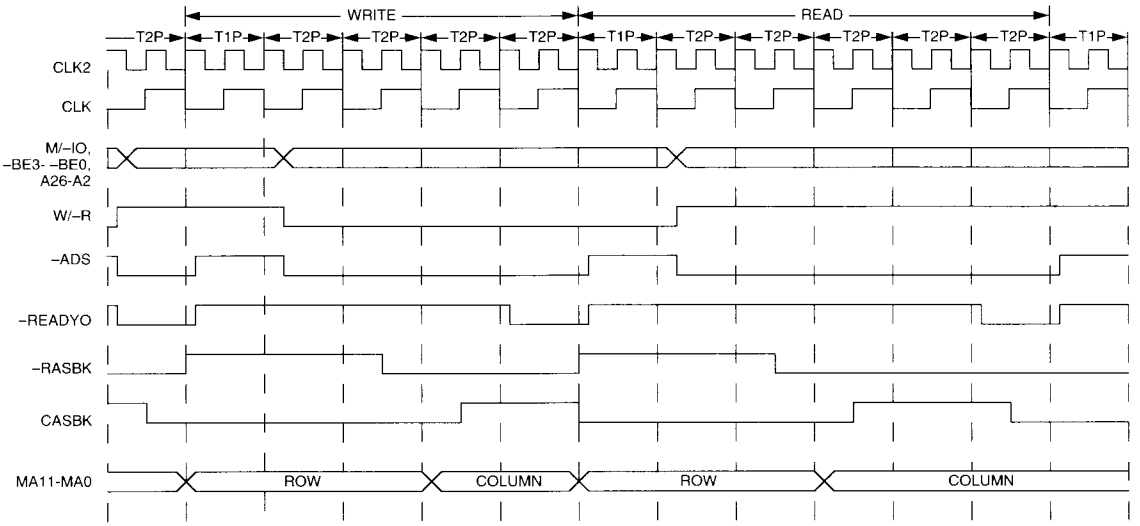
This diagram shows a read and write cycle with on-board memory on the MD bus. Signals shown are for a two-way interleaved cycle to the first two banks of system memory in non-pipelined mode. The –RASBK and CASBK signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET bit 5 (ESTART) is set active (0) in this diagram.

FIGURE 6. PAGE MODE, PAGE HITS, PIPELINED, TWO-WAY INTERLEAVED



This diagram shows read and write cycles for page mode, page hit operations. Two-way interleaving is shown on the first two memory banks for a pipelined cycle. The –RASBK and CASBK signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. Note here that RAMSET bit 5 (ESTART) is set inactive (1) and CASTMA bit 5 (tCST) is set to three CLK2s (0).

FIGURE 7. DRAM BLOCK TIMING - PAGE MODE ON (PAGE MISSES)



This diagram shows a read and write cycle for page mode, page miss operations. The –RASBK and CASBK signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. Note here that the VL82C330 is running in pipelined mode. The RAMSET bit 5 (ESTART) is active (0). RAS pre-charge time is set at five CLK2s, RAS to CAS (tRCD) delay time is set at two CLK2s (1).

Power-up Defaults

The DRAM system resets to a default state on power-up that allows any configuration to run, although it is a less than optimum state until BIOS or POST configures the registers with desired values. The defaults are:

- One bank of 256K DRAM
- Direct mapping from logical to physical DRAM banks
- Page mode on
- Timing for 100 ns DRAMs in 33 MHz system

Hold Request Arbiter

The hold request arbiter is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated by either DMAHRQ or OUT1 going active.

At the end of a hold request from either source, the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter gives an acknowledge signal to that source and leaves the HRQ line active. This continues as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold does the arbiter negate the HRQ signal and return control back to the CPU. The acknowledge to the DMA is via the VL82C330's DMAHLDA output. The acknowledge signalling for refresh is more complex due to the coupled and decoupled refresh modes. In coupled mode, an acknowledge occurs in the form of an active signal on the VL82C330's –REFRESH pin. A completely different mechanism is used in decoupled refresh mode. See the sections on "refresh" for details.

Programmable Refresh Control

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
REFCTL (06)	Decup	Slow Refresh Divider-System Board			10/16 IO	Slow Refresh Divider-Slots		

System Board DRAM Refresh

The VL82C330 performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. Refresh may be performed in a coupled mode or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the VL82C330 has complete control over the timing of on-board DRAM refresh and off-board refresh but the timing of each is independent.

When set to coupled refresh mode (D7 = 0), the VL82C330 refresh circuitry controls system board refresh and slot bus refresh in a synchronous manner. In that mode, the division specified by bits 0 to 2 applies to on- and off-board refresh and bits 4 to 6 have no effect. Only in decoupled mode (D7 = 1) do the three bits 4 to 6 of the VL82C330's REFCTL register apply. In decoupled mode, the VL82C330 refreshes the on-board DRAM independent of the Bus Controller's refresh of the slot bus resident memory. It uses the division rate specified in those bits while the slot bus refresh is performed at the rate specified by the code in bits 0 to 2.

Refer to the section "Sleep Mode Control Subsystem" for the range of refresh division mapped to the three bits 0 to 2 and the three bits 4 to 6.

Coupled Refresh Control
This is the PC/AT-compatible refresh mode. If bits 0 to 2 of the REFCTL register are set to their default value of 0h, the15 µs compatible timing is used. Other valid values, as specified in the section "Sleep Mode Control Subsystem," cause the refresh to occur at a slower rate in support of newer, low power, slow refresh DRAMs. These slower rates are all divisions of the normal 15 µs timer provided by the Bus Controller on pin OUT1.

In sleep mode, CASBK before –RASBK refresh may be used for on-board memory. This significantly reduces power requirements. The DRAMs generate their own refresh addresses internally. Therefore, the VL82C330 is not required to drive the memory address bus during refresh. When not in sleep mode, –RASBK-only refresh mode is used.

Decoupled Refresh Control
Decoupled refresh mode provides advantages to the user. It allows system board memory and slot memory to be refreshed at different rates. This is useful if slow refresh DRAMs are used in one location and not the other. More importantly, it lowers the refresh overhead rate. System board refreshes are performed during slot bus cycles. Therefore, it is not necessary to add refresh cycles and their attendant overhead. Similarly, when the VL82C330 instructs the Bus Controller to perform a slot bus refresh, it can then allow the CPU to continue execution. Only if the CPU requires a slot bus access during this time, will refresh overhead occur.

SLTPTR - Critical Memory Control Element

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLOTHI (01)	1	1	1	1	1	1	A25	A24
SLOTLO (02)	A23	A22	A21	A20	A19	A18	A17	A16

The two indexed configuration registers SLOTHI and SLOTLO in combination are referred to as SLTPTR. They represent a pointer to a 64K memory boundary between 256K and 64M. Ten bits are required to specify this range. They are used to compare to address lines A16-A25. SLTPTR sets the 64K boundary above which CPU addresses are directed to the AT slot bus. Any system board memory from 1 Mbyte up to SLTPTR is accessible as on-board extended memory. Slot bus DRAM extended memory resides from SLTPTR up to 16 Mbytes. If the SLTPTR is greater than 16 Mbytes, no slot accesses are made above SLTPTR since the required address lines for this capability are not available on the slot bus in an ISA system. The VL82C330 prevents aliasing of the slot bus extended memory space for CPU addresses above 16 Mbytes.

When the on-board EMS backfill system is disabled SLTPTR can also be set below 1 Mbyte. At least one bank of 256K RAMs must be on the system board on reset for a physical memory size of 1 Mbytes. The minimum valid value for SLTPTR is 0004h to allow slot memory cards, especially EEMS capable boards, to backfill down to 256K instead of using the built-in EEMS system. However, any value between 0004h and 0009h makes the portion of system board DRAM from that address to A0000H inaccessible when the on-board EMS system is inactive. The set of valid values for slot DRAM access is 0004h-03FFh.

Exceptions to the above are SLTPTR values 000Ah through 000Fh whose access is determined by the configuration of indexed registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS described in the "Shadow Ram Subsystem" and "Sleep Mode Control Subsystem" sections. Therefore, setting SLTPTR between 000Ah and 000Fh is treated the same as if the value were 0010h. Default = 03FFh indicates that no slot accesses occur.

Note: The slot pointer must point to 1M or higher (≥10h) if use of the EMS backfill registers is required. Pointing SLTPTR below 640K and using the backfill registers is incompatible. Therefore, any time the SLTPTR is set between 00h and 09h the EMS backfill register enable bit in configuration register EMSEN1 is cleared. A smart BIOS setup routine does not allow this condition in actual operation. See the section "Shadow Ram Subsystem" for more details. Also see the description of the additional memory control feature provided by CRTL17-CRTL6.

EMS Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
EMSEN1 (0B)	EMS Enable	BF Enable	Reserved	EMS MAP	B/EC000	B/E8000	B/E4000	B/E0000
EMSEN2 (0C)	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000

The EMS system consists of 72 mapping registers. They are split into a standard and alternate set of 36 registers each. The VL82C386 chip set supports the full LIM EMS 4.0 specification with any of the valid memory maps of 1 Mbyte and higher. The alternate register set allows rapid hardware context switching. Note that the VL82C386 chip set is capable of translating addresses via the EMS registers over the entire 32 Mbyte range of possible system board memory.

The EMS system is split into two parts, the 12 EMS page registers which cover the range from C0000h-EFFFFh and the 24 backfill registers that cover 40000h-9FFFFh. Bit D7 of configuration register EMSEN1 is a global enable for the EMS page registers. Each of the 12 registers can then be individually disabled if there are system address conflicts. Bits 0-7 of EMSEN2 and bits 0-3 of EMSEN1 provide this function. The 24 EMS backfill registers are enabled by setting bit 6 of EMSEN1. These registers are all enabled or all disabled. No individual control is provided. If a full LIM EMS 4.0 system is desired, both bits 6 and 7 of EMSEN1 are set as are the desired EMS page register enable bits. Note that when EMS enable, bit 7 = 0, the state of BF enable, bit 6, has no effect on the system.

The normal EMS page register mapping to C0000h-EFFFFh can be altered by changing EMSEN1 bit 4 from 0 to 1. In this case, the 12 page registers map to AXXXXh, DXXXXh, and BXXXXh in that order. In this case, EMSEN1 bits 3 through 0 work to enable or disable the BXXXXh registers rather than the EXXXXh registers. Similarly, EMSEN2 bits 3-0 work to enable or disable the AXXXXXh registers rather than the CXXXXh registers.

When the backfill EMS registers are not used, the EMS driver allocates all memory above SLTPTR for EMS page memory. It also can use the system board memory at the same addresses as the enabled EMS page registers and any other 16K segments in the A0000h-BC000h and F0000h-FC000h areas for which the shadow code is 00b as set in configuration registers AAXS, BAXS, and FAXS. When the backfill registers are active, EMS pages can also be allocated for all system board memory from 40000h-9FFFFh. There is no wasted DRAM in a VL82C386-based system. All memory not allocated for other purposes can be used as expanded memory.

The SLTPTR has critical effects on the EMS system. Only one effect is hardware related. When SLTPTR is set to a value from 0004h-0009h, bit 6 of EMSEN1 is cleared. This disables the EMS backfill registers. Placement of SLTPTR is otherwise used by the EMS driver to determine the area of memory that can be allocated for use as EMS pages. Table 7 summarizes the effect of SLTPTR on the EMS system.

The EMS driver also interacts with the shadow control system through configuration registers AAXS-FAXS. Any enable EMS page registers override the shadow control in their respective 16 Kbyte ranges. System board memory at the same address range as the EMS page registers can be allocated to the EMS memory pool by the EMS driver software. In addition, other non-EMS 16K segments can be allocated to the pool if they are not shadowed or otherwise in use. This is determined by the two shadow control bits for a specific segment. When the bits are 00b, the system board memory may be allocated to the pool. Table 8 summarizes the interaction between EMS and shadow control.

TABLE 7. EFFECT OF SLTPTR WITH EMS SYSTEM ENABLED

Slot Pointer Location	Effect
256K-640K	EMS backfill register automatically disabled. EMS page registers remain operational.
	CPU addresses 0-SLTPTR are on-board accesses.
	CPU addresses SLTPTR-16M are slot accesses.
	On-board memory > SLTPTR =EMS page memory.
640K-1M 000Ah-000Fh	Not allowed. Respond as if Slot Pointer=0010h. (See next case.)
1M-16M 0010h-0100h	CPU addresses 0-640K is system board (DOS) memory if backfill is not enabled, else 0-256K is system board memory.
	CPU addresses 1M-SLTPTR are system board extended memory accesses.
	CPU addresses from SLTPTR to 16M accesses slot bus, extended memory.
	EMS translation accesses system board RAM from SLTPTR to RAM top. System board RAM from 256 to 640K if backfill EMS is enabled.
16M-64M 0100h-03FFh	CPU addresses from 0 to SLTPTR are system board accesses.
	EMS translation accesses system board RAM from SLTPTR to RAM top. System board RAM from 256-640K if backfill EMS is enabled.

Note: Table 7 does not mention what occurs for accesses between A0000h and FFFFFh. When EMS is off, the result of CPU accesses to this memory region is determined solely by configuration of registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. When the EMS system is enabled, the active EMS registers between CXXXXh and EXXXXh override the settings in any areas that overlap the configurations in CAXS, DAXS, and EAXS. CPU addresses that fall in the realm of EMS register control are not directly passed to the slots or the system board. The addresses are translated and access reserved areas of system board DRAM above SLTPTR. Table 8 summarizes the rules that are followed for all cases.

TABLE 8. INTERACTION BETWEEN EMS AND SHADOW CONTROL

EMS Enable (Bit 7)	EMS Page Enable	Shadow Control		Effect
0	Don't Care	0	0	R/W slot bus or ROM chip selects.
		1	0	Read system board or write slot (shadow).
		1	1	R/W system board.
		0	1	Read slot or ROM chip selects, write system board.
1	0 (Note 1)	0	0	CPU accesses slots, EMS may access on-board DRAM.
		1	0	Shadowed, EMS does not use.
		1	1	Used by other resource, EMS driver does not allocate.
		0	1	Setup mode active. EMS driver does not allocate (Note 2).
1	1 (Note 3)	X	X	EMS overrides use of this area. CPU accesses translated by EMS. System board DRAM used by EMS memory pages.

Note 1: This case not only applies to the areas from C0000h-EFFFFh for which the EMS enable bit is turned off, but also to the A0000h-BFFFFh and F0000h-FFFFFh areas of memory.

Note 2: When an EMS driver is installed, this case should not exist. A shadow setup routine uses this code. It then changes it to 10b to enable the shadow feature. However, if an EMS driver sees this code, it does not allocate the system board DRAM in this area.

Note 3: In the areas where active EMS registers reside in the CXXXXh-EXXXXh area, the control bits are overridden. Any CPU accesses to this memory space are translated and the system board memory at these addresses is allocated to the EMS page memory pool.

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Table 9 shows a programmer's model of the register set. The register set is accessed by writing a command byte to the index register located at I/O address E8h. Bits D0-D5 contain the address of the desired EMS register from 0-35. Setting bit D6 to a 1 activates auto-increment. This feature is described in detail below. Bit D7 contains the desired register set to be accessed; the standard or the alternate set. I/O port addresses EAh and EBh then provide a window into the page register specified in the index register. Address EAh allows access to A14-A21. EBh allows access to A22-A25. Sixteen-bit I/O reads and writes can be used to gain access to A14-A25 in one operation via address EAh.

After initial accesses to port addresses at EAh and EBh, subsequent accesses are to the same page segment register until a new register number is written to the lower six bits of the index port at port address E8h or unless bit D6 of the index port was previously set to a logic 1. In this case, any access to port address EBh increments the page register number. (This new value is seen by a read to the index register port E8h.) The next read or write is to the next sequential page register. This feature allows the entire register set to be changed with a single access to the index register with either byte or word I/O access. For byte accesses, the lower byte at port address EAh must be written first. The access to the upper byte at EBh causes an auto-increment. Since all word accesses are made to port EAh, each one causes an auto-increment. This is due to the fact that the chip set actually breaks the word into two byte chunks, writing EAh followed by EBh.

The auto-increment feature speeds the already fast hardware driven context switching capability by minimizing the number of software instructions and, therefore, machine cycles required to read and save one context of the EMS registers, then retrieve and write another.

Configuration Enable/Disable
A write to port F9h with bit 7 of MISCSET = 0 cause EMS ports E9h, EAh, and EBh to become read-only until a write to port FBh occurs. E8h remains read/write. This allows the EMS Data Registers to be read but not modified. More information on this feature is available in the "Dedicated Internal Control Registers" section.

TABLE 9. EMS INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
	Set #	Auto-inc	A5	A4	A3	A2	A1	A0
	0 = Std 1 = Alt	0 = Off 1 = On						

Data Port	Page Segment	Data Port EBh								Data Port EAh							
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	C0/A0	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1	C4/A4	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
2	C8/A8	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
3	CC/AC	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
4	D0000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
5	D4000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
6	D8000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
7	DC000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
8	E0/B0	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
9	E4/B4	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
A	E8/B8	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
B	EC/BC	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
C	40000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
D	44000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
E	48000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
F	4C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
10	50000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
11	54000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
12	58000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
13	5C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
14	60000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
15	64000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
16	68000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
17	6C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
18	70000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
19	74000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1A	78000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1B	7C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1C	80000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1D	84000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1E	88000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1F	8C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
20	90000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
21	94000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
22	98000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
23	9C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14

Note: A 1 indicates reserved bits that read back as logic 1.

Shadow RAM Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	

Six indexed configuration registers are provided to give complete control over each of the 64K memory segments between 640K and 1M. The registers are called AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. Each register contains two bits for each 16K paragraph in the 64K segment controlled by that register. Refer to the section "Functional Summary of Indexed Registers" for more details.

The four modes provided are:

1. Normal PC/AT-compatible operation. This is R/W slot bus or ROM chip select depending on the memory space.
2. R/W system board DRAM. This allows complete access to DRAM in the given 16 Kbyte region.
3. Read-only DRAM. This is the normal shadow operational mode though it could be used to protect data previously written to a memory area while configured for mode 2. In this mode, writes are directed to the slot bus.
4. Shadow setup mode. In the E000 and F000 segments, reads cause on-board ROM chip selects and writes to the same address are to system board DRAM. In the segments A000-D000, reads are from the slot bus and writes are to the system board DRAM. This allows shadowing of system board ROM as well as ROMs on a slot card.

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Middle BIOS Alias Control

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider	Slot Bus Divider	Bus Mode

Bit 5 of the MISCSET indexed configuration register is used to enable the middle BIOS region (00FE0000h-00FFFFFFFh). When the bit is a 0, this address space produces a –ROMCS. This setting is the power-on reset default. When the bit is set to logic 1, accesses to this address range are directed to the system board DRAM.

The middle and upper BIOS spaces are never shadowed.

NUMERICAL PROCESSOR INTERFACE

The VL82C330 supports both the Intel 387DX and the Weitek 3167 numeric coprocessors for use in high performance floating point math applications.

Intel 387DX

The VL82C330 contains several dedicated pins in order to provide the interface between the 387DX and the 386DX. The 386DX and 387DX are designed to interface directly without external logic. However, logic is required in order to make a system hardware compatible with the PC/AT and software compatible with the PC/AT and original IBM PC. The following sections describe the interface logic broken into several parts.

System Reset Logic

System reset is an internally generated signal caused by a reset signal to the VL82C330 (RSTDRV), usually in response to the POWERGOOD signal. This signal initiates a reset to the CPU and to the 387DX.

CPU-Only Reset Logic

A CPU reset without a coprocessor reset can occur for one of two reasons. The first is usually done in order to switch from protected to real mode. The signal which causes it is shown as "Hot" reset. It is triggered by setting bit 0 of I/O port 92h to a 1, by a read of I/O port EFh, or by receipt of an external –RC signal. The latter signal causes a CPU-only reset as soon as received. There is a 6.72 µs delay between the occurrence of either of the first two events and activation of the RESCPU signal.

Internal detection of a shutdown command from the CPU also triggers a CPU-only reset.

In both of the above cases, reset is also synchronized to CLK2 and lasts for 16 CLK2 cycles.

387-Only Reset Logic

For PC/AT-compatibility, a 387-only reset is provided via a I/O write to F1h. This action provides a reset to the 387DX synchronized to CLK2 of 80 CLK2 cycles duration. –READYO does not go active after the write to F1h for 100 CLK2 cycles after the falling edge of RES387. There may be incompatibility with some software due to the fact that a hardware reset does not put a 387DX into the same internal state as does a reset of the 287. For this reason, the F1h reset function may be disabled by setting bit 6 of register MISCSET = 1.

Error/Interrupt Logic
For PC/AT-compatibility, –ERROR387 active generates interrupt 13. It also latches –BUSY386 active. This later action is required in order to prevent the 386DX from attempting to use the coprocessor until the error handling interrupt routine is executed. The interrupt handler clears the latched –BUSY by performing a write to I/O port F0h.

Busy Logic
The –BUSY386 signal can be produced from four sources. It always occurs in response to the –BUSY387 input. It also occurs as latched by the –ERROR387 signal. In the third case, a toggle busy logic block can drive it. This block is required for compatibility with software that uses non-standard instructions to detect the presence of a coprocessor. When a coprocessor is not present, –BUSY386 is pulsed active for 16 CLK2 cycles whenever an I/O cycle is detected with A31 high.

Busy test logic is invoked only on system reset. At this time, the 386DX self-test mode is triggered. This adds 33 ms at 16 MHz and 16 ms at 33 MHz to the CPU reset time. At the end of the self-test, the BIOS can read the CPU self-test result register and perform whatever function is desired on failure. Note that when a CPU-only reset is invoked, this self-test is not performed. Therefore, "Hot" resets are performed as fast as possible.

PEREQ Logic
The PEREQ387 signal is always passed directly to the PEREQ386 pin. In addition, PEREQ386 is driven and held active as soon as –BUSY387 goes inactive after occurrence of an active –ERROR387 signal. Control of the PEREQ386 signal to follow the PEREQ387 signal is performed by a write to I/O port F0h.

387DX Ready Control
On reads or writes to the 387DX's I/O space, the VL82C330 automatically asserts –READYO to the 386DX processor after one wait state unless the –READYI line to the VL82C330 is asserted before the end of one wait state. This prevents a separate hang-up when a 387DX is not present.

Weitek 3167
The Weitek 3167 is a more powerful numeric coprocessor than the 387DX. It uses a superset of the 387DX pins. It is a memory mapped device and uses all 32 address lines to decode a space from C0000000h-C1FFFFFFh. The fact that it is not a standard part causes no backward compatibility issues. As such, it interfaces easily to the system. Two signals are provided on the VL82C330. WTKIRQ is used to OR this interrupt with the IRQ13 line for the 387DX. –READYI is required for any external add-in devices including a cache controller. If more than one external source of –READYI exists, they must be externally ORed.

DEDICATED INTERNAL CONTROL REGISTERS
All Special Features (SF) decodes are between E8h and FFh as shown in Table 10. While the IBM Technical Reference Manual considers F8h-FFh reserved for coprocessor use, only F8h, FAh, FCh, and FEh are actually used. SF sandwiches some registers in this region. The recommended method is to decode the F8h-FFh range then AND with address bit –A0. This properly maps only the even addresses in this range to the coprocessor. I/O ports F0h and F1h are fully decoded due to the presence of other ports at F4h and F5h. It is possible to disable the SF functions mapped in the FXh range if they conflict with a specific design implementation. This feature is described later in this specification.

Note: The dedicated I/O registers at E8h, EAh, and E9h are described separately in the "EMS Subsystem" section. The dedicated I/O registers at ECh and EDh are described in the "Functional Summary of Indexed Registers" section.

TABLE 10. DEDICATED I/O CONTROL REGISTERS

Port Address	Function
E8h	EMS Index Register
E9h	EMS Active Set
EAh	EMS Data Port Low Byte
EBh	EMS Data Port High Byte
ECh	Configuration Index Register
EDh	Configuration Data Port
EEh	Fast A20* **
EFh	Fast Reset* **
F0h	Coprocessor Busy Clear
F1h	Coprocessor Reset
F4h	Slow CPU**
F5h	Fast CPU**
F8h	Coprocessor
F9h	Configuration Disable**
FAh	Coprocessor
FBh	Configuration Enable**
FCh	Coprocessor
FEh	Coprocessor

* Also can be activated through port 92h for PS/2-compatibility.

** These decodes can be disabled in case of conflict.

Note: All I/O accesses to the above registers must be byte size except the EMS data port (EAh and EBh) which may be either byte or word operation.

EMS Register Set (I/O Address E9h)

E9h	D7	D6	D5	D4	D3	D2	D1	D0
EMS Register Set	1	1	1	1	1	1	1	1

A read of this address returns FFh. A read of this register also activates the standard EMS register set. A write activates the alternate EMS register set. Neither of these actions has any effect if the EMS subsystem has not been enabled by setting the EMS enable bits in the EMSEN register described in the "EMS Subsystem" and "Functional Summary of Indexed Registers" sections. Default on reset is the standard register set.

Note: This function has no relationship and is totally independent of the control afforded by bit 7 of register E8h. Bit 7 controls which register set is selected for updates to the base addresses for the EMS translation. It is possible to select and update either the standard or alternate EMS register set independent of which set is currently active. After a write to port F9h when bit 7 of the MISCSET the register = 0, E9h becomes read-only until a write to port FBh is performed.

Fast A20 (I/O Address EEh or 92h)

EEh	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	1	1	1	1	1	1	1	1

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	Reset

A read of I/O port EEh enables Fast A20 and returns a value of FFh. A write disables Fast A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the Keyboard Controller to control A20. Internally, this signal and A20GATE are ORed so that either event controls the A20 address line and generates –BLKA20. Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the A20 input for strict PC/AT-compatibility.

Fast A20 is also controlled via bit 1 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 1 = 1, A20 is active. When bit 1 = 0, A20 always = 0. This feature is fully integrated with the Fast A20 control achieved through EEh, i.e. a read of EEh followed by a read of bit 1 of port 92h returns a logic 1.

After a write to port F9h when bit 7 of the MISCSET the register = 0, EEh becomes read-only until a write to port FBh is performed. If bit 7 of register MISCSET = 1, EEh can not be read or written.

Fast CPU Reset (I/O Address EFh or 92h)

EFh	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	Reset

This register provides an alternative to use of the –RC input in order to reset the processor. A read of EFh resets the processor. This reset signal must be ORed internally with the –RC input so that either event invokes a reset. This may provide a faster way for the system to jump between real and protected mode. Reset timing is the same as described below for the Port A reset.

Fast CPU reset can also be controlled via bit 0 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 0 = 1, a reset operation is triggered. Reset pulses are high for 16 CLK2s. This latch remains set until written again or until the VL82C330 is externally reset.

After a write to port F9h when bit 7 of register MISCSET = 0, EFh becomes read-only until a write to port FBh is performed. If bit 7 of the MISCSET the configuration register = 1, EFh can not be read or written.

Note that in order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low, otherwise, the reset vector is not fetched and the system hangs up. Therefore, before issuing a "Hot" reset command, either via I/O port 92H or I/O port EFh as described above, one of the following must occur:

1. Set bit 1 to 1 in Port A. (Writing 03h to this register effectively accomplishes both goals with a single I/O instruction.)
2. Perform a read of EEh to enable A20.

Coprocessor Control (I/O Address 0F0h and 0F1h)

0F0h	D7	D6	D5	D4	D3	D2	D1	D0
Clear/Busy	X	X	X	X	X	X	X	X

0F1h	D7	D6	D5	D4	D3	D2	D1	D0
Reset Copro	X	X	X	X	X	X	X	X

A write to I/O port F0h clears the D-flop which holds –BUSY386 and PEREQ386 active after an –ERROR387 signal occurs. A write to I/O port F1h resets the 387DX. This write results in a positive pulse 80 CLK2 cycles wide and is synchronized to CLK2. –READYO is held inactive during this entire period for 100 CLK2s after the falling edge of RES387.

Bit 6 of MISCSET must be set to 0, otherwise a write to F1h does not cause a reset.

CPU Speed (I/O Address 0F4h and 0F5h)

0F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU Speed	X	X	X	X	X	X	X	X

0F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU Speed	X	X	X	X	X	X	X	X

A write to Port 0F5h causes the CPU to run at normal "fast" speed. A write to Port 0F4h invokes the CLK2 divider circuit. This is selected by writing the appropriate code to the MISCSET register described later in this document. The programmable range provided allows 12 to 33 MHz systems to run at or below 8 MHz. Default on reset is "fast" speed.

If bit 7 of the MISCSET register = 1, this CPU speed feature is disabled. See the description under MISCSET in the section titled "Functional Summary of Indexed Registers" for more details. The speed control activated by the BIOS through the keyboard controller is always available to access this function.

Configuration Enable/Disable Registers (I/O Addresses 0FBh and 0F9h)

0FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

0F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described above, the configuration registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to 0FBh enables the configuration registers. A write to 0F9h disables the configuration registers. When disabled, the registers in range E8h to EFh are read-only except for E8h and ECh which remain read/write. This allows the EMS data registers and the configuration registers to be read but not modified.

If bit 7 of the MISCSET register = 1, the configuration enable/disable feature is disabled. See the description under MISCSET in the section "Functional Summary of Indexed Registers" for more details.

Sleep Mode Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP (13)	Enable	Power Down CLK2 Divider			Ext Ctrl 3	Ext Ctrl 2	Ext Ctrl 1	SYSCLK

Sleep mode operation is provided for battery operated laptop microcomputer support. The sleep indexed configuration register is provided to control this function. Bits 0, 4-6 are set with the desired values by the BIOS on POR. Then only bit 7 needs to be toggled to get in and out of sleep mode during operation. Bits 1-3 also have a special, optional function which may require control in the course of an operating session. For maximum power savings, it is recommended that a halt instruction be executed immediately after setting bit 7. Any interrupt brings the CPU out of halt mode.

Bit 7 is set to 1 to invoke all chip set sleep functions. When set, CLK2 is divided by the value coded in bits 4-6 of the sleep register. These bits provide a code used to divide the CLK2 down for sleep mode. Division from 2 to 64 is programmable. The range is specified in the "Functional Summary of Indexed Registers" section.

When used with non-static CPU's the greatest division is selected that remains above the minimum operational frequency.

Normally, –RASBK-only refresh is performed. This requires driving the memory address lines and power is consumed. When bit 7 = 1, the Refresh Controller switches to CASBK before –RASBK refresh. If CASBK before –RASBK refresh is not desired while in sleep mode, setting bit 6 of CTRL1 = 1 maintains standard refresh operation.

The VL82C330 is brought out of sleep mode by resetting bit 7 to a logic 0. This can be done by providing a hardware reset to the VL82C330 or by a CPU write of 0 to bit 7. A hardware reset or an INTA cycle of the VL82C330 also resets this bit.

Bits 1-3 provide for software control of an external device. The state of each bit is ORed with bit 7 and the ORed output is connected to an external pin on the VL82C330. This causes the external pin to be active whenever the sleep mode is active (high) or whenever bit 1 is set high.

Bit 0 - The sleep register is "shadowed" in the Bus Controller. That is; it exists at the same address as a write-only register in the Bus Controller. However, only bits 0 and 7 are valid in the Bus Controller. See the VL82C331 ISA Bus Controller data sheet for more details. In the VL82C330, bit 0 is a read/write bit without function. This bit is provided so that software can detect the last state written to it in the Bus Controller.

When bit 1 of CTRL1 = 0, the –SLP/MISS (pin 6) provides an external indication of the inverse state of bit 7 of the SLEEP register. That is, when pin 6 is low, sleep mode is active. This can be used as an external indicator of sleep mode or as an external sleep mode activation signal for other devices.

See sleep mode operation in the VL82C331 ISA Bus Controller data sheet and in the section "Sleep Mode Control Subsystem" in this data sheet for additional information.

Turbo/Slow CPU Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider		Slot Bus Divider		Bus Mode

It has become standard for fast PC/AT-compatibles to provide means to slow operation for older, speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. Bits 3-4 of the MISCSET indexed configuration register are used to specify a CLK2 divider that is active when the slow CPU mode is activated. This range provides the capability to operate at 8 MHz or under, for any actual CPU speed from 12 to 33 MHz.

One way this mode may be toggled on and off is by external control of the TURBO input pin. When TURBO is low, the slow mode is activated and the CLK2 divider is in effect. When TURBO is high or during HLDA cycles, CLK2 runs at the same speed as TCLK2 (only if the SF TURBO request is also active, see above). The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a "hot key" combination such as Ctrl Alt +. This input is often externally ANDed with a mechanical turbo switch on the front panel.

For SF compatibility, another method is provided if separately enabled. A write to I/O port 0F4h also selects the CLK2 divider circuit for slow operation. A write to 0F5h returns to full speed operation. The SF must be enabled (bit 7 of MISCSET = 0) for the latter mechanism to be active. The SF internal speed control mechanism is ANDed with the TURBO input pin. In this way, any single request for slow operation causes it to occur.

Note: The state of TURBO has no impact on the slot clock frequency. See the sections "Functional Summary of Indexed Registers" and "Dedictated Internal Control Registers" for additional data.

SPECIAL CYCLES

HALT/SHUTDOWN DETECTION

The VL82C330 detects and responds as described below to halt and shutdown operations from the CPU.

The chip set detects halt only to differentiate it from the shutdown cycle. No further action is taken in response to halt except to acknowledge it by asserting –READYO after two wait states.

Shutdown is handled differently. This bus cycle is executed by the CPU in response to a critical internal processing error. The VL82C330 responds by asserting –READYO after two wait states, then issuing a CPU-only reset for 16 CLK2 cycles.

ISA CYCLES

The VL82C330 provides no time-out feature for ISA bus cycles. The ISA Bus Controller performs these cycles based on the programmed number of wait states. There is no limit enforced on IOCHRDY.

MEMORY CYCLES

Memory cycles above on-board memory below 16M are passed to the ISA bus. Cycles above on-board memory and above 16M are handled by the VL82C330 which generates a –READYO after two wait states.

TABLE 11. 386 HALT/SHUTDOWN DETECTION

D/–C	W/–R	–BEO	Mode
0	1	1	Halt
0	1	0	Shutdown

Memory mapped devices in the region, therefore, have two wait states to decode this cycle as their own and gate off the VL82C330's –READYO signal before it becomes the system ready signal.

COPROCESSOR CYCLES

When the VL82C330 detects a memory access to the Weitek 3167 memory space, it generates a –READYO in approximately 7.5 µs if it does not receive a –READYI signal within this time.

When the VL82C330 detects a 387 NPX access, it generates a –READYO signal in one wait state if a –READYI signal is not received.

ROM CYCLES

With power-on-reset defaults, three address regions result in generation of –ROMCS and access of ROM data on the MD bus. These are:

1) 000E0000h-000FFFFFh
   Accesses can be altered via EAXS, FAXS, EMSEN1, or bit 7 of RAMSET. See detailed discussions of these actions elsewhere in the data sheet.
2) 00FE0000h-00FFFFFFh
   ROM access to this range can be disabled by setting bit 5 of MISCSET = 1. This is required in systems having more than 16M of on-board DRAM, optional otherwise.
3) FFFE0000h-FFFFFFFFh
   Because not all 32 CPU addresses are input to the VL82C330, a partial decode results in a wider range of ROM cycle access. See Table 11A for more information.

Timing of ROM cycles is handled by the VL82C331 ISA Bus Controller. See the "ROM Access Control" subsection paragraph of that specification for further information.

SYSTEM RESET OPTIONS

This section describes all reset modes of the VL82C330 based on their activating signal. They have been discussed in other applicable sections of this document and are summarized as an aid the reader.

RSTDRV: Hardware reset pin from the ISA Bus Controller. This signal causes all internal state machines to be reset. The internal configuration registers are reset to their default values shown in Table 12. Resets are issued to the 386 and the 387. The –BUSY386 signal is active for at least eight CLK2 cycles before and after the falling edge of the RES386 signal. This invokes the self-test mode of the 386DX. Systems that desire to use this feature can then read the result of this test in the 386DX's EAX register and decide what to do based on the result. Otherwise, it can be ignored.

–RC: When active, a CPU-only reset is issued immediately on RES386 for 16 CLK2 cycles synchronous with CLK2.

REG_92: Setting bit 0 of I/O port 92h causes a 386-only reset. After approximately 6.75 µs, a RES386 is activated

TABLE 11A. TOPCAT VL82C330 SYSTEM RESPONSES TO ADDRESS SPACE ABOVE 16 MBYTES

A31	A30	A29	A28	A27	A26	A25-A0	System Response until READYO Generation
0	X	0	X	X	0	X	Programmed ws in memory map, ELSE*
0	X	0	X	X	1	X	*
0	X	1	X	X	X	X	*
1	X	0	X	X	X	X	*
1	X	1	X	X	1	3FE0000–3FFFFFF	Ready in 8.4 µs if no prior 3167 READY+ –ROMCS, ROM cycle for programmed ROM ws

* Accesses in these areas alias to the ISA bus below 16M in the VL82C330A series devices. In the VL82C330 series parts, –READYO is generated after two wait states and no further action is taken.

\+ This region is decoded as Weitek 3167 accesses. In the VL82C330A series parts, a system READY is generated ater 8.4 ms unless the first attempted access to this space results in an externally generated READY prior to time-out. In this latter case, the VL82C330A generates no READY for accesses to this region. The effect of this method is to allow the Weitek to generate all of its own READYs when it is present in a system. In the absence of a 3167, the VL82C330A generates READY after the 8.4 µs time-out in order to prevent system hang-ups. In VL82C330 series parts, –READYO is always generated after 8.4 ms unless an external READY occurs before the time-out.

for 16 CLK2 cycles. See the section "Dedicated Internal Control Register" for more details.

REG_EF: A read of I/O port EFh causes a 386-only reset. After approximately 6.75 µs, a RES386 is activated for 16 CLK2 cycles. SF must be enabled for this feature to function. See the section "Dedicated Internal Control Register" for more details.

OUT_F1: A write to I/O port F1h causes an 387-only reset. RES387 is activated for 80 CLK2 cycles. Ready assertion is held off for another 100 CLK2 cycles. See the section "Dedicated Internal Control Registers" for details.

SHUTDOWN: Detection of the shutdown condition causes a 386-only reset for 16 CLK2 cycles. See the section "Halt/Shutdown Detection" for additional information.

IN-CIRCUIT TEST LOGIC

The VL82C330 is designed to make system board testing as easy as possible. The –TRI input causes all pins on the VL82C330 go to a high impedance state. This can be used to isolate the VL82C330 so other components in the system can be tested.

The –TRI input can also be used to put the VL82C330 into a special test mode called In-Circuit Test (ICT). The purpose of ICT is not to functionally test the VL82C330 while it is inserted in a circuit board, but to test that the part is connected correctly and all the pins can be toggled high and low in a predictable pattern.

IN-CIRCUIT TEST DESCRIPTION

ICT INPUT		ICT INPUT		ICT INPUT		ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
A17	2	A14	5	A11	9	A8	12	–REFRESH	109
A16	3	A13	6	A10	10	A7	13	–CHS0/–MW	103
A15	4	A12	7	A9	11	A6	15	–CHS1/–MR	102
A5	16	A3	18	–BE3	20	–	–	CLK2	32
A4	17	A2	19	–BE2	21	–	–	–SLP/MISS	35
–BE1	22	D/–C	25	HLDA	28	–	–	–ERROR386	37
–BE0	23	M/–IO	26	–READYI	29	–	–	–BUSY386	38
W/–R	24	–ADS	27	CLK2IN	30	–	–	PEREQ386	39
–READYO	34	RES387	41	–ERROR387	43	PEREQ387	46	HRQ	40
RESCPU	36	–BUSY387	42	TCLK2	44	WTKIRQ	47	SLEEP1	49
–RAMW	52	MA10	57	MA7	62	–	–	SLEEP2	50
–DEN	53	MA9	58	MA6	63	–	–	SLEEP3	51
–MDLAT	55	MA8	60	MA5	64	–	–	–ROMCS	54
MA4	66	LBE2	74	CASBK0	80	–	–	XD7	86
MA3	67	LBE1	75	–RASBK3	81	–	–	XD6	87
MA2	69	LBE0	76	–RASBK2	82	–	–	XD5	88
MA1	71	CASBK3	77	–RASBK1	83	–	–	XD4	89
MA0	72	CASBK2	78	–RASBK0	85	–	–	XD3	90
LBE3	73	CASBK1	79	BUSCLK	98	–	–	XD2	91
–CHREADY	104	BUSOSC	106	OSC	110	–	–	XD1	92
DMAHRQ	105	OUT1	107	–IOR	112	–	–	XD0	93
–IOW	113	TURBO	115	A31	117	–	–	–BLKA20	94
–RC	114	A20GATE	116	A29	118	–	–	–BRDRAM	95
A26	119	A23	122	A20	125	–	–	DMAHLDA	99
A25	120	A22	123	A19	126	–	–	IRQ13	100
A24	121	A21	124	A18	127	–	–	CHM/–IO	101

During ICT, each output may be toggled by one or more of the inputs. This allows for a board level tester to check the solder connection of each pin. The sequence for enabling ICT is as follows:

1. Tester drives –TRI pin low.
2. Tester drives XD0 with a value of 1.
3. Tester simultaneously pulses –IOR and –IOW low for at least 100 ns.
4. Tester drives –TRI pin high.
5. VL82C330 remains in ICT mode until the RSTDRV pin is activated or until steps 1-4 are repeated with XD0 = 0.

CONFIGURATION REGISTER SET

SOFTWARE ACCESS

Index Registers (I/O Address ECh)
The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address EDh. All subsequent data port reads and writes accesses the register at this address until the index register is written with a new 8-bit address. This register is readable. It always returns the last value written to it.

The Configuration Registers can only be accessed via the CPU and are limited to byte reads and writes.

Data Port Register (I/O Address EDh)
Each register accessible through I/O address EDh is functionally described below. It is accessed first by writing its address to the index register at I/O address ECh, then by accessing the data port at I/O address EDh.

FUNCTIONAL SUMMARY

Indexed Registers

Version (00h) (Read-only)
D2-D7 contains a read-only code which indicates that this part is a VLSI Technology PC/AT-compatible VL82C330. D0 and D1 contain the version number of this chip. The first production version of this chip uses the code F2h. Breaking the code into two bit pieces reveals it to be "330" Rev "2."

SLOTHI and SLOTLO (01h and 02h) (Default = FF,FF)
These two registers represent the upper address bits of the base address where off-board (slot) memory accesses begin. In combination they are referred to as SLTPTR. (See the "SLTPTR - Critical Memory Control Element" section.) SLOTLO contains a full eight bits corresponding to A16-A23. Reading this byte returns the last value written. SLOTHI only contains two active bits corresponding to A24 and A25. Reading this register returns the last values written to bits 0 and 1 and logic 1's in all other bit positions. (Default = 03FFh, no off-board memory accesses.)

RAMMAP (03h) (Default = E0h)
Bit 7 in conjunction with the EAXS register, determines system response to memory accesses between E0000h-EFFFFh. When set to a logic 1 and the EAXS code for the specific 16K segment is 00b, reads generate a –ROMCS and a ROM access is performed from the MD bus. When set to a logic 0 and the EAXS code for the specific 16K segment is 00b, reads and writes are performed to the slot bus. This feature allows systems not using a 128K BIOS to access memory devices on the slot bus in the E0000h-EFFFFh area. See EAXS below for further details. Accesses to the area between FE0000h-FEFFFFh also respond in the above manner except that EAXS has no control over this memory space. However, in this area there is an interaction with the mid-BIOS control provided by bit 5 of MISCSET5 as described below.

Bits 4-0 specify one of the valid memory maps as shown Table 1. Note that not all possible 6-bit codes are assigned to valid memory maps.

RAMMOV (04H) (Default = F0h)
Bits 3-0 specify a switching function which determines which internal –RAS3 - –RAS0 and CAS3-CAS0 signals drive which external –RASBK3 - –RASBK0 and CASBK3-CASBK0 pins. (Default = 0.)

Refer to Table 2 for the remap configuration register code mapping.

RAMSET (05h) (Default =7Ch)
Bits 7-6 program the drive current on lines MA0-MA10 and on –RAMW according to the following codes:
00 = 150 pF drive
01 = 300 pF drive (Default)
10 = 450 pF drive
11 = 600 pF drive

Bit 5 is set to 0 in order to allow a cycle to begin one CLK2 earlier. This provides extra access time. (Default = 1 Early Start Disable.) Early Start may be enabled in systems running at 20 MHz or below.

Bit 4 programs the drive level on the –RASBK pins.
1 = 12 mA drive (Default = 1)
0 = 24 mA drive

Bit 3 indicates whether page mode is active on Bank A.
0 = Disabled
1 = Enabled (Default)

Bit 2 indicates whether page mode is active on Bank B.
0 = Disabled
1 = Enabled (Default)

Bit 1 indicates the interleave mode for Bank A. It is encoded as follows:
0 = Interleave on bit 1 for all DRAMs (Default)
1 = Interleave on bit 10 for all DRAMs

Bit 0 indicates the interleave mode for Bank B. It is encoded as follows:
0 = Interleave on bit 1 for all DRAMs (Default)
1 = Interleave on bit 10 for all DRAMs

REFCTL (06h) (Default = 00h)
Bit 7 is 0 for coupled refresh mode and 1 for decoupled refresh mode. (Default = 0.)

Bits 6-4 provide three bits to specify a divider for on-board refresh.
000 = ÷ 1 (Default)
001 = ÷ 2
010 = ÷ 4
011 = ÷ 8
100 = ÷ 16

Bit 3 controls internal I/O decode. When bit 3 = 0, full 16-bit decode is performed. When bit 3 = 1, 10-bit I/O decode is performed. (Default = 0.)

Bits 2-0 provide three bits which specify a divider for off-board refresh.
000 = ÷ 1 (Default)
001 = ÷ 2
010 = ÷ 4
011 = ÷ 8
100 = ÷ 16

RASTMA - RAS Timing for DRAM Banks 0 and 1 (07h) (Default = FFh)
Bit 7 indicates the –RASBK to column address delay:
0 = 1/2 CLK2
1 = 1 CLK2 (Default)

Bit 6 indicates number of clock delays between –RASBK and CASBK (tRCD). Actual clock delays encoded by this bit is:
0 = 1 CLK2
1 = 2 CLK2s (Default)

Bits 5-3 indicate the number of clock periods of –RASBK precharge time (tRP). Bit encoding relative to the number of clocks is:
010 = 2 CLK2s
011 = 3 CLK2s
100 = 4 CLK2s
101 = 5 CLK2s
110 = 6 CLK2s
111 = 7 CLK2s (Default)

Bits 2-0 indicate the number of clock periods of –RASBK active time (tRAS). Bit encoding relative to the number of clocks is:
000 = 2 CLK2s
001 = 3 CLK2s
010 = 4 CLK2s
011 = 5 CLK2s
100 = 6 CLK2s
101 = 7 CLK2s
110 = 8 CLK2s
111 = 9 CLK2s (Default)

CASTMA - CAS Timing for DRAM Banks 0 and 1 (08h) (Default = FFh)
Bits 7-6 indicate the number of clock cycles of CAS active time during memory writes (tCASW):
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s
11 = 4 CLK2s (Default)

Bit 5 indicates the number of CLK2s of delay that occur before CAS goes active after the start of the status cycle (tCST). This parameter is applicable during all write operations.
0 = 3 CLK2s
1 = 4 CLK2s (Default)

Bits 4-3 indicate the number of clock cycles of CAS precharge time (tCP). Bit encoding relative to the number of clocks is:
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s
11 = 4 CLK2s (Default)

Bits 2-0 indicate the number of clock cycles of CAS active time during memory reads (tCASR). Bit encoding relative to the number of clocks is:
000 = 2 CLK2s
001 = 3 CLK2s
010 = 4 CLK2s
011 = 5 CLK2s
100 = 6 CLK2s
101 = 7 CLK2s
110 = 8 CLK2s
111 = 8 CLK2s (Default)

RASTMB - RAS Timing for DRAM Banks 2 and 3 (09h) (Default = FFh)
See RASTMA for bit definitions.

CASTMB - CAS Timing for DRAM Banks 2 and 3 (0Ah) (Default = FFh)
See CASTMA for bit definitions.

EMSEN1 (0Bh) (Default = 00h)
Bit 7 is set as global enable for the EMS translation registers from C0000h-EC000h.
0 = EMS disable (Default)
1 = EMS enable

Bit 6 is set as the global enable for the EMS backfill translation registers from 40000-9C000h.
0 = Backfill disable (Default)
1 = Backfill enable

Bit 4 determines the EMS window range.
0 = EMS Map 0
1 = EMS Map 1

Each bit below is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled.

Page Controlled by each bit:

Bit 0	EMS Page 8
Bit 1	EMS Page 9
Bit 2	EMS Page 10
Bit 3	EMS Page 11

EMSEN2 (0Ch) (Default = 00h)
Each bit is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled. When disabled, an attempted access to the associated address space actually accesses that address directly. When enabled and the entire EMS system is enabled by having bit 7 of the EMSEN1 register set, an access to the associated page is redirected to the address contained in the page register concatenated with 386 address bits A0-A13. Whether bits 0-3 control the AXXXXh-CXXXXh range is determined by the state of bit 4 of EMSEN1. Bits 4-7 control the DXXXXh range in either state of bit 4 of EMSEN1. Bits 4-7 control the DXXXXh range in either state of bit 4 of EMSEN1. (Default value for this register is 0; all EMS page registers are disabled.)

Page Controlled by each bit:

Bit 0	EMS Page 0
Bit 1	EMS Page 1
Bit 2	EMS Page 2
Bit 3	EMS Page 3
Bit 4	EMS Page 4
Bit 5	EMS Page 5
Bit 6	EMS Page 6
Bit 7	EMS Page 7

The following registers provide control over the memory range from 640K to 1 Mbyte.

In the registers summarized below, each pair of bits control one 16K page as defined by the following table:

	Read	Write
Slot Bus*	0	0
System Board	1	1

*In the address space F0000h-FFFFFh, default means accesses are from on-board ROM space. Default accesses in areas from A0000h-DFFFFh are from the slot bus. Default in the area from E0000h-EFFFFh can be either on-board ROM or slot bus accesses depending on the state of bit 7 of RAMMAP.

This table translates to the following four cases:
00 = Read default, write slot bus
01 = Setup mode: read default, write system board
10 = Read system board, write slot bus
11 = Read/write system board

AAXS (0Dh) *Default is always the slot bus (Default = 00h)
Bits 6-7 - Segment at AC000h
Bits 4-5 - Segment at A8000h
Bits 2-3 - Segment at A4000h
Bits 0-1 - Segment at A0000h

BAXS (0Eh) *Default is always the slot bus (Default = 00h)
Bits 6-7 - Segment at BC000h
Bits 4-5 - Segment at B8000h
Bits 2-3 - Segment at B4000h
Bits 0-1 - Segment at B0000h

CAXS (0Fh) *Default is always the slot bus (Default = 00h)
Bits 6-7 - Segment at CC000h
Bits 4-5 - Segment at C8000h
Bits 2-3 - Segment at C4000h
Bits 0-1 - Segment at C0000h

DAXS (10h) *Default is always the slot bus. (Default = 00h)
Bits 6-7 - Segment at DC000h
Bits 4-5 - Segment at D8000h
Bits 2-3 - Segment at D4000h
Bits 0-1 - Segment at D0000h

EAXS (11h) *Default may be on-board BIOS ROM access or slot bus access. (Default = 00h)
This memory space is a special case in that "default" can be one of two locations depending on the state of bit 7 of RAMMAP.

RAMMAP Bit 7	EAXS	Operation
0	00	Read/write slot bus
1	00	Read on-board ROM, write slot bus (–ROMCS active)
0	01	Shadow setup mode: read slot bus, write system board
1	01	Shadow setup mode: read on-bus ROM, write system board
X	10	Read system board/ write slot bus (shadow active)

Bits 6-7 - Segment at EC000h
Bits 4-5 - Segment at E8000h
Bits 2-3 - Segment at E4000h
Bits 0-1 - Segment at E0000h

FAXS (12h) *Default may be on-board BIOS ROM access. (Default = 00h)
Bits 6-7 - Segment at FC000h
Bits 4-5 - Segment at F8000h
Bits 2-3 - Segment at F4000h
Bits 0-1 - Segment at F0000h

SLEEP (13h) (Default = 01h)
Bit 7 - Power-down enable.
0 = Default operational setting. Normal clock speed.
1 = Invokes clock divider set in bits 4 through 6.

This bit is reset to 0 and normal operation resumes when rewritten or when the VL82C330 receives a hardware reset.

Bits 6-4 - Power-down CLK2 divider. These bits provide a code used to divide the CLK2 down for sleep mode. The codes are:
000 = ÷1 Default (/1 clock)
001 = ÷2
010 = ÷3
011 = ÷4
100 = ÷8
101 = ÷16
110 = ÷32
111 = ÷64

Bits 3-1 provide for software control of an external device. The state of these bits is ORed with bit 7 and the ORed output is connected to an external pin on the VL82C330. This causes the external pin to be active whenever the sleep mode is active (high) or whenever bit 1 is set high. (Default = 00b.)

Bit 0 is a simple latch that provides no functionality in the VL82C330. However, a read always reflects the last write to this bit. (Default = 1.)

MISCSET (14h) (Default = 06h)
When bit 7 = 1, the special features accesses via ports EEh, EFh, F4h, F5h, F9h, and FBh are disable. These features are described in the "Dedicated Internal Control Registers" section earlier in this document.
0 = enabled (Default)
1 = disabled

Bit 6 controls coprocessor software reset.
0 = enabled (Default)
1 = disabled

Bit 5 controls the middle BIOS space from 00FE0000h-00FFFFFh. Two options are provided:
0 = This space mirrors the 000E0000h-000FFFFFh space. –ROMCS is generated for this space. (Default)
1 = This space maps directly to read/ write on-board DRAM.

Bits 4-3 specify the CLK2 divider that is invoked when the TURBO input pin is low or when a write to port 0F4h is performed.
00 = CLK2 ÷1 (Default)
01 = CLK2 ÷2
10 = CLK2 ÷3
11 = CLK2 ÷4

Bits 2-1 are the value used for division of TCLK2 or BUSOSC to generate BUSCLK.
00 = ÷ 1
01 = ÷ 2
10 = ÷ 3
11 = ÷ 4 (Default)

Bit 0 indicates the BUSCLK divider source.
0 = TCLK2 (Default)
1 = BUSOSC

TEST (15h) (Default = 00h)
This register is reserved for "to be determined" factory test functions. It must never be written during normal operation.

CTRL1 (16h) (Default = 00h)
This register contains additional system functional controls. Bits 1, 2, and 3 are reserved for interface to a future TOPCAT-compatible circuit. Do not write 1's to these bits. Bit 0 also will be used for this future circuit but it also controls a function in this version of the VL82C320. See below for details.

Bit 7 provides for disk controller compatibility. With fast CPUs, some disks can be overrun by programmed I/O. This bit provides a way to compensate by forcing the first memory cycle after an I/O cycle to be executive at non-turbo speed.
0 = slow programmed I/O (Default)
1 = normal programmed I/O

Bit 6 provides the option to not perform CASBK before –RASBK refresh while sleep mode is active. When set to 1, normal refresh is performed while in sleep mode. This consumes more power because the VL82C330 must drive the MA10-MA0 and –RAMW signals to all DRAM chips. When set to 0, CASBK before –RASBK refresh occurs while in sleep mode. (Default =0)

Bits 5 and 4 are used to open a 64K or 128K window at the top of DOS memory for access by slot bus cards. This allows accesses to be directed off-board in this region but then come back on-board in order to access on-board extended memory. The slot pointer (SLTPTR) can not be used to provide this function because all accesses above slot pointer are off-board and there is no way to gain access to on-board memory above this pointer except through the EMS hardware. These bits affect only the CPU address space from 512K-640K.

0X - on-board accesses in the 512K-640K region (Default = 00)
10 - 576K-640K accesses slot bus 512K-576K on-board accesses
11 - 512K-640K accesses slot bus

Special cases: This feature is inactive when EMS backfill is enabled. An attempt to set a code other than 0Xb with EMS backfill enabled will fail to change the code. If this feature is activated with codes 1Xb and EMS backfill is later activated, the code will automatically change to 00b disabling slot bus accesses in this region.

Use of SLTPTR in the same range is totally compatible. SLTPTR rules. If SLTPTR = 576K or 512K, the setting of bits 5 and 4 of CTRL1 doesn't matter. Accesses will be directed to the slot bus in this region and will also remain off-board above 640K.

Bit 3 is reserved (Default = 0)

Bit 2 is reserved (Default = 0)

Bit 1 is reserved (Default = 0)

Bit 0 changes the definition of the –SLP/MISS pin from –SLP output to MISS input when set to "1". (Default = 0) For use with a future TOPCAT product.

TABLE 12. INDEXED CONFIGURATION MAP

Index Port	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	A7	A6	A5	A4	A3	A2	A1	A0

	Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1	1	1	1	0	0	0	0
01	SLOTHI	1	1	1	1	1	1	A25	A24
02	SLOTLO	A23	A22	A21	A20	A19	A18	A17	A16
03	RAMMAP	ROMSLOT	1	1	DRAM Memory Map Code				
04	RAMMOV	1	1	1	1	RASBK - CAS Swap Code			
05	RAMSET	DRAM Drive		ESTART	RAS DRV	Page Md A	Page Md B	Bank A Int	Bank B Int
06	REFCTL	Decup	Slow Refresh Divider - System Board			10/16 IO	Slow Refresh Divider - Slots		
07	RASTMA	RAS ADDSEL	tRCD	tRP		tRAS			
08	CASTMA	tCASW		tCST	tCP	tCASR			
09	RASTMB	RAS ADDSEL	tRCD	tRP		tRAS			
0A	CASTMB	tCASW		tCST	tCP	tCASR			
0B	EMSEN1	EMS Enable	BF Enable	Reserved	EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
0C	EMSEN2	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
0D	AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
0E	BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
0F	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11	EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
12	FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
13	SLEEP	Enable	Power Down CLK2 Divider			Ext Ctrl 3	Ext Ctrl 2	Ext Ctrl 1	SYSCLK
14	MISCSET	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider		Slot Bus Divider		Bus Mode
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved

Note: A 1 indicates reserved bits that read back as logic 1.

TABLE 13. DEFAULT CONFIGURATION VALUES AFTER RESET

Data Port EDh (R/W)		D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1R	1R	1R	1R	0R	0R	1R	0R
01	SLOTHI	1R	1R	1R	1R	1R	1R	1	1
02	SLOTLO	1	1	1	1	1	1	1	1
03	RAMMAP	1	1R	1R	0	0	0	0	0
04	RAMMOV	1R	1R	1R	1R	0	0	0	0
05	RAMSET	0	1	1	1	1	1	0	0
06	REFCTL	0	0	0	0	0	0	0	0
07	RASTMA	1	1	1	1	1	1	1	1
08	CASTMA	1	1	1	1	1	1	1	1
09	RASTMB	1	1	1	1	1	1	1	1
0A	CASTMB	1	1	1	1	1	1	1	1
0B	EMSEN1	0	0	0	0	0	0	0	0
0C	EMSEN2	0	0	0	0	0	0	0	0
0D	AAXS	0	0	0	0	0	0	0	0
0E	BAXS	0	0	0	0	0	0	0	0
0F	CAXS	0	0	0	0	0	0	0	0
10	DAXS	0	0	0	0	0	0	0	0
11	EAXS	0	0	0	0	0	0	0	0
12	FAXS	0	0	0	0	0	0	0	0
13	SLEEP	0	0	0	0	0	0	0	1
14	MISCSET	0	0	0	0	0	1	1	0
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	0	0	0	0	0	0	0	0

Note: Values followed by "R" are read-only and have no logical function. Reserved bits in the TEST register are for factory test. Read/write results to this register are undefined.

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
t1	TCLK2 Period	15		ns	
t2	TCLK2 High Time	6.5		ns	2.0 V
t3	TCLK2 Low Time	6.5		ns	2.0 V
t4	BUSOSC Period	15		ns	
t5	BUSOSC, OSC High Time	6.5		ns	1.5 V
t6	BUSOSC, OSC Low Time	6.5		ns	1.5 V
t7	CLK2IN High Time	5		ns	2.0 V
t8	CLK2IN Low Time	5		ns	2.0 V
tD9	TCLK2 to CLK2 Delay		25	ns	CL=50 pF
t10	CLK2 Fall Time		4	ns	3.7 V to 0.8 V @ CL=50
t11	CLK2 Rise Time		4	ns	0.8 V to 3.7 V @ CL=50
tD12	TCLK2 to BUSCLK Delay		25	ns	CL=50 pF
tD13	BUSOSC to BUSCLK Delay		25	ns	CL=50 pF
t14	BUSCLK Fall Time		9	ns	3.7 V to 0.8 V @ CL=50
t15	BUSCLK Rise Time		12	ns	0.8 V to 3.7 V @ CL=50
tD16	CLK2IN to RES386 Delay	3	10	ns	CL=30 pF
tD17	CLK2IN to RES387 Delay	3	10	ns	CL=30 pF
tD18	CLK2IN to –READYO Delay	3	15	ns	CL=30 pF
tD19	CLK2IN to HRQ Delay	3	18	ns	CL=50 pF
tSU20	–ADS to CLK2IN Setup Time	15		ns	
tH21	–ADS from CLK2IN Hold Time	4		ns	
tSU22	W/–R, M/–IO, D/–C to CLK2IN Setup Time	15		ns	ESTART OFF
tSU22a	W/–R, M/–IO, D/–C to CLK2IN Setup Time	26		ns	ESTART ON
tH23	W/–R, M/–IO, D/–C from CLK2IN Hold Time	4		ns	
tSU24	A31,A29, A26-A2 to CLK2IN Setup Time	15		ns	ESTART OFF
tSU24A	A31, A29, A26-A2 to CLK2IN Setup Time	26		ns	ESTART ON
tH26	A31, A29, A25-A2 from CLK2IN Hold Time	4		ns	
tSU27	–BE3- –BE0 to CLK2IN Setup Time	4		ns	
tH28	–BE3- –BE0 from CLK2IN Hold Time	4		ns	
tSU30	HLDA to CLK2IN Setup Time	10		ns	
tH31	HLDA to CLK2IN Hold Time	4		ns	
tSU32	–READYIN to CLK2IN Setup Time	8		ns	
tH33	–READYIN from CLK2IN Hold Time	4		ns	
tD34	CLK2IN to –RASBK3- –RASBK0 Delay	3	17	ns	CL=300 pF

Note: Minimum propogation delays noted as "tDX" are characterized but not tested.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tD35	CLK2IN to –RAMW Delay	3	20	ns	CL=300 pF
tD36	CLK2IN to CASBK3-CASBK0 Delay	3	16	ns	CL=50 pF
tD37	CLK2IN to –BRDRAM Delay	3	18	ns	CL=50 pF
tD38	CLK2IN to –DEN Delay	3	17	ns	CL=50 pF
tD39	CLK2IN to –MDLAT Delay	3	19	ns	CL=50 pF
tD40	CLK2IN to –ROMCS Delay	3	25	ns	CL=50 pF
tD41	A31, A29, A26-A2 to MA10-MA0 Delay	3	34	ns	CL=300 pF
tD42	CLK2IN to MA10-MA0 Delay	3	24	ns	CL=300 pF
tD43	CLK2IN to MA10-MA0 Delay	3	24	ns	CL=300 pF
tD44	–BE3- –BE0 Delay	3	23	ns	CL=50 pF
tD45	CLK2IN to LBE3-LBE0 Delay	3	24	ns	CL=50 pF
tD46	CLK2IN to –CHS0/–MW, –CHS1/–MR CHM/–IO Going Low Delay	3	20	ns	CL=50 pF
tD47	BUSCLK to –CHS0/–MW, –CHS1/–MR, CHM/–IO Going High Delay	3	24	ns	CL=50 pF
tSU48	–CHREADY to BUSCLK Setup Time	8		ns	
tH49	–CHREADY from BUSCLK Hold Time	3		ns	
tSU50	XD7-XD0 to –IOW High Setup Time	30		ns	
tH51	XD7-XD0 from –IOW High Hold Time	5		ns	
tD52	–IOR Low to XD7-XD0 Delay	5	50	ns	CL=50 pF
tD53	–IOW High to SLEEP3-SLEEP1, –SLP/MISS Delay	4	35	ns	CL=50 pF
tD54	A20GATE to –BLKA20 Delay	4	20	ns	CL=50 pF
tD56	–IOW High or –IOR Low to –BLKA20 Delay	5	25	ns	CL=50 pF
tSU57	DMAHRQ to BUSCLK Setup Time	10		ns	
tH58	DMAHRQ from BUSCLK Hold Time	10		ns	
tD59	BUSCLK to DMAHLDA Delay	3	35	ns	CL=50 pF
tD60	CLK2IN to DMAHLDA Delay	3	25	ns	CL=50 pF
tD61	BUSCLK to –REFRESH Low Delay	3	28	ns	CL=200 pF
tD62	CLK2IN to –REFRESH Low Delay	3	28	ns	CL=200 pF
tD63	BUSCLK to –REFRESH Float Delay	3	20	ns	
tD65	WTKIRQ to IRQ13 Delay	3	20	ns	CL=50 pF
tD66	–ERROR387 Low to IRQ13 Delay	3	25	ns	CL=50 pF
tD67	–IOW Low to IRQ13 Low Delay	3	25	ns	CL=50 pF
tD68	PEREQ387 to PEREQ386 Delay	3	20	ns	CL=50 pF
tD69	–BUSY387 High to PEREQ386 High Delay	3	20	ns	CL=50 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tD70	–IOW Low to PEREQ386 Low Delay	3	25	ns	CL=50 pF
tD71	–BUSY387 to –BUSY386 Delay	3	20	ns	CL=50 pF
tD72	–IOW Low to –BUSY386 Delay	3	25	ns	CL=50 pF
tD73	CLK2IN to –BUSY386 Delay	3	20	ns	CL=50 pF
tD74	CLK2IN to –ERROR386 Delay	3	20	ns	CL=50 pF
tSU75	RSTDRV to CLK2IN Setup Time	7		ns	
tH76	RSTDRV from CLK2IN Hold Time	3		ns	
	OUT1, TURBO, –RC, –TRI			ns	No AC Specs on these Pins
tSU77	–CHS0/–MW, –CHS1/–MR to CLK2IN Setup	12		ns	CL=50 pF
tH78	–CHS0/–MW, –CHS1/–MR from CLK2IN Hold	4		ns	
tD79	–CHS0/–MW to –RAMW Delay	3	25	ns	CL=50 pF
tD80	–CHS0/–MW, –CHS1/–MR to –BRDRAM Delay	3	25	ns	CL=50 pF
tD81	A23-A1 to –BRDRAM Delay	3	40	ns	CL=50 pF

4

FIGURE 8. CLOCK TIMING

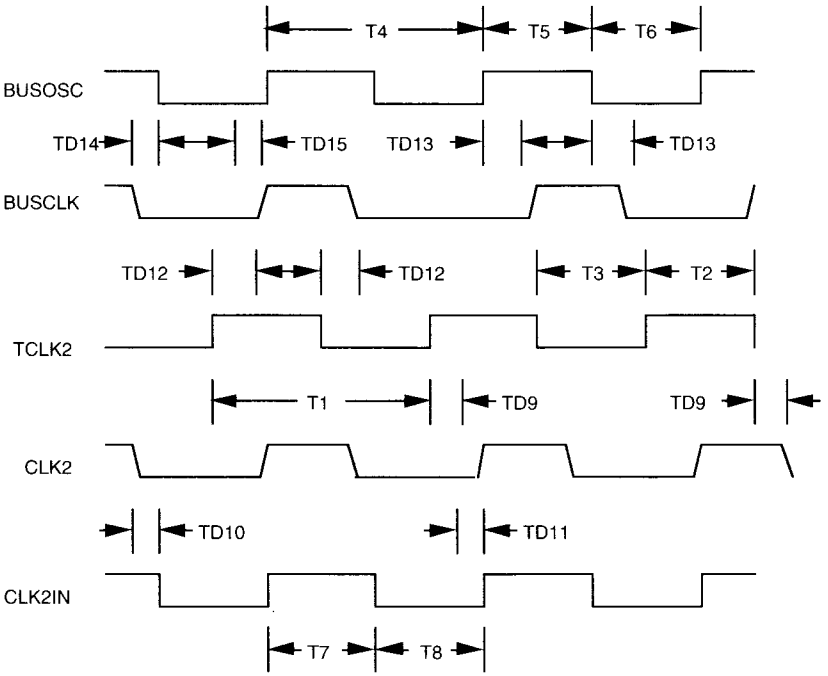


FIGURE 8A. CPU INTERFACE TIMING

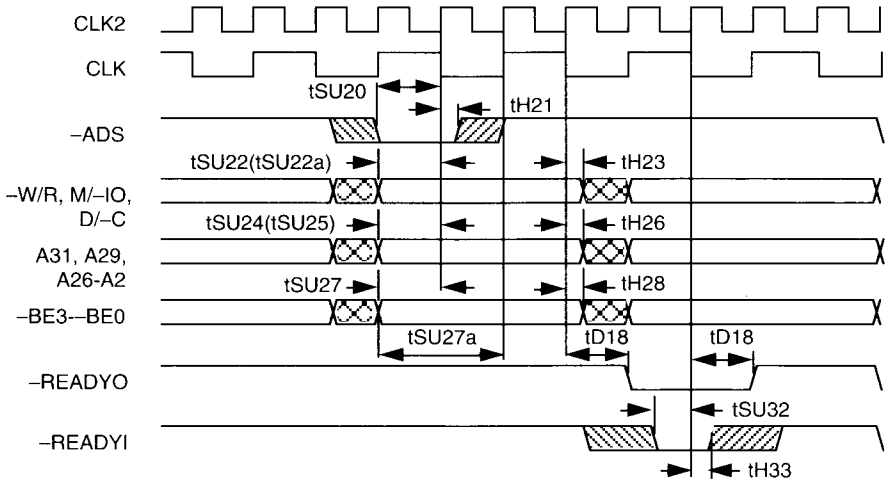


FIGURE 9.

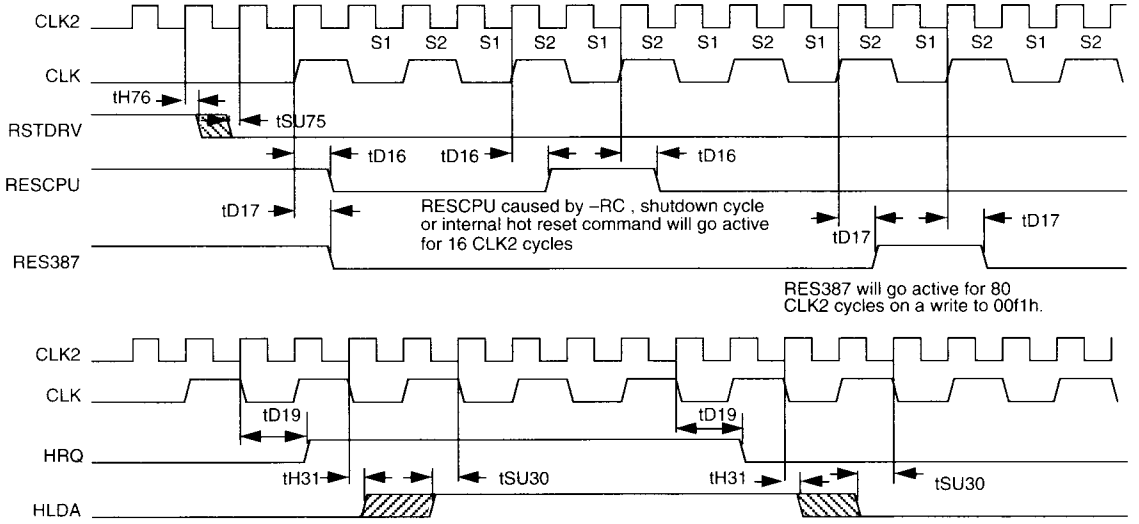


FIGURE 10.

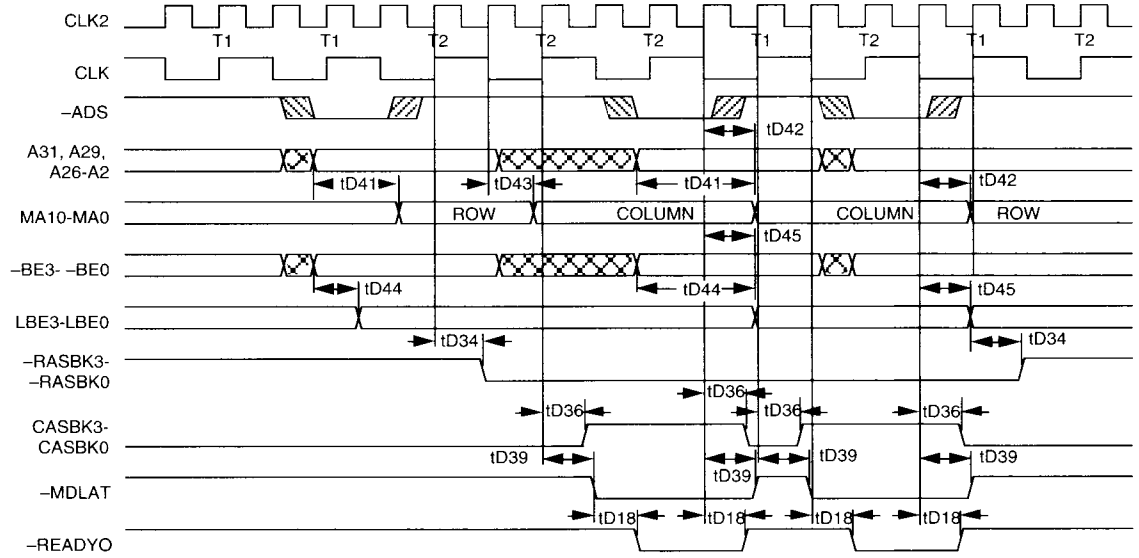
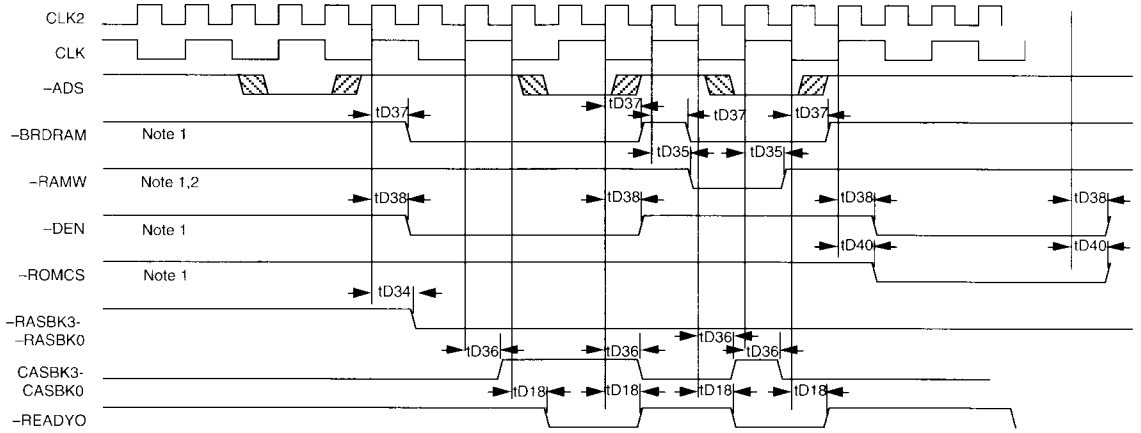


FIGURE 11.



Note: 1. -BRDRAM, -RAMW, -DEN, and -ROMCS are all shown assuming ESTART is inactive. If ESTART is active, these signals will go active one CLK2 cycle earlier. ESTART has no effect on these signals changing to the inactive state.
2. -RAMW will return in active from the same CLK2 edge when CASBK goes inactive.

FIGURE 12.

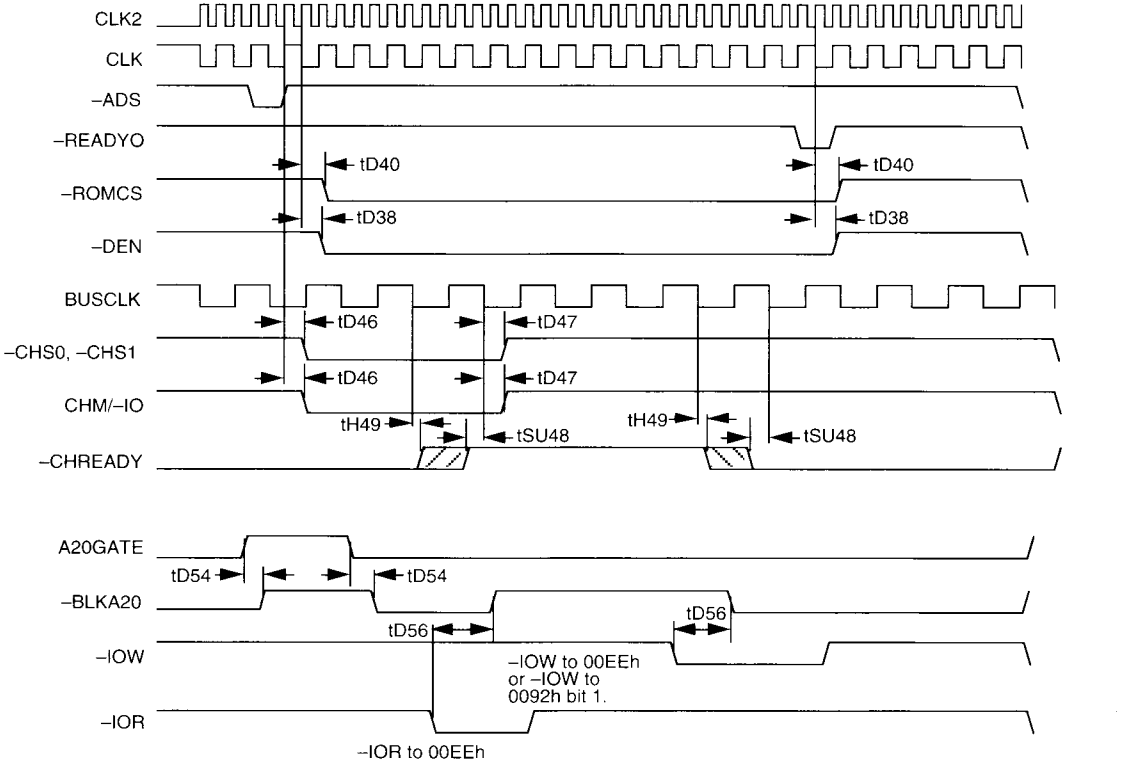


FIGURE 12A.

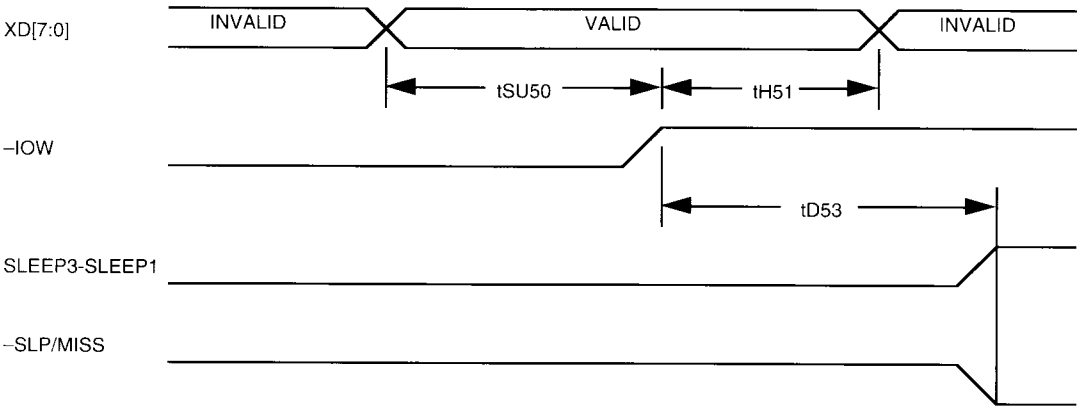


FIGURE 12 B.

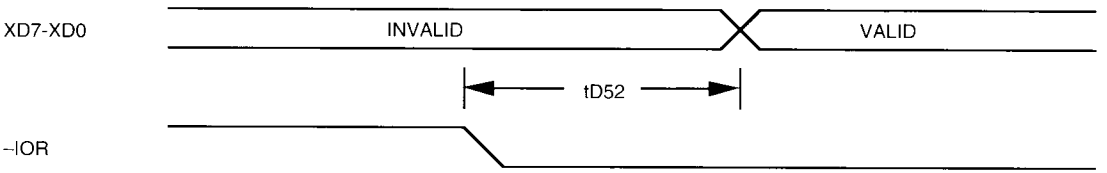


FIGURE 13.

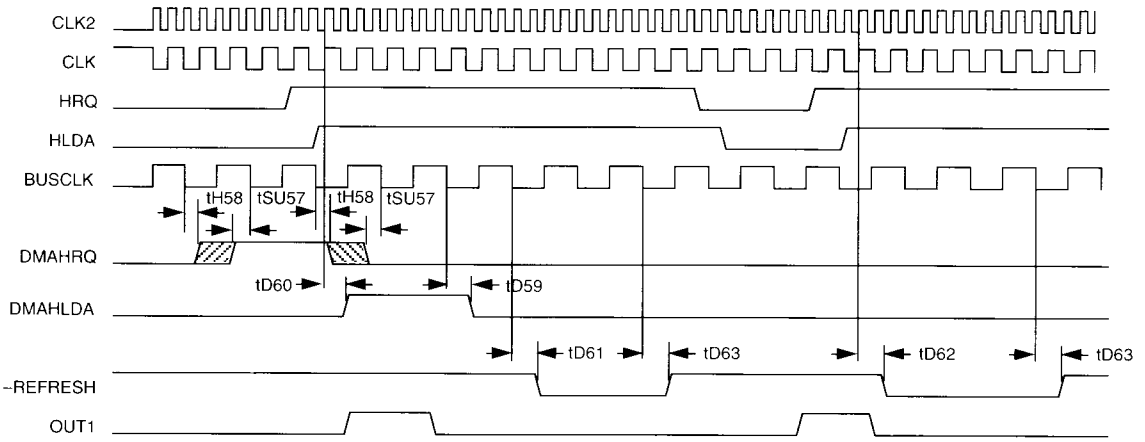


FIGURE 14.

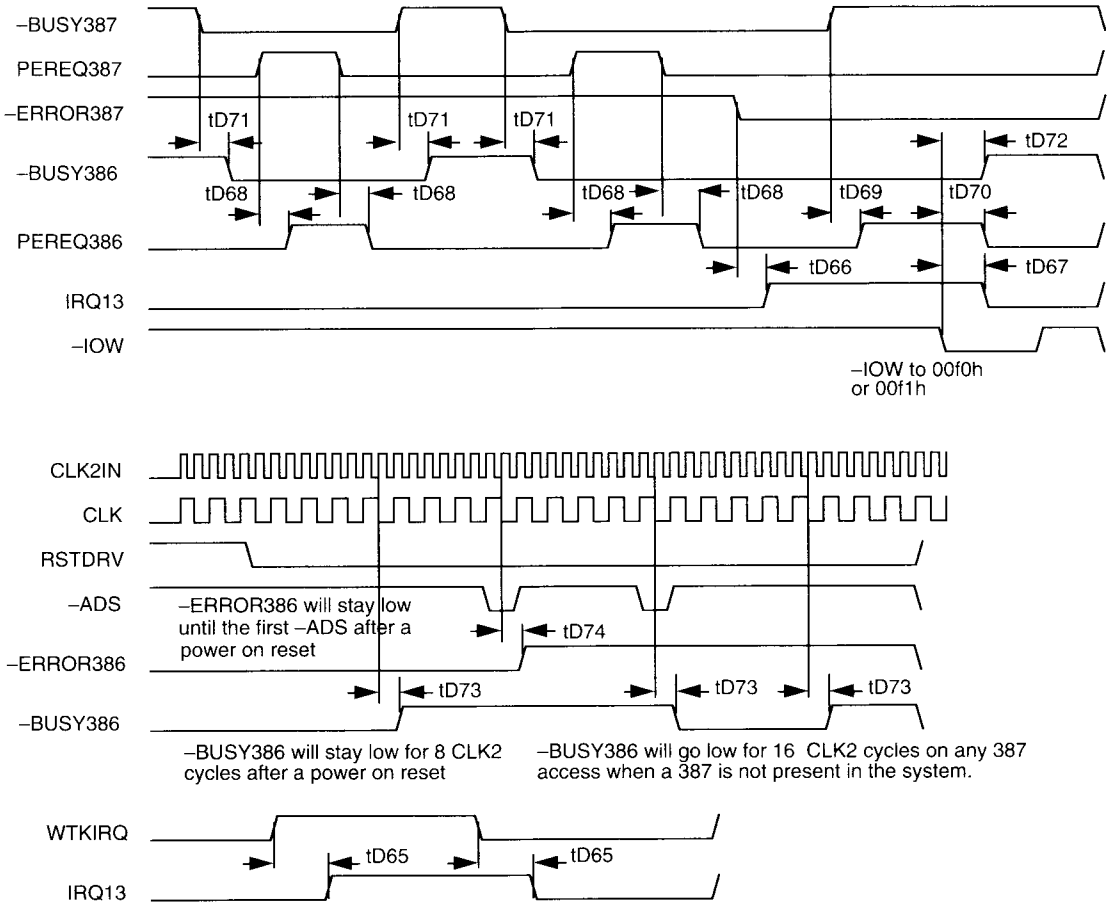

-BUSY387
PEREQ387
-ERROR387
-BUSY386
PEREQ386
IRQ13
-IOW
tD71
tD71
tD71
tD72
tD68
tD68
tD68
tD68
tD69
tD70
tD66
tD67
-IOW to 00f0h
or 00f1h
CLK2IN
CLK
RSTDRV
-ADS
-ERROR386
-BUSY386
-ERROR386 will stay low
until the first -ADS after a
power on reset
tD74
tD73
tD73
tD73
-BUSY386 will stay low for 8 CLK2
cycles after a power on reset
-BUSY386 will go low for 16 CLK2 cycles on any 387
access when a 387 is not present in the system.
WTKIRQ
IRQ13
tD65
tD65

FIGURE 14A.

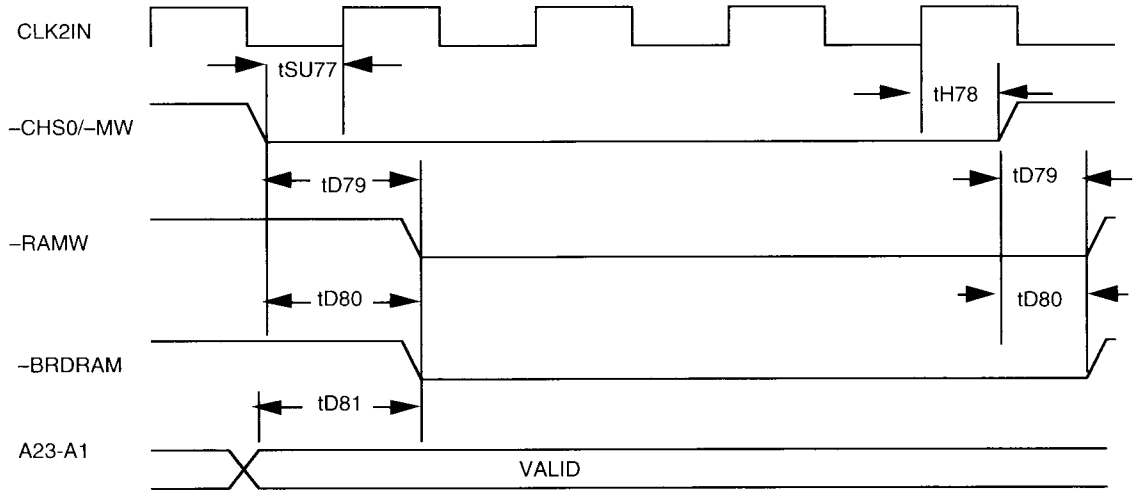
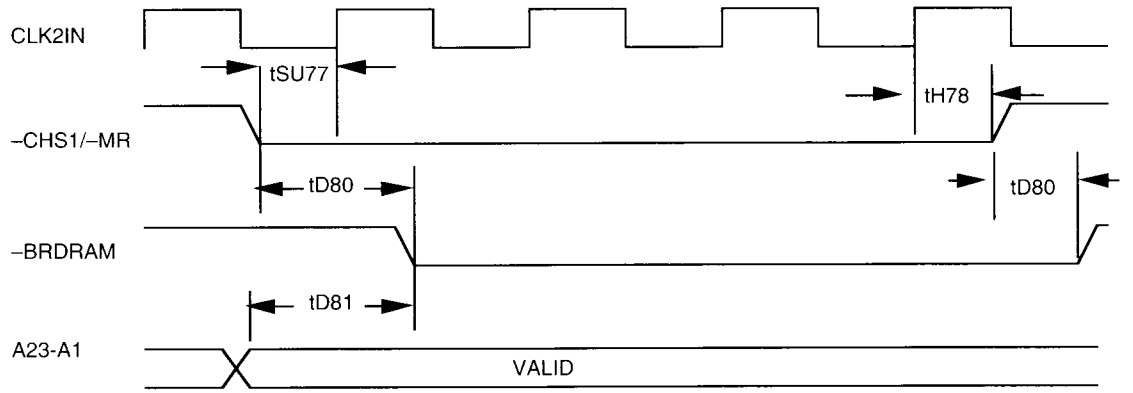


FIGURE 14B.



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground	−0.5 V to 7.0 V
Applied Output Voltage	−0.5 V to VDD + 0.3 V
Applied Input Voltage	−0.5 V to VDD + 0.3 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	−0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs
VILC	Input Low Voltage	−0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD − 0.8	VDD + 0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD − 0.45		V	IOH = −1 mA, Note 12
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOH2	Output High Voltage	VDD − 0.45		V	IOH = −2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, Note 3
VOH3	Output High Voltage	VDD − 0.45		V	IOH = −12 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 12 mA, bit 4 of RAMSET = 0 IOL = 24 mA, bit 4 of RAMSET = 1, Note 4
VOH4	Output High Voltage	VDD − 0.45		V	IOH = −6 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 10 mA, bits 7 and 6 of RAMSET = 00 IOL = 20 mA, bits 7 and 6 of RAMSET = 01 IOL = 30 mA, bits 7 and 6 of RAMSET = 10 IOL = 40 mA, bits 7 and 6 of RAMSET = 11, Note 4
VOH5	Output High Voltage	2.4		V	IOH = −6 mA, bit 7 of RAMSET = 0 IOH = −12 mA, bit 7 of RAMSET = 1, Note 4
VOL6	Output Low Voltage		0.45	V	IOL = 8 mA, Note 6
VOL7	Output Low Voltage		0.45	V	IOL = 24 mA, Note 7
VOL8	Output Low Voltage		0.45	V	IOL = 4 mA, Note 8

DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
ILI	Input Leakage Current	–10	10	µA	VIN = 0 V or VDD, Note 9
IIL	Input Leakage Current		–500	µA	VIN = 0 V, Note 10
IIH	Input Leakage Current		500	µA	VIN = VDD, Note 11
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Power Supply Current		500	µA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	Based on CLK2 Frequency
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	
VILTC	Input Low Voltage	–0.5	0.8	V	TCLK2 Input Levels
VIHTC	Input High Voltage	2.8	VDD + 0.5	V	TCLK2 Input Levels

Notes:
1. Pins: –BUSY386, PEREQ386, –ERROR386, –ROMCS, IRQ13, XD7-XD0, SLEEP3-SLEEP1.
2. Pins: –READYO, HRQ, RESCPU, CASBK3-CASBK0, RES387, LBE3-LBE0, –BRDRAM, –DEN, –MDLAT, –CHS0/–MW, –CHS1/–MR, CHM/–IO, –BLKA20, BUSCLK, DMAHLDA.
3. Pins: CLK2.
4. Pins: –RASBK3- –RASBK0.
5. Pins: MA10-MA0, –RAMW.
6. Pin: –SLP/MISS is an open drain output.
7. Pin: –REFRESH is an open drain output.
8. Pins: SLEEP3-SLEEP1 are open drain outputs.
9. All inputs except those listed in notes 10 and 11.
10. Pins: –ERROR387, –BUSY387, –TRI, W/–R, D/–C, M/–IO, –ADS, A31, A29 and A26 have internal pull ups.
11. Pins: PEREQ387 and WTIRQ have internal pull downs.
12. Pins: –BUSY386, PEREQ386, –ERROR386, –ROMCS, IRQ13, XD7-XD0.

100-PIN PLASTIC QUAD FLAT PACK

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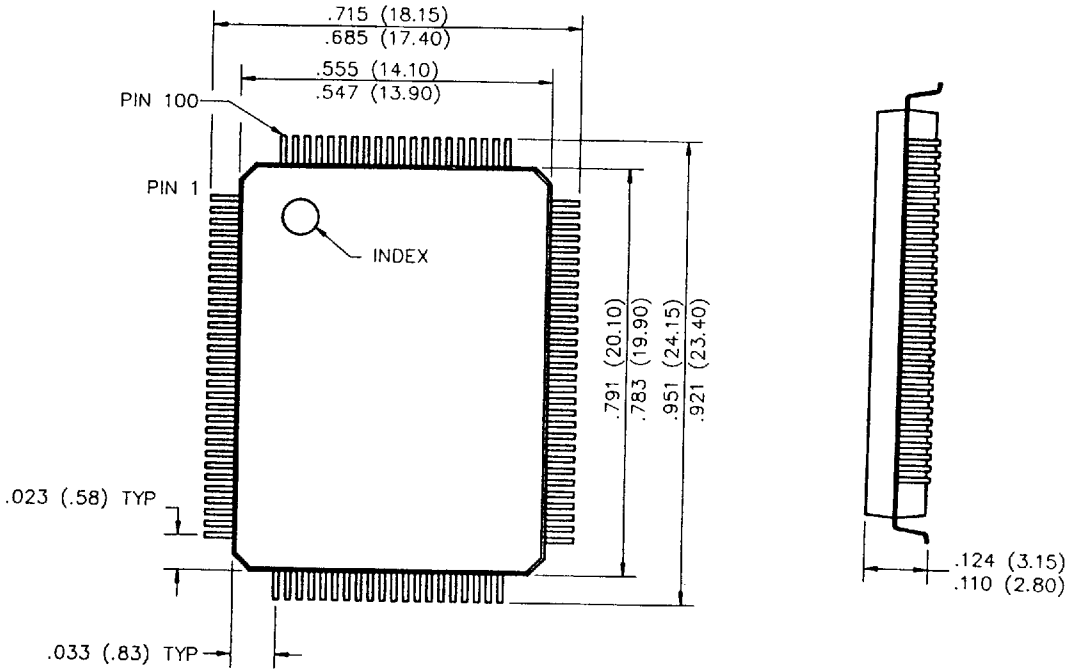
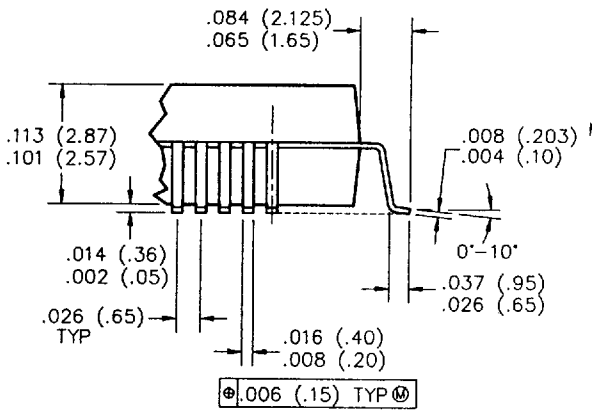
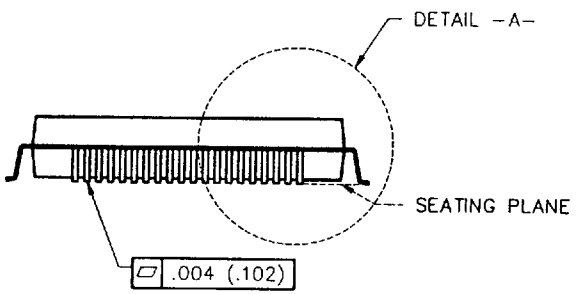




DETAIL –A–

NOTES:
1. CONTROLLING DIMENSION IS MM.



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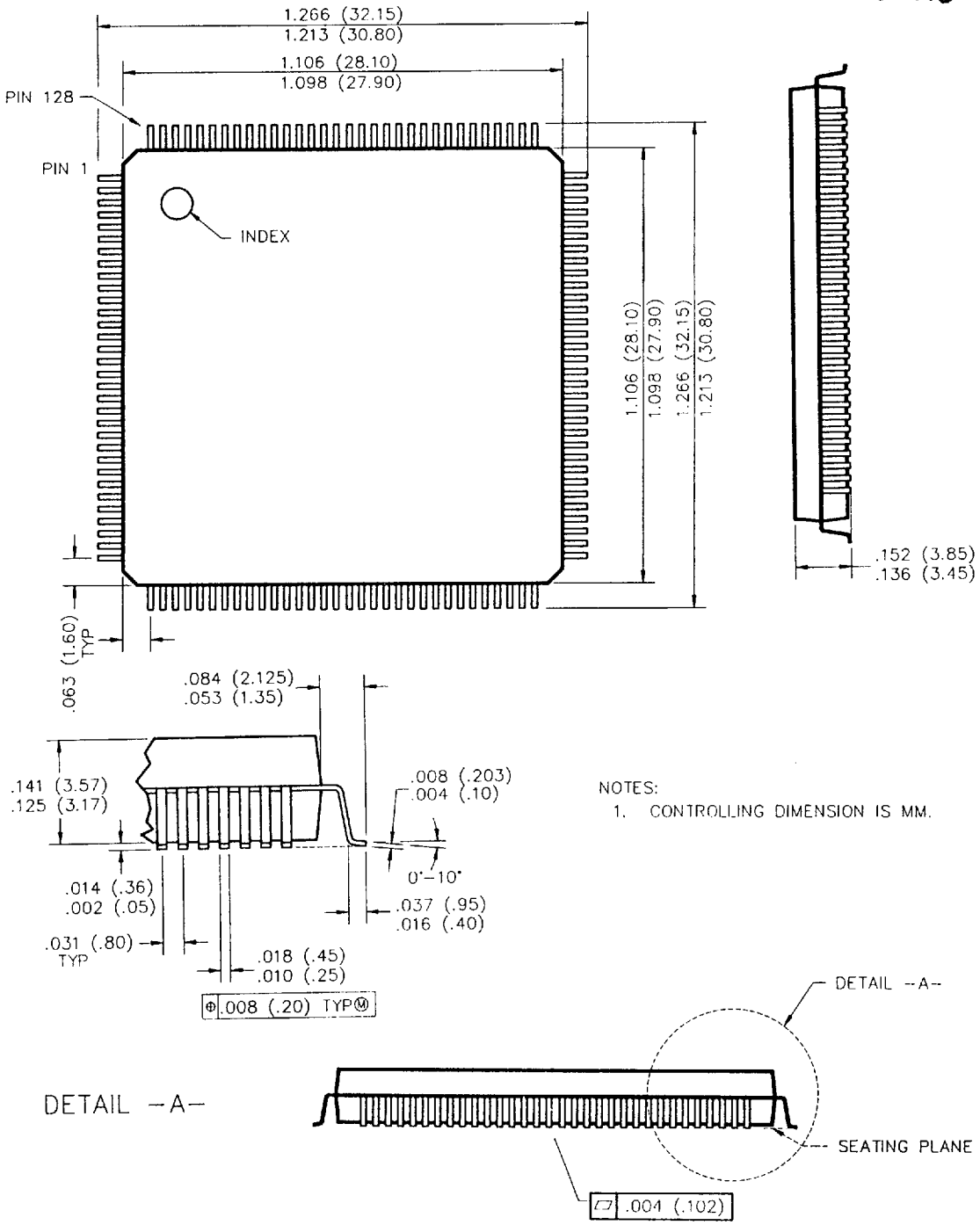
128-PIN PLASTIC FLAT PACK

V L S I TECHNOLOGY INC T-90-20

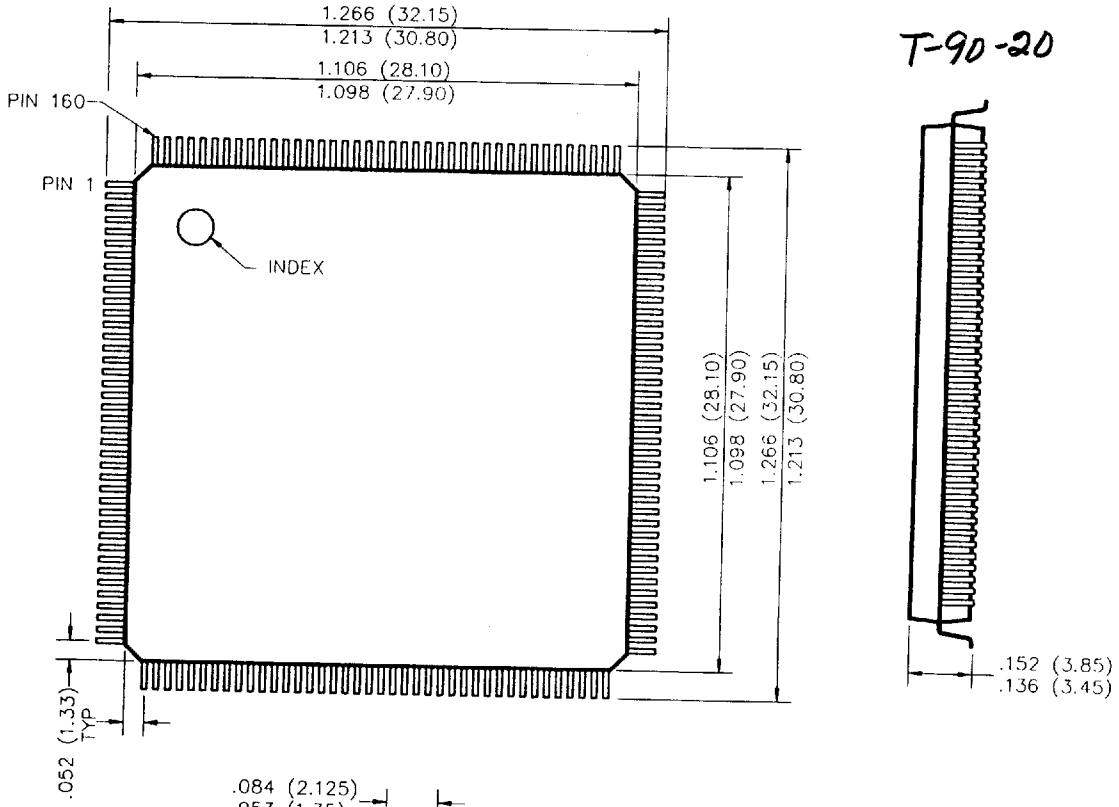


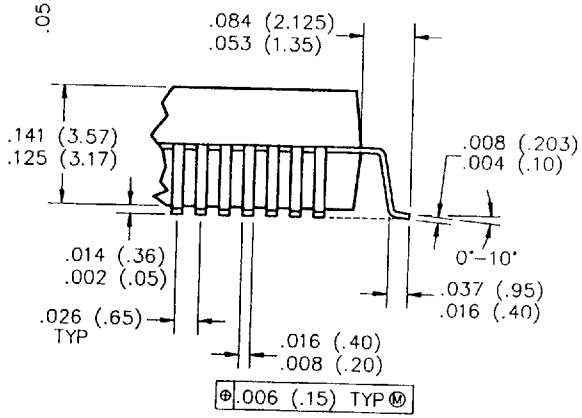
NOTES:
1. CONTROLLING DIMENSION IS MM.

160-PIN PLASTIC QUAD FLAT PACK

V L S I TECHNOLOGY INC

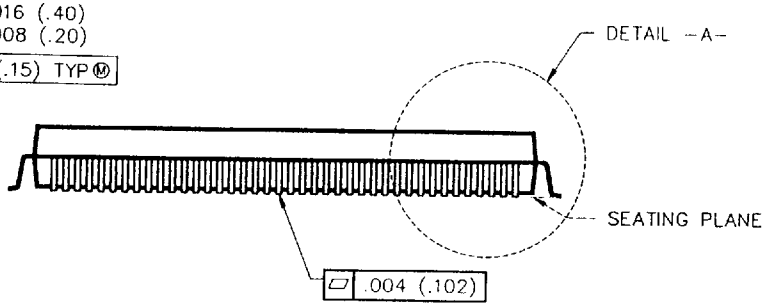
T-90-20





NOTES:
1. CONTROLLING DIMENSION IS MM.

DETAIL –A–



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