VLSI Technology, Inc.

Lynx Mobile Solution For 586-Class Processors

Product Bulletin

Overview

The VL82C520 Lynx/M chipset is VLSI's system solution optimized for the expanding mobile Pentium™ market. Carrying forward VLSI's mobile strategy and leveraging successful desktop innovations to offer a complete solution, Lynx/M leaps forward and integrates the system controller into a single Ball Grid Array (BGA) package. Included in the Lynx/M solution is a PCI "Super I/O" controller that integrates all the standard mobile peripherals. The Lynx/M offers a total solution compatible with the Common Architecture industry standard implementing highly efficient DDMA (Distributed DMA), Serial IRQ, and features for primary PCI hot docking using a Common Architecture compatible PCI to PCI bridge in the docking station.

Lynx/M System Controller, VL82C521

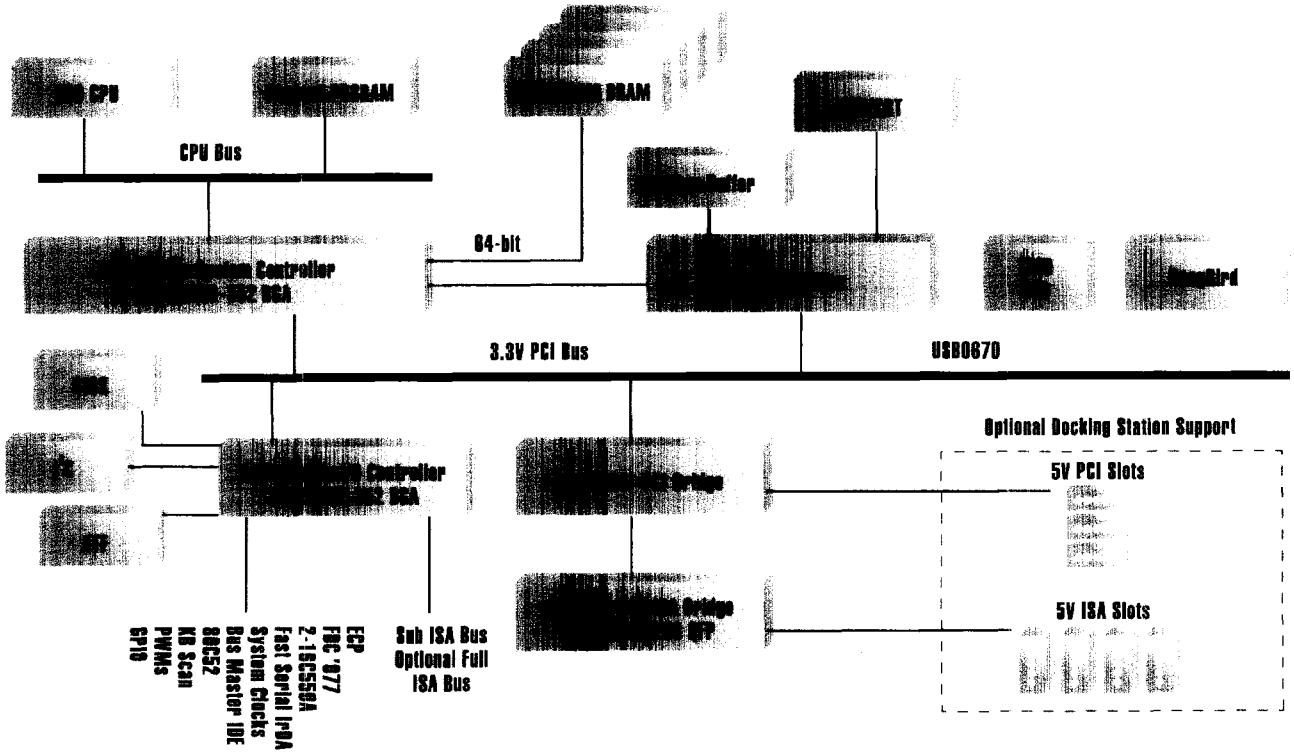
Packaged in a space-efficient low-profile 352 BGA, the Lynx/M System Controller is the heart of the solution. BGA packaging allows integrating functions usually partitioned into multiple packages. The integrated functions include a 66MHz CPU interface, 3.3V mobile PCI 2.1 compliant bus controller, 64-bit SDRAM, EDO, and FPM DRAM controller with nine-deep fast access smart write-buffers, on-board L2 256KB write-back cache controller, and VLSI's WATTSmart™ power management control. The DRAM interface provides drive for up to 24 memory devices thereby eliminating the need for external drivers. Also, selecting SDRAM provides the opportunity to implement a high performance system without an L2 cache.

Lynx/M Peripheral Controller, VL82C522

The Lynx/M chipset also includes a PCI Super I/O device, the Lynx/M Mobile Peripheral Controller (MPC). This device, also packaged in a low-profile 352 BGA, integrates a PCI 2.1 compliant bus interface, a fully buffered Bus Mastering IDE controller, an '077 floppy disk controller, Enhanced Capabilities Port (ECP), two 16550 UARTs with modem functionality, an SMB/I2C bus, an IrDA 1.1 compatible Fast Infrared communications port with ASK functionality, a Real-Time Clock, two pulse-width modulator outputs (PWM), and a 33MHz 8052 microcontroller. Two on-board PLLs with buffering provide all rhe required system clocks from only two crystal inputs; 14.318MHz and 32KHz.

A Sub-ISA bus supporting 8- or 16-bit I/O or DDMA transfers, and ISA Bus Mastering supports audio devices. Additionally, eight positive PCI address decodes provide support to Sub-ISA peripherals.

The 8052 provides the keyboard controller functionality with built-in scan for matrix keyboards and system boot controller functionality to ompletely wake up any part or all of the system from any level of



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suspend. The wake-up event can be a system event, timer, or any key depression on the keyboard. The MPC also provides up to 25 GPIO pins with expansion capabilities to provide flexible control of system components.

Singular ROM architecture enabled by the integrated 8052 keyboard controller saves both PCB space and cost by permitting a solitary ROM, Flash, or SRAM device to be used for keyboard, graphics and system BIOS.

WATTSMART™ Power Management

Incorporated in the Lynx/M chipset, the WATTSmart™ is a System Management Mode-based power management system. WATTSmart™ includes multiple system event monitoring, a watchdog timer, System Management Interrupt (SMI) generation, multiple I/O traps, CPU Stop Clock control, and provides three general purpose System Management I/O pins (SMIOs) for control and monitoring of external devices.

Virtually all activity resources are available as speed up events and to generate SMIs. SMIs can be generated by activity or after a period of inactivity. An SMI that is generated from activity is generally for a powered-down device, and the SMM handler can restore the device to normal operation. An SMI from activity can also be used to resume the system, start the clocks, etc.

Background

Lynx/M incorporates functions from previous desktop and mobile chipsets. Baselining from proven core system blocks and modifying to reflect new market requirements allows VLSI to meet the Time-To-Market expectations while minimizing risk.

Designed for Mobile

Utilizing high-pin count BGA packaging allows Lynx/M to reduce board space requirements by greater than 45%. This allows room on the PCB for additional functionality while reducing the complexity of multi-layer system boards.

Accessing VLSI's internal fab technology allows Lynx/M a path to an advanced 0.6µm CMOS process thereby achieving a true 3.3V system without performance trade-offs.

Features

- Support for Pentium and Pentium-class CPUs
- 64-bit wide SDRAM, EDO, and FPM DRAM controller
- Nine-deep, 64-bit fast-access smart write buffers
- Fully PCI 2.1 compliant, 33MHz, synchronous or asynchronous, high performance (120 MB/s) PCI bus with full concurrency to support high bandwidth multi-media
- Flexible L2 write-back cache controller supporting 3-1-1-1-1-1-1-1 burst cycles
- Highly integrated chipset in low-profile BGA packages
- Active Thermal Feedback (ATF) for closed-loop thermal control of the CPU
- PCI bridge support for high-performance primary PCI hot docking
- Common Architecture Serial Bus minimizes docking connector pin count
- SMB/I2C system management bus improves battery monitoring.
- Singular ROM for keyboard, System and graphics BIOS
- Full 2 channel Bus Mastering IDE controller
- Integrated '077 FDC
- Two 16550 UARTs
- 8052 keyboard controller with built-in scan for matrix keyboards and boot controller functionality
- System clocks from power-managed PLLs with on-board buffering for distribution
- Two PWMs to provide LCD backlight and contrast control
- Parallel port with PS2, EPP and ECP extensions
- Built-in IrDA 1.1 Fast Infrared communications port
- Multiple VCC rails and on-board level shifters to provide independent power-down and true 5.0 Vdc peripheral support
- Support for three PS2 ports
- Real-Time Clock with CMOS
- 25 GPIO pins with expansion
- Built-in Sub-ISA bus for 16-bit DMA ISA Master audio device
- Supports 3.3V and 0V suspend with multiple resume events, I/O trapping, and audio 0V suspend/resume
- Bus Keeper I/Os to reduce battery drain in suspend mode
- Supports shut-down option for CPU core power during powered suspend to maximize battery life
- Supports CPU clock division emulation to effectively reduce CPU clock frequency
- Plug-N-Play support
- Compliant with Microsoft recommendations for Win '95

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