VLSI TECHNOLOGY, INC.

PRODUCT SPECIFICATION

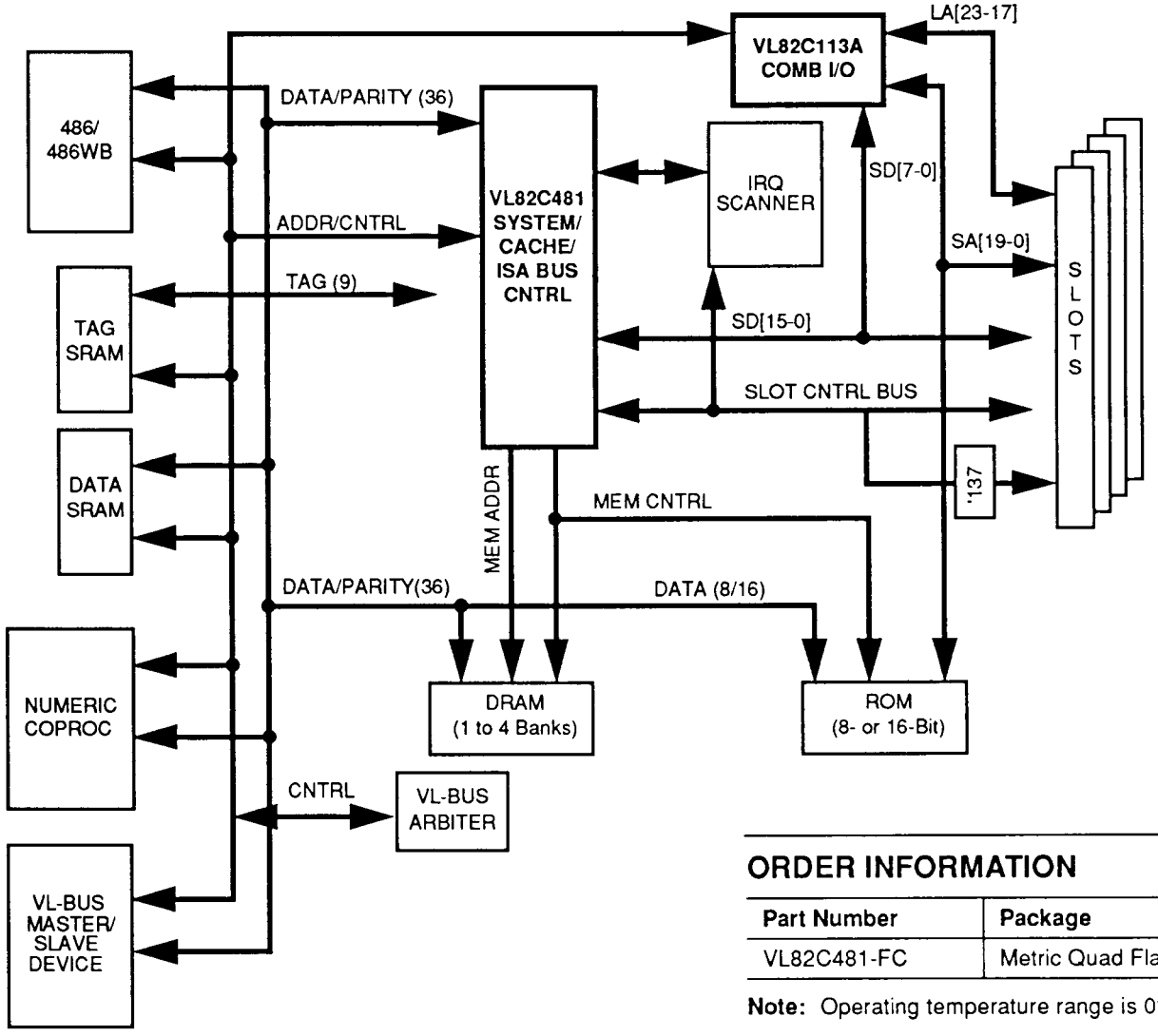
VL82C481

486 SYSTEM/CACHE/ISA BUS CONTROLLER

FEATURES

- Fully compatible with 486-based ISA bus systems
- Power-on reset option selects various operational modes
- Up to 40 MHz CPU operation
- Includes full support for CPU's with internal write-back cache (P24T, etc.)
- Comprehensive VESA VL-Bus support
- Replaces the following peripheral logic on the motherboard:
  - Two 82C37A DMA controllers
  - 74LS612 Memory mappers (extended to support 64 MB)
  - Two 82C59A Interrupt controllers
  - 82C54 Timer
  - 82284 Clock generator and ready interface
  - 82288 Bus controller
- Memory controller features include:
  - Up to 64 MB system memory
  - One to four banks 32 bits wide
  - 256K, 1M or 4M DRAM
  - Double-sided SIMMs
  - Page Mode DRAM access
  - Two-way interleave support
  - Programmable RAS#/CAS# timing
  - Burst read and write support
  - Parity generation/checking for on-board DRAM
  - Staggered RAS# refresh
- Supports:
  - 8- or 16-bit wide BIOS ROM
  - Shadow RAM in the 640K-1M area
  - Asynchronous ISA bus operation up to 16 MHz
  - Relocation of slot ROMs
  - Access to devices residing on the local bus
  - Weitek 4167 numeric coprocessor
- Includes:
  - Memory/refresh controller
  - Port A, B, and NMI logic
  - Bus steering logic
  - Turbo control
  - Hidden refresh
  - Three-stateable outputs for board testing

VL82C481-BASED ISA BUS SYSTEM DIAGRAM

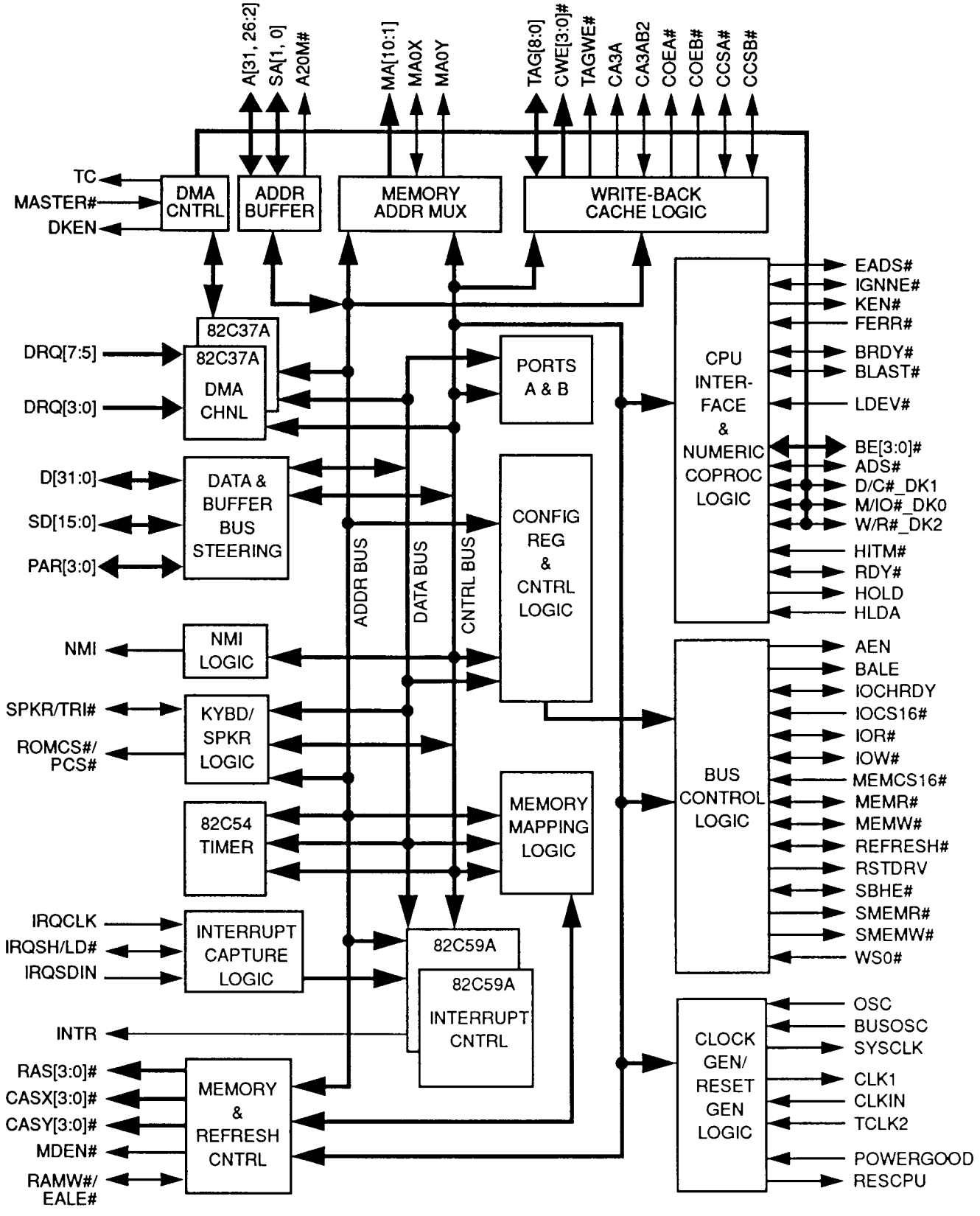


ORDER INFORMATION

Part Number	Package
VL82C481-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

VL82C481 BLOCK DIAGRAM



FEATURES (Cont.)

- Selectable slow DRAM refresh saves power
- On-chip write-back cache controller:
  - External tags
  - Direct map
  - Separate "dirty" RAM not required
  - 2-1-1-1 reads with two banks, 2-2-2-2 with one bank
  - 32 KB to 1 MB cache size
  - One wait state writes on cache-hits
  - Optional zero wait state writes supported
  - Optional one wait state reads supported
- Other Features:
  - Programmable for 10- or 16-bit internal I/O addressing
  - Programmable drive on the DRAM and ISA bus signals
  - Programmable memory access to define "fast-bus", local bus, slot bus, non-cacheable and write-protect areas
  - Input pin defines access to local bus devices
  - Optional keyboard command blocking for fast A20GATE and CPU reset
- 0.8-micron CMOS technology
- 208-lead MQFP (Metric Quad Flat Pack), 0°C to +70°C operating temperature

OVERVIEW

The VL82C481 Controller is designed to control 486DX or 486SX/487SX-based ISA bus systems operating at up to 40 MHz. It also supports 486-family CPUs that contain an integrated write-back cache (P24T, etc.). The VL82C481 replaces the following devices on the motherboard:

- Two 82C37A DMA controllers
- Two 82C59A interrupt controllers
- 82C54 timer
- 74LS612 memory mapper
- 82284 clock generator and ready interface
- 82288 bus controller
- The following controller blocks are also included on-chip: Memory/refresh controller
- Port B and NMI logic
- Bus steering logic
- Turbo Mode control logic
- Parity checking logic
- Parity generation logic
- Write-back, look-aside cache controller

The VL82C481 supports the Weitek 4167 numeric coprocessor.

The memory controller logic is capable of accessing up to 64 MB. There can be up to four banks of 256K, 1M, or 4M DRAMs used in a system. The VL82C481 can drive two banks without external buffering. Built-in Page Mode operation and up to two-way interleaving allow the PC designer to maximize system performance using low-cost DRAMs. Programmable DRAM timing is provided for RAS# precharge, RAS-to-CAS delay, and CAS# pulse width.

The VL82C481's write-back cache controller logic supports one or two banks of direct map write-back cache with external tag storage. The cache controller can perform 2-1-1-1 reads with two banks or 2-2-2-2 reads with one bank. It can also perform 3-2-2-2 cycle reads for support of slower SRAMs at higher frequencies. The VL82C481 can perform one wait state writes on cache-hits. An optional zero wait state write mode is provided for use with fast cache SRAMs. The cacheable DRAM range includes 2 MB up to 64 MB utilizing cache data SRAM sizes of 32 KB through 1 MB, respectively.

The HITM# input is provided to force the VL82C481 to abort DRAM or cache cycles when a hit on a dirty line in the CPU write-back cache is detected. The DRAM or cache cycle is subsequently restarted after the CPU has written back the dirty data.

Shadowing features are supported on 16K boundaries between A0000h and FFFFFh (640KB - 1MB). Simultaneous use of shadowed ROM and direct system board access is possible in a non-overlapping fashion throughout this memory space. Control over four access options is provided:

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

Three special programmable address regions are provided. The Fast Bus Clock Region allows accesses to certain memory regions at a faster ISA bus clock rate for fast on-board or off-board devices. A Non-Cacheable Region and/or a Write-Protected Region may be defined by a set of six registers that allow memory in the region 640 KB to 1 MB to be marked as non-cacheable and/or write-protected in increments of 16 KB. A further set of registers allows a memory range anywhere in the first 64 MB of memory to be marked as a DRAM region, an ISA bus region, or a local bus region, either cacheable or non-cacheable in increments of 2 KB, 64 KB, or 1 MB.

Further support for VL-Bus devices that reside on the local bus is provided through use of the LDEV# (Local Device) input, which deselects the VL82C481 during CPU cycles and causes the VL82C481 to generate VL-Bus memory cycles when active during DMA and Master Mode cycles. Also, a memory range anywhere in the first 64 MB of memory can be programmed via the internal mapping registers. This allows the VL82C481 to access a VL-Bus device as a CPU bus memory device during DMA or Master Mode transfers and deselect the VL82C481 during CPU cycles.

The VL82C481 handles system board refresh directly and also controls the timing of slot bus refresh. Refresh may be performed in three different modes: Synchronous, Asynchronous, or Decoupled Mode. In the Synchronous Mode, slot bus and on-board DRAM refresh cycles proceed simultaneously with all memory cycles held until both have completed. The Asynchronous Mode allows on- and off-board refreshes to be initiated simultaneously, but to complete asynchronously, allowing earlier access to DRAM. In the Decoupled Mode, a separate refresh counter is used for slot bus refresh, allowing on-board DRAM and system refreshes to proceed independently, with DRAM refreshes initiated during bus idle cycles. CAS-before-RAS refresh is also supported. Refreshes are staggered to minimize power supply loading and attenuate noise on the VDD and VSS pins. The VL82C481 supports the ISA bus standard refresh period of 15.625 µs as well as 125 µs.

The interrupt controller logic consists of two 82C59A megacells with eight interrupt request lines each. The two megacells are cascaded internally and three of the interrupt request inputs are connected to internal circuitry, so a total of 13 external interrupt request lines are available. These 13 interrupt request lines, plus the Weitek interrupt request line, the ten-channel check line, and the Turbo/Non-Turbo line are scanned in through one pin on the VL82C481. Two external 74LS166s are required for scanning in these 16 signals.

The interval timer includes one 82C54 counter/timer megacell. The counter/-timer has three independent 16-bit counters and six programmable counter modes.

The two DMA controllers are 82C37A compatible. Each controls data transfers between an I/O channel and on- or off-board memory. The DMA controllers can transfer data over the full 64 MB range available. Internal latches are provided for latching the middle address bits output by the 82C37A megacells on the data bus. The 74LS612 memory mappers are integrated to generate the upper address bits.

The VL82C481 can be programmed for asynchronous or synchronous operation of the ISA bus.

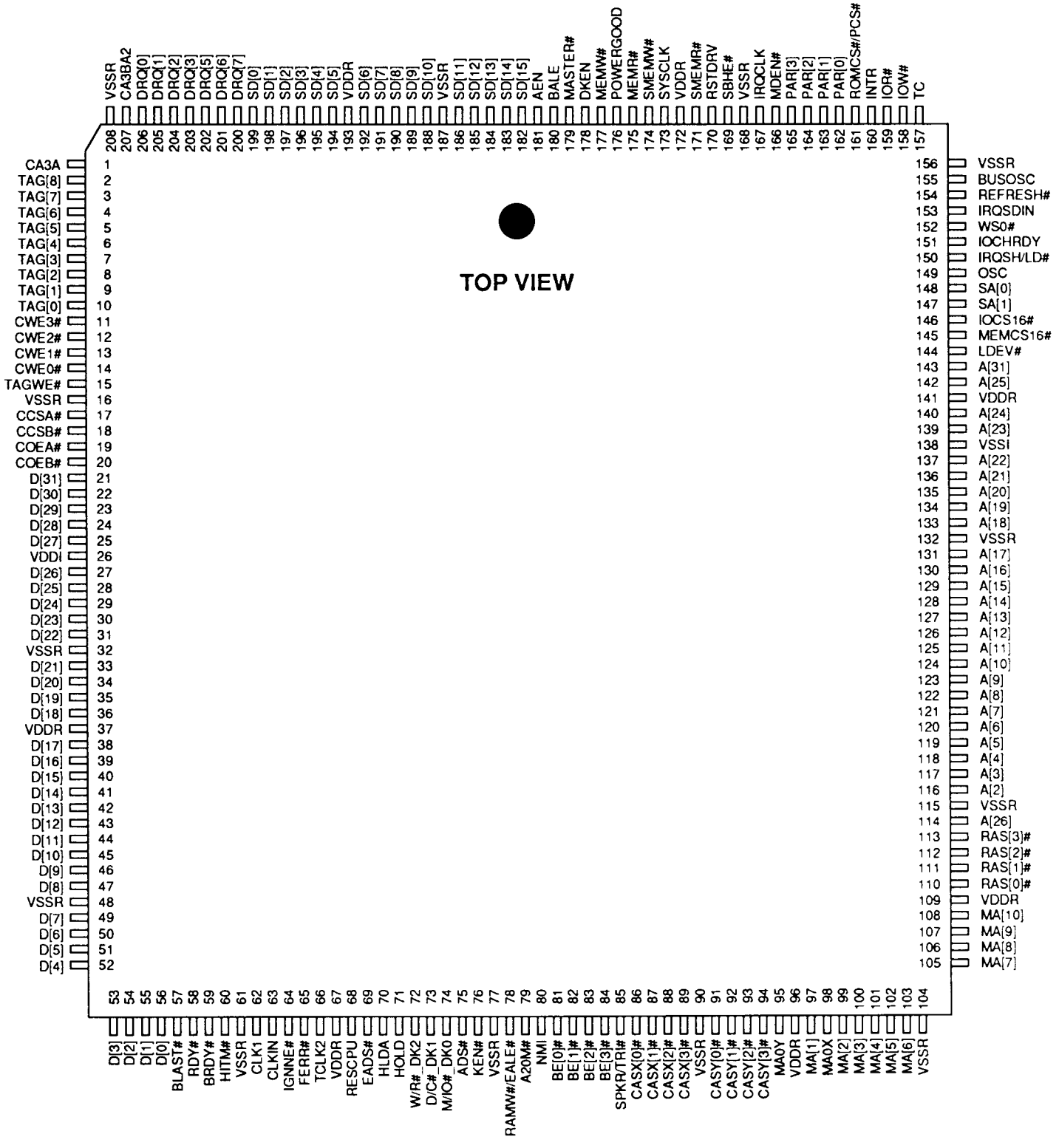
The VL82C481 also performs all of the data buffer control functions required for a 486-based ISA bus system. Under the control of the CPU, the VL82C481 routes data to and from the CPU local D bus, the internal XD bus, and the slots (SD bus). During CPU ISA bus reads, the data is latched for synchronization with the CPU. Parity is checked for D bus DRAM read operations. On power-on default, the chip does not generate parity for CPU writes to DRAM, but does generate cache write-back cycles. However, a mode is provided in which the VL82C481will generate parity during either CPU writes or VL master writes. Even parity is generated and checked.

When the DMA requestor or external bus master is the bus owner, the VL82C481 allows data transfer between the slot SD bus and the CPU local D bus. The chip also performs low-to-high and high-to-low byte swaps on the 16-bit SD bus. Parity is generated by the VL82C481 during DMA or Master Mode writes to on-board DRAM.

The VL82C481 Controller functions are programmable via a set of internal configuration registers. The state of various interface pins at reset is used to determine the default configuration.

The VL82C481 also provides a single input, SPKR/TRI#, to disable all of its outputs for board level testability.

VL82C481 PIN DIAGRAM



PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
1	CA3A	IO(3,6)		8	39	D[16]	IO	TTL	8
2	TAG[8]	IO	TTL	8	40	D[15]	IO	TTL	8
3	TAG[7]	IO	TTL	8	41	D[14]	IO	TTL	8
4	TAG[6]	IO	TTL	8	42	D[13]	IO	TTL	8
5	TAG[5]	IO	TTL	8	43	D[12]	IO	TTL	8
6	TAG[4]	IO	TTL	8	44	D[11]	IO	TTL	8
7	TAG[3]	IO	TTL	8	45	D[10]	IO	TTL	8
8	TAG[2]	IO	TTL	8	46	D[9]	IO	TTL	8
9	TAG[1]	IO	TTL	8	47	D[8]	IO	TTL	8
10	TAG[0]	IO	TTL	8	48	VSSR	GND		
11	CWE[3]#	IO(4)	TTL	8	49	D[7]	IO	TTL	8
12	CWE[2]#	IO(4)	TTL	8	50	D[6]	IO	TTL	8
13	CWE[1]#	IO(4)	TTL	8	51	D[5]	IO	TTL	8
14	CWE[0]#	IO(4)	TTL	8	52	D[4]	IO	TTL	8
15	TAGWE#	IO(4)	TTL	8	53	D[3]	IO	TTL	8
16	VSSR	GND			54	D[2]	IO	TTL	8
17	CCSA#	IO(1)	TTL	8	55	D[1]	IO	TTL	8
18	CCSB#	IO(1)	TTL	8	56	D[0]	IO	TTL	8
19	COEA#	O	TTL	8	57	BLAST#	IO	TTL	
20	COEB#	IO(3,6)		8	58	RDY#	IO(6)	TTL	8
21	D[31]	IO	TTL	8	59	BRDY#	IO(6)	TTL	8
22	D[30]	IO	TTL	8	60	HITM#	IO(5)	TTL	
23	D[29]	IO	TTL	8	61	VSSR	GND		
24	D[28]	IO	TTL	8	62	CLK1	O		24
25	D[27]	IO	TTL	8	63	CLKIN	I	CMOS	
26	VDDI	PWR			64	IGNNE#	IO(1,6)	TTL	8
27	D[26]	IO	TTL	8	65	FERR#	IO(6)	TTL	
28	D[25]	IO	TTL	8	66	TCLK2	I	CMOS	
29	D[24]	IO	TTL	8	67	VDDR	PWR		
30	D[23]	IO	TTL	8	68	RESCPU	O		8
31	D[22]	IO	TTL	8	69	EADS#	IO(6)	TTL	8
32	VSSR	GND			70	HLDA	I	TTL	
33	D[21]	IO	TTL	8	71	HOLD	O		8
34	D[20]	IO	TTL	8	72	W/R#_DK2	IO	TTL	8
35	D[19]	IO	TTL	8	73	D/C#_DK1	IO	TTL	8
36	D[18]	IO	TTL	8	74	M/IO#_DK0	IO	TTL	8
37	VDDR	PWR			75	ADS#	IO	TTL	8
38	D[17]	IO	TTL	8	76	KEN#	IO(5)	TTL	

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
77	VSSR	GND			115	VSSR	GND		
78	RAMW#/EALE#	IO(1)	TTL	24/48	116	A[2]	IO	TTL	8
79	A20M#	O		8	117	A[3]	IO	TTL	8
80	NMI	O		8	118	A[4]	IO	TTL	8
81	BE[0]#	IO	TTL	8	119	A[5]	IO	TTL	8
82	BE[1]#	IO	TTL	8	120	A[6]	IO	TTL	8
83	BE[2]#	IO	TTL	8	121	A[7]	IO	TTL	8
84	BE[3]#	IO	TTL	8	122	A[8]	IO	TTL	8
85	SPKR/TRI#	IO(6)	TTL	24	123	A[9]	IO	TTL	8
86	CASX[0]#	O(6)		12	124	A[10]	IO	TTL	8
87	CASX[1]#	O(6)		12	125	A[11]	IO	TTL	8
88	CASX[2]#	O(6)		12	126	A[12]	IO	TTL	8
89	CASX[3]#	O(6)		12	127	A[13]	IO	TTL	8
90	VSSR	GND			128	A[14]	IO	TTL	8
91	CASY[0]#	O(6)		12	129	A[15]	IO	TTL	8
92	CASY[1]#	O(6)		12	130	A[16]	IO	TTL	8
93	CASY[2]#	O(6)		12	131	A[17]	IO	TTL	8
94	CASY[3]#	O(6)		12	132	VSSR	GND		
95	MA0Y	IO-PU(3)	TTL	12/24	133	A[18]	IO	TTL	8
96	VDDR	PWR			134	A[19]	IO	TTL	8
97	MA[1]	O		24/48	135	A[20]	IO	TTL	8
98	MA0X	IO(1,6)	TTL	12/24	136	A[21]	IO	TTL	8
99	MA[2]	O		24/48	137	A[22]	IO	TTL	8
100	MA[3]	O		24/48	138	VSSI	GND		
101	MA[4]	O		24/48	139	A[23]	IO	TTL	8
102	MA[5]	O		24/48	140	A[24]	IO	TTL	8
103	MA[6]	O		24/48	141	VDDR	PWR		
104	VSSR	GND			142	A[25]	IO	TTL	8
105	MA[7]	O		24/48	143	A[31]	IO	TTL	8
106	MA[8]	O		24/48	144	LDEV#	I	TTL	
107	MA[9]	O		24/48	145	MEMCS16#	I	TTL	
108	MA[10]	O		24/48	146	IOCS16#	I	TTL	
109	VDDR	PWR			147	SA[1]	IO	TTL	12/24
110	RAS[0]#	O		12/24	148	SA[0]	IO	TTL	12/24
111	RAS[1]#	O		12/24	149	OSC	I	TTL	
112	RAS[2]#	O		12/24	150	IRQSH/LD#	IO(1)	TTL	8
113	RAS[3]#	O		12/24	151	IOCHRDY	IO-OD(2)	TTL	8
114	A[26]	IO	TTL	8	152	WS0#	I	TTL	

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
153	IRQSDIN	I	TTL		181	AEN	O		12/24
154	REFRESH#	IO-OD(2)	TTL-S	8	182	SD[15]	IO	TTL	12/24
155	BUSOSC	I(6)	TTL		183	SD[14]	IO	TTL	12/24
156	VSSR	GND			184	SD[13]	IO	TTL	12/24
157	TC	O		12/24	185	SD[12]	IO	TTL	12/24
158	IOW#	IO(2)	TTL	12/24	186	SD[11]	IO	TTL	12/24
159	IOR#	IO(2)	TTL	12/24	187	VSSR	GND		
160	INTR	O		8	188	SD[10]	IO	TTL	12/24
161	ROMCS#/PCS#	IO(4)		8	189	SD[9]	IO	TTL	12/24
162	PAR[0]	IO	TTL	8	190	SD[8]	IO	TTL	12/24
163	PAR[1]	IO	TTL	8	191	SD[7]	IO	TTL	12/24
164	PAR[2]	IO	TTL	8	192	SD[6]	IO	TTL	12/24
165	PAR[3]	IO	TTL	8	193	VDDR	PWR		
166	MDEN#	O		8	194	SD[5]	IO	TTL	12/24
167	IRQCLK	I	TTL		195	SD[4]	IO	TTL	12/24
168	VSSR	GND			196	SD[3]	IO	TTL	12/24
169	SBHE#	IO		12/24	197	SD[2]	IO	TTL	12/24
170	RSTDRV	O		12/24	198	SD[1]	IO	TTL	12/24
171	SMEMR#	O(2)		12/24	199	SD[0]	IO	TTL	12/24
172	VDDR	PWR			200	DRQ[7]	I(6)	TTL-S	
173	SYSCLK	O		12/24	201	DRQ[6]	I(6)	TTL-S	
174	SMEMW#	O(2)		12/24	202	DRQ[5]	I(6)	TTL-S	
175	MEMR#	IO(2)	TTL	12/24	203	DRQ[3]	I(6)	TTL-S	
176	POWERGOOD	I(6)	TTL-S		204	DRQ[2]	I(6)	TTL-S	
177	MEMW#	IO(2)	TTL	12/24	205	DRQ[1]	I(6)	TTL-S	
178	DKEN	O	TTL	8	206	DRQ[0]	I(6)	TTL-S	
179	MASTER#	I	TTL		207	CA3BA2	IO(1,6)	TTL	8
180	BALE	IO	TTL	12/24	208	VSSR	GND		

Notes: (1) These pins are input during power-on reset and are used to configure the VL82C481.
(2) These pins require an external pull-up resistor.
(3) These pins are used to enter test mode on power-on reset when made low.
(4) These pins are inputs only during power-on reset. They are inputs for internal system setup only.
(5) Indicates a high-impedance with approximately 10 KΩ minimum resistance to VSS (internal pull-down resistor on pin).
(6) Indicates a high-impedance with approximately 10 KΩ minimum resistance to VDD (internal pull-up resistor on pin).

Legend:

CMOS	CMOS-compatible input	OD	Open drain
I	Input pin	PWR	Power supply pin
IO	Bidirectional pin	S	Indicates a Schmitt-trigger input with hysteresis for noise immunity.
GND	Ground pin	TTL	TTL-compatible input
O	Output pin		

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A[31], A[26], A[25], A[24], A[23], A[22:18], A[17:2]	143, 114, 142, 140, 139, 137:133, 131:116	IO-TTL	Address bus bits 31, 26 through 21, and 19 through 2 - The bidirectional address bus is driven by the bus master. It is driven out by the VL82C481 during Non-Master Mode DMA and refresh cycles when HLDA is active and MASTER# is inactive. The signals A[25:2] allow access to 64 MB of system memory. A[31] and A[26] are used for disabling DRAM access so that system ROM and the VL-Bus devices can be accessed. **A[31] A[26]** 0 0 = normal memory access, up to 64MB DRAM selected 0 1 = other bus slaves (VL82C481 is deselected, 7 µs time-out) 1 0 = other bus slaves (VL82C481 is deselected, 7 µs time-out) 1 1 = ROM and aliased ISA bus access
ADS#	75	IO-TTL	Address Status: Active low ADS# is driven by the CPU as an indication that the address and control signals currently supplied by the CPU are valid. This signal is used internally to indicate that the data and command are valid and determine the beginning of a memory or I/O cycle. ADS# is driven by the VL82C481 when HLDA is active and is made low for one CPU clock cycle at the beginning of DMA or Master Mode cycles when a local bus region is selected by the PMR Registers.
BE[3:0]#	84:81	IO-TTL	Byte Enable bits 3 through 0 - These signals are normally inputs to the VL82C481 and indicate which bytes on D[31:0] are involved in a memory or I/O access. They are ignored during all DRAM reads. They are driven by the VL82C481 when HLDA is active and indicate which one or two bytes are involved in an 8- or 16-bit DMA or Master Mode transfer between slot I/O and a local bus device.
BLAST#	57	IO-TTL	Burst Last - This is an input to the VL82C481 indicating when to terminate the current burst cycle, if the length of the burst cycle is less than four double-words. It is driven low by the VL82C481 when HLDA is active, however, the VL82C481 does not support the burst mode during DMA or Master Mode cycles. It is used as an input only during one of the test modes.
A20M#	79	O	A20 Mask - This asserted output signal instructs the CPU to mask address bit 20 for all operations.
BRDY#	59	IO-TTL[6]	Burst Ready - The active low BRDY# signal indicates to the CPU that the current DRAM cycle is complete. It is driven low when valid data has been presented to the CPU in response to a read command or when data has been accepted in response to a write command from the CPU. The VL82C481 drives BRDY# on all local bus DRAM and cache read accesses. It never drives it in response to slot bus accesses (see RDY# definition). The VL82C481 enables the BRDY# three-state output only when it needs to drive it low, and leaves it enabled for just **one-half** CPU clock cycle after it has driven it high again. When HLDA is active, BRDY# is an input to the VL82C481 and may be driven by a local bus device to terminate Local Bus DMA or Master Mode cycles. This pin has an internal pull-up resistor
CLK1	62	O	1X Clock - This output is a CMOS level pulse train whose frequency is normally one-half that of the TCLK2 signal. It is used by the VL82C481, 486, and other on-board logic. Its frequency can be programmed to slower rates for Non-Turbo Mode operation.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CLKIN	63	I-CMOS	Input Clock - CLKIN is the fundamental clock input to the VL82C481. It must be the same clock as that supplied to the 486.
M/IO#_DK0	74	IO-TTL	Memory Input/Output and DMA Acknowledge 0 - When HLDA is low, M/IO#_DK0 is driven by the local bus master and is decoded with D/C#_DK1 and W/R#_DK2 to indicate the type of bus cycle requested. When HLDA is high, this is an output signal which, along with D/C#_DK1 and W/R#_DK2, represents the encoded channel number being serviced at the beginning of DMA or Master Mode acknowledge cycles until DKEN goes active, after which it is driven high during the rest of the DMA cycle or to the memory or I/O status during Master Mode cycles.
D/C#_DK1	73	IO-TTL	Data/Control and DMA Acknowledge 1 - When HLDA is low, D/C#_DK1 is driven by the local bus master and is decoded with M/IO#_DK0 and W/R#_DK2 to indicate the type of bus cycle requested. When HLDA is high, this is an output signal which, along with M/IO#_DK0 and W/R#_DK2, represents the encoded channel number being serviced at the beginning of DMA or Master Mode acknowledge cycles until DKEN goes active, after which it is driven high during the rest of the DMA or Master Mode cycle.
W/R#_DK2	72	IO-TTL	Write/Read and DMA Acknowledge 2 - When HLDA is low, W/R#_DK2 is driven by the local bus master and is decoded with D/C#_DK1 and M/IO#_DK0 to indicate the type of bus cycle requested. When HLDA is high, this is an output signal which, along with D/C#_DK1 and M/IO#_DK0, represents the encoded channel number being serviced at the beginning of DMA or Master Mode acknowledge cycles until DKEN goes active, after which it is driven to the read or write status during the rest of the DMA or Master Mode cycle.
D[31:0]	21:25, 27:31, 33:36, 38:47, 49:56	IO-TTL	CPU Data bus bits 31 through 0 - This is the data bus directly connected to the CPU and other external devices.
EADS#	69	IO-TTL[6]	External Address - This signal indicates a primary cache invalidation address is on the address bus. It is driven low by the VL82C481 to perform primary cache invalidations during DMA and Master Mode cycles. It is three-stated when the VL82C481 does not own the bus (i.e., DMA or Master Mode cycles), except when optionally used for invalidating write-protected memory locations and in the Non-Turbo Mode. It is monitored during VL-Bus Master cycles in write-back cache mode to determine when HITM# is to be sampled.
FERR#	65	IO-TTL[6]	Floating Point Error - The FERR# input indicates a floating point error. When active, it generates an interrupt IRQ13 internal to the VL82C481. This input pin is active low. FERR# has an internal pull-up resistor. It is used as an output only in one of the test modes.
HITM#	60	IO-TTL[5]	Hit Modified - The HITM# input is used to detect a hit on a modified line in the CPU write-back cache during DMA and Master Mode accesses to DRAM, in which case it causes the VL82C481 to back off the bus to permit the CPU write-back. It is also monitored during VL-Bus master accesses to DRAM, and causes the access to be aborted when active. It is also used to detect the presence of a CPU with write-back cache during power-on reset; if high during POR, then a write-back CPU is present, if low during POR then a write-back CPU is not present. It has an internal pull-down resistor to force it low when not connected. It is also used as a test-mode output.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
HLDA	70	I-TTL	Hold Acknowledge - The active high HLDA signal is issued by the CPU in response to the HOLD driven by the VL82C481. It indicates that the CPU is floating its outputs to the high impedance state so that another master can take control of the bus.
HOLD	71	O	Hold Request - The active high HOLD pin is driven by the VL82C481 to the CPU. It indicates that a bus master, such as a DMA or refresh controller, is requesting control of the bus. This signal is synchronized to CLKIN.
IGNNE#	64	IO-TTL(6)	Ignore Numeric Error Output [POR input] - This active low output instructs the CPU to ignore the present numeric error. It is enabled when a dummy write is performed to either port F0h or F1h while FERR# is active. At power-on reset (POR), this pin is used to set SA[1] timing.
INTR	160	O	Interrupt Request - An active high output used to interrupt the CPU. It is generated by the 82C59A megacells any time a valid interrupt request input is received.
KEN#	76	IO-TTL(5)	Cache Enable - The KEN# signal is an output which determines whether the current cycle is cacheable in the primary cache. This signal is normally low, but is driven inactive during the first and subsequent T2 cycles of all CPU memory accesses defined as non-cacheable. It is an input only when one of the test modes is enabled.
NMI	80	O	Non-Maskable Interrupt - An active high output which indicates to the CPU that an external non-maskable interrupt has been generated. This signal is asserted by either a parity error or an I/O channel error. The NMI output is enabled by resetting the MSB (most significant bit) of I/O port 70h. NMI is disabled on reset.
RDY#	58	IO-TTL(6)	Non-Burst Ready - The active low RDY# signal is driven by the VL82C481 as an indication that the current memory or I/O slot bus cycle or cache write cycle is complete. The VL82C481 enables the RDY# three-state output only when it needs to drive it low and leaves it enabled for just one-half CPU clock cycle after it has driven it high again. When HLDA is active, RDY# is an input to the VL82C481 and may be driven by local bus devices to terminate DMA and Master Mode cycles. This pin has an internal pull-up resistor
RESCPU	68	O	Reset CPU - This active high signal is used to reset the CPU and is asserted in response to one of the following: 1. A dummy read from I/O port EFh. 2. The LSB (least significant bit) of Port A is set to '1 by an active write. 3. The POWERGOOD signal changes state. 4. Shutdown command. RESCPU is synchronized to CLKIN.
TCLK2	66	I-CMOS	Clock - This input is connected to a crystal oscillator whose frequency is twice the system frequency. The signal is divided down in frequency and sent to the CLK output.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
CASX[3:0]#, CASY[3:0]#	89:86, 94:91	O(6) O(6)	Column Address Strobes - The CASX[3:0]# and CASY[3:0]# signals generate active low column address strobes for DRAM banks during on-board memory bus cycles. The active period for these signals is determined by the number of wait states and the configuration mode. These pins have internal pull-up resistors.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MA[10:1]	108:105, 103:99, 97	O	Memory Address bus bits 10 through 1 - The MA[10:1] address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the local CPU bus address. They allow addressing of up to 64 MB of memory by the VL82C481.
MA0X	98	IO-TTL[1,6]	Memory Address bus bit 0, Banks 0 and 2 (POR input) - MA0X is a multiplexed row/-column address bit for Banks 0 and 2. It is interleaved with MA0Y to ensure that DRAM setup and hold times are met for A[3] during fast burst mode interleave. At power-on reset it selects high speed operation when low.
MA0Y	95	IO-TTL[3,6]	Memory Address bus bit 0, Banks 1 and 3 (POR input) - MA0Y is a multiplexed row/-column address bit for banks 1 and 3. It is interleaved with MA0X to ensure that DRAM setup and hold times are met for A[3] during fast burst mode interleave This pin is an input during power-on reset and selects a test-mode when low. It has an internal pull-up resistor.
MDEN#	166	O	Memory Data Word Enable - An active low signal which enables the output of the memory data buffers.
PAR[3:0]	165:162	IO-TTL	Parity bits 0 through 3 - Each parity bit signal is associated with one byte of the data bus. Even parity is generated on PAR[3:0] and written to memory along with their corresponding bytes during DMA, master and cache write-back operations. During CPU write operations to memory, the parity bit pins may be three-stated to allow the CPU to generate parity, or they may be selected as outputs to make the VL82C481 generate parity for CPU writes. During memory read operations these pins become inputs and are used along with their respective data bytes to determine whether a parity error has occurred.
RAMW#/EALE#	78	IO-TTL	RAM Write (output) and Early Address Latch Enable [POR input] - This active low output controls DRAM memory write enable and buffer direction, except during ISA bus cycles and refresh cycles. During ISA bus cycles and at the start of refresh, this signal functions as Early Address Latch Enable for systems that use the VL82C113A (VL82C114 does not require EALE#). RAMW#/EALE# is forced low during the start of a refresh cycle or ISA bus cycle; it is driven high when BALE is high for all CPU slot ISA bus cycles. At power-on reset (POR) this pin is used to set system and slot BIOS ROM location (ROMMOV2, ROMSET[6] Register).
RAS[3:0]#	110:113	O	Row Address Strobe bits 3 through 0 - These signals are sent to each of the four DRAM banks to strobe in the row address during on-board memory bus cycles.
CACHE CONTRTOLLER INTERFACE SIGNALS			
TAG[8:0]	10:2	IO-TTL	Tag Data bus bits 8 through 0 - A private bus for communication of tags between the VL82C481 and the tag RAM. TAG[8] has an internal pull-up resistor.
CWE[3:0]#	11:14	IO[4]	Cache Write Enable bits - These four signals enable writes to the cache SRAMs, Banks A and B (one enable per byte).
TAGWE#	15	IO[4]	Cache Tag Write Enable - This active low signal enables writes to the tag SRAM for updates during line-fills or clean-writes.
CA3A	1	IO-TTL[3,6]	Cache Address 3, Bank A (output) POR input - This output signal drives the cache Bank A, Address 3. This pin is an input during power-on reset and selects a test mode when low. It has an internal pull-up resistor.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CA3BA2	207	IO-TTL[1,6]	Cache Address 3, Bank B or Cache Address 2, Bank A (output) - In Double Cache Data Bank Mode, this output signal drives the cache Bank B Address 3. In Single Cache Data Bank Mode, this output drives the cache Bank A Address 2. This pin selects the system ROM width during power-on reset (16 bits when low, 8 bits when high). It has an internal pull-up resistor.
CCSA#	17	IO-TTL[1]	Chip Select, Cache Bank A [POR Input] - This active low output signal enables the cache data SRAMs in Bank A during read/write access. At power-on reset (POR), this pin is used along with CCSB# to set the DRAM interface output drive current.
CCSB#	18	IO-TTL[1]	Chip Select, Cache Bank B [POR Input] - This active low output signal enables the cache data SRAMs in Bank B during read/write access. At power-on reset (POR), this pin is used along with CCSA# to set the DRAM interface output drive current.
COEA#	19	O	Cache Output Enable, Bank A [POR Input] - This active low output signal enables the bus drive circuitry of cache data SRAMs in Bank A.
COEB#	20	IO-TTL[3,6]	Cache Output Enable, Bank B - This active low output signal enables the bus drive circuitry of cache data SRAMs in Bank B. This pin is an input during power-on reset and selects a test mode when low. It has an internal pull-up resistor.
PERIPHERAL INTERFACE SIGNALS			
LDEV#	144	I-TTL	Local Bus Device Access - On CPU accesses, this signal must be made low by a local bus device if a CPU access is to a local bus device. When active, it causes the VL82C481 to be deselected. The time by which LDEV# must be asserted depends on the configuration register programming and the access address.
ROMCS#/PCS#	161	IO[4]	ROM Chip Select and Peripheral Chip Select - During ISA bus CPU cycles, this signal is used as the ROM chip select. All other times, it is used as the peripheral chip select for the keyboard controller and real-time clock. This pin is an input during power-on reset to control one of the test modes (it is ignored at POR during normal operation).
POWERGOOD	176	I-TTL-S[6]	System Power-On Reset - An active high input which indicates that the power to the board is stable. A Schmitt-trigger input is used. This allows the input to be connected directly to an RC network.
SPKR/TRI#	85	I-TTL[6]	Speaker and Three-state - The active high SPKR output drives an externally buffered speaker. This signal is an input when the POWERGOOD input is low. If sampled low, it forces the VL82C481 into the Three-State Mode where all outputs and bidirectional pins are driven to a high impedance state. This pin has an internal pull-up resistor.
BUS INTERFACE SIGNALS			
AEN	181	O	Address Enable - AEN is an active high output that indicates a DMA transfer cycle to the I/O resources on the bus. It is asserted only when the DMA controller is the bus owner (HLDA = '1, MASTER# = '1). The I/O resource with an active DMA acknowledge signal should only respond to the I/O command lines and all the other I/O resources should ignore the commands.
BALE	180	O	Bus Address Latch Enable - BALE is an active high pulse which is generated at the beginning of any bus cycle initiated by the CPU. It indicates when the SA[19:0], LA[23:17], AEN, and SBHE# signals are valid. BALE is forced high any time HLDA is high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUSOSC	155	I-TTLI[6]	System Bus Clock - This signal is supplied by an external oscillator. It has a nominal 50% duty cycle and normally a frequency of 16 MHz. It is used for ISA bus operations. If an oscillator is connected to this pin, SYSCLK can be programmed to be BUSOSC +2, +4, +6, or +8. If SYSCLK is to be derived from TCLK2, the BUSOSC is held high or low and is used in conjunction with the CLKCTL Register to determine the clock divider value. BUSOSC has an internal pull-up resistor.
DKEN	178	O	DMA Acknowledge Enable (output) - DKEN enables an external 3-to-8 decoder for the generation of the DMA acknowledge signals from M/IO#_DK0, D/C#_DK1 and W/R#_DK2 when these signals are valid at the beginning of a DMA cycle. It is also used to latch the DMA acknowledges when active (high).
DRQ[7:5], DRQ[3:0]	200:202, 203:206	I-TTL-S[6]	DMA Request bits 7 through 5 and 3 through 0 - The asynchronous DMA request inputs are used by external devices to indicate when they need service from the internal DMA controllers. DRQ[3:0] are used for transfers between 8-bit I/O adapters and system memory. DRQ[7:5] are used for transfers between 16-bit I/O adapters and system memory. DRQ[4] is not available externally as it is used to cascade the two DMA controllers together. All DRQ pins have internal pull-up resistors.
IOCHRDY	151	IO-OD-TTL[2]	I/O Channel Ready - The IOCHRDY input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that can not present read data or strobe in write data in this amount of time must use IOCHRDY to extend these cycles. In DMA Mode, this pin is always driven low by the VL82C481 that generate local bus cycles to allow for local bus latency; the VL82C481 never drives IOCHRDY high, but three-states it when not driven low. This pin requires an external 10K pull-up resistor
IOCS16#	146	I-TTL	16-Bit I/O Chip Select - This input determines when a 16-to-8 bit conversion is needed for CPU accesses. A conversion is done any time the VL82C481 requests a 16-bit I/O cycle and IOCS16# is sampled high. A command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long when a conversion is needed. If sampled low, an I/O access is performed in one wait state with one command delay inserted. The IOCS16# signal is ignored by the DMA and refresh controller for DMA and refresh cycles, respectively.
IOW# IOR#	158 159	IO-TTL[2] IO-TTL[2]	I/O Read I/O Write IOR# and IOW# are active low inputs when an external bus master is in control (HLDA = '1, MASTER# = '0). They function as outputs at all other times. When HLDA is low, they are driven by the internal ISA bus controller. During DMA transfer cycles (HLDA = '1, MASTER# = '1), they are driven by the 82C37A DMA controllers. They are inactive during a refresh cycle. Both the pins require external 10K pull-up resistors.
IRQSDIN	153	I-TTL	Interrupt Request Data In - This input signal accepts the scanned asynchronous interrupt requests [IRQs] from external 74LS166 shift registers into the 82C59A megacells. IRQ[0], IRQ[2] and IRQ[13] are not available as external inputs because

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
			they are used internally. All IRQ inputs pins except IRQ[8]# are active high. NMI is not a scanned input. The following interrupt requests are captured by the scan input: • IRQ[15], IRQ[14], IRQ[12:9], IRQ[8]#, IRQ[7:1] • WEIRQ - Weitek numeric coprocessor error • TURBO - Determines CPU speed. Low = slow, high = full speed. Its state may be read from the NTBREF Register. The hold signals to the 486 are continuously generated in order to slow its operation. • IOCHCK# - I/O bus error. If I/O checking enabled, IOCHCK# assertion by a peripheral device generates an NMI to the CPU if bit 3 of Port B is set to '0. The state of the IOCHCK# signal can be read as data bit 6 (CHAN_CHK) in Port B.
IRQCLK	167	I-TTL	Interrupt Request Scan Clock - This signal is the input clock to the interrupt request scanner within the VL82C481. It is the same signal used to clock the external 74LS166 shift registers to shift the captured interrupt information into the VL82C481.
IRQSH/LD#	150	IO-TTL(1)	Interrupt Request Load and Shift Control [POR input] - When low, this signal causes the external 74LS166 interrupt shift registers to load new interrupt information when clocked; when high, it causes the shift registers to shift when clocked. Load (IRQSH/LD# low) occurs once every seventeenth IRQCLK. At power-on reset (POR), this pin is used to set the slot drive current (SLTDRV, BUSCTL[5]).
MASTER#	179	I-TTL	Master - This active low input is driven by an external device to disable the VL82C481's DMA controllers and obtain access to the system bus. When asserted, it indicates that an external bus master has control of the bus. During non-ISA device read or write cycles it may be driven low by external logic to indicate when a VL-Bus master (as opposed to the CPU) is making the request. This is used for snoop control.
MEMCS16#	145	I-TTL	16-Bit Memory Chip Select - This active low input is used to determine when a 16-to-8 bit conversion is needed for CPU accesses. A conversion is done anytime the VL82C481 requests a 16-bit memory cycle and MEMCS16# is sampled high. If sampled high with the BUSCTL Register in the default configuration, a command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long. If sampled low, a memory access is performed in one wait state with no command delays inserted. The MEMCS16# signal is ignored by the DMA and refresh controller for DMA and refresh cycles, respectively.
MEMR# MEMW#	175 177	IO-TTL(2) IO-TTL(2)	Memory Read Memory Write The active low signals MEMR# and MEMW# are inputs when an external bus master is in control (HLDA = '1, MASTER# = '0). They are outputs at all other times. When HLDA is low MEMW# is driven from the ISA bus controller. They are driven by internal 82C37A DMA controllers during DMA cycles. Both the pins require external 10K pull-up resistors.
OSC	149	I-TTL	Oscillator Input - OSC is the buffered input of the external 14.31818 MHz oscillator with a duty cycle of 45-55%.
REFRESH#	154	IO-OD TTL-S(2)	Memory Refresh - The REFRESH# signal is pulled low whenever a refresh cycle is initiated. An external bus master activates this signal when it requires a refresh cycle from the refresh controller. The internal refresh controller activates this line every 15.6 µs to prevent loss of DRAM data. REFRESH# is an open-drain output capable of sinking 24 mA and requires an external pull-up resistor.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
RSTDRV	170	O	Reset - This active high output is a system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSOSC input. On reset, this signal remains high for at least as long as the RESCPU signal. It may therefore be used to drive the 486's AHOLD input to initiate a 486 self-test sequence on power-on reset only.
SA[1:0]	147:148	IO-TTL	System Address bus bits 1 and 0 - These signals represent the lower two bits of the system address bus. They act as inputs when an external bus master is in control (HLDA = '1, MASTER# = '0) and are outputs at all other times. When HLDA is low, SA[1:0] are generated by decoding the CPU byte enables, BE[3:0]#. They are driven by the 82C37A DMA controllers during DMA transfer cycles. SA[0] is always connected directly to the ISA bus. SA[1] is connected to the ISA bus if discrete SA buffers or the VL82C114 is used. If the VL82C113A is used, then SA[1] is connected only to the A[1] input of the VL82C113A (which then drives the ISA bus SA[1] signal). IGNNE# is used to set SA[1] timing at power-on reset for use with/without the VL82C113A.
SBHE#	169	IO-TTL	System Byte High Enable - An active low SBHE# indicates that valid data is on the upper byte of system data bus, SD[15:8]. Its functionality is similar to that of the SA[1:0] signals. SBHE# is forced low during 16-bit DMA cycles and is the complement of SA[0] during 8-bit DMA cycles.
SD[15:0]	182:186, 188:192, 194:199	IO-T	System Data bus bits 15 through 0 - The bidirectional SD[15:0] signals are directly connected to the slots.
SMEMR#	171	O(2)	System Memory Read
SMEMW#	174	O(2)	System Memory Write
			The SMEMR# and SMEMW# outputs are active during memory read and write cycles, respectively, when the address is below 1 MB.
			Both the pins require external 10K pull-up resistors.
SYSCLK	173	O	System Clock - The SYSCLK output is 1/2, 1/3, 1/4, 1/6, or 1/8 the frequency of TCLK2 or BUSOSC depending on the BUSOSC pin status and the five lower bits in the CLKCTL Register. The bus control signals BALE, IOR#, IOW#, MEMR#, and MEMW# are synchronized to SYSCLK.
TC	157	O	Terminal Count - This active high output indicates that one of the DMA channels has transferred all data.
WS0#	152	I-TTL	Wait State Terminate - An active low input which indicates a shorter access cycle. It is pulled low by a peripheral on the slot bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWER AND GROUND PINS			
VSSI	138	GND	Core Ground connection - 0 volts.
VSSR	16, 32, 48, 61, 77, 90, 104, 115, 132, 156, 168, 187, 208	GND	Ring Ground connection - 0 volts.
VDDI	26	PWR	Core Power connection - Nominally +5 volts.
VDDR	37, 67, 96, 109, 141, 172, 193	PWR	Ring Power connection - Nominally +5 volts.

Note: Refer to the Notes and Legend on 8 for details on the Signal Type.

REGISTER SUMMARY

SYSTEM CONFIGURATION

The VL82C481 offers hardware configured options to ensure that it resets to a usable state with the various physical configurations available. During reset, the output pins listed in Table become inputs and their value is loaded into the configuration registers as shown or are used to configure the system. There is no internal default for these bits, therefore the pins shown must be set to the required value during reset.

TABLE 1. SYSTEM CONFIGURATION INITIALIZATION

Pin Name	Register Name	Register Bit	Bit Name	Functional Description
CCSB#, CCSA#	RAMSET	2, 1	RAMDRV0, RAMDRV1	**RAMDRV [1:0]** / **MA[10:1], RAMW#** / **MA0X, MA0Y** / **RAS#** '00 — 12 mA — 12 mA — 12 mA '01 — 24 mA — 12 mA — 12 mA '10 — 24 mA — 24 mA — 12 mA '11 — 24 mA — 24 mA — 24 mA
RAMW#/EALE#	ROMSET	6	ROMMOV2	System and Slot BIOS ROM Move: '0 = D Bus '1 = SD Bus
CA3BA2 (weak PU)	ROMSET	7	ROMWID	ROM Width: '0 = 16-bit '1 = 8-bit
IRQSH/LD#	BUSCTL	5	SLTDRV	Slot Current Drive: '0 = 12 mA '1 = 24 mA
IGNNE# (weak PU)	-	-	-	SA1 Timing during 32-bit ISA Conversion Cycles: '0 = SA1 generated as normal for when it is connected directly to the ISA bus. '1 = SA1 generated early in 32 => 16 or 32 => 8-bit conversion cycles for VL82C107 or VL82C113A compatibility
MA0X (weak PU)	XCTL	6	HSPD	Frequency of Operation: 0 -> High frequency (above 40 MHz) (sets HSPD bit in XCTL when low, which adds extra wait states to DRAM cache, causes KEN# generation to be delayed, and adds synchronization delay to EADS#, RDY#) 1 -> Normal Frequency (up to 40 MHz)
HITM# (weak PD)	RAMSET	6	P24T	Selects 486 operating mode 0 -> Normal 486 Mode 1 -> P24T Mode **Note:** P24T Mode is entered if this input goes high at any time, regardless of reset. Ignored if MA0Y = '0 at POR.

Note: CA3A [CK2], MA0Y [VSN], COEB# [SNC], and ROMCS# [NPX] are all used to enter test modes at POR when made low. These signals have internal pull-ups; no external resistors are required for normal operation.

INDEXED CONFIGURATION REGISTER FORMATS

The following diagrams show the Indexed Configuration Register formats. Power-on reset values are shown above the diagrams for each register or set of registers.

TABLE 2. INDEXED CONFIGURATION REGISTER FORMATS

Index Port (R/W) — **ECh**

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
Index Address of a Configuration Register							

Data Port (R/W) — **EDh**

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
Data for a Configuration Register							

Version - VER (R-O) — **00h**

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0
Product Code						Device Version	

DRAM Programmable Timing - RAMTMG (R/W) — **01h**

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

TSTRT[1:0]	TRP[1:0]	TRCD[1:0]	TCAS[1:0]
Earliest Cycle Start Point 00 = Begin first T2 01 = Mid first T2 1X = End first T2	RAS Precharge 00 = 1T 01 = 2T 10 = 3T 11 = 4T	RAS/CAS Delay 00 = 1T 01 = 2T 10 = 3T 11 = 4T	CAS Width Read/Write Cache Disabled: 00 = 1T (R), 1T (W) 01 = 1.5T (R), 1T (W) 10 = 2T (R), 1T (W) 11 = 2T (R), 2T (W) Cache Enabled or XCTL[6] (HSPD bit) = 1: 00 = 2T (R), 1T (W) 01 = 2T (R), 1T (W) 10 = 3T (R), 1T (W) 11 = 3T (R), 2T (W)

INDEXED CONFIGURATION REGISTER FORMATS (Cont.)

DRAM Configuration Register 0 - RAMCFG0 (R/W) — 02h

7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	0
	DRAM Bank 1 Type		S/D 1		DRAM Bank 0 Type		S/D 0

DRAM Configuration Register 1 - RAMCFG1 (R/W) — 03h

7	6	5	4	3	2	1	0
1	0	0	0	1	0	0	0
	DRAM Bank 3 Type		S/D 3		DRAM Bank 2 Type		S/D 2

00 = None 10 = 1M
01 = 256K 11 = 4M

SIMM Side:
0 = Single
1 = Double

DRAM Control Register - RAMSET (R/W) — 04h

7	6	5	4	3	2	1	0
0	0	0	0	HITM#	CCSB#	CCSA#	0

INTLV[2:0]	RTODIS	P24T	RAMDRV1, RAMDRV0	PGMD
Interleave Select: 000 = No Interleave 001 = Banks 0, 1 010 = Banks 0, 3 011 = Banks 1, 2 100 = Banks 2, 3 101 = Banks 0, 1 & 2, 3 110 = Banks 0, 3 & 1, 2 111 = Not Used	RAS# Time-Out Disable: 0=Enable 1=Disable	Enable P24T Mode (read only): 0 = Disable 1 = Enable	MA[10:0], RAMW#/EALE#, RAS#, MA0X, MA0Y Drive Current: 00 = 12 mA (All) 01 = 24 mA (MA, RAMW#/EALE#), 12 mA (RAS#, MA0X, MA0Y) 10 = 24 mA (All except RAS#), 12 mA (RAS#) 11 = 24 mA (All)	Page Mode: 0 = Enable 1 = Burst Only

Non-Turbo and Refresh Control Register - NTBREF (R/W) — 05h

7	6	5	4	3	2	1	0
0	0	0	TURBO	0	0	0	0

NTB[2:0]	TURBO	REFMD[1:0]	CASREF	REFSPD
Interleave Select: 000 = Full Speed 001 = Full Speed +2 ... ... 111 = Full Speed +8	State of TURBO Signal (Read-Only)	Refresh Mode: 00 = Synchronous 01 = Asynchronous 1X = Decoupled	CAS-before-RAS Refresh: 0 = Disable 1 = Enable	Refresh Period: 0 = 15.625 µs 1 = 125 µs

INDEXED CONFIGURATION REGISTER FORMATS (Cont.)

Clock Control Register - CLKCTL (R/W) **06h**

7	6	5	4	3	2	1	0
0	0	0	1	1	(Note)	1	1

FBEN	CLK2DIV[1:0]	FCLKDIV[1:0]	BOSCSNS	SCLKDIV[1:0]
Enable SYSCLK Freq. Change in Fast Bus Clock Region: 0 = Disable 1 = Enable	CLK Divider in Non-Turbo Mode: 00->CLK = TCLK2 +2 01->CLK = TCLK2 +4 10->CLK = TCLK2 +6 11->CLK = TCLK2 +8	Fast Clock Divider BUSOSC/TCLK2: 00->+2/2 01->+4/4 10->+6/6 11->+8/8	BUSCLK Pin Status: 0 = Slow Clock 1 = Fast Clock	Slow Clock Divider BUSOSC/TCLK2: 00->+2/4 01->+4/6 10->+6/8 11->+8/12

Note: Reset value is 0 if an oscillator is connected to the BUSOSC pin, else the state of the BUSOSC pin is reflected.

Miscellaneous Control Register - MISCSET (R/W) **07h**

7	6	5	4	3	2	1	0
0	TAG[8]	0	0	0	0	0	0

SEGCEN	TAG8	CWETIME	FASTRC	CEN	ENPAR#	CWS_OFF	CACHCKCTL
Segment Cacheability Enable for Secondary Cache: 0 = Disable 1 = Enable	Reflects Value of TAG8 Pin	CWE Turn-Off Time: 0 = Late 1 = Early	Fast Internal RC#: 0=Disable 1=Enable	Primary Cache Enable: 0=Disable 1=Enable	Enable Parity Gen/Check: 0 = Enable 1 = Disable	Conditional Wait States: 0 = Enable 1 = Disable	Cache Control Clock Adjustment: 0 = Enable 1 = Disable

DMA Control Register - DMACTL (R/W) **08h**

7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0

ENABLEFF	FFPTR	DMAWS8[1:0]	DMAWS16[1:0]	DMACLK	MEMTM
Enable Extended DMA Address: 0 = Disable 1 = Enable	Enable Access to Upper Page Registers: 0 = Lower 1 = Upper	8-Bit DMA Wait States: 00 = 2 WS 01 = 4 WS 10 = 3 WS 11 = 3 WS	16-Bit DMA Wait States: 00 = 2 WS 01 = 4 WS 10 = 3 WS 11 = 3 WS	DMA Clock: 0=SYSCLK+2 1=SYSCLK	DMA MEMR# Signal Delay: 0 = PC/AT Comp. 1 = 1 DMA CLK Early

INDEXED CONFIGURATION REGISTER FORMATS (Cont.)

Bus Control Register - BUSCTL (R/W) 09h

7	6	5	4	3	2	1	0
0	0	IRQSH/LD#	0	0	0	0	0

VSF#	10/16IO	SLTDRV	DSKTMG	CMDLY2	CMDLY1	16WS	8WS
VLSI Special Feature (Enable I/O Space EEh-FFh): 0 = Enable 1 = Disable	10/16-Bit I/O Address Decode: 0 = 16-Bit Decode 1 = 10-Bit Decode	Slot Drive Current: 0 = 12 mA 1 = 24 mA	Disk I/O Timing: 0 = Slow 1 = Fast	Command Delay for 8- & 16-Bit I/O & 8-Bit Memory Cycles: 0 = 0 SYSCLK 1 = 1 SYSCLK	Command Delay for 16-Bit Memory Cycles: 0 = 0 SYSCLK 1 = 1 SYSCLK	16-Bit Wait States: 0 = 0 WS 1 = 1 WS	8-Bit Wait States: 0 = 4 WS 1 = 5 WS

Fast Bus Clock Region Register - FBCR (R/W) 0Bh

7	6	5	4	3	2	1	0
A23	A22	A21	A20	A19	A18	A17	A16

Address Bits 23-16 of Memory Region Selected for Fast Bus Clock Access

ROM Control Register - ROMSET (R/W) 0Ch

7	6	5	4	3	2	1	0
!CA3BA2	RAMW#	0	0	0	0	0	0

ROMWID	ROMMOV[2:0]	MBIOS	FMPRGM	ROMWS[1:0]
BIOS ROM Width (Read-Only): 0 = 8-Bit 1 = 16-Bit	System and Slot ROM Location Code	Mid BIOS Enable: 0 = Enable 1 = Disable	Flash Memory Program: 0 = Enable 1 = Disable	ROM Wait States 00 = 3 WS 01 = 1 WS 10 = 2 WS 11 = 3 WS

INDEXED CONFIGURATION REGISTER FORMATS (Cont.)

A0000h-FFFFFh Segment Access Control Registers - AAXS, BAXS, DAXS, EAXS, FAXS (R/W) **0Dh-12h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

AC000 Access	A8000 Access	A4000 Access	A0000 Access
BC000 Access	B8000 Access	B4000 Access	B0000 Access
CC000 Access	C8000 Access	C4000 Access	C0000 Access
DC000 Access	D8000 Access	D4000 Access	D0000 Access
EC000 Access	E8000 Access	E4000 Access	E0000 Access
FC000 Access	F8000 Access	F4000 Access	F0000 Access

00 = Read/Write Slot Bus
01 = Read Slot, Write System Board
10 = Read System Board, Write Slot Bus
11 = Read/Write System Board

A0000h-FFFFFh Segment Cacheability Control Registers - ACBL, BCBL, DCBL, ECBL, FCBL (R/W) **13h-18h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

AC000 Access	A8000 Access	A4000 Access	A0000 Access
BC000 Access	B8000 Access	B4000 Access	B0000 Access
CC000 Access	C8000 Access	C4000 Access	C0000 Access
DC000 Access	D8000 Access	D4000 Access	D0000 Access
EC000 Access	E8000 Access	E4000 Access	E0000 Access
FC000 Access	F8000 Access	F4000 Access	F0000 Access

00 = Not Write Protected, Cacheable
10 = Write Protected, Cacheable
X1 = Not Cacheable

Cache Controller Setup Register - CACHCTL (R/W) **19h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

DBLBNK	ZWSW	TSIZE9	VEN	DTYBIT	CSIZE[2:0]
Cache Banks (Data SRAMs): 0 = 1 Bank 1 = 2 Banks	Zero or One Wait State Writes: 0 = 1 WS Writes 1 = 0 WS Writes	Tag Size: 0 = 8-Bit 1 = 9-Bit	Valid Bit Enable: 0 = Disable 1 = Enable	Dirty Bit: 0 = Enable 1 = Disable	Cache Size: 000 = Cache Disable 001 = 32 KB 010 = 64 KB 011 = 128 KB 100 = 256 KB 101 = 512 KB 110 = 1 MB 111 = Direct Access

INDEXED CONFIGURATION REGISTER FORMATS (Cont.)

Programmed Memory Region Address Register 1 - PMRA1 (R/W) 20h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0

Select Bus:
0 = ISA Bus
1 = Local Bus

Cacheability:
0 = Cache
1 = Non-cache

Start Address and Memory Region Size:

0	A23	A22	A21	A20	A19	Start Address of a 512 KB Region in Lower 16 MB of Memory
1	0	A26	A25	A24	A23	Start Address of an 8 MB Region in Lower 128 MB of Memory
1	1	A17	A16	A15	A14	Start Address of a 16 MB Region in the Range C0000h-FFFFFh

Programmed Memory Region Enable Register 1 - PMRE1 (R/W) 21h

7	6	5	4	3	2	1	0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

Sub-Region Enables for Remapping and/or Primary Cacheability:
0 = Default Mapping Cacheability 1 = Mapping and Cacheability Defined by PMRA

Programmed Memory Region Address Register 2 - PMRA2 (R/W) 22h

7	6	5	4	3	2	1	0
LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0

Programmed Memory Region Enable Register 2 - PMRE2 (R/W) 23h

7	6	5	4	3	2	1	0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

Extension Control Register - XCTL (R/W) 24h

7	6	5	4	3	2	1	0
0	!MA0X	0	0	0	0	0	0

KBLK	HSPD	EADSTS	EADSGEN	CRWS	GENPAR	LDVDLY	ISALDV
Keyboard Command Blocking: 0 = Disable 1 = Enable	Operating Speed: 0 = Normal 1 = High	EADS# Three-state Control: 0 = Normally Enabled 1 = Normally Three-stated	Generate EADS# for VL-Bus Masters: 0 = Disable 1 = Enable	Add Cache Read Wait State: 0 = Disable 1 = Enable	Generate DRAM Parity for CPU: 0 = Disable 1 = Enable	LDEV# Sample Point: 0 = 1st T2 1 = 2nd T2	Monitor LDEV# for DMA/Master Cycles: 0 = Disable 1 = Enable

TABLE 3. INDEXED CONFIGURATION REGISTERS MAP

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
The following I/O mapped registers are used to access the Indexed Configuration Registers:									
ECh (R/W)	Index Port	A7	A6	A5	A4	A3	A2	A1	A0
EDh (R/W)	Data Port	D7	D6	D5	D4	D3	D2	D1	D0
The following registers are accessed by writing their address into the Index Port and reading/writing their data via the Data Port.									
00h (R-O)	VER	Product Code						Device Version	
01h (R/W)	RAMTMG	TSTRT[1:0]		TRP[1:0]		TRCD[1:0]		TCAS[1:0]	
02h (R/W)	RAMCFG0	1	DRAM Bank 1 Type		S/D 1	1	DRAM Bank 0 Type		S/D 0
03h (R/W)	RAMCFG1	1	DRAM Bank 3 Type		S/D 3	1	DRAM Bank 2 Type		S/D 2
04h (R/W)	RAMSET	INTLV[2:0]			RTODIS	P24T	RAMDRV[1:0]		PGMD
05h (R/W)	NTBREF	NTB[2:0]			TURBO	REFMOD[1:0]		CASREF	REFSPD
06h (R/W)	CLKCTL	FBEN	CLKDIV[1:0]		FCLKDIV[1:0]		BOSCSNS	SCLKDIV[1:0]	
07h (R/W)	MISCSET	SEGCEN	TAG[8]	CWETIME	FASTRC	CEN	ENPAR#	CWS_OFF	CACHCKCTL
08h (R/W)	DMACTL	ENBLFF	FFPTR	DMAWS8[1:0]		DMAWS16[1:0]		DMACLK	MEMTM
09h (R/W)	BUSCTL	VSF#	10/16IO	SLTDRV	DSKTMG	CMDLY2	CMDLY1	16WS	8WS
0Bh (R/W)	FBCR	A23	A22	A21	A20	A19	A18	A17	A16
0Ch (R/W)	ROMSET	ROMWID	ROMMOV[2:0]			MBIOS	FMPRGM	ROMWS[1:0]	
0Dh (R/W)	AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
0Eh (R/W)	BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
0Fh (R/W)	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10h (R/W)	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11h (R/W)	EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
12h (R/W)	FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
13h (R/W)	ACBL	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
14h (R/W)	BCBL	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
15h (R/W)	CCBL	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
16h (R/W)	DCBL	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
17h (R/W)	ECBL	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
18h (R/W)	FCBL	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
19h (R/W)	CACHCTL	DBLBNK	ZWSW	TSIZE9	VEN	DTYBIT	CSIZE[2:0]		
20h (R/W)	PMRA1	LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0
21h (R/W)	PMRE1	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
22h (R/W)	PMRA2	LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0
23h (R/W)	PMRE2	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
24h (R/W)	XCTL	KBLK	HSPD	EADST	EADSGEN	CRWS	GENPAR	LDVDLY	ISALDV

TABLE 4. DEDICATED I/O CONTROL REGISTERS

Port Address	Name	Access	Functional Description
61h	Port B	R/W	Miscellaneous control bits
70h	NMI Enable	W	Enables non-maskable interrupts.
92h	Port A	R/W	Fast A20 and reset control.
ECh	Configuration Index Port	R/W	Contains the address of one of the Configuration Registers mentioned in Table 2.
EDh	Configuration Data Port		Contains the data written to the Configuration Register selected by the Configuration Index Port.
EEh*+	Fast A20 Register	R/W	A dummy read enables Fast A20. A dummy write disables Fast A20.
EFh*+	Fast CPU Reset Register	R	A dummy read resets the CPU.
F0h	Coprocessor Busy Register	W	A dummy write clears IRQ[13] and sets BSCPU#.
F1h	Coprocessor Reset Register	W	A dummy write clears IRQ[13] and sets BSCPU#.
F4h+	Slow CPU Register	W	A dummy write enables the Fast Clock and Turbo Mode for the CPU.
F5h+	Fast CPU Register	W	A dummy write enables the Fast Clock and Turbo Mode for the CPU.
F9h+	Configuration Enable Register	W	A dummy write disables access to the Configuration Registers.
FBh+	Configuration Enable Register	W	A dummy write disables access to the Configuration Registers.

* Also can be activated through Port 92h for PS/2 compatibility.
\+ These decodes can be disabled by setting the MSB of the BUSCTL Register in case of conflict.

AC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
CLOCK TIMINGS						
f_TC2	TCLK2 Frequency		80	MHz		2x processor clock
tP_TC2	TCLK2 Period	12.5		ns	1	
tH_TC2	TCLK2 High Time	5		ns	1	VIH = 2.0 V
tL_TC2	TCLK2 Low Time	5		ns	1	VIL = 0.8 V
tD_CLK1	TCLK2 to CLK1 Delay	3	35	ns		CL = 50 pF
tH_CLK1	CLK1 High Time	10		ns	1	@TCLK2 = 80 MHz, VOH = 2 V
tL_CLK1	CLK1 Low Time	10		ns	1	@TCLK2 = 80 MHz, VOL = 0.8 V
tR_CLK1	CLK1 Rise Time		3	ns	1	0.8 V to 3.6 V, CL = 50 pF
tFA_CLK1	CLK1 Fall Time		3	ns	1	3.6 V to 0.8 V, CL = 50 pF
f_CKIN	CLKIN Frequency		40	MHz		Processor clock
tP_CKIN	CLKIN Period	25		ns	1	
tH_CKIN	CLKIN High Time	10		ns	1	VIH = 2.0 V
tL_CKIN	CLKIN Low Time	10		ns	1	VIL = 0.8 V
f_IQCK	IRQCLK Frequency		80	MHz		2x processor clock frequency
tP_IQCK	IRQCLK Period	12.5		ns	1	
tH_IQCK	IRQCLK High Time	5		ns	1	VIL = 0.8 V, VIH = 2.0 V
tL_IQCK	IRQCLK Low Time	5		ns	1	VIL = 0.8 V, VIH = 2.0 V
tP_BOSC	BUSOSC Period	20		ns	1	
tH_BOSC	BUSOSC High Time	9		ns	1	VIL = 0.8 V, VIH = 2.0 V
tL_BOSC	BUSOSC Low Time	9		ns	1	VIL = 0.8 V, VIH = 2.0 V
tFA_SCK	SYSCLK Fall Time		10	ns	1	VOL = 0.8 V, VOH = 2.0 V, CL = 200 pF
tR_SCK	SYSCLK Rise Time		10	ns	1	VOL = 0.8 V, VOH = 2.0 V, CL = 200 pF
tD1_SCK	TCLK2 to SYSCLK Delay	5	48	ns		CL = 200 pF
tD2_SCK	BUSOSC to SYSCLK Delay	5	50	ns		CL = 200 pF
tP_OSC	OSC Period	69.8		ns	1	14.31818 MHz clock
tH_OSC	OSC High Time	20		ns	1	VIL = 0.8 V, VIH = 2.0 V
tL_OSC	OSC Low Time	20		ns	1	VIL = 0.8 V, VIH = 2.0 V
CPU INTERFACE SYNCHRONOUS TIMINGS						
tS1_CPU	ADS#, M/IO#, W/R#, D/C# to CLKIN Setup Time	19		ns	2	To +ve Edge of CLKIN, TSTRT[1:0] = 00
tS2_CPU	ADS#, M/IO#, W/R#, D/C# to CLKIN Setup Time	10		ns	2	To +ve Edge of CLKIN, TSTRT[1:0] = '01 or '10
tS3_CPU	A[31, 26:2], BE[3:0]#, to CLKIN Setup Time	19		ns	2	To +ve Edge of CLKIN, end of T1, if TSTRT[1:0] = '00 To -ve Edge of CLKIN, middle of first T2, if TSTRT[1:0] = '01 To +ve Edge of CLKIN, end of first T2, if TSTRT[1:0] = '10

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tS4_CPU	HLDA to CLKIN Setup Time	7		ns	2	
tS5_CPU	BLAST# to CLKIN Setup Time	8		ns	2	
tS6_CPU	D[31:0], PAR[3:0] to CLKIN Setup Time	5		ns	2	For parity check and local bus DMA/Master Mode cycles
tS7_CPU	RDY#, BRDY# to CLKIN Setup Time	5		ns	2	Local bus time-out or local bus DMA/Master Mode cycles
tS8_CPU	LDEV# to CLKIN Setup Time	10		ns	2	To +ve Edge of CLKIN, end of T1, if TSTRT[1:0] = '00 and on-board DRAM region To -ve Edge of CLKIN, middle of first T2, if TSTRT[1:0] = '01 and on-board DRAM region To +ve Edge of CLKIN, end of first T2, if TSTRT[1:0] = '10 or not on-board DRAM region
tS9_CPU	HITM# to CLKIN Setup Time	10		ns	2	
tH1_CPU	ADS#, M/IO#, W/R#, D/C#, A[31, 26:2], BE[3:0]#, HLDA, BLAST#, RDY#, BRDY#, D[31:0], PAR[3:0], LDEV# from CLKIN Hold Time	3		ns	2	
tD1_CPU	CLKIN to A[31, 26:2], BE[3:0]#, M/IO#, W/R#, D/C#, ADS#, BLAST# Delay	4	14	ns	3	CL = 50 pF. HLDA Cycles, T1 of local bus cycles
tD3_CPU	A[31, 26:2] to KEN#, EADS# Delay		30	ns	3	CL = 50 pF. State change occurs only in T2 cycles
tD4_CPU	CLKIN to RDY#, BRDY#, EADS#, KEN# Delay	4	19	ns	3	CL = 50 pF
tD5_CPU	LDEV# to KEN# Delay		10	ns	3	CL = 50 pF. State change occurs only in T2 cycles
tD1_HOLD	CLKIN to HOLD Delay	4	18	ns	3	CL = 50 pF
tD1_RCPU	CLKIN to RESCPU Delay	4	19	ns	3	CL = 50 pF
tD1_NMI	CLKIN to NMI Delay (Parity Error)	4	19	ns	3	CL = 50 pF
tF1_CPU(1)	CLKIN to A[31, 26:2], BE[3:0]#, ADS#, M/IO#, W/R#, D/C#, BLAST# Float Delay	4	18	ns	4	CL = 50 pF. HLDA inactive cycles
tA1_CPU	CLKIN to D[31:0] Active Delay	4	19	ns	4	CL = 50 pF. Slot bus reads, second T2 or local bus ROM reads, last T2
tF2_CPU(1)	CLKIN to D[31:0] Float Delay	4	18	ns	4	CL = 50 pF. After slot bus or local ROM read
tF3_CPU(1)	CLKIN to RDY#, BRDY# Float Delay	4	18	ns	4	CL = 50 pF. Two clocks after driven active
DRAM CONTROLLER INTERFACE TIMING (CPU CYCLES)						
tD1_MA	A[31, 26:2], to MA0X, MA0Y, MA[10:1] Delay	4	40	ns	3	CL (MA[10:1]) = 680 pF, CL (MA0X, MA0Y) = 340 pF, Conditional WS disabled

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tD2_MA	A[31, 26:2], A31 to MA0X, MA0Y, MA[10:1] Delay	4	22	ns	3	CL (MA[10:1]) = 600 pF, CL (MA0X, MA0Y) = 300 pF, Conditional WS enabled
tD3_MA	CLKIN to MA0X, MA0Y, MA[10:1] Delay	4	28	ns	3	CL (MA[10:1]) = 680 pF, CL (MA0X, MA0Y) = 340 pF
tD1_RAS	CLKIN to RAS# Delay	4	16	ns	3	CL = 150 pF
tD1_CAS	CLKIN to CAS# Delay	4	14	ns	3	CL = 150 pF. Read cycles, TCAS[1:0] = 1T, 1.5T, or 2T-4121 cycles
tD1_MDEN	CLKIN to MDEN# Delay	4	11	ns	3	CL = 50 pF. Read cycles, TCAS[1:0] = 1T, 1.5T, or 2T-4121 cycles
tD2_MDEN	CLKIN to MDEN# Delay	4	16	ns	3	CL = 50 pF. Write cycles, or TCAS[1:0] = 2T, non-4121 cycles
tD1_RAMW	W/R# to RAMW#/EALE# Delay	4	20	ns	3	CL = 680 pF. Function of pin is RAMW#, T1 of write cycles
tD1_BECS	BE[3:0]# to CAS# Delay	4	20	ns	3	CL = 150 pF
tD1_PAR	D[31:0] to PAR[3:0] delay	4	11	ns	10-3	CL = 100 pF. GENPAR = '1
DRAM CONTROLLER INTERFACE TIMING (HLDA/REFRESH CYCLES)						
tD4_MA	A[31, 26:2] to MA0X, MA0Y, MA[10:1] Delay	4	15	ns	3	CL (MA[10:1]) = 680 pF, CL (MA0X, MA0Y) = 340 pF, DMA/Master Mode cycles
tD3_CAS(1)	CMD# to CAS# Delay	4	25	ns	3	CL = 150 pF. DMA/Master Mode cycles
tD2_RAMW(1)	MEMW# to RAMW#/EALE# Delay	4	30	ns	3	CL = 680 pF. Function of pin is RAMW#
tD2_RAS(1)	HLDA High to RAS# High Delay	4	25	ns	3	CL = 150 pF. Start of HLDA cycles
tD3_RAS(1)	MEMW#/MEMR# to RAS# Delay	4	25	ns	3	CL = 150 pF. DMA/Master Mode cycles
tD4_CAS(1)	OSC to CAS# Low Delay	4	25	ns	3	CL = 150 pF, DMA/Master Mode cycles, CAS-before-RAS refresh
tD5_CAS(1)	MEMW#/MEMR# to CAS# High Delay	4	25	ns	3	CL = 150 pF. DMA/Master Mode cycles
tD5_MA(1)	OSC to MA0X, MA0Y, MA[10:1] Delay	4	35	ns	3	CL (MA[10:1]) = 680 pF, CL (MA0X, MA0Y) = 340 pF, Row -> column address switch
tA1_PAR(1)	MEMW# Low to PAR[3:0] Active Delay	4	25	ns	4	CL = 50 pF
tF1_PAR(1)	MEMW# High to PAR[3:0] Float Delay	4	25	ns	4	CL = 50 pF
tD1_PAR(1)	SD[15:0] to PAR[3:0] Delay	4	48	ns	3	CL = 50 pF
tD4_RAS(1)	OSC to RAS# Delay	4	25	ns	3	CL = 150 pF +ve edge OSC for RAS[0,2]# Refresh –ve edge OSC for RAS[1,3]# Refresh
CACHE CONTROLLER INTERFACE TIMING (CPU CYCLES)						
tS1_TAG	TAG[8:0] to CLKIN –ve Edge Setup Time	6		ns	2	1 WS write-hits when bits ZWSW = '0 and CACHCKCTL = '1. Middle T2 sample time

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tS2_TAG	TAG[8:0] to CLKIN +ve Edge Setup Time	20		ns	2	End T2 Setup to Control DRAM accesses
tD1_TAG	TAG[8:0] to RDY#, BRDY Delay	4	15	ns	3	CL = 50 pF. 0 WS read/write-hits
tD2_TAG	TAGWE# Falling to TAG[8:0] Out Delay	4	15	ns	3	CL = 50 pF. 1 WS write-hits
tD1_COE	CLKIN to COEA#, COEB# Delay	4	11	ns	3	CL = 100 pF. Read-hits
tD1_CCS	CLKIN to CCSA#, CCSB# Delay	4	20	ns	3	CL = 100 pF. Write-hits and read-miss updates
tD_CA	CLKIN to CA3A, CA3BA2 Delay	4	13	ns	3	CL = 100 pF. All cache accesses
tD1_CWE(1)	CLKIN –ve Edge to CWE[3:0]# Delay	8	12	ns	3	CL = 50 pF. 1 WS write-hits or read-miss updates, CACHCKCTL = '0
tD1_TWE(1)	CLKIN –ve Edge to TAGWE# Delay	8	12	ns	3	CL = 50 pF. 1 WS write-hits or read-miss updates, CACHCKCTL = '0
tS3_TAG(2)	TAG[8:0] to CLK1 –ve Edge Setup Time	8.5		ns	2	0 WS write-hits, middle T2 sample time. ZWSW = '1
tD2_CWE(2)	CLK1 –ve edge to CWE[3:0]# –ve Edge Delay	4	10	ns	3	CL = 50 pF. 0 WS write-hits
tD3_CWE(2)	CLK1 +ve edge to CWE[3:0]# +ve Edge Delay	4	9	ns	3	CL = 50 pF. 0 WS write-hits, CWETIME = '1
tD4_CWE(2)	CLKIN +ve edge to CWE[3:0]# +ve Edge Delay	4	15	ns	3	CL = 50 pF. 0 WS write-hits CWETIME = '0
CACHE CONTROLLER INTERFACE TIMING (HLDA CYCLES)						
tD5_CWE	MEMW# to CWE[3:0]# Delay	4	25	ns	3	CL = 50 pF. DMA/Master Mode write-hits
tD2_COE	MEMR# to COEA#, COEB# Delay	4	25	ns	3	CL = 100 pF. DMA/Master Mode read-hits
tD2_CCS	A[2] to CCSA#, CCSB# Delay	4	25	ns	3	CL = 100 pF. DMA/Master Mode cycles
ISA BUS TIMINGS (CPU CYCLES)						
tD1_RMCS(1)	CLKIN to ROMCS#/PCS# Delay	4	20	ns	3	CL = 50 pF. End first T2 ROM access
tD1_EALE(1)	SYSCLK to RAMW#/EALE# Delay	–6	16	ns	5	CL = 50 pF. Function of pin is EALE#
tD1_BALE(1)	SYSCLK to BALE Delay	–6	10	ns	5	CL = 200 pF
tD1_CMD(1)	SYSCLK to CMD#(3) Delay	–6	17	ns	5	CL = 200 pF
tD1_SCMD(1)	SYSCLK to SCMD#(4) Delay	–6	17	ns	5	CL = 200 pF. Addresses below 1 MB
tF1_SCMD(1)	SYSCLK to SCMD#(4) Float Delay	–5	25	ns	6	CL = 200 pF. Addresses below 1 MB
tD1_PCS(1)	SYSCLK to ROMCS#/PCS# Delay	4	40	ns	5	CL = 50 pF. Function of pin is PCS#
tD1_SA(1)	SYSCLK to SA[1:0] Delay (Conversion Cycle)	–5	16	ns	5	CL = 200 pF
tD1_SD(1)	SYSCLK to SD[15:0] Delay	–1	35	ns	6	CL = 200 pF. Slot write cycles
tF1_SD(1)	SYSCLK to SD[15:0] Float Delay	–2	30	ns	5	CL = 200 pF. Slot write cycles
tD1_SPKR(1)	IOW# inactive to NMI, SPKR Delay	4	50	ns	7	CL = 50 pF. After write strobe to Port 61h (SPKR/NMI)
tD1_A20M(1)	IOW#, IOR# Low to A20M# Low Delay	4	50	ns	7	CL = 50 pF. For write to Port 64h or read from EEh

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tD1_IGNE	IOW# Low to IGNNE# Low Delay	4	50	ns	7	CL = 50 pF. For write to Port F0h or F1h
tS1_CS16(1)	MEMCS16#, IOCS16# to SYSCLK Setup Time	35		ns	5	
tH1_CS16(1)	MEMCS16#, IOCS16# from SYSCLK Hold Time	–2		ns	5	
tS1_WS0(1)	WS0# to SYSCLK Setup Time	33		ns	5	
tH1_WS0(1)	WS0# from SYSCLK Hold	–2		ns	5	
tS1_CHR(1)	IOCHRDY to SYSCLK Setup	30		ns	5	
tH1_CHR(1)	IOCHRDY from SYSCLK Hold Time	–2		ns	5	
tS1_SD(1)	SD[15:0] to SYSCLK Setup Time	35		ns	5	To latch data during off-board read cycles
tH1_SD(1)	SD[15:0] from SYSCLK Hold Time	6		ns	5	To latch data during off-board read cycles
tS2_D(1)	D[31:0] to SYSCLK Setup Time	35		ns	5	To latch data during off-board read cycles
tH2_D(1)	D[31:0] from SYSCLK Hold Time	6		ns	5	To latch data during off-board read cycles
tD1_D(1)	D[31:0] to SD[15:0] Delay	4	30	ns	3	CL = 50 pF. Slot bus -> on-board writes
tD2_SD(1)	D[31:0] to SD[15:0] Delay	4	25	ns	3	CL = 200 pF. Slot bus <- on-board reads
tS1_IOX(1)	IOCS16# to IOR#, IOW# Setup Time	15		ns	7	To meet data steering requirements
tH1_IOX(1)	IOCS16# from IOR#, IOW# Hold Time	5		ns	7	To meet data steering requirements
tS1_MEMX(1)	MEMCS16# to MEMR#, MEMW# Setup Time	15		ns	7	To meet data steering requirements
tH1_MEMX(1)	MEMCS16# from MEMR#, MEMW# Hold Time	5		ns	7	To meet data steering requirements
tS3_D(1)	D[31:0] from SYSCLK Setup Time	75		ns	5	Internal register access - CPU writes
tH3_D(1)	D[31:0] from SYSCLK Hold Time	30		ns	5	Internal register access - CPU writes
ISA BUS INTERFACE TIMINGS (MASTER MODE)						
tD1_BE(1)	SA[1:0] to BE[3:0]# Delay	3	25	ns	8	CL = 50 pF. Used to generate MBE[3:0]
tD2_PCS(1)	A[23:2], SA[1:0] to ROMCS#/PCS# Delay	3	40	ns	8	CL = 50 pF. Function of pin is PCS#
tD2_SCMD(1)	MEMW#, MEMR# to SCMD#(4) Delay	3	30	ns	7	CL = 200 pF
tA1_SCMD(1)	A[23:2]0 to SCMD#(4) Active Delay	3	25	ns	8	CL = 200 pF
tF2_SCMD(1)	A[23:2]0 to SCMD#(4) Float Delay	3	25	ns	8	CL = 200 pF
tS1_A(1)	A[23:2], SA[1:0] to CMD#(5) Setup Time	30		ns	7	
tH1_A(1)	A[23:2], SA[1:0] from CMD#(5) Hold Time	20		ns	7	

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tS2_SD[1]	SD[15:0] to IOW# Setup Time	55		ns	7	Internal register access
tH2_SD[1]	SD[15:0] from IOW# Hold Time	20		ns	7	Internal register access
tD3_SD[1]	IOR# Low to SD[15:0] Delay	5	120	ns	7	CL = 200 pF. Internal register access
tF2_SD[1]	IOR# High to SD[15:0] Float Delay	4	30	ns	7	CL = 200 pF. Internal register access
tA2_SD[1]	CMD#[5] Low to SD[15:0] Active Delay	4	35	ns	7	CL = 200 pF. On-board memory read
tF3_SD[1]	CMD#[5] High to SD[15:0] Float Delay	4	35	ns	7	CL = 200 pF. On-board memory read
tA3_SD[1]	CMD#[5] Low to SD[7:0] Active Delay	4	50	ns	7	CL = 200 pF. Odd byte write to 8-bit add-on card
tF4_SD[1]	CMD#[5] High to SD[7:0] Float Delay	4	35	ns	7	CL = 200 pF. Odd byte write to 8-bit add-on card
ISA BUS INTERFACE TIMINGS (REFRESH MODE)						
tD1_RFSH	CLKIN to REFRESH# Low Delay	–8	35	ns	5	CL = 200 pF. Waiting for arbiter switch
tF1_RFSH[1]	SYSCLK to REFRESH# Float Delay	–7	18	ns	6	CL = 200 pF
tD2_SA[1]	SYSCLK to SA[1:0] Delay	–4	40	ns	5	CL = 200 pF
tD1_A[1]	SYSCLK to A[16:2] Delay	–4	40	ns	5	CL = 50 pF
tD1_MEMR[1]	SYSCLK to MEMR#, SMEMR# Delay	–5	30	ns	5	CL = 200 pF
tS1_RFSH[1]	REFRESH# to CLKIN Setup Time	30		ns	5	External bus master refresh
tH1_RFSH[1]	REFRESH# from CLKIN Hold Time	5		ns	5	External bus master refresh
tA1_SMR[1]	REFRESH# to SMEMR# Active Delay	4	40	ns	7	CL = 200 pF. External bus master refresh
tS2_CHR[1]	IOCHRDY to SYSCLK Setup Time	25		ns	5	
tH2_CHR[1]	IOCHRDY from SYSCLK Hold Time	0		ns	5	
tD6_MA	CLKIN to MA0Y, MA0X, MA[10:1] Delay	4	40	ns	3	CL = (MA[10:1]) = 680 pF, CL = (MA0X, MA0Y) = 340 pF, Generate refresh address
tS1_DRQ[1]	DRQ to SYSCLK Setup Time	20		ns	5	
tD1_DK[1]	SYSCLK to DK[2:0] Delay	–2	70	ns	5	CL = 50 pF
tD2_DK[1]	CLKIN to DK[2:0] Invalid Delay	4	16	ns		CL = 50 pF. Local bus DMA cycles
tF1_DK[1]	SYSCLK to DK[2:0] Float Delay	–2	70	ns	6	CL = 50 pF. End of DMA transfer cycle
tD1_DKEN[1]	SYSCLK to DKEN Delay	–2	70	ns	5	CL = 50 pF
tD2_CMD[1]	SYSCLK to CMD#[3] Delay	–5	60	ns	5	CL = 200 pF
tD2_A[1]	SYSCLK to A[26:2], BE[3:0]# Delay	0	90	ns	5	CL = 50 pF
tA1_A[1]	SYSCLK to A[26:2], BE[3:0]# Active Delay	0	90	ns	6	CL = 50 pF

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tF1_A[1]	SYSCLK to A[26:2], BE[3:0]# Float Delay	0	90	ns	6	CL = 50 pF
tD3_SA[1]	SYSCLK to SA[1:0] Delay	0	95	ns	5	CL = 200 pF
tD1_TC[1]	SYSCLK to T/C Delay	–5	60	ns	5	CL = 100 pF
tS3_CHR[1]	IOCHRDY to SYSCLK Setup Time	45		ns	5	
tH3_CHR[1]	IOCHRDY from SYSCLK Hold Time	15		ns	5	
tD2_SCMD[1]	SYSCLK to SCMD#[4] Delay	–5	60	ns	5	CL = 200 pF
tA2_SCMD[1]	SCMD#[4] Active from SYSCLK Delay	–5	60	ns	6	CL = 200 pF
tF2_SCMD[1]	SCMD#[4] Float from SYSCLK Delay	–5	60	ns	6	CL = 200 pF
BUS ARBITRATION TIMINGS						
tD1_AEN[1]	MASTER# to AEN Delay	3	35	ns	8	CL = 200 pF
tD2_AEN[1]	HLDA to AEN Delay	3	35	ns	8	CL = 200 pF
tD2_BALE[1]	HLDA to BALE Delay	3	35	ns	8	CL = 200 pF
tA1_SAMR[1]	REFRESH# to SA[1:0], MEMR#, SMEMR# Active Delay	3	30	ns	7	CL = 200 pF. Start of external refresh cycle
tF1_SAMR[1]	REFRESH# to SA[1:0], MEMR#, SMEMR# Float Delay	3	30	ns	7	CL = 200 pF. End of external refresh cycle
tA2_A[1]	REFRESH# to A[31, 26:2], BE[3:0]# Active Delay	3	30	ns	7	CL = 50 pF
tF2_A[1]	REFRESH# to A[31, 26:2], BE[3:0]# Float Delay	3	30	ns	7	CL = 50 pF
tF1_SACD[1]	HLDA High to SA[1:0] CMD#[5] Float Delay	3	30	ns	8	CL = 200 pF
tA1_SACD[1]	HLDA High to SA[1:0] CMD#[5] Active	3	30	ns	8	CL = 200 pF
INTERRUPT TIMINGS						
tD1_INTR	FERR# to INTR Delay	5	150	ns	8	CL = 50 pF
tD3_INTR[1]	OSC to INTR Delay	5	130	ns	9	CL = 50 pF
tD1_ ISLD	IRQCLK to IRQSH/LD# Delay	3	10	ns	5	CL = 50 pF
tS1_ ISDI	IRQSDIN to IRQCLK Setup Time	5		ns	5	
tH1_ ISDI	IRQSDIN from IRQCLK Hold Time	3		ns	5	
MISCELLANEOUS TIMINGS						
tS1_PWG[1]	POWERGOOD to OSC Setup Time	15		ns	9	
tH1_PWG[1]	POWERGOOD from OSC Hold Time	10		ns	9	
tD1_RSD	CLKIN to RSTDRV Delay	–10	20	ns	5	CL = 200 pF
tD2_SPKR[1]	OSC to SPKR Delay	5	120	ns	9	CL = 50 pF

AC CHARACTERISTICS (Cont.)

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
tA1_DRAM(1)	CLKIN to MA[10:1], MA0X, MA0Y, RAS[3:0]#, CASX[3:0]#, CASY[3:0]# Active	4	50	ns	4	Following fourth ADS# after power-on reset

1 These timing specifications are guaranteed by design.

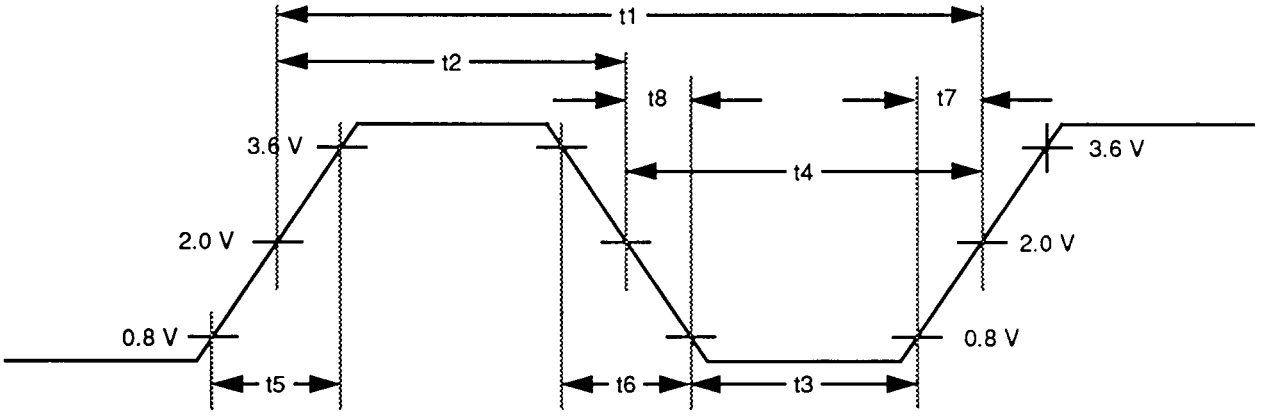
2 These timing specifications apply to zero wait state write systems only and are characterized, but not tested in production. To support zero wait state writes at 25/33 MHz, two minimum skew clock buffers on CLK1 as glue logic components are needed in the system.

3 CMD# refers to the signals MEMR#, MEMW#, IOR#, and IOW#

4 SCMD# refers to the signals SMEMR# and SMEMW#.

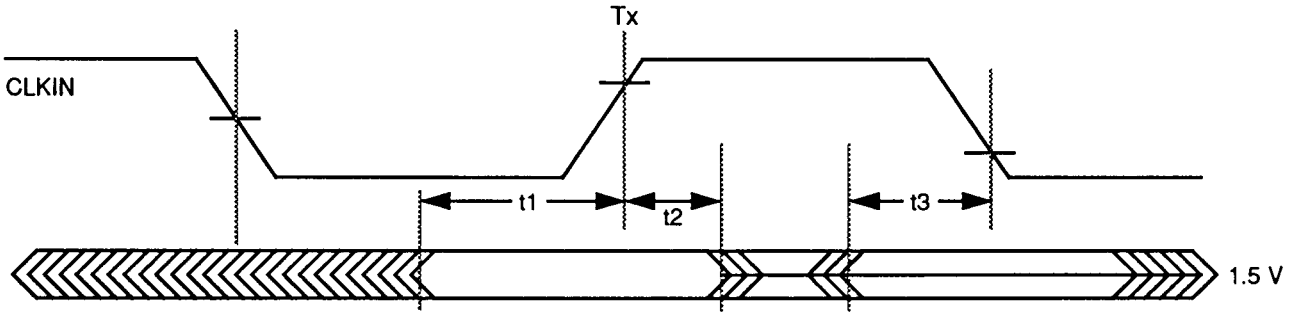
5 CMD# refers to the signals MEMR# and MEMW#.

FIGURE 1. CLOCK WAVEFORMS



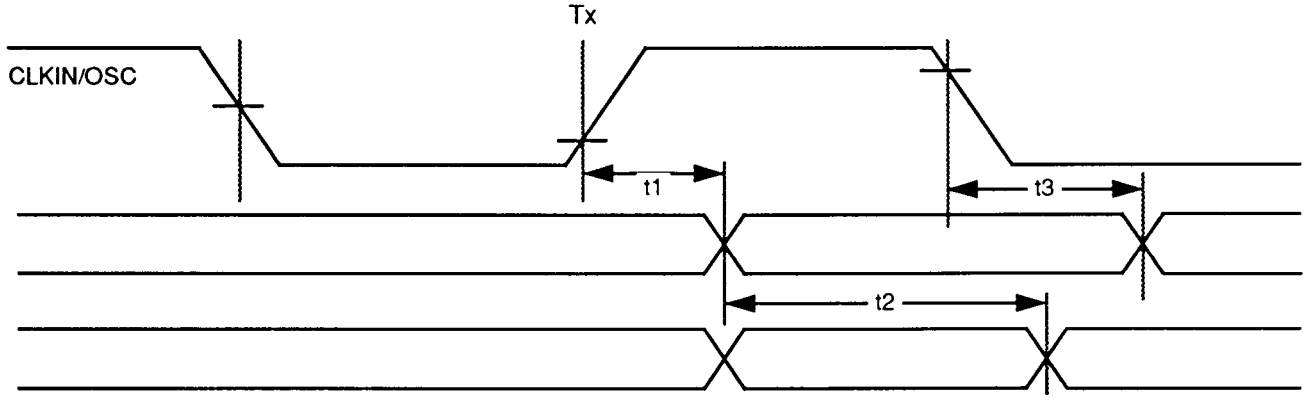
t1 = tP_TC2, tP_CKIN, tP_BOSC, tP_OSC, tP_IQCK
t2 = tH_TC2, tH_CLK1, tH_CKIN, tH_BOSC, tH_OSC, tH_IQCK
t3 = tL_TC2, tL_CKIN, tL_CLK1, tL_BOSC, tL_OSC
t5 = tR_CLK1
t6 = tFA_CLK1
t7 = tR_SCK
t8 = tFA_SCK

FIGURE 2. CPU INTERFACE, CACHE CONTROLLER AND DRAM CONTROLLER (1)



t1 = tS1_CPU, tS2_CPU, tS3_CPU, tS4_CPU, tS5_CPU, tS6_CPU, tS7_CPU, tS8_CPU,tS9_CPU, tS2_TAG
t2 = tH1_CPU
t3 = tS1_TAG, tS3_TAG

FIGURE 3. CPU INTERFACE CACHE CONTROLLER AND DRAM CONTROLLER (2)

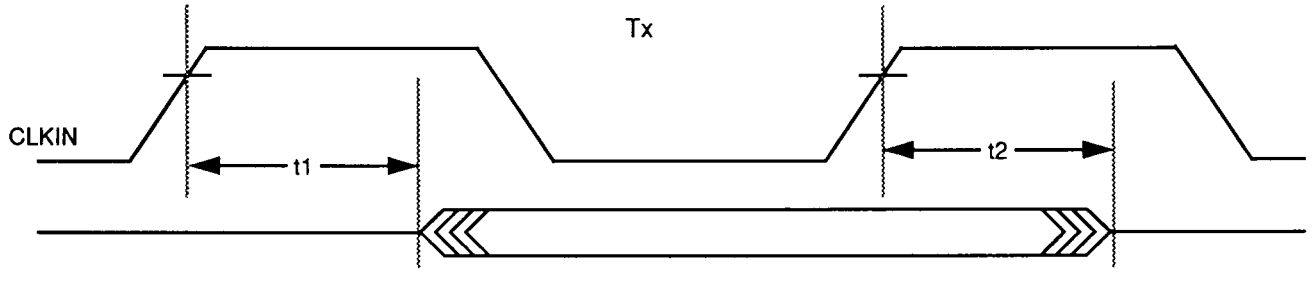


t1 = tD1_CPU, tD4_CPU, tD1_HOLD, tD1_RCPU, tD1_NMI, tD3_MA, tD1_RQAS, tD1_CAS, tD1_MDEN, tD2_MDEN, tD1_RMCS, tD1_BECS, tD5_MA, tD6_MA, tD4_RAS, tD4_CAS, tD1_RFSH, tD1_COE, tD1_CCS, tD2CA, tD1_CWE, tD1_CWE, tD3_CWE, tD4_CWE

t2 = tD3_CPU, tD1_MA, tD2_MA, tD4_MA, tD2_RAMW, tD2_RAS, tD3_RAS, tD3_CAS, tD1_PAR, tD1_D, tD2_SD, tD2_CAS, tD1_TAG, tD2_TAG, tD1_CA, tD5_CWE, tD2_COE, tD2_CCS, tD1_RAMW, tD5_CPU

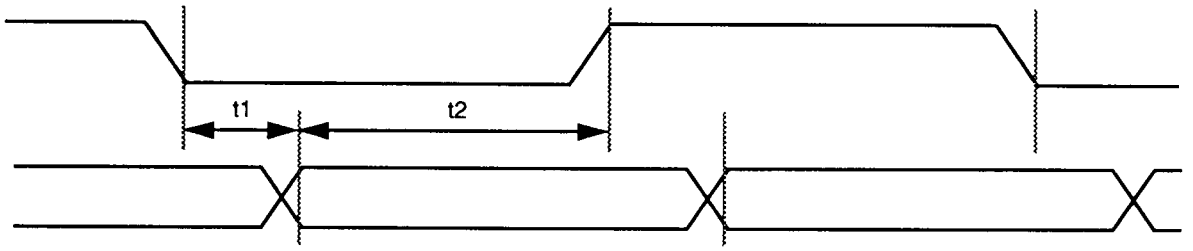
t3 = tD2_CWE

FIGURE 4. CPU INTERFACE AND DRAM CONTROLLER (3)



t1 = tA1_CPU, tA1_DRAM, tA1_PAR
t2 = tF1_CPU, tF2_CPU, tF3_CPU, tF1_PAR

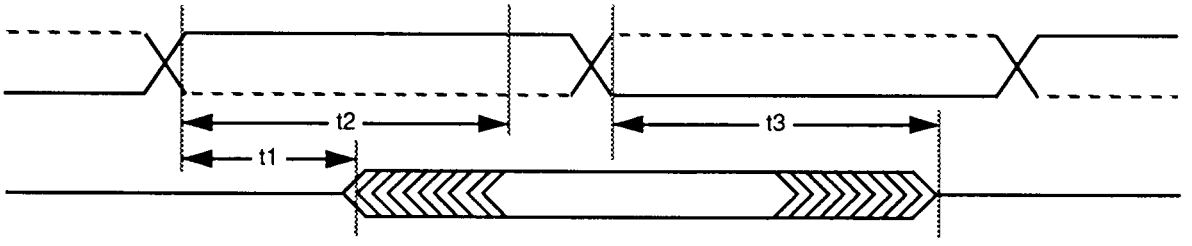
FIGURE 5. ISA BUS CONTROLLER (1)



t1 = tD1_EALE, tD1_BALE, tD1_CMD, tD1_SCMD, tH1_CS1`6, tHJ1_WS0, tH1_CHR, tH1_SD, tH2_D, tF1_RFSH, tD2_SA, tD1_ISLD, tH1_ISDI, tD1_A, tD1_MEMR, tH1_RFSH, tH2_CHR, tD1_DK, tH3_D, tD1_TC, tD1_DKEN, tD2_CMD, tD1_A, tD3_SA, tH3_CHR, tD2_SCD, tH1_D, tD1_RSD, tD1_SA, tD1_SD, tD1_PCS, tD1_PCS

t2 = tS1_CS16, tS1_WS0, tS2_CHR, tS1_SD, tS2_D, tS1_RFSH, tS2_CHR, tS1_DRQ, tS3_CHR, tS1_ISDI, tS3_D

FIGURE 6. ISA BUS CONTROLLER (2)

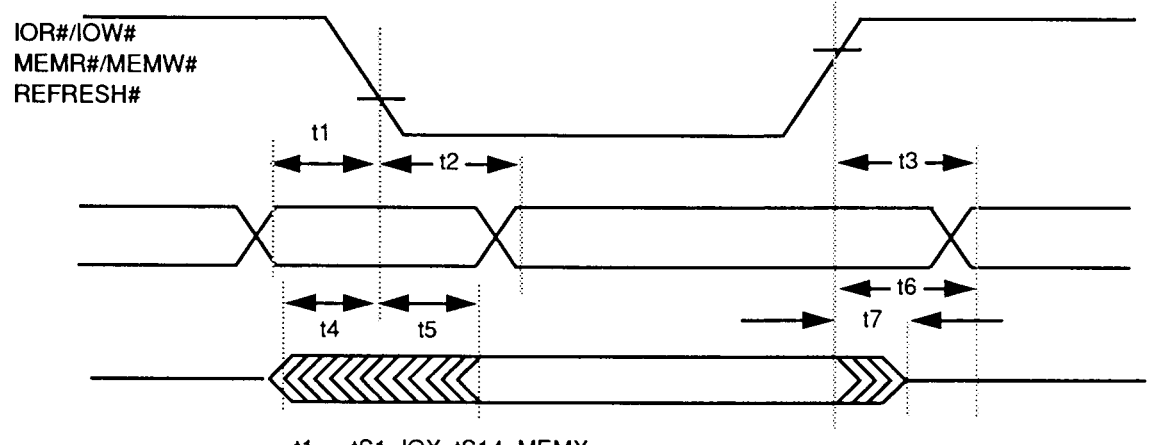


t1 = tA_DK, tA1_A, tA2_SCD

t2 = tD1_SD

t3 = tF1_SCMD, tF1_SD, tF1_RFSH, tF1_DK, tF1_A, tF2_SCD

FIGURE 7. ISA BUS CONTROLLER (3)



t1 = tS1_IOX, tS14_MEMX

t2 = tD1_IGNE, tH1_MEMX, tD2_SCMD, tD1_A20M

t3 = tD1_SPKR, tH1_IOX, tD2_SCMD

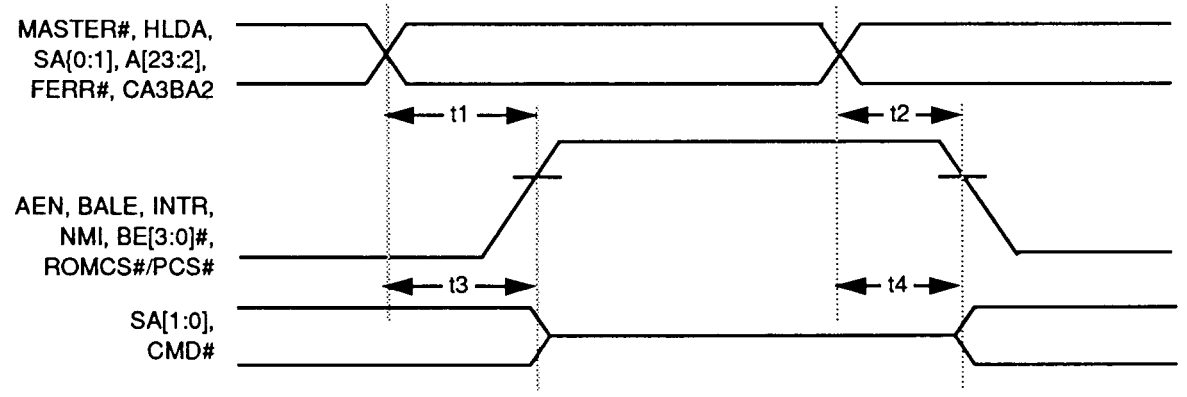
t4 = tS2_SD, tS1_A

t5 = tD3_SD, tA2_SD, tA3_SD, tA1, SMR

t6 = tF2_SD, tF3_SD, tF4_SD, tF1_SMR, tH1_A

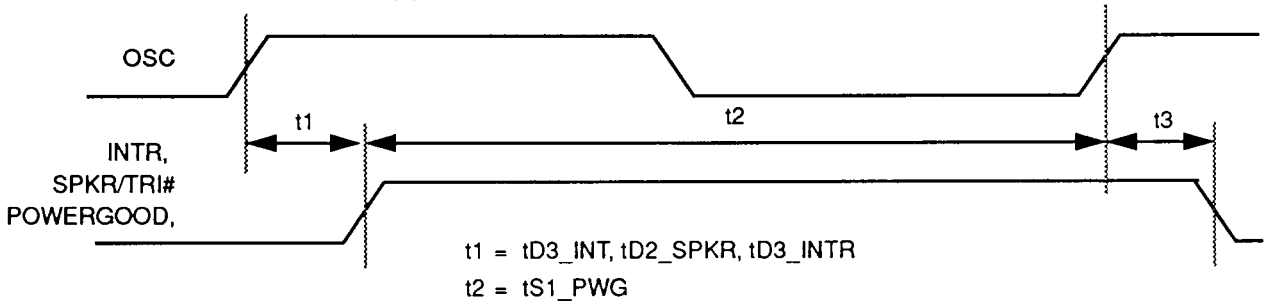
t7 = tH2_SD

FIGURE 8. ISA BUS CONTROLLER (4)



t1 = tD1_AEN, tD2_AEN, tD2_BALE, tD1_NMI, tD1_BE, tD2_PCS, tD1_INTRE
t2 = tD1_AEN, tD2_AEN, tD2_BALE, tD1_NMI, tD2_PPS
t3 = tF1_SACD, tF1_SCMD
t4 = tA1_SACD, tA1_SCMD

FIGURE 9. ISA BUS CONTROLLER (5)



t1 = tD3_INT, tD2_SPKR, tD3_INTR
t2 = tS1_PWG
t3 = tH1_PWG

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground Potential –0.5 V to VDD + 0.3 V

Applied Output Voltage –0.5 V to VDD + 0.3 V

Applied Input Voltage –0.5 V to + 7.0 V

Power Dissipation 1 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs
VILC	Input Low Voltage	–0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD – 0.8	VDD + 0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD – 0.45		V	IOH = –1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 6 mA, Note 2
VOH2	Output High Voltage	VDD – 0.45		V	IOH = –2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, SLTDRV = 0 IOL = 24 mA, SLTDRV = 1, Note 3
VOH3	Output High Voltage	VDD – 0.4		V	IOH = –6 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 24 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 24 mA, RAMDRV[1:0] = 00 IOL = 48 mA, RAMDRV[1:0] = 01 IOL = 48 mA, RAMDRV[1:0] = 10 IOL =48 mA, RAMDRV[1:0] = 11, Note 5
VOH4	Output High Voltage	2.4		V	IOH = –6 mA, Note 5
VOL6	Output Low Voltage		0.45	V	IOL = 24 mA, Note 6
VOH5	Output High Voltage	2.4		V	IOH = –24 mA, Note 6
VOL7	Output Low Voltage		0.45	V	IOL = 12 mA, RAMDRV[1:0] = 00 IOL = 12 mA, RAMDRV[1:0] = 01 IOL = 24 mA, RAMDRV[1:0] = 10 IOL = 24 mA, RAMDRV[1:0] = 11, Note 7
VOH7	Output High Voltage	VDD – 0.45		V	IOH = –6 mA, Note 7
VOL8	Output Low Voltage		0.45	V	IOL = 12 mA, Note 8
VOH8	Output High Voltage	VDD – 0.45		V	IOH = –6 mA, Note 8
VOL9	Output Low Voltage		0.45	V	IOL = 6 mA, Note 11
ILI	Input Leakage Current	–10	10	µA	Note 9
IIL	Input Leakage Current	–500	10	µA	Note 10
IIH	Input Leakage Current	–10	500	µA	Note 12

(Continued on next page.)

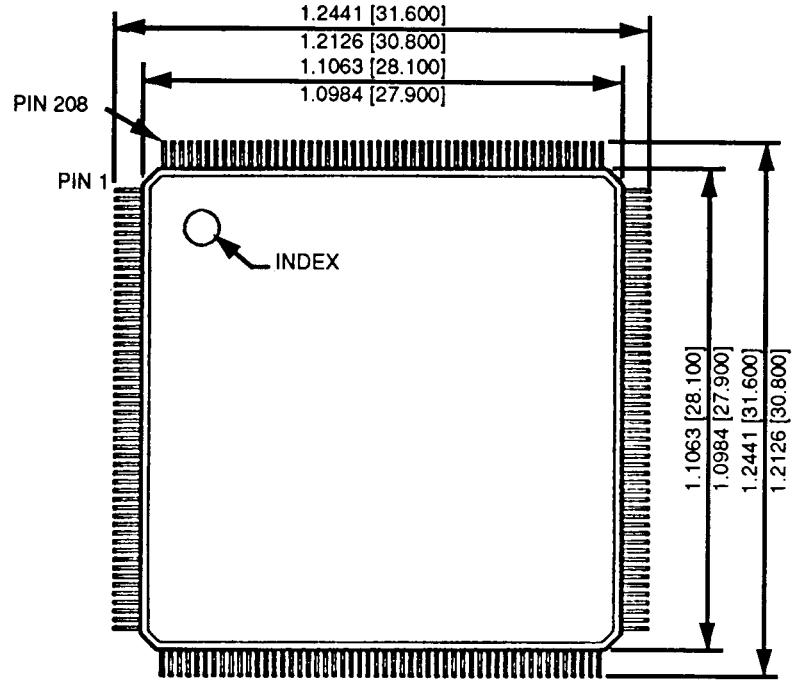
DC CHARACTERISTICS (Cont.)

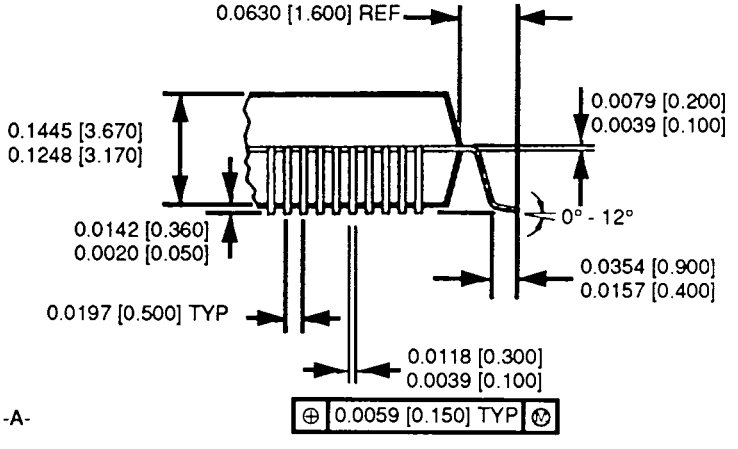
Symbol	Parameter	Min	Max	Unit	Condition
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Power Supply Current		500	µA	
IDDOP	Dynamic Power Supply Current		5	mA/MHz	No DC Loads
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance	VDD – 0.45	10	pF	

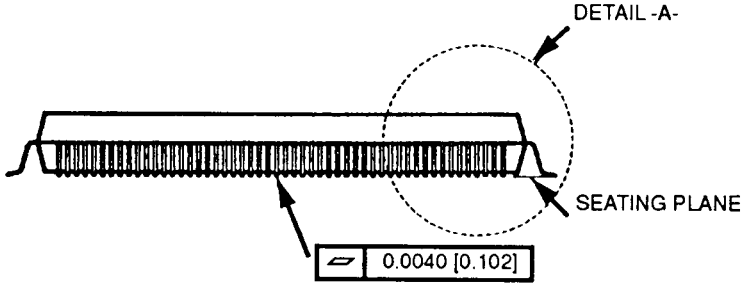
Notes:
1. Pins: HOLD, INTR, NMI, ROMCS#/PCS#, A20M#, ADS#.
2. Pins: TAG[8:0], CWE[3:0]#, CCSA#, CCSB#, COEB#, TAGWE#, RDY#, BRDY#, RESCPU, PAR[3:0], SPKR/TRI#, A[31], A[26:2], BE[3:0]#, D[31:0], DKEN, W/R#_DK2, CA3A, IGNNE#, BLAST#, D/C#_DK1, M/IO#_DK0, CAS[3:0]#, MDEN#, FERR#, CA3BA2, KEN#, EADS#.
3. Pins: SD[15:0], SA[1], SA[0], IOW#, IOR#, MEMW#, MEMR#, RSTDRV, BALE, SMEMW#, SMEMR#, SYSCLK, AEN, TC, SBHE#.
4. Pins: REFRESH#.
5. Pins: MA[10:1], RAMW#/EALE#.
6. Pins: CLK1
7. Pins: RAS[3:0]#, MA0X, MA0Y.
8. Pins: CASX[3:0]#, CASY[3:0]#.
9. All inputs except those listed in Notes 10 and 12 (below).
10. Pins: CA3A, RDY#, BRDY#, FERR#, CA3BA2, DRQ[7:5], DRQ[3:0], BUSOSC, POWERGOOD, SPKR/TRI#, CASX[3:0]#, CASY[3:0]#, TAG8, A20M#, A20, IGNNE#, MA0X, MA0Y, COEB#, EADS#.
11. Pins: IOCHRDY, A[26], A[31].
12. Pins: KEN#, HITM#.

MECHANICAL PACKAGE OUTLINE

208 Lead Plastic Quad Flat Pack (Dwg No.25-90006*A)







Notes:

1. Controlling dimension in mm.
2. Dimensions are in inches (millimeters).

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