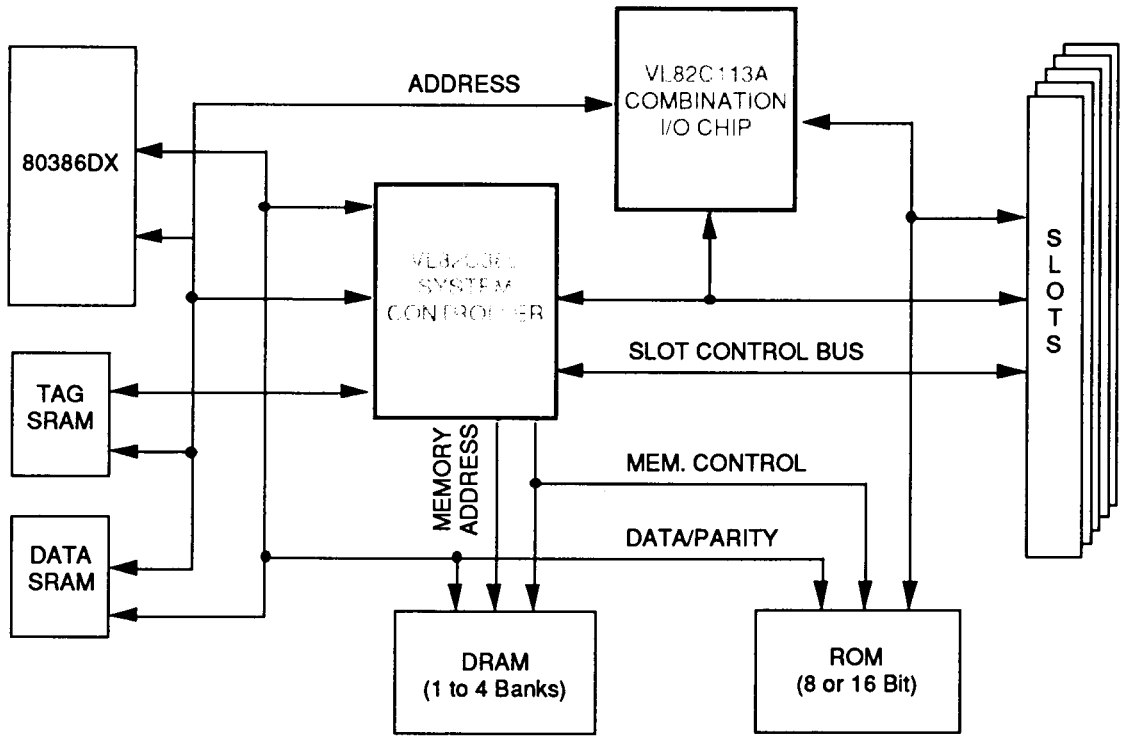
VL82C380 SINGLE-CHIP 386DX PC/AT ISA CONTROLLER WITH ON-CHIP CACHE CONTROLLER



OVERVIEW

VLSI Technology, Inc.'s VL82C380 is a highly integrated 32-bit single-chip PC/AT controller with on-chip cache controller designed for use in 386DX-based ISA systems operating at up to 40 MHz. Its cache controller is designed with a look-aside, write-back architecture for increased write performance as well as read performance. Full coherency is maintained during DMA/Master Mode cycles.

The VL82C380 is a highly integration solution. A complete system can be implemented using only the CPU, BIOS, DRAM, VL82C380, VL82C113A Combination I/O and 3 SSI TTL's, plus optional TAG and Data SRAMs.

Tag SRAMs can be either 8- or 9-bit (7- or 8-bit tag plus a dirty bit). Dirty and Valid bits are optional; each may be disabled in order to increase cacheable DRAM range. The Dirty bit, when used, indicates that the cache has been updated but not the corresponding locations in DRAM. The Valid bit, when used, indicates that both the cache and corresponding DRAM locations have been updated.

Only on-board DRAM is cached; this prevents coherency issues associated with caching system memory located on the ISA bus.

Full coherency is maintained during DMA/Master mode cycles, so flushing and invalidating operations are unnecessary. Set-up/sizing mode (programmable) provides direct access to the cache data SRAMs.

The Memory Controller logic is capable of accessing up to 64 MB. There can be up to 4 banks of 256K, 1M, or 4M DRAMs used in the system. The VL82C380 can drive two banks without external buffering. Built-in page-mode operation and up to 2-way interleaving allow the PC designer to maximize system performance using low-cost DRAMs. Programmable DRAM timing is provided for RAS precharge, RAS to CAS delay, and CAS pulse width.

CONTROLLER OPERATION

Three special programmable address regions are provided. The Fast Bus Clock Region allows accesses to certain memory regions at a faster ISA clock rate for fast on-board or off-board devices. A set of registers allows a memory range anywhere in the first 64 MB of memory to be marked as a DRAM region, an ISA bus region, or a Local Bus region, either cacheable or non-cacheable in increments of 2 KB, 64 KB, or 1 MB.

Further support for devices that reside on the Local Bus is provided through use of the Local Bus Access input, which deselects the VL82C380 during CPU cycles. Also, a memory range anywhere in the first 64 MB of memory can be programmed via the internal mapping registers to make the VL82C380 access a Local Bus Device as a CPU-bus memory device during DMA or Master Mode transfers.

The VL82C380 handles system board refresh directly and also controls the timing of slot bus refresh. Refresh may be performed in synchronous, asynchronous, or decoupled mode. The VL82C380 supports the PC/AT standard refresh period of 15.625 microseconds as well as 125 microseconds.

The Interrupt Controller logic consists of two 8259 megacells with 8 interrupt request lines each. The two megacells are cascaded internally and two of the interrupt request inputs are connected to internal circuitry, so a total of 13 external interrupt request lines are available. Interrupts are scanned into the VL82C380 serially.

The Interval Timer includes one 8254 Counter/Timer megacell. The Counter/Timer has three independent 16-bit counters and six programmable counter modes.

The two DMA controllers are 8237 compatible. Each controls data transfers between an I/O channel and on-board or off-board memory. The DMA controllers can transfer data over the full 64M range available. Internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus, and 74LS612 memory mappers are integrated to generate the upper address bits.

The VL82C380 can be programmed for asynchronous or synchronous operation of the AT bus.

The VL82C380 also performs all of the data buffer control functions required for an 80386DX-based PC/AT system. Under the control of the CPU, the VL82C380 routes data to and from the CPU's D bus, the internal XD bus, and the slots (SD bus). During CPU ISA bus reads, the data is latched for synchronization with the CPU. Parity is checked for D bus DRAM read operations. The chip does not generate parity for CPU writes to DRAM.

When the DMA requestor or external bus master is the bus owner, the VL82C380 allows data transfer between the slot SD bus and the CPU local D bus. The chip also performs low-to-high and high-to-low byte swaps on the 16-bit SD bus. Parity is generated by the VL82C380 during DMA or MASTER writes to on-board DRAM. The chip also provides a single input to disable all of its outputs for board level testability.

VL82C380 Controller functions are programmable via a set of internal configuration registers. The state of various interface pins at reset is used to determine the default configuration. A dip switch can be used to establish the initial configuration.

The VL82C380's cache controller is a direct-map, look-aside, write-back design with external tags which can control one or two banks of cache SRAM. TAG SRAM can be either x8 or x9, and commodity SRAMs can be used for both TAG and data.

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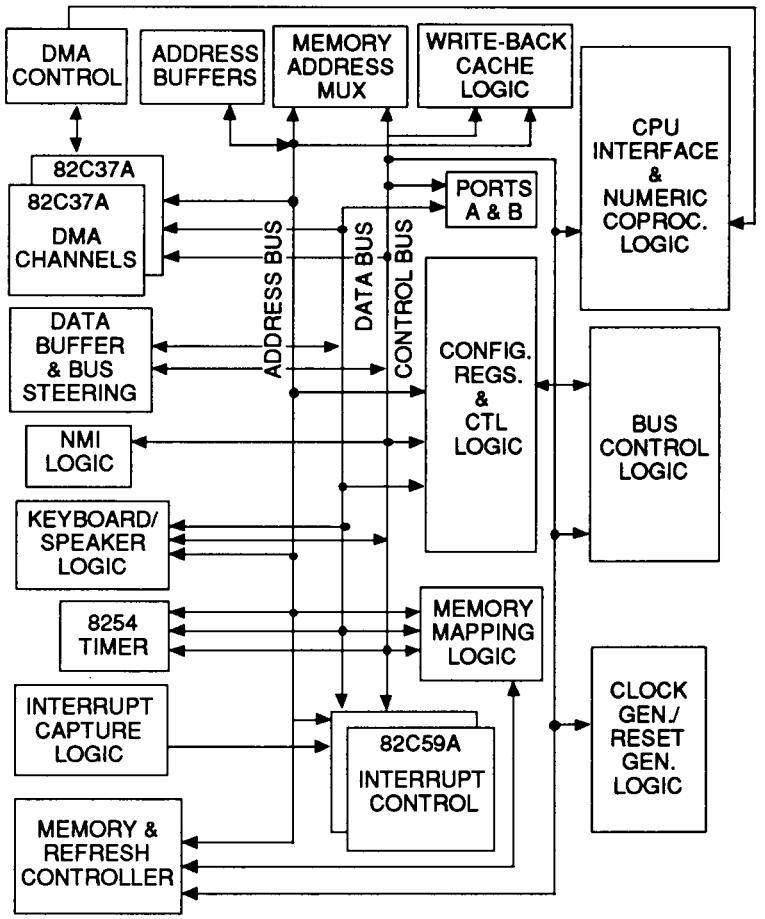

PACKAGING

PART NUMBER	DESCRIPTION	PACKAGE
VL82C380-FC	Single-Chip 386DX PC/AT ISA Controller with On-Chip Cache Controller	208-lead Metric Quad Flat Pack
NOTE: Operating temperature range is 0°C to +70°C		

VL82C380 SINGLE-CHIP 386DX PC/AT ISA CONTROLLER WITH ON-CHIP CACHE CONTROLLER

SYSTEM SUPPORT

VLSI Technology offers extensive support for system designers to assist them in their design applications.

- Samples of the VL82C380 Single-chip 386DX Controller
- Evaluation boards available
- Documentation
  - Data sheet
  - Sample schematics
- Support
  - Support provided by VLSI Technology's Applications Group

RELATED PRODUCTS LISTING

VL82C113A – The SCAMP™ Combination I/O chip is an integrated periperal controller that has been optimized for use with VLSI's VL82C380, VL82C486, VL82C310, VL82C311, and VL82C311L single-chip controllers in PC/AT-compatible computer systems. This chip combines a keyboard controller and a real-time clock with the slot address latches/ buffers which are normally required in PC/AT -compatible systems. The VL82C113A was developed with VLSI's 1.0 micron CMOS technology and is available in a 100-lead MQFP. When used with VLSI's single-chip controllers, this chip allows designers to implement a very cost-effective minimum chip count motherboard.

VL82C386-SET – TOPCAT 386DX a very high-integration three-chip set for use in the design of PC/AT-compatible based systems. This chip set is intended for use in 80386DX microprocessor-based systems with clock speeds from 16 to 33 MHz.

VL82C310/VL82C311/VL82C311L – The SCAMP Controller chips are very cost-effective mid-range featured chips that are designed for use in notebook, laptop, portable, and cached desktop PC/AT-compatible based systems. These chips are intended for use in 286 and 386SX microprocessor-based systems with clock speeds from 10 to 25 MHz.

VL82C486 – Single-chip high-performance 486 PC/AT-compatible controller for use in 486SX- and 486DX-based personal computer systmes running up to 33 MHz.

VL82C380 SINGLE-CHIP 386DX PC/AT ISA CONTROLLER WITH ON-CHIP CACHE CONTROLLER

FEATURES	BENEFITS
• Highly integrated system solution using VL82C380 single-chip ISA controller, VL82C113A Combination I/O Chip and 3 TTLs.	• Smaller PC board, higher reliability, lower power consumption
• Supports one- or two-bank write-back cache – External TAGs – 32 Kbyte to 1 Mbyte cache size – 0 or 1 wait state writes – Separate dirty RAM not required; first write to clean, valid line sets dirty bit	• Increased write performance with flexible system design
• Caches main system DRAM only	• Eliminates coherency problems associated with caching memory on the ISA bus
• Maintains full coherency during DMA/MASTER mode cycles	• Never requires flushing or invalidating
• Optional remap of video and hard disk ROM BIOS onto motherboard, allowing use of single BIOS ROM	• Allows fast video refresh and requires only one BIOS ROM
• Optional bus acceleration for video accesses, with programmable address regions	• Increased video perfomance
• Software-configurable	• Eliminates hardware switches
• Utilizes proven 8254, 8237, 8259 megacells used in all previous VLSI Technology PC/AT chipsets	• Uses proven, reliable, high-performance technology
• High-performance memory controller: – One wait state reads up to 33 MHz, Zero wait state reads up to 40 MHz – Automatic configuring of Bank start address – Each bank individually configurable for any supported DRAM type – Shadow RAM support from 640K to 1M in 16K segments – Staggered refresh reduces power supply peak currents – Decoupled-mode refresh improves performance – Programmable refresh frequency for support of slow-refresh DRAMs – Up to 64 Mbytes of motherboard memory in one to four banks using 256K, 1M, and/or 4 Mbit DRAM, all motherboard memory is cacheble – Direct-drive up to 2 banks (32 Mbyte) of mother board memory – Two-way page mode interleave – Supports 32-bit non-interleaved or interleaved configurations – Programmable RAS/CAS timing supported for Cycle-start, Trp, Trcd, and Tcas	• Single-board design for cached/non-cached systems provides a wide range of differentiating performance options

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