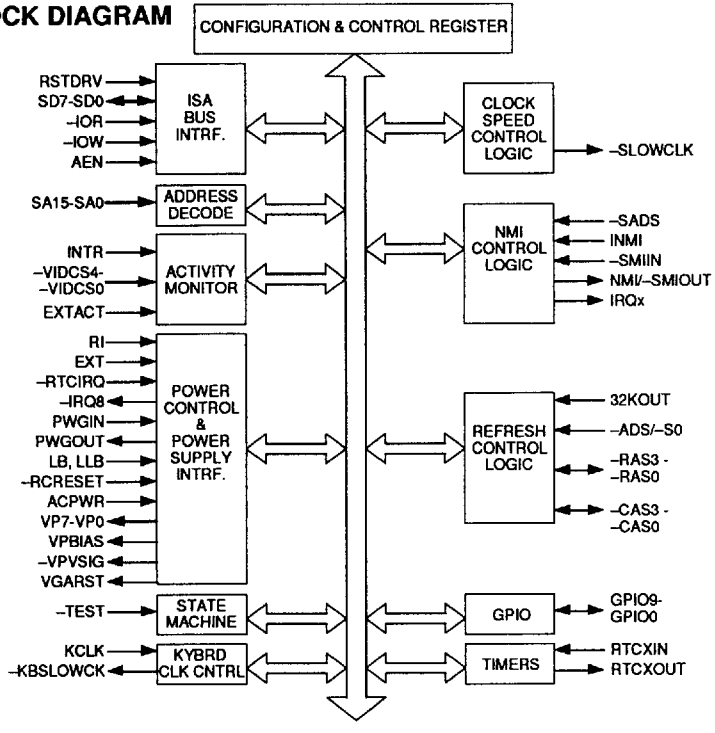
VL82C323

SCAMP™ II 5 VOLT POWER MANAGEMENT UNIT

FEATURES

- Supports X86-based PC/AT-compatible systems
- Provides system activity monitoring, peripheral control, power supply control, mode timers, and general purpose I/O for laptop/notebook power management
- Includes the logic to support X86 processors with the Systems Management Mode (SMM) feature
- Five operation modes:
  - On Mode
  - Doze Mode
  - Sleep Mode
  - Suspend Mode
  - Off Mode
- Independent programmable timers for power saving modes
- Independent programmable timers for LCD and backlight control
- Ten individual power control outputs:
  - Three for LCD power
  - Seven general purpose for peripherals
- Two to four low battery warning monitors
- Multiple power-on sources from Suspend/Off Mode:
  - Push-button
  - Real-time clock alarm
  - Modem ring
- AC power monitoring to disable PMU function
- Suspend Mode refresh options: none, CAS-before-RAS, Self-Refresh
- Leakage control of outputs during Suspend Mode
- Wide range of LCD panel power-up/-down sequencing
- Ten general purpose I/O ports; eight with additional I/O features:
  - One programmable blinking I/O
  - Two optional low battery inputs
- Watchdog timer to turn-off system power if low battery NMI is not serviced
- Programmable interrupt generation on:
  - PMU power mode
  - Low battery warning
  - External input
  - LCD panel timer
  - Reschedule Suspend Mode Interrupt by BIOS
  - Activity detection
- Generated interrupt selectable as IRQx, NMI, or SMI
- Controls SCAMP™ I or SCAMP II (VL82C310 or VL82C316) –SLEEP pin
- Real-time clock alarm IRQ output pin for SCAMP I Controller
- 1.5-micron CMOS technology
- 100-lead (thin) metric quad flat pack (MQFP)

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C323-FC	(Thin) Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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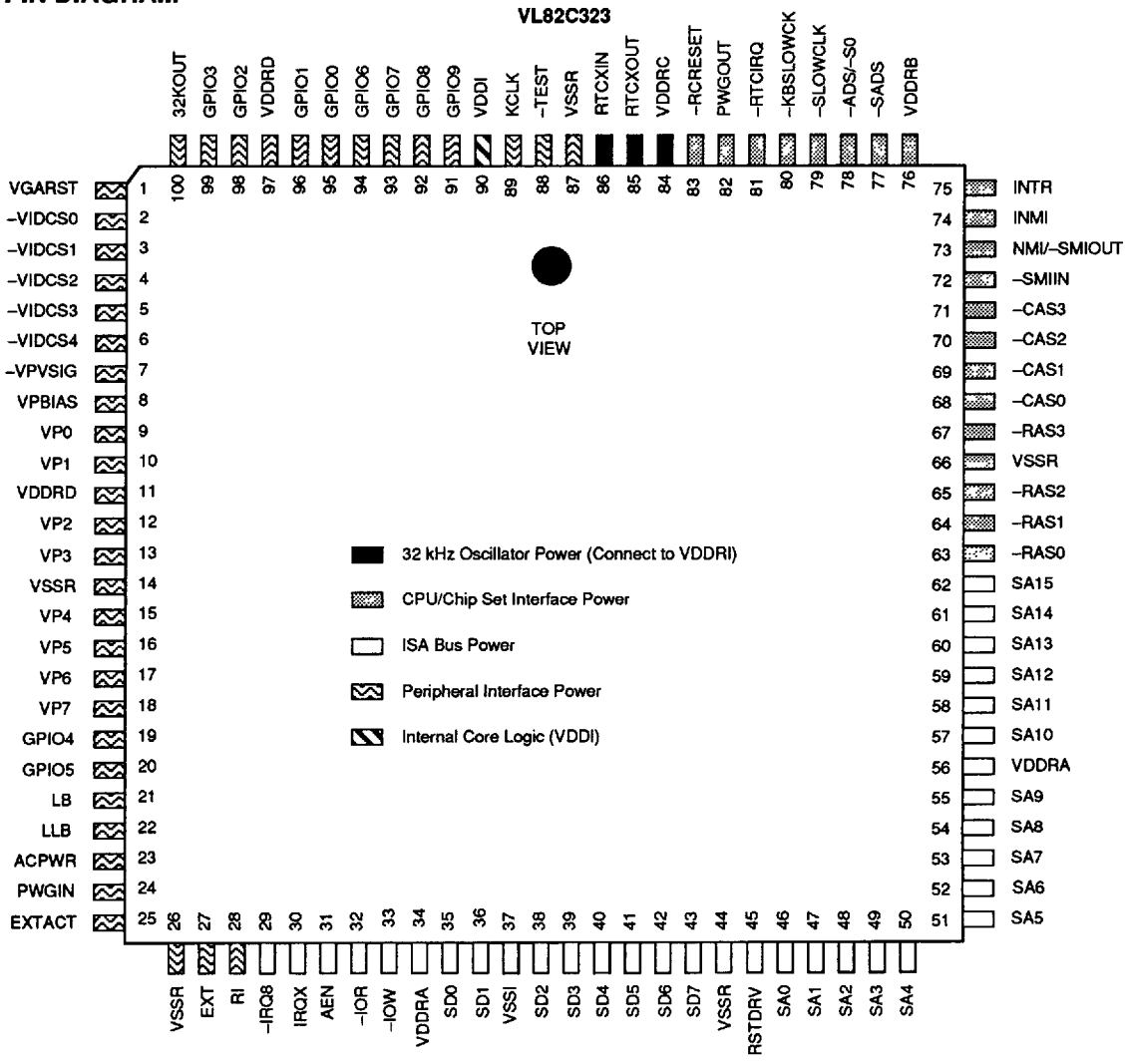
PIN DIAGRAM



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PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail
1	VGARST	O-1		8.0	D	34	VDDRA		PWR		
2	–VIDCS0	IO-3 (Note 1, 3)	TTL	12.0	D	35	SD0	IO-4	TTL	24.0	A
3	–VIDCS1	IO-3 (Note 1, 3)	TTL	12.0	D	36	SD1	IO-4	TTL	24.0	A
4	–VIDCS2	IO-3 (Note 1, 3)	TTL	12.0	D	37	VSSI		GND		
5	–VIDCS3	IO-3 (Note 1, 3)	TTL	12.0	D	38	SD2	IO-4	TTL	24.0	A
6	–VIDCS4	IO-3 (Note 1, 3)	TTL	12.0	D	39	SD3	IO-4	TTL	24.0	A
7	–VPVSIG	O-1		8.0	D	40	SD4	IO-4	TTL	24.0	A
8	VPBIAS	O-1		8.0	D	41	SD5	IO-4	TTL	24.0	A
9	VP0	O-1		8.0	D	42	SD6	IO-4	TTL	24.0	A
10	VP1	O-1		8.0	D	43	SD7	IO-4	TTL	24.0	A
11	VDDRD		PWR			44	VSSR		GND		
12	VP2	O-1		8.0	D	45	RSTDRV (Note 2)	IO-1	TTL	8.0	A
13	VP3	O-1		8.0	D	46	SA0 (Note 2)	IO-1	TTL	8.0	A
14	VSSR		GND			47	SA1 (Note 2)	IO-1	TTL	8.0	A
15	VP4	O-1		8.0	D	48	SA2 (Note 2)	IO-1	TTL	8.0	A
16	VP5	O-1		8.0	D	49	SA3 (Note 2)	IO-1	TTL	8.0	A
17	VP6	O-1		8.0	D	50	SA4 (Note 2)	IO-1	TTL	8.0	A
18	VP7	O-1		8.0	D	51	SA5 (Note 2)	IO-1	TTL	8.0	A
19	GPIO4	IO-3 (Note 1)	TTL	12.0	D	52	SA6 (Note 2)	IO-1	TTL	8.0	A
20	GPIO5	IO-3 (Note 1)	TTL	12.0	D	53	SA7 (Note 2)	IO-1	TTL	8.0	A
21	LB	I (Note 1)	TTL		D	54	SA8 (Note 2)	IO-1	TTL	8.0	A
22	LLB	I (Note 1)	TTL		D	55	SA9 (Note 2)	IO-1	TTL	8.0	A
23	ACPWR	I (Note 1)	TTL		D	56	VDDRA		PWR		
24	PWGIN	I (Note 1)	CMOS-S		D	57	SA10 (Note 2)	IO-1	TTL	8.0	A
25	EXTACT	I (Note 1)	TTL		D	58	SA11 (Note 2)	IO-1	TTL	8.0	A
26	VSSR		GND			59	SA12 (Note 2)	IO-1	TTL	8.0	A
27	EXT	I (Note 1)	TTL		D	60	SA13 (Note 2)	IO-1	TTL	8.0	
28	RI	I (Note 1)	CMOS-S		A	61	SA14 (Note 2)	IO-1	TTL	8.0	A
29	–IRQ8	O-1		8.0	A	62	SA15 (Note 2)	IO-1	TTL	8.0	A
30	IRQx	O-1		8.0	A	63	–RAS0	IO-2	TTL	12.0	B
31	AEN (Note 2)	IO-1	TTL	8.0	A	64	–RAS1	IO-2	TTL	12.0	B
32	–IOR (Note 2)	IO-1	TTL	8.0	A	65	–RAS2	IO-2	TTL	12.0	B
33	–IOW (Note 2)	IO-1	TTL	8.0	A	66	VSSR		GND		

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PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail
67	–RAS3	IO-2	TTL	12.0	B	84	VDDRC		PWR		
68	–CAS0	IO-2	TTL	12.0	B	85	RTCXOUT	O			C
69	–CAS1	IO-2	TTL	12.0	B	86	RTCXIN	I	CMOS		C
70	–CAS2	IO-2	TTL	12.0	B	87	VSSR		GND		
71	–CAS3	IO-2	TTL	12.0	B	88	–TEST	I-PU	TTL		D
72	–SMIIN	I	CMOS-S		B	89	KCLK	IO-3 (Note 1, 3)	CMOS	12.0	D
73	NMI/–SMIOUT	O-1		8.0	B	90	VDDI		PWR		
74	INMI (Note 2)	IO-1	TTL	8.0	B	91	GPIO9	IO-2	TTL	12.0	D
75	INTR (Note 2)	IO-1	TTL	8.0	B	92	GPIO8	IO-2	TTL	12.0	D
76	VDDRB		PWR			93	GPIO7	IO-3 (Note 1)	TTL	12.0	D
77	–SADS (Note 2)	IO-1	TTL	8.0	B	94	GPIO6	IO-3 (Note 1)	TTL	12.0	D
78	–ADS/–S0 (Note 2)	IO-1	TTL	8.0	B	95	GPIO0	IO-2	TTL	12.0	D
79	–SLOWCLK	O-1	TTL	8.0	B	96	GPIO1	IO-2	TTL	12.0	D
80	–KBSLOWCK	O-1		8.0	B	97	VDDRD		PWR		
81	–RTCIRQ	I	TTL		B	98	GPIO2	IO-2	TTL	12.0	D
82	PWGOUT	O-1		8.0	B	99	GPIO3	IO-2	TTL	12.0	D
83	–RCRESET	I	CMOS-S		B	100	32KOUT	O-1		8.0	D

Notes: 1. These inputs have no P-diodes.

2. These pins are outputs only when the VL82C323 is in the Suspend or Off Modes.

3. These pins are outputs only when the VL82C323 is in the Off Mode.

Legend:

CMOS	CMOS-compatible input
GND	A ground pin
I	Input-only pin
IO	Bidirectional pin
PU	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VDD.
PWR	A power supply pin
TTL	TTL-compatible input
-S	Indicates a Schmitt-trigger input with hystersis for noise immunity.
-1	Pad type with 8.0 mA drive.
-2	Pad type with 12.0 mA drive.
-3	Pad type with 12.0 mA drive plus Note 1 above.
-4	Pad type with 24.0 mA drive.

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SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
VGARST	1	VGA Reset - An output signal that is sent to the VGA controller's reset input.
–VIDCS4 - –VIDCS0	6-2	Video Controller Chip Select bits 4 through 0 - These are the VGA controller write enable signals. They lack P-diodes on the inputs and may be driven above the VDDRD power supply level.
–VPVSIG	7	Video Power Signal - An active low, open drain output signal used to control the LCD clock and data buffer.
VPBIAS	8	Video Power Bias - This power control output signal is used for controlling the LCD display's bias power. Its polarity is the same as VP0.
VP0	9	Video Power bit 0 - This power control output signal is used for controlling the LCD panel power. Its polarity is determined by the Polarity Register.
VP1	10	Video Power bit 1 - This power control signal is used for controlling the LCD backlight power. Its polarity is determined by the Polarity Register.
VP7-VP2	18-15, 13, 12	Video Power bits 7 through 2 - These power control signals are used for controlling user selected power. Their polarity is determined by the Polarity Register.
LB	21	Low Battery - An active high input signal from the power supply to the VL82C323 that indicates the battery level is low. It is the first low-level battery warning signal. This input has no P-diode and may be driven above the VDDRD power supply level.
LLB	22	Low Low Battery - An active high input signal from the power supply to the VL82C323 that indicates the battery level is low. It is the second low-level battery warning signal. This input has no P-diode and may be driven above the VDDRD power supply level.
ACPWR	23	AC Power - An input signal from the power supply that informs the VL82C323 that the system is running on AC power. When this signal is high, the VL82C323 disables Doze, Sleep, and LCD Timers which in turn disables the automatic hardware power saving features. This input has no P-diode and may be driven above the VDDRD power supply level.
PWGIN	24	Power Good - An input signal from the power supply to the VL82C323 that indicates that the power is stable. This input has no P-diode and may be driven above the VDDRD power supply level.
EXTACT	25	External Activity - On the rising edge of this input signal the VL82C323 will exit from the Doze or Sleep Mode, or generate an interrupt. It has no effect in the On Mode. This input has no P-diode and may be driven above the VDDRD power supply level.
EXT	27	External Wake-up - This active high input signal is intended for use with an external push-button switch. A rising edge on this input while the VL82C323 is not in the Suspend or Off Modes will generate an interrupt. This input has no P-diode and may be driven above the VDDRD power supply level.
RI	28	Ring Indicator - This active high input signal is intended for use with an external modem. The VL82C323 puts the system into the On Mode when it detects a pre-programmed number of transitions while in the Suspend or Off Modes. This input has no P-diode and may be driven above the VDDRD power supply level.
–IRQ8	29	RTC Interrupt Request - An output signal regenerated by the VL82C323 from the VL82C107 Combination I/O chip and sent to VL82C310. In systems using the VL82C316 SCAMP Controller, this signal is not connected; the RTC is built into the VL82C316.
IRQx	30	Interrupt Request output. This signal may be connected to any unused IRQ output. IRQ15 is a popular choice.
AEN	31	Address Enable - System bus address enable signal from the system bus. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.

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SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
–IOR	32	I/O Read - A command generated by the VL82C310 or VL82C316 SCAMP Controller and sent to the VL82C323. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–IOW	33	I/O Write - A command generated by the VL82C310 or VL82C316 SCAMP Controller and sent to the VL82C323. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
SD7-SD0	43-38, 36, 35	System Data bus bits 7 through 0 - This bus connects directly to the VL82C310 or VL82C316 SCAMP Controller's system data bus and used to transfer data between the two.
RSTDRV	45	Reset Drive - The system reset input from the system bus. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
SA15-SA0	62-57, 55-46	System Address bus bits 15 through 0 - System address lines from the VL82C310 or VL82C316 SCAMP Controller. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–RAS3 - –RAS0	67, 65-63	DRAM Row Address Strobe bits 3 through 0 - These signals are wired OR with the –RAS lines from the VL82C310 or VL82C316 SCAMP Controller. They are driven by the VL82C323 only in the Suspend Mode and three-state when they are not in the Suspend Mode. The SCAMP Controller three-states these signals in the Suspend Mode. If unconnected or not driven, these signals must be pulled up to VDDRB.
–CAS3 - –CAS0	71-68	DRAM Column Address Strobe bits 3 through 0 - These signals are wired OR with –CAS lines from the VL82C310 or VL82C316 SCAMP Controller. These signals are driven by the VL82C323 only in the Suspend Mode and three-state when they are not in the Suspend Mode. The SCAMP Controller three-states these signals in the Suspend Mode. If unconnected or not driven, these signals must be pulled up to a supply which collapses in the Suspend Mode.
–SMIIN	72	System Management Interrupt Input - An input to the VL82C323 from a connected shared –SMI line with the CPU and VL82C316 SCAMP II Controller.
NMI/–SMIOUT	73	Non-Maskable Interrupt or System Management Interrupt Output – This pin is a dual function pin. Depending upon the desired function, it can be either an NMI output to the CPU or an –SMI output to the VL82C316 SCAMP II Controller.
INMI	74	Input Non-Maskable Interrupt - An input from the from VL82C310 or VL82C316 SCAMP Controller to the VL82C323 that reports PC/AT standard NMIs. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
INTR	75	Interrupt Request - An active high input that is used to interrupt the CPU. It is generated by the VL82C310 or VL82C316 SCAMP Controller and sent to both the CPU and VL82C323. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–SADS	77	SMI Address Strobe - A signal generated by the VL82C316 SCAMP Controller that is used to latch CPU addresses during accesses to SMI address space. A falling edge on this signal causes –SMIOUT to go high. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–ADS/–S0	78	Address Strobe or S0 - Connect to the –ADS input if the CPU is a 386. Connect to –S0 input if the CPU is a 286. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–SLOWCLK	79	Slow Clock - This input signal is the CPU clock speed control signal to VL82C310 or VL82C316 SCAMP Controller. When –SLOWCLK is low, the SCAMP Controller reduces the CPU clock speed to its the programmed divided clock speed.
–KBSLOWCK	80	Keyboard Slow Clock - An output signal that controls the keyboard clock. When low, the VL82C107 SCAMP Combination I/O chip stops the keyboard clock. When high, the VL82C107 starts the keyboard clock.

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SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
–RTCIRQ	81	RTC Interrupt Request - A signal generated by the VL82C107 SCAMP Combination I/O chip and sent to the VL82C323. If the VL82C323 is in either the Suspend or Off Modes and detects any transition on this pin, it puts the system into the On Mode.
PWGOUT	82	Power Good Output - An output signal from the VL82C323 sent to the VL82C310 or VL82C316 SCAMP Controller informing the Controller that the power is good.
–RCRESET	83	RC Reset - External RC reset signal to reset the VL82C323 itself when its power is first applied.
RTCXOUT	85	32 kHz clock feedback.
RTCXIN	86	32 kHz input from the crystal.
–TEST	88	Reserved for testing the VL82C323 (internal pull-up).
KCLK	89	Keyboard Clock - Keyboard clock input from keyboard. When a transition is detected on this signal, the VL82C323 drives –KBSLOWCK high to enable the clock to the keyboard controller.
GPIO9-GPIO0	91-94, 20-19, 99, 98, 96-95	General Purpose Input/Output bits 9 through 0 - General purpose I/O low battery NMI warning option. Note that GPIO7-GPIO4 have no P-diodes and may be driven above the VDDRD power supply level when used as inputs. If used as outputs, an external pull-up resistor is required on GPIO7-GPIO4.
32KOUT	100	Refresh clock for VGA controller in the Suspend Mode.
VDDRA	34, 56	ISA bus interface power.
VDDRB	76	System interface power. Must be the same as VDDI.
VDDRC	84	32 kHz oscillator power. Connects to the same supply as VDDI, but should be separately filtered.
VDDRD	11, 97	Peripheral supply voltage. See the section titled "Operating Voltage Options" under DC Characteristics for additional information.
VDDRI	90	Core logic power.
VSSI	37	Core Logic ground reference.
VSSR	14, 26, 44 66, 87	Pad ring ground reference for VDDRA, VDDRB, VDDRC and VDDRD.

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FUNCTIONAL DESCRIPTION

The VL82C323 SCAMP Power Management Unit (PMU) is intended to be used in conjunction with the VL82C310 SCAMP I System Controller or VL82C316 SCAMP II 5 Volt Power-Managed 386SX Controller and the VL82C107 SCAMP Combination I/O chip. The VL82C323 PMU dramatically reduces overall system power consumption and provides special features for laptop/notebook PC/AT-compatible computers. The power reduction is accomplished via an activity monitor which detects inactivity in the system, and reduces the CPU clock frequency and/or removes power from peripheral devices.

The VL82C323 has five operation modes:

- On Mode
- Doze Mode
- Sleep Mode
- Suspend Mode
- Off Mode

By monitoring the system activity, the VL82C323 switches between modes to achieve power saving without impacting system performance. The VL82C323 also provides an auto power-on feature to turn-on the system power via a push-button switch, modem ring indicator, or real-time clock time of day alarm.

The VL82C323 supports a suspend/resume function in conjunction with the BIOS to allow the user to turn the system power off and save the system information from the current application. When the system power is turned back on, the user is able to resume the application from the point where it was suspended.

PC/AT BUS INTERFACE

The VL82C323 resides on the ISA bus. The control signals –IOR, –IOW, and AEN are used to interface to the VL82C310 or VL82C316 SCAMP Controllers (here after referred to as SCAMP Controller unless specifying an individual device). The SCAMP Controller presents the address and data on the SA and SD buses and ISA bus control signals for all I/O cycles. The VL82C323 is tied to SA15-SA0 and SD7-SD0 buses. The VL82C323 constantly monitors SA15-SA0. If an access of the VL82C323's internal registers occur, the VL82C323 either places the data on SD7-SD0 while –IOR is asserted for an I/O read operation or it latches the data at the rising edge of the –IOW for an I/O write operation. The VL82C323 does not drive the –IOCHRDY signal so the SCAMP Controller uses its programmed number of I/O wait modes to terminate the bus cycle. The VL82C323 fully decodes SA15-SA0.

SCAMP CONTROLLER AND VL82C107 COMBINATION I/O INTERFACE

Clock Switching

The VL82C323 controls the CPU clock speed via the –SLOWCLK pin of the SCAMP Controller if the SCAMP Controller has its Sleep Mode enabled. When the VL82C323 is in the Doze or Sleep Mode, it drives the –SLOWCLK signal low. The SCAMP Controller slows down the clock when it detects a transition from high-to-low on its –SLOWCLK input pin. When it detects a transition from low-to-high, it speeds up to the maximum programmed CPU clock speed. The –SLOWCLK signal is a glitch-free signal and provides a 250 ns minimum pulse width. The frequency of the slow clock depends on the minimum speed of the CPU and can be set by the BIOS during system initialization in the Configuration Registers of the SCAMP Controller.

Please refer to the VL82C310 and VL82C316 SCAMP Controller data manuals for detailed information. Normally, the slow clock frequency is set to the minimum clock speed the CPU will support, i.e., 2 MHz for 386SX-LP and 4 MHz for 386DX.

The VL82C323 drives the –SLOWCLK pin high without exiting the Doze or Sleep Mode for an INTR. It pushes each interrupt occurrence on an internal Stack Register and an end-of-interrupt (EOI) instruction pops each interrupt occurrence from the stack to prevent multiple nested interrupts from slowing the CPU clock until the last EOI. The depth of the stack is 15 deep. When the last EOI is received, the VL82C323 waits for 15 to 30 µs before it drives the –SLOWCLK pin low. This forces the SCAMP Controller back into slow CPU clock operation. The VL82C323 flushes the stack if the AUTOFLUSH bit (bit 6) in the MISCSET Register is set and the VL82C323 enters the On Mode from the Doze or Sleep Mode. If the FLUSH bit (bit 5) in the MISCSET Register is set, the stack operation is disabled and the VL82C323 drives the –SLOWCLK pin low 15 to 30 µs after any EOI. The SCAMP Controller switches to maximum CPU clock speed for DMA or refresh operations automatically. If the –SLOWCLK pin is switched from high-to-low during a DMA operation, the SCAMP Controller waits for the completion of the DMA cycle and then slows down the CPU clock.

If the MSK_VIDM bit (bit 6) in the ACTMASK Register is set, any low transition on the –VIDCS inputs (–VIDCS4 - –VIDCS0) is not treated as an activity detection. The VL82C323 temporarily brings the –SLOWCLK pin high for 8 ms without exiting from the Doze or Sleep Mode. If the MSK_VIDM bit is reset, any low transition on the –VIDCS inputs causes an activity detection. Please refer to the section titled "System Activity Monitor" for more information.

At the end of any NMI service routine, the BIOS writes any data to the NMICAUSE-I Register. The VL82C323 then waits for 15 to 30 µs and drives the –SLOWCLK pin low, restoring slow CPU clock speed. If the BIOS fails to do so, eventually an EOI occurs in response to a Doze Timer interrupt and the VL82C323 brings the –SLOWCLK pin low at that time.

If the EN_HICLK bit (bit 0) in the MISCSET Register is set, the –SLOWCLK and –KBSLOWCK pins stay high but the VL82C323 enters the Doze and Sleep Modes. However, the CPU clock remains at high speed but some unused peripheral devices can still be turned off. This is for the calculation intensive application programs.

If the ACPWR signal is high, the Doze Timer is disabled and the power management function via the internal hardware timer scheme is disabled. However, the Doze or Sleep Modes are still available by a command to the Status Register.

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VL82C323 Registers
The VL82C323's internal registers are accessed by an indexed address and data register scheme which is compatible with the SCAMP Controller. The index value is first written to the Index Register (ECh) and the data is read or written from the Data Register (EDh). The Index Register is a read/write register. When reading the Index Register, the SCAMP Controller returns the value to the CPU. The Index Register is a write-only register in the VL82C323.

The VL82C323's register range is from C0h to DFh. Write access to the Data Registers is locked out when entering the Suspend and Off Modes, and when power is first applied to the VL82C323. Bit 0 (LOCKOUT) in the Supply Register is set to indicate that a write access is not allowed. To unlock it for a write access, the CPU must first read the Supply Register. Once the write access is unlocked, the VL82C323 stays unlocked until it enters either the Suspend or Off Mode, or when –RCRESET is asserted.

RTC –IRQ8 Interrupt Handling in a VL82C310/VL82C107 System
The VL82C323 can be placed into the On Mode by the real-time clock's (RTC) time of day interrupt. The –RTCIRQ pin is an edge sensitive input from the VL82C107 SCAMP Combination I/O chip. In the Suspend Mode, the system power is off and the RTC logic in the VL82C107 and VL82C323 remains powered. In order to prevent leakage through the unpowered VL82C310, the –RTCIRQ signal from the VL82C107 is connected to the VL82C323. The VL82C323 will regenerate the –IRQ8 signal to the VL82C310 from the VL82C107 in normal operation. An external pull-up resistor is required on the –RTCIRQ input pin of the VL82C323 because the VL82C107 uses an open drain output buffer for –RTCIRQ.

Note: The above discussion only applies to use of the VL82C323 in a VL82C310/VL82C107-based system. The RTC is built into the VL82C316. In systems using the VL82C316, the VL82C323's –IRQ8 output signal is not connected to the VL82C316 and leakage control of this signal is not an issue. However, the –RTCIRQ output of the VL82C316 is connected to the VL82C323's –RTCIRQ input to support the time of day wake-up feature.

Keyboard Clock Control
To further reduce power consumption, the VL82C323 controls the keyboard clock in the VL82C107 through two control signals, –KBSLOWCK and KCLK. When the VL82C323 is in either the Doze or Sleep Mode, it drives the –KBSLOWCK signal low and the VL82C107 stops the clock to the keyboard controller. Only when the VL82C323 detects a high-to-low transition on the KCLK signal from the keyboard or an access to the port 60h or 64h occurs, does it drive –KBSLOWCK high for 0.5 to 1.0 seconds, activating the keyboard controller. Any activity other than a keyboard access does not cause the –KBSLOWCK signal to go high unless the VL82C323 returns to the On Mode. The –KBSLOWCK signal is a glitch-free signal and provides a 142 ns minimum width pulse.

Note: The VL82C316 does not have a –KBSLOWCK input. Rather it emulates the above feature internally and provides more advanced and programmable capabilities.

POWER SUPPLY INTERFACE
The VL82C323 controls the power to individual system devices to achieve maximum power savings. It is designed to interface to an intelligent power supply. To take full advantage of the VL82C323's features, the power supply should have the following features.

Power Control Signals
The LB and LLB input signals are used to report low battery conditions. The VL82C323 has ten power control output signals: VP7-VP0, VPBIAS, and –VPVSIG. VP7-VP2 are general purpose power control outputs. VP1 is used to control the LCD backlight power. VP0 is used to control the LCD panel power. VPBIAS is used to control the LCD bias power and –VPVSIG is used to control the LCD clock and data buffer. PWGIN is an input signal from the power supply indicating that the power is good. PWGOUT is an output signal to the SCAMP Controller. ACPWR is an input signal from the power supply to indicate the system is running on AC power. Figure 1 shows how the power supply interfaces to the VL82C323.

LCD Panel Power-Up/Down Sequencing
Most LCD panels have a +5 volt power supply and a bias power supply. These power sources, along with the clock and data lines to the LCD panel, are required to be sequenced correctly to prevent damage to the LCD panel. In addition, isolation must be provided between the LCD controller and the LCD panel to prevent destructive CMOS latch-up when power is applied. The VP0, VPBIAS, and –VPVSIG signals are provided to serve this purpose.

Warning: Improper LCD power sequencing may cause LCD panel damage.

The polarity of VPBIAS and VP0 are controlled by bit 0 in the Polarity Register. The polarity of –VPVSIG is defined to be active low for power-on, and is not programmable.

VP0 is active when bit 0 is set in the PWR Register for the currently active mode, and (in most cases) when the LCD Timer has not timed out.

When power is first applied to the VL82C323, –RCRESET clears the EN_LCDSEQ, LCDTMG0, and LCDTMG1 bits (bits 4-2) in the MISCSET Register, and sets the MSK_LCD bit (bit 1) in the NMIMASK-II Register. This selects the BIOS LCD power sequencing. VP0 and VPBIAS are active high, –VPVSIG is active low and all are inactive or in the Off Mode. From this point, LCD power sequencing may be done either by the BIOS directly manipulating these signals or automatically by the VL82C323 in the Automatic LCD Power Sequence Mode.

Automatic LCD Power Sequence Mode:
This is the simplest method and should be used when the panel timing requirements can be satisfied by the VL82C323.

The Automatic LCD Power Sequence Mode is enabled by setting the EN_LCDSEQ bit in the MISCSET

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Register. When set, VP0, VPBIAS, and –VPVSIG become automatically sequenced outputs and can not be directly controlled by software. The LCDTMG1 and LCDTMG0 bits of the MISCSET Register specify a power sequencing delay time (see Table 16 for more information). VP0 must remain inactive while these bits are programmed, otherwise the VPBIAS and –VPVSIG outputs change state. The initial conditions must be:

1) EN_LCDSEQ, LCDTMG1, and LCDTMG0 are low,
2) the D0 bits in the PWRON and PWRDOZE Registers are low (automatic sequencing disabled, VP0, VPBIAS, and –VPVSIG off).

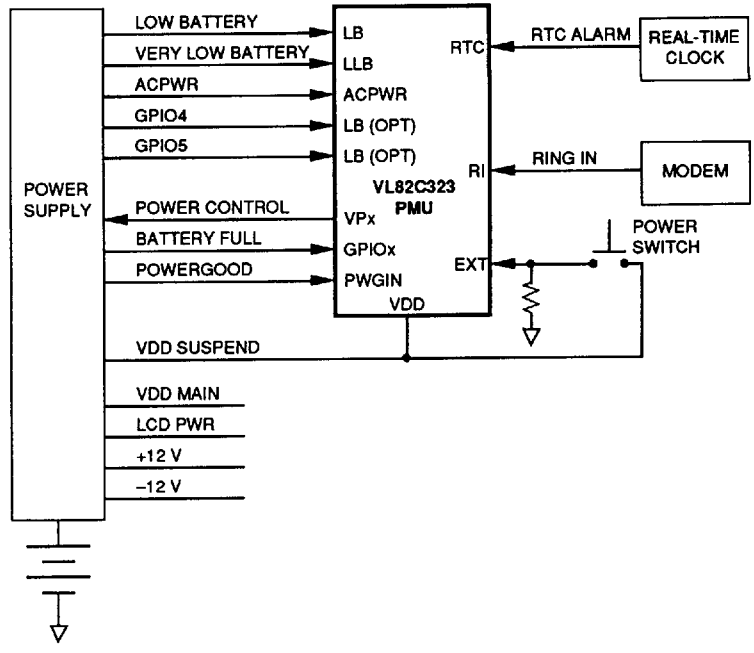
First, EN_LCDSEQ is set. Then LCDTMG1 and LCDTMG0 are set to the desired delay time. Finally, the D0 bits in the PWRON and PWRDOZE Registers are set to allow the display to turn-on in the On or Doze Modes while the LCD Timer has not timed out. Next, VP0 goes active, –VPVSIG goes active after the programmed delay and after another equal delay, VPBIAS goes active. When the display is to be powered down, VPBIAS goes inactive. Then after the delay, –VPVSIG goes inactive, and after another delay VP0 goes off. If the Automatic LCD Power Sequence Mode is enabled when the VL82C323 enters either the Suspend or Off Mode, the LCD sequentially turns off.

BIOS Controlled LCD Power Sequencing

This method is only for special displays that can not be handled with the Automatic Sequence Mode. The BIOS has direct control over the VP0, –VPVSIG, and VPBIAS signals. After –RCRESET, VP0 is controlled normally by the appropriate PWR Register's D0 bit. –VPVSIG and VPBIAS can be activated by setting the LCDTMG1 and LCDTMG0 bits in the MISCSET Register high. To make practical use of this hardware, the BIOS must enable some NMIs.

If the MSK_LCD bit (bit 1) in the NMIMASK-II Register is cleared, the LCD Timer no longer affects VP0. When it times out, it generates an NMI and the BIOS can then control VP0, –VPVSIG and VPBIAS in the proper order and timing. Of course, one or more activity detection NMIs should also be enabled so that the BIOS can turn the LCD back on again. If the EN_LCDSEQ bit is low, the LCDTMG1 and LCDTMG0 bits are cleared when the VL82C323 enters the Off Mode. Figure 2 shows the LCD power sequencing/isolation circuitry.

FIGURE 1. POWER SUPPLY INTERFACE



PMU Reset and Initialization

The VL82C323 requires the –RCRESET input signal to reset itself when power is first applied to it. This signal is generated from an external RC network so a Schmitt-trigger input is used. The resistor should be a 100 kΩ pull-up tied to the VL82C323's VDD, and the capacitor should be a 1.0 µF connected to VSS. The RC network must tie to the same power source as the VL82C323. The PWGIN signal does not affect the initialization of the VL82C323. After the internal registers are written by the CPU, the information remains the same regardless of assertion or deassertion of the PWGIN signal, until a low on the –RCRESET pin is detected or the registers are rewritten by the CPU.

AC Power Monitoring

The ACPWR input informs the VL82C323 that the system is running on AC power. If the ACPWR signal is high, the VL82C323 disables the Doze, Sleep, and LCD Timers which in turn, disables the automatic hardware power saving features. Since these timers are disabled, the system is running at maximum speed and peripheral devices are not turned off. Only the BL Timer is enabled for controlling the LCD backlight. Once the BL backlight is turned off, it is turned back on by any keyboard activity. However, all the power saving features may still be controlled by software when AC power is applied.

Low Battery Warning

The battery condition can be monitored by the power supply or by an external voltage comparison circuit. The VL82C323 has two dedicated pins, LB and LLB, to monitor the battery level. LB is the first-level low battery warning signal. LLB is a very low level battery warning. If a low battery input is high, and the corresponding NMI is unmasked, the VL82C323 will generate an NMI every 15 seconds. The BIOS can

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flash a warning message on the screen, turn-on a low battery indicator, or save the current application and command the VL82C323 to enter the Suspend Mode. The VL82C323 also has two additional GPIO pins that can be programmed as low battery inputs for more levels of battery condition detection. The low battery inputs are debounced. To be recognized, these inputs must be high for two to four seconds if the FASTDB bit (bit 7) in the MISCSET Register is cleared, or 30 to 60 ms if the FASTDB bit is set. See the sections titled "LB, LLB NMI" and "GPIO4 and GPIO5/LB1 and LB2 NMI" for more information.

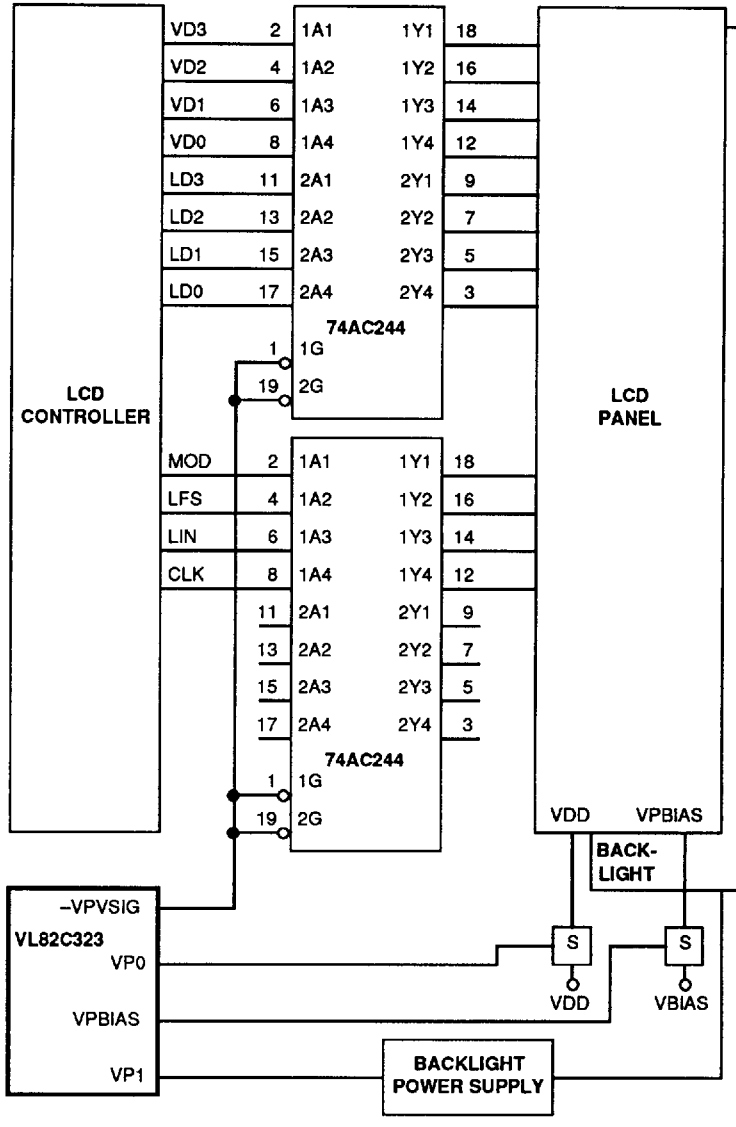
PWGIN and PWGOUT

The PWGIN input is an active high signal from the power supply. PWGIN does not reset the VL82C323 when it goes low. When a transition of PWGIN from low-to-high is detected and after a delay of 0.5 to 1.0 seconds, the VL82C323 asserts the PWGOUT signal high to the SCAMP Controller. If the PWGIN input goes low when the VL82C323 is not in the Suspend or Off Modes, the VL82C323 asserts the PWGOUT signal low immediately and places itself into the Off Mode. PWGOUT goes low before PWGIN goes low if the VL82C323 is commanded to enter either the Suspend or Off Mode.

INTERRUPT GENERATION AND HANDLING

There are 13 different sources for generation of a power management interrupt output logically ORed together by the VL82C323. These can be masked off independently by bits in the NMIMASK-I and II Registers. At power-on all NMIs are masked. When an internal NMI is generated, it generates a minimum 570 ns wide pulse. The cause of the NMI is latched and can be read from the NMICAUSE-I and II Registers. The NMICAUSE-I and II Registers are cleared when read. A read of the NMICAUSE-I Register also clears the NMI cause code in the Status Register. The NMI may also be read from the Status Register for an INMI, Sleep NMI, Activity NMI, Suspend NMI, EXT NMI, LB NMI, and LLB NMI. If any of the NMIs in the NMICAUSE-II Register are enabled, the BIOS should

FIGURE 2. LCD POWER SEQUENCING/ISOLATION CIRCUITRY



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read the NMICAUSE-I and II Registers for NMI information and should not rely on the Status Register. Reading the NMIMASK-I Register does not affect the NMICAUSE-I and II Registers.

A timer is provided to automatically place the VL82C323 in the Off Mode if the LLB NMI is not serviced. See the section titled "Timers" for additional information

Although this specification refers to NMI throughout, the internally generated interrupt can be routed to –SMI or NMI, IRQx, both or neither.

NMI or IRQx Option:
If the MSK_NMI bit (bit 6) in the NMIMASK-I Register is cleared, the NMI pin is driven by the OR of all internally generated interrupts and by the INMI pin. If set, only the INMI drives the NMI output pin. If the MSK_IRQx bit (bit 7) in the NMIMASK-I Register is cleared, the IRQx output is active if any other bit besides the I_NMI bit, is set in either the NMICAUSE-I and II Registers. If set, IRQx remains inactive.

SMI (System Management Interrupt) Option:
(Applies only to X86 processors with the SMM, System Management Mode, feature.)

The programmable options described in the previous paragraph are only true if bit 4 (ALT_INT) of the MISCSET Register is 0 (default case). When ALT_INT is changed to 1, the IRQx output is disabled, the NMI pin definition changes to –SMIOUT, and the –SMIIN input is enabled. In this case, the –SMIOUT pin is driven low by the OR of all internally generated interrupts. It will remain low until the falling edge of the –SADS input pin. Reading the NMI_CAUSE Registers determines why the SMI was generated and re-enables SMI generation when –SMIIN returns inactive high. –SMIIN is also monitored for wake-up from the Doze and Sleep Modes.

Note: The VL82C310 SCAMP I Controller does not support the System Management Mode.

INMI
The INMI input comes from the SCAMP Controller for reporting PC/AT standard NMIs such as parity error or IOCHCHK. If the MSK_NMI bit in the NMIMASK-I Register is set, INMI still causes the NMI output to be active but internally generated interrupts do not.

Doze Timer NMI
When VL82C323 detects no activity and the Doze Timer times out, it generates an NMI if the MSK_DOZE bit (bit 0) is cleared in the NMIMASK-II Register. The VL82C323 remains in the On Mode.

Sleep Timer NMI
If the MSK_SLEEP bit (bit 4) in the NMIMASK-I Register is cleared, the VL82C323 generates an NMI when the Sleep Timer times out and remains in the Doze Mode.

Activity NMI and LCD Activity NMI
If the MSK_DOZE bit is cleared, activity detection occurring while the VL82C323 is in the Doze Mode generates an Activity NMI. The ACT_NMI bit (bit 6) in the NMICAUSE-I Register is set and the VL82C323 remains in the Doze Mode. If the MSK_SLEEP bit in the NMIMASK-I Register is cleared, the VL82C323 behaves the same way as in the Sleep Mode.

If MSK_LCD bit (bit 1) in the NMIMASK-II Register is cleared and the LCD Timer has previously timed out, activity that triggers the LCD Timer causes an LCD Activity NMI. The ACT_LCD_NMI bit (bit 7) in the NMICAUSE-I Register will be set. If EN_LCDSEQ is set, the LCD power is automatically sequenced on; otherwise, the BIOS must turn it on via the power control bits.

Suspend Timer NMI
If the MSK_SUSPEND bit (bit 5) in the NMIMASK-I Register is cleared, the VL82C323 generates an NMI when the Suspend Timer times out and it remains in the Sleep Mode. The BIOS saves the system status and commands the VL82C323 to enter the Suspend Mode. If the MSK_SUSPEND bit is set, the Suspend Timer is disabled. Refer to the section titled "Suspend Mode" for more information on entering Suspend.

Rescheduled Suspend NMI
When the Suspend Timer times out or the EXT pin goes high, the VL82C323 will generate an NMI to inform the BIOS to start the Suspend procedure. However, the application program may be in the middle of something that may cause the system to not be resumeable if entering the Suspend Mode at this moment. If so, a rescheduled Suspend NMI is provided to inform the BIOS to try to enter into the Suspend Mode whenever it is possible. When the MSK_RESCH bit (bit 2) in the NMIMASK-II Register is cleared, the VL82C323 will generate the rescheduled NMI every 60 ms. This feature can also be used to generate tick interrupts for the power management software. See the section titled "Suspend Reschedule Timer" also.

EXT NMI
EXT is a rising edge sensitive internally debounced input and is intended for use with an external push-button switch. A rising transition on this input while the VL82C323 is not in the Suspend or Off Mode will generate an NMI. Software can then save the status and the VL82C323 will enter either the Suspend or Off Mode.

LB NMI and LLB NMI
LB and LLB are active high inputs. The LB and LLB NMIs are masked by the MSK_LB and MSK_LLB bits, (bits 2 and 3) respectively, in the NMIMASK-I Register. If a low battery input is high and the corresponding NMI is unmasked, the PMU will generate an NMI every 15 seconds until it enters either the Suspend or Off Mode. (If the IRQx output is used, this is not the case. IRQx is latched active and remains active until the NMICAUSE-I Register is read.)

GPIO4 and GPIO5/LB1 and LB2 NMIs
When the MSK_GPLBx bits (bits 3 and 4) in the NMIMASK-II Register are unmasked, GPIO4 and GPIO5 can be used as LB1 and LB2 low battery warning inputs, respectively. These are active high inputs and are GPIO input pins at power-on reset.

LCD Timer NMI
If the MSK_LCD bit in the NMIMASK-II Register is cleared, the VL82C323 will generate an NMI when the LCD Timer times out. If the EN_LCDSEQ bit is set, the LCD power will be automatically sequenced off, otherwise the BIOS must turn it off.

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SYSTEM ACTIVITY MONITOR

The System Activity Monitor is used to monitor I/O or video activity. If no activity is detected for a period of time (determined by one of several timers), the VL82C323 can generate an NMI or enter a power saving mode. If activity is detected, the VL82C323 can generate an NMI or enter the On Mode. There are eight system operations treated as a detection of activity and each of these can be masked independently in the ACTMASK Register. A bit will be set in the Activity Register for each unmasked activity that has occurred since the last time the register was read. The Activity Register is cleared when read.

Listed below are the eight different types of unmasked activities that are monitored by the System Activity Monitor and which mask bits they correspond to in the ACTMASK Register. However, the eighth activity listed (External Activity) has no corresponding mask bit.

Parallel I/O Ports	Bit 0 (MSK_PIO) Activity: Any read or write access to LPT1, LPT2, or LPT3. Their address ranges are: LPT1 - 378h to 37Fh LPT2 - 278h to 27Fh LPT3 - 3BCh to 3BFh
Keyboard Ports	Bit 1 (MSK_KBD) Activity: A read of the keyboard port 60h.
RTC Ports	Bit 2 (MSK_RTC) Activity: Any read or write access to the RTC ports 70h and 71h.
Serial Ports	Bit 3 (MSK_SIO) Activity: Any read or write access to the COM1-COM4 ports. Their address ranges are: COM1 is 3F8h to 3FFh COM2 is 2F8h to 2FFh COM3 is 3E8h to 3EFh COM4 is 2E8h to 2EFh
Floppy Disk Port	Bit 4 (MSK_FLP) Activity: A read or write to the floppy disk data port 3F5h.
Hard Disk Port	Bit 5 (MSK_HD) Activity: A read or write to the hard disk port, 1F0h to 1F7h.
Video Memory Writes	Bit 6 (MSK_VIDM) Activity: A high-to-low transition on –VIDCS4 - –VIDCS0. (A low on any of the –VIDCS inputs indicates a memory write is occurring. Typically, one of the –VIDCS inputs is connected to the video memory write signal of the VGA. The unused –VIDCS signals are pulled up with an external resistor or connected to VDDRD of the VL82C323.) Detection of the high-to-low transition is treated as an activity and the VL82C323 will exit from the Doze or Sleep Mode if bit 6 is not masked. If bit 6 is masked, the high-to-low transition causes the –SLOWCLK pin to go high for 8 ms without exiting from the Doze or Sleep Mode, temporarily speeding up the CPU clock.
Programmable I/O	Bit 7 (MSK_IORNG) Activity: A programmable I/O range to the Activity Monitor allows the designer to monitor a non-standard I/O device for activity. This I/O address is specified in the IORNG Register. The I/O range can be 8 or 16 bytes long. The default programmable I/O range is 16 bytes long.
External Activity	No Corresponding Mask Bit A rising edge on the EXTACT pin will be sensed as activity, however, there is no mask bit for this activity nor is it reported in the Activity Register.

OPERATION MODES

The VL82C323 has five operational modes:

- On Mode
- Doze Mode
- Sleep Mode
- Suspend Mode
- Off Mode

Each mode can be entered through a timer time-out or by a detection of activity. They also can be entered any time by writing bit 1 (MODE1, Mode MSB) and bit 0 (MODE0, Mode LSB) of the Status Register.

On Mode

When the VL82C323 is first powered up (from the Off Mode), an –RCRESET is generated and places the VL82C323 into the On Mode. In the On Mode, all power control outputs are controlled by the PWRON Register.

If the VL82C323 is in the Suspend or Off Mode, the On Mode is entered when either the EXT, RI or –RTCIRQ pins go high. Once this occurs, the Doze, BL, and LCD Timers are retriggered.

When in the Doze or Sleep Mode, the On Mode is entered when the Activity Monitor detects activity. The activity will also retrigger the Doze Timer.

If ACPWR is high, the Doze Timer is disabled and causes the hardware power saving features of the VL82C323 to be disabled except for the BL Timer. Unless commanded to change modes, the VL82C323 remains in the On Mode, with its –SLOWCLK output pin high.

Doze Mode

The Doze Mode may only be entered from the On Mode. If the MSK_DOZE bit (bit 0) in the NMIMASK-II Register is set, the Doze Mode is entered when the Activity Monitor has not detected activity within the specified amount of time set by the Doze Timer Register. Any unmasked activity causes an exit from the Doze Mode and into the On Mode. Alternatively, if the MSK_DOZE bit is cleared, the VL82C323 generates an NMI and remains in the On Mode until the BIOS commands it to enter the Doze or some other mode. Any unmasked activity causes an activity NMI. In the Doze Mode, the power control outputs are controlled by the PWRDOZE Register, the –SLOWCLK pin will go low and the SCAMP Controller may slow down the CPU clock. Interrupts, NMIs, or video memory writes temporarily forces the –SLOWCLK output pin high (as described in the section titled "SCAMP Controller and the VL82C107 Interface").

Sleep Mode

If the MSK_SLEEP bit (bit 4) in the NMIMASK-I Register is set, the Sleep Mode is automatically entered from the Doze Mode when the activity monitor has not detected activity within the time

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specified by the Sleep Timer Register. Any unmasked activity causes an exit from the Sleep Mode and into the On Mode. Alternatively, if the MSK_SLEEP bit is cleared, the VL82C323 generates an NMI and remains in the Doze Mode until the CPU commands it to enter the Sleep Mode. Any unmasked activity causes an activity NMI. The –SLOWCLK pin's behavior is the same as when it is in the Doze Mode. The power control outputs are controlled by the PWRSLEEP Register.

Suspend Mode

If software support is provided for the Suspend Mode, the VL82C323 can be programmed to generate an NMI after the Suspend Timer times out, or in response to a low-to-high transition on the EXT input pin when the VL82C323 is not in the Suspend or Off Modes. After saving the system information, the BIOS can place the VL82C323 in the Suspend Mode via the Status Register. The BIOS may halt the CPU but it is not necessary. The BIOS must not read data or instructions from DRAM after issuing the Suspend command. The power control outputs are controlled by the PWRSUSPEND Register.

Refresh Control:

The –RAS and –CAS lines from the SCAMP Controller are bused to the VL82C323. The VL82C323 three-states its outputs connected to these lines during normal operation. There are three programmable options when the Suspend Mode is active.

1. VL82C323 Performs CAS-before-RAS Refresh: When the VL82C323 is commanded to enter the Suspend Mode and PWGOUT is driven low to the SCAMP Controller, the VL82C323 takes over refresh of on-board DRAM. It performs CAS-before-RAS refresh cycles at a rate determined by the SLWREF bit (bit 2) in the Control Register.
2. VL82C323 Enables DRAM's Self-Refresh Mode: When the VL82C323 is commanded to enter the Suspend Mode and PWGGD is driven low to the SCAMP Controller, the VL82C323 performs a 1024 cycle CAS-before-RAS refresh burst to DRAM. Self-Refresh Mode is then activated by holding the –RAS and –CAS lines low.
3. VL82C323 does not Perform Refresh: When the VL82C323 is commanded to enter the Suspend Mode and PWGGD is driven low to the SCAMP Controller, the VL82C323 enters the Suspend Mode and provides the usual leakage control functions but leaves the –RAS and –CAS lines three-stated. Use this mode if the VL82C316 SCAMP II Controller's Suspend Mode refresh option is desired.

Resume From Suspend:

Only activity on the EXT, RI, or –RTCIRQ input pins can cause an exit from the Suspend Mode and place the VL82C323 into the On Mode. The cause of the resume can be examined in the WU0 and WU1 bits (bits 5 and 6) in the Status Register. The BIOS must read the RESUME bit (bit 7) in the Status Register to determine if a cold boot or return from the Suspend Mode has occurred. If the RESUME bit is true, the BIOS restores all information and verifies the data in the main memory and video memory is still valid. The RESUME bit is reset when read.

When a wake-up event occurs, the VL82C323 enters the On Mode and turns VDD on 0.5 to 1.0 seconds later after PWGIN goes high. The digital signals that were three-stated or held low return to their normal levels. After PWGOUT is driven high, the VL82C323 discontinues the on-board DRAM refresh (if Refresh Control options 1 or 2 have been selected) and the SCAMP Controller takes over.

Off Mode

The VL82C323 enters the Off Mode after a falling edge on the PWGIN input or when the CPU writes the code for the Off Mode (FFh) to the Status Register. The Auto Power Off Timer described in the "Timers" section also causes the VL82C323 to enter the Off Mode.

The Off Mode is meaningful only when the VL82C323 is powered from a battery while the rest of the system is turned off. This type of connection is necessary only if the VL82C323 must wake-up the system from the Off Mode by activating the VP outputs in response to transitions on the EXT, RI or –RTCIRQ inputs. If this function is not implemented, the VL82C323 may be powered off along with the system power, as with a switch, and the Off Mode does not exist.

In the Off Mode, all devices except battery backed up devices in the computer are powered off. Only –RCRESET or activity on the EXT, RI, or –RTCIRQ inputs can cause an exit from the Off Mode and place it into the On Mode. When powered up from the Off Mode, burst refresh is not activated and if –RCRESET was not asserted, the contents of the VL82C323's internal registers are not changed after waking up from the Off Mode.

TIMERS

There are ten timers in the VL82C323. Some timers are associated with the activity monitors controlling mode transitions. Detailed description of the timers follows.

Doze Timer

The Doze Timer is programmable from 1/8 to 1 second with a resolution of 1/8 of a second, and from 2 to 14 seconds with a resolution of 2 seconds. Setting a zero value to the Doze Timer disables it and setting any non-zero value enables it. Any activity detected by the Activity Monitor retriggers the Doze Timer. The default value for the Doze Timer is 4 seconds.

Sleep Timer

The Sleep Timer is programmable from 1 to 15 minutes with a resolution of 1 minutes. Setting a zero value to the Sleep Timer disables it and setting any non-zero value enables it. Any activity detected by the Activity Monitor retriggers the Sleep Timer. The Sleep Timer is triggered when the Doze Mode is entered and is cleared when the Doze Mode is exited. The default value for the Sleep Timer is 2 minutes.

Suspend Timer

The Suspend Timer is programmable from 5 to 75 minutes with a resolution of 5 minutes. Setting a zero value to the Suspend Timer disables it and setting any non-zero value enables it. Any activity detected by the Activity Monitor retriggers the Suspend Timer. The Suspend Timer is triggered when the Sleep Mode is entered and is cleared when the Sleep Mode is exited. The default of the MSK_SUSPEND bit (bit 5) in the NMIMASK-I Register is

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masked so it disables the Suspend Timer. The default value for the Suspend Timer is 5 minutes.

Backlight (BL) Timer
The BL Timer is programmable from 1 to 15 minutes with a resolution of 2 minutes. Setting a zero value to the BL Timer disables it and setting any non-zero value enables it. The BL Timer is always enabled and is retriggered when the Activity Monitor detects any keyboard activity. The default value for the BL Timer is 2 minutes.

LCD Timer
The LCD Timer is programmable from 1 to 15 minutes with a resolution of 1 minutes. Setting a zero value to the LCD Timer disables it and setting a non-zero value enables it. It is disabled if ACPWR is true and is triggered when the VL82C323 goes from the Off or Suspend Modes to the On Mode, and when keyboard activity occurs or when the –VIDCS inputs are asserted. The default value for the LCD Timer is 2 minutes.

Suspend Reschedule Timer
The Suspend Reschedule Timer is fixed at 60 ms. While the MSK_RESCH bit in the NMIMASK-II Register is cleared, the VL82C323 generates a Suspend Reschedule NMI every 60 ms. The Suspend Reschedule Timer can be retriggered by momentarily setting and clearing the MSK_RESCH bit (bit 2) in the NMIMASK-II Register. This feature can be used to generate reliable tick interrupts for the power management software if the System Clock Timer has been reprogrammed by the application or OS software. The Suspend Reschedule Timer is retriggered at each INT8, it never times out, but if other software takes over the System Clock Timer, it times out and repeatedly generates an NMI until masked.

Auto Power Off Timer
If an LLB NMI is unmasked and is not serviced within three minutes while LLB remains continuously true, the VL82C323 automatically enters the Off Mode.

VIDCS Timer
A fixed 8 ms timer is provided for the video memory write operations. If the MSK_VIDM bit (bit 6) in the ACTMASK Register is set, any low transitions on the –VIDCS inputs are not treated as an activity detection. The VL82C323 temporarily brings the –SLOWCLK pin high for 8 ms without exiting from the Doze or Sleep Modes. If the MSK_VIDM bit is cleared, the VIDCS Timer is disabled. Default is disabled.

Low Battery Timer
The Low Battery (LB) Timer is enabled in the On, Doze, and Sleep Modes. The LB Timer is fixed to 15 seconds. An NMI is generated by the LB Timer every 15 seconds until a timer period elapses during which all low battery inputs are continuously false. This is also true for LLB, LB1 (GPIO4), and LB2 (GPIO5).

Power-On Fault Timer
If PWGIN fails to go high within 1 to 2 seconds after a wake-up, the VL82C323 returns to the previous mode (either the Off or Suspend Mode).

Time Register
The Time Register is read-only register. It contains the value of a counter that counts cycles of the 32 kHz clock whenever it is running. Unlike the System Clock Timer, it can not be altered by the application software and can provide a reliable relative time reference for the power management software. It is cleared when –RCRESET is active.

POWER-ON
There are three power-on inputs to the VL82C323:
- –RTCIRQ
- RI
- EXT

These inputs can bring the VL82C323 out of the Suspend or Off Modes and into the On Mode. Since these inputs control the power on/off for the system, care must be taken to ensure these inputs never float. To ensure these inputs are always driven, tie any unused inputs low.

Real Time Clock Power-On
–RTCIRQ is an edge sensitive input, intended for use with the real-time clock's wake-up alarm from the VL82C107 SCAMP Combination I/O chip. Any transition on this input forces the VL82C323 into the On Mode. The VL82C323 generates an –IRQ8 output to the VL82C310 SCAMP I Controller to prevent leakage while in the Suspend Mode.

Note: The above discussion only applies when using the VL82C323 in a VL82C310/ VL82C107-based system. The RTC is built into the VL82C316. In systems using the VL82C316, the VL82C323's –IRQ8 output signal is not connected to the VL82C316 and leakage control of this signal is not an issue. However, the –RTCIRQ output of the VL82C316 is connected to the VL82C323's –RTCIRQ input to support the time of day wake-up feature.

Ring Indicator Power-On
RI is a rising edge sensitive input, intended for use with a modem ring indicator output. The number of rising edges required for this input to be recognized is specified in bits D6-D4 (RING2-RING0) of the Control Register. The default is one transition. If these bits are zero, the RI input is disabled. If enabled, the programmed number of edges forces the VL82C323 into the On Mode.

External Switch Power-On
EXT is a rising edge sensitive input, intended for use with an external source. A rising transition on this input while the VL82C323 is in either the Off or Suspend Mode forces it into the On Mode. A transition in the On, Doze, or Sleep Modes generates an NMI.

EXT is internally debounced. A rising edge immediately generates an NMI if EXT has been sampled low at least twice by a 32 Hz debounce clock prior to the rising edge. The VL82C323 does not respond to any activity on any other wake-up input until after the EXT input has been sampled low twice by the debounce clock.

LEAKAGE CONTROL DURING SUSPEND AND OFF MODES
Leakage control is active during the Suspend and Off Modes in order to provide absolute minimal current consumption. However, there is a set of signals for which the system designer must externally control leakage either because they must remain functional during the Off Mode or to prevent the design of the VL82C323 from placing restrictions on the user's circuits.

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These signals are:
LB, LLB, RI, EXT, –RTCIRQ, ACPWR, PWGIN, –RCRESET, RTCXOUT, RTCXIN and GPIO9-GPIO0.

GPIO
The VL82C323 has ten general purpose pins that may be individually programmed as inputs or outputs. Some can be programmed as blinking outputs, low battery inputs, or AND/OR inputs or output. They default to general purpose inputs at power-on. If not used, they must be tied low to prevent leakage. Alternatively, they may be programmed as outputs to prevent leakage. For example, these could be used for monitoring the power supply status, EEPROM interface, or as software controlled VP outputs.

Blinking Option
The GPIO3 pin can be used as a programmable audio and/or blinking generator. The blinking option is enabled by setting the EN_BLK bit (bit 0) in the Blinking Register. Default is reset. The blink generator produces an audible output frequency which blinks on and off. The frequency, blink rate, and number of blinks are also programmed by the Blinking Register. When used to drive a LED rather than a speaker, the use of audio frequencies results in an LED that flashes at the blink rate but is unaffected by the audio frequency. This feature might be useful to drive an LED indicator, speaker, or both in response to a low battery indication or as an indicator that the Suspend Mode is active, for example.

Low Battery Option
The GPIO4 and GPIO5 pins may be used as an optional low battery warning inputs. Please refer to the section titled "GPIO4 and GPIO5/LB1 and LB2 NMI" for a detailed description.

TABLE 1. REGISTER DESCRIPTIONS

Register	Index	Register	Index
STATUS	C0h	LCD	CFh
SUPPLY	C1h	BL	D0h
CONTROL	C2h	NMIMASK-II	D1h
ACTMASK	C3h	NMICAUSE-I	D2h
NMIMASK-I	C4h	NMICAUSE-II	D3h
IORNG	C5h	MISCSET	D4h
PWRON	C6h	REVID	D5h
PWRDOZE	C7h	BLINKING	D6h
PWRSLEEP	C8h	GPDIR	D7h
PWRSUSPEND	C9h	GPEN	D8h
POLARITY	CAh	ANDOR	D9h
OUTPUT	CBh	Reserved	DAh
DOZE	CCh	ACTIVITY	DBh
SLEEP	CDh	TIME	DCh
SUSPEND	CEh		

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TABLE 2. STATUS REGISTER (C0h)

Bit	Name	Function
D7	RESUME	Resuming from Suspend (Warm Start)
D6	WU1	Wake-up Code MSB
D5	WU0	Wake-up Code LSB
D4	NMI2	NMI Cause Code
D3	NMI1	NMI Cause Code
D2	NMI0	NMI Cause Code
D1	MODE1	Mode MSB
D0	MODE0	Mode LSB

–RCRESET clears all bits. D4-D2 are cleared when the NMICAUSE-I Register is read. D7 is cleared after the Status Register is read.

Only D0 and D1 are affected by a write. The CPU can write the mode code to this register to put the VL82C323 into another mode. Writing 0FFh puts it in the Off Mode. The NMI cause, mode, and wake-up codes are decoded in Table 3.

TABLE 3. NMI CAUSE, MODE, AND WAKE-UP CODES

NMI		Mode		Wake-up	
Code	Cause	Code	Cause	Code	Cause
000	None or INMI	00	On	00	
001	EXT Input	01	Doze	01	EXT Input
010	LB	10	Sleep	10	–RTCIRQ Input
011	LLB Time-out	11	Suspend	11	RI Input
100	Sleep Time-out				
101	Suspend Time-out				
110	Sleep to On (Activity)				

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SUPPLY REGISTER (C1h)
This register has different functions for read and write. This GPIO2-GPIO0 pins are programmed as inputs or outputs by D2-D0 and are read and written on D6-D4. For read operations, D7-D4, D1, and D2 are driven directly by the input pins. D3 is set when system activity is detected and is cleared when the Supply Register is read.

TABLE 4. SUPPLY REGISTER - READ

Bit	Name	Function
D7	ACPWR	
D6	GPIN2	General Purpose Input
D5	GPIN1	
D4	GPIN0	
D3	ACTIVITY	System Activity Present
D2	LLB	Low Battery 2 (Second Warning)
D1	LB	Low Battery 1 (First Warning)
D0	LOCKOUT	PMU Registers Write-Protected

TABLE 5. SUPPLY REGISTER - WRITE

Bit	Name	Default	Function
D7	Reserved	0	
D6	GPOUT2	0	General Purpose Output
D5	GPOUT1	0	
D4	GPOUT0	0	
D3	Reserved	0	
D2	GPDIR2	0	General Purpose I/O Direction Control
D1	GPDIR1	0	
D0	GPDIR0	0	

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TABLE 6. CONTROL REGISTER (C2h)

Bit	Name	Default	Function
D7	Reserved	0	
D6	RING2	0	RI Pulse Required for Turn-on
D5	RING1	0	
D4	RING0	1	
D3	Reserved	0	
D2	SLWREF	0	1 = Slow Refresh DRAM
D1	SUSPREF1	0	00 = CAS-before-RAS 01 = Self-Refresh 1X = Refresh Inactive
D0	SUSPREF0	0	

The RING2-RING0 bits are used to set the number of RI pulses required for turn-on. The default value of RING0 is 1 so that only one pulse is required for turn-on. If set to 0, RI is disabled.

TABLE 7. ACTMASK REGISTER (C3h)

Bit	Name	Default	Function
D7	MSK_IORNG	1	Mask Access to 16 Ports at IORNG5-IORNG0
D6	MSK_VIDM	0	Mask Access to Video Memory
D5	MSK_HD	0	Mask Hard Disk Activity
D4	MSK_FLP	0	Mask Access to Port 3F5
D3	MSK_SIO	0	Mask Access to COM1-COM4
D2	MSK_RTC	1	Mask Access to Port 70h, 71h
D1	MSK_KBD	0	Mask Keyboard Access to Port 60h Reads
D0	MSK_PIO	0	Mask Access to LPT1-LPT3

The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources. This register affects only the ACTIVITY output.

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TABLE 8. NMIMASK-I REGISTER (C4h)

Bit	Name	Default	Function
D7	MSK_IRQx	1	Mask IRQx Output
D6	MSK_NMI	0	Mask NMI Output
D5	MSK_SUSPEND	1	Mask Suspend Time-out
D4	MSK_SLEEP	1	Mask Sleep Time-out
D3	MSK_LLB	1	Mask LLB Input
D2	MSK_LB	1	Mask LB Input
D1	MSK_EXT	1	Mask EXT Input
D0	Reserved	0	

The register masks the various NMI sources. In the Default Mode, only the INMI input can generate NMI.

TABLE 9. IORNG REGISTER (C5h)

Bit	Name	Default	Function
D7	RNGSIZE	0	1 = 8 Bytes, 0 = 16 Bytes
D6	IORNG6	0	Maskable I/O Range Base Address
D5	IORNG5	0	
D4	IORNG4	0	
D3	IORNG3	0	
D2	IORNG2	0	
D1	IORNG1	0	
D0	IORNG0	0	

IORNG6-IORNG0 are the base address bits SA9-SA3 for the maskable I/O port range in the activity monitor. RNGSIZE is the size of the range. IORNG0 is ignored when RNGSIZE is low.

POWER REGISTERS (C6-C9h)
The bits in the Power Registers, D7-D0, correspond directly with the power control outputs VP7-VP0. In a particular mode, the corresponding PWR Register's outputs control the VP pins. The exception is VP0 and VP1 which are the LCD and BL power, respectively. These outputs are ANDed with the LCD and BL Timer outputs prior to driving the pins. All bits are then exclusive NORed with the Polarity Register and the result drives the pins. VPBIAS, –VPVSIG, and VP0 are controlled as described in the "Automatic LCD Power Sequencing" section. The default values for these registers are as shown in Table 10, where 1 indicates that the controlled device is on.

POLARITY REGISTER (CAh)
The Polarity Register controls the polarity of the VP outputs. If a logic low is required on any of the VP7-VP0 pins to turn the external device on, the corresponding bit in the Polarity Register must be low. If a high is required, set the bit high. The default value is 0FFh. The polarity of VPBIAS is the same as VP0. –VPVSIG is always low true.

OUTPUT REGISTER (CBh)
The Output Register is a read-only register. For each VP7-VP0 output that is on, the corresponding bit in the Output Register will be set.

TIMER REGISTERS (CC-D0h)
Loading a value into a Timer Register enables the timer and selects the time-out. All Timer Registers have four significant bits (bits 3-0). Data written to the upper bits has no effect. The upper bits are 0 when read back. Except for the Doze Timer, all Timer Registers can be set for a time-out from 1 to 15 time units, where a unit is the resolution of the timer. A zero disables the timer. Reading a Timer Register returns the value that was last written to it, not the actual time remaining. The default values are tabulated in Tables 11 and 12.

TABLE 10. POWER REGISTERS (C6-C9h)

Register	Default	Index
PWRON	FEh	C6h
PWRDOZE	FEh	C7h
PWRSLEEP	FCh	C8h
PWRSUSPEND	00h	C9h

TABLE 11. TIMER REGISTERS (CC-D0h)

Timer	Range	Default	Index
Doze	1/8-14 sec	4 sec	CCh
Sleep	1-15 min	2 min	CDh
Suspend	5-75 min	0 (disabled)	CEh
LCD	1-15 min	2 min	CFh
BL	1-15 min	2 min	D0h

TABLE 12. DOZE TIMER PROGRAMMING

D3-D0	Time	D3-D0	Time
0000	Disabled	1000	1 sec
0001	1/8 sec	1001	2 sec
0010	1/4 sec	1010	4 sec
0011	3/8 sec	1011	6 sec
0100	1/2 sec	1100	8 sec
0101	5/8 sec	1101	10 sec
0110	3/4 sec	1110	12 sec
0111	7/8 sec	1111	14 sec

TABLE 13. NMIMASK-II REGISTER (D1h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	MSK_GPLB2	1	Mask off the LB2 NMI option from GPIO5. 1 = Mask. When this bit is low, the GPIO5 is used as LB2 input.
D3	MSK_GPLB1	1	Mask off the LB1 NMI option from GPIO4. 1 = Mask. When this bit is low, the GPIO4 is used as LB1 input.
D2	MSK_RESCH	1	Mask off the Suspend reschedule NMI. 1 = Mask.
D1	MSK_LCD	1	Mask off the NMI caused by the LCD Timer time-out. 1 = Mask.
D0	MSK_DOZE	1	Mask off the NMI caused by the Doze Timer time-out. 1 = Mask.

TABLE 14. NMICAUSE-I REGISTER (D2h)

Bit	Name	Default	Function
D7	ACT_LCD_NMI	0	LCD Timer Retrigger Activity
D6	ACT_NMI	0	Activity NMI from Doze or Sleep
D5	SUSPEND_NMI	0	Suspend NMI
D4	SLEEP_NMI	0	Sleep NMI
D3	LLB_NMI	0	LLB NMI
D2	LB_NMI	0	LB NMI
D1	EXT_NMI	0	EXT Input NMI
D0	I_NMI	0	PC/AT-compatible specified NMI generated by the SCAMP Controller.

The NMI cause can also be examined by reading the Status Register. Additional NMICAUSE Registers are provided to give more flexibility of using the VL82C323. Reading the NMICAUSE-I Register clears the NMICAUSE-I Register and the NMI cause codes in the Status Register. It also clears the IRQx output, if it is unmasked. The NMICAUSE-I Register is cleared at the trailing edge of the –IOR signal. A double buffer method is used to prevent loss of the NMI while it is cleared. Writing any data to it indicates the end of a VL82C323 NMI service routine but does not change the contents of the register.

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TABLE 15. NMICAUSE-II REGISTER (D3h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	GPLB2_NMI	0	GPLB2 NMI
D3	GPLB1_NMI	0	GPLB1 NMI
D2	RESCH_NMI	0	Rescheduled NMI
D1	LCD_NMI	0	LCD NMI
D0	DOZE_NMI	0	Doze NMI

The NMICAUSE-II Register is cleared by reading it. It is a read-only register.

TABLE 16. MISCSET REGISTER (D4h)

Bit	Name	Default	Function
D7	FASTDB	0	Low battery NMI debouce time. Low = 2-4 seconds and high = 30-60 ms.
D6	AUTOFLUSH	0	When set, it allows automatic stack flush when entering the On Mode.
D5	FLUSH	0	When set, it flushes and inhibits the INTR stack.
D4	EN_LCDSEQ	0	When the EN_LCDSEQ bit is set, the VL82C323 performs the LCD power-up/down sequencing.
D3	LCDTMG1	0	LCDTMG0 and LCDTMG1 are used to select the LCD power-up/down sequencing if the EN_LCDSEQ bit is set. If the EN_LCDSEQ is not set, LCDTMG0 controls –VPVSIG and LCDTMG1 controls the VPBIAS outputs individually.
D2	LCDTMG0	0	**1 0 Delay** 0 0 8 ms 0 1 15 ms 1 0 31 ms 1 1 125 ms
D1	ALT_INT	0	Enable –SMI generation and disable NMI and IRQx outputs.
D0	EN_HICLK	0	When high, forces –SLOWCLK pin to go high in the Doze or Sleep Mode.

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TABLE 17. REVID REGISTER (D5h)

Bit	Name	Default	Function
D7	ID3	0	Used for the ID number of the VL82C323.
D6	ID2	0	
D5	ID1	0	
D4	ID0	0	
D3	Reserved	0	
D2	REV2	0	Used for revision number of the VL82C323.
D1	REV1	0	
D0	REV0	0	

TABLE 18. BLINKING REGISTER (D6h)

Bit	Name	Default	Function
D7	Reserved		
D6	BLKPERD1	0	**1 0 Period** 0 0 1 Hz 0 1 2 Hz 1 0 4 Hz 1 1 8 Hz
D5	BLKPERD0	0	
D4	BLKNBR1	0	**1 0 Number** 0 0 1 0 1 2 1 0 4 1 1 Continuous
D3	BLKNBR0	0	
D2	BLKFRQ1	0	**1 0 Frequency** 0 0 512 Hz 0 1 1024 Hz 1 0 1365 Hz 1 1 2048 Hz
D1	BLKFRQ0	0	
D0	EN_BLK	0	Used to enable the blinking option of the GPIO3. 1 = enable.

EXAMPLE OF BLINKING REGISTER

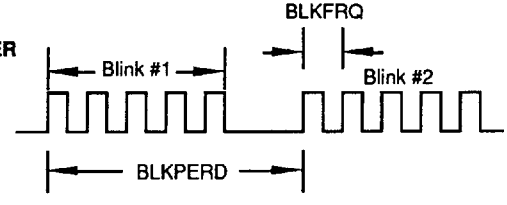


TABLE 19. GPDIR REGISTER (D7h)

Bit	Name	Default	Function
D7	Reserved		
D6	GPDIR9	0	GPDIR9-GPDI3 are used as general purpose I/O pins. The direction of GPIO can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D5	GPDIR8	0	
D4	GPDIR7	0	
D3	GPDIR6	0	
D2	GPDIR5	0	
D1	GPDIR4	0	
D0	GPDIR3	0	

GPDATA REGISTER (D8h)
This register has different functions for read and write.

TABLE 20. GPDATA REGISTER - READ

Bit	Name	Default	Function
D7	Reserved		
D6	GPIN9	0	If the corresponding bit in the GPDIR Register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D5	GPIN8	0	
D4	GPIN7	0	
D3	GPIN6	0	
D2	GPIN5	0	
D1	GPIN4	0	
D0	GPIN3	0	

TABLE 21. GPDATA REGISTER - WRITE

Bit	Name	Default	Function
D7	Reserved		
D6	GPOUT9	0	If the corresponding bit in the GPDIR Register is to output, the value of the GPIO pin can be set by this register.
D5	GPOUT8	0	
D4	GPOUT7	0	
D3	GPOUT6	0	
D2	GPOUT5	0	
D1	GPOUT4	0	
D0	GPOUT3	0	

TABLE 22. ANDOR REGISTER (D9h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	Reserved		
D3	SEL_POL	1	If set, GPIO9 is the output of the AND/OR function. If cleared, GPIO9 is the output of the NAND/NOR function.
D2	SEL_AND	0	If EN_ANDOR is enabled, SEL_AND = 1 selects the AND function and SEL_AND = 0 selects the OR function.
D1	EN_AO8	0	Enable the AND/OR function for the GPIO8. When this bit and the EN_ANDOR bit are both set, GPIO8 becomes an input of the AND/OR function.
D0	EN_ANDOR	0	Enables the AND/OR function for GPIO9, GPIO7, and GPIO6. When set, GPIO7 and GPIO6 become the inputs of the AND/OR function and GPIO9 becomes the output.

TABLE 23. ACTIVITY REGISTER (DBh)

Bit	Name	Default	Function
D7	IORNG	0	I/O Range Activity
D6	VIDM	0	Video Memory Activity
D5	HD	0	Hard Disk Activity
D4	FLP	0	Floppy Disk Activity
D3	SIO	0	COM Port Activity
D2	RTC	0	Real-time Clock Access
D1	KBD	0	Keyboard Port 60h Read Activity
D0	PIO	0	LPT1-LPT3 Activity

TABLE 24. TIME REGISTER (DCh)

Bit	Significance
D7	1 s
D6	500 ms
D5	250 ms
D4	125 ms
D3	62.5 ms
D2	31.25 ms
D1	15.625 ms
D0	7.8125 ms

The Time Register contains the relative time in units of 1/128 second. It is a read-only register and is cleared only by –RCRESET.

FIGURE 3. POWER MANAGEMENT MODE FLOW

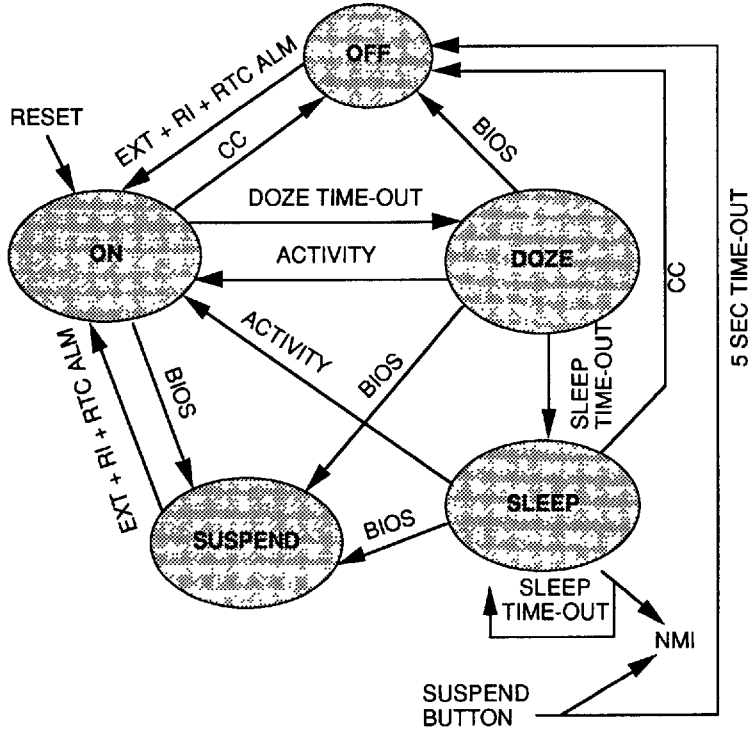


FIGURE 4. VL82C316 SCAMP II 5 VOLT CONTROLLER NOTEBOOK SYSTEM BLOCK DIAGRAM IN SMM SYSTEMS

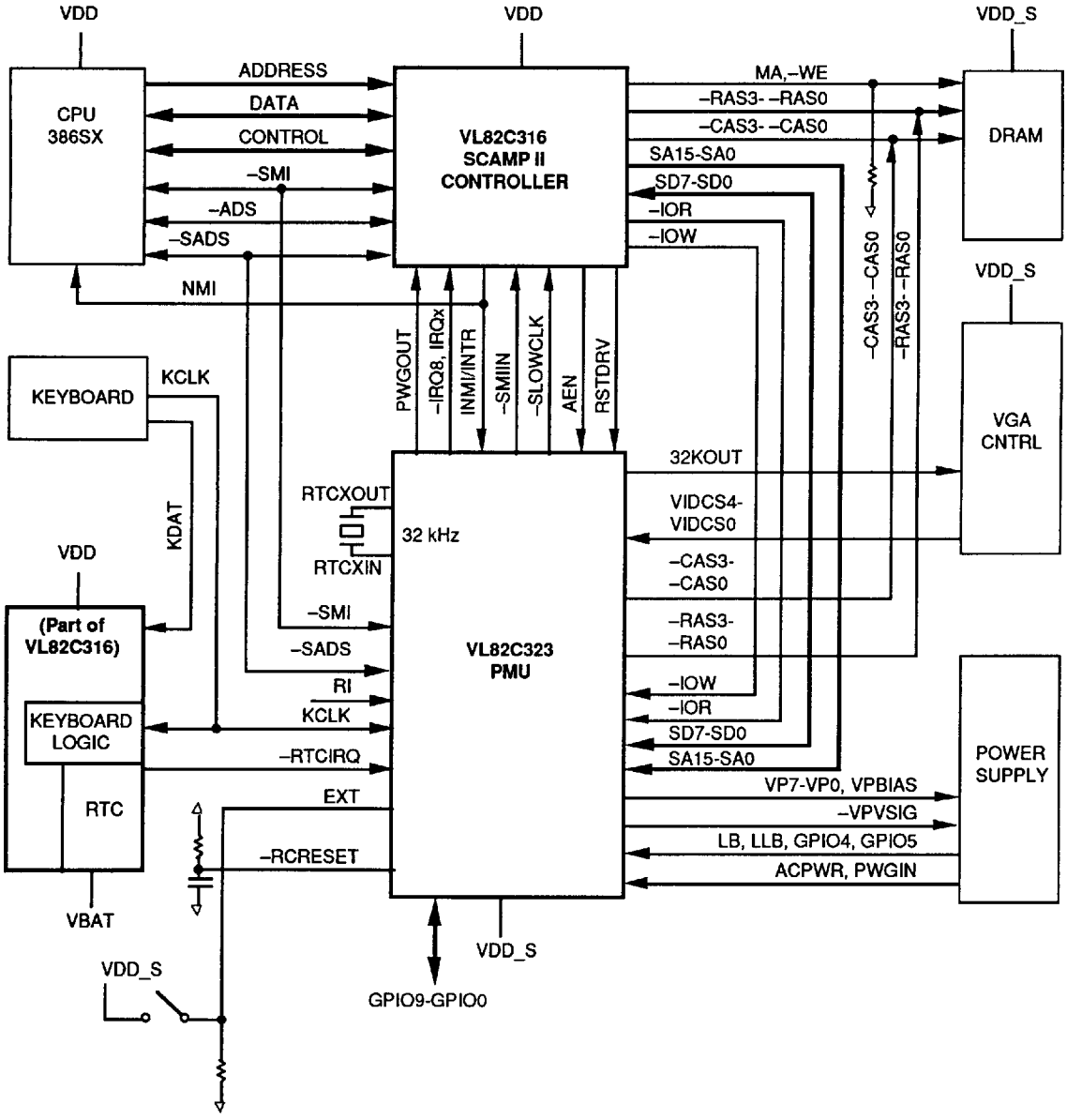
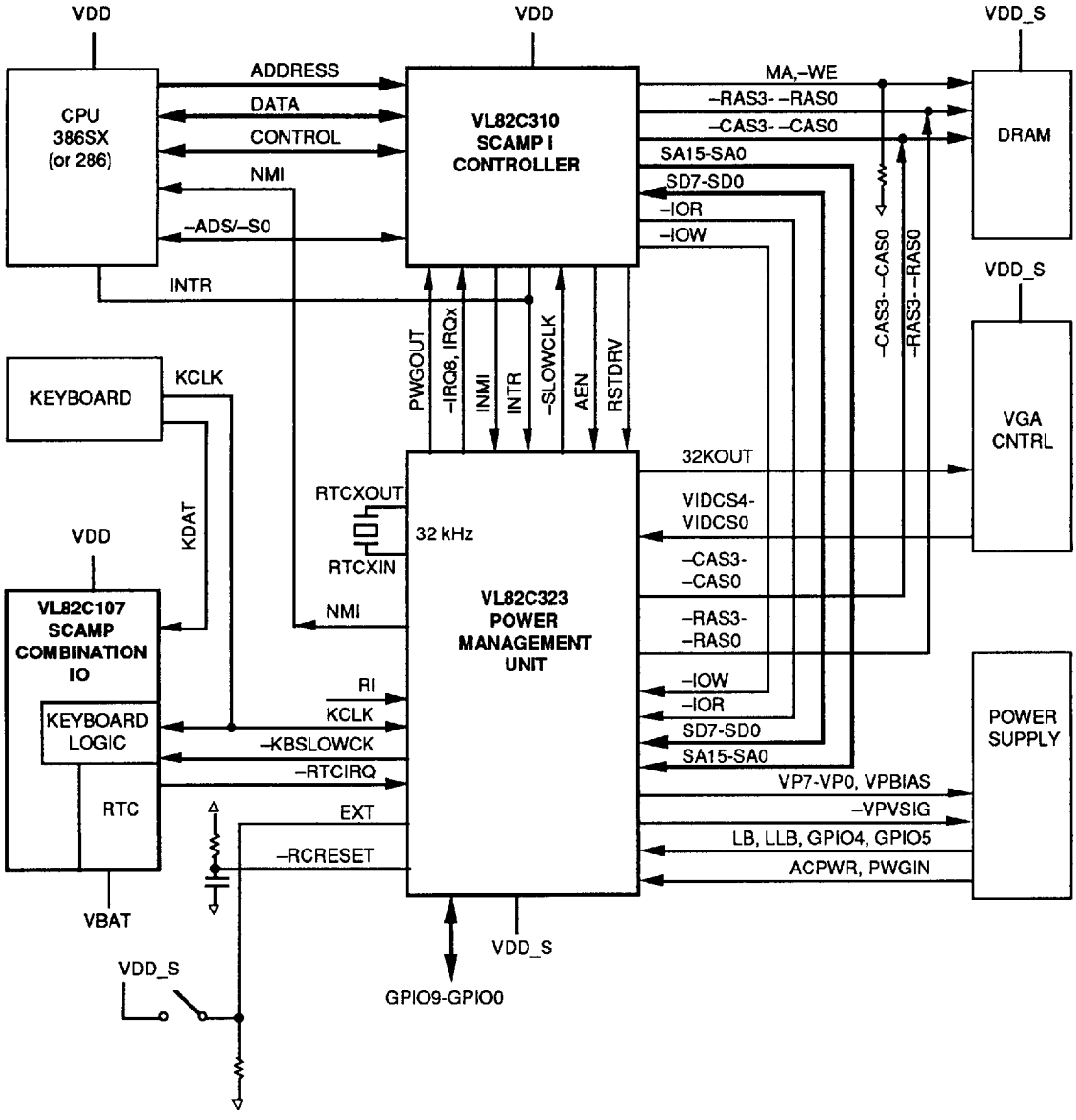


FIGURE 5. VL82C310 SCAMP I NOTEBOOK SYSTEM BLOCK DIAGRAM



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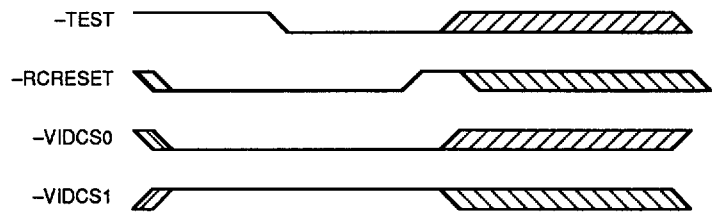
IN-CIRCUIT TEST MODE

During In-Circuit Test (ICT) Mode each output may be toggled by one or more of the inputs. This allows a board level tester to check the solder connection of each pin.

Table 25 shows the input to output mapping for each pin while the ICT Mode is active. The "Pin Name" column shows the first of the two signals in an I/O mapping pair. As an example, pin 3 (–VIDCS1), is used as an input while VP0 is used as the output.

The sequence for enabling ICT Mode:



To clear ICT Mode, –IOW and –IOR must be low and ACPWR high.

TABLE 25. PIN ASSIGNMENT FOR IN-CIRCUIT TEST

Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection	Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection
1	VGARST	Out	From	–VIDCS0	24	PWGIN	In	To	VP3
2	–VIDCS0	In	To	VGARST	25	EXTACT	In	To	GPIO5
3	–VIDCS1	In	To	VP0	26	VSSR			
4	–VIDCS2	In	To	–VPVSIG	27	EXT	In	To	U34*
5	–VIDCS3	In	To	VP1	28	RI	In	To	U34*
6	–VIDCS4	In	To	VPBIAS	29	–IRQ8	Out	From	AEN
7	–VPVSIG	Out	From	–VIDCS2	30	IRQx	Out	From	AEN
8	VPBIAS	Out	From	–VIDCS4	31	AEN	In	To	IRQX
9	VP0	Out	From	–VIDCS1	32	–IOR	In	To	U34*
10	VP1	Out	From	–VIDCS3	33	–IOW	In	To	U34*
11	VDDRD				34	VDDRA			
12	VP2	Out	From	LLB	35	SD0	In	To	U34*
13	VP3	Out	From	PWGIN	36	SD1	In	To	
14	VSSR				37	VSSI			
15	VP4	Out	From	LB	38	SD2	In	To	U34*
16	VP5	Out	From	ACPWR	39	SD3	In	To	U34*
17	VP6	Out	From	LB	40	SD4	In	To	U34*
18	VP7	Out	From	ACPWR	41	SD5	In	To	U34*
19	GPIO4	Out	From	U34*	42	SD6	In	To	U34*
20	GPIO5	Out	From	EXTACT	43	SD7	In	To	U34*
21	LB	In	To	VP4/VP6	44	VSSR			
22	LLB	In	To	VP2	45	RSTDRV	In	To	U34*
23	ACPWR	In	To	VP5/VP7	46	SA0	In	To	U34*

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TABLE 25. PIN ASSIGNMENT FOR IN-CIRCUIT TEST (Cont.)

Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection	Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection
47	SA1	In	To	U34*	74	INMI	In	To	U34*
48	SA2	In	To	U34*	75	INTR	In	To	NMI/–SMIOUT
49	SA3	In	To	U34*	76	VDDRB			
50	SA4	In	To	U34*	77	–SADS	In	To	U34*
51	SA5	In	To	U34*	78	–ADS/–S0	Out	To	–SLOWCLK
52	SA6	In	To	U34*	79	–SLOWCLK	Out	To	–ADS
53	SA7	In	To	U34*	80	–KBSLOWCK	Out	To	–RTCIRQ
54	SA8	In	To	U34*	81	–RTCIRQ	In	To	–KBSLOWCK
55	SA9	In	To	U34*	82	PWGOUT	Out	From	–RTCIRQ
56	VDDRA				83	–RCRESET	In	To	U34*
57	SA10	In	To	U34*	84	VDDRC			
58	SA11	In	To	U34*	85	RTCXOUT			
59	SA12	In	To	U34*	86	RTCXIN			
60	SA13	In	To	U34*	87	VSSR			
61	SA14	In	To	U34*	88	–TEST	In	To	PWGOUT
62	SA15	In	To	U34*	89	KCLK	In	To	U34*
63	–RAS0	Out	From	SA15	90	VDDI			
64	–RAS1	Out	From	SA14	91	GPIO9	In	To	U34*
65	–RAS2	Out	From	SA13	92	GPIO8	In	To	U34*
66	VSSR				93	GPIO7	In	To	U34*
67	–RAS3	Out	From	SA12	94	GPIO6	In	To	U34*
68	–CAS0	Out	From	SA11	95	GPIO0	In	To	U34*
69	–CAS1	Out	From	SA10	96	GPIO1	In	To	U34*
70	–CAS2	Out	From	–CAS3	97	VDDRD			
71	–CAS3	In	To	–CAS2	98	GPIO2	In	To	U34*
72	–SMIIN	In	To	U34*	99	GPIO3	In	To	U34*
73	NMI/–SMIOUT	Out	From	INTR	100	32KOUT	Out	From	U34*

Notes: * U34 signals are tested differently. U34 is a large NAND gate and all signals listed at "To" are inputs to the NAND gate. The two signals listed as "From" are connected to the output of the NAND gate.

–IOR –> –IOW –> SA5 –> SA6 –> SA7 –> SA8 –> SA9 –>
–> SD0 –> SD1 –> SD2 –> SD3 –> SD4 –> SD5 –> SD6 –> SD7 –>
–> GPIO0 –> GPIO1 –> GPIO2 –> GPIO3 –> GPIO6 –> GPIO7 –> GPIO8 –> GPIO9 –>
–> SA0 –> SA1 –> SA2 –> SA3 –> SA4 –> RSTDRV –> –SADS –> KCLK –> INMI –>
–> EXT –> RI –> –SMIIN –> –RCRESET –>>>> To I/O Pads GPIO4/32KOUT

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write Timings					
tSU1	Address Setup Time	55		ns	
tH2	Address Hold Time	20		ns	
tSU3	AEN Setup Time	55		ns	
tH4	AEN Hold Time	20		ns	
tPW5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL = 200 pF
tH9	Read Data Hold	5	50	ns	CL = 50 pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
VL82C323 Pin Timing					
t10	–RAS Precharge Time (Burst Refresh)	125		ns	
t11	–RAS On Time (Burst Refresh)	250		ns	
tD12	Burst Refresh to Suspend Refresh Delay	15	31	µs	
t13	–RAS On Time Suspend Mode Refresh	170	610	ns	
t14	Suspend Refresh Cycle Time (Std. Ref.)	15		µs	
t15	Suspend Refresh Cycle Time (Slow Ref.)	124		µs	
tD16	PWGIN to PWGOUT Delay from –RCRESET	0.53	1.035	s	
tD17	–RCRESET to PWGOUT Delay	0.53	1.035	s	
tD18	–RCRESET to VP7-VP2 Delay	0	40	ns	

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AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
VL82C323 Pin Timing (Cont.)					
tD19	PWGOUT to VP1 Delay from –RCRESET				0.5 sec Typical
tD20	EXT to VP7-VP2 Delay	0	40	ns	
tD21	PWGIN to PWGOUT Delay from EXT	0.53	1.03	s	
tD22	PWGOUT to VP1 Delay from EXT				0.5 sec Typical
tD23	INMI to NMI Delay	0	40	ns	
tPW24	EXT Pulse Width Low	63		ms	
t25	–SLOWCLK or –KBSLOWCK Low	288		ns	
t26	–SLOWCLK or –KBSLOWCK High	288		ns	
tPW27	EXTACT Pulse Width High	60		ns	
tD28	Resume Command to PMU Refresh Burst Delay	0.53	1.03	s	
tD29	Suspend Command to Suspend Active Delay	0.53	1.03	s	
t30	PWGOUT Low to PMU Driving –CAS Low	560		ns	
t31	–CAS Low to Start of 1024 Refresh Burst	150		ns	
tPW32	NMI Pulse Width High	570		ns	
t33	–SADS to –NMI/–SMIOUT		40	ns	

FIGURE 6. WRITE CYCLE TIMING

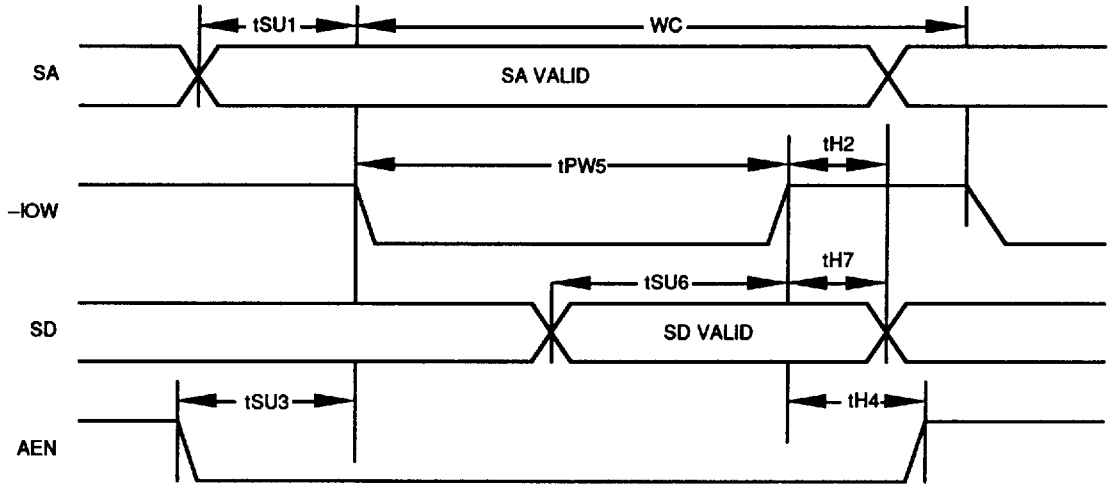

FIGURE 7. READ CYCLE TIMING

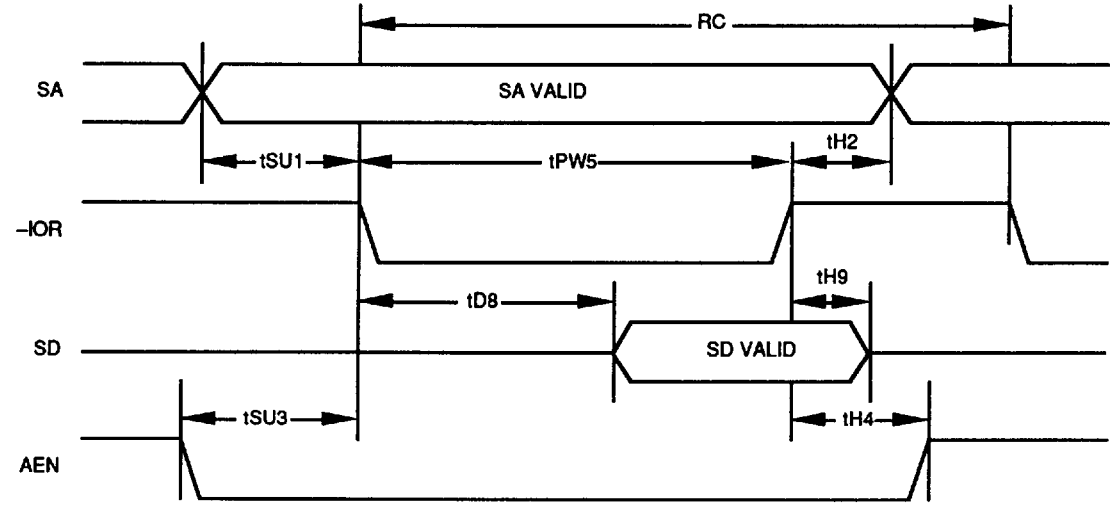

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FIGURE 8. –RAS TIMING: ENTERING SUSPEND MODE WITH PMU DRIVEN REFRESH
(See Figure 23 for more system details)

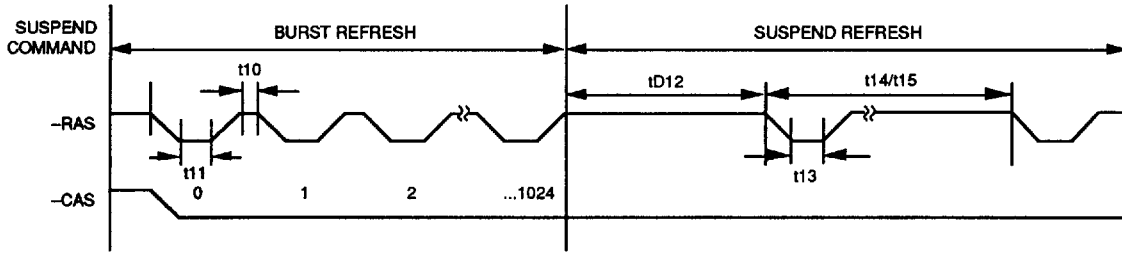


FIGURE 9. –RAS TIMING: LEAVING SUSPEND MODE WITH PMU DRIVEN REFRESH
(See Figure 23 for more system details)

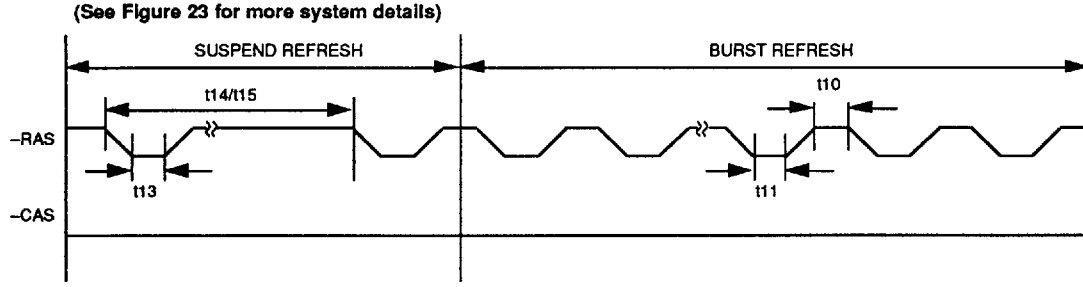


FIGURE 10.–RAS TIMING: ENTERING SELF-REFRESH MODE

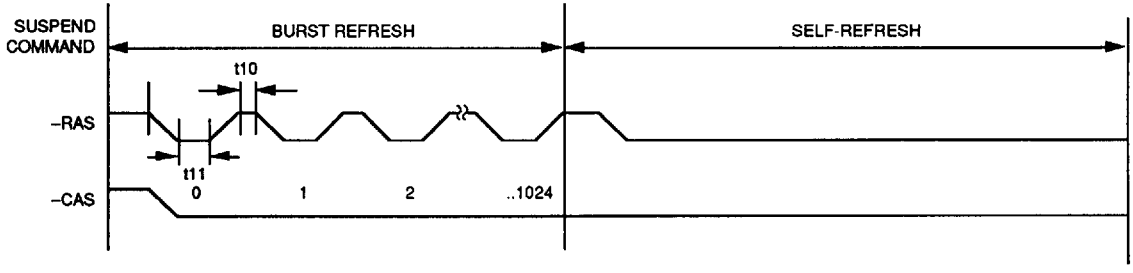


FIGURE 11.–RAS TIMING: LEAVING SELF-REFRESH MODE

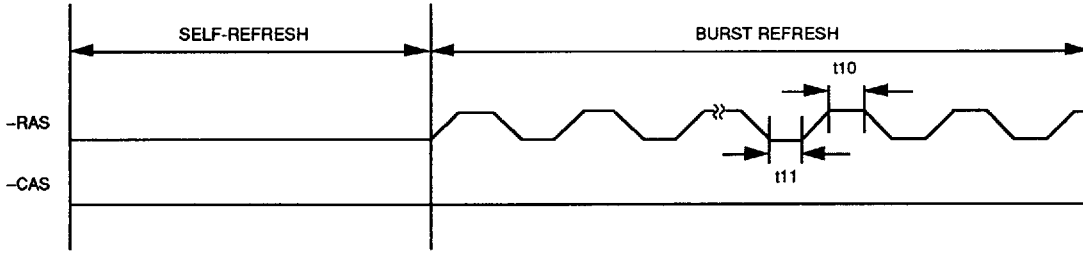
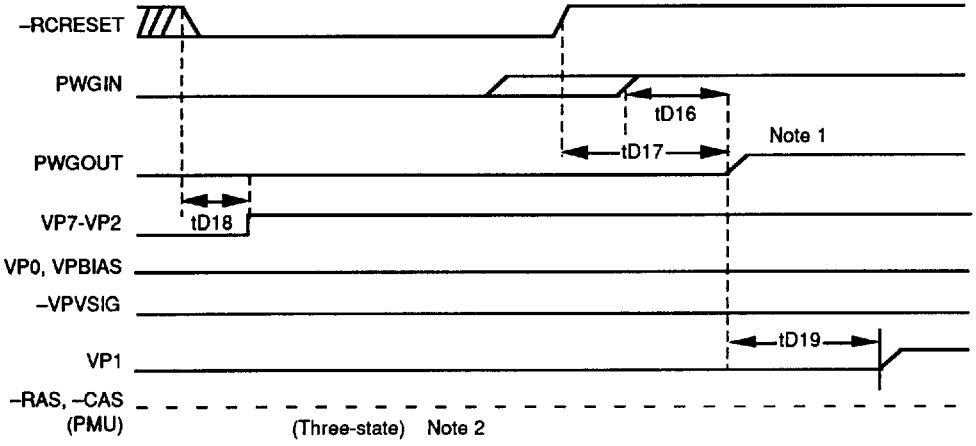


FIGURE 12. POWER-UP FROM –RCRESET TIMING (NO LCD AUTO-SEQUENCING)



Notes: 1. –RCRESET and PWGIN, whichever activates last 0.5 to 1.0 sec later, the VL82C323 drives PWGOUT high.

2. –RAS and –CAS from the VL82C323 are three-stated except when the VL82C323 enters the Suspend Mode. During the Suspend Mode the VL82C323 performs CAS-before-RAS refresh.

FIGURE 13. POWER-UP FROM EXT TIMING (NO LCD AUTO-SEQUENCING)

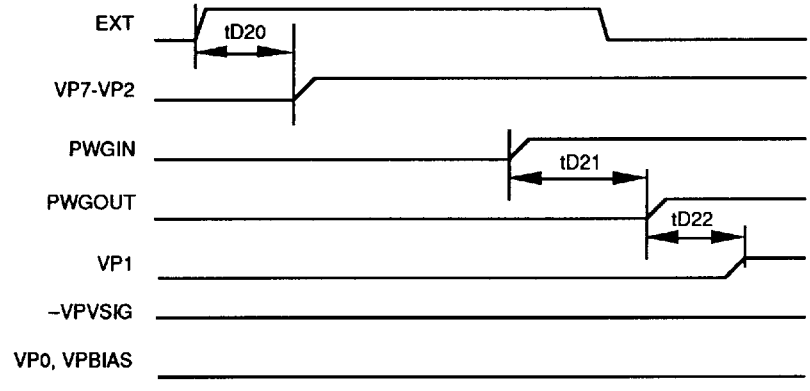


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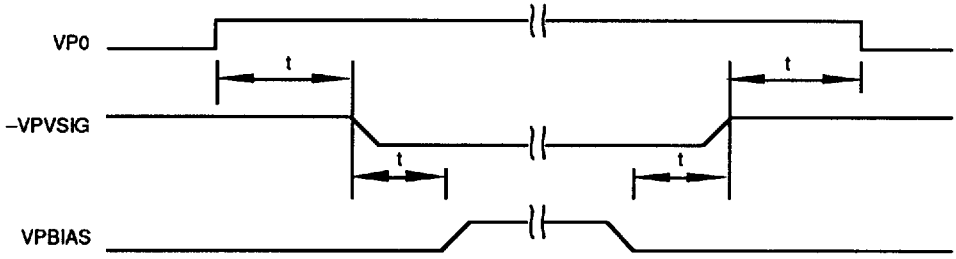
FIGURE 14. LCD AUTO-SEQUENCING TIMING



Note: t = the LCD sequencing time. t is based on the setup of D4 (data bit 4) of the MISCSET Register. The following table shows the requirements to enable LCD sequencing.

D4 = 1

D3	D2	t Delay
0	0	8 ms
0	1	15 ms
1	0	31 ms
1	1	125 ms

FIGURE 15. INMI TO NMI TIMING (NMI MODE)

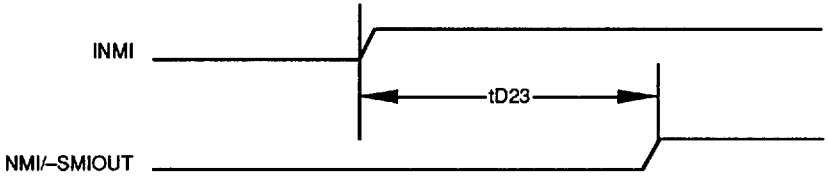
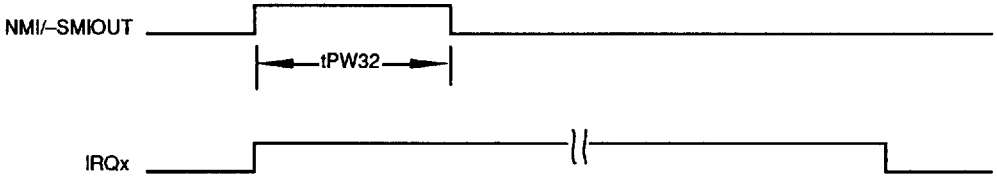


FIGURE 16. INTERNAL INTERRUPT GENERATION TIMING (NMI MODE)



Note: –SMI remains active until the falling edge of –SADS. IRQx remains active until the NMICAUSE Register is read.

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FIGURE 17. –SADS TO –SMIOUT TIMING

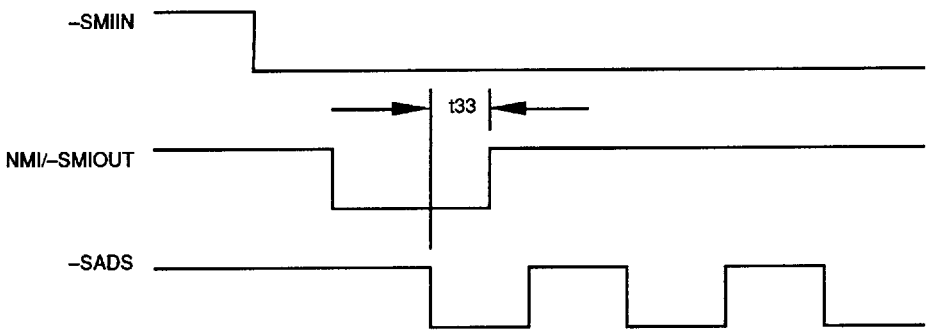
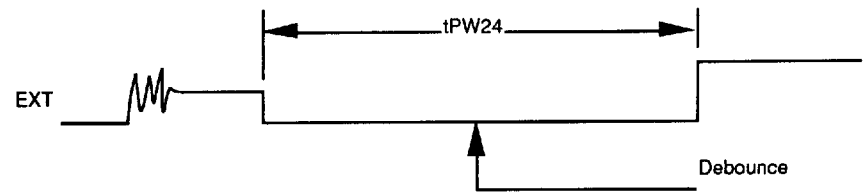


FIGURE 18. EXT TIMING (EXT CAUSES NMI FOR SUSPEND)



Note: EXT is internally debounced. It is required to go low for a minimum of 63 ms.

FIGURE 19. CLOCK CONTROL SWITCHING TIMING

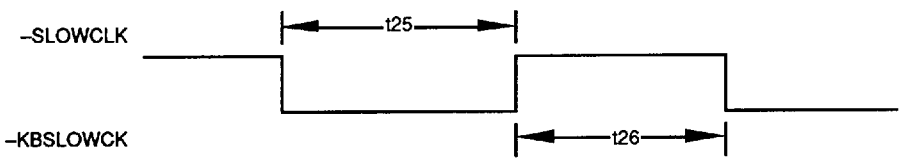
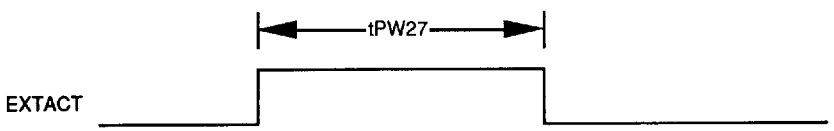


FIGURE 20. EXTACT TIMING



Note: EXTACT can remain high or low.

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FIGURE 21. POWER MODE TIMING

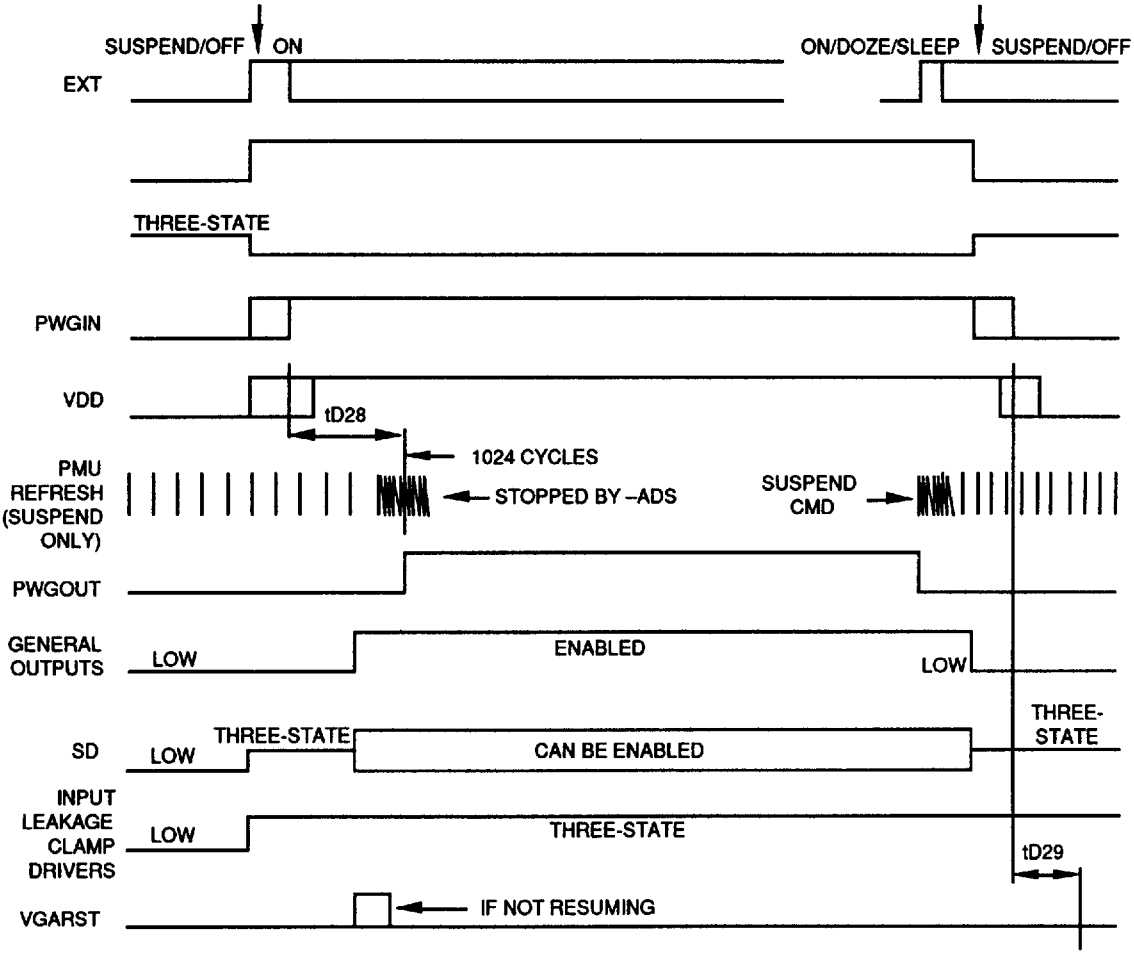
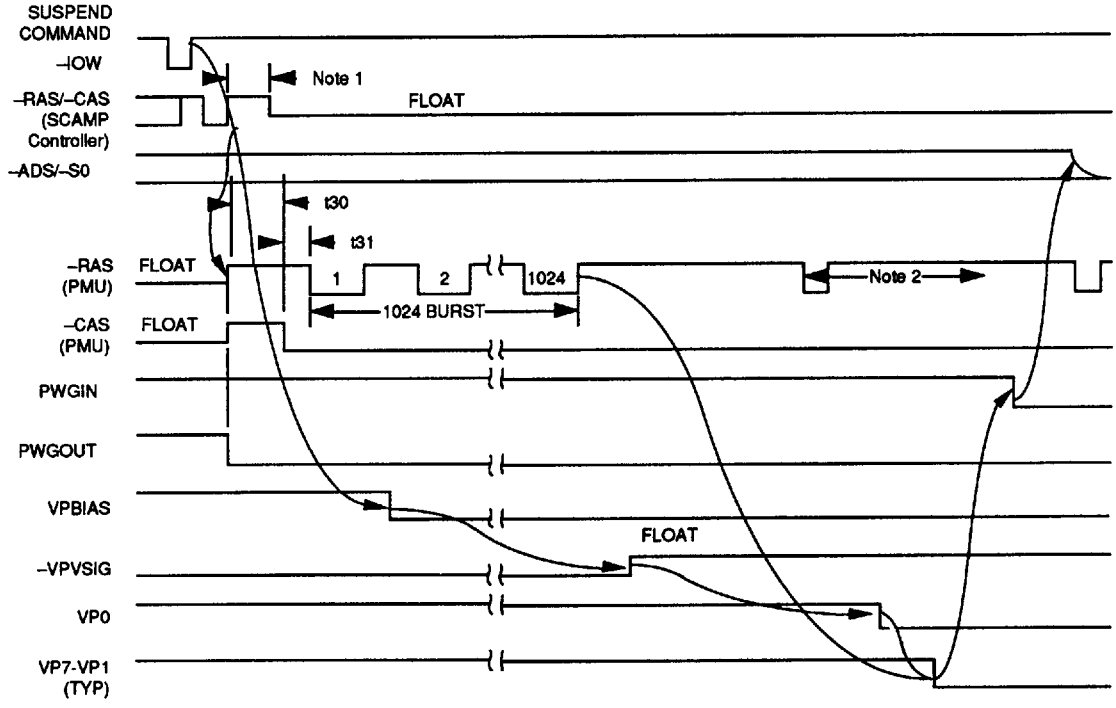


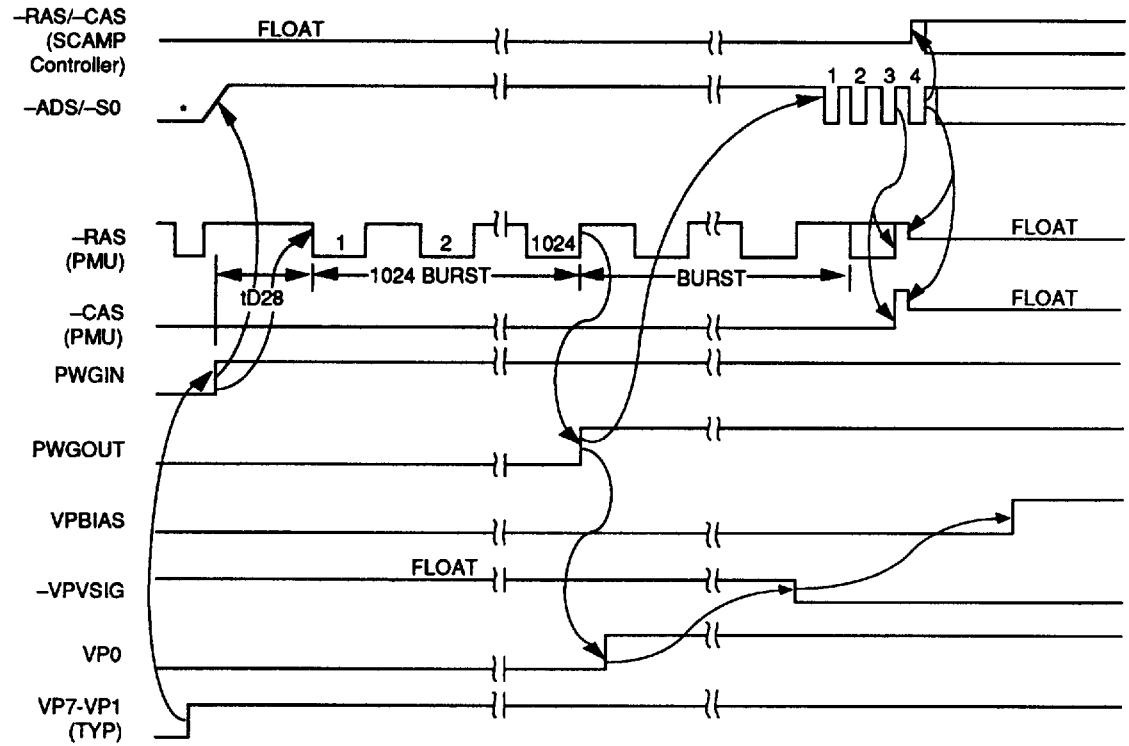
FIGURE 22. ON MODE TO SUSPEND MODE TIMING



Notes: 1. The SCAMP Controller floats RAS-before-CAS line within 400 ns after the falling edge of PWGOUT.

2. After completion of the 1024 cycle refresh burst, normal CAS-before-RAS refresh occurs at the programmed rate (15 or 122 µs).

FIGURE 23. SUSPEND MODE TO ON MODE TIMING



* Driven low by the VL82C323 during the Suspend Mode.

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FIGURE 24. OFF MODE TO ON MODE TIMING WITH LCD SEQUENCING

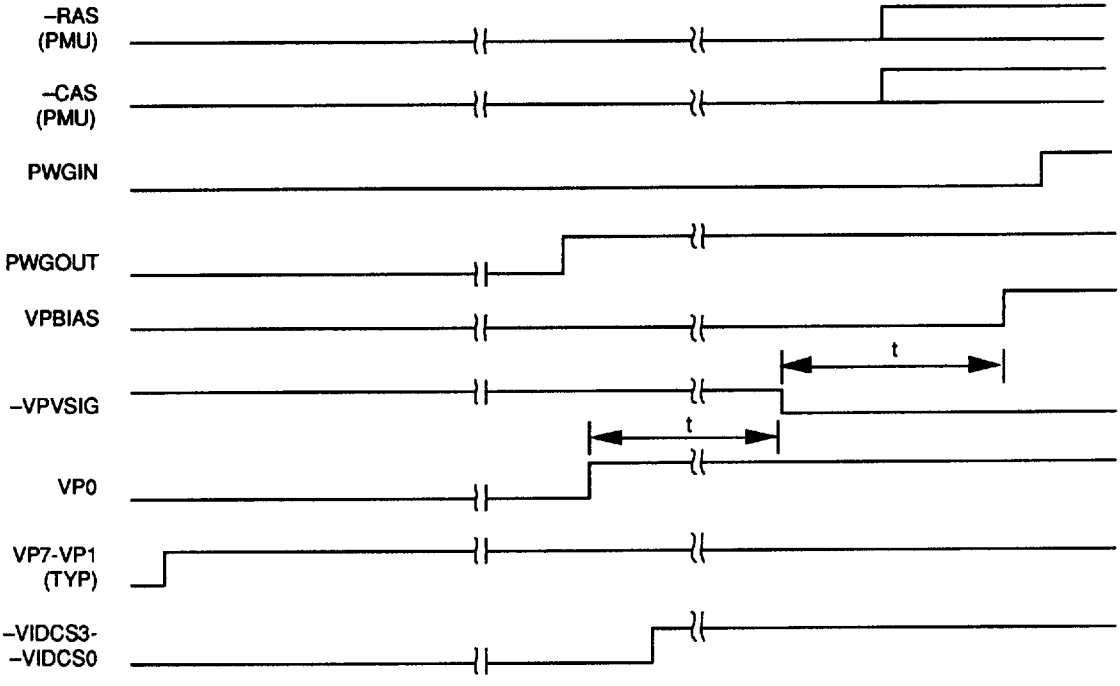

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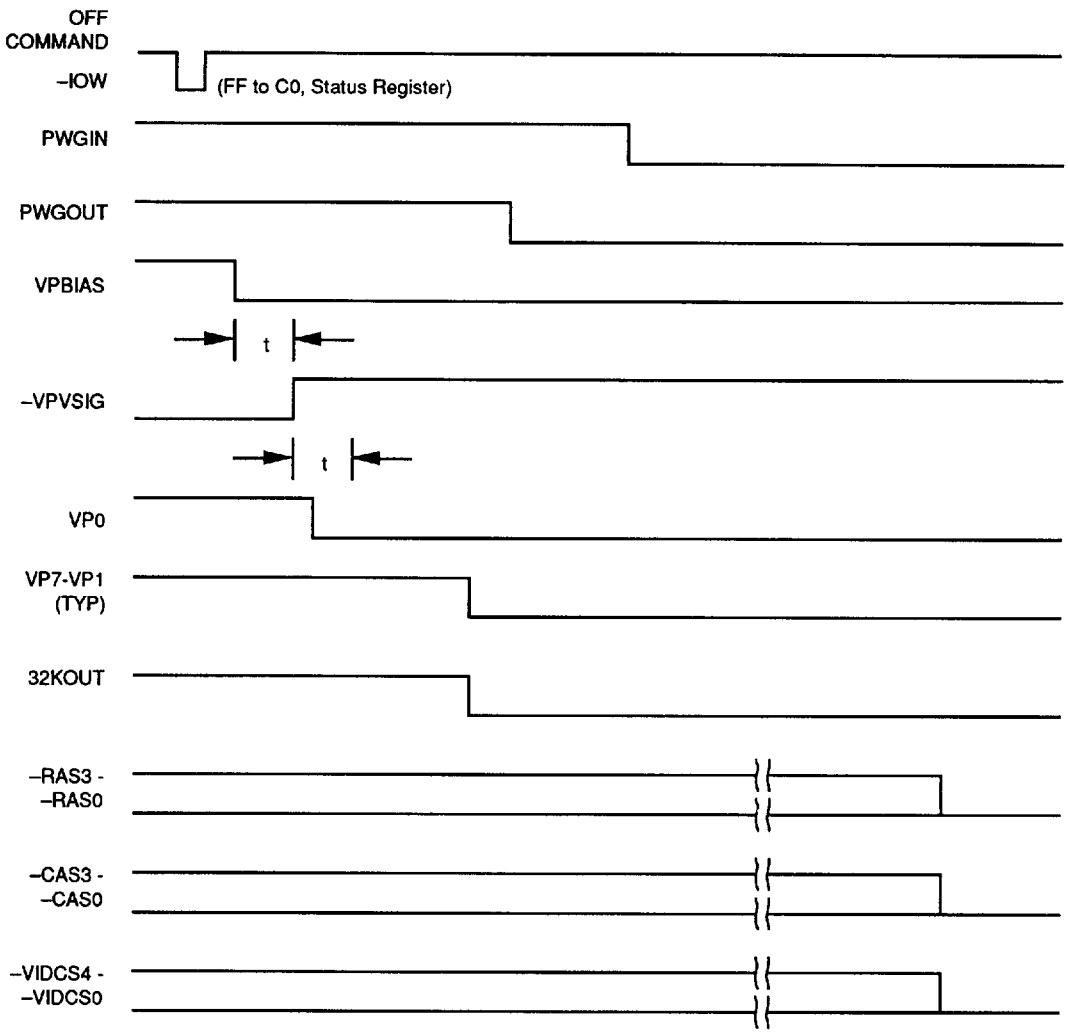
FIGURE 25. ON MODE TO OFF MODE TIMING WITH LCD SEQUENCING



Programmed by bits 2 and 3 (LCDTMG1, LCDTMG0) in the MISCSET Register with bit 4 (EN_LCDSEQ) high. 8 ms default.

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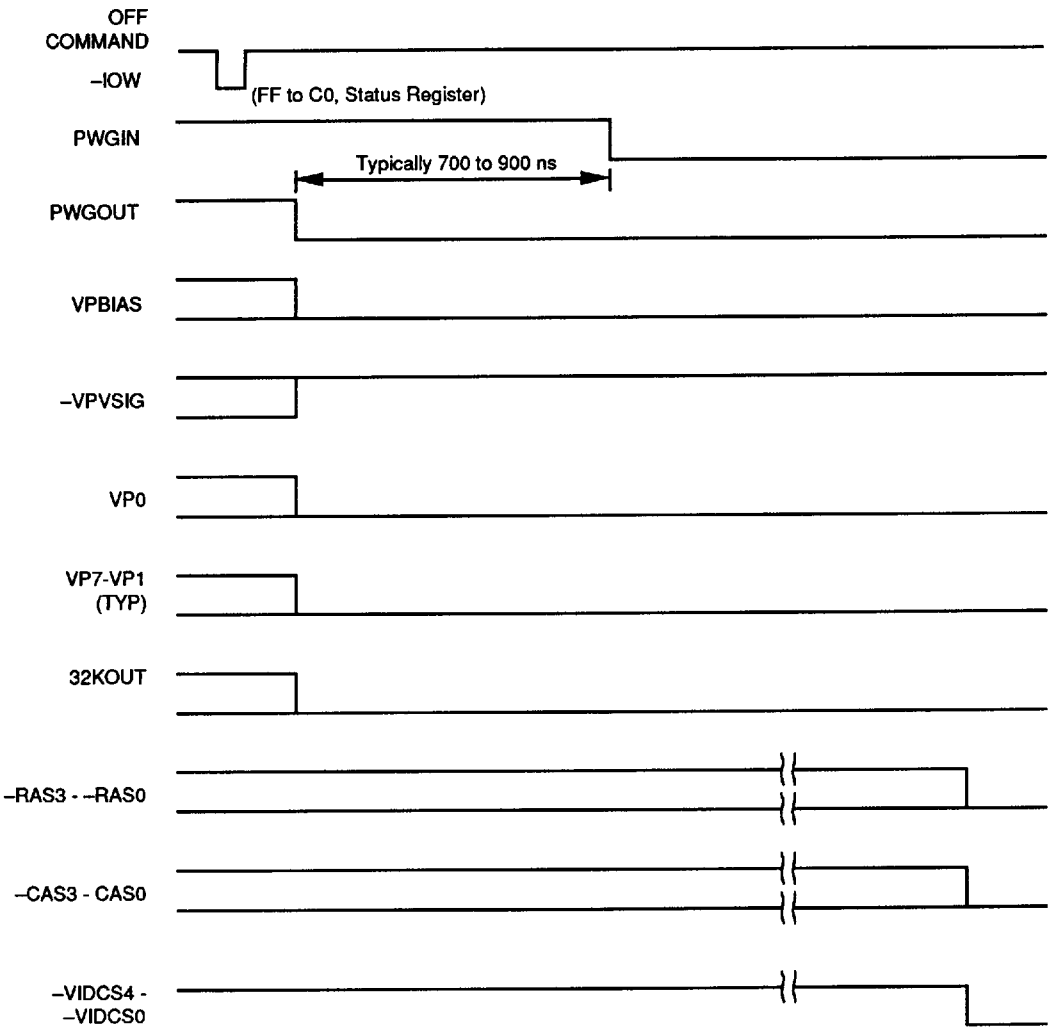
FIGURE 26. ON MODE TO OFF MODE TIMING WITH NO LCD SEQUENCING



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ABSOLUTE MAXIMUM RATINGS

Ambient Temperature −10°C to +70°C

Storage Temperature −65°C to +150°C

Supply Voltage to Ground Potential −0.5 V to 7.0 V

Applied Output Voltage −0.5 V to VDD + 0.5 V

Applied Input Voltage −0.5 V to VDD + 0.5 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

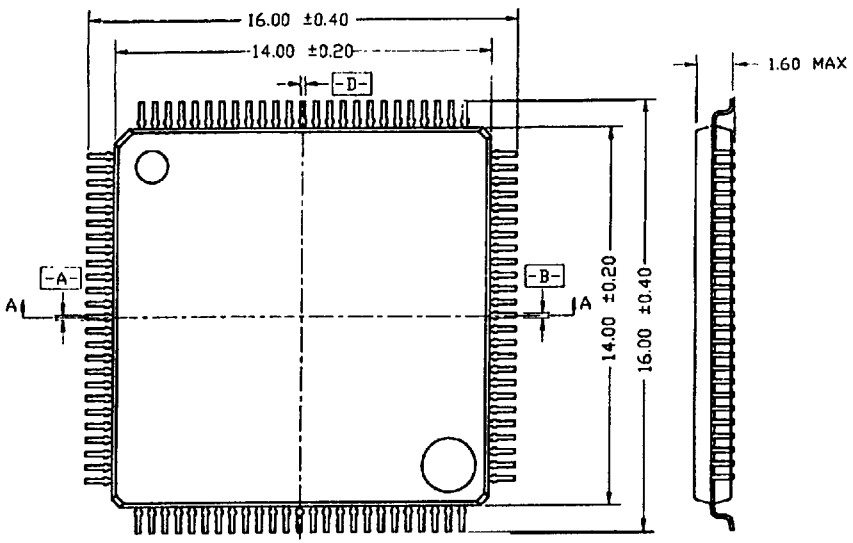
DC CHARACTERISTICS - 5.0 VOLT OPERATION: TA = 0°C to +70°C, VDD = 5.0 V ±10, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	−0.3	0.8	V	TTL-Compatible Inputs
VIH	Input High Voltage	2.4	VDD + 0.3	V	TTL-Compatible Inputs
VILC	Input Low Voltage	−0.3	VDD x 0.2	V	CMOS-Compatible Inputs
VIHC	Input High Voltage	VDD x 0.70	VDD + 0.3	V	CMOS-Compatible Inputs
VOL1	Output Low Voltage for Pins with -1 Pad Types*		0.45	V	IOL = 8 mA
			0.20	V	IOL = 100 µA
VOL2	Output Low Voltage for Pins with -2 Pad Types*		0.45	V	IOL = 12 mA
			0.20	V	IOL = 100 µA
VOL3	Output Low Voltage for Pins with -3 Pad Types*		0.45	V	IOL = 12 mA
			0.20	V	IOL = 100 µA
VOL4	Output Low Voltage for Pins with -4 Pad Types*		0.45	V	IOL = 24 mA
			0.20	V	IOL = 100 µA
VOH1	Output High Voltage for Pins with -1 Pad Types*	2.4	3	V	IOH = −4 mA
		VDD − 0.20		V	IOH = −100 µA
VOH2	Output High Voltage for Pins with -2 Pad Types*	2.4		V	IOH = −6 mA
		VDD − 0.20		V	IOH = −100 µA
VOH3	Output High Voltage for Pins with -3 Pad Types*	2.4		V	IOH = −6 mA
		3.5		V	IOH = −100 µA
VOH4	Output High Voltage for Pins with -4 Pad Types*	2.4		V	IOH = −6 mA
		VDD − 0.20		V	IOH = −100 µA
ILI	Input Leakage Current		±3	µA	0.1 V ≤ VIN ≤ VDD − 0.1 V
ILO	Output Three-State Leakage Current		±3	µA	0.1 V ≤ VOUT ≤ VDD − 0.1 V
LIPU	Input Current - Internal Pull-up	−30	−500	µA	VIN = 0.1 V
IDDSB	Static Power Supply Current		225	µA	No DC Loads. Outputs Open. VIL = 0.1 V, VIH = VDD − 0.1 V
IDDOP	Dynamic Power Supply Current		3.5	mA/MHz	No DC Loads. Outputs Open. VIL = 0.1 V, VIH = VDD − 0.1 V
CIN	Input or Output Capacitance		10	pF	
			15	pF	
COUT	Output Capacitance		10	pF	

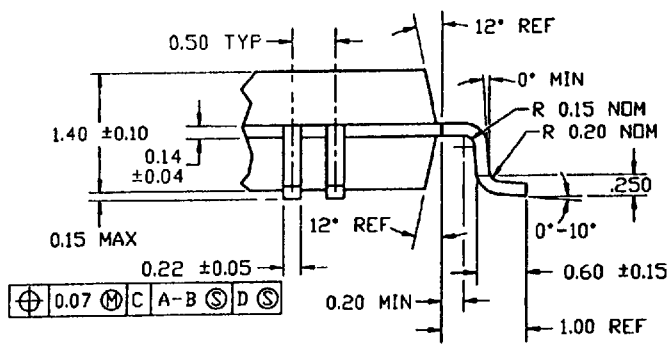
* Refer to the table "Pin Type by Operational State" on pages 3 and 4 for pad type information.

PACKAGE OUTLINE

100-LEAD THIN (PLASTIC) QUAD FLAT PACK



SECTION A-A



Notes:
1. All dimensions are in millimeters.
2. Leadframe material copper (OLIN 7025 or KLF125)
3. Mark of SG Indicates same side gate at mold.
4. To be molded cavity down (see section A-A).