VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

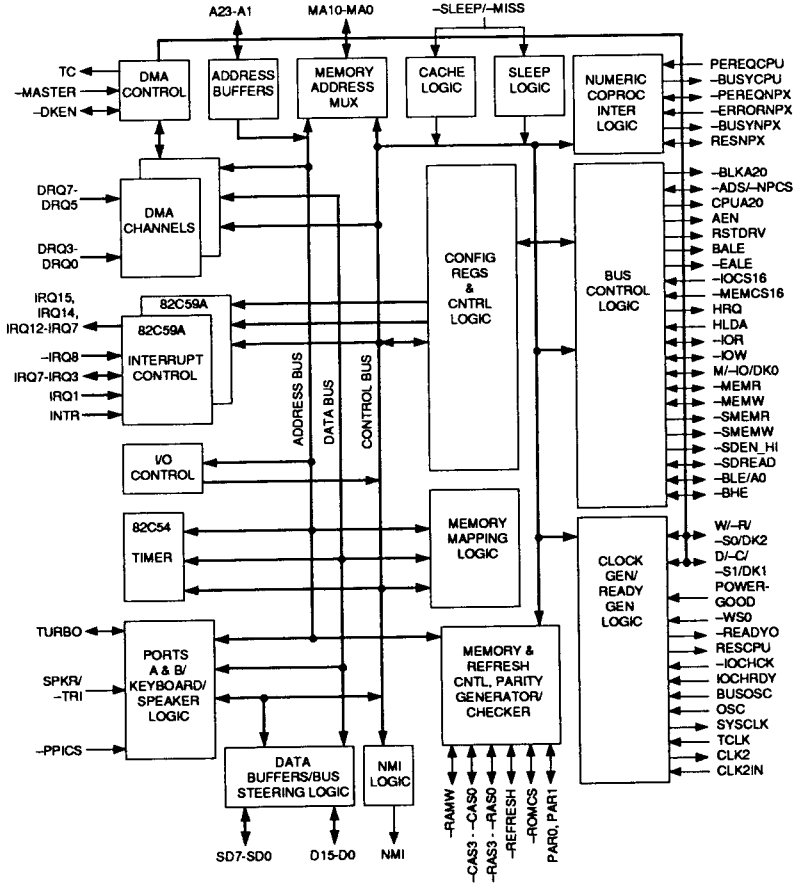
VL82C310/VL82C311/VL82C311L

SINGLE CHIP AT, MID-RANGE PERFORMANCE SCAMP™ CONTROLLER

FEATURES

- Fully compatible with 286- or 386SX-based PC/AT compatible systems (VL82C311L is 286 compatible only)
- Up to 25 MHz system clock in a 386SX-based system and up to 20 MHz in a 286-based system
- Replaces the following peripheral logic on motherboard:
  - Two 82C37A DMA controllers
  - 74LS612 memory mapper
  - Two 82C59A interrupt controllers
  - 82C54 timer
  - 82284 clock generator and ready interface
  - 82288 bus controller
- Includes:
  - Memory/refresh controller
  - Port B and NMI logic
  - Bus steering logic
  - Parity generation logic
  - Parity checking logic
  - Turbo Mode control logic
  - Staggered refresh to minimize power supply load variations
  - Three-state control pin for board level testability
- Memory controller features include:
  - Programmable option for page mode or non-page mode operation
  - Two-way block interleaving
  - Programmable option for zero and one wait state operation
  - Capability to drive up to four banks directly
- VL82C310 power saving features include:
  - Sleep Mode
  - Slow DRAM refresh
  - Low power page interleave memory mode
- Supports:
  - Up to 16 MB system memory
  - LIM EMS 4.0® over entire system memory

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C310-FC (SCAMP-LT)	Metric Quad Flat Pack
VL82C310-25FC (SCAMP-LT 25 MHz)	Metric Quad Flat Pack
VL82C311-FC (SCAMP-DT)	Metric Quad Flat Pack
VL82C311-25FC (SCAMP-DT 25 MHz)	Metric Quad Flat Pack
VL82C311L-FC (SCAMP-DT 286 Only)	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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LIM EMS 4.0 is a registered trademark of Lotus Development Corp., Intel Corp., and Microsoft Corp.

FEATURES (cont.)

- JEIDA IC Memory Card (VL82C310 only)
- VL82C325 (SX) Cache Controller
- Four 16-bit wide banks of 256K, 1M, or 4M DRAM or SRAM
- Shadow RAM in 640K to 1M range
- 287 and 387SX numeric coprocessors
- 8- and 16-bit wide BIOS ROMs
- Asynchronous slot bus operation
- Systems with up to 16 MHz backplane operation
- Relocation of video and slot ROMs

- Other advanced features:
  - Programmable I/O decode for 10- or 16-bit addresses
  - Hardware configurable setup to minimize custom BIOS requirements
  - Programmable drive current to reduce ringing on DRAM and slot bus interface signals
  - Programmable, extendable peripheral cycle
  - Capability to disable software coprocessor reset
  - Automatic bus speed-up on video access
- 1.0-micron CMOS technology
- 160-lead metric quad flat pack (MQFP)

DESCRIPTION

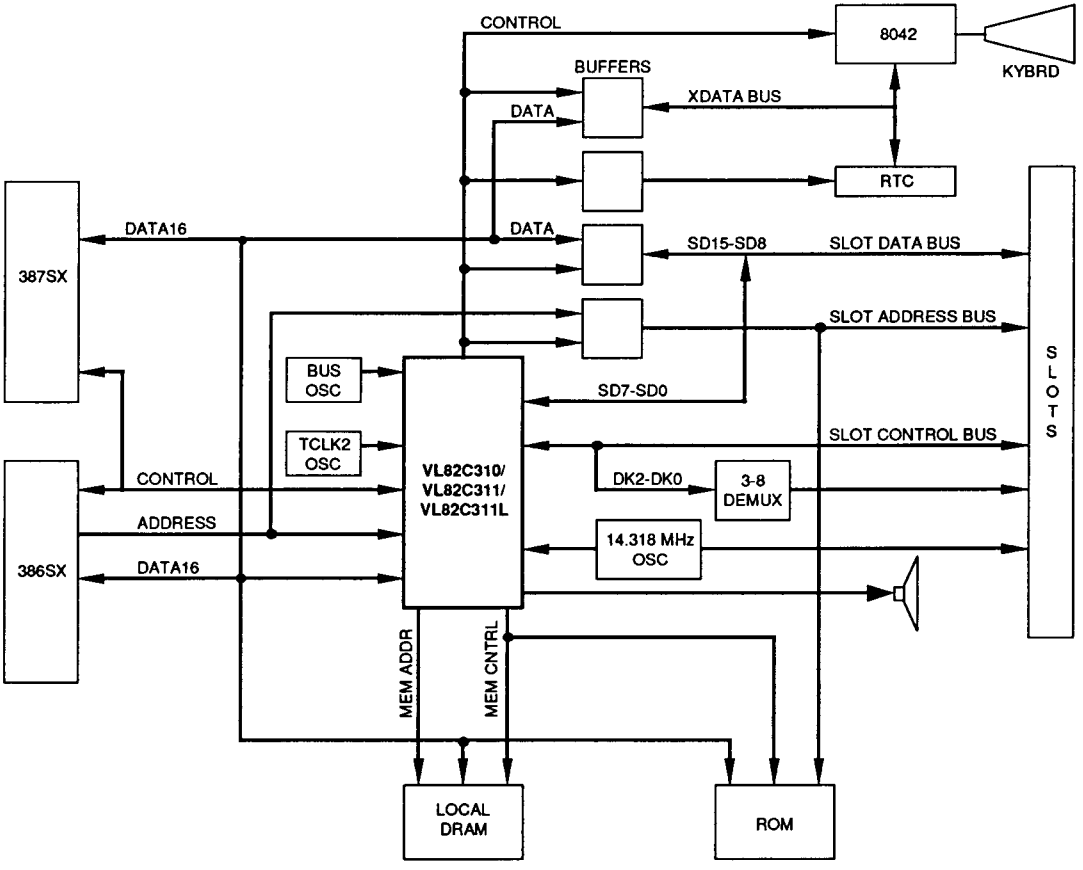
The VL82C310, VL82C311 and VL82C311L are Single Chip AT, Mid-range Performance (SCAMP™) Controllers for 286- or 386SX-based PC/AT-compatible systems. (The VL82C311L is for 286-based systems only.)

The VL82C310/VL82C311/VL82C311L includes the dual 82C37 DMA controllers, dual 82C59A programmable interrupt controllers, 82C54 programmable interval timer, 82284 clock and ready generator, 82288 bus controller and the logic for address/data bus control, memory control, shut down, refresh generation and refresh/DMA arbitration.

OVERVIEW

The VL82C310/VL82C311/VL82C311L Controllers (from here-in referred to as SCAMP Controller unless referring to a specific Controller, which will be called out by the device number) are designed to perform in 286- or 386SX-based PC/AT-compatible systems running up

SCAMP CONTROLLER-BASED PC/AT BLOCK DIAGRAM



to 25 MHz, and replaces the following devices on the motherboard:

- Two 82C37A DMA controllers
- Two 82C59A interrupt controllers
- 82C54 timer
- 74LS612 memory mapper
- 82284 clock generator and ready interface
- 82288 bus controller

The SCAMP Controller also includes the following:

- Memory/refresh controller
- Port B and NMI logic
- Bus steering logic
- Turbo Mode control logic
- Parity checking logic
- Parity generation logic

The SCAMP Controller supports LIM EMS 4.0, 287 and 387SX numeric coprocessors.

The memory controller logic is capable of accessing up to 16 MB of on-board DRAM. There can be up to four banks of 256K, 1M, or 4M attached in the system. The SCAMP Controller can drive four banks without external buffering. Built-in Page Mode operation and two-way interleaving allow the PC designer to maximize system performance using low cost DRAMs. Support is also included for zero and one wait state operation of system DRAM.

There are 36 Mapping Registers in the SCAMP Controller for full LIM EMS 4.0 standard support. The system allows backfill down to 256K for EMS support and provides 24 mapping registers covering this space. Twelve of the 36 Page Registers cover the EMS space from C0000h to EFFFFh. All registers are capable of translating over the complete range of on-board DRAM. Users preferring an alternate, plug-in EMS solution can disable the on-board EMS system as well as system board DRAM, as required, down to zero.

Shadowing features are supported on 16K boundaries between C0000h and DFFFFh, and on 32K boundaries between A0000h and BFFFFh and between E0000h and FFFFFh. Simultaneous use of EMS, shadowed ROM, and direct system board access is possible in a non-overlapping fashion throughout this memory space. Control over four access options is provided. These controls are overridden by EMS in the segments for which it is enabled. The options are:

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM

The SCAMP Controller handles system board refresh directly and controls the timing of slot bus refresh. Refresh is performed in the standard PC/AT Mode where on- and off-board refreshes are performed synchronously. Refreshes are staggered to minimize power supply loading and attenuate noise on the VDD and VSS pins. In the SCAMP Controller, refresh can be programmed to support CAS-before-RAS refresh operation or standard RAS-only refresh operation. The SCAMP Controller supports the PC/AT standard refresh period of 15.625 µs as well as 125 µs.

The VL82C310 (only) has eight Mapping Registers to support 32 MB of JEIDA IC Memory Card, also known as PC Card. Four of these registers are used as pointers to the CPU memory space between A0000h and FFFFFh and the other four point to four pages in the IC Memory Card.

The 287 numeric coprocessor is supported when the SCAMP Controller is strapped for 286 Mode. When configured for 386SX Mode, the 387SX is supported. A software coprocessor reset does not leave a 387SX in the same state as the reset of a 287 does. The SCAMP Controller can be programmed to disable these software resets if problems arise.

The interrupt controller logic consists of two 82C59 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally and two of the interrupt request inputs are connected to internal circuitry allowing a total of 13 external interrupt requests. There is a special programmable logic included in the SCAMP Controller which allows glitch-free inputs on all the interrupt request pins.

The interval timer includes one 82C54 counter/timer megacell. The counter/timer has three independent 16-bit counters and six programmable counter modes.

The DMA controllers are 82C37 compatible. The DMAs control data transfers between an I/O channel and on- or off-board memory. DMA can transfer data over the full 16 MB range available. There are internal latches provided for latching the middle address bits output by the 82C37 megacells on the data bus, and 74LS612 memory mappers are provided to generate the upper address bits.

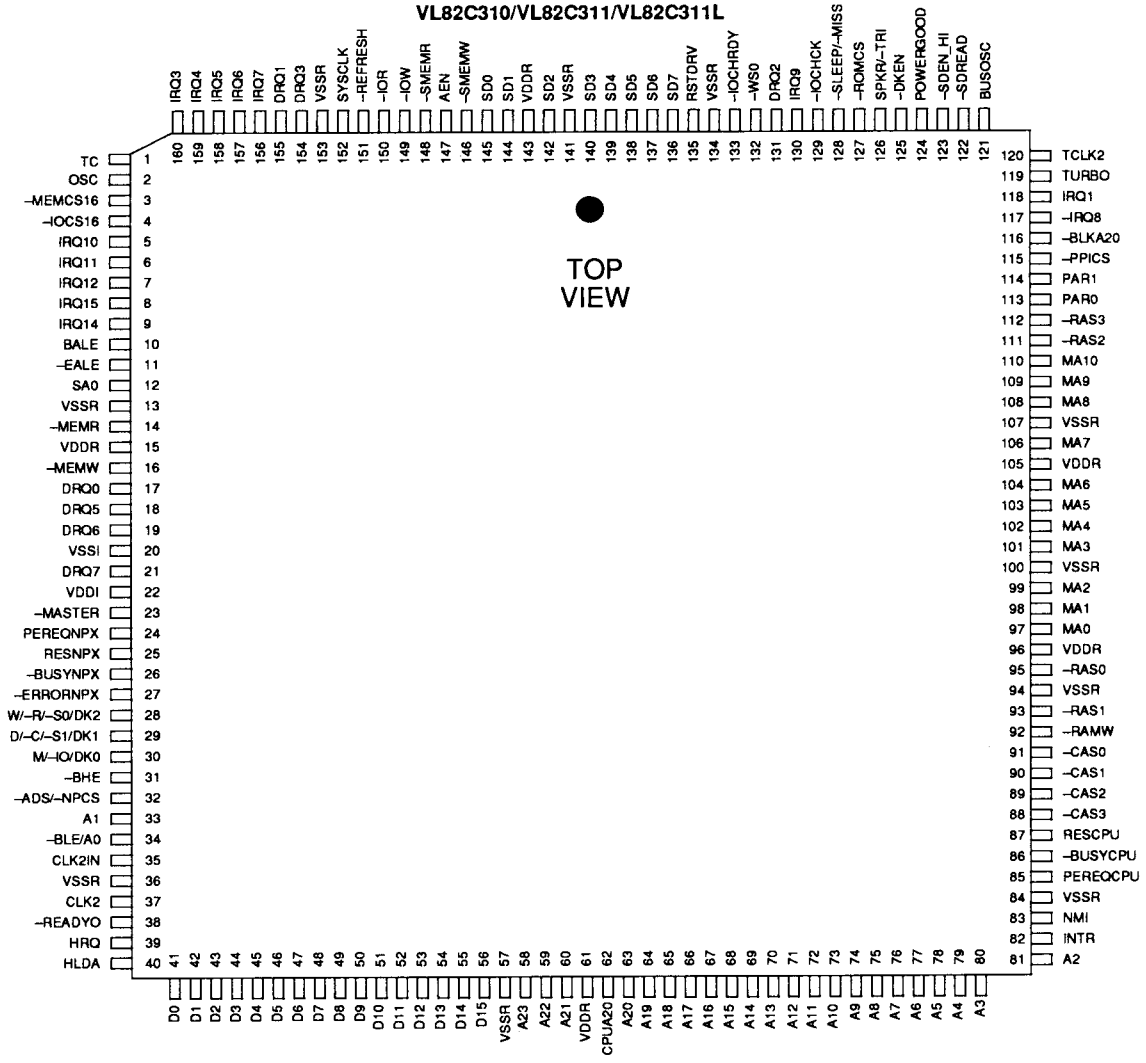
The SCAMP Controller can be programmed for asynchronous or synchronous operation of the AT bus.

The SCAMP Controller also performs all of the data buffer control functions required for a 286- or 386SX-based PC/AT system. Under the control of the CPU, the SCAMP Controller routes data to and from the CPU's D bus, the XD bus, and the slots (SD bus). The parity is checked for D bus DRAM read operations. The data is latched for synchronization with the CPU. Parity is generated for all data written to the D bus.

The SCAMP Controller generates control signals for external buffers to perform high-to-low and low-to-high byte swaps on the SD bus. For transfers between two peripherals on the slot bus, the flow control outputs of the SCAMP Controller disables the external data buffers. The SCAMP Controller also provides the feature of a single input, –TRI, to disable all of its outputs for board level testability.

The SCAMP Controller's functions are programmable via a set of internal Configuration Registers. The state of the memory address bus, parity pins, –ROMCS, –SDREAD, –DKEN, and –PPICS pins on reset is used to determine the default configuration. A dip switch can be used to establish the initial configuration.

PIN DIAGRAM



Note: Pin 128 is –SLEEP/–MISS for VL82C310, while VSSR for VL82C311/VL82C311L

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A20	63	IO-TTL	Address bus bit 20 - A20 is driven out during CPU, non-Master DMA, and Refresh Modes. During CPU Modes, this bit is equivalent to CPUA20 if internally generated signal A20GATE is high, otherwise A20 is forced low. During Master Mode cycles, this signal is an input.
A23-A21, A19-A1	58-60, 64-81, 33	IO-TTL	Address bus bits 23 through 21 and 19 through 1 - These Address bits are driven by the CPU when the CPU is the Bus Master. They are driven out by the SCAMP Controller whenever HLDA is active and –MASTER is high (non-Master Mode cycles). These bits allow direct access for up to 16 MB of memory.
–ADS/–NPCS	32	IO-TPU	Address Strobe or Numeric Coprocessor Chip Select - When the SCAMP Controller is programmed for 386SX support, this pin is the active low Address Strobe input signal. When programmed for 286 support, it is the numeric coprocessor chip select output, –NPCS . –ADS is driven by the 386SX as an indicator that the address and control signals currently supplied by the CPU are valid. This signal is used internally to indicate that the data and the command are valid and to determine the beginning of a memory cycle. –NPCS provides decoding of the 287 coprocessor's I/O space in when configured for 286 Mode. This is the entire F8h-FFh region when VLSI Special Features (VSF) are disabled. When VSF is enabled, only I/O accesses to F8h, FAh, FCh, and FEh cause –NPCS to be active.
–BHE	31	IO-TTL	Byte High Enable (active low) - Driven by the CPU, this signal is used to select the upper byte of a 16-bit wide memory location. This signal is driven by the SCAMP Controller whenever HLDA is active and –MASTER is high (non-Master Mode cycles).
–BLE/A0	34	IO-TPU	Byte Low Enable (active low) in 386SX Mode or A0 in 286 Mode - Driven by the CPU, this signal is used to select the lower byte of a 16-bit wide memory location. –BLE/A0 is an input during CPU cycles, and an output during HLDA cycles. This pin is pulled up internally.
–BUSYCPU	86	O	Busy CPU (active low) - This output signal sent to the CPU is generated by three sources. It always occurs in response to the –BUSYNPX input. It is also derived from –ERRORNPX and at system reset. –BUSYCPU toggles every refresh period when a coprocessor access is made when a cache controller is present and the coprocessor is absent in the system. This is to prevent system hang-up.
CLK2	37	O	This output signal is a CMOS level signal which is the frequency of, and in phase with, the TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
CLK2IN	35	I-CMOS	This is the main clock input to the SCAMP Controller state machine and is connected to the CLK2 signal that is output by the SCAMP Controllers.
CPUA20	62	IO-TPU	CPU Address Bit 20 input - It is an output during Master Mode and DMA cycles. This pin is pulled up internally.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
D/–C/–S1/DK1	29	IO-TPU	This pin has three functions depending on the operating mode. It is DATA or active low CODE enable driven by the CPU in 386SX Mode or –S1 in 286 Mode. This signal is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/–R/–S0 definition for bus cycle types. During DMA acknowledge cycles, this is an output signal which along with DK0 and DK2 represents the encoded channel number being serviced. This pin is pulled up internally.
D15-D0	56-41	IO-TTL	Data bus bit 15 through 0 - This is the data bus directly connected to the CPU. It is also referred to as the local data bus.
–DKEN	125	IO-CMOS	Decoder Enable (active low) - This signal enables an external 3-to-8 decoder for the generation of the DMA acknowledge signals from DK0-DK2. –DKEN along with –PPICS is used at power-on reset to select the frequency of the bus clock, SYSCLK, for normal operation. Refer to the section "System Configuration" for further details.
HLDA	40	I-TTL	Hold Acknowledge - This active high signal is issued by the CPU in response to the HRQ driven by the SCAMP Controller. It indicates that the CPU is floating its outputs to the high impedance state, so that another Master may take control of the bus.
HRQ	39	O	Hold Request - An active high output that is driven by the SCAMP Controller to the CPU. It indicates that a Bus Master, such as a DMA or refresh controller, is requesting control of the bus. It is synchronized to CLK2.
INTR	82	O	Interrupt Request - INTR is used to interrupt the CPU and is generated by the 82C59 megacells any time a valid interrupt request input is received.
M/–IO/DK0	30	IO-TPU	Memory or (active low) I/O enable - This signal is driven by the CPU. With the remaining CPU control signals M/–IO is decoded to indicate the type of bus cycle requested. See W/–R/–S0 definition for bus cycle types. During DMA acknowledge cycles, this is an output signal which along with DK1 and DK2 represents the encoded channel number being serviced. This pin is pulled up internally.
NMI	83	O	Non-Maskable Interrupt - This output is used to drive the NMI input to the CPU. It is asserted by either a parity error or an I/O channel error. The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.
PEREQCPU	85	O	Processor Extension Request - An active high signal that is sent to the CPU in response to a PEREQNPX which is issued by the coprocessor to the SCAMP Controller. It indicates to the CPU that the coprocessor is requesting a data operand to be sent to or from memory by the CPU. For PC/AT compatibility, PEREQCPU is returned active on occurrence of an –ERRORNPX after –BUSYNPX has gone inactive. A write to F0h by the interrupt 13 handler returns control of the PEREQCPU signal to directly follow the PEREQNPX input.
–READYO	38	O	Ready Out (active low) - This signal is an indication that the current memory or I/O bus cycle is complete. It is generated from the internal DRAM controller or the synchronized version of –IOCHRDY for slot bus accesses. Outside the chip, it is ORed with any other local bus I/O or Master. The culmination of these ORed READY signals is sent to the CPU.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
RESCPU	87	O	Reset CPU - An active high signal sent to the CPU by the SCAMP Controller. It is issued in response to the control bit for software reset located in the Port A register or in response to a dummy read from I/O port EFh. It is also issued in response to an active POWERGOOD input and in response to detection of a shutdown command. In all cases it is synchronized to CLK2.
TCLK2	120	I-CMOS	This input is connected to a crystal oscillator whose frequency is twice the system frequency. The CMOS level oscillator output is converted internally to CMOS levels and sent to the CLK2 output.
W/–R/–S0/DK2	28	I/O-TPU	This pin has three functions depending on the operating mode. It is a write or an active low read enable input driven by the CPU in 386SX Mode or –S0 in 286 Mode. This signal is decoded with M/–IO and D/–C/–S1 to indicate the type of bus cycle requested. The bus cycle types include interrupt acknowledge, halt, shutdown, I/O reads and writes, memory data reads and writes, and memory code reads. During DMA acknowledge cycles, this is an output signal which along with DK0 and DK1 represents the encoded channel number being serviced. This pin is pulled up internally.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
–CAS3 - –CAS0	88-91	O	Active low Column Address bit 3 through 0 - These signals are sent to their respective RAM banks to strobe in the column address during on-board memory bus cycles. There is a –CAS signal for the upper and lower bytes of each of the two 16-bit DRAM memory banks. The active period for this signal is determined by the number of wait states and Page Mode configuration. For clarity, alternate names may also be used for these signals as shown in the following table where the digit in the Alternate Name indicates the DRAM bank the signal drives. L indicates it drives the low byte and H indicates it drives the high byte. These signals are three-stated following a system reset for a period of four –ADSs and should be pulled up externally to avoid corrupting the data bus (typical 10k ohms).

Standard Name	Alternate Name
–CAS0	–CAS0L
–CAS1	–CAS0H
–CAS2	–CAS1L
–CAS3	–CAS1H

MA10-MA0	110-97	IO-CMOS	Memory Address bits 0 through 10 - These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the CPU bus addresses. They allow addressing of up to 16 MB of memory. MA10-MA0 pins are used at power-on reset for configuration purpose. Refer to the section "System Configuration" for further details.
–RAMW	92	IO-CMOS	RAM Write (active low) - This signal is output to the DRAM memory to control the direction of data flow of the on-board memory. It is a result of the address and bus control decode. It is active during on-board memory write cycles and high at all other times. –RAMW selects the processor type, 386SX or 286, at power-on reset. When tied high, 386SX is assumed otherwise 286 is assumed to be used in the system.
–RAS3- –RAS0	112, 111, 93, 99	O	Row Address bits 3 through 0 (active low) - These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
COPROCESSOR SIGNALS			
–BUSYNPX	26	I-TPU	Coprocessor Busy (active low) - Driven by the coprocessor, this signal indicates that it is currently executing a previous instruction and is not ready to accept another. –BUSYNPX is decoded internally to produce IRQ13 and to control PEREQCPU.
–ERRORNPX	27	I-TPU	Coprocessor Error (active low) - Sent from the coprocessor, this signal indicates that an error has occurred in the previous instruction. –ERRORNPX is internally gated and latched with –BUSYNPX to produce IRQ13.
PEREQNPX	24	I-TPD	Coprocessor Extension Request - This is an active high input signal. It is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQCPU during NPX interrupts.
RESNPX	25	O	Coprocessor Reset - This output is connected to the coprocessor reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. A write to port F1h resets only the coprocessor. The coprocessor instruction FINIT should be executed after an F1h generated reset in a 386SX system. Otherwise the 387SX is not initialized to the same state that a 287 is placed in by hardware reset alone. For compatibility, the F1h reset may be disabled by setting bit 6, F1CTL, of the MISCSET Register.
SD DATA BUS CONTROL SIGNALS			
SD7-SD0	136-140, 142 144, 145	IO-TTL	System Data bus bits 7 through 0 - This bus connects directly to the slots. It is used to transfer data to and from the low byte of local and system devices.
–SDEN_HI	123	O	System Data High Enable - This output is the enable signal for the SD15-SD8 to D15-D8 transceiver.
–SDREAD	122	IO-CMOS	System Data Read (active low) - The direction control signal for the SD bus data transceivers. This pin is used at power-on reset to select the external or default system configuration. This pin must be connected to a jumper. Refer to the section "System Configuration" for further details.
PERIPHERAL INTERFACE SIGNALS			
–PPICS	115	IO-CMOS	The –PPICS output is an active low chip select for the keyboard controller and real-time clock. The –PPICS output is active any time a system bus address is decoded at 60h, 64h, 70h, or 71h. It is intended to be used as enable of a decoder which generates chip select for the keyboard controller. –PPICS, in conjunction with the –DKEN pin, at power-on reset selects the bus clock, SYSCLK, frequency for normal operation. Refer to the section "System Configuration" for further details.
–ROMCS	127	IO-CMOS	ROM Chip Select - This output is active in CPU Mode only (HLDA is negated). It is active anytime the address on the A bus selects the address range between FE0000h-FFFFFFh or 0E0000h-0FFFFFh during a memory read/write cycle. This pin is used for the system configuration purpose at power-on reset. –ROMCS when pulled low, selects 12 mA current drive for the slot signals. It should be tied high for 24 mA current drive. Refer to section "System Configuration" for further details.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SLEEP/–MISS	128	I-TPU	Sleep Enable (active low) or Miss (active low) - Depending on the state of the PINFNC bit (bit 1 SLPCTL Register) this pin will function as a –SLEEP pin, for low-power applications, or as a –MISS pin for interface with the VL82C325 Cache Controller. Refer to "Sleep Mode Control Logic" section for further information. When using the VL82C311 or VL82C311L, this is pin is used only as the –MISS signal.
SPKR/–TRI	126	I/O-TPU	Speaker or Three-state (active low) - This output drives an externally buffered speaker. This signal is created by gating the output of timer 2. Bit 1 of Port B, 61h, is used to enable the speaker output, and bit 0 is used to gate the output of the timer. This signal is an input when the POWER-GOOD input is low. If this input is sampled low, it forces the SCAMP Controller into the Three-state Mode where all outputs and bidirectional pins are driven to a high impedance state. SPKR is pulled up internally.
TURBO	119	I-TTL	Turbo - An active high level input to the SCAMP Controller that determines the speed at which the system board operates. This input signal is normally an externally ANDed signal from the keyboard controller and Turbo switch. Internally, it is ANDed with a software controlled latch. When high, operation is at full speed. When low, CLK2 is divided to operate at 8 MHz or lower for any valid CPU speed.
BUS INTERFACE SIGNALS			
AEN	147	O	Address Enable - This output goes high anytime the inputs HLDA and –MASTER are both high.
BALE	10	O	Buffered Address Latch Enable - An active high pulse that is generated at the beginning of any bus cycle initiated from the CPU which is not directed to on-board DRAM. BALE is forced high anytime HLDA is high.
–BLKA20	116	O	Block A20 - This active low signal indicates the dividing line of the 1 MB memory boundary. It is a logic OR of the internal A20GATE signal and Port A bit 1.
BUSOSC	121	I-TPU	Bus Oscillator - Supplied from an external oscillator, this signal is used for AT Bus operations and for non-TURBO processor cycles. If SYSCLK is to be derived from TCLK2, the BUSOSC input is used to determine the clock divisor to be used. During normal operation, the BUSOSC pin can be used in conjunction with an internal register to select SYSCLK to be TCLK2/2, TCLK2/4, TCLK2/6, or TCLK2/8. If an oscillator is connected to this pin, SYSCLK can be programmed to be BUSOSC/2, BUSOSC/4, BUSOSC/6, or BUSOSC/8.
DRQ7-DRQ5, DRQ3-DRQ0	21, 19, 18, 154, 131, 155, 17	I-TSPU	DMA Request - These asynchronous inputs are used by external devices to indicate when they need service from the internal DMA controllers. DRQ3-DRQ0 are used for transfers between 8-bit I/O adapters and system memory. DRQ7-DRQ5 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together. All DRQ pins have internal pull-ups.
–EALE	11	O	Early Address Latch Enable - An active low pulse that is generated at the beginning of any bus cycle initiated from the CPU which is not directed at the on-board DRAM. –EALE is forced low anytime HLDA is high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–IOCHCK	129	I-TTL	I/O Channel Check (active low) - An input signal used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHCK assertion by a peripheral device generates an NMI to the processor. The state of the –IOCHCK signal is read as data bit D6 of the Port B register.
–IOCHRDY	133	I-TTL	I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, the DMA controllers, or the refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals, and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data or strobe in write data in this amount of time must use –IOCHRDY to extend these cycles.
–IOCS16	4	I-TTL	16-bit I/O Chip Select - An input used to determine when a 16- to 8-bit conversion is needed for CPU accesses. A 16-to-8 conversion is done anytime the SCAMP Controller requests a 16-bit I/O cycle and –IOCS16 is sampled high. If –IOCS16 is sampled high, a command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long. If sampled low, an I/O access is performed in one wait state with one command delay inserted.
–IOR	150	IO-TTL	I/O Read - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –IOR is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, it is driven by the 82C37 DMA controller megacells. This pin requires an external 10k ohm pull-up resistor.
–IOW	149	IO-TTL	I/O Write - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –IOW is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, it is driven by the 82C37 DMA controller megacells. This pin requires an external 10k ohm pull-up resistor.
IRQ15, IRQ14, IRQ12-IRQ9, IRQ7-IRQ3, IRQ1, –IRQ8	8, 9, 7-5, 130 156-160, 118, 117	I-TSPU	Interrupt Request - These signals are the asynchronous interrupt request inputs for the 82C59 megacells. IRQ0, IRQ2, and IRQ13 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 82C54 counter 0. IRQ2 is used to cascade the two 82C59 megacells together. IRQ13 is used for numeric coprocessor error. All IRQ input pins except –IRQ8 are active high and have internal pull-ups. –IRQ8 is an active low input. All IRQ pins have a special programmable logic to reduce noise sensitivity. The logic is controlled by bit IRQIN in the BUSCTL Register. When this bit is set, the input to these pins must be stable for at least 105 ns to generate an interrupt.
–MASTER	23	I-TTL	Master (active low) - An input that is used by an external device to disable the internal DMA controllers and to get access to the system bus. When asserted, it indicates that an external Bus Master has control of the bus.
–MEMCS16	3	I-TTL	16-bit Memory Chip Select - This input is used to determine when a 16- to 8-bit conversion is needed for CPU accesses. A 16-to-8 conversion is done anytime the SCAMP Controller requests a 16-bit memory cycle and –MEMCS16 is sampled high. If –MEMCS16 is sampled high, a command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long. If sampled low, a memory access is performed in one wait state with no command delays inserted.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–MEMR	14	IO-TTL	Memory Read - When HLDA is high and –MASTER is low, this signal is an input. It is an output at all other times. When HLDA is low, –MEMR is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, it is driven by the 82C37 DMA controller megacells. This pin requires an external 10k ohm pull-up resistor.
–MEMW	16	IO-TTL	Memory Write - When HLDA is high and –MASTER is low, this signal is an input. It is an output at all other times. When HLDA is low, –MEMW is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, it is driven by the 82C37 DMA controller megacells. This pin requires an external 10k ohm pull-up resistor.
OSC	2	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
PAR1-PAR0	114, 113	IO-TTL	Parity bit byte 1 and 0 - These bits are generated by the parity generation circuitry. They are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred. PAR1-PAR0 are used at power-on reset to program ROM wait states. Refer to the "System Configuration" section for further details. These pins have to be pulled up when they are not used for power-on reset configuration and parity checking/generation is disabled.
POWERGOOD	124	I-TSPU	System power-on reset - This input signals that power to the board is stable. A Schmitt-trigger input is used. This allows the input to be connected directly to an RC network.
–REFRESH	151	IT-OD	Refresh (active low) - An I/O signal that is pulled low whenever a refresh cycle is initiated. It is used as an input to sense refresh requests from external sources such as Bus Masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23-A17. –REFRESH is an open drain output capable of sinking 24 mA and requires an external pull-up resistor.
RSTDRV	135	O	System Reset - This active high output signal is generated from the POWERGOOD input. RSTDRV is synchronized to the BUSOSC input.
SA0	12	IO-TTL	System Address bus bit 0.
–SMEMR	148	O	Memory Read - This signal is active during refresh cycles and memory read cycles to addresses below 1 MB. This pin requires an external 10k ohm pull-up resistor.
–SMEMW	146	O	Memory Write - This signal is active during memory write cycles to addresses below 1 MB. This pin requires an external 10k ohm pull-up resistor.
SYSCLK	152	O	System Clock - This output is 1/2, 1/4, 1/6, or 1/8 the frequency of TCLK2 or BUSOSC depending on the BUSOSC pin status and the four lower bits in the CLKCTL Register. The bus control signals BALE, –IOR, –IOW, –MEMR and –MEMW are synchronized to SYSCLK.
TC	1	O	Terminal Count - An output that indicates one of the DMA channel's terminal count has been reached. This signal directly drives the system bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–WS0	132	I-TSPU	Wait State terminate - This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWER AND GROUND PINS			
VDDR	15, 61, 96, 105, 143	PWR	Pad-ring power connection - These pins along with the VSSR pins should be separately bypassed.
VSSR	13, 36, 57, 84, 94, 100, 107, 134, 141, 153	GND	Pad-ring ground connection.
VDDI	22	PWR	Core-logic power connection - This pin along with the VSSI should be separately bypassed.
VSSI	20	GND	Core-logic ground connection.

SIGNAL LEGEND

Signal Code	Signal Type
I-CMOS	CMOS level input
I-TTL	TTL level input
I-TPU	TTL level input with 30k ohm pull-up resistor
I-TST	TTL level Schmitt-trigger input
IO-TTL	TTL level input/output
IO-TOD	TTL level input/output open drain
IO-TODNP	TTL level input/output open drain with 3k ohm NMOS pull-up
IO-TODPU	TTL level input/output open drain with 30k ohm pull-up resistor
IO-TODS	TTL level with open drain output/Schmitt-trigger input
IO-TPU	TTL level input/output with 30k ohm pull-up resistor
O	CMOS and TTL level compatible output
GND	Ground
PWR	Power

FUNCTIONAL DESCRIPTION

The SCAMP Controller can broadly be divided into two blocks; the system controller block and the ISA bus controller block as shown in Figure 1. The system controller block includes the 82284 clock generator, ready generator, and the logic for address/data bus control, memory control, and shutdown. The ISA bus controller block includes the dual 82C37 DMA controllers, dual 82C59A programmable interrupt controllers, 82C54 programmable interval timer, and the logic for refresh generation and refresh/DMA arbitration.

The following sections cover detailed operational information for the various logical groupings of SCAMP Controller's subsystems. In most of these sections, the effect of configurable elements that can be controlled via I/O Registers is discussed at length.

CPU INTERFACE

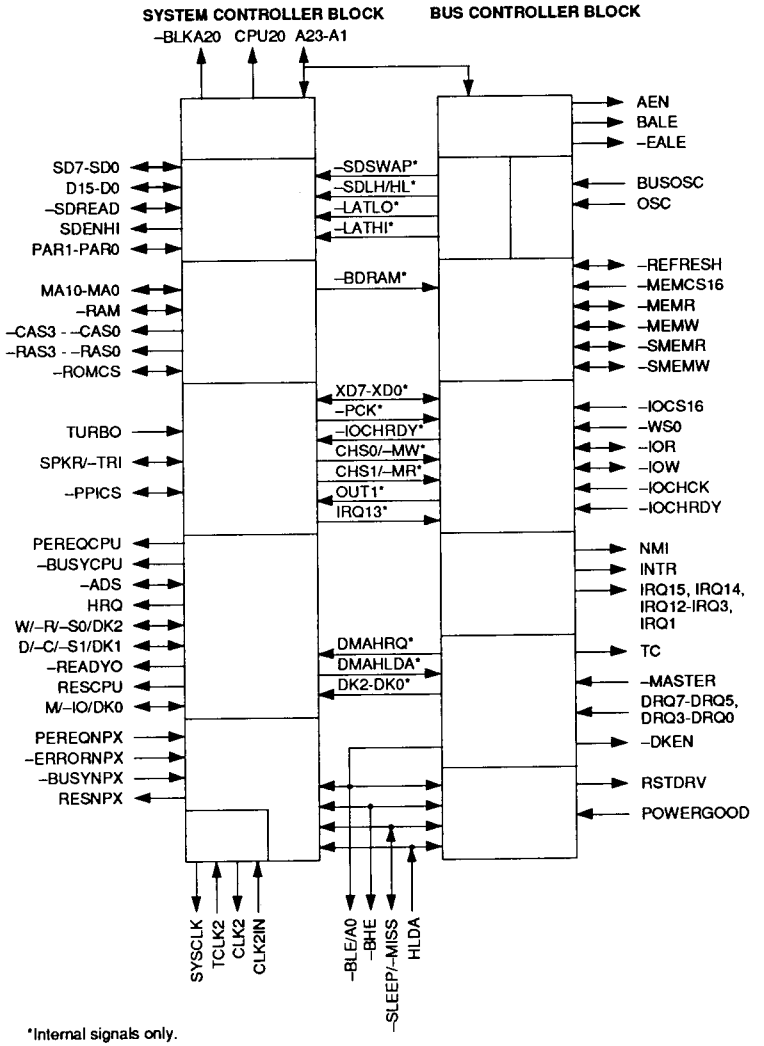
The VL82C310 and VL82C311 can be used with a 386SX or 286 processor. The VL82C311L can only be used with a 286 processor. The processor type has to be selected at power-on. The status of the pin –RAMW is strobed at power-on reset. If it is 1, 386SX is assumed to be connected. If –RAMW is held low, 286 cycles are initiated by the SCAMP Controller.

The SCAMP Controller handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the CPU's bus status and address signals, then decodes the bus access. The interface of the SCAMP Controller with a 286 and 386SX is shown in Figure 2.

Local Bus Accesses

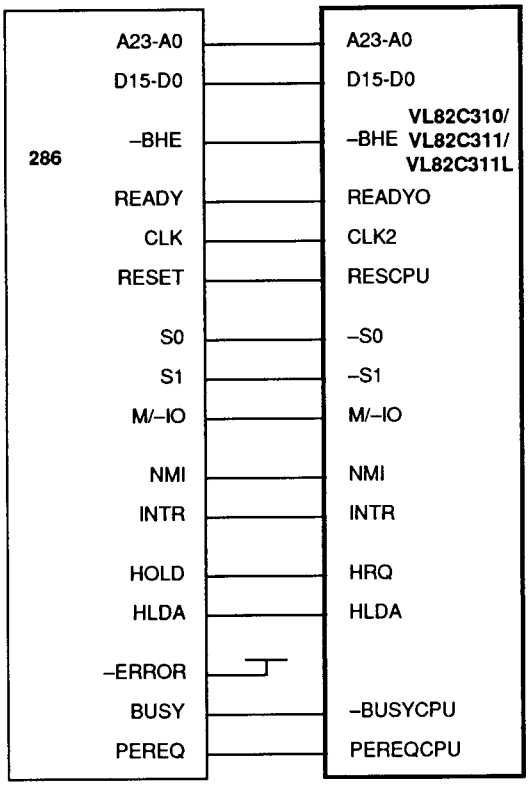
Upon receiving the CPU's bus status signals and address, the SCAMP Controller latches these signals with –ADS. (In 386SX Mode, this enables the CPU to continue with pipelined operation.) If the decoded address and M/–IO point to the on-board memory, a bank request is issued to the on-chip DRAM controller. The DRAM controller then delivers the appropriate signals to the on-board memory. It senses when the data has been transferred and returns a –READYO signal. –READYO is externally gated with ready signals from the coprocessor or other external

FIGURE 1. SCAMP CONTROLLER SUBSYSTEMS

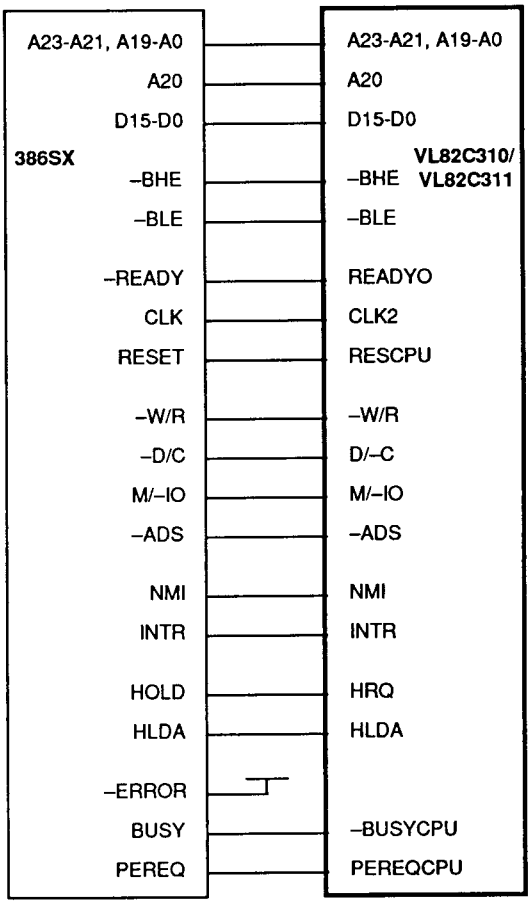


*Internal signals only.

FIGURE 2. CPU INTERFACE



INTERFACE WITH 286



INTERFACE WITH 386SX

devices on the D bus to form the final –READY signal driven to the CPU. This –READY signal is synchronized properly with the CPU's CLK2 signal.

Slot Bus Accesses
The CPU makes slot bus accesses when the SCAMP Controller decodes the CPU's control signals as either an I/O cycle or an off-board memory access (the latter includes ROM accesses). In this case, the SCAMP Controller latches and decodes the CPU's control signals and handles control of the slot transfer. The CPU is prevented from executing another slot cycle until the previous slot cycle is completed. During a slot cycle, the –READY signal returned to the CPU from the SCAMP Controller is delayed until the data transfer is over.

Bus Arbitration
The internal signals related to bus arbitration are DMAHRQ, DMAHLDA, and OUT1. The related external signals are HRQ and HLDA. When the DMAHRQ (DMA Hold Request) is generated by the internal DMA controllers, the hold request signal, HRQ, is synchronized with the CPU clock and relayed to the CPU. The CPU responds with HLDA (Hold Acknowledge) to the SCAMP Controller. In response, an internal signal DMAHLDA, which is an input to the DMA controllers, is generated and the bus control is transferred to either an internal DMA controller or an external Master.

During a refresh cycle, OUT1 is generated internally from a timer. HRQ is sent to the CPU and HLDA is returned to indicate the CPU has given up the bus for refresh cycles.

System Reset
System Reset occurs in response to the POWERGOOD signal.

There are three reset signals, RESCPU, RESNPX, and RSTDRV generated from the SCAMP Controller. The CPU reset signal, RESCPU, and the coprocessor reset signal, RESNPX, can be generated individually as described in later sections, or as a result of a system reset when RSTDRV is also generated.

The input signal POWERGOOD is low during power-on reset, but is not affected during a software reset. When a system reset is generated, the signal RSTDRV is enabled on the next high going edge of BUSOSC which in turn three-states –RAS and –CAS. When out of reset, POWERGOOD is inactivated if a hardware reset, and RSTDRV is also disabled. The –RAS and –CAS outputs are then activated on the fourth high-to-low transition of the –ADS input if operating in the 386SX Mode or the fourth high-to-low transition of the –S1 signal if operating in the 286 Mode. This is depicted in Figure 3.

CPU-Only Reset
A CPU reset without a coprocessor reset can occur for one of three reasons. Two ways are usually used for switching from the Protected Mode to the Real Mode. One way of achieving this is by setting bit 0 of I/O port 92h to a 1, or by a dummy read of I/O port EFh. There is a 6.72 µs delay between the occurrence of either of the first two events and activation of the RESCPU signal. The second way is to generate the internal signal –RC by writing FCh or FEh to I/O port 64h. The RESCPU signal is generated after either 6.72 µs or about 50 µs delay depending on the FASTRC bit of the MISCSET Register.

Internal detection of a shutdown command from the CPU also triggers a CPU-only reset. Shutdown commands are different for the 286 and 386SX.

In all the above cases, reset is also synchronized to CLK2 and lasts for 16 CLK2 cycles.

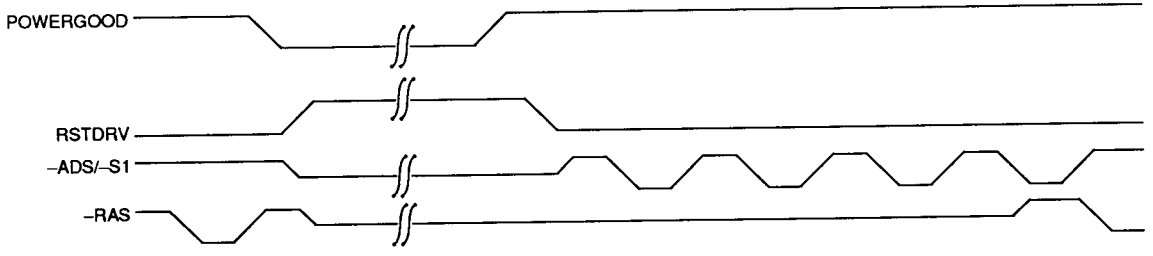
CPU Self-Test Request
The CPU self-test request is generated only at system reset. This is achieved by activating the signal –BUSYCPU at least eight CLK2 cycles before the falling edge of RESCPU and disabling it at least eight CLK2 cycles after that edge of RESCPU.

If a 386SX is used in the system, its self-test mode is triggered. This adds 33 ms (at 16 MHz) to the CPU reset time. At the end of the self-test, the BIOS can read the CPU self-test result register and perform whatever function is desired on failure. The CPU self-test request is generated in the 286 Mode also. However, the 286 does not have a Self-Test Mode and ignores the minimum 16 CLK2 period low signal on the –BUSYCPU pin.

Note that there is no self-test performed when CPU-only reset is invoked. This results in the faster execution of a "hot reset".

NUMERIC COPROCESSOR INTERFACE
The SCAMP Controller supports either the Intel i287™ or i387SX™ numeric coprocessors for use in high performance floating point math applications. In a 286-based system, only the 287

FIGURE 3. RESET SEQUENCE



may be used. Similarly, a 386SX system requires a 387SX coprocessor. It is not possible to mix CPUs and coprocessors.

If the system contains a coprocessor, the interface signals –ERRORNPX, –BUSYNPX, and PEREQNPX are sent from the coprocessor to the SCAMP Controller and decoded to produce the proper interface signals for the CPU. The same decode determines activation of the RESNPX output to the coprocessor. This interface provides PC/AT compatibility for use with the 287 or 387SX.

The SCAMP Controller contains several dedicated pins in order to provide the interface between the coprocessor and the CPU. Figure 4 shows the interface between the SCAMP Controller and the coprocessors. The processors and the coprocessors are designed to interface directly without external logic. However, logic is required in order to make a system hardware compatible with the PC/AT and software compatible with the PC/AT and original IBM PC.

Coprocessor-Only Reset Logic
For PC/AT compatibility, coprocessor-only reset is provided via a dummy I/O write to F1h. This action provides a reset to the coprocessor synchronized to CLK2 of an 80 CLK2 cycle duration. –READYO goes active 50 CLK2 cycles after the falling edge of RESNPX once a dummy write to F1h is performed. There may be incompatibility with some software due to the fact that a hardware reset does not put a 387SX into the same internal state as does a reset of the 287. For this reason, the F1h reset function may be disabled by setting Configuration Register MISCSET bit 6 = 1.

Error/Interrupt Logic
–ERRORNPX, when active, generates IRQ13 for PC/AT compatibility. It also latches –BUSYCPU. This is done in order to prevent the CPU from attempting to use the coprocessor until the error handling interrupt routine is executed. The interrupt handler inactivates the latched –BUSYCPU by performing a dummy write to I/O port F0h.

Busy Logic
There are three sources generating the –BUSYCPU signal. It is always activated in response to the –BUSYNPX input. It is also generated by latching the –ERRORNPX signal as described above and at system reset.

The state of –BUSYNPX is always passed through to –BUSYCPU indicating that the NPX is processing a command. On occurrence of an –ERRORNPX signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RESNPX. The former case is the normal mechanism used to reset the active latched signal. The latter two are resets. Since –ERRORNPX generates IRQ13, for PC/AT compatibility, –BUSYCPU is held active to prevent software access of the coprocessor until the interrupt service routine writes F0h.

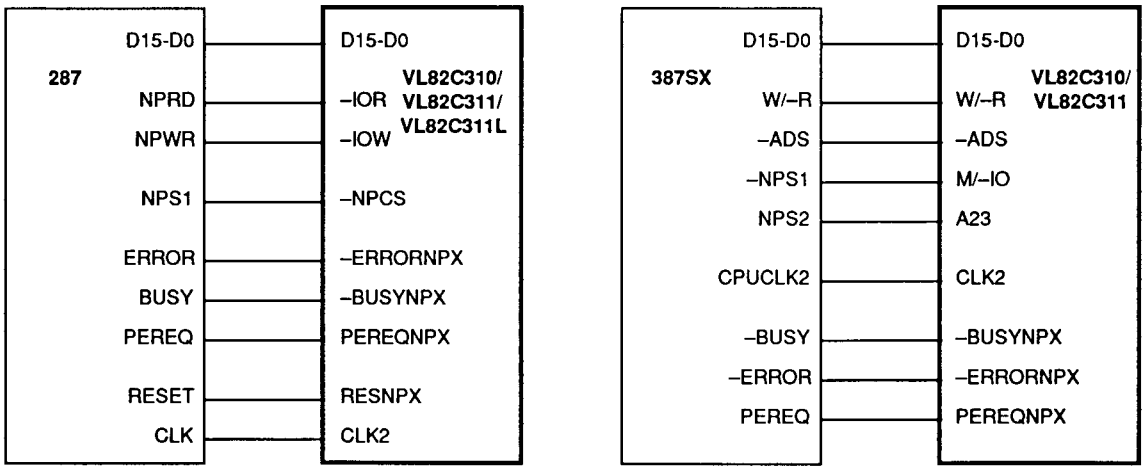
When a system includes a cache controller but not a numeric coprocessor, an access to the numeric coprocessor, especially during serial caching, can hang-up the system because the –BUSYCPU signal can not get activated since –ERRORNPX is disabled. The –BUSYCPU pin is toggled every refresh period (15.625 µs or 125 µs) to circumvent this problem.

PEREQ Logic
–BUSYNPX is latched in at the falling edge of the –ERRORNPX signal and ORed with the PEREQNPX signal to generate PEREQCPU signal.

The PEREQCPU signal reflects only PEREQNPX signal after a dummy write to the coprocessor busy clear register (I/O port F0h).

DRAM CONTROLLER
The DRAM Controller logic of the SCAMP Controller is designed for the optimum performance of the 286 and 386SX in a PC/AT environment. The SCAMP Controller supports up to 16 MB of 256K, 1M, or 4M DRAM in four 16-bit banks. The DRAM speed can be 60, 80, 100, or 120 ns.

FIGURE 4. NUMERIC COPROCESSOR INTERFACE



Both Page Mode and two-way block interleaving are supported. The drive current programmability of the memory address lines and control signals are beneficial in reducing ringing. RAS precharge control is also available in VL82C310 to lower DRAM operating power consumption.

Two Configuration Registers, RAMMAP and RAMSET, internal to the SCAMP Controller are used to control the memory map, DRAM timing, and Page Mode and Interleave Mode operations. These features are discussed in the following sections.

Since interleaving requires pairs of banks, various controls described below act on memory in bank pairs. The short hand notation Bank A is used when describing something that affects DRAM Banks 0 and 1 as a set. Similarly, Bank B is used to describe DRAM Banks 2 and 3 as a set.

DRAM Bank Configuration

There can be up to four 16-bit banks used with the SCAMP Controller. Each 16-bit bank of memory is further divided into two 8-bit banks. Each byte contains its own parity bit for a total of 18 bits per bank.

A single bank can consist of the following DRAM types:

Qty	DRAM Types Useable
18	256K x 1
18	1M x 1
18	4M x 1
6	four 256K x 4 + two 256K x 1
6	four 1M x 4 + two 1M x 1

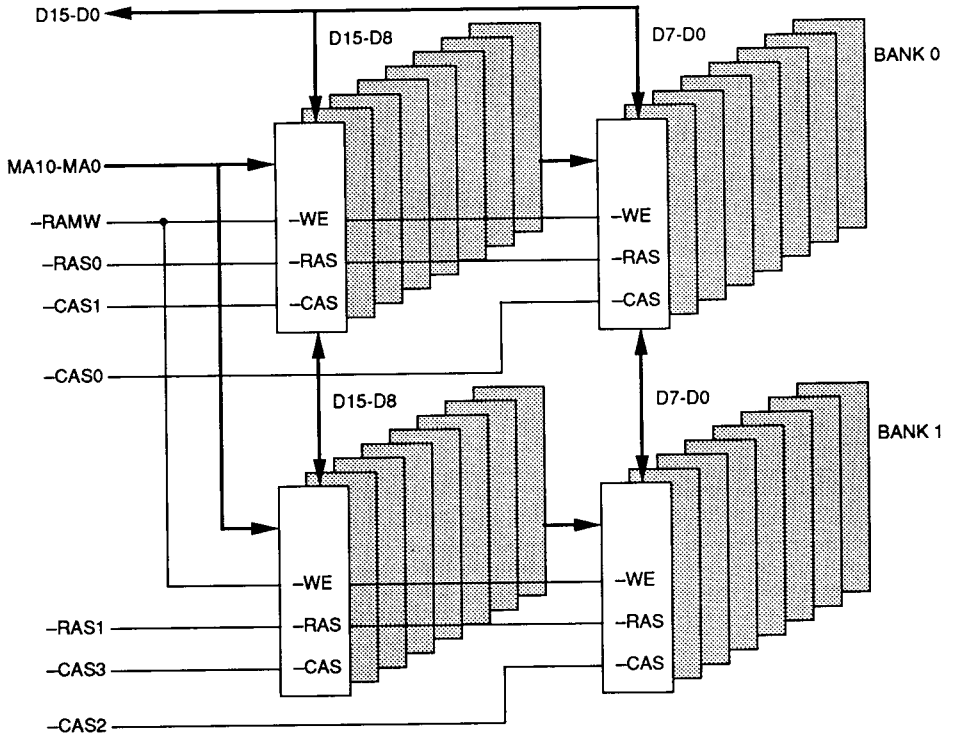
The parts used in multiple banks can consist of all one DRAM type or mixtures of two types. It is not possible to use all three types in a single system simultaneously and not all combinations of any two types are supported.

The SCAMP Controller provides four –RAS signals and four –CAS signals. They can be used directly to drive two banks as shown in Figure 5.

When the SCAMP Controller is used in a system to support four banks of DRAM, –CAS0 and –CAS1 are used to drive the lower byte and upper byte, respectively, of Banks 0 and 2, while –CAS2 and –CAS3 are used to drive those of Banks 1 and 3. This is depicted in Figure 6.

The drive of pins MA10-MA0 and –RAMW is determined at power-on reset by the state of the MA9 pin. If pulled low, 150 pF drive is selected. The drive is 300 pF if MA9 is pulled up. MA9 has to be either high or low at power-on reset. The drive of these pins can also be programmed by the RAMDRV bit of the MISCSET Register. It is a read/write bit and reflects MA9 at power-on reset.

FIGURE 5. TWO BANK DRAM SYSTEM

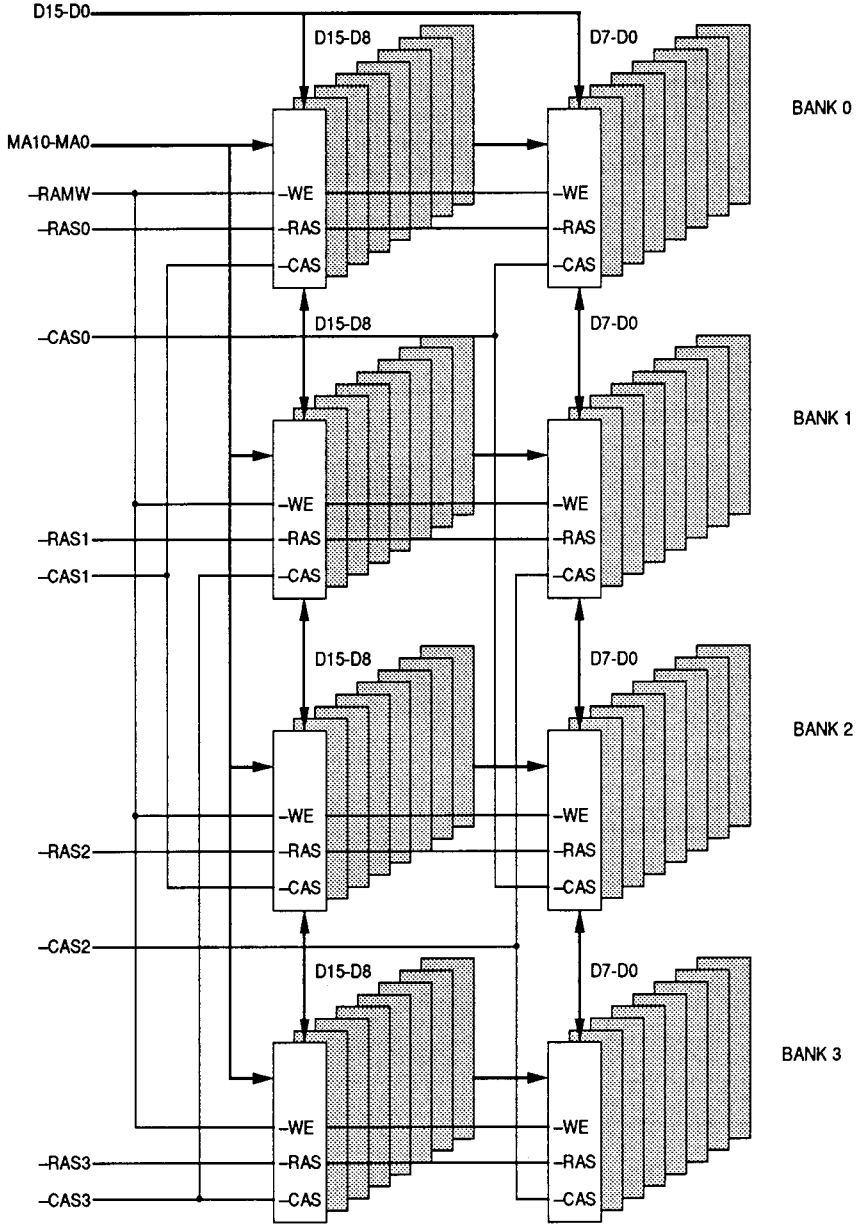


Memory Maps

The memory maps are selected by the Index Configuration Register RAMMAP. The SCAMP Controller supports 13 memory maps and two special cases. These maps are shown in Tables 1 and 2. The tables show the DRAM combinations that are addressable in each of four 16-bit memory banks. The RAMMAP3-RAMMAP0 column indicates the binary values written in bits 3-0 of the Indexed Configuration Register RAMMAP in order to select each map.

RAMMAP1 and RAMMAP0 indicate the number of populated banks when all the banks have similar DRAM types. RAMMAP3 and RAMMAP2 select DRAM type as follows.

FIGURE 6. FOUR BANK DRAM SYSTEM



RAMMAP3, RAMMAP2 =
00 = 256K
01 = 1M
10 = 4M
11 = Mixed DRAMS

RAMMAP1, RAMMAP0 =
00 = 1 Bank
01 = 2 Banks
10 = 3 Banks
11 = 4 Banks

When RAMMAP3 and RAMMAP2 = 11, RAMMAP1 and RAMMAP0 do not indicate the number of populated DRAM banks.

The memory map of Banks 0 and 1 when populated with 256K DRAM allows EMS and shadowing but no extended memory. A memory map with 0.5M total DRAM is the only case

TABLE 1. DRAM MEMORY MAPS

Bank 3	Bank 2	Bank 1	Bank 0	Total Memory (MB)	384K Remap?	RAMMAP3-RAMMAP0
			256K	0.5	No	0000
		256K	256K	1.0	Yes	0001
	256K	256K	256K	1.5	No	0010
256K	256K	256K	256K	2.0	Yes	0011
			1M	2.0	Yes	0100
		1M	1M	4.0	Yes	0101
	1M	1M	1M	6.0	No	0110
1M	1M	1M	1M	8.0	No	0111
			4M	8.0	No	1000
		4M	4M	16.0	No	1001
4M	4M	256K	256K	0.5/1.0/8.0/16.0	Note 1	Note 1
	1M	256K	256K	3.0	Yes	1100
1M	1M	256K	256K	5.0	No	1101
	4M	1M	1M	12.0	No	1110

Note 1: In this case, all the four banks may or may not be populated; Banks 3 and 2 may each have 4M, and Banks 1 and 0 may each have 256K DRAMS. 384K of memory can be remapped only when the lower two banks are populated with 256K DRAMS. When RAMMAP1 and RAMMAP0 is 00 or 01 (number of banks is 1 or 2), Banks 3 and 2 are ignored and depending on the RAMMAP1 and RAMMAP0 value either Bank 0 or Banks 0 and 1 are considered. If RAMMAP1 and RAMMAP0 is 10 or 11, the Banks 3 and 2 are remapped to the lower two banks. In this case, also depending on the RAMMAP1 and RAMMAP0 value, either Bank 0 (remapped Bank 2) or Banks 0 and 1 (remapped Banks 2 and 3) are considered, but the total memory is now 8M or 16M. This is shown in Table 2.

TABLE 2. DRAM MEMORY MAPS - SPECIAL CASE

Bank 3	Bank 2	Bank 1	Bank 0	Total Memory (MB)	384K Remap?	RAMMAP3-RAMMAP0
			256K	0.5	No	0000
		256K	256K	1.0	Yes	0001
	Remapped		4M	8.0	No	1010
Remapped	Remapped	4M	4M	16.0	No	1011

where there is no DRAM available for shadow, extended, or expanded memory. All other memory maps support shadow, expanded, and extended memory.

Page Mode and Interleave Mode Operations

Both Page Mode and Interleave Mode operations are available on the system board DRAM in order to raise performance and decrease system cost. Table 3 shows the Page Mode and Interleave Mode options available for each possible memory map. These options are selected by programming of the Configuration Registers RAMSET and RAMMAP. When the –PGMD bit is set to 0, paging is active on all memory maps for the enabled bank pairs. The Page Mode can also be activated by pulling MA6 low at power-on reset. Interleaving requires pairs of banks. Detailed operation of each mode is given in the following sections.

Interleave Mode Operation

If both banks of a pair are populated with like DRAM types, two-way block interleaving occurs on a 1K boundary. If the four banks are not populated with like DRAMS, two-way interleaving occurs on pairs that are of the same type. In a system with three banks populated, the first two banks interleave but the third does not. Table 4 shows the interleaving options that occur versus the number of populated banks. All combinations not shown are unsupported. There is no Configuration Register programmability for enabling the Interleave Mode. All interleaving options (none, or two-way) occur automatically as the result of the memory map programmed into RAMMAP.

TABLE 3. PAGE/INTERLEAVE VERSUS MEMORY MAP

16-Bit DRAM Banks				Page/Interleave				
B		A		Page Mode On		Page Mode Off		Total Memory
Bank 3	Bank 2	Bank 1	Bank 0	B	A	B	A	
			256K		Page		Linear	0.5M
		256K	256K		2/P*		2/NP	1.0M
	256K	256K	256K	Page	2/P	Linear	2/NP	1.5M
256K	256K	256K	256K	2/P	2/P	2/NP	2/NP	2.0M
	1M	256K	256K	Page	2/P	Linear	2/NP	3.0M
1M	1M	256K	256K	2/P	2/P	2/NP	2/NP	5.0M
			1M		Page		Linear	2.0M
		1M	1M		2/P		2/NP	4.0M
	1M	1M	1M	Page	2/P	Linear	2/NP	6.0M
1M	1M	1M	1M	2/P	2/P	2/NP	2/NP	8.0M
	4M	1M	1M	Page	2/P	Linear	2/NP	12.0M
			4M		Page		Linear	8.0M
		4M	4M		2/P		2/NP	16.0M

*Two-way interleaving on page boundary of 1K.

TABLE 4. AUTOMATIC INTERLEAVE VS POPULATED BANKS

Populated?		Bank B Address Mode	Populated?		Bank A Address Mode
Bank 3	Bank 2		Bank 1	Bank 0	
No	No	N/A	No	Yes	Linear
No	No	N/A	Yes	Yes	2-Way Interleave
No	Yes	Linear	Yes	Yes	2-Way Interleave
Yes	Yes	2-Way Interleave	Yes	Yes	2-Way Interleave

Tables 5, 6, and 7 show how the CPU address lines are used to accomplish the interleave options possible with the three supported DRAM types. The top portion of each table shows the CPU address lines that are strobed onto MA10-MA0 by –CAS, the column address strobe. The middle portion of each table shows the CPU address lines strobed onto MA10-MA0 by –RAS, the row address strobe. The bank select box shows the CPU address bit(s) used for interleaving. The bank enable decodes further qualify whether the CPU address is in the range of current memory map.

Page Mode Operation

Page Mode is controlled by the bit –PGMD in the Configuration Register RAMSET. When low, this bit enables Page Mode operation on all DRAM banks. The Page Mode can also be enabled at power-on reset by pulling MA6 low. When activated for a bank pair, the Page Mode is active whether one bank or both are populated.

The Page Mode operation results in no additional wait state penalty for either read or writes which immediately follow reads to the same DRAM page. A page-miss causes a two wait state penalty if a bank-hit, and a one wait state penalty if a bank-miss.

When pairs of banks are installed, interleaving is automatically enabled. The combination of Page Mode with interleaving results in the best possible combination of fast system memory operation using the most cost-effective DRAMs. When accesses between interleaved banks occur, CAS precharging of the next bank to be accessed occurs while –CAS is active on the current bank. This has the effect of multiplying the effective page size by the number of banks being interleaved, thus increasing the odds of page-hit cycles.

RAS Shut-Off
(VL82C310 Feature Only)

In a DRAM system, the row addresses are put on the memory address lines first. One of the –RAS signals is then used to latch in this address. The column address appears after it, and is latched in with a –CAS signal. In a bank-hit/page-hit cycle, only a new column address is required because the

TABLE 5. 256K DRAM PAGE/ INTERLEAVE MAPPING

	No Interleave	2-Way Block Interleave	Memory Address
Column Address	3	3	0
	4	4	1
	5	5	2
	6	6	3
	7	7	4
	8	8	5
	9	9	6
	1	1	7
	2	2	8
			9
			10
Row Address	18	18	0
	17	17	1
	16	16	2
	15	15	3
	14	14	4
	13	13	5
	12	12	6
	11	11	7
	10	19	8
			9
			10
Bank Selects	19	10	
Bank Enable Decode	20	20	

TABLE 6. 1M DRAM PAGE/ INTERLEAVE MAPPING

	No Interleave	2-Way Block Interleave	Memory Address
Column Address	3	3	0
	4	4	1
	5	5	2
	6	6	3
	7	7	4
	8	8	5
	9	9	6
	1	1	7
	2	2	8
	10	11	9
			10
Row Address	18	18	0
	17	17	1
	16	16	2
	15	15	3
	14	14	4
	13	13	5
	12	12	6
	11	20	7
	19	19	8
	20	21	9
			10
Bank Selects	21	10	
Bank Enable Decode	22	22	

TABLE 7. 4M DRAM PAGE/ INTERLEAVE MAPPING

	No Interleave	2-Way Block Interleave	Memory Address
Column Address	3	3	0
	4	4	1
	5	5	2
	6	6	3
	7	7	4
	8	8	5
	9	9	6
	1	1	7
	2	2	8
	10	11	9
	11	12	10
Row Address	18	18	0
	17	17	1
	16	16	2
	15	15	3
	14	14	4
	13	13	5
	12	12	6
	20	20	7
	19	19	8
	21	21	9
	22	23	10
Bank Selects	23	10	
Bank Enable Decode			

successive memory accesses are in the same page. A new –CAS edge needs to be generated for this purpose but there is no need for a new –RAS edge as shown in Figure 7.

However, a new –RAS edge is required when the successive memory accesses are in different pages or different banks. If the accesses are in the same bank (page-miss cycle), the same –RAS (–RAS0 in Figure 7) signal requires a new edge. If a bank-switch occurs, a new edge should be on the other –RAS line (–RAS1 in Figure 7). The –RAS line has to be negated before a new edge can occur. The time from which it is negated to the time when a low going edge occurs is called RAS precharge time which typically is a considerable portion of the DRAM access time.

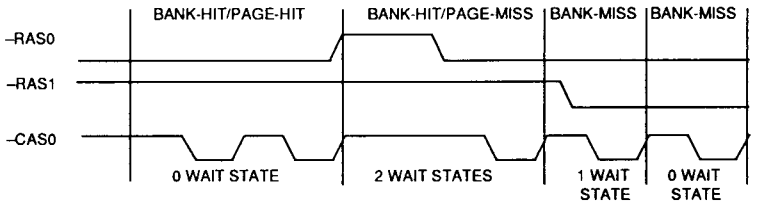
The bank-miss cycles are faster than the page-miss/bank-hit cycles because a different –RAS line can be activated as soon as a miss occurs. In the page-miss/bank-hit cycles, the same –RAS line has to be precharged and then pulled low which is slower. In the VL82C310, a bank-miss cycle has one wait state while a page-miss/bank-hit cycle has two wait states.

In a normal Page Mode operation, both the –RAS lines are kept active when a bank-miss occurs. This expedites the memory accesses because there is no RAS precharge penalty. However, there is a price to be paid in higher power consumption. A DRAM bank consumes more power when RAS is active. This can be of disadvantage in the Power Saving Mode. The power consumption is reduced by enabling the RASOFF bit in the RAMSET Register. This activates only one –RAS line and hence, power is consumed in only one DRAM bank. The saving in power consumption is achieved at the expense of a slight loss in overall memory system performance.

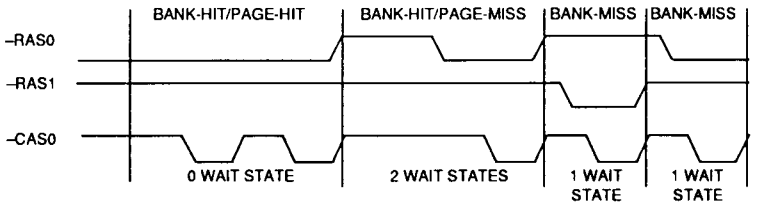
DRAM Refresh

The SCAMP Controller supports the PC/AT-compatible Refresh Mode with a refresh period of 15.625 µs and the slow Refresh Mode with refresh period of 125 µs. In the slow Refresh Mode, the time to refresh the entire DRAM is 64 ms instead of the standard 4 ms. It performs on-board DRAM refresh and controls both on-board and off-board refresh timing. Refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. A register, Refresh Control Register REFCTL, is provided to select the refresh period.

FIGURE 7. RAS SHUT-OFF



RASOFF BIT DISABLED FOR NORMAL OPERATION



RASOFF BIT ENABLED FOR POWER SAVING

System Board Refresh

The entire system board DRAM is refreshed every 4 ms or every 64 ms as programmed by the REFSPD bit in the REFCTL Register. The refresh cycle can be RAS-only refresh or CAS-before-RAS refresh as selected by the bit CASREF. The type of refresh cycle should be programmed at power-on and the bit CASREF should not be altered during the normal operation.

Off-Board DRAM Refresh

The SCAMP Controller contains all the control circuitry necessary to generate a refresh cycle for the off-board DRAMs. The –MEMR signal will go low a minimum of one SYSCLK cycle after –REFRESH goes low. –MEMR will stay low for two SYSCLK cycles unless extended by –IOCHRDY. A low on –IOCHRDY will extend the –MEMR and –REFRESH pulse until –IOCHRDY is returned high.

A 12-bit refresh address counter is included in the SCAMP Controller. The address is driven onto the address lines A11-A0. The signals A16-A12 are driven to 1 while the contents of the page register 74LS612 are driven on the lines A23-A17. The address lines A7-A0 are latched on to the slot bus SA7-SA0 using external latches. At the end of the refresh cycle, when –REFRESH goes high, the counter is incremented to the next refresh address.

DRAM REGISTERS

DRAM MAP REGISTER (RAMMAP)

The 8-bit Index Configuration Register RAMMAP is used to select a memory map and remap a portion of the memory to the top of the existing memory.

RAMMAP Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (03h)	1	RAMMOV1, RAMMOV0		REMP384	MEMAP3	MEMAP2	MEMAP1	MEMAP0
POR Values	1	MA8	MA7	MA4	MA3	MA2	MA1	MA0

Bit	Name	Function
7		Reserved: This bit is read-only and always returns logic 1.
6-5	ROMMOV1, ROMMOV0	System and Slot ROM Move bits 1-0: These bits relocate video ROM and fixed disk ROM, address range C0000h-CFFFFh, to the system board, and move the on-board ROM space E0000h-EFFFFh to the slot address range. The initial power-on reset value of these bits are set the same as pins MA8 and MA7 at the end of the reset period. Refer to the section "Relocating System and Slot ROM" for more details.
4	REMP384	Remap 384K Memory: This bit, when set, remaps 384K memory to the top of the current memory map. The remapping option is available only if the total memory is 1M, 2M, 3M, or 4M. The initial power-on reset value of this bit is set the same as pin MA4 at the end of the reset period. This bit is disabled if the total memory is not 1M, 2M, 3M, or 4M. Remapping is explained in the section "Remapping of Memory Range A0000h-FFFFh."
3-0	MEMAP3-MEMAP0	DRAM Memory Map 3-0: These bits specify one of the valid memory maps shown in Tables 1 and 2. The initial power-on reset value of these bits are set the same as pins MA3-MA0 at the end of the reset period.

DRAM CONTROL REGISTER (RAMSET)

The Index Configuration Register RAMSET is used to select the Page or non-Page Mode operation, to enable parity checking, and select the drive current on the memory address lines MA10-MA0 and –RAMW pin.

RAMSET Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (05h)	1	1	1	DRAMWS	–FASTSX	–PGMD	–ENPAR	RASOFF
POR Values	1	1	1	MA5	0	MA6	0	0

Bit	Name	Function
7-5		Reserved: These bits are read-only and always returns logic 1.
4	DRAMWS	DRAM Wait States: This bit controls the number of wait states to be inserted in each DRAM access. A wait state is defined as two CLK2 periods. When this bit is high, one wait state is inserted. When this bit is low, zero wait state is inserted. The initial power-on reset value of this bit is set the same as MA5 at the end of the reset period.
3	–FASTSX	Fast Page-Miss/Bank-Hit Cycles for 386SX: This bit, in conjunction with DRAMWS bit, decides the number of wait states to be introduced in page-miss/bank-hit DRAM access cycles in a 386SX-based system as follows: DRAMWS –FASTSX 0 0 2 Wait States 0 1 3 Wait States 1 X Don't Care The default value of this bit is 0.
2	–PGMD	Page Mode Banks A and B: This bit indicates whether Page Mode is active on Banks A (0 and 1) and B (2 and 3). The Page Mode is disabled when –PGMD is set to 1. Resetting this bit to 0 enables the Page Mode. The initial power-on value of this bit is set the same as MA6 pin at the end of the reset period.
1	–ENPAR	Enable Parity: When low, enables parity generation and checking, and disables it when high. The power-on reset default of this bit is 0.
0	RASOFF	RAS Shut-off: This bit, when set, enables only one –RAS line and disables all the other unused –RAS lines when a bank-miss occurs. When 0, it allows two –RAS lines to be active when a bank-miss occurs. The power-on default value of this bit is 0. (Available in the VL82C310 only.)

REFRESH CONTROL REGISTER (REFCTL)

The Refresh Control Register is used for programming the Refresh Mode and for selecting a slow or standard refresh period.

REFCTL Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
REFCTL (06h)	1	1	1	1	1	1	CASREF	REFSPD
POR Values	1	1	1	1	1	1	0	0

Bit	Name	Function
7-2		These bits are read-only and always returns logic 1.
1	CASREF	Enable CAS-Before-RAS Refresh: This bit, when set, enables CAS-before-RAS refresh. RAS-only refresh is selected if CASREF is 0. The default value of this bit is 0.
0	REFSPD	Refresh Period: This bit determines the refresh period. If set to 1, it enables slow Refresh Mode in which a refresh cycle occurs every 125 µs. When 0, PC-AT Standard Mode is selected and the refresh period is 15.625 µs. The default value of this bit is 0 selecting the standard refresh rate.

ADDRESS MAPPER/DECODER

The SCAMP Controller offers several address mapping and decoding options for better system performance and flexibility. The available options include a slot pointer, ROM/EPROM shadowing, mapping of 384K memory to the top of the available physical memory, JEIDA IC Memory Card support, and EMS support.

SLOT POINTER (SLTPTR)

The slot pointer sets the 64K boundary between 256K and 16M above which CPU addresses are directed to the AT slot bus. Eight bits are required to specify this range. They are compared with the address lines A16-A23. Any system board memory from 1MB up to SLTPTR is accessible as on-board extended memory. The slot bus DRAM extended memory resides from SLTPTR up to 16MB in SCAMP Controller.

SLTPTR can also be set below 1MB when the on-board EMS backfill system is disabled. The minimum valid value for SLTPTR is 00h to facilitate the use of SRAM. The bank select signals internal to the device are disabled resulting in inactive –RAS and –CAS lines when SLTPTR is 00h. The SLTPTR can not have values 01h, 02h, and 03h. For this reason, at least one bank of 256K RAM must be on the system board on reset for a physical memory size of 512K bytes. The next valid value for SLTPTR is 04h to allow slot memory cards, especially EMS capable boards, to backfill down to 256K. This capability is provided for users who prefer not to use the built-in EMS system. Any value between 04h and 09h makes the portion of system board DRAM from that address to A0000h inaccessible when the on-board EMS system is inactive. The useable values for SLTPTR are 04h-FDh. A value of FEh or FFh results in

SLTPTR Register - Read/Write

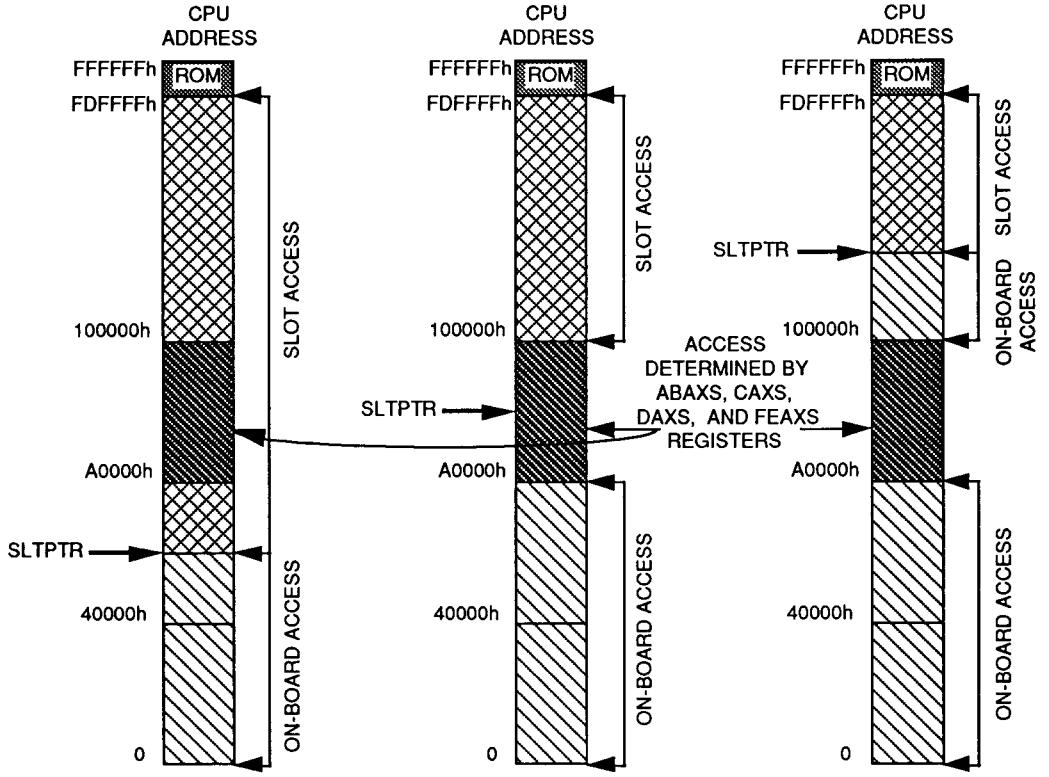
Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SLTPTR (02h)	A23	A22	A21	A20	A19	A18	A17	A16
POR Values	1	1	1	1	1	1	1	1

no off-board accesses since CPU accesses in the FE0000h and FF0000h segments always result in ROM chip selects. Any out of range value is treated the same as FFh. Refer to Table 8 and Figure 9 for more on the effect of the slot pointer.

TABLE 8. EFFECT OF SLOT POINTER

Slot Pointer Value	Slot Pointer Location	Effect
0004h-0009h	256K-640K	CPU addr 0h to SLTPTR = > system board access, CPU addr SLTPTR to 640K and 1M to 16M = > slot bus, CPU addr 640K to 1M = > determined by ABAXS, CAXS, DAXS, FEAXS Registers, CPU addr > 16M = > no accesses.
000Ah-000Fh	640K-1M	Respond as if SLTPTR = 0010h (see next case).
0010h-00FFh	1M-16M	CPU addr 0 to 640K = > system board accesses, CPU addr 640K to 1M = > determined by ABAXS, CAXS, DAXS, FEAXS Registers, CPU addr 1M to SLTPTR = > system board access. CPU addr SLTPTR to 16M = > if value 10h-FDh then slot bus else ROM. CPU addr > 16M = > no access.

FIGURE 8. EFFECT OF SLOT POINTER



It should be noted that the slot pointer must point to 1M or higher (≥10h) if use of the EMS Backfill Registers is required. Pointing SLTPTR below 640K and using the Backfill Registers is incompatible. Therefore, any time the SLTPTR is set between 00h and 09h the EMS Backfill Register enable bit in Configuration Register EMSEN1 is cleared. A smart BIOS set up routine does not allow this condition in actual operation.

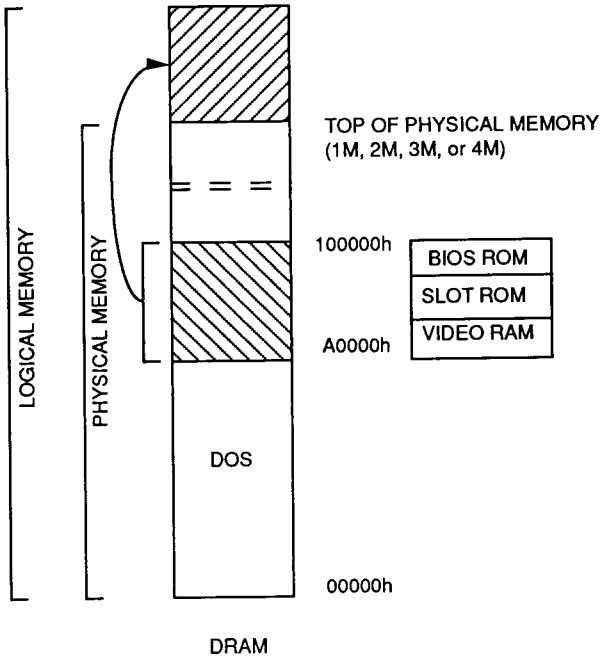
Remapping of Memory Range A0000h-FFFFFh

DOS utilizes 640K memory from address locations 00000h to 9FFFFh. The memory range from A0000h to FFFFFh is used for video RAM, BIOS ROM, video BIOS, etc. If a system has more than 640K DRAM, the DRAM between A0000h and FFFFFh can be accessed directly by enabling read and/or write shadow RAM. This 384K of DRAM can be remapped to another memory range to also be utilized.

Remapping of memory between A0000h and FFFFFh is achieved with bit REMAP in the Indexed Configuration Register RAMMAP. The SCAMP Controller allows remapping of this memory only if the total system DRAM memory is 1M, 2M, 3M, or 4M. The 384K of memory is then remapped to the top of the system memory as shown Figure 9.

EMS and shadow RAM are unavailable in this mode if the system memory is 1M. For 2M, 3M, and 4M memory, shadow RAM is not available if this mode is activated. However, EMS support is still available.

FIGURE 9. REMAPPING OF 384K DRAM



Relocating System and Slot ROM

A PC/AT motherboard normally includes 640K DRAM located in the address range from 00000h to 9FFFFh, and 128K ROM residing from E0000h to FFFFFh. The memory accesses from A0000h to DFFFFh are directed towards the slots. The video buffers occupy memory space from A0000h to BFFFFh while C0000h to DFFFFh is available for installable ROM (e.g., video ROM, fixed disk ROM). In PC/AT, BIOS ROM is located from F0000h to FFFFFh. The ROM locations E0000 to EFFFFh are available for other purposes. The VL82C310 offers flexibility of having video ROM and fixed disk ROM either on the system board or on the slot bus.

The video ROM and the fixed disk ROM, memory range C0000h to CFFFFh, can be relocated to the on-board ROM range with the bits ROMMOV1 and ROMMOV0 in the RAMMAP Register. Similary, the on-board memory range E0000h to EFFFFh can be moved to the slots by the same bits. This is achieved at power-on reset by configuring these bits with MA8 and MA7 pins. The two bits can also be controlled by software. Refer to Table 9.

Note: The DRAM mapping is not affected by these bits. Also note that on-board ROM means that the signal –ROMCS is generated and data is read from the D bus.

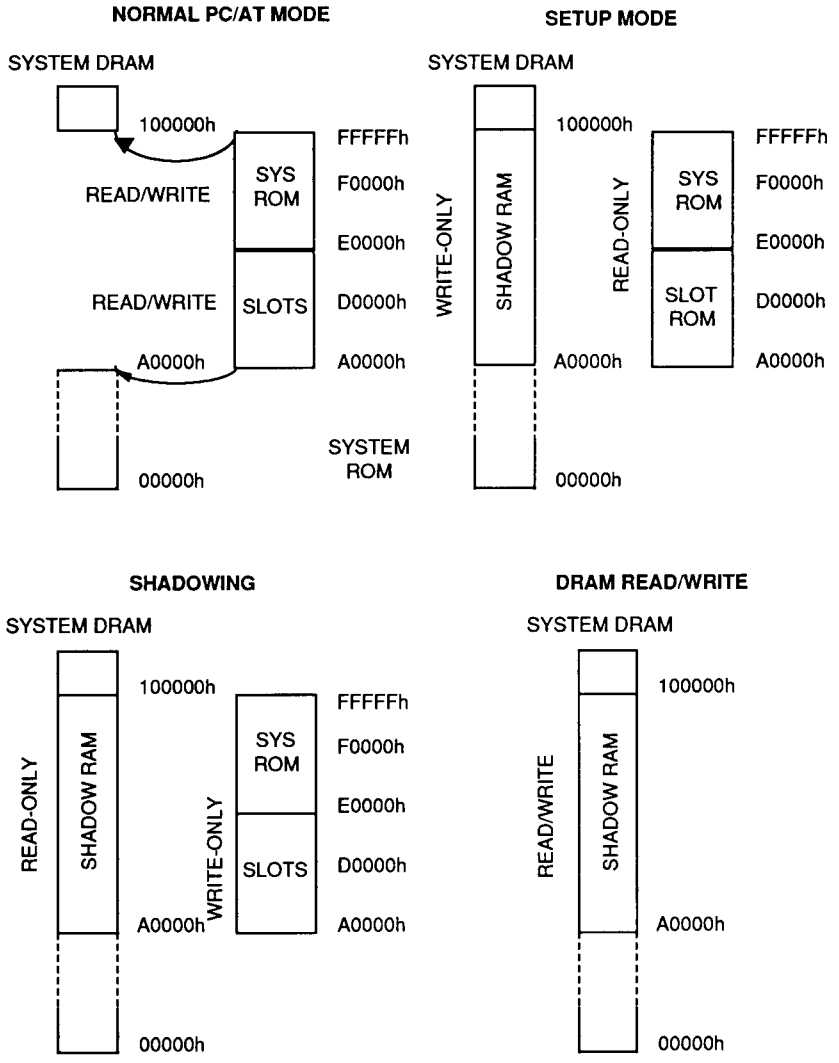
TABLE 9. RELOCATION OF SYSTEM AND SLOT ROM

ROMMOV1, ROMMOV0	00	01	10	11
E8000h	On-board ROM	Slot bus	On-board ROM	Slot bus
E0000h	On-board ROM	Slot bus	Slot bus	Slot bus
C8000h (fixed disk ROM)	Slot bus	Slot bus	Slot bus	On-board ROM
C0000h (video ROM)	Slot bus	Slot bus	On-board ROM	On-board ROM

SHADOWING

For better performance, data from slow memory devices like ROM is copied into RAM to speed up memory accesses. This is called shadowing. The SCAMP Controller supports shadowing of the BIOS ROM and the installable slot ROM (also called adapter ROM).

FIGURE 10. SHADOW RAM CONTROL



Four Indexed Configuration Registers are provided to give complete control over each of the 64K memory segments between A0000h and FFFFFh. The registers are called ABAXS, CAXS, DAXS, and FEAXS. Registers CAXS and DAXS contain two bits for each 16K segment in the memory address range C0000h and DFFFFh while ABAXS and FEAXS contain two bits for each 32K segment in the memory ranges A0000h-BFFFFh and E0000h-FFFFFh, respectively.

Shadowing can be enabled by writing 10 in the two bits provided for each segment. Each segment can be enabled independent of the other segment. The ROM contents should be copied to the DRAM before shadowing is enabled. The two bits should be set to 01 for this purpose.

Shadowing is disabled when remapping of 384K memory (A0000h-FFFFFh) is selected.

Shadowing Indexed Configuration Registers

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
ABAXS (0Eh)	B8000 Access		B0000 Access		A8000 Access		A0000 Access	
CAXS (0Fh)	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
DAXS (10h)	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
FEAXS (11h)	F8000 Access		F0000 Access		E8000 Access		E0000 Access	
POR Values	0	0	0	0	0	0	0	0

The two bits for each segment select four modes as follows:

1. 00 Read/Write Slot Bus (Default)
   Normal PC/AT compatible operation. This may be R/W slot bus or ROM chip select depending on the memory space.
2. 01 Setup Mode: Read Slot Bus, Write System Board
   Shadow setup mode. In the E0000 and F0000 segments reads cause on-board ROM chip selects and writes to the same address are to system board DRAM. In the segments C0000-D0000 reads are from the slot bus and writes are to system board DRAM. This allows shadowing of system board ROM as well as ROMs on a slot card.
3. 10 Read System Board/Write Slot Bus
   Read-only DRAM. This is the normal shadow operational mode though it could be used to protect data previously written to a memory area while configured for Mode 2. In this mode, writes are directed to the slot bus.
4. 11 Read/Write System Board
   R/W system board DRAM. This allows complete access to DRAM in the given 16K or 32K region.

EMS SYSTEM

The original PC/XT design had an address limit of 1M due to the type of processor used. It is possible to address more than 1M of memory with a 286 or a 386SX. Expanded Memory Specification (EMS) exploits this additional memory by mapping CPU addresses below 1M to memory above 1M in 16K blocks.

Out of 1M memory, the first 256K (00000h-3FFFFh) is reserved as system memory, 128K memory from A0000h to BFFFFh is used as video memory, the uppermost 64K (F0000h-FFFFFh) is reserved for ROM BIOS. That leaves two areas of memory, 40000h-9FFFFh and C0000h-EFFFFh, mappable to EMS.

The SCAMP Controller supports the LIM EMS 4.0 specification with any of the valid memory maps of 1M bytes and higher. The EMS system consists of 36 Mapping Registers. The SCAMP Controller is capable of translating addresses via the EMS Registers over the entire 16 MB range of possible system board memory. The mapping registers hold addresses of the memory locations above 1M which are mapped to the 16K blocks in the range 40000h-9FFFFh and C0000h-EFFFFh. This is shown in Figure 11.

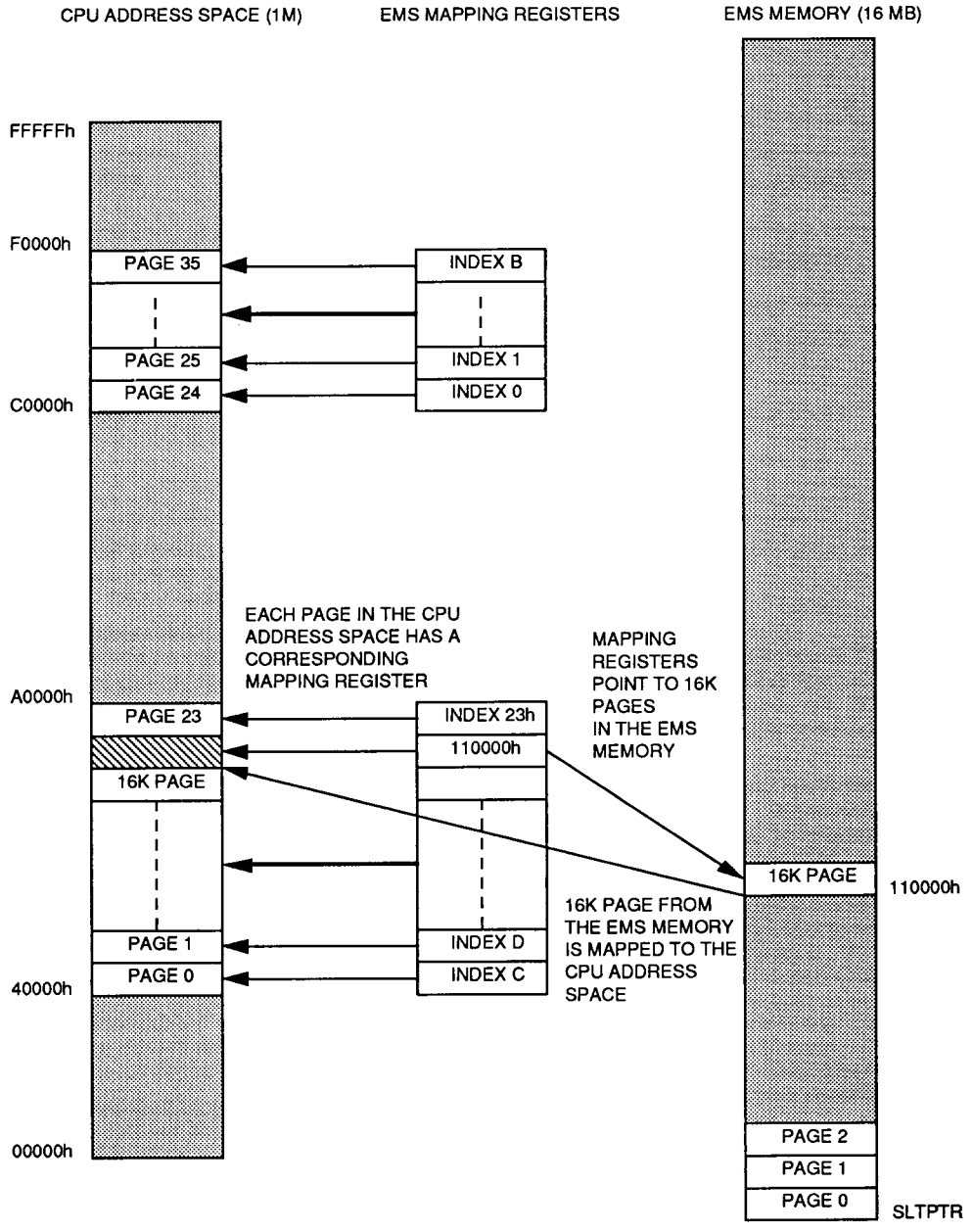
The EMS Mapping Registers are split into two parts, the 12 primary EMS Page Registers which cover the range C0000h-EFFFFh and the 24 backfill registers that cover 40000h-9FFFFh.

When the Backfill EMS Registers are not used, the EMS driver allocates all memory above SLTPTR for EMS page memory. It also can use the system board memory at the same addresses

as the enabled EMS Page Registers and any other 32K segment in the A0000h-BFFFFh and F0000h-FFFFFh area for which the shadow code is 00 (read/write slot bus) as set in Configuration Registers ABAXS and FEAXS, respectively. When the Backfill Registers are active, EMS pages can also be allocated for all system board memory from 40000h to 9FFFFh.

There is no wasted DRAM in a SCAMP Controller-based system. All memory not allocated for other purposes can be used as expanded memory.

FIGURE 11. EMS MAPPING



EMS Index Register and EMS Data Ports

Table 10 shows a programmer's model of the register set. Registers 0h-Bh are called the EMS Page Registers. Registers 0Ch-23h are the Backfill Registers. The register set is accessed by writing a byte to the Index Register located at I/O address E8h. Bits D0-D5 contain the address of the desired EMS Register from 0 to 35. Setting bit D6 to a 1 activates auto-increment. I/O port

TABLE 10. EMS INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
	1	Auto-Inc	A5	A4	A3	A2	A1	A0
		0 = Off 1 = On						

Index Port	Page Segment	Data Port (EBh) D15	D14	D13	D12	D11	D10	D9	D8	Data Port (EAh) D7	D6	D5	D4	D3	D2	D1	D0
0	C0/A0	1*	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1	C4/A4	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
2	C8/A8	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
3	CC/AC	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
4	D0	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
5	D4	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
6	D8	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
7	DC	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
8	B0/E0	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
9	B4/E4	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
A	B8/E8	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
B	BC/EC	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
C	40000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
D	44000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
E	48000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
F	4C000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
10	50000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
11	54000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
12	58000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
13	5C000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
14	60000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
15	64000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
16	68000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
17	6C000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
18	70000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
19	74000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1A	78000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1B	7C000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1C	80000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1D	84000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1E	88000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1F	8C000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
20	90000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
21	94000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
22	98000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
23	9C000	1	1	1	1	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14

*Reserved bits; that read back as logic 1.

addresses EAh and EBh then provide a window into the Page Register specified in the Index Register. Address EAh allows access to A21-A14. EBh allows access to A23-A22. 16-bit I/O reads and writes can be used to gain access to A23-A14 in one operation via address EAh.

After initial accesses to data ports at EAh and EBh subsequent accesses are to the same Page Register until a new register number is written to the lower six bits of the Index Port at port address E8h or unless bit D6 of the Index Port was previously set to a logic 1. In this case, any access to Data Port at EBh increments the Page Register number. This new value is seen by a read to the Index Port (E8h). The next read or write is to the next sequential Page Register. This feature allows the entire register set to be changed with a single access to the Index Register.

For byte accesses, the lower byte at port address EAh must be written first. The access to the upper byte at EBh causes an auto-increment. Since all word accesses are made to port EAh, each access causes an auto-increment. This is due to the fact that the SCAMP Controller actually breaks the word into two byte chunks, writing EAh followed by EBh.

The auto-increment feature speeds the already fast hardware driven context switching capability by minimizing the number of software instructions and, therefore, machine cycles required to read and save one context of the EMS Registers, then retrieve and write another.

EMS Configuration Registers
The EMS system has two Configuration Registers available to enable 12 EMS Page Registers globally, as well as individually, to control 24 Backfill Registers globally, and to remap the memory range used by LIM EMS 4.0.

Each of the 12 registers can then be individually disabled if there are system address conflicts. Bits 3-0 of EMSEN1 and 7-0 of EMSEN2 provide this function.

If a full LIM 4.0 EMS system is desired, both bits 6 and 7 of EMSEN1 are set as are the desired EMS Page Register enable bits.

EMS Configurations Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
EMSEN1 (0Bh)	EMSENAB	BFENAB	1	EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
POR Values	0	0	1	0	0	0	0	0
EMSEN2 (0Ch)	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
POR Values	0	0	0	0	0	0	0	0

Bit	Name	Function
EMSEN1 Bit 7	EMSENAB	Enable EMS: This bit is a global enable for the EMS Page Registers. When EMSENAB is 1, the EMS Page Registers are enabled.
EMSEN1 Bit 6	BFENAB	Enable Backfill: The 24 EMS Backfill Registers are enabled by setting this bit. No individual control is provided for these 24 registers. This bit is cleared when SLTPTR is set to a value from 0004h to 0009h.
EMSEN1 Bit 5		This bit is read-only and always returns logic 1.
EMSEN1 Bit 4	EMSMAP	EMS Mapping: The normal EMS Page Register mapping to C0000h-EFFFFh can be altered by setting bit EMSMPA. The 12 Page Registers then map to AXXXXh, BXXXXh, and DXXXXh. The EMSEN1 bits 3-0 are used to enable or disable the BXXXXh Registers rather than the EXXXXh Registers. Similarly, EMSEN2 bits 3-0 enable or disable the AXXXXh Registers rather than the CXXXXh Registers.
EMSEN1 Bits 3-0 EMSEN2 Bits 7-0		Enable EMS Page Register: The EMSEN1 bits 3-0 are used to enable or disable the EMS Page Registers associated with the memory range B0000h-BFFFFh and E0000H-EFFFFh at 16K boundaries. Similarly EMSEN2 bits 3-0 control the registers for range A0000h-AFFFFh and C0000h-CFFFFh, and EMSEN2 bits 7-4 control those for D0000h-DFFFFh. When set, these bits enable the related EMS Page Registers. EMSEN1 bits 3-0 control the EMS Page Registers for the range E0000h-EFFFFh if EMSMAP bit is 0 and the registers for B0000h-BFFFFh if EMSMAP = 1. Similarly for EMSEN2 bits 3-0 EMSMAP = 0 enables control of C0000h-CFFFFh range and EMSMAP = 1 allows control of A0000h-AFFFFh range.

Effect of Slot Pointer on EMS Subsystem
The SLTPTR has critical effects on the EMS system. Only one effect is hardware related. When SLTPTR is set to a value from 0004h to 0009h, bit BFENAB of the Index Configuration Register EMSEN1 is cleared. This disables the EMS Backfill Registers. Placement of SLTPTR is otherwise used by the EMS driver to determine the area of memory that can be allocated for use as EMS pages. Table 11 summarizes the effect of SLTPTR on the EMS system.

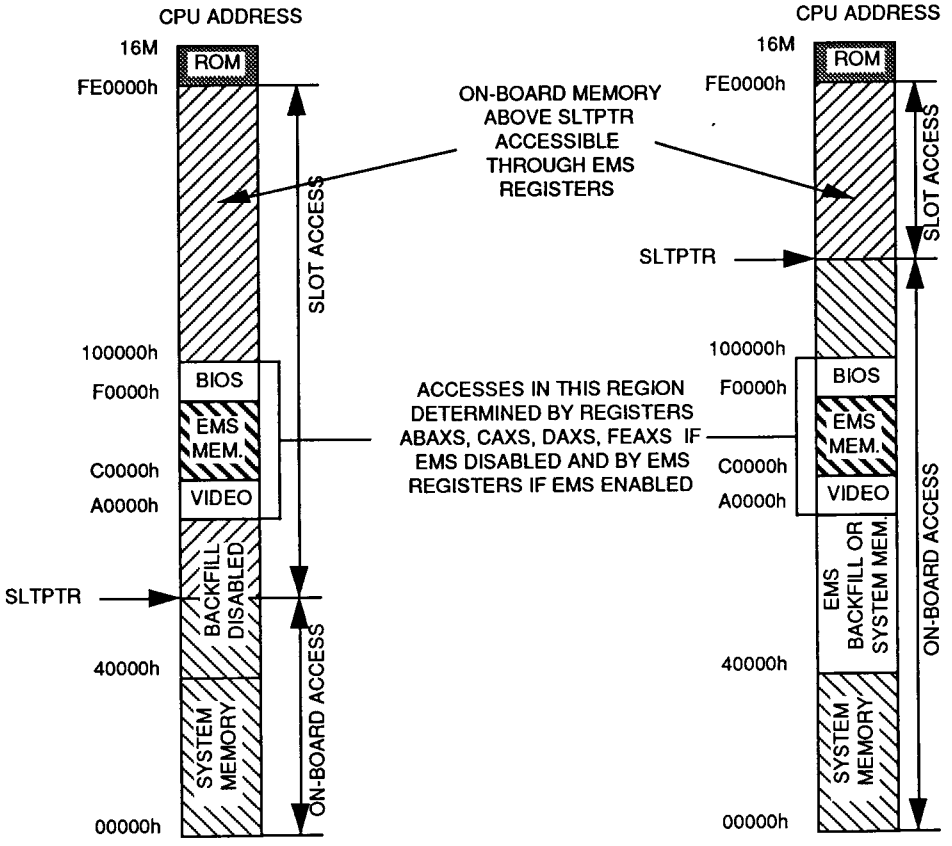
TABLE 11. EFFECT OF SLTPTR WITH EMS SYSTEM ENABLED

Slot Pointer Value	Slot Pointer Location	Effect
00h		No DRAM cycle initiated. This is to support the use of SRAM.
0004h-0009h	256K-640K	EMS Backfill Registers automatically disabled. EMS Page Registers remain operational. CPU addr 0h to SLTPTR = > system board accesses, CPU addr SLTPTR to 640K and 1M to 16M = > slot bus, CPU addr 640K to 1M = > see Note 1, CPU addr > 16M = > no accesses. On-board memory ? SLTPTR accessible through EMS Registers.
000Ah-000Fh	640K-1M	Respond as if SLTPTR = 0010h. (See next case.)
0010h-00FFh	1M-16M	CPU addr 0 to 256K = > system board accesses, CPU addr 256K to 640K = > system board access if Backfill Registers are disabled, CPU addr 640K to 1M + > see Note 1, CPU addr 1M to SLTPTR = > system board access. CPU addr SLTPTR to 16M = > see Note 2, CPU addr > 16M = > no accesses. EMS translation accesses system board RAM from SLTPTR to RAM top. Also, system board RAM from 256K-640K is used for EMS if Backfill EMS is enabled.

Notes: 1. When EMS is off and 384K DRAM in the address range A0000h-FFFFFh is not remapped, the result of CPU accesses to this memory region is determined solely by configuration of registers ABAXS, CAXS, DAXS, and FEAXS. When the EMS system is enabled, the active EMS Registers between A0000h and EFFFFh override the settings in any areas that overlap the configurations in ABAXS, CAXS, DAXS, and FEAXS. CPU addresses that fall in the realm of EMS Register control is not directly passed to the slots or the system board. The addresses are translated and access reserved areas of system board DRAM above SLTPTR.

2. Slot bus is accessed when the CPU address is between SLTPTR and FDFFFFh. The accesses from FE0000h to FFFFFFh (16M) are directed towards ROM.

FIGURE 12. SLTPTR, EMS, AND SHADOW CONTROL



Shadow Control and EMS Subsystem

The EMS control logic also interacts with the shadow control system through Configuration Registers ABAXS, CAXS, DAXS and FEAXS. Any enabled EMS Page Register overrides the shadow control in its range. System board memory in the same address range as the EMS Page Registers can be allocated to the EMS memory pool by the EMS driver software. In addition, other non-EMS segments can be allocated to the pool if they are not shadowed or otherwise in use. This is determined by the two shadow controls bits in ABAXS, CAXS, DAXS and FEAXS for a specific segment. When the bits are 00 (read/write slot) the system board memory may be allocated to the pool. Table 12 summarizes the interaction between EMS and shadow control.

TABLE 12. INTERACTION BETWEEN EMS AND SHADOW CONTROL

EMS ENAB	EMS Page Enable*	Shadow Control**	Effect
0	Don't care	00	R/W slot bus or ROMCS (Note 1).
		01	Read slot or ROMCS, write system board.
		10	Read system board or write slot (shadow).
		11	R/W system board.
1	0 (Note 2)	00	CPU accesses slots, EMS may access on-board DRAM.
		01	Setup Mode active. EMS driver may allocate (Note 3).
		10	Shadowed, EMS does not use.
		11	Used by other resource, EMS does not allocate.
1	1	XX	EMS overrides use of this area. CPU accesses translated by EMS. System board DRAM used by EMS system for EMS memory pages.

Notes: * Bits 3-0 of register EMSEN1 and bits 7-0 of register EMSEN2.

** Bits 7 and 6, 5 and 4, 3 and 2, and 1 and 0 of registers ABAXS, CAXS, DAXS, and FEAXS.

1. Accesses in the AXXXXh, BXXXXh, CXXXXh, and DXXXXh regions are directed to the slot bus. Accesses in the EXXXXh and FXXXXh regions generate on-board ROM chip selects.
2. This case not only applies to the areas C0000h-EFFFFh for which the EMS page enable bit is turned off, but also to the A0000h-BFFFFh and F0000h-FFFFFh area of memory. This information is supplied for use by the EMS driver code developers. Hardware operation in this mode is the same as the first case in this table.
3. When an EMS driver is installed this case should not exist. A shadow setup routine uses this code. It should then change it to 10b to enable the shadow feature. However, if an EMS driver sees this code it may allocate the system board DRAM in this area.

JEIDA IC Memory Card Support
This feature is available in the VL82C310 only.

The VL82C310 supports JEIDA IC Memory Card of up to 32 MB for use in laptop and notebook computers.

The 32 MB of memory on the memory card can be divided into 2048 pages, each 16 KB long. There are eight total Mapping Registers provided in the VL82C310 to map up to four of the 16 KB pages of IC memory card memory into the CPU address space. Four of the eight registers hold pointers required to map each 16 KB page into the CPU address space between A0000h and FFFFFh (address lines SA19-SA14). The other four of the eight total registers contain pointers into the IC card's memory space. These four IC memory card registers are associated in a one-to-one basis with the other four CPU address space registers. The correlation existing between the Mapping Registers for the IC memory card and those for the CPU address space are fixed and are arranged in 16 KB pages numbered "Page 0, 1, 2, and 3" (see Table 13). When the CPU accesses a 16 KB page pointed to by one of the CPU Address Mapping Registers, the CPU address is translated to access the 16 KB page pointed to by the associated IC memory card Mapping Register (see Figure 13 for a graphical representation).

The Mapping Registers are accessed via the Index Register at I/O address E8h. The lower six bits of this register are used to access one of the eight Mapping Registers. The mapping registers for CPU address space are accessed if the Index Register data is 30h, 32h, 34h, or 36h, while the Mapping Registers for IC memory card are selected if the lower six bits are 31h, 33h, 35h, or 37h.

The port addresses EAh and EBh are used for byte accesses to the Mapping Registers. The instructions for writing a byte to the Page 0 Mapping Register for IC memory card are:

```
MOV   AL,31     ; Page 0 Mapping
                  Register for IC
                  memory card
OUT   E8,AL
MOV   AL,data   ;
OUT   EA,AL     ; Write low byte
or
OUT   EB,AL     ; Write high byte
```

The Mapping Registers are word accessible at port address EAh. The Mapping Registers for CPU address space return FFh in the upper byte when a word read is performed.

The lower six bits of port EAh allow access to SA19-SA14 during CPU memory cycles. The memory address lines, MA10-MA0, are accessed by the lower three bits of port EBh and all eight bits of port EAh. The MA10-MA0 pins are connected to the address lines 24-14 of the IC memory card allowing access to 32 MB memory.

The four pages can be independently enabled using the Configuration Register MCDCTL. The register has four bits available, one for each page.

It should be noted that the auto-increment feature is not available in this mode. Also, when an invalid memory access is made for a disabled page, 0s are driven out on the address lines used for IC memory card support.

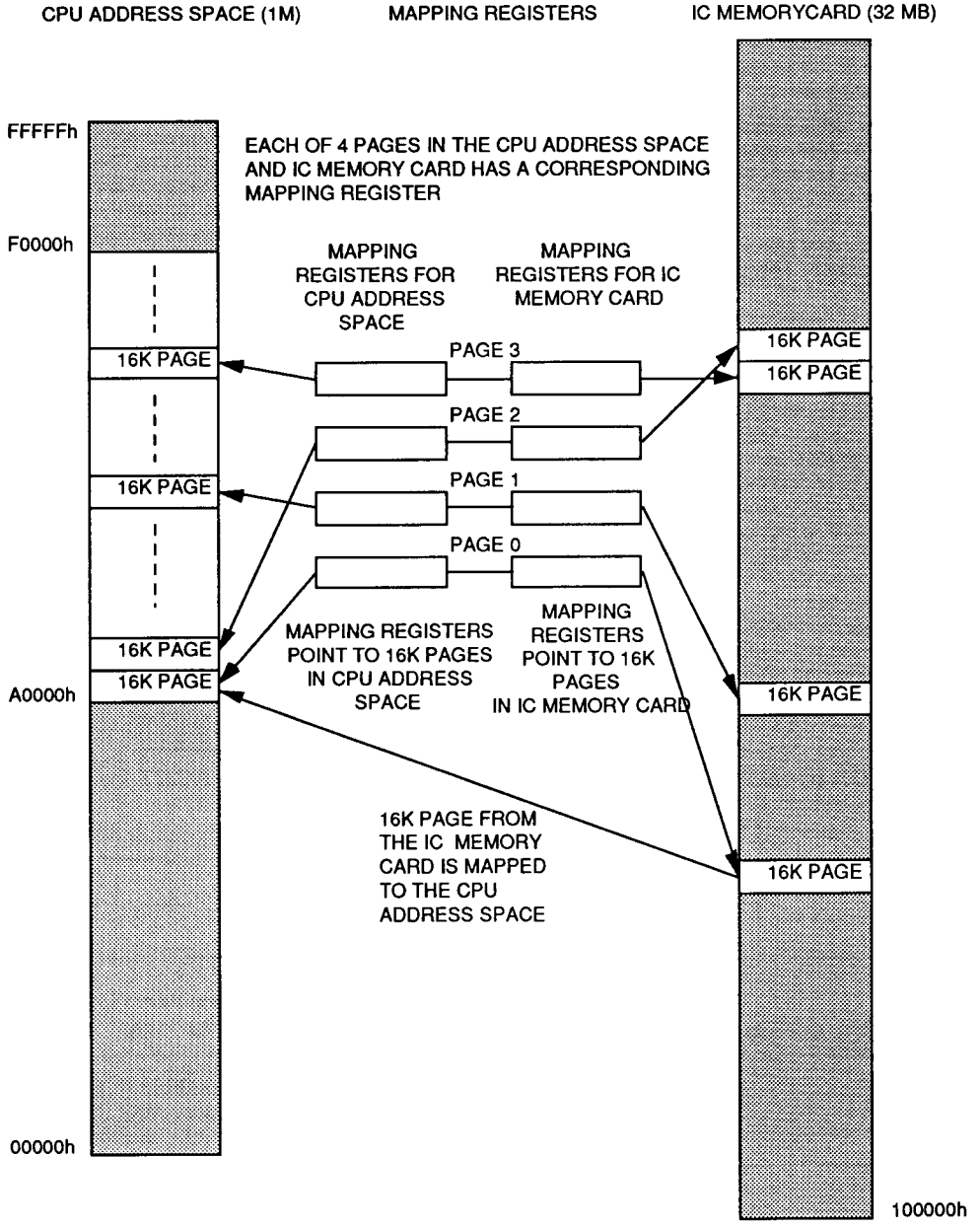
The memory card pages share the same CPU address space with EMS pages and shadowed memory. The memory card pages having the lowest priority makes it imperative for the software to ensure that EMS or shadowing is not enabled in the CPU address space where a memory card page is assigned.

TABLE 13. JEIDA IC MEMORY CARD INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
			A5	A4	A3	A2	A1	A0

Index Port (E8h)	Page Segment	Data Port (EBh) D15	D14	D13	D12	D11	D10	D9	D8	Data Port (EAh) D7	D6	D5	D4	D3	D2	D1	D0
30	0	1*	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
31	0	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32	1	1*	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
33	1	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
34	2	1*	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
35	2	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
36	3	1*	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
37	3	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

FIGURE 13. MEMORY MAPPING FOR JEIDA IC MEMORY CARD



Memory Card Control Register
The Memory Card Control Register, MCDCTL, is available for enabling the Mapping Registers. The four bits of this register controls a pair of Mapping Registers associated with a page. A pair of Mapping Registers consists of one for the CPU address space and one for the IC memory card. This register exists in the VL82C310 only.

MCDCTL Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
MCDCTL (0Ah)	1	1	1	1	MCPGEN3	MCPGEN2	MCPGEN1	MCPGEN0
POR Values	1	1	1	1	0	0	0	0

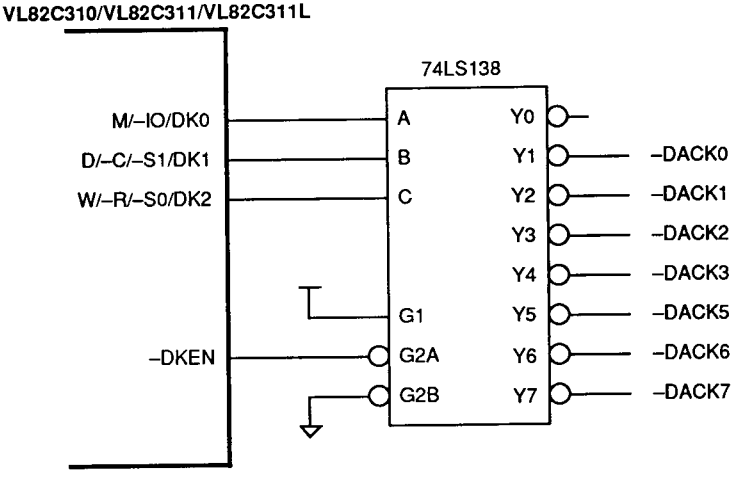
Bit	Name	Function
7-4		These bits are read-only and always returns logic 1.
3-0	MCPGEN3-MCPGEN0	Memory Card Page Enable: These bits are used to enable the Mapping Registers for CPU address space and IC memory card. Each bit controls a pair of Mapping Registers associated with one page. The bits when high, enable the Mapping Registers and allow access to four 16 KB pages. MCPGEN0 enables the Mapping Registers at address 30h and 31h, MCPGEN1 controls those at 32h and 33h, MCPGEN2 allows access to 34h and 35h, while the registers at 36h and 37h are controlled by MCPGEN3. At power-on, all four bits are disabled.

DIRECT MEMORY ACCESS (DMA)
The DMA controllers are 82C37 compatible, have internal latches provided for latching the middle address bits output by the 82C37 megacells on the data bus, and have 74LS612 memory mappers provided to generate the upper address bits.

The DMA logic controls transfers between an I/O channel and on- or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged the DMA controller drives the CPU address bus and the slot address bus. DMAs can occur over the full 16 MB range available.

The seven DMA acknowledge signals are encoded within the SCAMP Controller to generate external signals DK2-DK0. They have to be decoded externally using a 3-8 demultiplexer (74LS138). An enable signal, –DKEN, is generated by the SCAMP Controller for use by the demultiplexer. Figure 14 depicts interface between the SCAMP Controller and the 74LS138.

FIGURE 14. DECODING DMA ACKNOWLEDGE SIGNALS



DMA Controller Registers

The 82C37 megacells can be programmed any time HLDA is inactive, i.e., when the DMA controllers are not in operation. Table 14 lists the addresses of all registers which can be read or written in the 82C37 megacells. Addresses under DMA2 are for the 16-bit DMA channels and DMA1 corresponds to the 8-bit channels. When writing to a channel's address or word count register, the data is written into both the base register and current register simultaneously. When reading a channel address or word count register, only the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16-bit registers. The value on the data bus is written into the upper byte or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the "clear byte pointer flip-flop" command. After this command, the first read/write to an address or word count register will read/write to the low byte of the 16-bit register and the byte pointer flip-flop will toggle to a 1. The next read/write to an address or word count register will read/write to the high byte of the 16-bit register and the byte pointer flip-flop will toggle back to a 0. Refer to the 82C37 data sheet for more information on programming the 82C37 megacell.

The 82C37 DMA controller megacells allow the user to program the active level (low or high) of the DREQ and DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DREQ signals active high and the DACK signals active low.

When programming the 16-bit channels (channels 5, 6, and 7) the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16-bit channels is the number of 16-bit words to be transferred, not the number of bytes as is the case for the 8-bit channels.

It is recommended that all internal locations, especially the mode registers, in the 82C37 megacells be loaded with some valid value. This should be done even if the channels are not used.

TABLE 14. DMA CONTROLLER REGISTERS

Hex Address		
DMA2	DMA1	Register Function
0C0	000	Ch 0 Base and Current Address Register
0C2	001	Ch 0 Base and Current Word Count Register
0C4	002	Ch 1 Base and Current Address Register
0C6	003	Ch 1 Base and Current Word Count Register
0C8	004	Ch 2 Base and Current Address Register
0CA	005	Ch 2 Base and Current Word Count Register
0CC	006	Ch 3 Base and Current Address Register
0CE	007	Ch 3 Base and Current Word Count Register
0D0	008	Read Status Register/Write Command Register
0D2	009	Write Request Register
0DR	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-Flop
0DA	00D	Read Temp Register/Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

Middle Address Bit Latches
The middle DMA address bits are held in an internal 8-bit register. The DMA controller will drive the value to be loaded onto the internal data bus and then issue an address strobe signal to latch the data bus value into this register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8-bit address increments across the 8-bit subpage boundary during block transfers. This register cannot be written to or read externally. It is loaded only from the address strobe signals from the megacells and the outputs go only to the A16-A8 pins.

Page Registers
A 74LS612 cell is used in the SCAMP Controller to generate the Page Registers for each DMA channel. The Page Registers provide the upper address bits during a DMA cycle. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8-bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16-bit channels (channels 5, 6, and 7) are every 128 kilobytes. There are a total of 16 8-bit registers in the 612 megacell.

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 080h and 08Fh not shown in the table are not used by the DMA channels but can be read or written to by the CPU.

TABLE 15. DMA PAGE REGISTERS ACCESS

A23-A16 Address	DMA Channel
87h	0
83h	1
81h	2
82h	3
8Bh	5
89h	6
8Ah	7
8Fh	Refresh

ROMDMA Register
The Indexed Configuration Register ROMDMA is used to program the extended DMA features.

ROMDMA Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA (15h)	ROMWS1, ROMWS0		DMAWS8		DMAWS16		DMACLK	MEMTM
POR Values	PAR1	PAR0	1	1	1	0	0	0

Bit	Name	Function
7, 6	ROMWS1, ROMWS0	ROM Wait States: These bits indicate the number of ROM wait states. These wait states are timed in slot bus cycles. The valid range is 1-3: 00 - 3 wait states 01 - 1 wait state 10 - 2 wait states 11 - 3 wait states The initial power-on reset value of ROMWS1 is set the same as PAR1 and of ROMWS0 is set the same as PAR0 at the end of the reset period.
5, 4	DMAWS8	8-Bit DMA Wait States: Bits 5 and 4 are encoded with the number of clocks the command is active for 8-bit DMA cycles: 00 - 2 DMA clocks 01 - 4 DMA clocks 10 - 3 DMA clocks 11 - 3 DMA clocks
3, 2	DMAWS16	16-Bit DMA Wait States: These bits specify the number of clocks the command is active for 16-bit DMA cycles: 00 - 2 DMA clocks 01 - 4 DMA clocks 10 - 3 DMA clocks 11 - 3 DMA clocks
1	DMACLK	DMA Clock: When set, this bit selects SYSCLK as an input clock for the DMA. When 0, the input clock to the DMA is SYSCLK/2. At power-on reset, SYSCLK/2 is selected as DMA clock.
0	MEMTM	–MEMR Signal Delay: This specifies the delay for the –MEMR signal. When 0, –MEMR is active at the same time as in the original PC/AT design. This is the default case. When 1, falling edge of –MEMR occurs one DMACLK earlier. In this latter case, the –MEMR timing during a memory to I/O DMA cycle is the same as that of the –XIOR signal during an I/O to memory DMA cycle.

CLOCK GENERATOR

The clock generator logic generates programmable frequency clock signals. The SCAMP Controller has a unique expanded clock feature by which the clock is automatically increased when video DRAM address range, A0000h-BFFFFh, is accessed. The logic diagram of the clock generator is shown in Figure 15.

The external input pins related to the clock generation are TCLK2, OSC, and BUSOSC. The output pins are CLK2 and SYSCLK.

Clock Signals

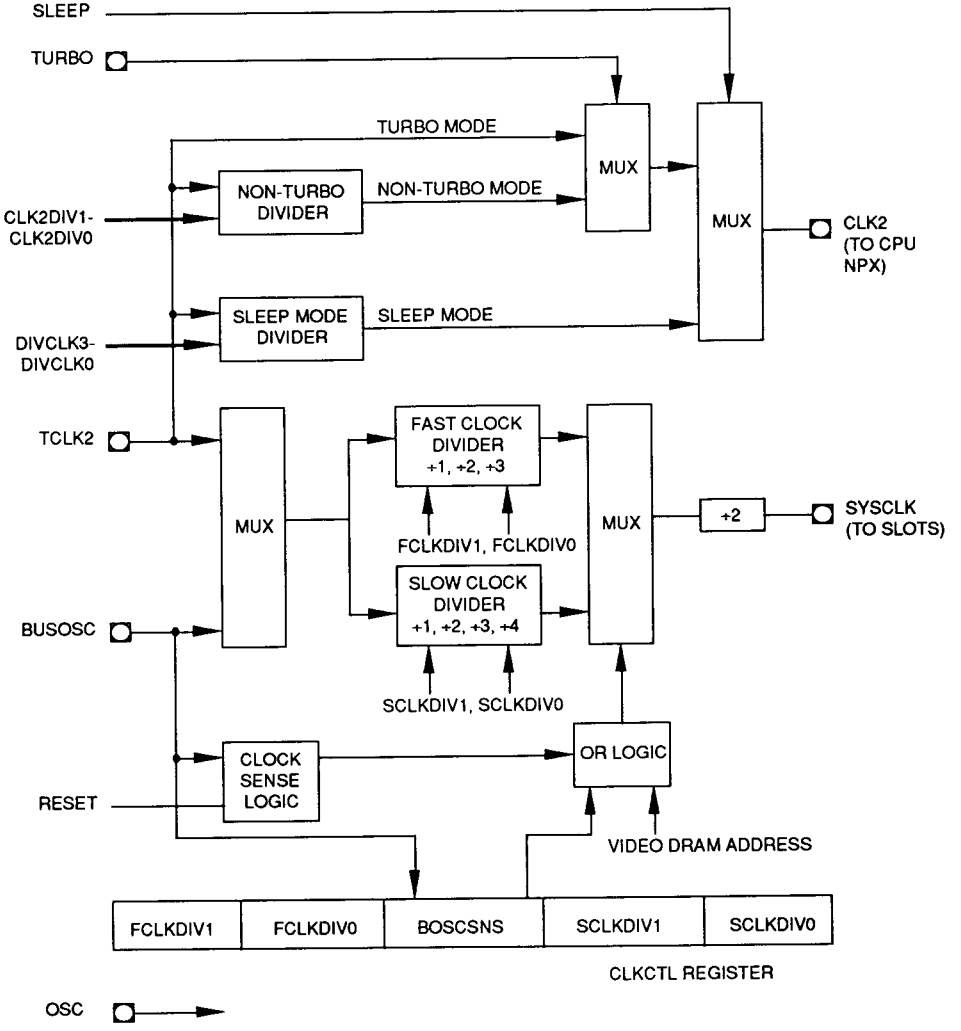
The SCAMP Controller supports systems with operating frequencies up to 25 MHz. The processor clock, CLK2, is connected to the CPU, the coprocessor, and other on-board logic for synchronization. It is derived from the input signal TCLK2 which is connected to a crystal oscillator of frequency twice the operating frequency. The frequency of CLK2 is programmable. The bits CLK2DIV1 and CLK2DIV0 of the Clock Control Register, CLKCTL, select CLK2 to be TCLK2, TCLK2/2, TCLK2/3, or TCLK2/4.

OSC is the buffered input of the external 14.318 MHz oscillator.

The bus clock, BUSOSC, is supplied from an external oscillator and is used for asynchronous AT bus operations.

The system clock output, SYSCLK, is a programmable clock. It is generated from either TCLK2 or BUSOSC as explained in the section "Programmable AT Bus Clock". The bus control outputs BALE, –IOR, –IOW, –MEMR, and –MEMW are synchronized to SYSCLK.

FIGURE 15. CLOCK GENERATOR LOGIC DIAGRAM



Programmable AT Bus Clock
The SCAMP Controller provides a special feature of programming the AT bus clock, SYSCLK, for an optimum performance. The frequency of synchronous SYSCLK can be varied from 5 MHz to 25 MHz using the BUSOSC pin and the CLKCTL Register. Thus, different SYSCLK frequencies can be used for different peripheral accesses. The logic diagram of the circuit that generates SYSCLK is shown in Figure 15.

The pin BUSOSC is sensed by the clock sense logic at power-on reset. If there is no external oscillator connected to BUSOSC, it can be used to select the frequency of SYSCLK. At power-on reset, the values of pins –DKEN and –PPICS are latched in to the bits SCLKDIV1 and SCLKDIV0 of register CLKCTL. TCLK2 is divided by a factor of 2, 4, 6, or 8 depending on the bit values of SCLKDIV1 and SCLKDIV0 to generate SYSCLK. Refer to Table 16.

TABLE 16. AT BUS CLOCK FREQUENCIES

BUSOSC	BOSCSNS/ Video DRAM	FCLKDIV1, FCLKDIV0	SCLKDIV1, SCLKDIV0	SYSCLK
BUSOSC	0	XX	00	BUSOSC/2
	0	XX	01	BUSOSC/4
	0	XX	10	BUSOSC/6
	0	XX	11	BUSOSC/8
	1	00	XX	BUSOSC/2
	1	01	XX	BUSOSC/4
	1	10	XX	BUSOSC/6
	1	11	XX	
0	0	XX	00	TCLK2/2
0	0	XX	01	TCLK2/4
0	0	XX	10	TCLK2/6
0	0	XX	11	TCLK2/8
1	1	00	XX	TCLK2/2
1	1	01	XX	TCLK2/4
1	1	10	XX	TCLK2/6
1	1	11	XX	

The frequency of SYSCLK for faster operation is programmable using bits FCLKDIV1 and FCLKDIV0. The clock TCLK2 is divided by 2, 4, or 6.

When there is no external oscillator connected to BUSOSC, the pin BUSOSC can be toggled to switch between the two dividers. When it is 0, the slow clock divider is active. If BUSOSC is held high, the fast clock divider is used for generating SYSCLK. The switching between the two dividers also occurs automatically in the SCAMP Controller when the bit ENVDSP in the register CLKCTL is enabled and the video DRAM address space, A0000h-BFFFFh, is accessed.

The bit BOSCSNS reflects the status of the BUSOSC pin and is a read-only bit when there is no oscillator connected to BUSOSC.

If BUSOSC has an oscillator connected to it, SYSCLK is derived from BUSOSC instead of TCLK2. The frequency of SYSCLK can then be varied using the bit BOSCSNS which now is a read/write bit. At power-on reset, the slow clock divider is enabled, dividing BUSOSC by a factor depending on bits SCLKDIV1 and SCLKDIV0. These two bits are configured at power-on reset by pins –DKEN and –PPICS. The fast clock divider is activated if BOSCSNS bit is 1 or a valid video DRAM address space is accessed in the SCAMP Controller with ENVDSP enabled. The division factor is determined by FCLKDIV1 and FCLKDIV0.

Clock Control Register (CLKCTL)

The register CLKCTL is used for determining SYSCLK frequency (as described in the section "Programmable AT Bus Clock"), setting CLK2 frequency, and enabling SYSCLK frequency switching in the video DRAM address range. Please refer to Figure 15 to see how all of the bits in the CLKCTL Register are related.

CLKCTL Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
CLKCTL (07h)	ENVDSP	CLK2DIV1, CLK2DIV0		FCLKDIV1, FCLKDIV0		BOSCSNS	SCLKDIV1, SCLKDIV0	
POR Values	0	0	0	1	0	See Descrip.	-DKEN	-PPICS

Bit	Name	Function
7	ENVDSP	Enable SYSCLK Frequency Switching in Video DRAM Address Range: This bit selects a different SYSCLK frequency when a memory access is made in the video DRAM address range of A000h-BFFFFh. When set low, ENVDSP disables the automatic frequency change in SYSCLK, and enables that feature if set high. The default value of this bit is 0.
6, 5	CLK2DIV1, CLK2DIV0	CLK2 Divider in Non-Turbo Mode: These bits specify the CLK2 divider value to be used when the TURBO pin is low or when a write to port F4h is performed. CLK2DIV1 / CLK2DIV0 / CLK2 0 / 0 / TCLK2 + 1 0 / 1 / TCLK2 + 2 1 / 0 / TCLK2 + 3 1 / 1 / TCLK2 + 4 The power-on reset default value of these bits is 00, selecting TCLK2 as the frequency of CLK2.
4, 3	FCLKDIV1, FCLKDIV0	Fast Clock Divider: These bits determine the frequency of SYSCLK when an access is made to the video DRAM address space with ENVDSP of this register set to 1, or when BOSCNS bit is 1. FCLKDIV1 / FCLKDIV0 / SYSCLK 0 / 0 / CLOCK/2 0 / 1 / CLOCK/4 1 / 0 / CLOCK/6 1 / 1 / Reserved Where CLOCK is BUSOSC if asynchronized bus clock, or TCLK2 if it is synchronized. The default value is 10.
2	BOSCSNS	BUSOSC Status: This bit reflects the state of the BUSOSC pin when there is no external oscillator connected to the BUSOSC pin. In that case, this bit is read-only. If there is an oscillator present, this bit becomes a read/write one selecting SYSCLK frequency as explained in the section "Programmable AT Bus Clock". The power-on reset default value of this bit is 0 if external BUSOSC is present and BUSOSC pin status if it is not.
1, 0	SCLKDIV1 SCLKDIV0	Slow Clock Divider: These bits are used for selecting the frequency of SYSCLK during system DRAM accesses, and when BOSCSNS bit is 0. SCLKDIV1 / SCLKDIV0 / SYSCLK 0 / 0 / CLOCK/2 0 / 1 / CLOCK/4 1 / 0 / CLOCK/6 1 / 1 / CLOCK/8 Where CLOCK is BUSOSC if connected externally or TCLK2 if not. The default values are determined by the status of pins -DKEN and -PPICS at power-on reset.

SLEEP MODE CONTROL LOGIC
This feature is only in the VL82C310.

The Sleep Mode operation is provided for battery operated laptop microcomputer support. The SLPCTL Register and MISCSET Register are provided to control this function.

Sleep Mode Operation
The Sleep Mode can be activated by software as well as by hardware. The external pin –SLEEP/–MISS can be used to enable the Sleep Mode by hardware. It should be noted that the bit PINFNC in the SLPCTL Register selects the functionality of the –SLEEP/–MISS pin for the Sleep Mode. Refer to section "SLEEP Mode Configuration Register" for information. A 1-to-0 transition on this pin puts the device into the Sleep Mode. For activating the Sleep Mode by software, the bit SLP in the SLPCTL Register should be set high.

When the VL82C310 is in the Sleep Mode, the CLK2 divider and refresh dividers are activated and BUSOSC is shut-off from non-essential internal circuitry. The clocks going to the DMA circuit, interrupt controllers, and refresh logic are not shut-off.

For maximum power savings, it is recommended that a HALT instruction be executed immediately after setting the bit SLP. Power saving can also be accomplished by operating the CPU at the minimum allowable frequency. There are three bits available in the SLPCTL Register to select the clock frequency for the CPU. It should be noted that Turbo or non-Turbo Mode of operation has no effect on this frequency when the Sleep mode is activated.

The VL82C310 can be brought out of the Sleep Mode in one of four ways:
1) Clearing the SLP bit of the SLPCTL Register to 0 by software.
2) Driving a 0-to-1 input on the –SLEEP pin with the SLPMISS bit set to 0.
3) Interrupting the VL82C310.
4) Resetting the VL82C310.

Normal BUSOSC routing and clock speed are resumed when the device comes out of the Sleep Mode.

The Sleep Mode is suspended during refresh cycles, DMA cycles, or Master Mode cycles by automatically deactivating the sleep clock divider in response to the hold request. Upon completion of the cycle the system re-enters the Sleep Mode unless the SLP bit has been cleared.

Sleep Mode Configuration Register
This register exists only in the VL82C310.

The SLPCTL Register controls the Sleep Mode functionality. Bits 0 and 1 and 4 through 6 should be set with the desired values by the BIOS during Post. Only bit 7 needs to be toggled to get in and out of the Sleep Mode during operation.

SLPCTL Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SLPCTL (13h)	SLP	DIVCLK3-DIVCLK0				SLPSTS	PINFNC	ENSYSCK
POR Values	0	0	0	0	0	–SLEEP	0	1

Bit	Name	Function
7	SLP	Sleep Mode: This bit is set to 1 to invoke all sleep functions. When set, CLK2 is divided by the value coded in bits 6-4 of this register.
6-3	DIVCLK3-DIVCLK0	Power Down TCLK2 Divider: These bits provide a code used to divide the TCLK2 down for the Sleep Mode. Division from 1-1024 is programmable as specified below: Bit 6 Bit 5 Bit 4 Bit 3 Clock 0 0 0 0 +1 (Default) 0 0 0 1 +4 0 0 1 0 +8 0 0 1 1 +12 0 1 0 0 +16 0 1 0 1 +64 0 1 1 0 +128 0 1 1 1 +256 1 0 0 0 +1024 All the other combinations not mentioned here are reserved.
2	SLPSTS	–SLEEP Pin Status: This bit reflects the status of the –SLEEP pin. It is used by the software to check whether –SLEEP is active or not. The VL82C310 enters the Sleep Mode when –SLEEP is pulled low. If an interrupt occurs, the device comes out of the Sleep Mode but the pin still might be pulled low. The interrupt service routine can check this bit and activate the Sleep Mode by enabling the SLP bit.
1	PINFNC	Pin Function: In the VL82C310 this bit determines the function of the –SLEEP/–MISS pin. PINFNC –SLEEP/–MISS 0 –SLEEP 1 –MISS In the VL82C311 and VL82C311L this bit is always a 0 and is reserved for a special test mode and should never be written.
0	ENSYSCK	System Clock Enable: Resetting this bit to 0 disables the SYSCLK oscillator (BUSCLK/2) if bit 7 is set to 1. Returning bit 7 to 0 re-enables the oscillator signal. If bit 0 = 1, the oscillator is always enabled even in the Sleep Mode. In operation, bit 0 is set for the desired operational mode by the BIOS on power-up. Bit 7 is then controlled as required to jump in and out of the Sleep Mode during operation.

ISA BUS INTERFACE

The ISA bus is accessed in the CPU Mode, DMA Mode, Refresh mode, and Bus Master Mode.

In the CPU Mode, the 82288 megacell is responsible for generating the command signals –IOR, –IOW, –MEMR, –MEMW, –SMEMR, –SMEMW, and BALE. The SCAMP Controller samples the inputs –MEMCS16, –IOCS16, and –IOCHRDY. The signal –WS0 determines the length in wait states of each bus cycle.

During refresh the SCAMP Controller drives the –REFRESH signal, a refresh address, and the command –MEMR onto the bus to implement the Refresh Mode. The refresh circuit samples –IOCHRDY to determine if the –MEMR and –REFRESH pulses need to be extended. The output BALE is driven high during the refresh cycles.

In the DMA Mode, the DMA controllers generate the command and address signals. BALE is forced high for all DMA cycles. The SCAMP Controller asserts the AEN signal to indicate that the current address on the bus is for memory only and is not to be decoded as an I/O address. The DMA section samples –IOCHRDY to extend bus cycles longer than the internally defined cycle length.

The Bus Master Mode is an extension of the DMA Mode. A Bus Master can get control of the bus by requesting a DMA operation. Once the DMA is acknowledged, the –MASTER signal is pulled active and the SCAMP Controller relinquishes control of the bus to the Master.

BUSCTL Register

Three bus control options are provided and are programmable via the indexed BUSCTL Register. It controls the number of wait states to be inserted in the 8-bit and 16-bit slot cycles and determines the width of the BIOS ROM.

Zero wait state is possible on extremely fast boards that can pull the –WS0 line fast enough and more than five wait states are possible if –IOCHRDY is pulled low before the last normal wait state. However, –MEMCS16 or –IOCS16 must be pulled low before the last normal wait state even if –IOCHRDY has previously been activated.

BUSCTL Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL (16h)	ROMWID	SLTDRV	DSKTMG	1	CMDLY2	CMDLY1	16WS	8WS
POR Values	MA10	–ROMCS	0	0	0	0	0	0

Bit	Name	Function
7	ROMWID	ROM Width: This bit determines the width of the BIOS ROM. When set, the BIOS ROM is assumed to be 16-bit wide and connected to D15-D0. When 0, 8-bit BIOS ROM is assumed to be on D15-D8 (8-bit ROM resides on the upper byte of the D bus). The initial power-on reset value of this bit is set the same as MA10 at the end of the reset period.
6	SLTDRV	Slot Current Drive: This bit selects the current drive on the slot. If low, the current drive is 12 mA. Otherwise it is 24 mA. The default value of this bit is the status of the pin –ROMCS.
5	DSKTMG	Disk Timing: This bit determines the timing for programmed I/O. If set (1), normal programmed I/O will be invoked. If cleared (0), slow programmed I/O will be used. The power-on reset default value of this bit is 0.
4		Reserved: These bits are reserved and return logic value 1 when read. They are not write accessible.
3	CMDLY2	Command Delay 2: This bit, when set, allows addition of an extra command delay for 8-bit and 16-bit I/O cycles and for 8-bit memory cycles. When 0, there is no added command delays. The power-on default value of this bit is 0 resulting in PC/AT compatibility.
2	CMDLY1	Command Delay 1: This bit, if 0, allows PC/AT-compatible zero command delays on 16-bit memory cycles. An extra command delay is added if set to 1. The default is 0.
1	16WS	16-Bit Wait States: This bit determines whether to use zero or one wait state for 16-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible zero wait states are used. When to 1, one wait state is used to allow robust operation of add-in cards at faster slot speeds. The default value of this bit is 0 indicating zero wait states for 16-bit slot accesses.
0	8WS	8-Bit Wait States: When bit 0 = 1, an extra wait state is added for 8-bit slot bus accesses. This yields five rather than the normal four wait states. This allows slower boards to operate with equivalent performance when higher bus speeds are used. This bit is set to 0 at power-on reset initiating four wait states on 8-bit slot accesses.

KEYBOARD CONTROLLER INTERFACE

The SCAMP Controller is connected to the keyboard controller, 8042, as shown in Figure 16. Note that there is no A20GATE and –RC pins on the SCAMP Controller. The port pins P20 and P21 of 8042 are therefore not connected. These two signals are generated internally in the SCAMP Controller. The data lines are checked for a particular data sequence when the keyboard controller is selected to generate A20GATE and –RC.

For hardware compatibility, the generation of –RC is delayed by about 50 µs from the issuance of the command to generate a 6 µs pulse. A delay timer is used in the internal circuit for this purpose. This timer can be disabled by bit FASTRC in the MISCSET Register.

When this bit is 1, –RC is generated with only 6.72 µs delay. This provides an alternative for Fast CPU Reset.

Generation of A20GATE and –RC

The keyboard controller interface signals A20GATE and –RC are internal to the SCAMP Controller. These signals are generated in two ways in PC/AT. They are described below.

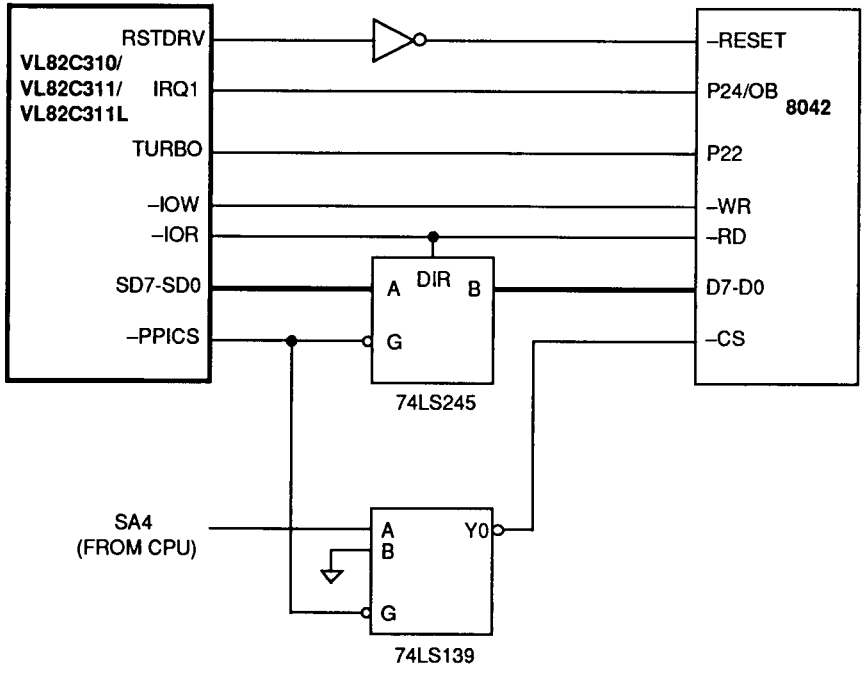
1) Data D1h is written to I/O address 64h. This is a write output port command from the CPU to the keyboard controller. The next byte written to I/O address 60h enables or disables A20GATE and –RC. Bit 0 of this byte is reflected on –RC while bit 1 gets propagated to A20GATE. It should be noted that the I/O address 60h does not have to be written immediately after writing D1h to the address 64h.

   Only A20GATE is generated in this way in SCAMP Controller because the generation of –RC by this method can hang-up the system. There is no delay involved in the generation of A20GATE.

2) If I/O address 64h is written with F0h-FFh, A20GATE and –RC are pulsed depending on the lower two bits of the data. If bit 0 is low, –RC is pulsed, and A20GATE is pulsed if bit 1 is low. In other words, a pulse appears on –RC pin if the data is FEh or FCh, and A20GATE is pulsed if it is FDh or FCh. The pulse duration is approximately 6 µs.

   The SCAMP Controller generates a pulsed –RC this way but there is no effect on A20GATE.

FIGURE 16. KEYBOARD CONTROLLER INTERFACE

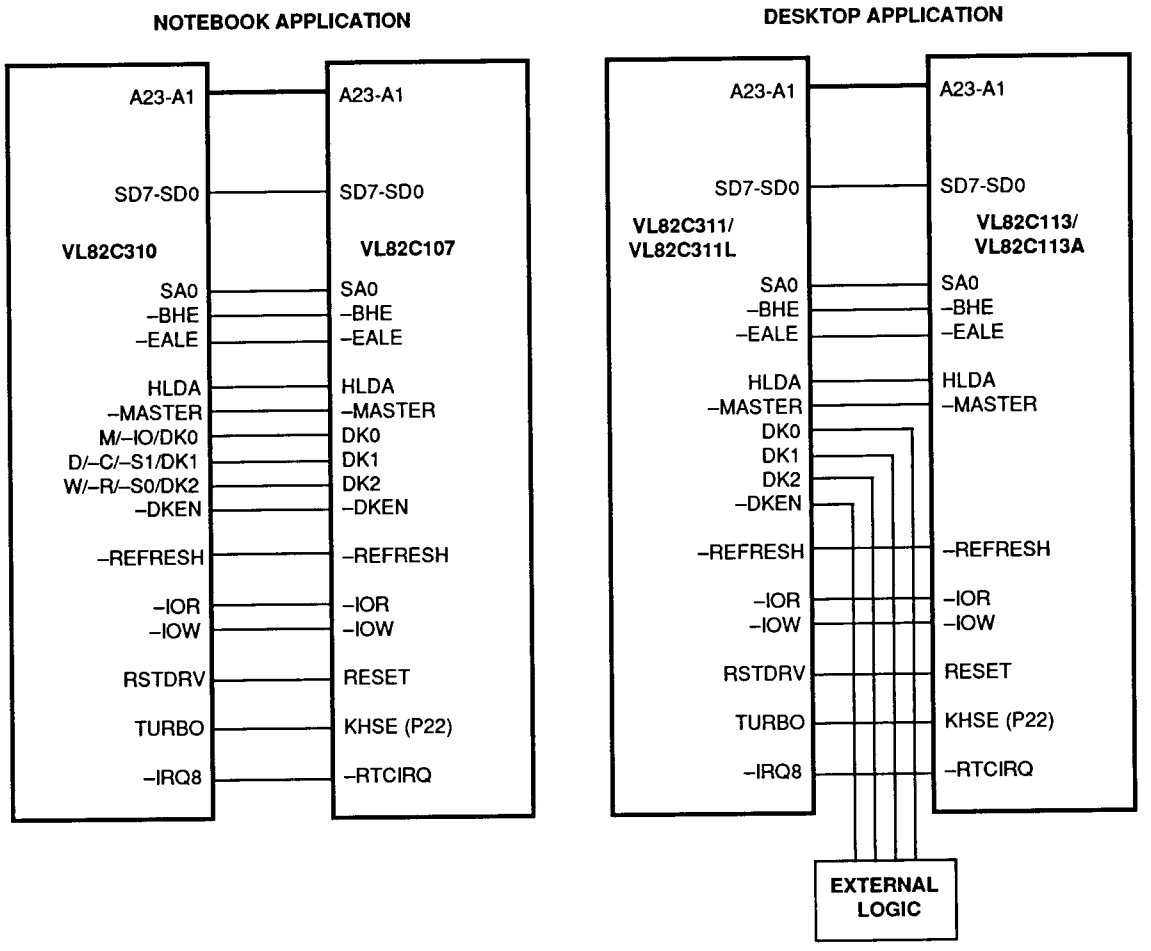


INTERFACE WITH SCAMP COMBINATION I/O CHIPS

This information is very preliminary and may change without notice.

The SCAMP Combination I/O chips include the glue logic required to design a PC/AT motherboard with a SCAMP Controller. The interface between the two is shown in Figure 17.

FIGURE 17. SCAMP CONTROLLER AND COMBINATION I/O INTERFACE



INTERFACE WITH THE VL82C325 CACHE CONTROLLER

The information in this section is preliminary and applies only to the VL82C310 and VL82C311.

The VL82C310 and VL82C311 support the VL82C325 Cache Controller for improving system performance. An external pin –SLEEP/–MISS is provided for this purpose. It is connected to the –MISS pin of the VL82C325 as shown in Figure 18. It should be noted that the bit PINFNC in the SLPCTL Register is used to select the functionality of the –SLEEP/–MISS in the VL82C310 and VL82C311. Please refer to the section "Sleep Mode Configuration Register" for more information.

Table 17 summarizes the response of the VL82C310 and VL82C311 to different bus cycles with the VL82C325 present in the system. The INTA, I/O read/write, halt/shutdown, and memory write cycles are initiated in the middle of T2 (or T1P for pipelined cycles).

The VL82C325 is effective during memory read cycles. When the CPU issues a memory read command, the VL82C325 informs the VL82C310 or VL82C311 about a cache-hit or cache-miss via the –MISS pin. It is pulled high in case of a cache-hit or pulled low if a cache-miss. The status of the –MISS signal changes during T2P1 as shown in Figures 19 and 20.

The VL82C310 or VL82C311 strobes the –MISS pin at the rising edge of T2P2. If there is a cache-hit, the memory read cycle is aborted by the VL82C310. This is achieved by not asserting the –CAS line. It should be noted that –RAS is activated. This is depicted in Figure 19. In case of a cache-miss, –CAS is asserted following the rising edge of T2P2 as shown in Figure 20. The –RAS line being already activated, a memory read is performed.

TABLE 17. RESPONSE TO BUS CYCLES WITH CACHE CONTROLLER

Bus Cycle Type					VL82C310/VL82C311 Response
M/–IO	D/–C	W/–R	386SX Cycle	Conditions	
0	0	0	INTA		INTA Cycle
0	0	1	Undefined		Undefined
0	1	0	I/O Read		I/O Read
0	1	1	I/O Write		I/O Write
1	0	0	Memory Code Read	Hit Miss	Aborted Memory Read Memory Read
1	0	1	Halt/Shutdown		Halt/Shutdown
1	1	0	Memory Data Read	Hit Miss	Aborted Memory Read Memory Read
1	1	1	Memory Data Write		Memory Write

FIGURE 18. INTERFACE WITH VL82C325 CACHE CONTROLLER

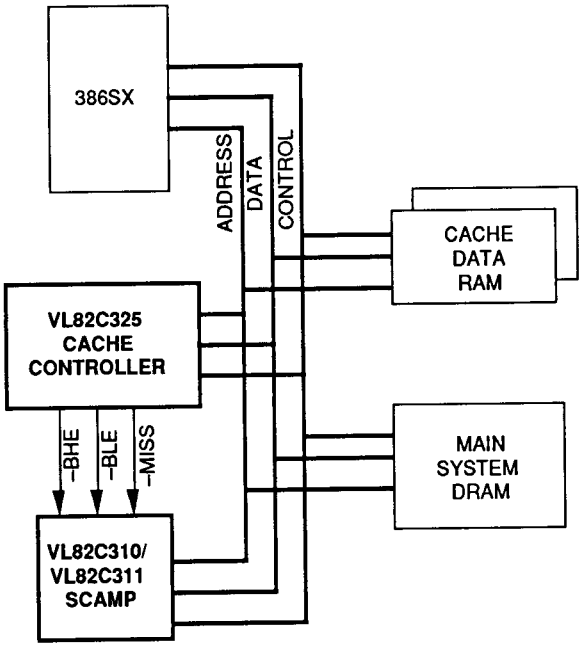


FIGURE 19. CACHE-HIT READ CYCLE

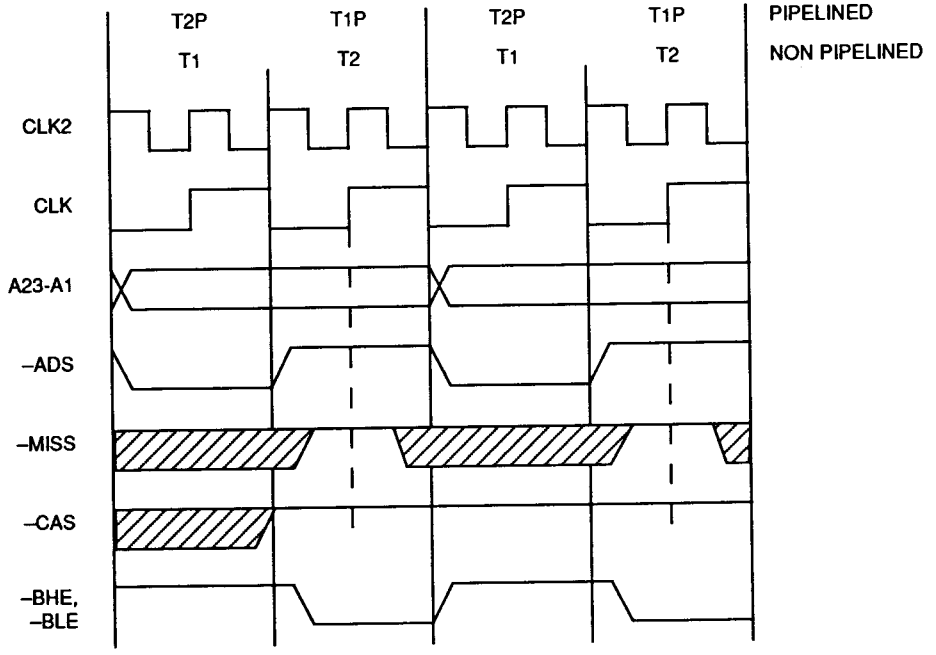
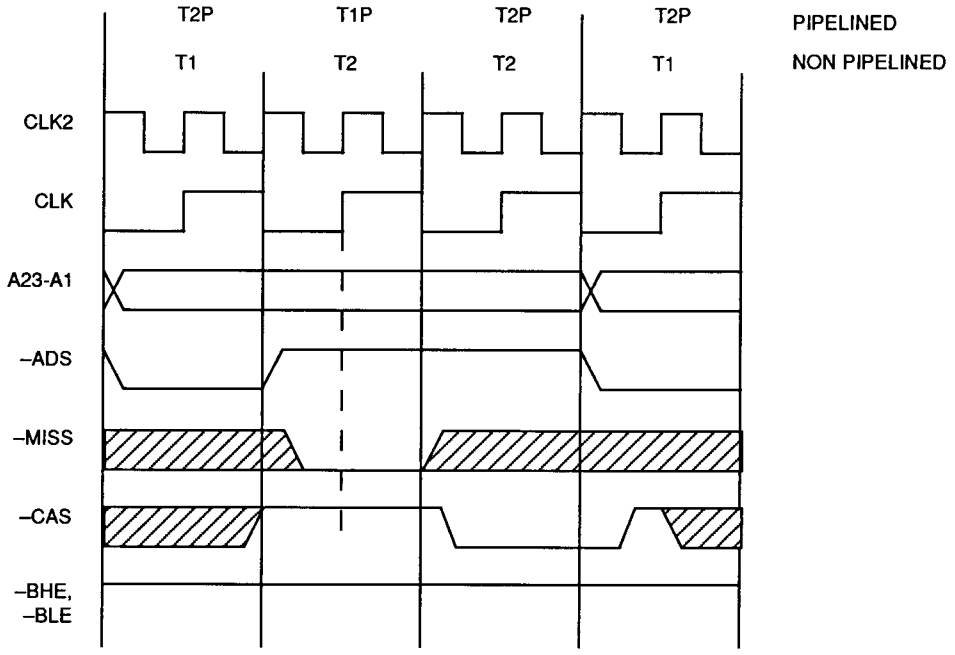


FIGURE 20. CACHE-MISS READ CYCLE



TURBO/SLOW CPU CONTROL

It has become standard for fast PC/AT compatibles to provide means to slow operation for older speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. One way this mode may be toggled on and off is by external control of the TURBO input pin. The slow mode is activated and the CLK2 divider is in effect when TURBO is low. When TURBO is high, CLK2 runs at the same speed as TCLK2 (only if the VLSI Special Feature Turbo request is also active, see below). This range provides the capability to operate at 8 MHz or under for any actual CPU speed from 12 to 33 MHz.

The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a key combination such as Ctrl Alt+/Ctrl Alt–. This input is often externally ANDed with a mechanical Turbo switch on the front panel.

The SCAMP Controller offers a way to control the CPU speed by software also. A dummy write to 0F5h returns to full speed operation if the TURBO pin is high. The bit –VSF of the MISCSET Register must be enabled for the software control. The slow operation can be enabled by either pulling the TURBO pin low or by performing a dummy write to I/O port 0F4h. When the bit –VSF is disabled, the CPU speed control is solely under control of the TURBO pin.

Note: The state of TURBO has no impact on the synchronous slot clock frequency. While selection of slow operating mode does affect the frequency of CLK2, it has no effect on the slot clock. The synchronous slot clock is derived from TCLK2 which is always constant.

PORT B AND NMI LOGIC

The SCAMP Controller generates the Non-Maskable Interrupt (NMI) output pin for the CPU. NMI is enabled by a write to I/O address 070h with D7 low. Once enabled, an NMI can be generated by the –IOCHCK input going low or a parity error. Each of these NMI sources has an enable bit in the Port B register to allow these inputs to cause an NMI when set high, or ignore the input if the bit is low.

The Port B register at I/O address 061h is included in the SCAMP Controller. This register contains bits to control the speaker output and NMI circuitry. Bits 0-3 are read/write bits, while bits 4-7 are read-only. Each bit of the register is defined below. Bits 0-3 are all set low by a reset.

Port B Register - Read/Write

Port B	D7	D6	D5	D4	D3	D2	D1	D0
061h	PCK	CHAN_CHK	OUT2	REFDET	ENA_IO_CHK	ENA_RAM_PCK	SPK_DAT	TIM2GAT_SPK

Bit	Name	Function
7	PCK	Parity Check: This bit indicates that an on-board RAM parity error has occurred. It can only be set if ENA_RAM_PCK is set 0. PCK should be cleared by writing a 1 to ENA_RAM_PCK.
6	CHAN_CHK	Channel Check: This bit indicates that a peripheral device is reporting an error. It can only be set if ENA_IO_CK is set low. CHAN_CHK should be cleared by writing a 1 to ENA_IO_CK.
5	OUT2	Timer Output bit 2 state: This bit indicates the current state of the OUT2 signal from the 82C54 megacell.
4	REFDET	Refresh Detect: This bit is tied to a toggle flip-flop which is clocked by REFRESH. It toggles to the opposite state every time a refresh cycle occurs.
3	ENA_IO_CHK	Enable I/O Check: When this bit is set low, it allows an NMI to be generated if the –IOCHCK input is pulled low. Otherwise, the –IOCHCK input is ignored and can not generate an NMI.
2	ENA_RAM_PCK	Enable RAM Parity Check: When this bit is set low, it allows parity errors from on-board RAM memory to cause an NMI. When high, on-board RAM parity errors will not cause an NMI.
1	SPK_DAT	Speaker Data: This bit is gated with the output of Counter 2 from the 82C54 megacell. When this bit is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When low, the SPKR output is forced low.
0	TIM2GAT_SPK	Speaker Timer 2 Gate: This bit goes to the gate 2 input on the 82C54 megacell to enable Counter 2 to produce a speaker frequency.

VLSI SPECIAL FEATURE
The port addresses F8h-FFh are reserved for coprocessor use in the IBM PC/AT. However, only F8h, FAh, FCh, and FEh are actually used. The VLSI Special Features (VSF) allows the use of unused port addresses in this range as well as special registers in the address range EEh-F7h.

The special registers provided for VLSI Special Features are Fast A20 (EEh), Fast Reset (EFh), Slow CPU (F4h), Fast CPU (F5h), Configuration Disable (F9h), and Configuration Enable (EBh).

This feature is controlled by the MISCSET Register. It is possible to disable the VSF functions mapped in the address range EEh-FFh if they conflict with a specific design implementation.

Miscellaneous Configuration Register (MISCSET)
The register MISCSET is used for controlling the VLSI Special Feature, enabling internal –RC generation with less delay, selecting cache controller speed, and configuring the interrupt pins for glitch-free operation.

MISCSET Register - Read/Write

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
MISCSET (14h)	–VSF	F1CTL	FASTRC	1	CACHSEL	RAMDRV	10/16 I/O	IRQIN
POR Values	0	0	0	1	1	MA9	0	1

Bit	Name	Function
7	–VSF	Enable I/O Space F0h-FFh: This bit is used to enable or disable the VSF options mapped into the coprocessor I/O space between F0h and FFh. When set, it disables the option. When 0, the options is enabled.
6	F1CTL	Coprocessor Software Reset: When low, a write to I/O port F1h causes generation of an RESNPX signal. When this bit is high, no RESNPX is generated by a write to F1h.
5	FASTRC	Fast –RC: For hardware compatibility, the internally generated –RC has 50 µs delay from the issuance of the command to write data FCh or FEh to port 0064h (which generates a low going 6 µs pulse on –RC). This delay can be removed using FASTRC bit. If set to 1, there is no delay introduced. The default value is 0.
4		Reserved: This bit is reserved and returns logic value 1 when read.
3		Reserved: This bit is reserved and returns logic value 1 when read.
2	RAMDRV	DRAM Interface Signal Drive: This bit determines the capacitive load on MA10-MA0 and –RAMW pins. If 0, the capacitive load limit is 150 pF. The limit is 300 pF if this bit is 1. This bit is software programmable and the value of it is the same as the state of MA9 at power-on reset.
1	10/16 IO	10/16 bit I/O Address Decode: When 0, full 16-bit address decode is performed. When set, 10 bit I/O decode is performed. The default value of this bit at power-on reset is 0.
0	IRQIN	Glitch-free Interrupt Request Pin Input: This bit, when set to 1, allows glitch-free input on the IRQ pins. The input to these pins then should be stable for at least 105 ns to generate an interrupt. The default value of this bit is 1.

DEDICATED INTERNAL CONTROL REGISTERS

The registers and features described below are a fully compatible superset of the VLSI Special Features (VSF). All port decodes are between E8h and FFh as shown in Table 18.

The dedicated EMS related I/O registers at E8h, EAh, and EBh are described in the section "EMS Index Register and EMS Data Ports".

TABLE 18. DEDICATED I/O CONTROL REGISTERS

Port Address	Function
E8h	EMS Index Register
E9h	Reserved
EAh	EMS Data Port Low Byte
EBh	EMS Data Port High Byte
ECh	Configuration Index Register
EDh	Configuration Data Port
EEh*†	Fast A20
EFh*†	Fast Reset
F0h	Coprocessor Busy Clear
F1h	Coprocessor Reset
F4h†	Slow CPU
F5h†	Fast CPU
F8h	Coprocessor
F9h†	Configuration Disable
FAh	Coprocessor
FBh†	Configuration Enable
FCh	Coprocessor
FEh	Coprocessor

* Also can be activated through port 92h for PS/2 compatibility.

† These decodes can be disabled in a case of a conflict.

Configuration Index Register - Read/Write

ECh	D7	D6	D5	D4	D3	D2	D1	D0
Config Index	X	X	X	X	X	X	X	X

The value written to this register is the 8-bit address of the Data Port which is accessed through the Data Port Register at I/O address EDh. All subsequent Data Port reads and writes access the register at this address until the Index Register is written with a new address. This register is readable. It always returns the last value written to it.

Configuration Data Port Register - Read/Write

EDh	D7	D6	D5	D4	D3	D2	D1	D0
Config Data	X	X	X	X	X	X	X	X

The registers accessible through I/O address EDh are summarized in the section "Register Summary". They are accessed by writing their addresses to the Index Register at I/O address ECh, then by accessing the Data Port at I/O address EDh.

Fast A20 Register - Read/Write

EEh (PC/AT)	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	1	1	1	1	1	1	1	1

92h (PS/2)	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	RESET

A dummy read enables A20 and returns a value of FFh. A dummy write disables A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the keyboard controller to control A20. This signal and the keyboard controller's A20 enable are ORed so that either event controls the A20 address line. Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the keyboard controller for strict PC/AT compatibility.

This register is also controlled via bit 1 of I/O Register 92h (Port A) for PS/2 compatibility. When bit 1 is high, A20 is active. When bit 1 is low, A20 is always 0. This feature is fully integrated with the Fast A20 control achieved through EEh; i.e., a dummy read of EEh followed by a read of bit 1 of port 92h returns a logic 1.

The register at EEh is controlled by the bit –VSF of the register MISCSET. –VSF should be 0 to access this register.

Fast CPU Reset Register - Read-Only

EFh (PC/AT)	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h (PS/2)	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	RESET

This register provides a fast alternative to the keyboard controller for resetting the CPU. A dummy read of EFh resets the processor and returns a value of FFh. This reset signal is internally ORed with the keyboard controller's reset signal, internal –RC, so that either event invokes a reset. This provides a much faster way for the system to jump between real and protected mode thus speeding up operation for OS/2. Reset timing is the same as described below for the Port A reset.

Fast CPU Reset can also be controlled via bit 0 of I/O Register 92h (Port A) for PS/2 compatibility. When RESET (bit 0) = 1, a reset operation is triggered after a minimum 6.72 µs delay. Reset pulses high for 16 CLK2s. This latch remains set until written again or until the SCAMP Controller is externally reset.

If bit –VSF of the MISCSET Register is 1, the Fast CPU Reset feature at EFh is disabled. The Fast Reset at 92h is always available as is the reset activated by the BIOS through the keyboard controller.

In order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low. Otherwise, the reset vector is not fetched and the system hangs. In some existing systems a Hot Reset without controlling A20 seems to work. However, this is because an error trap occurs which eventually supplies the reset vector to the system. A large number of software instructions occurs in this case and the result is a "not very fast" reset. Therefore, before issuing a Hot Reset command either via I/O port 92h or I/O port EFh as described above, one of the following must occur.

1) Set bit one to 1 in Port A. (Writing 03h to this register effectively accomplishes both goals with a single I/O instruction.)
2) Perform a dummy read of EEh to enable A20.

Coprocessor Control Registers - Write-Only

0F0h	D7	D6	D5	D4	D3	D2	D1	D0
Busy Clear	X	X	X	X	X	X	X	X

0F1h	D7	D6	D5	D4	D3	D2	D1	D0
Reset Coproc	X	X	X	X	X	X	X	X

A dummy write to I/O port F0h clears the D-flop which holds –BUSYCPU and PEREQCPU active after an –ERRORNPX signal occurs. This write is normally performed by the interrupt 13 service routine.

A dummy write to I/O port F1h resets the coprocessor. This write results in a positive pulse 40 CLK2 cycles wide and synchronized to CLK2. –READYO is held inactive for an additional 50 CLK2 cycles following the falling edge of RESNPX. Bit 6 of the MISCSET Register must be set to 0, otherwise a write to F1h does not cause a reset. This feature is provided for 387SX compatibility concerns. The 387SX is not put into the same state by reset as is a 286. An FNINT software instruction is also required for initializing the 387SX coprocessor.

CPU Speed Control Registers - Write-Only

0F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU	X	X	X	X	X	X	X	X

0F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU	X	X	X	X	X	X	X	X

A dummy write to port 0F5h causes the CPU to run at normal "fast" speed. A dummy write to port 0F4h invokes the CLK2 divider circuit. This is selected by writing the appropriate code to the MISCSET Register. The programmable range provided allows 12 to 33 MHz systems to run at or below 8 MHz. Default on reset is "fast" speed.

CPU speed control registers are controlled by the bit –VSF in the MISCSET Register. –VSF should be 0 to enable these registers. However, if –VSF is disabled, it is still possible to control the CPU speed with the keyboard controller if allowed by the BIOS.

An I/O read operation on these two addresses returns undefined data.

Configuration Enable/Disable Registers - Write-Only

0FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

0F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described below, the Configuration Registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A dummy write to 0FBh enables the Configuration Registers. A dummy write to 0F9h disables the Configuration Registers.

When disabled, the system is locked out from any write access to the configuration and control ports from address E8h through EFh. This includes the registers previously described in this subsection, the EMS Registers described in the section "EMS System", Memory Card Registers, and the Configuration Indexed Registers.

If bit –VSF of the MISCSET Register is disabled, the Configuration Enable/Disable feature is also disabled.

An I/O read operation from these two addresses returns undefined data.

Ports 0F9h and 0FBh control access to the Configuration Registers. A dummy write to 0FBh enables access. A dummy write to 0F9h disables access.

PARITY GENERATION AND DETECTION CIRCUIT

Parity generation and detection is completely PC/AT compatible. System board memory write cycles generate two parity bits, one for each byte of the 16-bit word bank. These bits are written out in coincident with the data write. On a CPU read, both system board DRAM bytes feed the parity generator. The resulting two parity bits are compared to the two stored parity bits. In case of a match failure, the NMI interrupt is sent to the CPU. This latter event only occurs after the NMI interrupt is enabled via a write to its enable bit in Port B. On power-on reset the NMI is disabled. This allows the BIOS Post to initialize memory prior to NMI activation. False parity error detection is thus avoided.

IN-CIRCUIT TEST LOGIC

The SCAMP Controller is designed to make system board testing as easy as possible. The –TRI input causes all pins on the SCAMP Controller go to a high impedance state. This can be used to isolate the SCAMP Controller so other components in the system can be tested.

The –TRI input can also be used to put the SCAMP Controller into a special test mode called In-Circuit Test (ICT). The purpose of ICT is not to test the SCAMP Controller functionally while it is inserted in a circuit board, but to test that the part is connected correctly and all the pins can be toggled high and low in a predictable pattern. It uses a type of multiplexing scheme between inputs and outputs to allow easy access and testing of each pin.

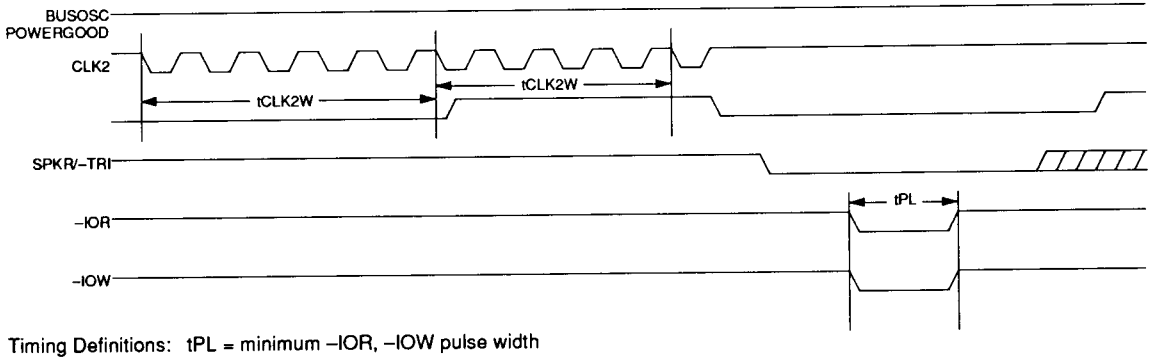
The SCAMP Controller has a number of internal test modes in order to completely test the functionality of the circuit. The test modes are disabled upon reset. In order to activate the ICT Mode, refer to the test mode timing diagram. If POWERGOOD is held low, the SPKR/–TRI pin becomes an input. Normally, this pin is pulled up by the internal pull-up resistor. If driven low during POWERGOOD low, all outputs and I/Os are three-stated. This can be used to isolate SCAMP Controller from other board components for debugging. The ICT Mode can then be invoked by toggling –IOR and –IOW together. The SPKR/–TRI pin should then be released (allowed to float) and the POWERGOOD input returned high. The ICT Mode will remain in effect until a reset is performed. Note that the BUSOSC and CLK2 input should be left inactive during the test register access, otherwise a reset will occur.

ICT MODE TIMING WAVEFORM - SCAMP CONTROLLER

The following procedure should be followed to place the SCAMP Controller into ICT Mode (refer to diagram below):

1. Drive POWERGOOD low.
2. Drive SPKR/–TRI pin low.
3. Invoke ICT mode by toggling –IOR and –IOW together.
4. Release SPKR/–TRI pin (i.e., allow it to float).
5. Return POWERGOOD high.

Important: CLK2 must initially be allowed to operate in conjunction with POWERGOOD as this is necessary to initialize internal logic. Once in ICT Mode, CLK2 and BUSOSC must not be allowed to operate as this will cause a system reset.



Timing Definitions: tPL = minimum –IOR, –IOW pulse width
tPL = 100 ns
tCLK2W = minimum 25 CLK2s

TABLE 19. PIN ASSIGNMENT FOR IN-CIRCUIT TEST

ICT Input		ICT Output		ICT Input		ICT Output		ICT Input		ICT Output	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
OSC	2	T/C	1	–CAS1	90	INTR	82	CPUHLDA	40	AD22	59
–MEMCS16	3	DBUS0	41	–CAS0	91	NMI	83	CPUA20	62	AD20	63
–IOCS16	4	DBUS1	42	–RAMWR	92	PEREQCPU	85	RESCPU	87	DBUS14	55
IRQ10	5	DBUS2	43	–RAS1	93	–BUSYCPU	86	–CAS3	88	DBUS15	56
IRQ11	6	DBUS3	44	–RAS0	95	AD21	60	–CAS2	89	AD3	80
IRQ12	7	DBUS4	45	MA0	97	AD19	64	TCKL2	120	–SDREAD	122
IRQ15	8	DBUS5	46	MA1	98	AD18	65	BUSOSC	121	–SDEN_HI	123
IRQ14	9	DBUS6	47	MA2	99	AD17	66	POWERGOOD	124	–DKEN	125
–MEMR	14	SA0	12	MA3	101	AD16	67	SPKR	126	–ROMCS	127
–MEMW	16	BALE	10	MA4	102	AD15	68	–SLEEP/–MISS	128	SD7	136
DRQ0	17	EALE	11	MA5	103	AD14	69	–IOCHK	129	AD2	81
DRQ5	18	DBUS7	48	MA6	104	AD13	70	–IOW	149	–SMEMR	148
DRQ6	19	DBUS8	49	MA7	106	AD12	71	–IOR	150	–REF	151
DRQ7	21	DBUS9	50	MA8	108	AD11	72	DRQ3	154	SYSCLK	152
–MASTER	23	DBUS10	51	MA9	109	AD10	73	IRQ4	159	–SMEMW	146
PEREQNPX	24	–S0/DK2	28	MA10	110	AD9	74	IRQ3	160	BAEN	147
RESNPX	25	–S1/DK1	29	–RAS2	111	AD8	75	IRQ9	130	SD6	137
BUSYNPX	26	DBUS11	52	–RAS3	112	AD7	76	DRQ2	131	SD5	138
–ERRORNPX	27	DBUS12	53	–PPICS	115	PAR0	113	–WS0	132	SD4	139
CLK2IN	35	DBUS13	54	–BLKA20	116	PAR1	114	IOCHRDY	133	RSTDRV	135
–BLE/AD0	34	M/–IO/DK0	30	IRQ8	117	AD6	77	DRQ1	155	SD3	140
CLK2	37	–BHE	31	IRQ1	118	AD5	78	IRQ7	156	SD2	142
–READYO	38	–ADS/–NPCS	32	TURBO	119	AD4	79	IRQ6	157	SD1	144
CPUHRQ	39	AD1	33			AD23	58	IRQ5	158	SD0	145

SPECIAL SCAMP CONTROLLER CYCLES AND RESET OPTIONS

HALT/SHUTDOWN Cycles

The SCAMP Controller detects and responds as described below to HALT and SHUTDOWN operations from the 286 and 386SX processors.

The SCAMP Controller detects HALT only to differentiate it from the SHUTDOWN cycle. No further action is taken in response to HALT except to acknowledge it by asserting –READYO. However, the BIOS, customized operating system, or software driver can use HALT in conjunction with the built-in Sleep Mode features to minimize power consumption and maximize battery life in portable systems.

VL82C310 Only - A HALT operation is performed in response to a HALT software instruction. Its intended use in a VL82C310-based system is in conjunction with the Sleep Mode functions described in the section "Sleep Mode Operation". The system is placed into Sleep Mode by writing the desired control bits to the Sleep Register. Software then executes the HALT instruction for minimum system power consumption. Any interrupting source, usually a timer or the keyboard, brings the CPU out of the HALT Mode. It then writes the Sleep Register in order to turn off the Sleep Mode. This brings the system back to full, high speed functionality.

SHUTDOWN is handled differently. This bus cycle is executed by the CPU in response to a critical internal processing error. SCAMP Controller responds by issuing a CPU-only reset for 16 CLK2 cycles. More detail on the CPU-only reset sequence is discussed in the section "CPU-Only Reset".

Detection of a HALT or SHUTDOWN cycle causes the SCAMP Controller to activate its –READYO signal after a one wait state delay.

ISA Cycles

When in the CPU Mode, the 82288 megacell is responsible for generating the command (–IOR, –IOW, –MEMR, –MEMW, –SMEMR, and –SMEMW) signals, BALE, and the timing for when the SA bus will be valid. The SCAMP Controller samples the inputs –MEMCS16, –IOCS16, –IOCHRDY and –WS0 and determines the length in wait states of each bus cycle.

Coprocessor Cycles

The SCAMP Controller generates a –READYO signal in one wait state during the coprocessor read cycles and in zero wait state during the coprocessor write cycles when in the 386SX Mode. In 286 Mode, coprocessor cycles are run as on-board slot bus cycles.

System Reset Options

This section describes all Reset Modes of the SCAMP Controller based on their activating signal. They have been discussed in other applicable sections of this document and are summarized in one place as an aid to the reader.

POWERGOOD — This signal causes all internal state machines to be reset. The internal Configuration Registers are reset to their default values shown in Table 23. A reset is issued to the CPU and the coprocessor via the RESCPU and RESNPX signals. RSTDRV is generated from POWERGOOD and is synchronized with BUSOSC. The –BUSYCPU signal is active for eight CLK2 cycles before and after the falling edge of the RESCPU signal. This invokes the Self-test Mode of the 386SX. Systems that desire to use this feature can then read the result of this test in the 386SX's EAX Register and decide what to do based on the result. Otherwise, it can be ignored. This has no effect on 286 systems.

REG_{92} — Setting bit 0 of I/O port 92h causes a CPU-only reset after a 6.72 µs delay. RESCPU is activated for 16 CLK2 cycles. See the section "Fast CPU Reset Register" for more details.

REG_{EF} — A dummy read of I/O port EFh causes a CPU-only reset after a 6.72 µs delay. RESCPU is activated for 16 CLK2 cycles. VLSI Special Features must be enabled for this feature to function. See the section "Fast CPU Reset Register" for more details.

OUT_64 — The CPU is reset when the I/O port 64h is loaded with value FCh or FEh. This generates an internal reset signal equivalent to –RC from a keyboard controller. The internal –RC is active after 6.72 µs or about 50 µs delay depending on the value of bit FASTRC in MISCSET Register. The pulse width of this signal is 16 CLK2 cycles. It generates RESCPU.

TABLE 20. 286 HALT/SHUTDOWN DETECTION

M/–IO	–S1	–S0	A1	Mode
1	0	0	1	HALT
1	0	0	0	SHUTDOWN

TABLE 21. 386SX HALT/SHUTDOWN DETECTION

M/–IO	D/–C	W/–R	A1	Mode
1	0	1	1	HALT
1	0	1	0	SHUTDOWN

OUT_F1 A dummy write to I/O port F1h causes a coprocessor-only reset. RESNPX is activated for 40 CLK2 cycles. Assertion of –READYO is delayed for 50 CLK2 cycles after RESNPX is deactivated. See the section "Coprocessor Control Registers" for details.

SHUT-DOWN Detection of the SHUTDOWN condition causes a CPU-only reset for 16 CLK2 cycles. See the section "HALT/ SHUTDOWN Cycles" for additional information.

REGISTER SUMMARY

System Configuration

The SCAMP Controller offers hardware configurable options so that a generic BIOS can be used for a system designed with the either the VL82C310, VL82C311, or VL82C311L. Table 22 details the mapping.

TABLE 22. CONFIGURATION REGISTER SUMMARY

Pin	Register Name	Register Bit	Bit Name	Functional Description	Default
MA3-MA0	RAMMAP	3-0	MEMAP3-MEMAP0	Memory Map Code 3-0 (Refer to Tables 1 and 2)	0000
MA4	RAMMAP	4	REMP384	Remap 384K DRAM (A0000-FFFFFh) 0 = Disabled 1 = Enabled	0
MA5	RAMSET	4	DRAMWS	DRAM Wait States 0 = 0 Wait state 1 = 1 Wait state	1
MA6	RAMSET	2	–PGMD	Page Mode Enable 0 = Enabled 1 = Disabled	1
MA7	RAMMAP	5	ROMMOV0	System and Slot ROM Move (Refer to Table 8)	00
MA8	RAMMAP	6	ROMMOV1		
MA9	MISCSET	2	RAMDRV	MA and –RAMW Drive 0 = 150 pF 1 = 300 pF	0
MA10	BUSCTL	7	ROMWID	ROM Width 0 = 8-bit 1 = 16-bit	
PAR0	ROMDMA	6	ROMWS0	BIOS ROM Wait State 0 / BIOS ROM Wait State 1 / Determine ROM Wait States: 00 = 3 wait states 01 = 1 wait state 10 = 2 wait states 11= 3 wait states	00
PAR1	ROMDMA	7	ROMWS1		
–RAMW				Processor Type 0 = 286 1 = 386SX	
–DKEN	CLKCTL	1	SCLKDIV1	Slow Clock Divider Bits 1 and 0 / Selects the SYSCLK frequency / where Clock is BUSOSC or TCLK2 00 = Clock +2 01 = Clock +4 10 = Clock +6 11 = Clock +8	01
–PPICS	CLKCTL	0	SCLKDIV0		
–ROMCS	BUSCTL	6	SLTDRV	Slot Current Drive 0 = 12 mA 1 = 24 mA	0
–SDREAD				System Configuration 0 = Externally configured 1 = Internal default	

SUMMARY OF CONFIGURATION REGISTERS

Index Port (R/W) **ECh**

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Index Address of a Configuration Register

Data Port (R/W) **EDh**

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Data for a Configuration Register

Version (R-O) **00h**

7	6	5	4	3	2	1	0
1	1	0	1	0	0	0	1

3 1 0 VL82C310 Version

Slot Pointer - SLTPTR (R/W) **02h**

7	6	5	4	3	2	1	0
A23	A22	A21	A20	A19	A18	A17	A16

64K Boundary between Board and Slot Memory

DRAM Map Register - RAMMAP (R/W) **03h**

7	6	5	4	3	2	1	0
	ROMMOV1, ROMMOV0		REMP384	MEMAP3	MEMAP2	MEMAP1	MEMAP0

System and Slot ROM Location Code

Remap 384K Memory
0 = Disable
1 = Enable

DRAM Memory Map Code

Reserved bit, returns 1 when read.

SUMMARY OF CONFIGURATION REGISTERS (Cont.)

DRAM Control Register - RAMSET (R/W) **05h**

7	6	5	4	3	2	1	0
			DRAMWS	–FASTSX	–PGMD	–ENPAR	RASOFF

- DRAMWS: DRAM Wait States; 0 = 0 Wait State; 1 = 1 Wait States
- –FASTSX: Wait States for Page-Miss/Bank-Hit cycles in 386SX System; 0 = 2 Wait States; 1 = 3 Wait States
- –PGMD: Enable Page Mode; 0 = Enable; 1 = Disable
- –ENPAR: Enable Parity Gen/Check; 0 = Enable; 1 = Disable
- RASOFF: RAS Shut-off (VL82C310 Only); 0 = No Shut-off; 1 = Shut-off Unused RAS

Refresh Control Register - REFCTL (R/W) **06h**

7	6	5	4	3	2	1	0
						CASREF	REFSPD

- CASREF: Refresh Mode; 0 = RAS Only; 1 = CAS before RAS
- REFSPD: Refresh Period; 0 = 15.625 µs (Standard); 1 = 125 µs (Slow)

Clock Control Register - CLKCTL (R/W) **07h**

7	6	5	4	3	2	1	0
ENVDSP	CLK2DIV1, CLK2DIV0		FCLKDIV1, FCLKDIV0		BOSCSNS	SCLKDIV1, SCLKDIV0	

- ENVDSP: Enable SYSCLK Freq Change in Video DRAM Address Range; 0 = Disable; 1 = Enable
- CLK2DIV1, CLK2DIV0: CLK2 Divider, Non-Turbo Mode; 00 = CLK2 = TCLK2 + 1; 01 = CLK2 = TCLK2 + 2; 10 = CLK2 = TCLK2 + 3; 11 = CLK2 = TCLK2 + 4
- FCLKDIV1, FCLKDIV0: Fast Clock Divider; 00 = +2; 01 = +4; 10 = +6; 11 = No Change
- BOSCSNS: BUSOSC Pin Status; 0 = Slow Clock; 1 = Fast Clock
- SCLKDIV1, SCLKDIV0: Slow Clock Divider; 00 = +2; 01 = +4; 10 = +6; 11 = +8

Memory Card Control Register - MCDCTL (R/W) (VL82C310 Only) **0Ah**

7	6	5	4	3	2	1	0
				MCPGEN3	MCPGEN2	MCPGEN1	MCPGEN0

- MCPGEN3–MCPGEN0: JEIDA IC Memory Card Page 3-0 Enable; 0 = Disable; 1 = Enable

Reserved bit, returns 1 when read.

SUMMARY OF CONFIGURATION REGISTERS (Cont.)

EMS Configuration Register 1 - EMSEN1 (R/W) **0Bh**

7	6	5	4	3	2	1	0
EMSENAB	BFENAB		EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
Enable EMS 0 = Disable 1 = Enable	Enable Backfill 0 = Disable 1 = Enable		EMS Mapping 0 = Map C0000h-EFFFFh 1 = Map A0000h-BFFFFh, D0000h-DFFFFh	Enable BC000 or EC000 Segment 0 = Disable 1 = Enable	Enable B8000 or E8000 Segment	Enable B4000 or E4000 Segment	Enable B0000 or E0000 Segment

EMS Configuration Register 2 - EMSEN2 (R/W) **0Ch**

7	6	5	4	3	2	1	0
DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
Enable DC000 Segment 0 = Disable 1 = Enable	Enable D8000 Segment 0 = Disable 1 = Enable	Enable D4000 Segment 0 = Disable 1 = Enable	Enable D0000 Segment 0 = Disable 1 = Enable	Enable AC000 or CC000 Segment 0 = Disable 1 = Enable	Enable A8000 or C8000 Segment 0 = Disable 1 = Enable	Enable A4000 or C4000 Segment 0 = Disable 1 = Enable	Enable A0000 or C0000 Segment 0 = Disable 1 = Enable

A0000h-BFFFFh Segment Access Control Register - ABAXS (R/W) **0Eh**

7	6	5	4	3	2	1	0
B8000 Access		B0000 Access		A8000 Access		A0000 Access	

C0000h-CFFFFh Segment Access Control Register - CAXS (R/W) **0Fh**

7	6	5	4	3	2	1	0
CC000 Access		C8000 Access		C4000 Access		C0000 Access	

D0000-DFFFFh Segment Access Control Register - DAXS (R/W) **10h**

7	6	5	4	3	2	1	0
DC000 Access		D8000 Access		D4000 Access		D0000 Access	

E0000-FFFFF Segment Access Control Register - FEAXS (R/W) **11h**

7	6	5	4	3	2	1	0
F8000 Access		F8000 Access		E8000 Access		E0000 Access	

00 = Read/Write Slot Bus
01 = Read Slot, Write System Board
10 = Read System Board, Write Slot Bus
11 = Read/Write System Board

Reserved bit, returns 1 when read.

SUMMARY OF CONFIGURATION REGISTERS (Cont.)

Sleep Mode Control Register - SLPCTL (R/W) VL82C310 Only) 13h

7	6	5	4	3	2	1	0
SLP	DIVCLK3	DIVCLK2	DIVCLK1	DIVCLK0	SLPSTS	PINFNC	ENSYSCK

- SLP: Sleep Mode 0 = Disable 1 = Enable Forced to 1 if 311
- DIVCLK3-DIVCLK0: Power Down TCLK2 Divider
  0000 = +1, 0001 = +4, 0010 = +8, 0011 = +12, 0100 = +16, 0101 = +64, 0110 = +128, 0111 = +256, 1000 = +1024
- SLPSTS: Status of –SLEEP/–MISS Pin (Read-only bit)
- PINFNC: Pin functionality of –SLEEP/–MISS in VL82C310: 1 = –MISS 0 = –SLEEP. Always 0 in VL82C311/ VL82C311L. This bit should never be written, it is reserved for a special test mode.
- ENSYSCK: System Clock Enable 0 = Disable 1 = Enable

Miscellaneous Control Register - MISCSET (R/W) 14h

7	6	5	4	3	2	1	0
–VSF	F1CTL	FASTRC			RAMDRV	10/16 IO	IRQIN

- –VSF: VLSI Special Feature (Enable IO Space EEh-FFh) 0 = Enable 1 = Disable
- F1CTL: Coprocessor Software Reset 0 = Enable 1 = Disable
- FASTRC: Fast Internal –RC 0 = Disable 1 = Enable
- RAMDRV: MA10-MA0 and –RAMW Drive 0 = 150 pF 1 = 300 pF
- 10/16 IO: 10/16 Bit I/O Address Decode 0 = 16 Bit Decode 1 = 10 Bit Decode
- IRQIN: Glitch-free Interrupt Request Input 0 = Disable 1 = Enable

ROM and DMA Control Register - ROMDMA (R/W) 15h

7	6	5	4	3	2	1	0
ROMWS1	ROMWS0	DMAWS8(1), DMAWS8(0)		DMAWS16(1), DMAWS16(0)		DMACLK	MEMTM

- ROMWS1-ROMWS0: ROM Wait States 00 = 3, 10 = 2, 01 = 1, 11 = 3
- DMAWS8(1), DMAWS8(0): 8-Bit Wait States 00 = 2, 10 = 3, 01 = 4, 11 = 3
- DMAWS16(1), DMAWS16(0): 16-Bit Wait States 00 = 2, 10 = 3, 01 = 4, 11 = 3
- DMACLK: DMA Clock 0 = SYSCLK/2 1 = SYSCLK
- MEMTM: DMA –MEMR Signal Delay 0 = PC/AT Compat. 1 = 1 DMACLK Early

Bus Control Register - BUSCTL (R/W) 16h

7	6	5	4	3	2	1	0
ROMWID	SLTDRV	DSKTMG		CMDLY2	CMDLY1	16WS	8WS

- ROMWID: BIOS ROM Width 0 = 8-Bit 1 = 16-Bit
- SLTDRV: Slot Current Drive 0 = 12 mA 1 = 24 mA
- DSKTMG: Disk I/O Timing 0 = Slow Programmed I/O 1 = Normal Programmed I/O
- CMDLY2: Command Delay for 8-, 16-Bit I/O and 8-Bit Memory Cycles 0 = 0 1 = 1
- CMDLY1: Command Delay for 16-Bit Memory Cycles 0 = 0 1 = 1
- 16WS: 16-Bit Wait States 0 = 0 1 = 1
- 8WS: 8-Bit Wait States 0 = 4 1 = 5

Reserved bit, returns 1 when read.

Version (00h)
D2-D7 contain a read-only code which indicates that this part is a VLSI Technology, Inc. SCAMP Controller. D0 and D1 contain the version number of this chip. By using this byte a smart BIOS can compensate for "feature" differences based on the version number. The first version of the SCAMP Controller contains the code D2h. Breaking the code into two bit pieces reveals the code to be "310" Rev "2". The code in the VL82C311 and VL82C311L is D6h.

Index Register
The value written to this register is the eight bit address of the Data Port which is accessed through the Data Port Register at I/O address EDh. All subsequent Data Port reads and writes access the register at this address until the Index Register is written with a new address. This register is readable. It always returns the last value written to it.

The Index Register in the SCAMP Controller is read/write.

Data Port Register
Each register accessible through I/O address EDh is functionally described in the Table 23. It is accessed first by writing its address to the Index Register at I/O address ECh, then by accessing the Data Port at I/O address EDh.

TABLE 23. INDEXED CONFIGURATION REGISTERS MAP

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	Index Port	A7	A6	A5	A4	A3	A2	A1	A0
EDh (R/W)	Data Port	D7	D6	D5	D4	D3	D2	D1	D0
00h (R-O)	VER	1	1	0	1	0	0	0	1
02h (R/W)	SLTPTR	A23	A22	A21	A20	A19	A18	A17	A16
03h (R/W)	RAMMAP	1	ROMMOV1, ROMMOV0		REMP384	MEMAP3	MEMAP2	MEMAP1	MEMAP0
05h (R/W)	RAMSET	1	1	1	DRAMWS	–FASTSX	–PGMD	–ENPAR	RASOFF
06h (R/W)	REFCTL	1	1	1	1	1	1	CASREF	REFSPD
07h (R/W)	CLKCTL	ENVDSP	CLK2DIV1, CLK2DIV0		FCLK2DIV1, FCLK2DIV0		BOSCSNS	SCLKDIV1, SCLKDIV0	
0Ah (R/W)	MCDCTL	1	1	1	1	MCPGEN3	MCPGEN2	MCPGEN1	MCPGEN0
0Bh (R/W)	EMSEN1	EMSENAB	BFENAB	1	EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
0Ch (R/W)	EMSEN2	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
0Eh (R/W)	ABAXS	B8000 Access		B0000 Access		A8000 Access		A0000 Access	
0Fh (R/W)	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10h (R/W)	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11h (R/W)	FEAXS	F8000 Access		F0000 Access		E8000 Access		E0000 Access	
13h (R/W)	SLPCTL	SLP	DIVCLK3-DIVCLK0				SLPSTS	PINFNC	ENSYCK
14h (R/W)	MISCSET	–VSF	F1CTL	FASTRC	1	1	RAMDRV	10/16IO	IRQIN
15h (R/W)	ROMDMA	ROMWS1	ROMWS0	DMAWS8(1), DMAWS8(0)		DMAWS16(1), DMAWS16(0)		DMACLK	MEMTM
16h (R/W)	BUSCTL	ROMWID	STLDRV	DSKTMG	1	CMDLY2	CMDLY1	16WS	8WS

TABLE 24. INDEXED CONFIGURATION REGISTERS RESET VALUES

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h (R-O)*	VER	1	1	0	1	0	0	0	1
02h (R/W)	SLTPTR	1	1	1	1	1	1	1	1
03h (R/W)	RAMMAP	1	MA8	MA7	MA4	MA3	MA2	MA1	MA0
05h (R/W)	RAMSET	1	1	1	MA5	0	MA6	0	0
06h (R/W)	REFCTL	1	1	1	1	1	1	0	0
07h (R/W)	CLKCTL	0	0	0	1	0	Note 1	–DKEN	–PPICS
0Ah (R/W)	MCDCTL	1	1	1	1	0	0	0	0
0Bh (R/W)	EMSEN1	0	0	1	0	0	0	0	0
0Ch (R/W)	EMSEN2	0	0	0	0	0	0	0	0
0Eh (R/W)	ABAXS	0	0	0	0	0	0	0	0
0Fh (R/W)	CAXS	0	0	0	0	0	0	0	0
10h (R/W)	DAXS	0	0	0	0	0	0	0	0
11h (R/W)	FEAXS	0	0	0	0	0	0	0	0
13h (R/W)	SLPCTL	0	0	0	0	0	–SLEEP	0	1
14h (R/W)	MISCSET	0	0	0	1	1	MA9	0	1
15h (R/W)	ROMDMA	PAR1	PAR0	1	1	1	0	0	0
16h (R/W)	BUSCTL	MA10	–ROMCS	1	1	0	0	0	0

Notes: * The reset value of VER is binary 11010101 in the VL82C311 and VL82C311L.

1. The default value of this bit is dependent on the external clock BUSOSC. If there is an external clock connected to the BOSOSC pin, the reset value is 0, otherwise the status of the BUSOSC pin is reflected in this bit.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
t1	TCLK2 Period	25		20		ns	
t2	TCLK2 High Time	10		8		ns	
t3	TCLK2 Low Time	10		8		ns	
t4	BUSOSC Period	31		31		ns	
t5	BUSOSC High Time	12		12		ns	
t6	BUSOSC Low Time	12		12		ns	
t7	CLK2IN High Time	8		8		ns	
t8	CLK2IN Low Time	8		8		ns	
t9	CLK2 Fall Time		5		5	ns	CL = 50 pF
t10	CLK2 Rise Time		5		5	ns	CL = 50 pF
tD11	TCLK2 to CLK2 Delay	4	35	4	35	ns	CL = 50 pF
t12	SYSCLK Fall Time		10		10	ns	CL = 200 pF
t13	SYSCLK Rise Time		10		10	ns	CL = 200 pF
tD14	TCLK2 to SYSCLK Delay	5	48	5	48	ns	CL = 200 pF
tD14a	BUSOSC to SYSCLK Delay	5	50	5	50	ns	CL = 200 pF
t15	OSC High Time	20		20		ns	
t16	OSC Low Time	20		20		ns	
tD17	CLK2IN to RESCPU Delay	4	13	4	12	ns	CL = 30 pF
tD18	CLK2IN to RESNPX Delay	4	13	4	12	ns	CL = 30 pF
tD19	CLK2IN to –READYO Delay	4	25	4	20	ns	CL = 30 pF
tD20	CLK2IN to –EALE Delay	4	20	4	20	ns	CL = 50 pF

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
tD21	CLK2IN to –ROMCS Delay	4	25	4	25	ns	CL = 50 pF
tD22	CLK2IN to –BUSYCPU Delay	4	25	4	25	ns	CL = 50 pF
tD23	CLK2IN to MA10-MA0 Delay	4	21	4	18	ns	CL = 300 pF
tD24	A23-A1 to MA10-MA0 Delay	5	43	5	43	ns	CL = 300 pF, EMS On
tD24a	A23-A1 to MA10-MA0 Delay	5	35	15	35	ns	CL = 300 pF, EMS Off
tD25	CLK2IN to –RAS3 - –RAS0 Delay	4	16	4	13	ns	CL = 150 pf
tD26	CLK2IN to –CAS3 - –CAS0 Delay	4	16	4	13	ns	CL = 150 pF
tD27	CLK2IN to –RAMWR Delay	4	25	4	25	ns	CL = 300 pF
tD28	CLK2IN to D15-D0 Active Delay	4		4		ns	CL = 100 pF, from –READYO
tD29	CLK2INto D15-D0 Valid Delay		35		35	ns	CL = 100 pF
tD30	CLK2IN to D15-D0 Float Delay	4	25	4	25	ns	CL = 100 pF
tD31	CLK2IN to PAR1-PAR0 Active Delay	4	25	4	25	ns	CL = 50 pF, from –RAMWR
tD32	D15-D0 to PAR1-PAR0 Delay	3	20	3	20	ns	CL = 50 pF
tD33	CLK2IN to PAR1-PAR0 Float Delay	4	25	4	25	ns	CL = 50 pF
tD34	PEREQNPX to PEREQCPU Delay	3	25	3	25	ns	CL = 50 pF
tD35	–BUSYNPX High to PEREQCPU High Delay	3	25	3	25	ns	CL = 50 pF
tD36	–BUSYNPX to –BUSYCPU Delay	3	25	3	25	ns	CL = 50 pF
tD37	SYSCLK to BALE Delay	–6	10	–6	10	ns	CL = 200 pF
tD38	SYSCLK to –CMD Delay	–6	17	–6	17	ns	CL = 200 pF
tD39	SYSCLK to –SCMD Valid Delay	–6	17	–6	17	ns	CL = 200 pF

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
tD40	SYSCLK to –SCMD Active Delay	–5	25	–5	25	ns	CL = 200 pF
tD41	SYSCLK to –SCMD Float Delay	–5	25	–5	25	ns	CL = 200 pF
tD42	CLK2IN to –PPICS Delay	4	40	4	40	ns	CL = 50 pF
tD43	CLK2IN to SA0 Delay	4	32	4	32	ns	CL = 200 pF
tD44	SYSCLK to SA0 Delay (Conv.)	–5	16	–5	16	ns	CL = 200 pF
tD45	SYSCLK to SD7-SD0 Active Delay	–1		–1		ns	CL = 200 pF
tD46	SYSCLK to SD7-SD0 Valid Delay		35		35	ns	CL = 200 pF
tD47	SYSCLK to SD7-SD0 Float Delay	–2	30	–2	30	ns	CL = 200 pF
tD48	SYSCLK to –SDREAD Delay	–2	30	–2	30	ns	CL = 50 pF
tD49	SYSCLK to –SDEN_HI Delay	–2	30	–2	30	ns	CL = 50 pF
tD50	–IOCS16 to –SDREAD, –SDEN_HI	4	32	4	32	ns	CL = 50 pF
tD51	CLK2IN to NMI Delay (Parity Error)	5	60	5	60	ns	CL = 50 pF
tD52	CPUA20 to A20 Delay	3	20	3	20	ns	CL = 50 pF
tD53	CLK2IN to MA10-MA0 Delay (Memory Card)	4	40	4	40	ns	CL = 300 pF
tD54	–IOW Low to PEREQCPU, –BUSYCPU	4	50	4	50	ns	CL = 50 pF
tD55	–IOW Inactive to BLKA20 Delay	4	50	4	50	ns	CL = 50 pF
tD56	–IOW Inactive to NMI,SPKR Delay	4	50	4	50	ns	CL = 50 pF
tD57	–IOR, –IOR Low to BLKA20 Delay	4	50	4	50	ns	CL = 50 pF
tSU60	–ADS to CLK2IN Setup Time	20		20		ns	

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
tH61	–ADS from CLK2IN Hold Time	5		5		ns	
tSU62	W/–R, M/–IO, D/–C to CLK2IN Setup	22		22		ns	
tH63	W/–R, M/–IO, D/–C from CLK2IN Hold	5		5		ns	
tSU64	A23-A21, CPUA20, A19-A1 to CLK2IN	20		20		ns	
tH65	A23-A21, CPUA20, A19-A1 from CLK2IN	4		4		ns	
tSU66	–BLE, –BHE to CLK2IN Setup Time	20		20		ns	
tSU66a	–BLE, –BHE to CLK2IN Setup Time	15		15		ns	Cache Enabled
tH67	–BLE, –BHE from CLK2IN Hold Time	4		4		ns	
tH67a	–BLE, –BHE from CLK2IN Hold Time	4		4		ns	Cache Enabled
tSU68	–SLEEP/–MISS Setup to CLK2IN	12		11		ns	Cache Enabled
tH69	–SLEEP/–MISS Hold from CLK2IN	4		4		ns	Cache Enabled
tSU70	D15-D0, PAR1-PAR0 to CLK2IN Setup	4		4		ns	
tH71	D15-D0, PAR1-PAR0 from CLK2IN Hold	13		13		ns	
tSU72	–MEMCS16 to SYSCLK Setup Time	35		35		ns	
tH73	–MEMCS16 from SYSCLK Hold	–2		–2		ns	
tSU74	–WS0 to SYSCLK Setup Time	33		33		ns	
tH75	–WS0 from SYSCLK Hold Time	–2		–2		ns	
tSU76	IOCHRDY to SYSCLK Setup Time	30		30		ns	
tH77	IOCHRDY from SYSCLK Hold Time	–2		–2		ns	
tSU78	–IOCS16 to SYSCLK Setup Time	35		35		ns	

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
tH79	–IOCS16 from SYSCLK Hold Time	–2		–2		ns	
tSU80	D15-D0 to SYSCLK Setup Time	35		35		ns	
tH81	D15-D0 to SYSCLK Hold Time	6		6			
tSU82	SD7-SD0 to SYSCLK Setup Time	35		35			
tH83	SD7-SD0 from SYSCLK Hold Time	6		6		ns	
tSU84	D15-D0 to SYSCLK Setup Time	75		75		ns	
tH85	D15-D0 from SYSCLK Hold Time	30		30		ns	
286 Mode Timing							
t1	TCLK2 Period	31		31		ns	
t7	CLK2IN High Time	12		12		ns	
t8	CLK2IN Low Time	12		12		ns	
tSU90	–S0/–S1 to CLK2IN Setup Time	13		13		ns	
tH91	–S0/–S1 from CLK2IN Hold Time	1		1		ns	
tSU92	M/–IO to CLK2IN Setup Time	35		35		ns	
tH93	M/–IO from CLK2IN Hold Time	1		1		ns	
tSU94	A23-A21, CPUA20, A19-A0, –BLE	35		35		ns	Setup to CLK2IN
tH95	A23-A21, CPUA20, A19-A0, –BLE	10		10		ns	Hold from CLK2IN
tSU96	–BHE to CLK2IN Setup Time	4		4		ns	
tH97	–BHE from CLK2IN Hold Time	1		1		ns	
tD98	CLK2IN to –NPCS Delay	4	25	4	25	ns	

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
Bus Arbitration Timing							
tD101	CLK2IN to HRQ Delay	4	25	4	25	ns	CL = 50 pF
tSU102	HLDA to CLK2IN Setup Time	15		15		ns	
tH103	HLDA from CLK2IN Hold Time	4		4		ns	
tD104	–MASTER to AEN Delay	3	35	3	35	ns	CL = 200 pF
tD105	HLDA to AEN Delay	3	35	3	35	ns	CL = 200 pF
tD106	HLDA to BALE Delay	3	35	3	35	ns	CL = 200 pF
tD107	–REFRESH to SA0, –MEMR, –SMEMR	3	30	3	30	ns	CL = 200 pF, Active
tD108	–REFRESH to SA0, –MEMR, –SMEMR	3	30	3	30	ns	CL = 200 pF, Float
tD109	–REFRESH to A23-A1, CPUA20, –BLE, –BHE	3	30	3	30	ns	CL = 50 pF, Active
tD110	–REFRESH to A23-A1, CPUA20, –BLE, –BHE	3	30	3	30	ns	CL = 50 pF, Float
tD111	HLDA High to SA0, –CMD Float	3	30	3	30	ns	CL = 200 pF
tD112	HLDA Low to SA0, –CMD Active	3	30	3	30	ns	CL = 200 pF
tD113	–MASTER Low to A20 Float	3	25	3	25	ns	CL = 50 pF
tD114	–MASTER High to A20 Active	3	25	3	25	ns	CL = 50 pF
tD115	–MASTER Low to CPUA20 Active	3	25	3	25	ns	CL = 50 pF
tD116	–MASTER High to CPUA20 Float	3	25	3	25	ns	CL = 50 pF
Interrupt Timing							
t117	Ext Interrupt Req Pulse Width Active	105		105		ns	
tD118	Ext IRQ to INTR High Delay	5	130	5	130	ns	CL = 50 pF

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
Interrupt Timing (Cont.)							
tD120	OSC to INTR High Delay	5	130	5	130	ns	CL = 50 pF
tD120a	OSC to INTR Delay	3	200	3	200	ns	CL = 50 pF
tSU121	Ext Interrupt to OSC Setup Time		15		15	ns	
tH122	Ext Interrupt from OSC Hold Time		10		10	ns	
tD123	–IOCHK to NMI Delay	3	40	3	40	ns	CL = 50 pF
tD124	–ERRORNPX Low to INTR Delay	5	150	5	150	ns	CL = 50 pF
Miscellaneous Timing							
t126	–IOCHCK Pulse Width	15		15		ns	
tSU127	POWERGOOD to OSC Setup Time	15		15		ns	
tH128	POWERGOOD from OSC Hold	10		10		ns	
tD129	SYSCLK to RSTDRV Delay	–10	20	–10	20	ns	CL = 200 pF
tD130	OSC to SPKR Delay	5	120	5	120	ns	CL = 50 pF
tD131	CLK2IN to MA10-MA0,–RAS3 - –RAS30, –CAS3 - –CAS0,–RAMW	4	50	4	50	ns	Active
DRAM Controller Timing (HLDA Cycles)							
tD132	–MEMW to –RAMW Delay	3	30	3	30	ns	CL = 300 pF
tD133	–MEMW/–MEMR to –RAS3 - –RAS0 Delay	4	25	4	25	ns	CL = 150 pF
tD134	OSC to -CAS3 - –CAS0 Low Delay	4	25	4	25	ns	CL = 150 pF
tD135	–MEMW/–MEMR to –CAS3 - –CAS0 High Delay	4	25	4	25	ns	CL = 150 pF

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
DRAM Controller Timing (HLDA cycles)							
tD136	OSC to MA10-MA0 Delay	5	35	5	35	ns	CL = 300 pF
tD137	A23-A1 to MA10-MA0 Delay (EMS On)	5	43	5	43	ns	CL = 300 pF
tD137a	A23-A1 to MA10-MA0 Delay (EMS Off)	5	35	5	35	ns	CL = 300 pF
tD138	A23-A14 to MA10-MA0 Delay (Memory Card)	5	45	5	45	ns	CL = 300 pF
tD139	–MEMW Low to PAR1-PAR0 Active Delay	4	25	4	25	ns	CL = 50 pF
tD140	–MEMW High to PAR1-PAR0 Float Delay	4	25	4	25	ns	CL = 50 pF
tD141	SD7-SD0 to PAR0 Delay Time	5	48	5	48	ns	CL = 50 pF
tD142	D15-D8 to PAR1 Delay Time	3	20	3	20	ns	CL = 50 pF
Data Steering Timing							
tD143	SD7-SD0 to D15-D8 Delay	4	30	4	30	ns	CL = 100 pF
tD144	SD7-SD0 to D7-D0 Delay	4	30	4	30	ns	CL = 100 pF
tD145	D7-D0 to SD7-D0 Delay	4	25	4	25	ns	CL = 200 pF
tD146	D15-D8 to SD7-SD0 Delay	4	25	4	25	ns	CL = 200 pF
tSU147	–IOCS16 to –IOR, –IOW Setup Time	15		15		ns	
tH148	–IOCS16 from –IOR, –IOW Hold Time	5		5		ns	
tSU149	–MEMCS16 to –MEMR, –MEMW	15		15		ns	Setup Time
tH150	–MEMCS16 from –MEMR, –MEMW	5		5		ns	Hold Time

Note: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
Master Mode Timing							
tD151	A20 to CPUA20 Delay	3	25	3	25	ns	CL = 50 pF
tD152	SA0 to A0/–BLE Delay	3	25	3	25	ns	CL = 50 pF
tD153	A23-A1, SA0 to –PPICS Delay	3	40	3	40	ns	CL = 50 pF
tD154	–MEMW/–MEMR to –SCMD Delay	3	30	3	30	ns	CL = 200 pF
tD155	A23-A20 to –SCMD Active Delay	3	25	3	25	ns	CL = 200 pF
tD156	A23-A20 to –SCMD Float Delay	3	25	3	25	ns	CL = 200 pF
tSU157	A23-A1, SA0, –BHE to –CMD Setup	30		30		ns	
tH158	A23-A1, SA0, –BHE from –CMD Hold	20		20		ns	
tSU161	SD7-SD0 to –IOW Setup Time	55		55		ns	
tH162	SD7-D0 from –IOW Hold Time	20		20		ns	
tSU163	D15-D8 to –IOW Setup Time	55		55		ns	
tH164	D15-D8 from –IOW Hold Time	20		20		ns	
tD165	–IOR low to SD7-SD0 Delay	5	120	5	120	ns	CL = 200 pF
tD165a	–IOR high to SD7-SD0 Float	4	30	4	30	ns	CL = 200 pF
tD166	–IOR Low to D15-D8 Delay	5	120	5	120	ns	CL = 100 pF
tD166a	–IOR High to D15-D9 Float	4	30	4	30	ns	CL = 100 pF
tD167	–CMD to –SDREAD Delay	4	30	4	30	ns	CL = 50 pF
tD172	–CMD Low to SD7-SD0 Active Delay	4	35	4	35	ns	CL = 200 pF
tD173	–CMD High to SD7-SD0 float Delay	4	35	4	35	ns	CL = 200 pF

Notes: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
Master Mode Timing (Cont.)							
tD174	–CMD low to D15-D0 Float Delay	4	35	4	35	ns	CL = 100 pF
tD175	SYSCLK to –REFRESH Float Delay	4	35	4	35	ns	CL = 100 pF
Refresh Mode Timing							
tD182	SYSCLK to –REFRESH Low Delay	–8	13	–8	13	ns	CL = 200 pF
tD183	SYSCLK to –REFRESH Float Delay	–7	18	–7	18	ns	CL = 200 pF
tD184	SYSCLK to SA0 Delay	–4	40	–4	40	ns	CL = 200 pF
tD185	SYSCLK to A16-A1, –BLE/A0 Delay	–4	40	–4	40	ns	CL = 50 pF
tD186	SYSCLK to MA10-MA0 Delay	–2	70	–2	70	ns	CL = 300 pF
tD188	SYSCLK to –MEMR Delay	–5	30	–5	30	ns	CL = 200 pF
tSU189	–REFRESH to SYSCLK Setup Time	30		30		ns	
tH189a	–REFRESH from SYSCLK Hold	5		5		ns	
tD190	SYSCLK to –SMEMR Delay	–5	30	–5	30	ns	CL = 200 pF
tD191	–REFRESH to –SMEMR Active Delay	4	40	4	40	ns	CL = 200 pF
tD192	–REFRESH to –SMEMR Float Delay	–5	30	–5	30	ns	CL = 200 pF
tSU193	IOCHRDY to SYSCLK Setup Time	25		25		ns	
tH194	IOCHRDY from SYSCLK Hold Time	0		0		ns	

Notes: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5V±5%, VSS = 0 V

Symbol	Parameter	20 MHz		25 MHz		Unit	Conditions
		Min	Max	Min	Max		
DMA Mode Timing							
tSU195	DRQ to SYSCLK Setup Time	20		20		ns	
tD197	SYSCLK to DK2-DK0 Active Delay					ns	
tD198	SYSCLK to DK2-DK0 Delay	–2	70	–2	70	ns	CL = 50 pF
tD199	SYSCLK to DK2-DK0 Float Delay					ns	CL = 50 pF
tD200	SYSCLK to –DKEN Delay	–2	70	–2	70	ns	CL = 50 pF
tD201	SYSCLK to –CMD Valid Delay	–5	60	–5	60	ns	CL = 200 pF
tD202	SYSCLK to A23-A1, CPUA20, –BLE, –BHE	0	90	0	90	ns	CL = 50 pF (Valid Delay)
tD205	SYSCLK to SA0 Valid Delay	0	95	0	95	ns	CL = 200 pF
tD205	SYSCLK to SA0 Valid Delay	0	95	0	95	ns	CL = 200 pF
tD205	SYSCLK to SA0 Valid Delay	0	95	0	95	ns	CL = 200 pF
tD205	SYSCLK to SA0 valid Delay	0	95	0	95	ns	CL = 200 pF
tD206	SYSCLK to T/C Delay	–5	60	–5	60	ns	CL = 100 pF
tSU207	IOCHRDY to SYSCLK Setup Time	25		25		ns	
tH208	IOCHRDY from SYSCLK Hold Time	15		15		ns	
tD209	SYSCLK to –SCMD Valid Delay	–5	60	–5	60	ns	CL = 200 pF
tD210	–SCMD Active from SYSCLK Delay					ns	CL = 200 pF
tD211	–SCMD Float from SYSCLK Delay					ns	CL = 200 pF

Notes: –CMD refers to signals –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to signals –SMEMR and –SMEMW.

TIMING DIAGRAMS

FIGURE 21. CLOCK TIMING

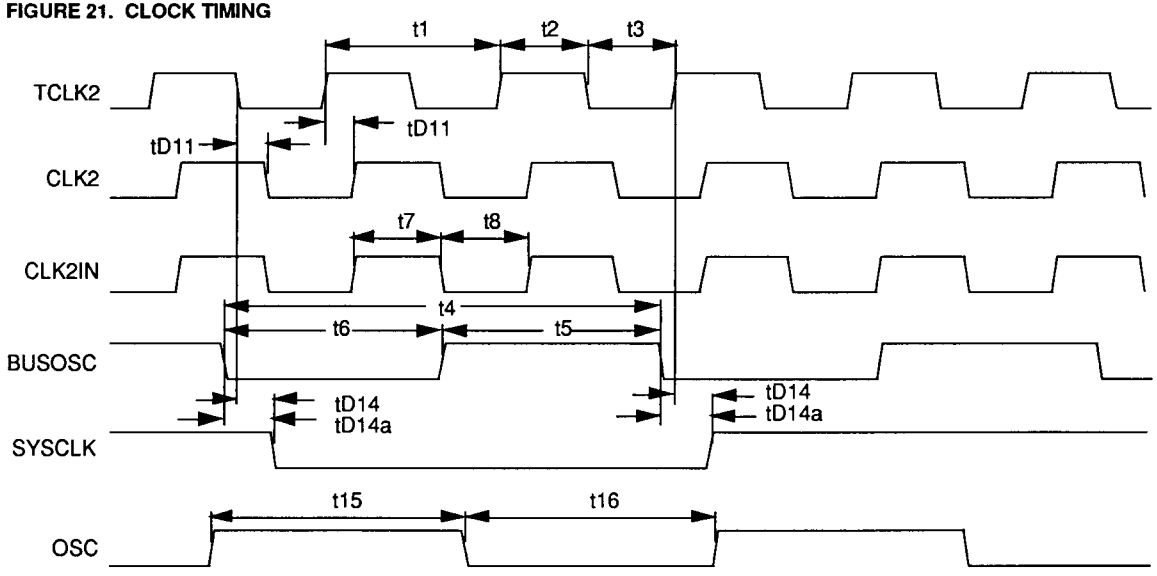


FIGURE 22. RESET TIMING

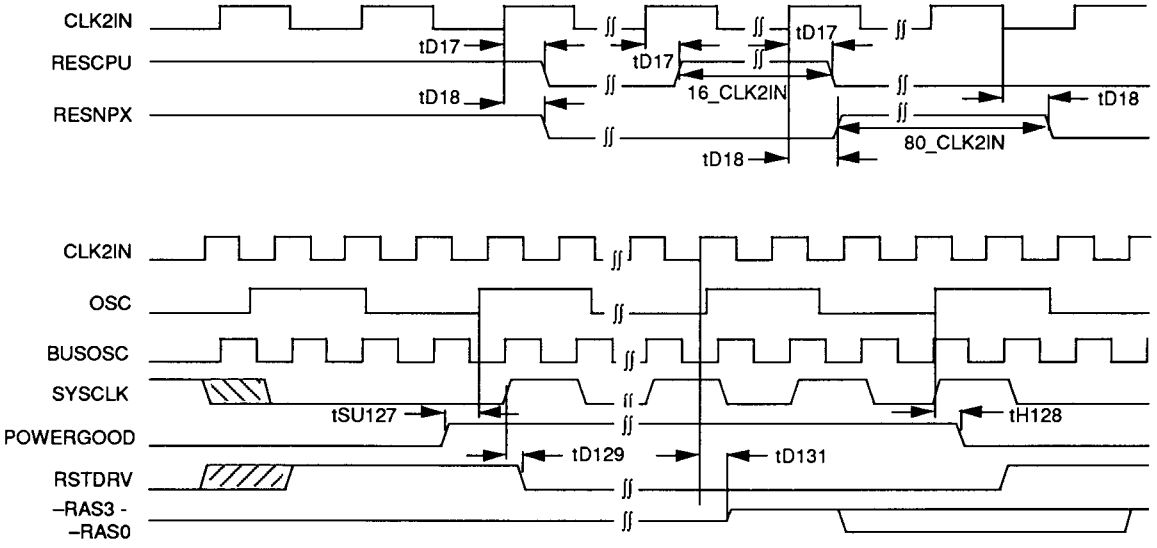


FIGURE 23. CPU INTERFACE TIMING - 286

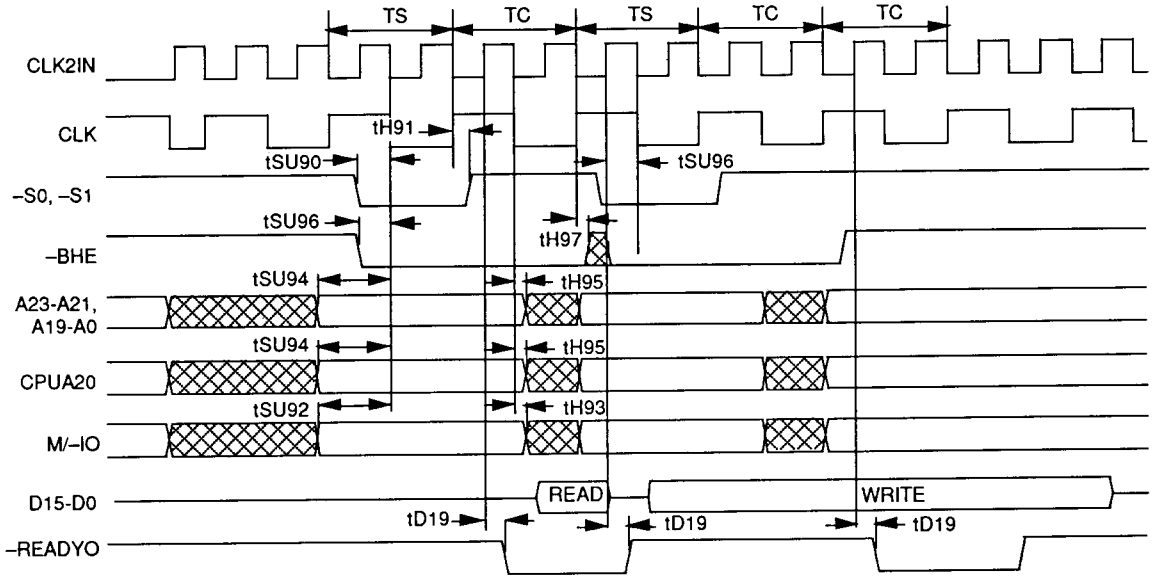


FIGURE 24. CPU INTERFACE TIMING - 386SX

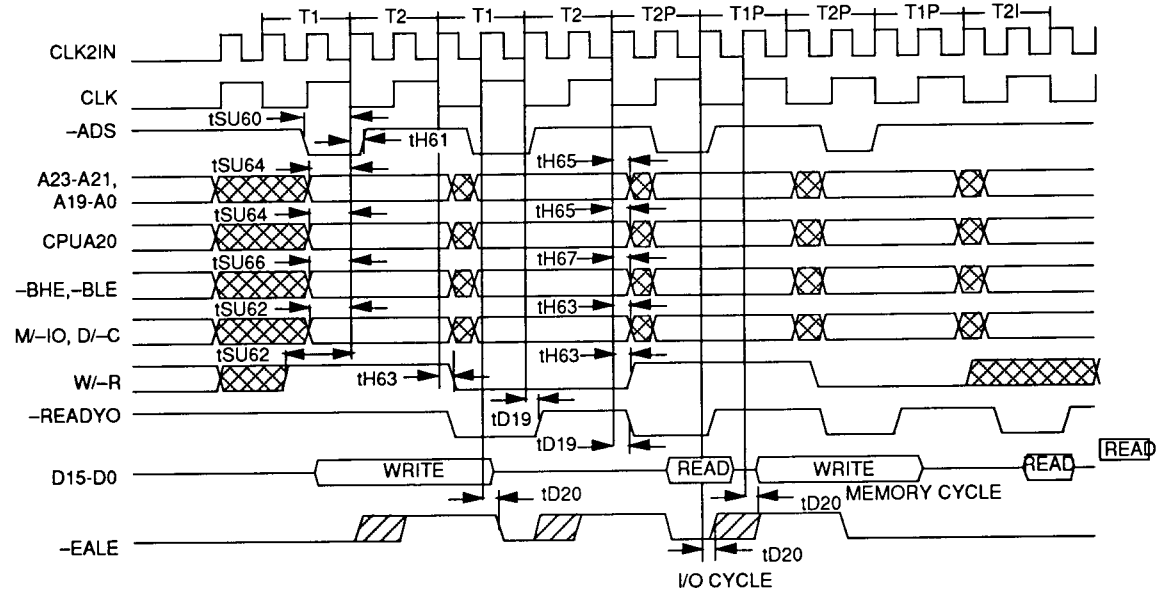


FIGURE 25. NUMERIC COPROCESSOR INTERFACE TIMING

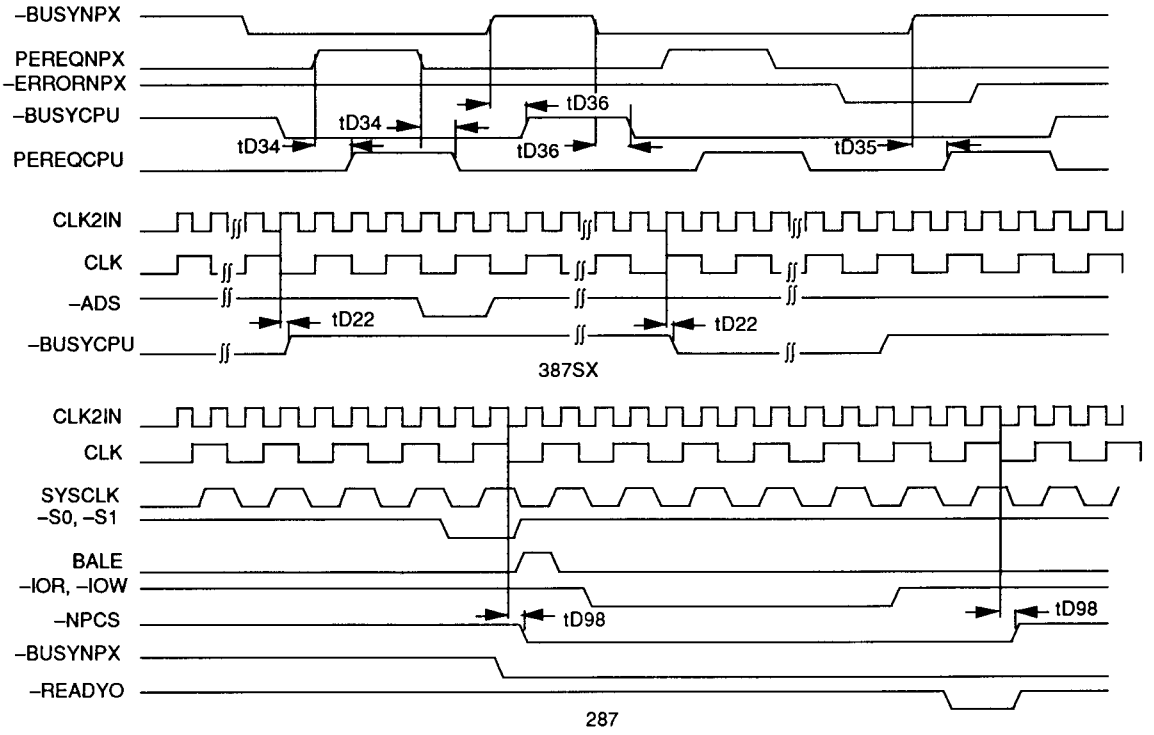


FIGURE 26. CPU MODE DRAM TIMING FOR 386SX

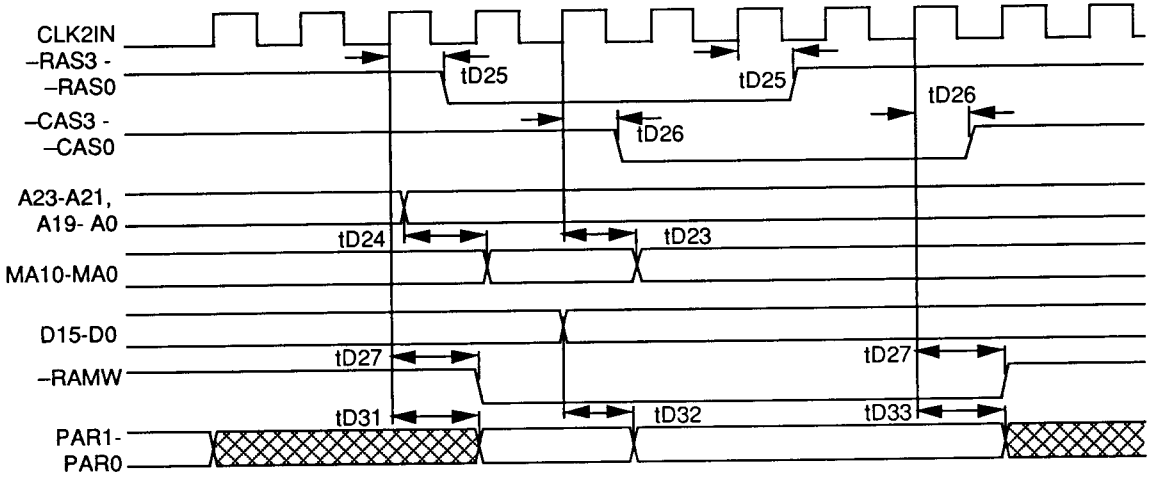
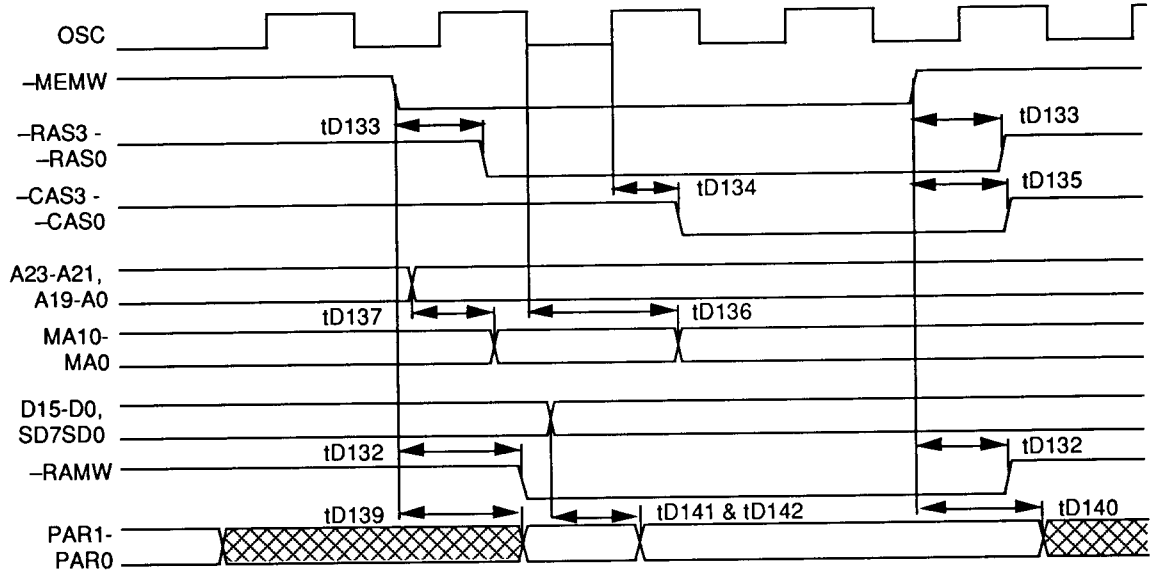
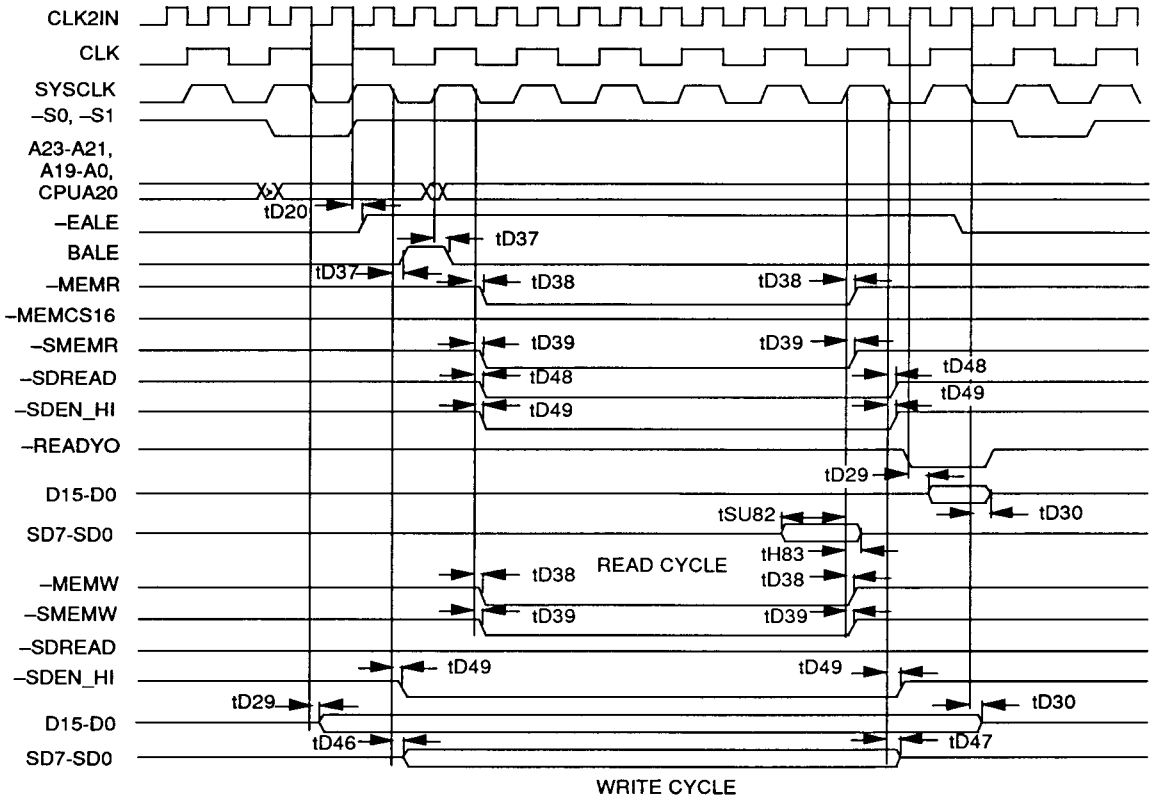


FIGURE 27. HLDA MODE DRAM TIMING



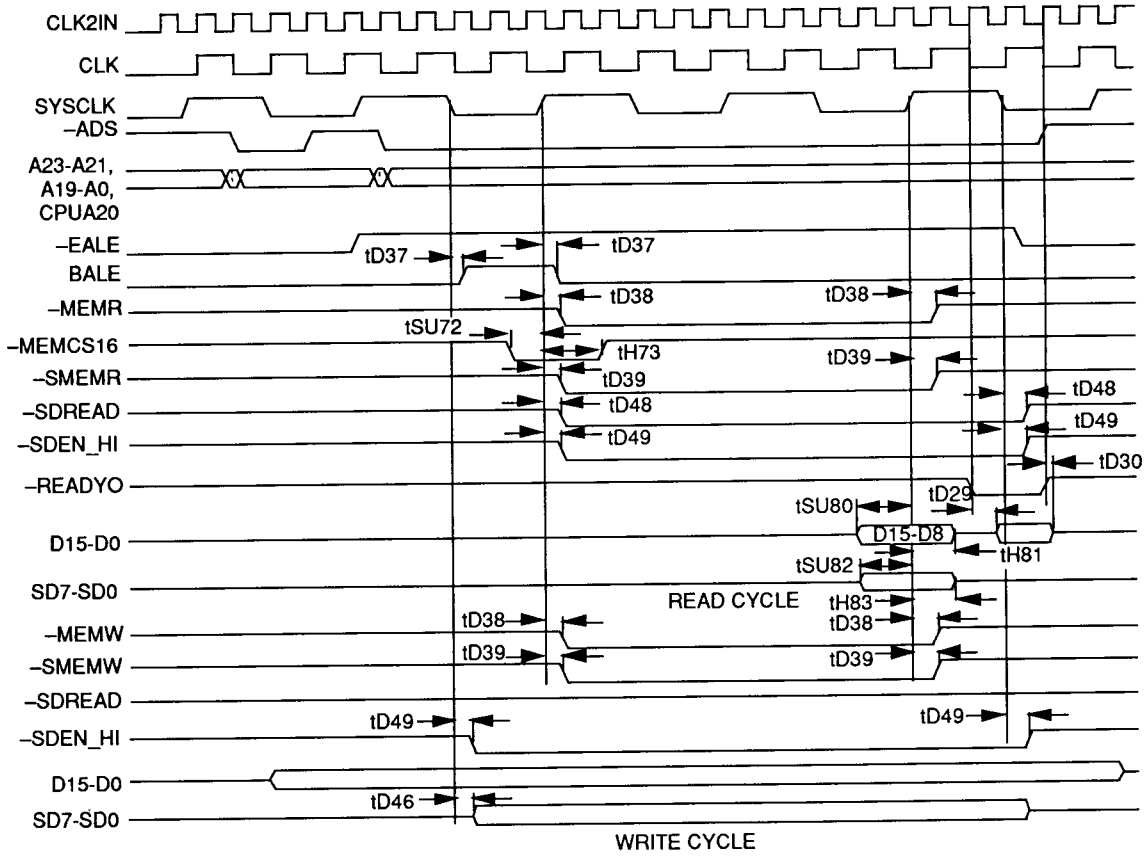
WRITE CYCLE

FIGURE 28. 286 OFFBOARD MEMORY CYCLE, 8-BIT



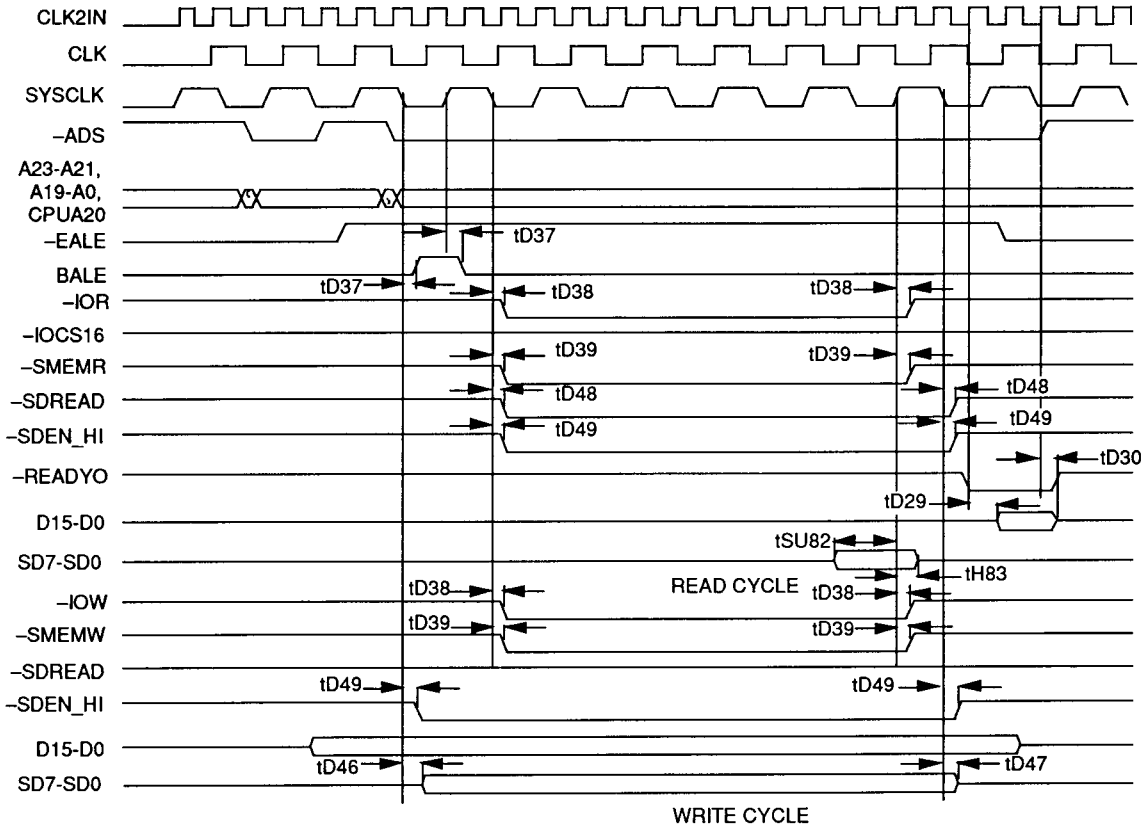
Note: –SMEMR and –SMEMW are three-state for addresses above 1M.

FIGURE 29. 386SX OFFBOARD MEMORY CYCLE, 16-BIT



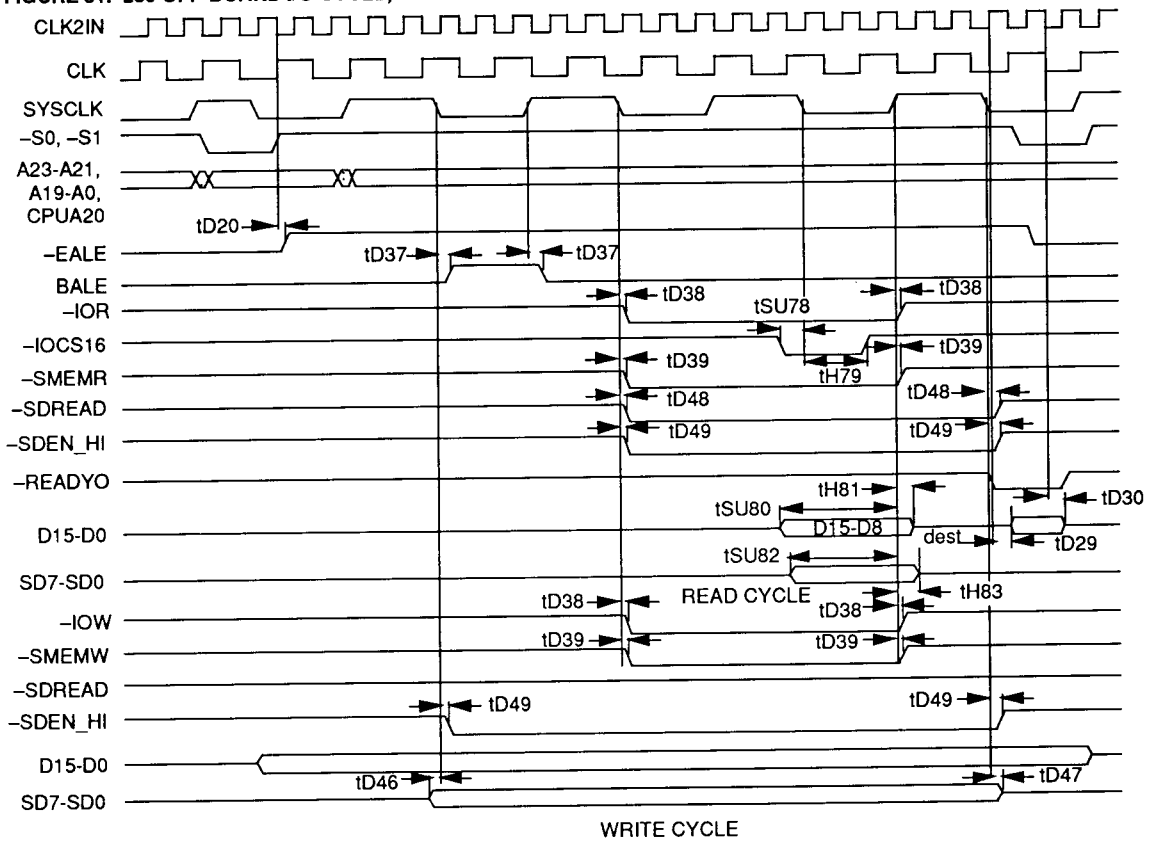
Note: -SMEMR and -SMEMW are three-state for addresses above 1M.

FIGURE 30. 386SX OFF-BOARD I/O CYCLE, 8-BIT



Note: -SMEMR and -SMEMW are three-state for addresses above 1M.

FIGURE 31. 286 OFF-BOARD I/O CYCLE, 16-BIT



Note: -SMEMR and -SMEMW are three-state for addresses above 1M.

FIGURE 32. ROM CYCLE

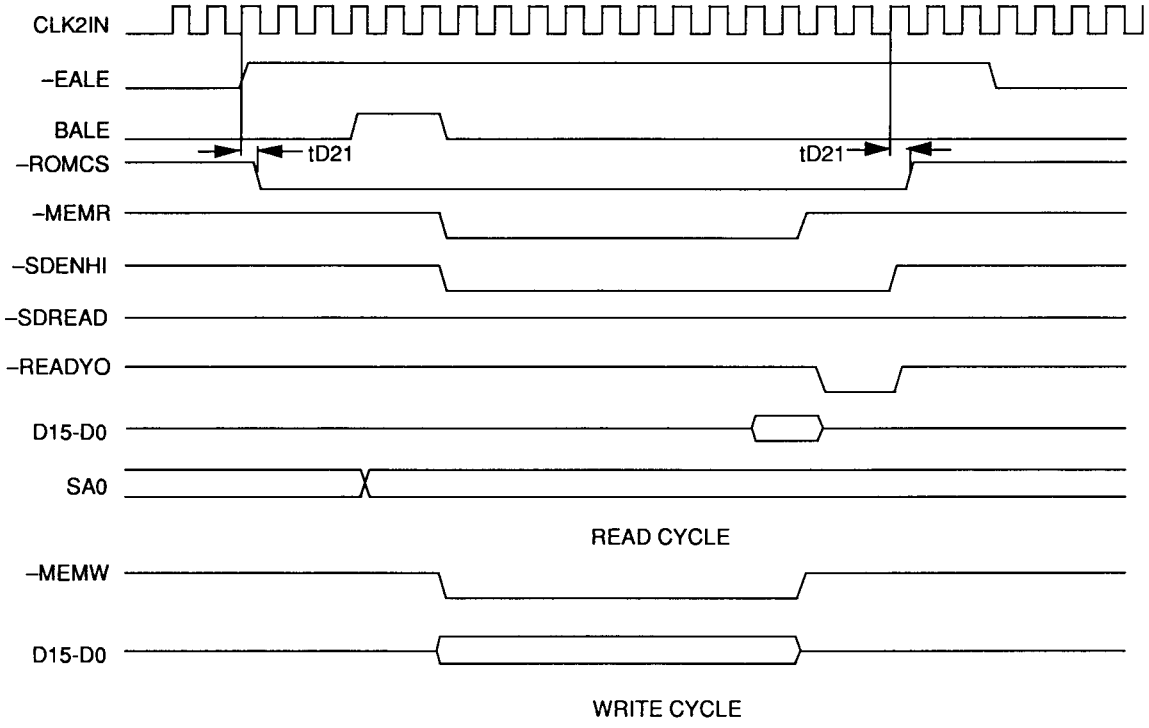


FIGURE 33. CPU MODE WS0 AND IOCHRDY TIMING

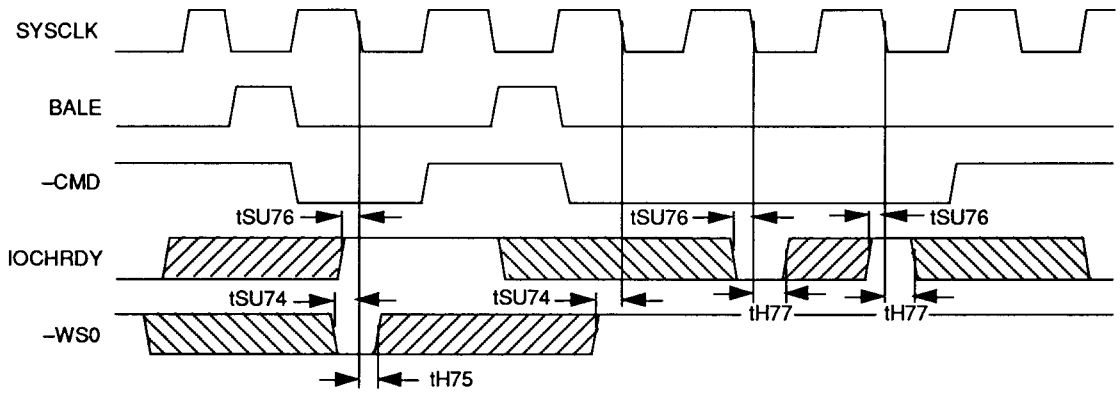


FIGURE 34. REFRESH TIMING

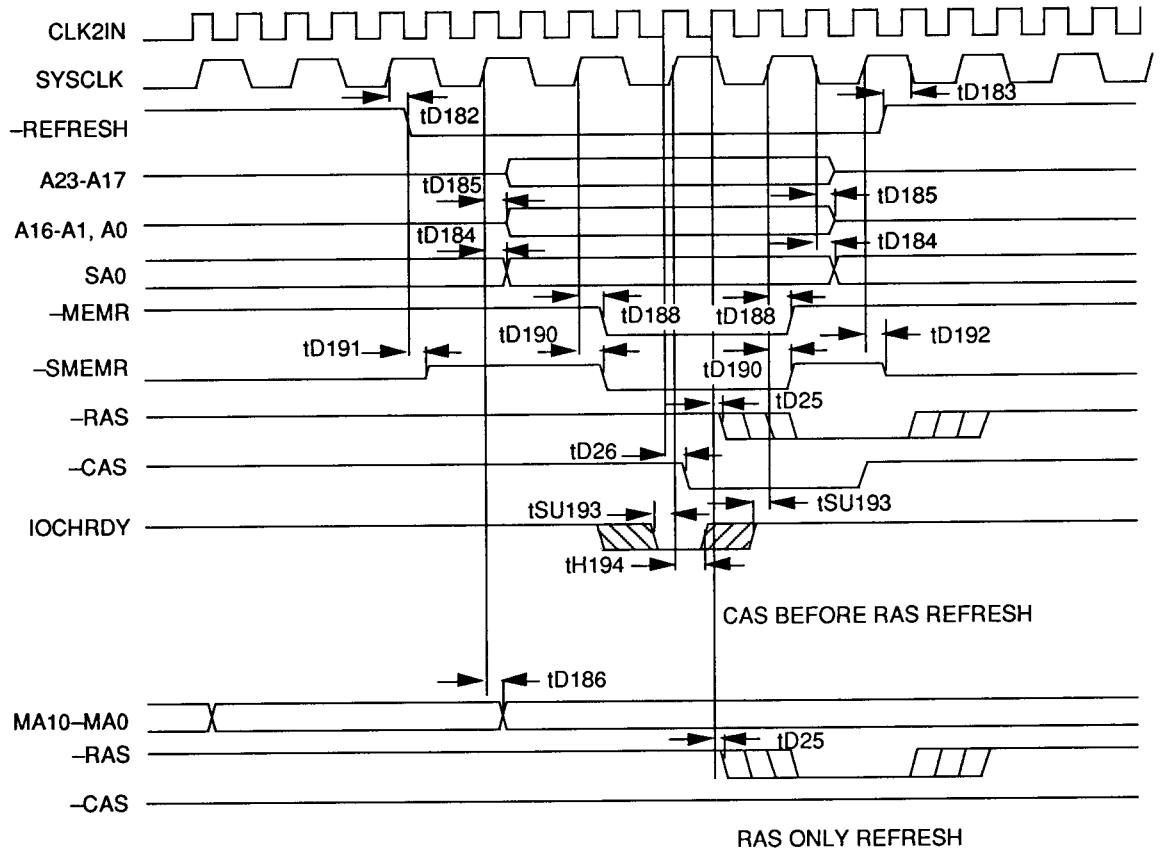
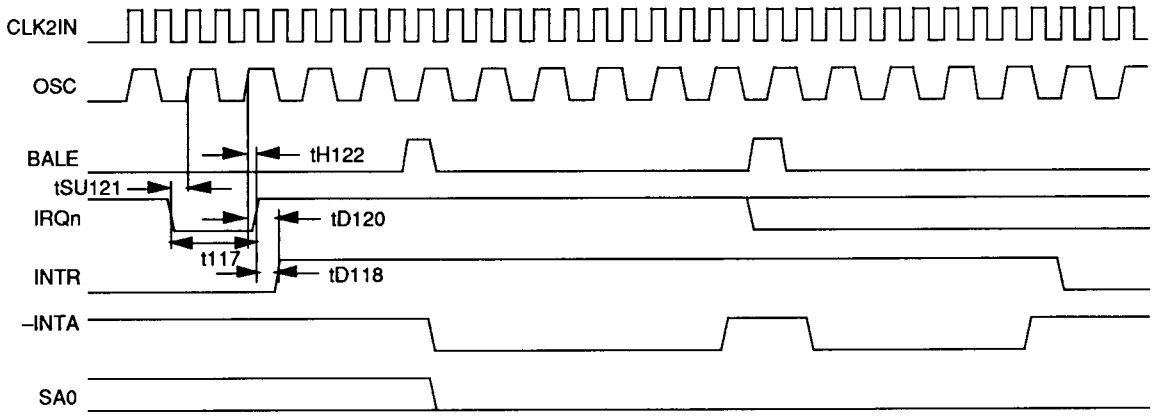


FIGURE 35. INTERRUPT ACKNOWLEDGE CYCLE



Note: –INTA is an internal signal.

FIGURE 36. MISCELLANEOUS TIMING

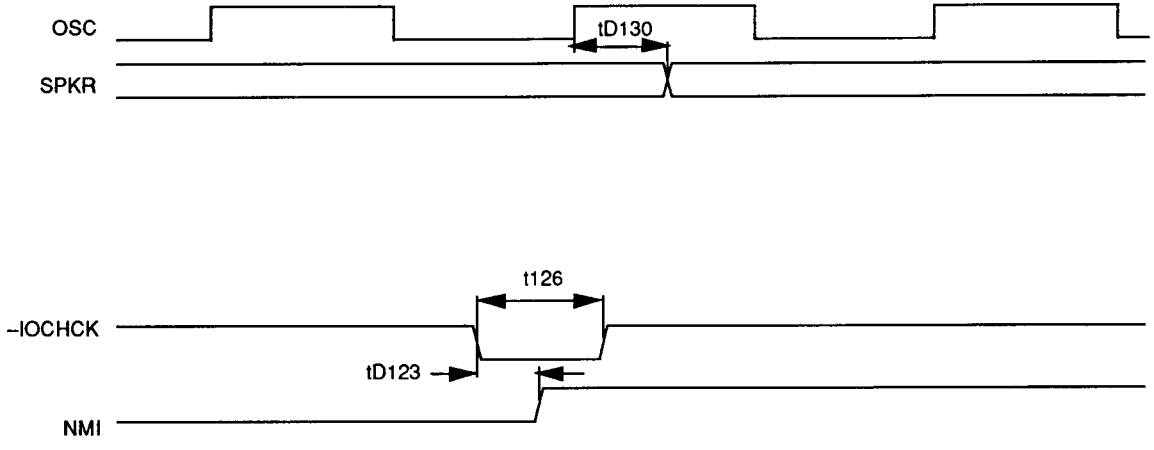


FIGURE 37. JEIDA MEMORY CARD TIMING

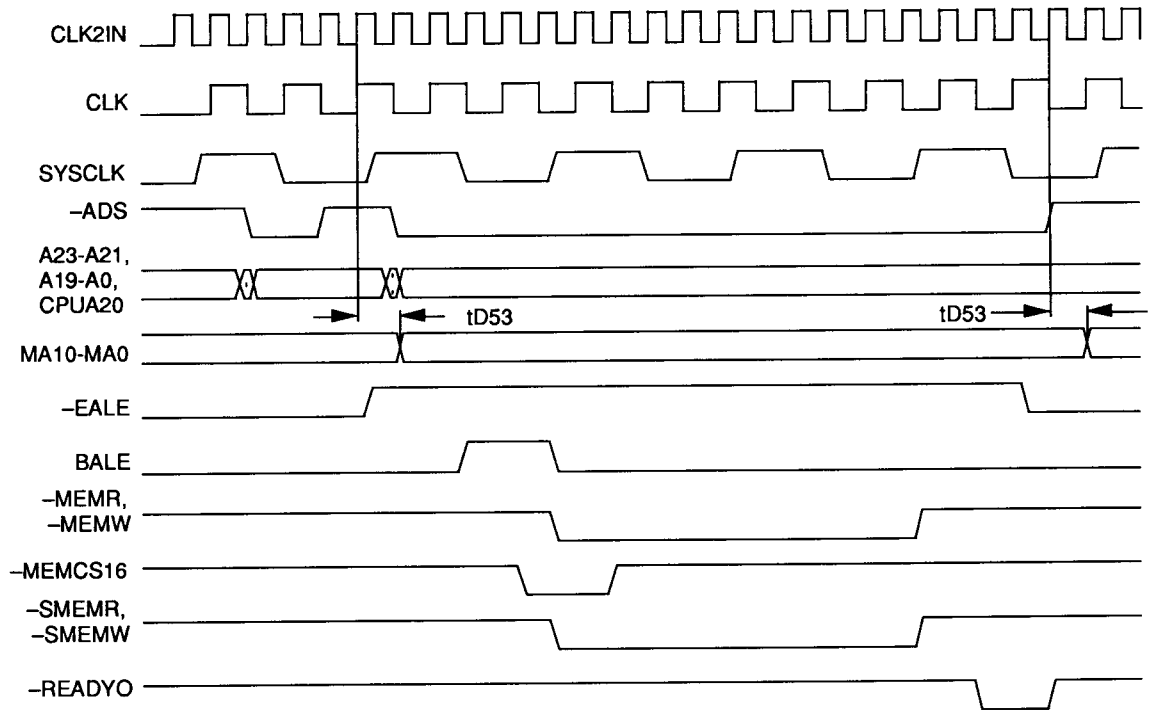


FIGURE 38. BUS ARBITRATION TIMING

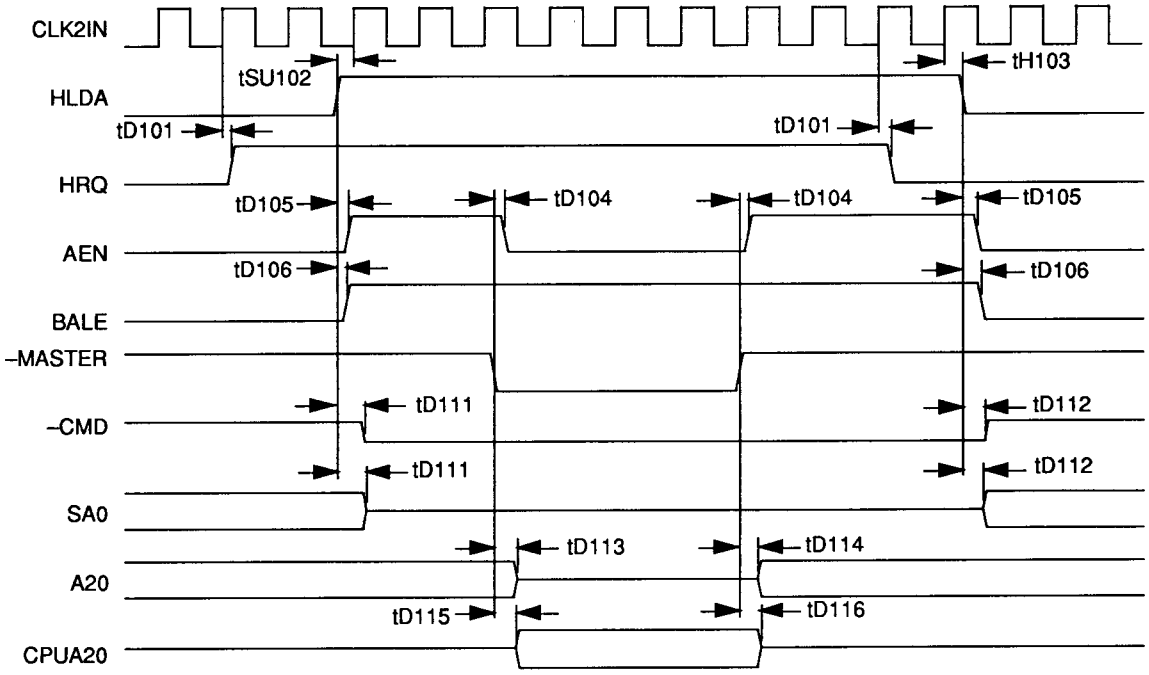
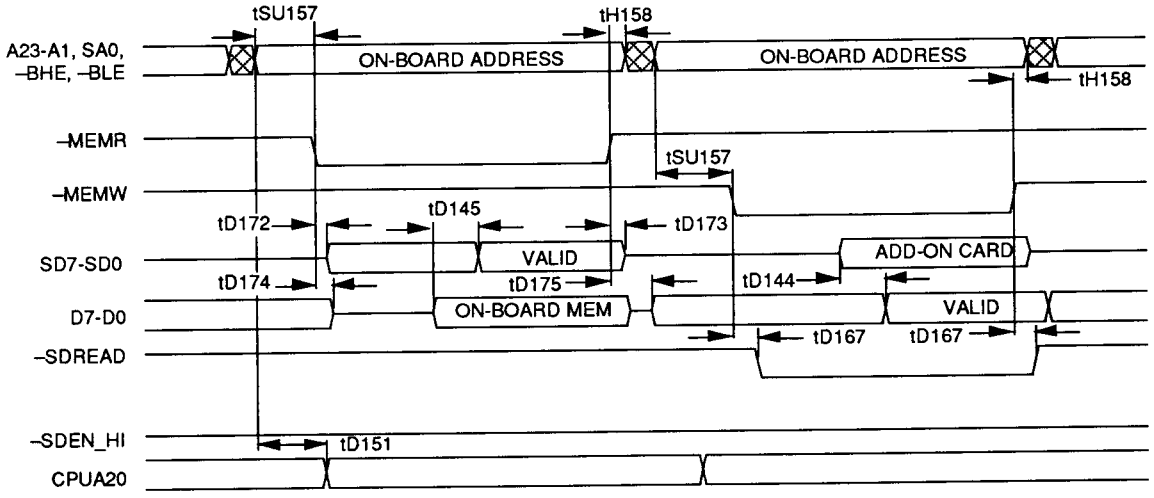
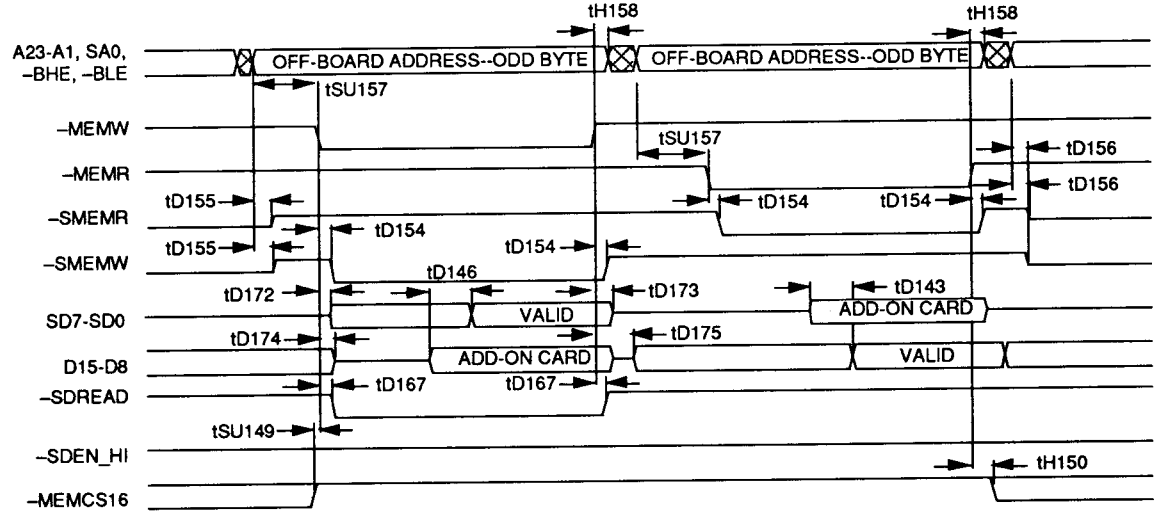


FIGURE 39. MASTER MODE CYCLE TIMING (ON-BOARD MEMORY ACCESSES)



Note: Also see Figure 27.

FIGURE 40. MASTER MODE CYCLE TIMING (OFF-BOARD MEMORY ACCESSES)



Note: -SMEMR and -SMEMW are three-state for addresses above 1 Meg. They should be pulled up externally with a 10k ohm resistor.

FIGURE 41. MASTER MODE CYCLE TIMING (I/O ACCESSES)

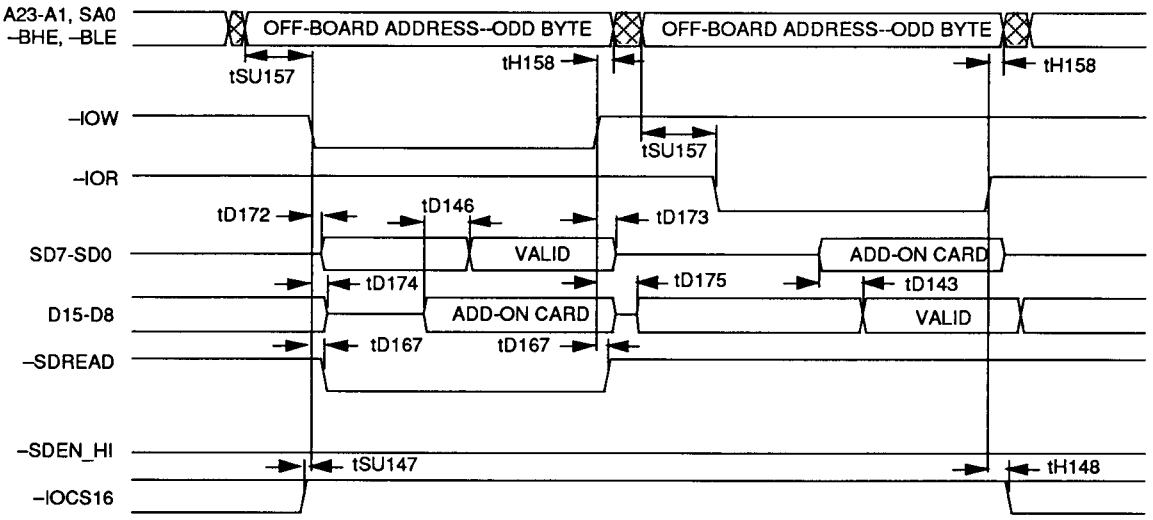


FIGURE 42. MASTER MODE CYCLE TIMING (INTERNAL REGISTER ACCESSES)

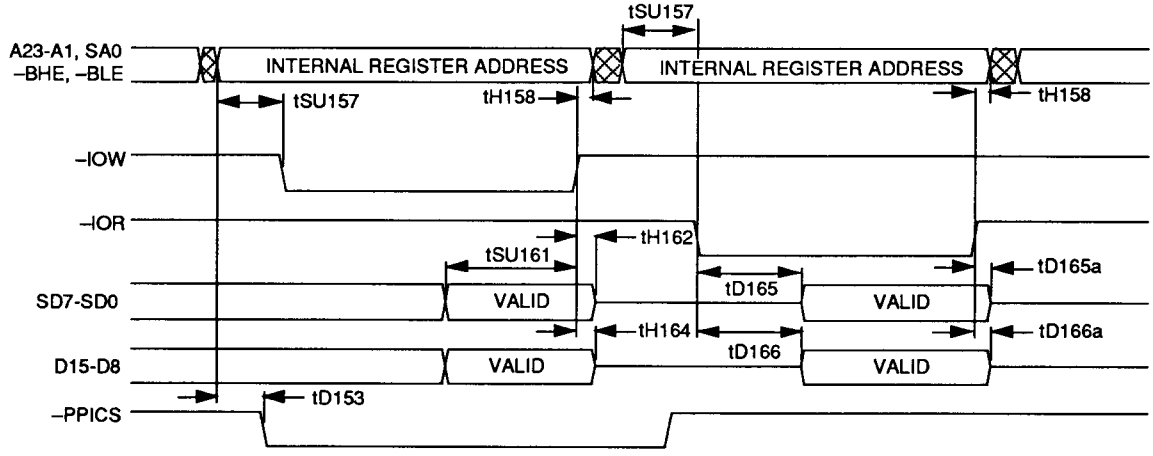


FIGURE 43. MASTER MODE REFRESH TIMING

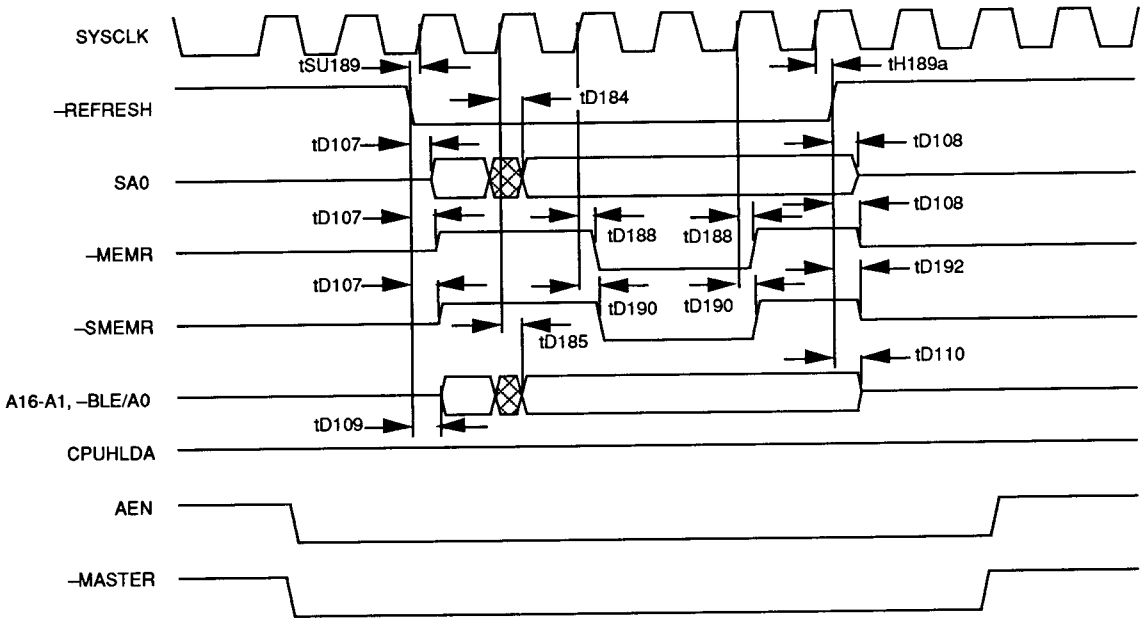
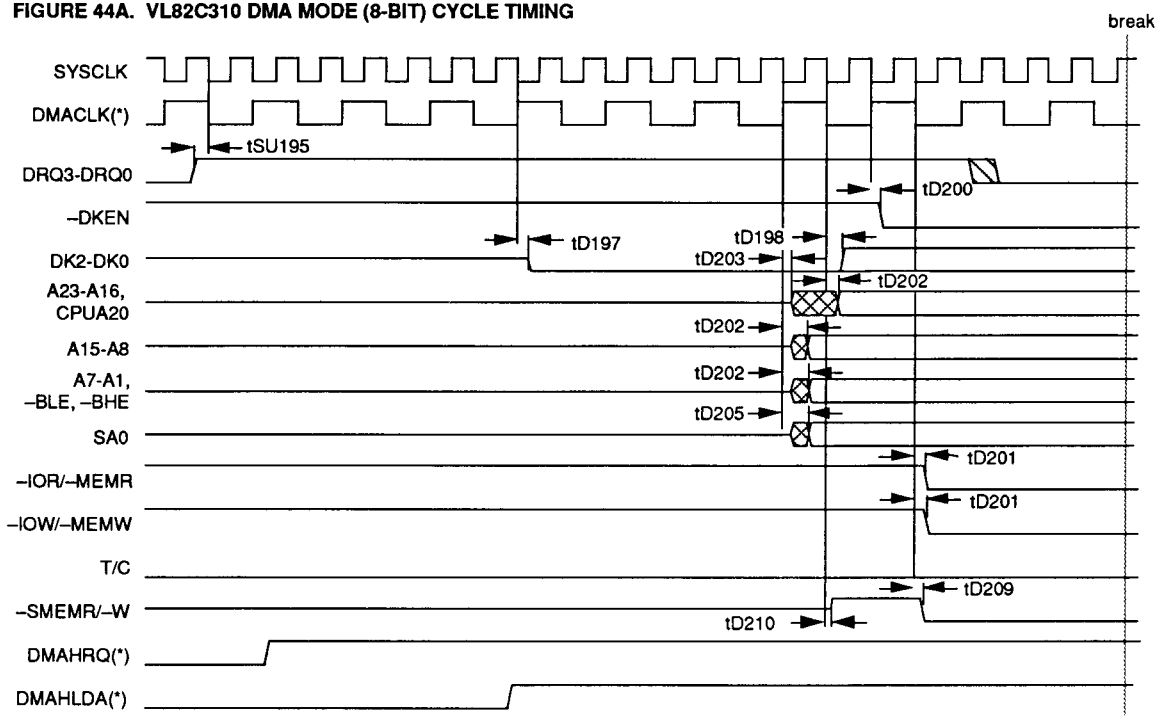


FIGURE 44A. VL82C310 DMA MODE (8-BIT) CYCLE TIMING

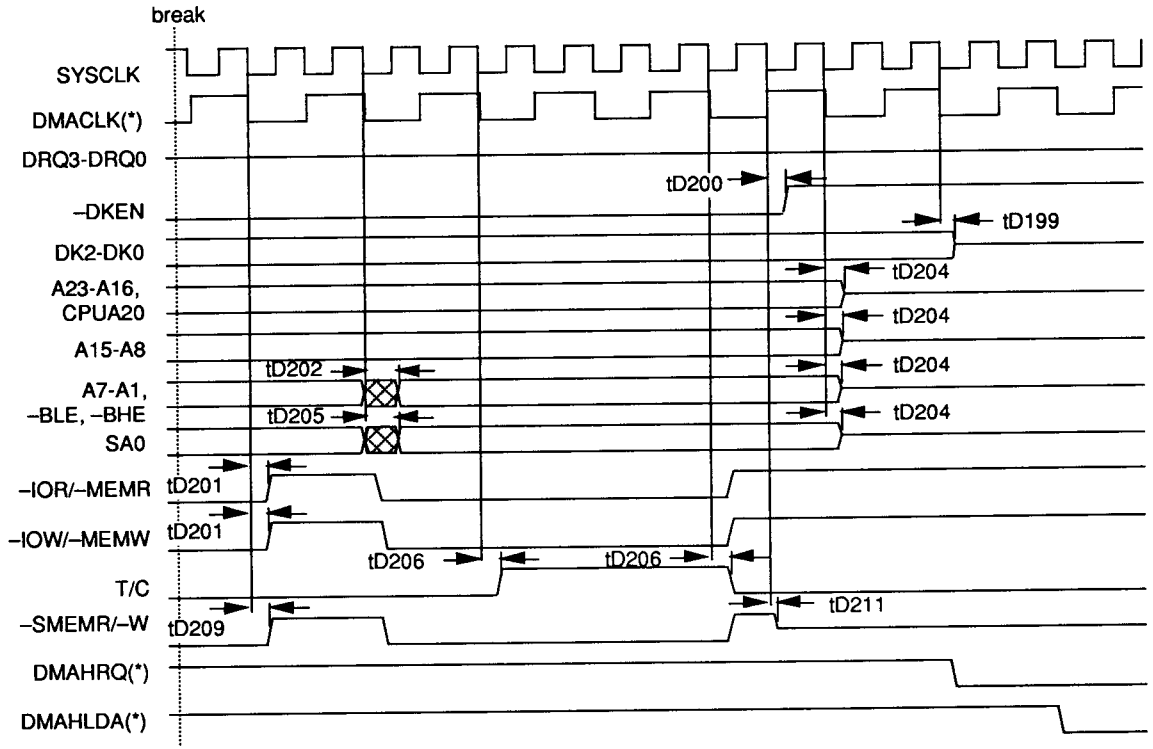


Notes: 1. -SMEMR and -SMEMW are three-state for addresses above 1 Meg. They should be pulled up externally with a 10k ohm resistor.

2. -MEMR timing shown with ROMDMA register bit 0 = 1. -IOW, -MEMW timing shown with DMA channels are programmed for extended write mode.

3. (*) internal signals.

FIGURE 44B. VL82C310 DMA MODE (8-BIT) CYCLE TIMING

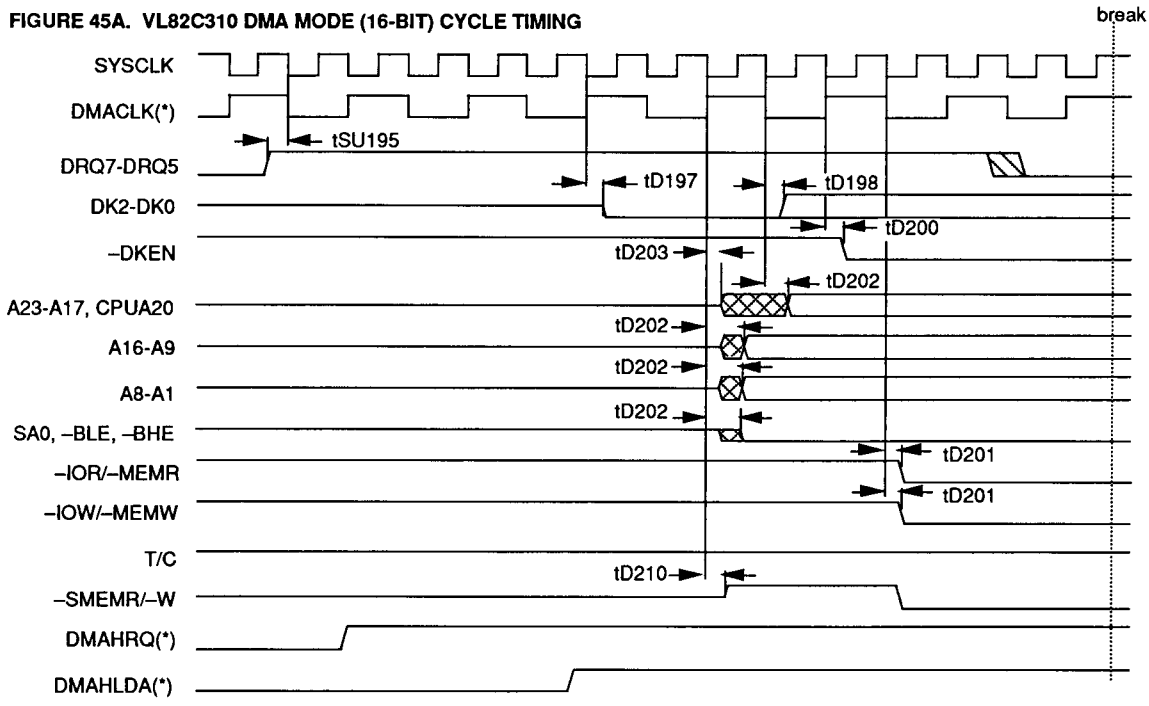


Notes: 1. -SMEMR and -SMEMW are three-state for addresses above 1 Meg. They should be pulled up externally with a 10k ohm resistor.

2. -MEMR timing shown with ROMDMA register bit 0 = 1. -IOW, -MEMW timing shown with DMA channels are programmed for extended write mode.

3. (*) internal signals.

FIGURE 45A. VL82C310 DMA MODE (16-BIT) CYCLE TIMING

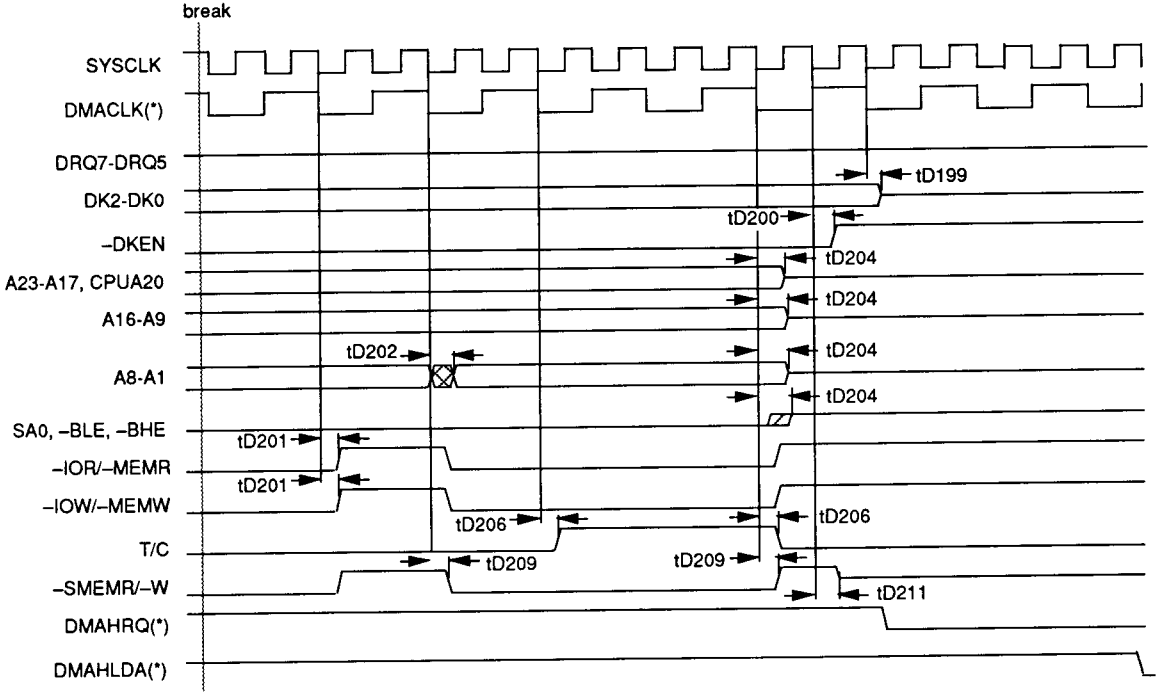


Notes: 1. -SMEMR and -SMEMW are three-state for addresses above 1 Meg. They should be pulled up externally with a 10k ohm resistor.

2. -MEMR timing shown with ROMDMA register bit 0 = 1. -IOW, -MEMW timing shown with DMA channels are programmed for extended write mode.

3. (*) internal signals.

FIGURE 45B. VL82C310 DMA MODE (16-BIT) CYCLE TIMING

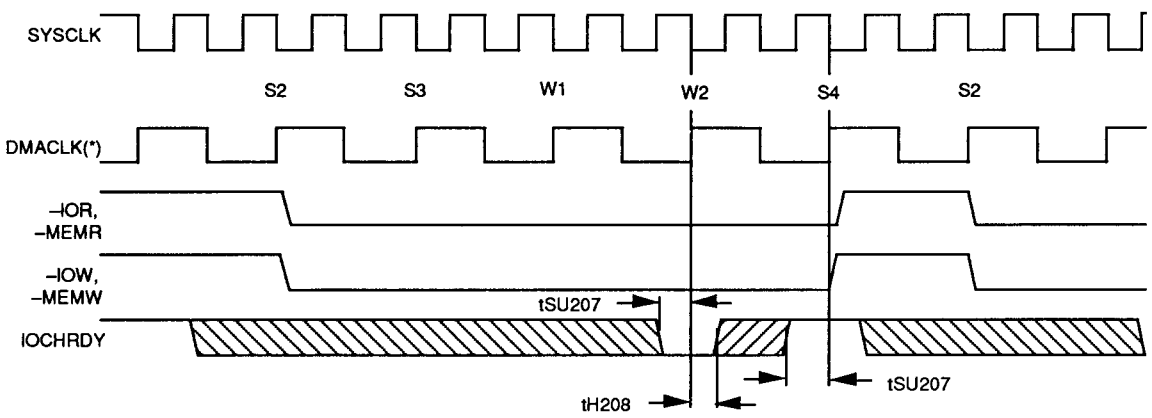


Notes: 1. -SMEMR and -SMEMW are three-state for addresses above 1 Meg. They should be pulled up externally with a 10k ohm resistor.

2. -MEMR timing shown with ROMDMA register bit 0 = 1. -IOW, -MEMW timing shown with DMA channels are programmed for extended write mode.

3. (*) internal signals.

FIGURE 46. IOCHRDY TIMING (DMA CYCLES)



Notes: 1. DMACLK is an internal signal.

2. The first wait state is automatically inserted by internal circuitry for all DMA cycles. Any additional wait states must be inserted using IOCHRDY.

FIGURE 47. DMA MODE DATA STEERING TIMING (ON-BOARD MEMORY ACCESSES)

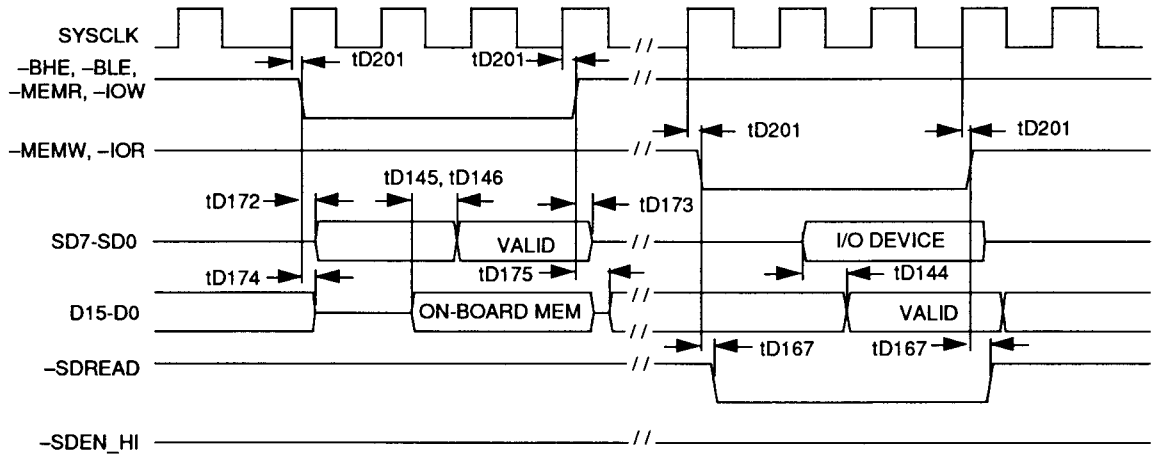
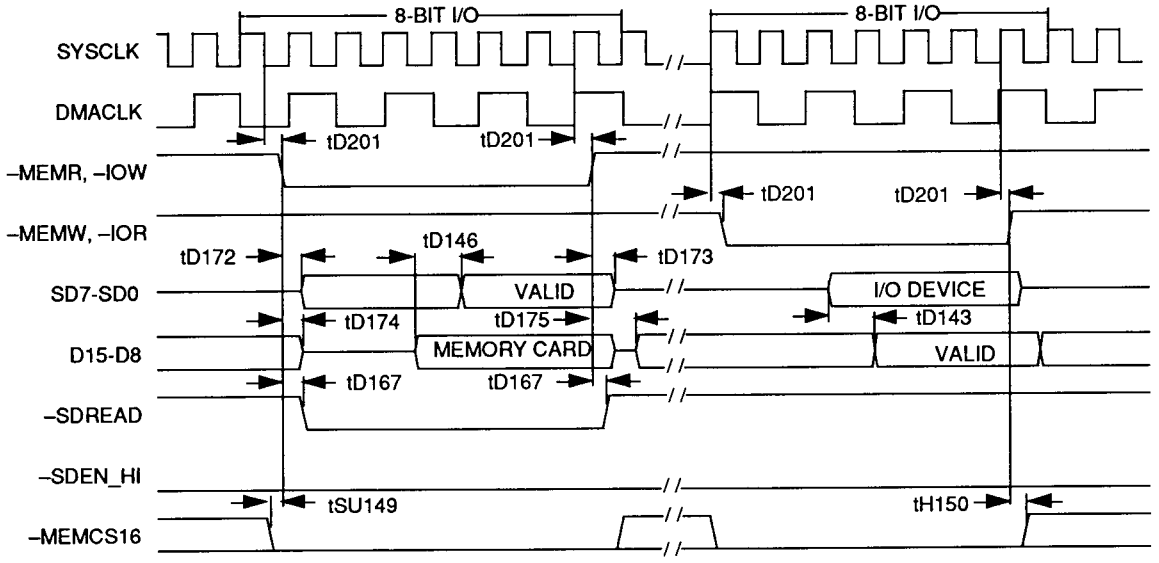


FIGURE 48. DMA MODE DATA STEERING TIMING (OFF-BOARD MEMORY ACCESSES)



Note: 8-bit DMA transfers shown.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature −10°C to +70°C

Storage Temperature −65°C to +150°C

Supply Voltage to Ground Potential −0.5 V to VDD + 0.3 V

Applied Output Voltage −0.5 V to VDD + 0.3 V

Applied Input Voltage −0.5 V to +7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device as indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameters	Min	Max	Unit	Conditions
VIL	Input Low Voltage	−0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs
VILC	Input Low Voltage	−0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD − 0.8	VDD + 0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD − 0.45		V	IOH = −1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 6 mA, Note 2
VOH2	Output High Voltage	VDD − 0.45		V	IOH = −2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, BUSCTL6 = 0 IOL = 24 mA, BUSCTL6 = 1, Note 3
VOH3	Output High Voltage	VDD − 0.45		V	IOH = −6 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 24 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 12 mA, RAMDRV = 0 IOL = 24 mA, RAMDRV = 1, Note 5
VOH4	Output High Voltage	2.4		V	IOH = −6 mA, Note 5
VOL6	Output Low Voltage		0.45	V	IOH = 24 mA, Note 6
VOH5	Output High Voltage	VDD − 0.45		V	IOH = −24 mA, Note 6

(Notes on next page.)

DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
ILI	Input Leakage Current	–10	10	µA	Note 7
IIL	Input Leakage Current	–500	10	µA	Note 8
IIH	Input Leakage Current	–10	500	µA	Note 9
IDDSB	Static Power Supply Current		500	µA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	No DC Loads
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

Notes: 1. Pins: HRQ, INTR, NMI, PEREQCPU, –BUSYCPU, –PPICS, –BLKA20, –ROMCS, –ADS/–NPCS.

2. Pins: T/C, –READYO, RESCPU, PAR1-PAR0, SPKR, RESNPX, –EALE, A23-A1, –BLE/A0, –BHE, CPUA20, D15-D0, –SDREAD, –SDEN_HI, –DKEN, W/–R,/–S0/DK2, D/–C/–S1/DK1, M/–IO/DK0.

3. Pins: SD7-SD0, SA0, –IOW, –IOR, –MEMW, –MEMR, RSTDRV, BALE, –SMEMW, –SMEMR, SYSCLK, AEN.

4. Pins: –REFRESH.

5. Pins: MA10-MA0, –RAS3 - –RAS0, –CAS3 - –CAS0, –RAMWR.

6. Pins: CLK2

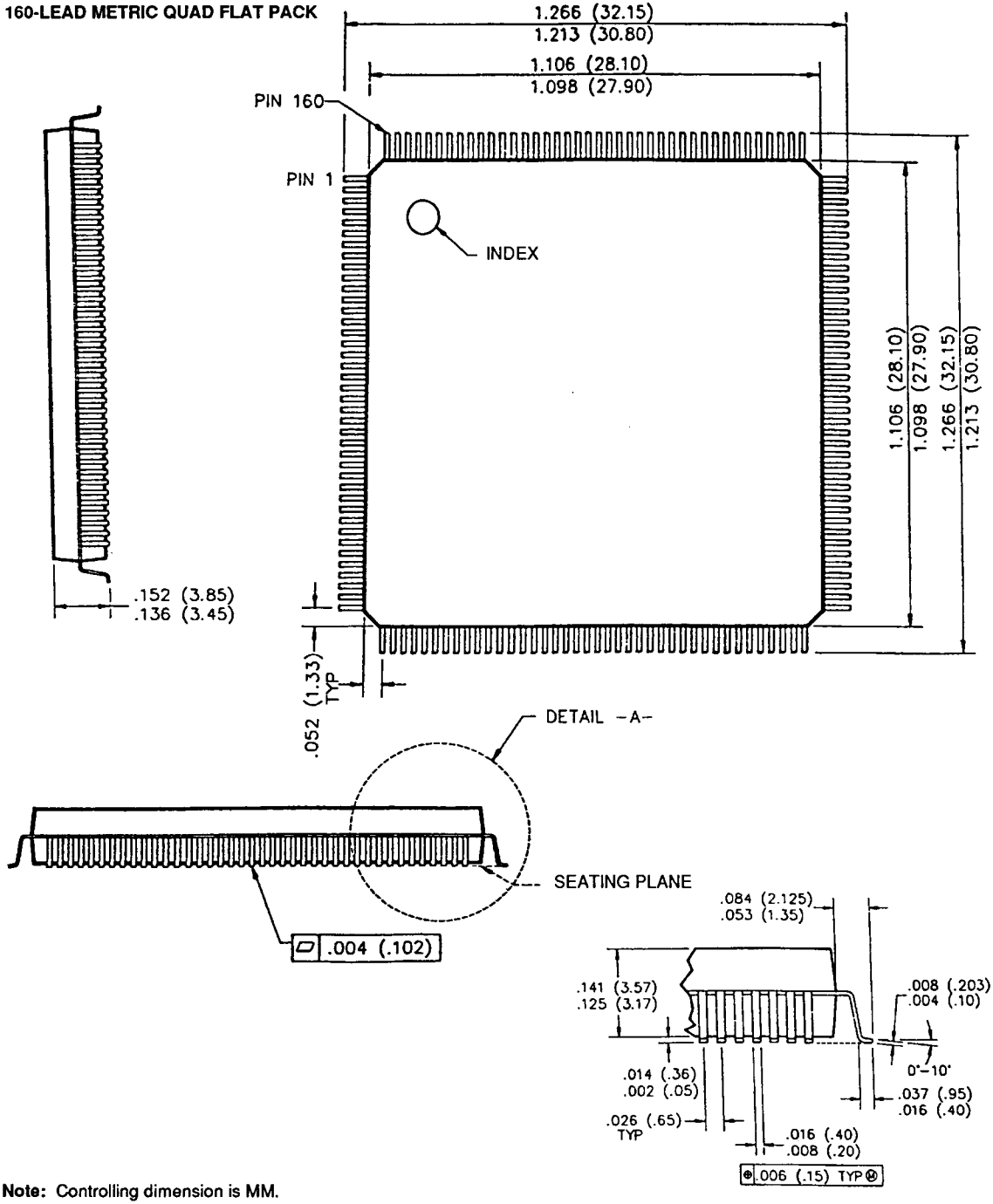
7. All inputs except those listed in Notes 8 and 9.

8. Pins: IRQ15, IRQ14, IRQ12-IRQ3, IRQ1, DRQ7-DR15, DRQ3-DR10, –BUSYNPX, –ERRORNPX, –BHE, –ADS/–NPCS, –BLE/A0, CPUA20, BUSOSC, POWERGOOD, SPKR, SELEEP/–MISS, W/–R/–S0/DK2, D/–C/–S1/DK1, M/–IO/DK0.

9. Pins: PEREQNPX.

PACKAGE OUTLINE

160-LEAD METRIC QUAD FLAT PACK



Note: Controlling dimension is MM.