VL82C114

COMBINATION I/O

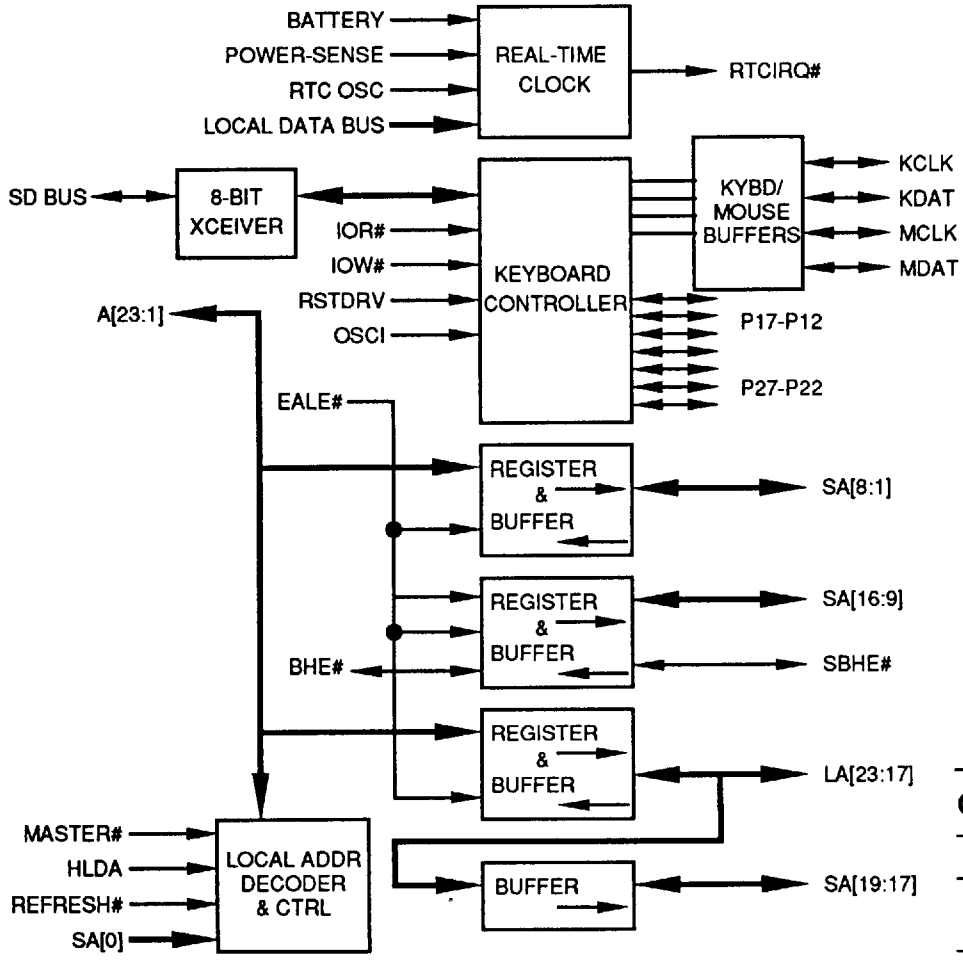
FEATURES

- Integrated peripheral controller that interfaces with several of VLSI's Single Chip System/ISA Bus Controllers:
  - VL82C480
  - VL82C481
  - VL82C486
  - VL82C310
  - VL82C311
  - VL82C311L
- Backwards compatible with the industry standard VL82C113A Combination I/O chip
- 146818A-compatible real-time clock
- 114 additional bytes of battery-backed CMOS RAM
- AT®-compatible keyboard controller with integrated PS/2® mouse support
- Processor to ISA bus address latches and buffers, which support 16- and 32-bit processors
- Supports processors with write-back cache controllers
- Real-time clock can be relocated via SA[15:0] address registers
- Includes ISA bus refresh counters for decoupled refresh
- 1.0-micron CMOS
- 100-lead MQFP (Metric Quad Flat Pack)

OVERVIEW

The VL82C114 Combination I/O chip, when used with VLSI's System Controller chips, allows designers to implement a very cost-effective minimum chip count motherboard. This chip combines a keyboard controller and a real-time clock with the address registers/latches and buffers which are normally required in ISA bus compatible systems. The VL82C114 features an AT-compatible keyboard controller with integrated PS/2 mouse support and a 146818A-compatible real-time clock. The VL82C114 also has114 additional bytes of battery-backed CMOS RAM for use in extended system setup. In addition, the VL82C114 provides support for processors with write-back cache controllers.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C114-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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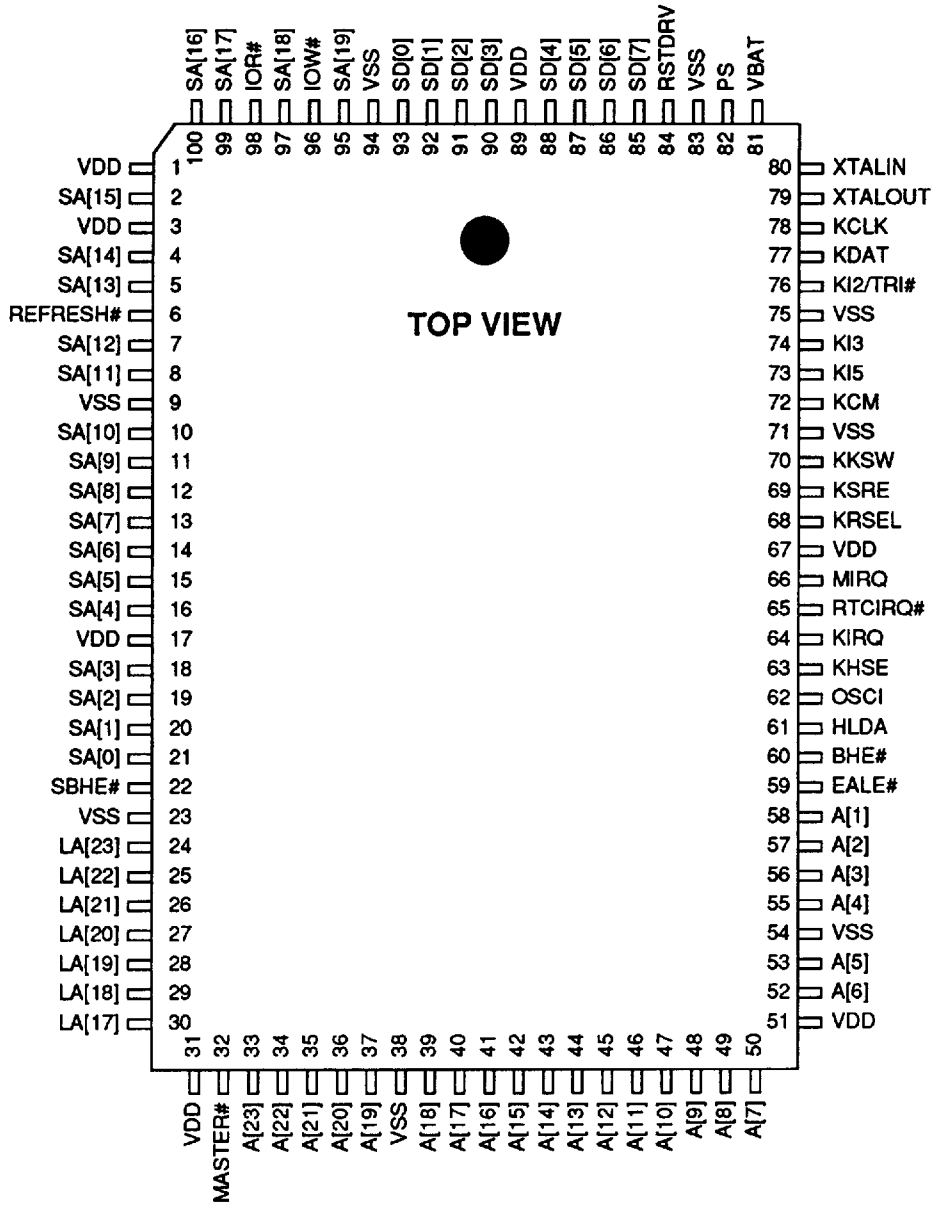
PIN DIAGRAM



PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
1	VDD	PWR			36	A[20]	IO	TTL	8
2	SA[15]	IO	TTL	24	37	A[19]	IO	TTL	8
3	VDD	PWR			38	VSS	GND		
4	SA[14]	IO	TTL	24	39	A[18]	IO	TTL	8
5	SA[13]	IO	TTL	24	40	A[17]	IO	TTL	8
6	REFRESH#	I	TTL		41	A[16]	IO	TTL	8
7	SA[12]	IO	TTL	24	42	A[15]	IO	TTL	8
8	SA[11]	IO	TTL	24	43	A[14]	IO	TTL	8
9	VSS	GND			44	A[13]	IO	TTL	8
10	SA[10]	IO	TTL	24	45	A[12]	IO	TTL	8
11	SA[9]	IO	TTL	24	46	A[11]	IO	TTL	8
12	SA[8]	IO	TTL	24	47	A[10]	IO	TTL	8
13	SA[7]	IO	TTL	24	48	A[9]	IO	TTL	8
14	SA[6]	IO	TTL	24	49	A[8]	IO	TTL	8
15	SA[5]	IO	TTL	24	50	A[7]	IO	TTL	8
16	SA[4]	IO		24	51	VDD	PWR		
17	VDD	PWR			52	A[6]	IO	TTL	8
18	SA[3]	IO	TTL	24	53	A[5]	IO	TTL	8
19	SA[2]	IO	TTL	24	54	VSS	GND		
20	SA[1]	IO	TTL	24	55	A[4]	IO	TTL	8
21	SA[0]	IO	TTL	24	56	A[3]	IO	TTL	8
22	SBHE#	IO	TTL	24	57	A[2]	IO	TTL	8
23	VSS	GND			58	A[1]	IO	TTL	8
24	LA[23]	IO	TTL	24	59	EALE#	I	TTL	
25	LA[22]	IO	TTL	24	60	BHE#	IO	TTL	8
26	LA[21]	IO	TTL	24	61	HLDA	I	TTL	
27	LA[20]	IO	TTL	24	62	OSCI	I	TTL-S	
28	LA[19]	IO	TTL	24	63	KHSE	IO-OD	TTL-S	12
29	LA[18]	IO	TTL	24	64	KIRQ	IO[3]	TTL	4
30	LA[17]	IO	TTL	24	65	RTCIRQ#	IO-OD[2]	TTL	12
31	VDD	PWR			66	MIRQ	O		4
32	MASTER#	I	TTL		67	VDD	PWR		
33	A[23]	IO	TTL	8	68	KRSEL	I	TTL	
34	A[22]	IO	TTL	8	69	KSRE	IO-OD	TTL-S	12
35	A[21]	IO	TTL	8	70	KKSW	I[3]	TTL	

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
71	VSS	GND			86	SD[6]	IO	TTL	24
72	KCM	I(3)	TTL		87	SD[5]	IO	TTL	24
73	KI5	IO(3)	TTL	4	88	SD[4]	IO	TTL	24
74	KI3	IO(3)	TTL	4	89	VDD	PWR		
75	VSS	GND			90	SD[3]	IO	TTL	24
76	KI2/TRI#	I(3)	TTL		91	SD[2]	IO	TTL	24
77	KDAT	IO(1)	TTL	12	92	SD[1]	IO	TTL	24
78	KCLK	IO(1)	TTL	12	93	SD[0]	IO	TTL	24
79	XTALOUT	O			94	VSS	GND		
80	XTALIN	I	CMOS	8	95	SA[19]	IO	TTL	24
81	VBAT	I	TTL		96	IOW#	I	TTL	
82	PS	I	TTL-S		97	SA[18]	IO	TTL	24
83	VSS	GND			98	IOR#	I	TTL	
84	RSTDRV	I	TTL		99	SA[17]	IO	TTL	24
85	SD[7]	IO	TTL	24	100	SA[16]	IO	TTL	24

Notes:

(1) During PS/2 Mode, these IO pins are TTL level with an open drain output/Schmitt-trigger input.

(2) Indicates a high-impedance with approximately 10 KΩ minimum resistance to VSS (internal pull-down resistor on pin).

(3) Indicates a high-impedance with approximately 10 KΩ minimum resistance to VDD (internal 30K ohm pull-up resistor on pin).

Legend:

CMOS	CMOS-compatible input
I	Input pin
IO	Bidirectional pin
GND	Ground pin
O	Output pin
OD	Open drain
PWR	Power supply pin
S	Indicates a Schmitt-trigger input with hysteresis for noise immunity.
TTL	TTL-compatible input

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
HLDA	61	I-TTL	Hold Acknowledge - This is the hold acknowledge signal directly from the CPU. It is used to control direction on address bus (A bus) and to enable the DACK# decoder signals.
A[23:1]	33:37, 39:50, 52, 53, 55:58	IO-TTL	Address bus bits 23 through 1 - The address bus signals are outputs when HLDA is high, MASTER# is low, and REFRESH# is high. They are inputs at all other times.
BHE#	60	IO-TTL	Byte High Enable - During Master Mode non-refresh cycles, this pin is an output and it tracks the SBHE# input. It is an input at all other times.
ISA BUS INTERFACE SIGNALS			
RSTDRV	84	I-TTL	System Reset - This active high input is a system reset generated from the POWERGOOD input.
IOR#	98	I-TTL	I/O Read Command
IOW#	96	I-TTL	I/O Write Command
MASTER#	32	I-TTL	Master - An active low input that is used by an external device to disable the DMA controllers and obtain access to the system bus. When asserted, it indicates that an external Bus Master has control of the bus.
REFRESH#	6	I-TTL	Refresh - This active low input signal is pulled low whenever a refresh cycle is initiated.
LA[23:17]	24:30	IO-TTL	Latchable Address bus bits 23 through 17 - The LA bus signals are inputs when HLDA is high, REFRESH# is high, and MASTER# is low. They are output signals driven by values from the A bus when HLDA is low and REFRESH# is high. If HLDA is high and REFRESH# is low, they are three-stated. In Non-486 Mode, the LA bus is latched internally with the EALE# input. In 486 Mode, the LA bus is not latched (flow-through) during CPU initiated cycles and is latched when IOR# or IOW# is active during DMA cycles.
SA[19-9]	95, 97, 99, 100, 2, 4, 5, 7, 8, 10, 11	IO-TTL	System Address bus bits 19 through 9 - The SA[19:9] bus signals are inputs when HLDA is high, REFRESH# is high, and MASTER# is low. They are output signals and driven by values from the A bus when HLDA is low and REFRESH# is high. SA[16:9] are three-stated when REFRESH# is low. SA[19:17] are driven low when REFRESH# is driven low. In Non-486 Mode, SA[19:9] are registered internally with the EALE# input. In 486 Mode, S[19:9] are not latched (flow-through) during CPU initiated cycles and are latched with IOR# or IOW# active during DMA cycles.
SA[8:1]	12:16, 18:20	IO-TTL	System Address bus bits 8 through 1 - The SA[8:1] bus signals are inputs when HLDA is high, REFRESH# is high, and MASTER# is low. They are outputs driven by values from the A bus at all other times. In Non-486 Mode, SA[8:1] are registered internally with the EALE# input. In 486 Mode, SA[8:1] are not latched (flow-through) during CPU initiated cycles and are latched with IOR# or IOW# active during DMA cycles. If the EALE# pin is grounded, 486 Mode, SA[1] is always an input and is used only in the address decode of internal peripheral registers/ports.
SA[0]	21	I-TTL	System Address bus bit 0 (least significant bit, LSB) - This signal is an input at all times and is used in the address decode of internal peripheral registers/ports.
SBHE#	22	IO-TTL	System Byte High Enable - This pin is controlled the same way as the SA bus. SBHE# is latched internally with the EALE# input in Non-486 Mode.
OSCI	62	I-TTL-S	Oscillator Input - The input for the 14.318 MHz oscillator.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description			
KEYBOARD CONTROLLER SIGNALS						
				Keyboard Controller Mode		
				PC/AT Mode KBDCTRL1 = 1		**PS/2 Mode KBDCTRL1 = 0**
KCLK	78	IO-TTL(1)	T0/-P26	Kbd Clock	T0/-P26	Kbd Clock
KDAT	77	IO-TTL(1)	T1/P27	Kbd Data	P10/-P27	Kbd Data
KCM	72	I-TTL(3)	P16	Color Input	P16	Input
KKSW	70	I-TTL(3)	P17	Key Switch	P17	Input
KHSE	63	IO-OD-TTL-S	P22	High Speed	P11/-P22	Mouse Data
KSRE	69	IO-OD-TTL-S	P23	Shadow RAM	T1/-P23	Mouse Clock
KIRQ	64	IO-TLL(3)	P24	Kbd Int Req	P24	Kbd Int Req
			This pin is sampled on the high-to-low transition of RSTDRV. If KIRQ is low, the keyboard function within the VL82C114 is disabled. If KIRQ is high, the keyboard is enabled. This pin is internally pulled up to VDD.			
MIRQ	66	O	P25	General Purpose Output	P25	Mouse Int Req
KRSEL	68	I-TTL	P14	RAM Slct	P14	Input
KI2/TRI#	76	I-TTL(3)	P12	Input	P12	Fuse Input
			This pin is sampled on the high-to-low transition of RSTDRV. If KI2/TRI# is low, all outputs will be three-stated. If KI2/TRI# is high, the chip will function normally. This pin is internally pulled up to VDD.			
KI3	74	IO-TTL(3)	P13 MISC0	Input Output	P13 MISC0	Input Output
KI5	73	IO-TTL(3)	P15 MISC1	Input Output	P15 MISC1	Input Output
SD DATA BUS SIGNALS						
SD[7:0]	85:88, 90:93	IO-TTL	System Data bus bits 7 through 0 - This bus connects directly to the slots. It is used to transfer data to/from the low byte of local and system devices.			
PERIPHERAL INTERFACE SIGNALS						
XTALIN	80	I-CMOS	The internal oscillator input for real-time clock crystal. It requires a 32.768 KHz external crystal or stand-alone oscillator.			
XTALOUT	79	O	The internal oscillator input for real-time clock crystal. See XTALIN. This pin is a "no connect" when an external oscillator is used.			
PS	82	I-TTL-S	Power-Sense - An active high input used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and the contents of the real-time clock may not be valid. This pin is connected to an external RC network.			
VBAT	81	I-TTL	Connected to the real-time clock's hold up battery between 2.4 and 5 volts.			
RTCIRQ#	65	IO-OD-TTL(2)	Real-Time Clock Interrupt Request output (active low) - This pin is an input when RSTDRV is high. It is sampled on the high-to-low transition of RSTDRV. If RTCIRQ# is low, the real-time clock's function within the VL82C114 is disabled. If RTCIRQ# is high, the real-time clock is enabled. Open drain output.			

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
ADDRESS BUS CONTROL SIGNAL			
EALE#	59	I-TTL	Early Address Latch Enable - An active low pulse that is generated at the beginning of any bus cycle initiated from the CPU which is not directed at the on-board DRAM. EALE# is used to select the 486 Mode. To select the 486 Mode, EALE# should be tied low. During the 486 Mode, SA[1] is an input only and the path from the CPU's A Bus to the SA and LA pins is flow through (no address latching) during CPU cycles.
POWER AND GROUND PINS			
VDD	1, 3, 17, 31, 51, 67, 89	PWR	Power Connection, nominally +5 volts.
VSS	9, 23, 38, 54, 71, 75, 83, 94	GND	Ground Connection, 0 volts.

Note: Refer to the Notes and Legend on page 4 for details on the Signal Type.

AC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Fig	Conditions
I/O READ/WRITE TIMING						
t5	Command Pulse Width	125		ns	1	
tSU6	Write Data Setup	60		ns	1	
tH7	Write Data Hold	20		ns	1	
tD8	Read Data Delay	0	130	ns	3	CL = 200 pF
tH9	Read Data Hold	13	60	ns	3	CL = 50
WC	Write Cycle	280		ns	1	
RC	Read Cycle	280		ns	3	
tSU1	Address Valid to EALE# Rising	23		ns	2	
tSA	SA Valid from EALE# Rising		35	ns	2	CL = 200 pF
tLA	Address Valid to LA Valid		36	ns	2	CL = 200 pF
tSALA	Sddress Valid to SA and LA valid in 486 mode		36	ns	2	CL = 200 pF
tSU10	CPU A Bus setup to IOR# or IOW# active	10		ns	2	
MASTER MODE TIMING						
tAM	A Bus Valid from SA/LA Input (Master Mode)		15	ns	4	CL = 200 pF
REAL-TIME CLOCK TIMING						
tPSPW	Power Sense Pulse Width	2		µs	5	
tPSD	Power Sense Delay	2		µs	5	
tVRTD	VRT Bit Delay		2	µs	5	

FIGURE 1. WRITE CYCLE TIMING (1)

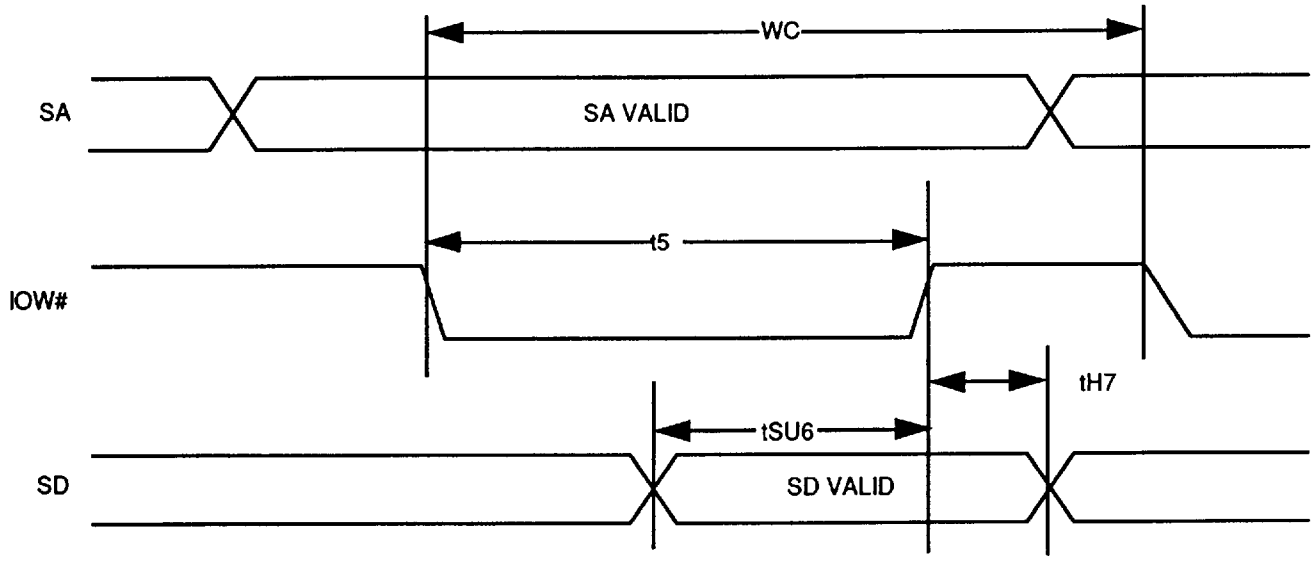


FIGURE 2. WRITE CYCLE TIMNG (2)

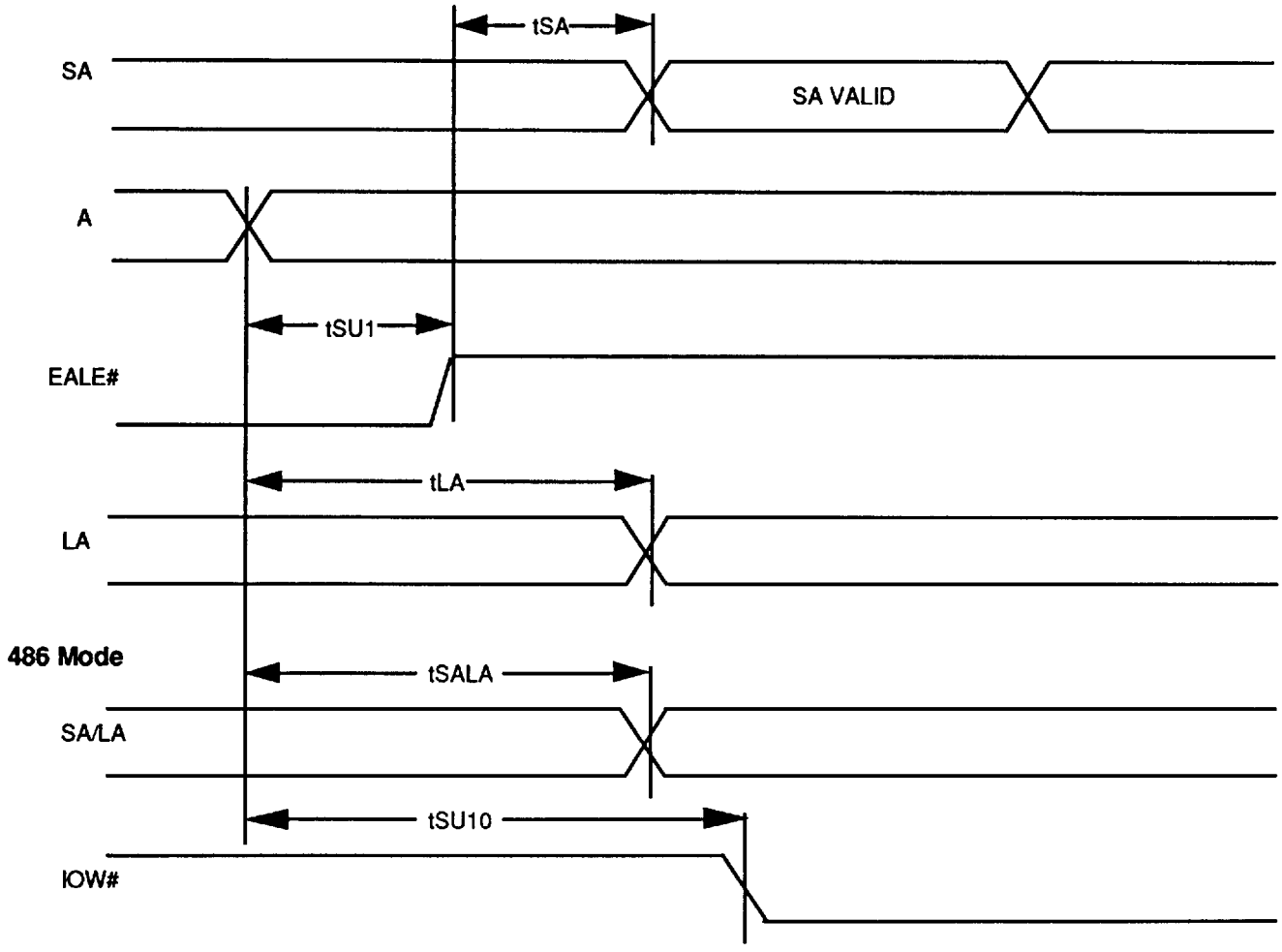


FIGURE 3. READ CYCLE TIMING

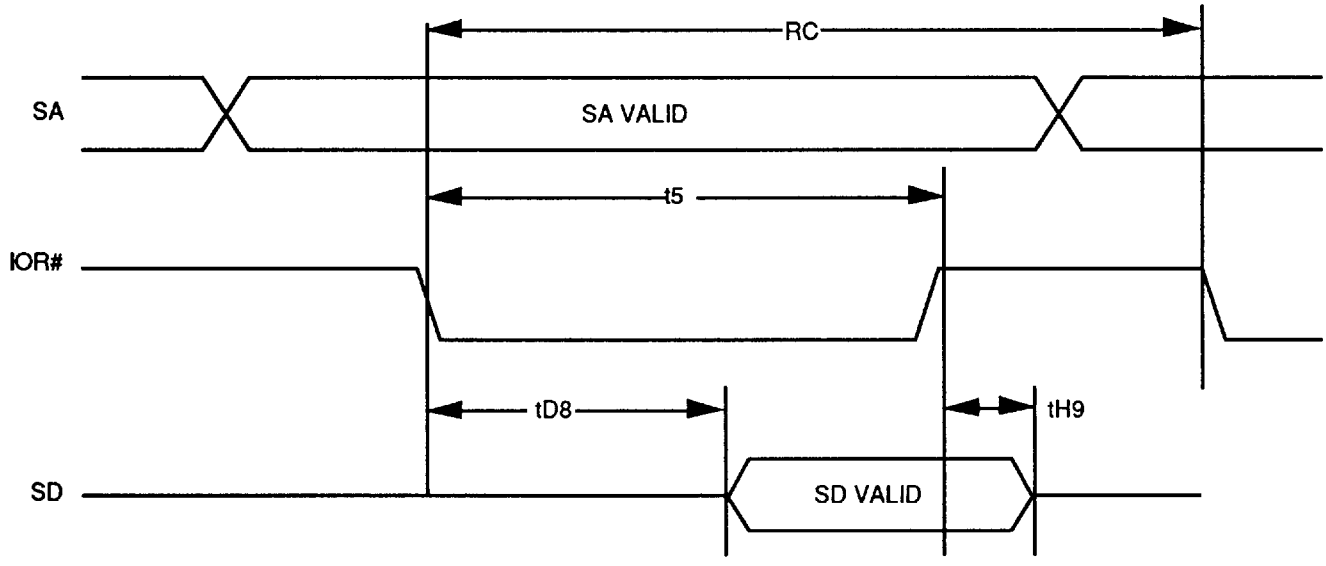


FIGURE 4. MASTER MODE BUS TIMING

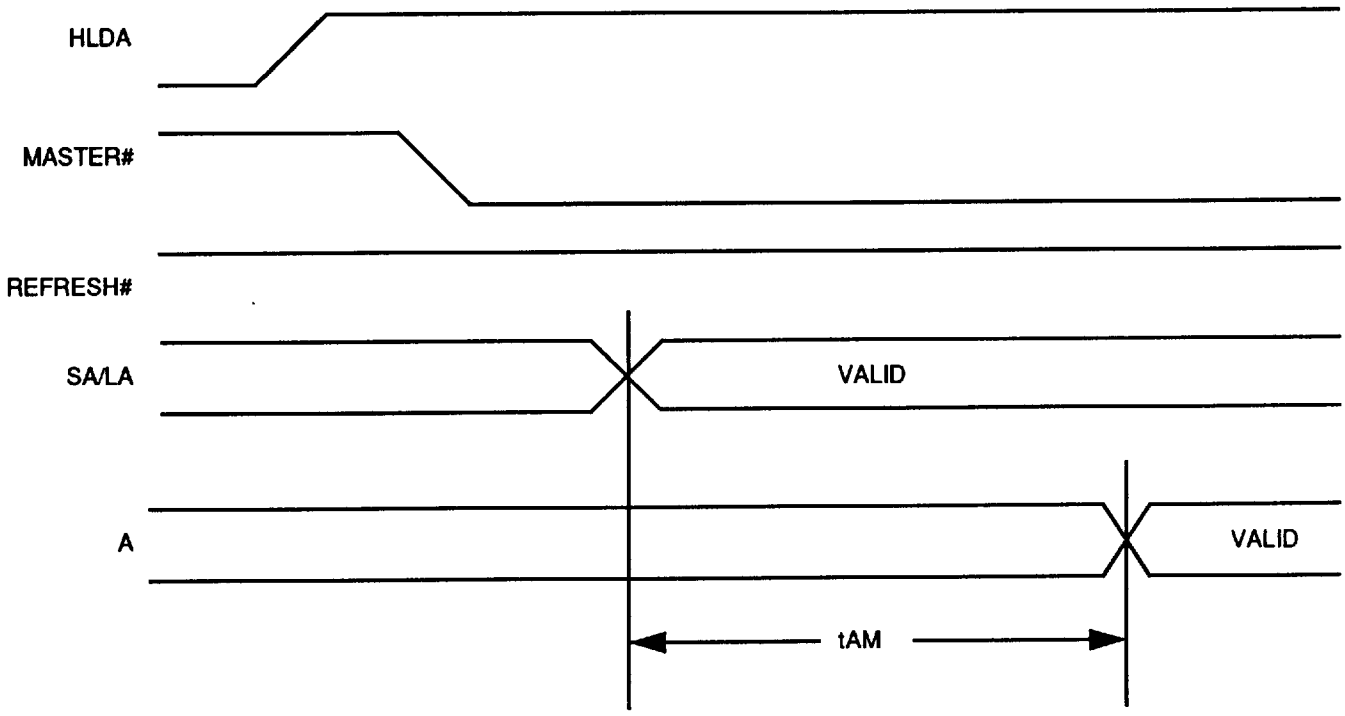
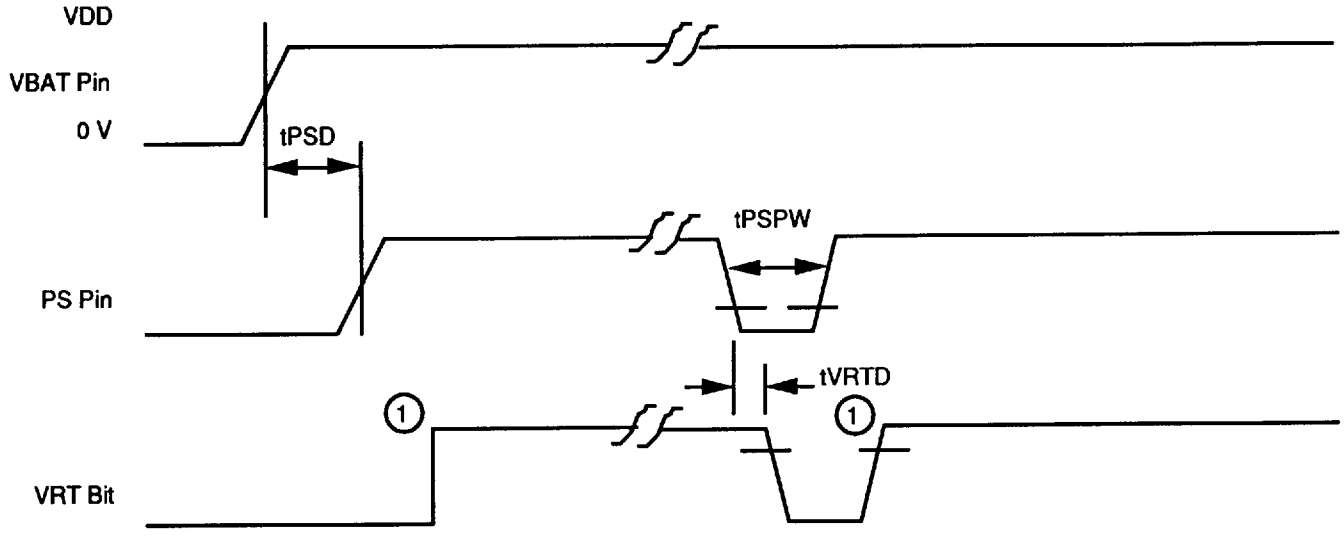
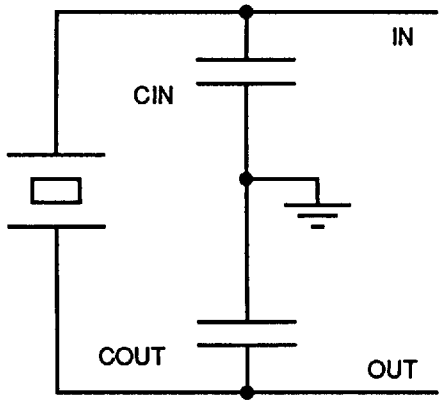


FIGURE 5. REAL-TIME CLOCK TIMING



(1) The VRT bit is set a '1 by reading Register D. The VRT bit can only be cleared by pulling the PS pin low (see REGISTER D ($0D)).

FIGURE 6. CRYSTAL OSCILLATOR CONFIGURATION



Notes: Frequency = 32.768 kHz
CIN = COUT = 10-22 pF (CIN may be a trimmer for precision timekeeping applications.)

Recommended Crystal Parameters:
Rs (max) ≤ 40 kΩ
Co (max) ≤ 1.7 pF
Ci (max) ≤ 12.5 pF
Parallel Resonance

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground Potential –0.5 V to VDD + 0.3 V

Applied Output Voltage –0.5 V to VDD + 0.3 V

Applied Input Voltage –0.5 V to + 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0 2.4	VDD + 0.5 VDD + 0.5	V V	TTL Level Inputs, Note 1 TTL Level Inputs, Note 2
VOL	Output Low Voltage		0.4 0.4 0.4 0.4	V V V V	IOL = 4 mA, Note 3A IOL = 8.0 mA, Note 4A IOL = 12.0 mA, Note 5 IOL = 24.0 mA, Note 6
VOH	Output High Voltage	2.4 2.4 2.4		V V V	IOH =0.8 mA, Note 3B IOH = 1.4 mA, Note 4B IOH = 2.4 mA, Note 6
IIH	Input High Current		10	µA	VIN = VDD, Note 7
IIL	Input Low Current	–10 –500	 50	µA µA	VIN = VSS + 0.2 V, Note 8 VIN = 0.8 V, Note 9
ILOL	Three-state Leakage Current	–50	 50	µA µA	VOUT = VSS + 0.2 V, Note 10 VOUT = VDD, Note 11
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
IDD	Operating Supply Current		40	mA	
IBAT	Supply Current, Standby Mode		5.0 5.0 50.0	µA µA µA	VBAT = 2.4 V VBAT = 3.0 V VBAT = 5.0 V
IDDQ	Static Supply Current		5.0	mA	

Notes: 1. Pins: REFRESH#, SA[0], SBHE#, MASTER#, EALE#, BHE#, HLDA, OSCI, KRSEL, KKSW, KCM, KI2/TRI#, IOW#, IOR#, SA[19:1], A[23:1], LA[23:17], SD[7:0], KIRQ, RTCIRQ#, KI3, KI5.

2. Pins: KHSE, KSRE, KDAT, KCLK, RSTDRV, PS.

3A. Pins: KIRQ, MIRQ, KI5, KI3.

3B. Pins: KIRQ, MIRQ, KI5, KI3, RTCIRQ#.

4A. Pins: A[23:1], BHE#.

4B. Pins: A[23:1], BHE#, KHSE/MDAT (PC/AT Mode only), KSRE/MCLK (PC/AT Mode Only).

5. Pins: KHSE, RTCIRQ#, KSRE, KDAT, KCLK.

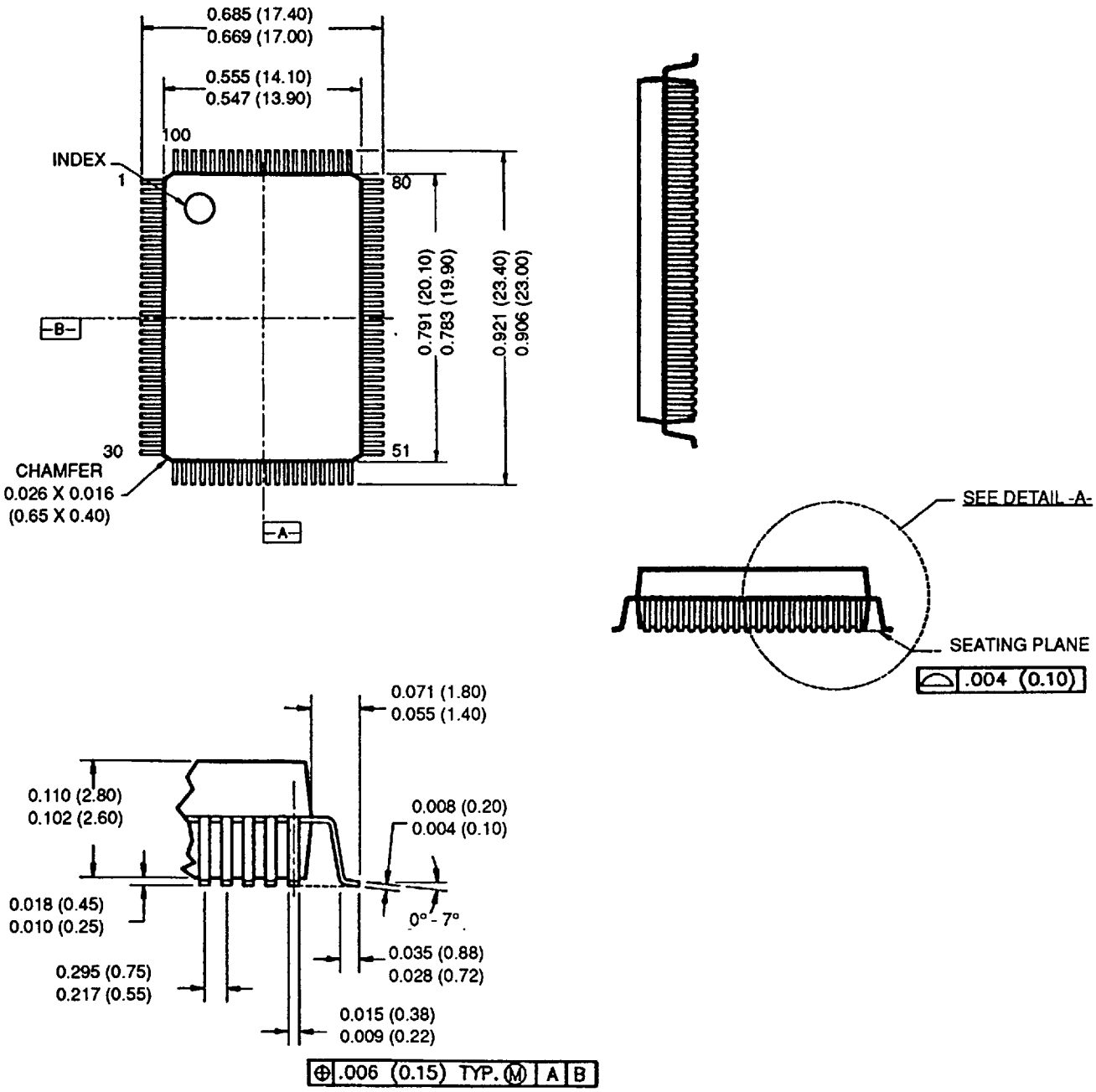
6. Pins: SBHE#, SA[19:1], LA[23:17], SD[7:0].

Notes (Cont.)

7. Pins: REFRESH#, SA[0], MASTER#, EALE#, HLDA, OSCI, KRSEL, KKSW, KCM, KI2/TRI#, PS, RSTDRV, IOW#, IOR#.
8. Pins: REFRESH#, SA[0], MASTER#, EALE#, HLDA, OSCI, KRSEL, PS, RSTDRV, IOW#, IOR#.
9. Pins: KIRQ, KKSW, KCM, KI5, KI3, KI2/TRI#.
10. Pins: SA[19:1], SBHE#, LA[23:17], A[23:1], SD[7:0], KHSE/MDAT, KSRE/MCLK, MIRQ, KDAT, KCLK, BHE#.
11. Pins: SA[19:1], SBHE#, LA[23:17], A[23:1], BHE#, KIRQ, KI5, KI3, SD[7:0], RTCIRQ#, MIRQ, KHSE/MDAT, KSRE/MCLK, KDAT, KCLK.

MECHANICAL PACKAGE OUTLINES

100 Lead Metric Quad Flat Pack (MQFP, Dwg No. 25-90007)**



Notes: 1. Controlling dimension is mm.
2. Dimensions are shown in inches (millimeters).