VLSI TECHNOLOGY, INC.

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PRELIMINARY

VL82C108

TOPCAT COMBO I/O CHIP

FEATURES

- Combines the following PC/AT®-compatible peripheral chips:
  - VL16C450 UART - COM1:
  - Parallel Printer Port - LPT1:
  - Keyboard/Mouse Ctrl. - KBD
- Serial ports fully 16C450-compatible
- Bidirectional line printer port
- CMOS direct drive of Centronics-type parallel interface
- PC/AT- or PS/2®-compatible keyboard and mouse controller
- IDE bus control signals include (two external 74LS245 and one 74ALS244 - or equivalent - buffers are required)
- Selectable chip select decodes
- Resides on SD bus directly
- Software controlled power-down with automatic keyboard "wakeup" option
- Single 100-lead plastic quad flat pack

DESCRIPTION

The VL82C108 Combo chip replaces with a single 100-pin chip, several of the commonly used peripherals found in PC/AT-compatible computers. This chip, when used with the VLSI PC/AT-compatible chip set, allows designers to implement a very cost effective, minimum chip count motherboard containing functions that are common to virtually all PCs.

The on-chip UART is completely software compatible with the VL16C450 ACE.

The bidirectional parallel port provides a PS/2 software compatible interface between a Centronics-type printer and the VL82C108. Direct drive is provided so that all that is needed to interface to the line printer port is a resistor/capacitor network. The bidirectional feature (option) is software programmable for backwards PC/AT-compatibility.

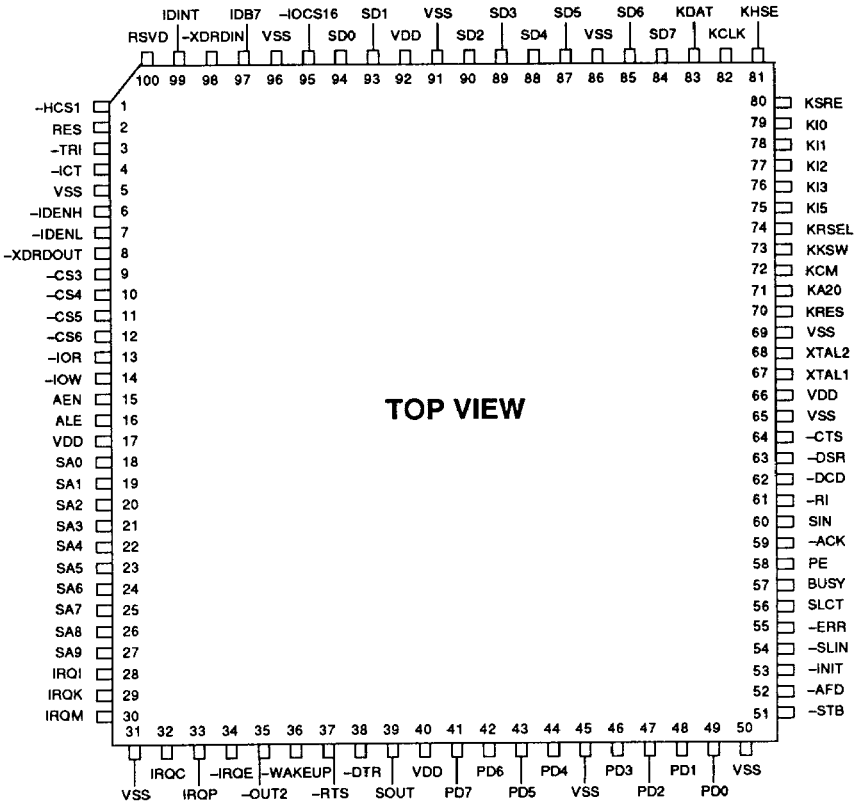
The keyboard/mouse controller is selectable as PC/AT- or PS/2-compatible.

Included is the control logic necessary for the support of the Integrated Drive Electronics (IDE) hard disk bus interface. Hard disk drives which support the IDE interface often refer to this interface as "AT Bus" compatible or "Embedded AT Bus" compatible.

The Combo I/O chip also includes selectable chip selects for the internal UART and printer port, and four fixed chip selects for external floppy and hard disk controllers.

PIN DIAGRAM

VL82C108



ORDER INFORMATION

Part Number	Package
VL82C108-FC	Plastic Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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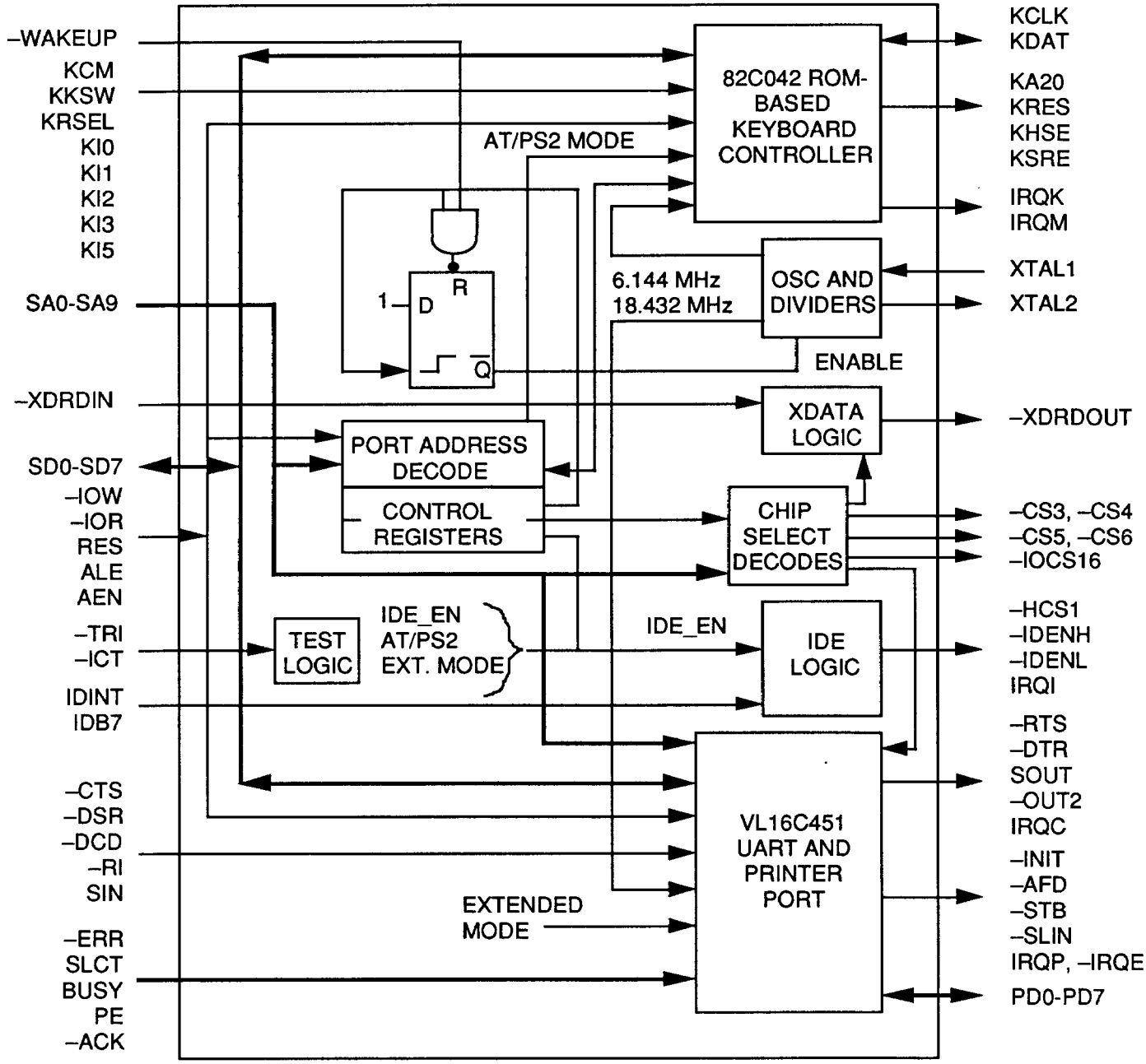
BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
COMMUNICATIONS PORT A (10 pins, 3F8H-3FFH or 2F8H-2FFH, IRQC)			
–RTS	37	O1	Request to Send
–DTR	38	O1	Data Terminal Ready
SOUT	39	O1	Serial Data Output
–CTS	64	I4	Clear to Send
–DSR	63	I4	Data Set Ready
–DCD	62	I4	Data Carrier Detect
–RI	61	I4	Ring Indicator
SIN	60	I4	Serial Input
IRQC	32	O6	Interrupt Request
–OUT2	35	O1	Output 2
PARALLEL PRINTER PORT (19 pins, 378H-37AH or 3BCH-3BFH or 278H-27FH, IRQP)			
PD0	49	IO5	Printer Data Port, Bit 0
PD1	48	IO5	Printer Data Port, Bit 1
PD2	47	IO5	Printer Data Port, Bit 2
PD3	46	IO5	Printer Data Port, Bit 3
PD4	44	IO5	Printer Data Port, Bit 4
PD5	43	IO5	Printer Data Port, Bit 5
PD6	42	IO5	Printer Data Port, Bit 6
PD7	41	IO5	Printer Data Port, Bit 7
–INIT	53	O4	Initialize Printer Signal
–AFD	52	O4	Autofeed Printer Signal
–STB	51	O4	Data Strobe to Printer
–SLIN	54	O4	Select Signal to Printer
–ERR	55	I4	Error Signal from Printer
SLCT	56	I4	Select Signal from Printer
BUSY	57	I4	Busy Signal from Printer
PE	58	I4	Paper Error Signal from Printer
–ACK	59	I4	Acknowledge Signal from Printer
IRQP	33	O6	Printer Interrupt Request Output
–IRQE	34	O1	Printer Interrupt Request Enabled Signal

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	AT Mode	Signal Description	PS/2 Mode	Signal Description
KEYBOARD CONTROLLER PORT (16 pins, IRQK, IRQM)						
KCLK	82	IO4	T0/–P26	Keyboard Clock	T0/–P26	Keyboard Clock
KDAT	83	IO4	T1/P27	Keyboard Data	P10/–P27	Keyboard Data
KCM	72	I4	P16	Color Input	P16	Input
KKSW	73	I4	P17	Key Sw Input	P17	Input
KA20	71	O1	P21	A20 Gate Output	P21	A20 Gate Output
KRES	70	O1	P20	Reset Command	P20	Reset Command
KHSE	81	O1/IO4	P22	High Speed	P11/–P22	Mouse Data
KSRE	80	O1/IO4	P23	Shadow RAM	T1/–P23	Mouse Clock
IRQK	29	O1	P24	Keyboard Intrp Request	P24	Keyboard Intrp Request
IRQM	30	O1	P25	Output	P25	Mouse Interrupt Request
KRSEL	74	I4	P14	RAM Select	P14	Input
KI0	79	IO6	P10	Input	MISCOUT1	Output
KI1	78	IO6	P11	Input	MISCOUT2	Output
KI2	77	I4	P12	Input	P12	Fuse Input
KI3	76	I4	P13	Input	P13	Input
KI5	75	I4	P15	Input	P15	Input

Signal Name	Pin Number	Signal Type	Signal Description
IDE BUS I/O (6 Pins, IRQI)			
–IDENH	6	O1	IDE Bus Transceiver High Byte Enable
–IDENL	7	O1	IDE Bus Transceiver Low Byte Enable
IDINT	99	I4	IDE Bus Interrupt Request Input
IDB7	97	IO6	IDE Bus Data Bit 7
–HCS1	1	O1	IDE Host Chip Select 1
–IRQI	28	O6	IDE Interrupt Request Output
COMMON BUS I/O (36 Pins)			
SD0	94	IO2	System Bus Data, Bit 0
SD1	93	IO2	System Bus Data, Bit 1
SD2	90	IO2	System Bus Data, Bit 2
SD3	89	IO2	System Bus Data, Bit 3
SD4	88	IO2	System Bus Data, Bit 4
SD5	87	IO2	System Bus Data, Bit 5
SD6	85	IO2	System Bus Data, Bit 6
SD7	84	IO2	System Bus Data, Bit 7
SA0	18	I1	System Bus Address, Bit 0
SA1	19	I1	System Bus Address, Bit 1

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SA2	20	I1	System Bus Address, Bit 2
SA3	21	I1	System Bus Address, Bit 3
SA4	22	I1	System Bus Address, Bit 4
SA5	23	I1	System Bus Address, Bit 5
SA6	24	I1	System Bus Address, Bit 6
SA7	25	I1	System Bus Address, Bit 7
SA8	26	I1	System Bus Address, Bit 8
SA9	27	I1	System Bus Address, Bit 9
XTAL1	67	NA	Crystal/Clock Input - 18.432 MHz
XTAL2	68	NA	Crystal/Clock Output - 18.432 MHz
–IOR	13	I1	System Bus I/O Read
–IOW	14	I1	System Bus I/O Write
RES	2	I5	System Reset
AEN	15	I1	System Bus Address Enable
ALE	16	I1	System Bus Address Latch Enable
–IOCS16	95	O8	System Bus I/O Chip Select 16
–CS3	9	O9	Chip Select 3 - Normally for external floppy disk controller.
–CS4	10	O1	Chip Select 4 - Normally –HCS0 for IDE.
–CS5	11	O9	Chip Select 5 - Normally for external floppy disk controller.
–CS6	12	O9	Chip Select 6 - Normally for external floppy disk controller.
–XDRDIN	98	I1	X Data Bus Direction Control Input
–XDRDOUT	8	O1	S Bus direction generated for CS during a read.
–WAKEUP	36	I4	Keyboard Wakeup Input.
–TRI	3	I4	Three-state Control Input - For all outputs to isolate chip for board tests.
–ICT	4	I4	In Circuit Test Mode Control
RSVD	100	I2	VLSI Reserved - DO NOT CONNECT TO VSS OR VDD.
POWER, GROUND, & UNCOMMITTED (13 Pins)			
VDD	17, 40, 66, 92		System Power: +5 V
VSS	5, 31, 45, 50, 65, 69, 86, 91, 96		System Ground

I/O LEGEND

	mA	Type	Comment
O1	2	TTL	
O4	12	TTL-OD	Open drain, weak pull-up, no VDD diode
O6	4	TTL-TS	Three-State
O8	24	TTL-OD	Open drain, fast active pull-up
O9	2	TTL-OD	Open drain
I1	–	TTL	
I2	–	CMOS	
I4	–	TTL	30k Ω pull-up
I5	–	TTL	Schmitt-trigger
IO2	24	TTL-TS	Three-State
IO4	12	TTL-OD	Open drain, slow turn-on, Schmitt-trigger
IO5	12	TTL-TS	Three-State
IO6	24	TTL-TS	Three-State, 30k Ω pull-up

FUNCTIONAL DESCRIPTION

Below is a detailed explanation of each of the major building blocks of the VL82C108 Combo chip. The following functional blocks are covered:

- 16C450 Serial Ports
- Parallel Printer Port
- Keyboard Controller
- Control and Chip Selects
- IDE Interface

SERIAL COMMUNICATIONS PORTS

The chip contains a UART based on the VL16C450 Megacell core. The baud-rate clock is the XTAL1 input (18.432 MHz) divided by ten. The 18.432 MHz signal is shared with the keyboard controller, which divides it by three to get an approximate 6 MHz reference clock. Please refer to the VL16C450 data sheet for the register descriptions.

COMA is accessed via internally generated CS1.

LINE PRINTER PORT

The Line Printer Port contains the functionality of the port included in the VL16C451, but offers a software programmable Extended Mode. These features are disabled on initial power-up, but may be turned on by setting the –EMODE bit of the Control Register (I/O PORT 102H in PS/2 mode). When the –EMODE bit is not enabled, the part functions exactly as a PC/AT-compatible printer port.

The Line Printer Port is accessed via internally generated programmable chip select CS2.

Register 0 - Line Printer Port Data

The Line Printer (LPT) Port is either uni- or bidirectional, depending on the state of the Extended Mode and Data Direction Control bits.

Compatibility Mode (–EMODE bit = 1) - When in compatibility mode, read operations to this register return the last data that was written to the LPT Port.

Extended Mode (–EMODE bit = 0) - Read operations return either the data last written to the LPT Data Register if the Direction Bit is set to Write (0) or the data that is present on the pins of the LPT Port if the direction is set to Read (1). Write operations latch data into the output register, but only drive the LPT Port when the Direction Bit is set to Write.

In either case, the bits of the LPT Data Register are defined as follows:

Register 1 - LPT Port Status

Bit	Description	
0	Data Bit 0	PD0
1	Data Bit 1	PD1
2	Data Bit 2	PD2
3	Data Bit 3	PD3
4	Data Bit 4	PD4
5	Data Bit 5	PD5
6	Data Bit 6	PD6
7	Data Bit 7	PD7

The LPT Status Register is a read-only register that contains interrupt status and real-time status of the LPT connector pins. The bits are described as follows:

Bit	Description
0	Reserved
1	Reserved
2	–IRQ
3	–ERROR
4	SLCT
5	PE
6	–ACK
7	–BUSY

Bits 0 and 1 - Reserved, read as "1's".

Bit 2 - Interrupt Status bit (active low) - A "0" indicates that the printer has acknowledged the previous transfer with an ACK handshake (bit 4 of the control register must be set to "1").

Bit 3 - Error Status bit - When reset, "0" indicates that the printer has had an error. A "1" indicates normal operation. This bit follows the state of the –ERR pin.

Bit 4 - Select Status bit, indicates the current status of the SLCT signal from the printer. A "0" indicates the printer is currently not selected (off-line). A "1" means the printer is currently selected.

Bit 5 - Paper Empty Status bit, a "0" indicates normal operation. A "1" indicates that the printer is currently out of paper. This bit follows the state of the PE pin.

Bit 6 - Acknowledge Status bit - A "0" indicates that the printer has received a character and is ready to accept another. A "1" indicates that the last operation to the printer has not been completed yet. This bit follows the state of the –ACK pin.

Bit 7 - Busy Status bit, a "0 indicates that the printer is busy and cannot receive data. A "1" indicates that the printer is ready to accept data. This bit follows the inversion of the state of the BUSY pin.

Register 2 - LPT Port Control

This port is a read/write port that is used to control the LPT direction as well as the Printer Control lines driven from the port. Write operations set or reset these bits, while read operations return the status of the last write operation to this register (except for bit 5 which is write-only and is always read back as a (1). The bits in this register are defined as follows:

Bit	Description
0	STROBE
1	AFD
2	–INIT
3	SLCT IN
4	IRQ EN
5	DIR (Write Only)
6	Reserved
7	Reserved

Bit 0 - Printer Strobe (STROBE) Control bit - When set (1), the STROBE signal is asserted on the LPT interface, causing the printer to latch the current data. When reset (0), the signal is negated.

Bit 1 - Autofeed (AFD) Control bit - When set (1), the AFD signal will be asserted on the LPT interface, causing the printer to automatically generate a line feed at the end of each line. When reset (0), the signal is negated.

Bit 2 - Initialize Printer (–INIT) Control bit - When set (1), the signal is negated. When reset (0), the INIT signal is asserted to the printer forcing a reset.

Bit 3 - Select Input (SLCT IN) Control bit - When set (1), the SLCT IN signal is asserted causing the printer to go "on-line". When reset (0), the signal is negated.

Bit 4 - Interrupt Request Enable (IRQ EN) Control bit - When set (1), enables interrupts from the LPT Port whenever the –ACK signal is asserted by the printer. When reset (0), interrupts are disabled.

Bit 5 - When –EMODE = 0 and the Direction (DIR) Control bit is set (1), the output buffers in the LPT Port are disabled allowing data driven from external sources to be read from the LPT Port. When reset (0), the output buffers are enabled, forcing the LPT pins to drive the LPT pins. The power-on-reset value of this is cleared (0). This bit is always read as a "1". When –EMODE = 1, this control bit has no effect on device operation.

Bits 6 and 7 - Reserved, read as "1's".

KEYBOARD CONTROLLER

The Keyboard Controller is accessed via internally decoded Port 060H (read/write data) and Port 064H (read status/write command).

PC/AT or PS/2 compatibility is controlled via bit one in the control register at address 103H.

FUNCTIONAL DESCRIPTION

The Micro Controller Unit (MCU) offers a subset of the instruction set of the 8042, with 8042-like instructions. Enhancements have been made to conditional jumps (jumps may be made between pages). The on-chip program ROM is normally loaded with the code that is required to support the PC/AT and PS/2 command sets and 128 bytes of conversion code. A small amount of scratchpad RAM is provided as an extension of the MCU register set for the purpose of keyboard to host interfacing.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simplify error handling in software. This logic is duplicated for the mouse interface.

User RAM support is provided. The program writes the 5-bit address (32-byte range in PS/2 Mode) to a register, and then reads or writes the data through accesses to another register, Port 60 DBB.

Parallel Ports 1 and 2 are provided, but are restricted to inputs only for P1 and outputs only to P2.

Support for Port 60 DBB (reads and writes) and Status Register (reads and writes) is provided in hardware for interface to the PC host.

Common PC/AT uses for the Parallel I/O bits are shown as follows:

- P16 - Color/Monochrome Input
- P17 - Key Switch Input
- P20 - Reset CPU Output
- P21 - A20 Gate Output
- P22 - Speed Select Output

KEYBOARD CONTROLLER INTERFACE TO PC/AT

The interface to the PC/AT consists of one register pair (60H/64H) for the keyboard and mouse. Access to the registers is determined by the state of A2 and the chip select. For host control signals involved, the command, status and data registers are accessed as shown below.

The Port 60 DBB read operations output the contents of the Output Buffer to D0-D7 (host bidirectional, three-stateable data bus), and clears the status of the Output Buffer Full (OBF/Status Register bit 0) bit.

Status read operations output the contents of the Status Register to D0-D7. No status is changed as a result of the read operation.

The Port 60 DBB write operations cause the Input Buffer DBB to be changed. The state of the C/D bit is cleared (Status Register bit 3, "0" indicates data) and the Input Buffer Full (IBF/Status Register bit 1) bit is set (1).

Command write operations are the same as DBB writes, except that the address is 64H. The C/D bit will be set (1) when a command has been written to address 64H.

–CS	–RD	–WR	A2	Register
0	0	1	0	Read - Data DBB Output Buffer
0	0	1	1	Read - Status
0	1	0	0	Write - Data DBB Input Buffer
0	1	0	1	Write - Command
1	x	x	x	Not Valid

KEYBOARD PORT INTERFACE PROTOCOL

Data transmission between the controller, the keyboard, and mouse consists of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start Bit (Always 0)
2	Data Bit 0 (LSB)
3-8	Data Bits 1-6
9	Data Bit 7 (MSB)
10	Parity Bit (Odd)
11	Stop Bit (Always 1)

FIGURE 1. IMPLEMENTED STATES FOR RECEIVE OPERATIONS

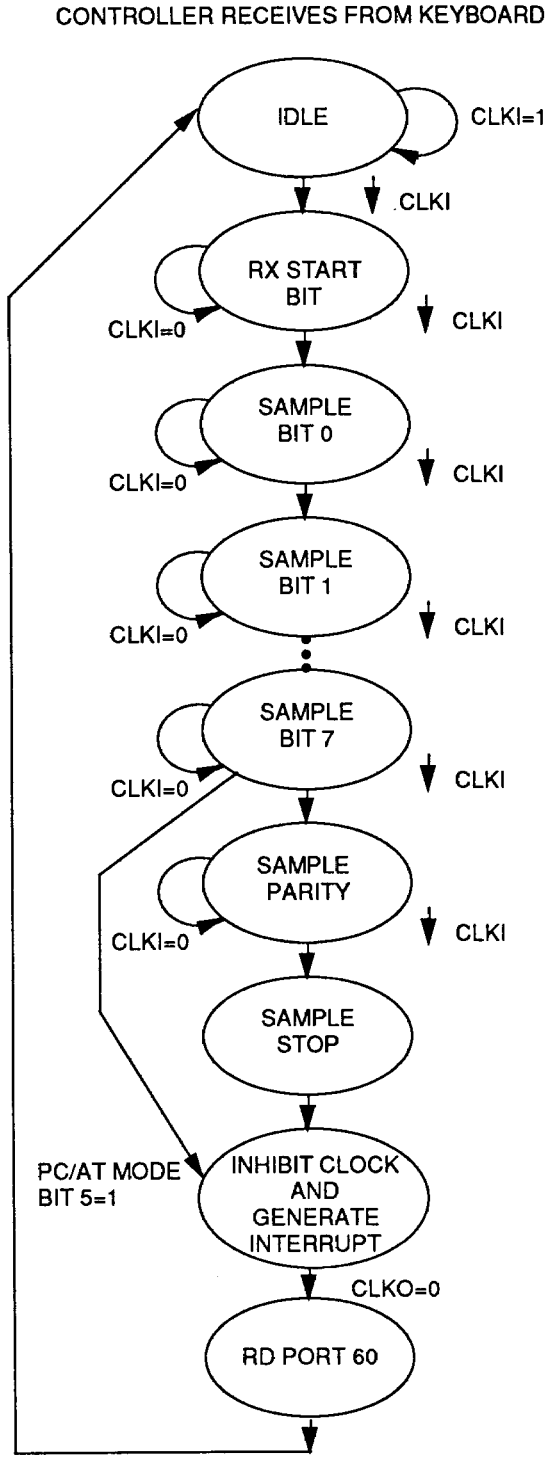
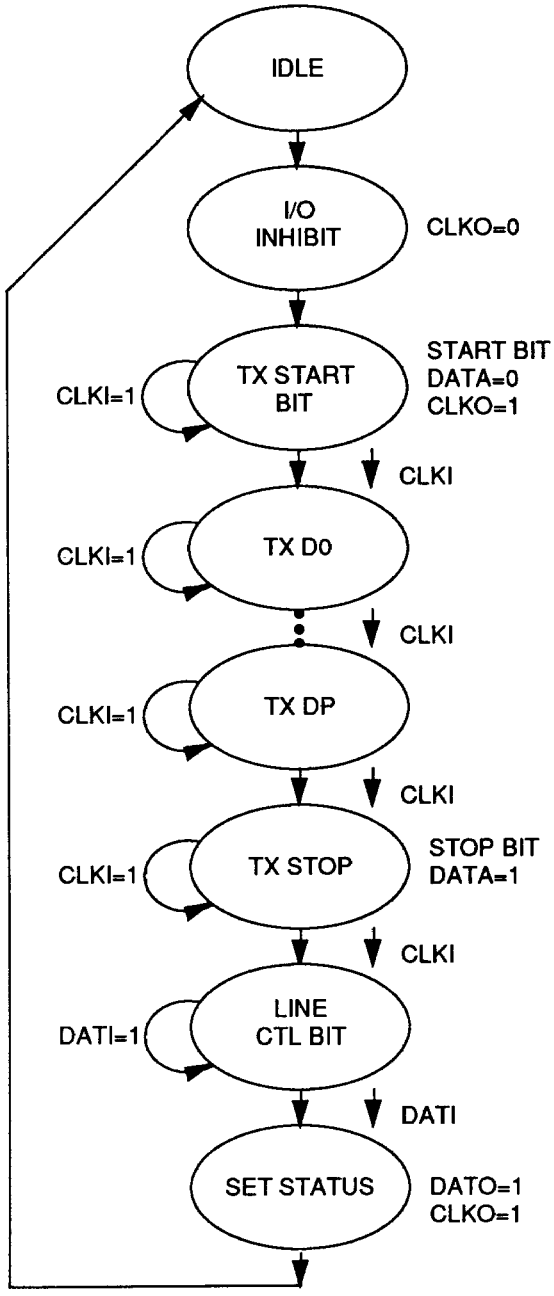


FIGURE 2. IMPLEMENTED STATES FOR TRANSMIT OPERATIONS

CONTROLLER TRANSMITS TO KEYBOARD



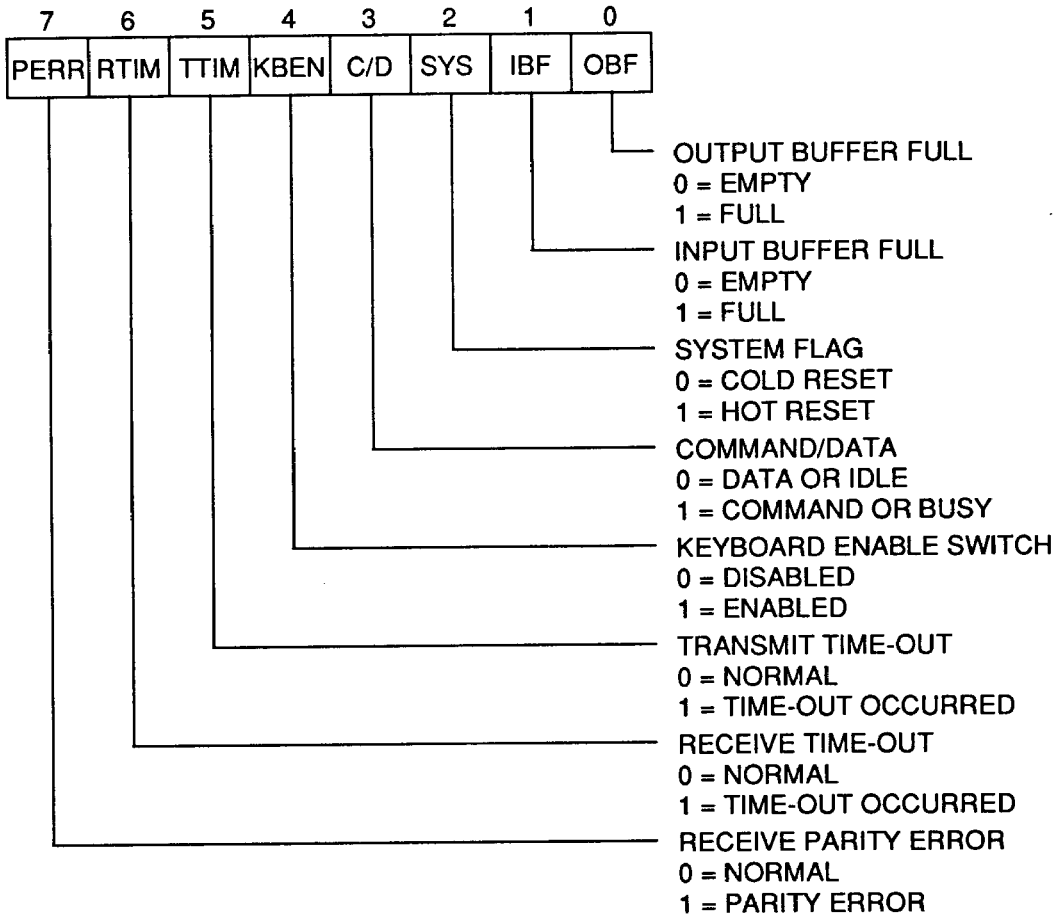
PROGRAMMER INTERFACE

The programmer interface to the keyboard controller is quite simple, consisting of four registers.

Register	R/W	I/O
Status	R	64H
Command	W	64H
Output Buffer	R	60H
Input Buffer	W	60H

The behavior of these registers differ according to the mode of operation (PC/AT or PS/2). There exists only one status register with different bit definitions for PC/AT mode and PS/2 mode. The bit definitions for the status register in each mode follows.

FIGURE 3. PC/AT STATUS REGISTER (READ ONLY - PORT 64H)



PC/AT Status Register

Bit 0 - Output Buffer Full (OBF) - This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to Port 60H.

Bit 1 - Input Buffer Full (IBF) - This flag is set on a write to Port 60H or 64H. It is cleared when the microcontroller reads the DBBIN contents into the accumulator.

Bit 2 - System Flag (SYS) - When set (1), indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (C/D) - When set (1), indicates that a command has been placed into the Input Data Buffer of the controller. A "0" indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input Data Buffer.

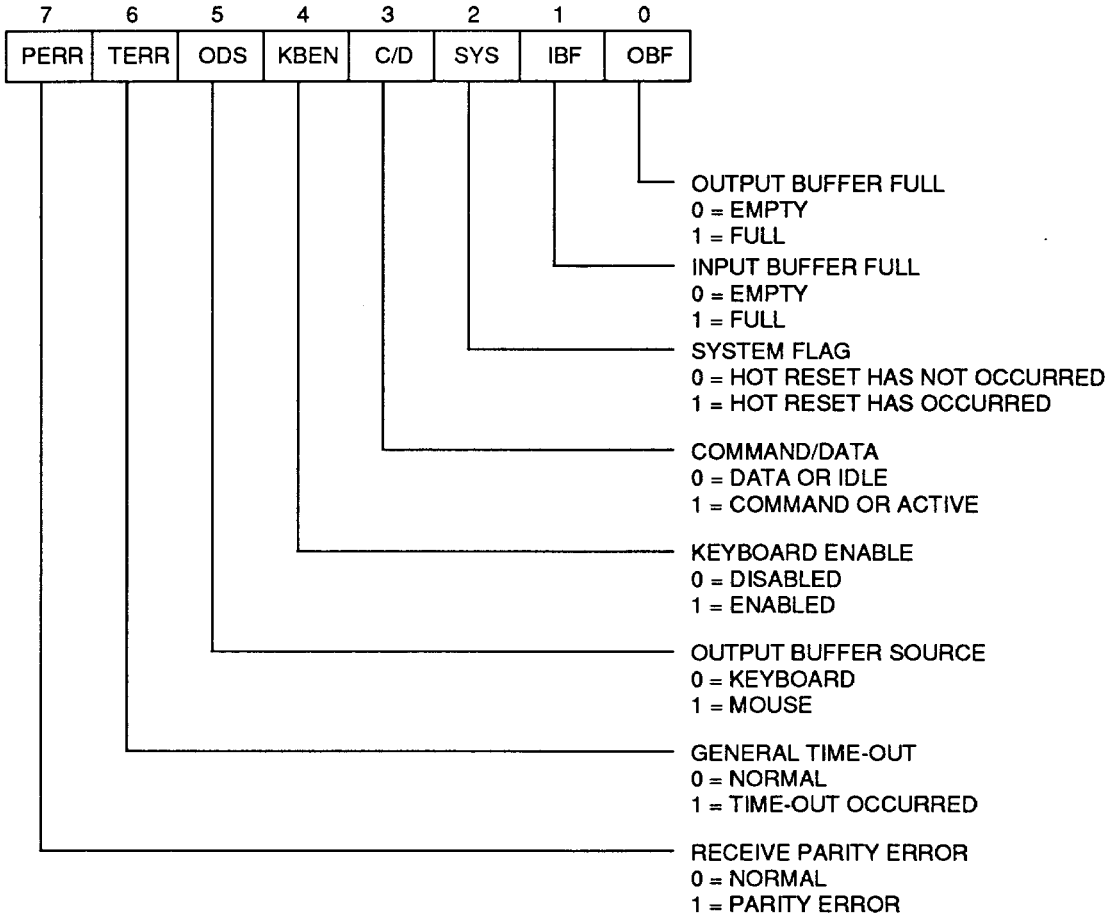
Bit 4 - Keyboard Enable (KBEN) indicates the state of the 'keyboard inhibit' switch input (KKSW). "0" indicates the keyboard is inhibited.

Bit 5 - Transmit Time-out (TTIM) - When set (1), indicates that a transmission to the keyboard was not completed before the controller's internal timer timed-out.

Bit 6 - Receive Time-out (RTIM) - When set (1), indicates that a transmission from the keyboard was not completed before the controller's internal timer timed-out.

Bit 7 - Parity Error (PERR) - When set (1), indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the KIRQ pin is set ["1" if the EKI bit/Mode Register bit 0 is set (1)].

FIGURE 4. PS/2 STATUS REGISTER (READ ONLY - PORT 64H)



PS/2 Status Register

Bit 0 - Output Buffer Full (OBF) - When set (1), indicates that data is available in the controller Data Bus Buffer, and that the CPU has not read the data yet. The CPU reads to PORT 60H reset the state of this bit.

Bit 1 - Input Buffer Full (IBF) - When set (1), indicates that data has been written to PORT 60H or 64H, and the controller has not read the data.

Bit 2 - System Flag (SYS) - When set (1), indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (C/D) - When set (1), indicates that a command has been placed into the Input Data Buffer of the controller. The controller uses this bit to determine if the byte written is a command to be executed. This bit is not reset until the command has completed its operation.

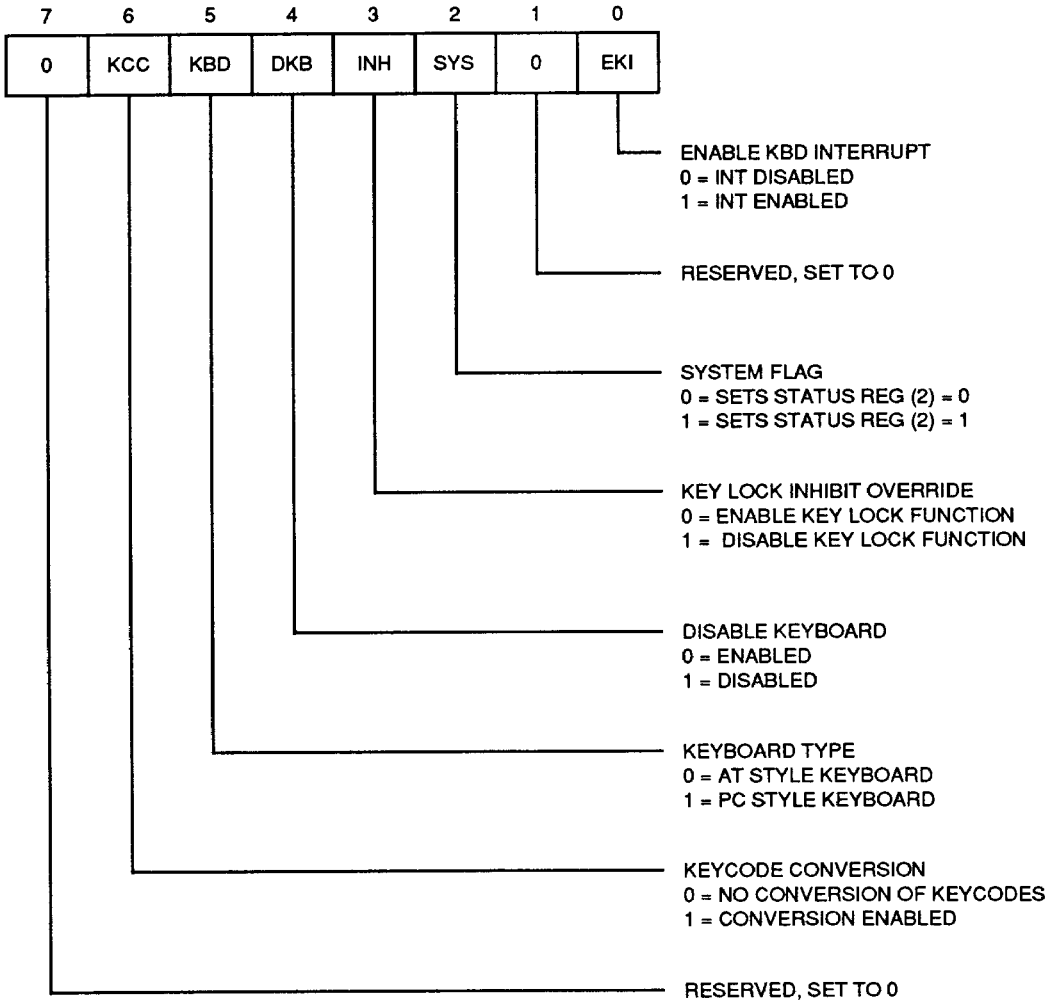
Bit 4 - Keyboard Enable (KBEN) indicates the state of the "keyboard inhibit" switch input (KKSW). "0" indicates the keyboard is inhibited.

Bit 5 - Output Buffer Data Source (ODS) - When set (1), indicates that the data in the output buffer is mouse data. When reset, it indicates the data is from the keyboard.

Bit 6 - Time-out Error (TERR) - When set (1), indicates that a transmission was started and that it did not complete within the normal time taken (approximately 11 KCKIN cycles). If the transmission originated from the controller, a FEH is placed in the output buffer. If the transmission originated from the keyboard, a FFH is placed in the output buffer.

Bit 7 - Parity Error (PERR) - When set (1), indicates that a parity error (even parity = error) occurred during the last transmission from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the KIRQ pin is set ["1" if the EKI bit/ Mode Register bit 0 is set (1)].

FIGURE 5. PC/AT MODE REGISTER (READ PORT 60H AFTER WRITE COMMAND 20H TO PORT 64H)



PC/AT MODE REGISTER

Bit 0 - Enable Keyboard Interrupt (EKI) - When set (1,) allows the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Bit 1 - Reserved, should be written as "0".

Bit 2 - System Flag (SYS) - When set (1), writes the System Flag bit of the Status Register to "1". This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Inhibit Override (INH) - When set (1), disables the keyboard inhibit function (P17 Switch).

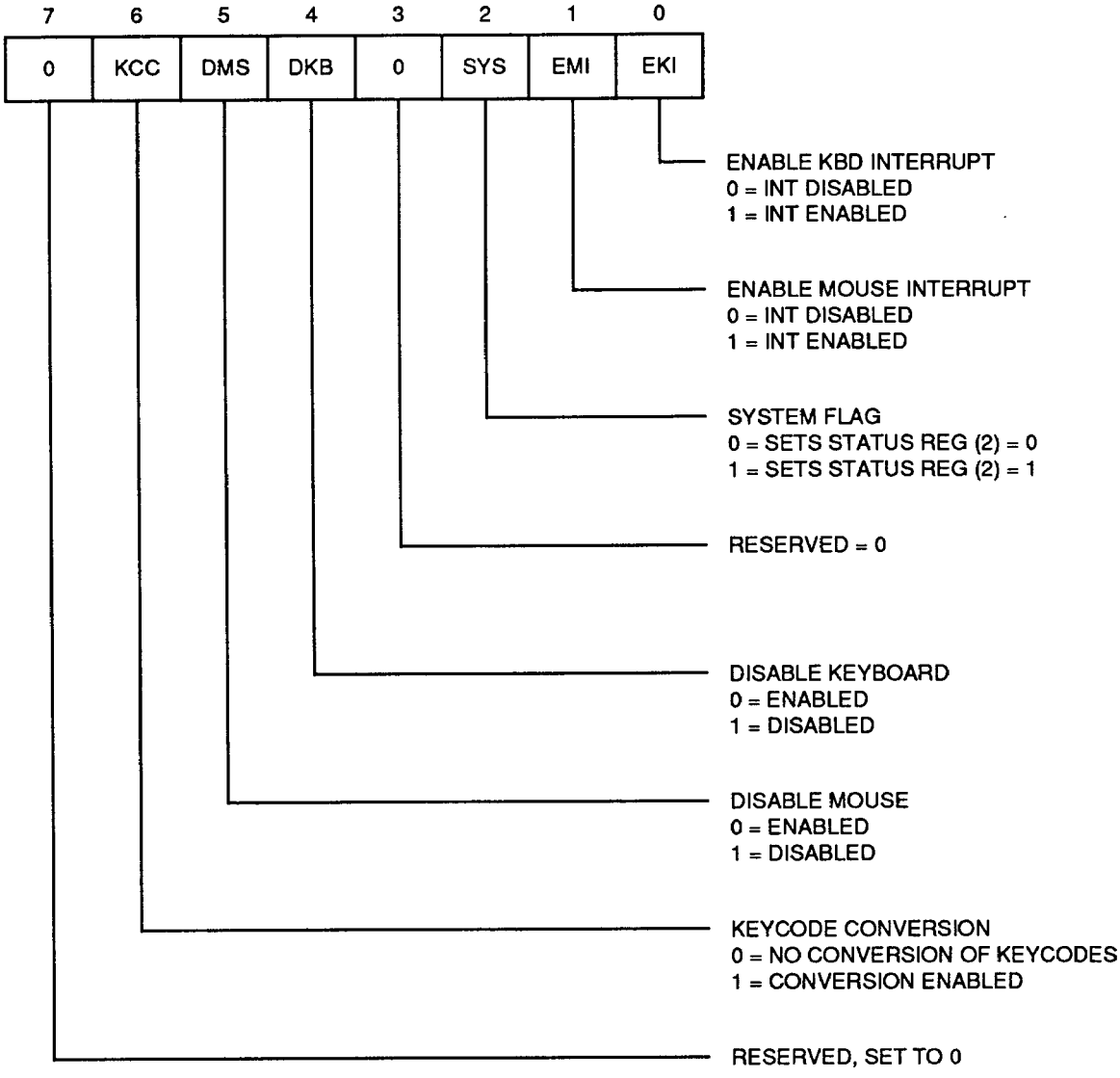
Bit 4 - Disable Keyboard (DKB) - When set (1), disables the keyboard by holding the –KCKOUT line low.

Bit 5 - Keyboard Type (KBD) - When set (1), allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.

Bit 6 - Keycode Conversion (KCC) - When set (1), causes the controller to convert the scan codes to PC format. When reset, the codes (AT keyboard) are passed along unconverted.

Bit 7 - Reserved, should be written as "0".

FIGURE 6. PS/2 MODE REGISTER (READ PORT 60H AFTER WRITE COMMAND 20H TO PORT 64H)



PS/2 MODE REGISTER

Bit 0 - Enable Keyboard Interrupt (EKI) - When set (1), allows the controller to generate a keyboard interrupt whenever data (keyboard or command) is written into the output buffer.

Bit 1 - Enable Mouse Interrupt (EMI) - When set (1), allows the controller to generate a mouse interrupt when mouse data is available in the output buffer.

Bit 2 - System Flag (SYS) - When set (1), writes the System Flag bit of the Status Register to "1". This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Reserved, "0".

Bit 4 - Disable Keyboard (DKB) - When set (1), disables the keyboard by holding the –KCKOUT high.

Bit 5 - Disable Mouse (DMS) - When set (1), disables the mouse by holding the –MCKOUT high.

Bit 6 - Keycode Conversion (KCC) - When set (1), causes the controller to convert the scan codes to PC format. When reset, the codes (AT keyboard) are passed along unconverted.

Bit 7 - Reserved, "0".

FIGURE 7. PC/AT KEYBOARD SCAN CODE TRANSLATION TO PC/XT SCAN CODE

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
00	ff
01	43
02	41
03	3f
04	3d
05	3b
06	3c
07	58
08	64
09	44
0a	42
0b	40
0c	3e
0d	0f
0e	29
0f	59
10	65
11	38
12	2a
13	70
14	1d
15	10
16	02
17	5a
18	66
19	71
1a	2c
1b	1f
1c	1e
1d	11
1e	03
1f	5b
20	67
21	2e
22	2d
23	20
24	12
25	05
26	04
27	5c
28	68
29	39
2a	2f
2b	21
2c	14
2d	13
2e	06
2f	5d

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
30	69
31	31
32	30
33	23
34	22
35	15
36	07
37	5e
38	6a
39	72
3a	32
3b	24
3c	16
3d	08
3e	09
3f	5f
40	6b
41	33
42	25
43	17
44	18
45	0b
46	0a
47	60
48	6c
49	34
4a	35
4b	26
4c	27
4d	19
4e	0c
4f	61
50	6d
51	73
52	28
53	74
54	1a
55	0d
56	62
57	6e
58	3a
59	36
5a	1c
5b	1b
5c	75
5d	2b
5e	63
5f	76

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
60	55
61	56
62	77
63	78
64	79
65	7a
66	oe
67	7b
68	7c
69	4f
6a	7d
6b	4b
6c	47
6d	7e
6e	7f
6f	6f
70	52
71	53
72	50
73	4c
74	4d
75	48
76	01
77	45
78	57
79	4e
7a	51
7b	4a
7c	37
7d	49
7e	46
7f	54

The following scan codes are converted by inline code:

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
83	41
84	54

Note: All other PC/AT scan codes are passed to the system untranslated.

COMMAND SET

The command set supported by the keyboard controller supports two modes of operation and a set of extensions to the AT command set for the PS/2. In both modes, the command is implemented by writing the command byte to PORT 64H. Any subsequent data is read from PORT 60H (see description of command 20) or written to PORT 60H (see description of command PORT 60H). The commands for each mode are shown in the table below:

PC/AT Mode:

Comm.	Description
20	Read Mode Register
60	Write Mode Register
AA	Self Test
AB	KBD Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port (P10-P17)
D0	Read Output Port (P20-P27)
D1	Write Output Port (P20-P27)
E0	Read Test Inputs (T0, T1)
F0-FF	Pulse Output Port (P20-P27)

Added PS/2 Commands:

Comm.	Description
21-3F	Read Keyboard Controller RAM (Byte 1-31)
61-7F	Write Keyboard Controller RAM (Byte 1-31)
A4	Test Password
A5	Load Password
A6	Enable Password
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
C1	Poll in Port Low (P10-P13 -> S4-S7)
C2	Poll in Port High (P14-P17 -> S4-S7)
D2	Write Keyboard Output Buffer
D3	Write Mouse Output Buffer
D4	Write to Mouse

The following is a description of each command:

20 Read the keyboard controller's Mode Register (PC/AT and PS/2) - The keyboard controller sends its current mode byte to the output buffer (accessed by a read of Port 60H).

21-3F Read the keyboard controller's RAM (PS/2) - Bits D4-D0 specify the address.

60 Write the keyboard controller's Mode Register (PC/AT and PS/2) - The next byte of data written to the keyboard data port (Port 60H) is placed in the controller's mode register.

61-7F Write the keyboard controller's RAM (PS/2) - This command writes to the internal keyboard controller RAM with the address specified in bits D4-D0.

A4 Test Password Installed (PS/2 only) - This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and KIRQ is asserted (if the EKI bit is set). Test result - FAH means that the password is installed, and F1H means that it is not.

A5 Load Password (PS/2 only) - This command initiates the password load procedure. Following this command, the controller will take data from the input buffer port (Port 60H) until a 00H is detected or a full eight byte password including a delimiter (e.g. <cr>) is loaded into the password latches. Note: this means that during password validation, the password can be a maximum of seven bytes with a delimiter such as <cr>.

A6 Enable Password (PS/2 only) - This command enables the security feature. The command is valid only when a password pattern is written into the controller (see A5 command). No other commands will be "honored" until the security sequence is completed and command A6 is cleared.

A7 Disable Mouse (PS/2 only) - This command sets bit 5 of the Mode Register which disables the mouse by driving the –MCKOUT line high.

A8 Enable Mouse (PS/2 only) - This command resets bit 5 of the Mode Register, thus enabling the mouse again.

A9 Mouse Interface Test (PS/2 only) - This command causes the controller to test the mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Mouse Clock Line Stuck Low
02	Mouse Clock Line Stuck High
03	Mouse Data Line Stuck Low
04	Mouse Data Line Stuck High

AA Self Test Command (PC/AT and PS/2) - This commands the controller to perform internal diagnostic tests. A 55H is placed in the output buffer if no errors were detected. The OBF bit is set and KIRQ is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT and PS/ 2) - This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Keyboard Clock Line Stuck Low
02	Keyboard Clock Line Stuck High
03	Keyboard Data Line Stuck Low
04	Keyboard Data Line Stuck High

AC Diagnostic Dump (PC/AT only, Reserved on PS/2) - Sends 16 bytes of the controller's RAM, the current state of the input port, and current state of the output port to the system.

AD Keyboard Disable (PC/AT and PS/2) - This command sets bit 4 of the Mode Register to a "1". This disables the keyboard by driving the clock line (–KCKOUT) high. Data will not be received. The keyboard will be enabled after the system sends data to be transmitted to the keyboard.

AE Keyboard Enable (PC/AT and PS/2) - This command resets bit 4 of the mode byte to a "0". This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT and PS/2) - This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port low (PS/2 only) - P1 bits 0-3 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to Port 64H.

C2 Poll Input Port high (PS/2 only) - P1 bits 4-7 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to Port 64H.

D0 Read Output Port (PC/AT and PS/2) - This command causes the controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
0	P20	–RC	–RC
1	P21	A20 Gate	A20 Gate
2	P22	Speed Sel	–MDOUT
3	P23	Shadow Enable	–MCKOUT
4	P24	Output Buffer Full	KIRQ
5	P25		MIRQ
6	P26	–KCKOUT	–KCKOUT
7	P27	KDOUT	–KDOUT

Note: P22 (bit 2) is the speed control pin used by Award BIOS, and this is different from what is used by Phoenix and AMI. However, the use of this bit is transparent to the 82C042.

D1 Write Output Port (PC/AT and PS/2) - The next byte of data written to the keyboard data port (Port 60H) will be written to the controller's output port. The definitions of the bits are as defined above. In PC/AT mode, P26 and P27 will not be altered. In PS/2 mode, P22, P23, P26 and P27 cannot be altered.

D2 Write Keyboard Output Buffer (PS/2 only) - The next byte written to the data buffer (Port 60H) is written to the output buffer (60H) as if initiated by the keyboard [the OBF bit is set (1) and KIRQ will be set if the EKI bit is set (1)].

D3 Write Mouse Output Buffer (PS/2 only) - The next byte written to the data buffer (Port 60H) is written to the output buffer as if initiated by the mouse [the OBF bit is set (1) and MIRQ will be set if the EMI bit is set (1)].

D4 Write to Mouse (PS/2 only) - The next byte written to the data buffer (Port 60H) is transmitted to the mouse.

Note: If data is written to the data buffer (Port 60H) and the command preceding it did not expect data from Port 60H, the data will be transmitted to the keyboard.

E0 Read Test Inputs (PC/AT and PS/2) - This command causes the controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Keyboard Data	Keyboard Clock
1	Keyboard Clock	Mouse Clock
3-7	Read as 0's	Read as 0's

F0-FF Pulse Output Port (PC/AT and PS/2) - Bits 0-3 of the controller's output port may be pulsed low for approximately 6 µs. Bits 0-3 of the command specify which bit will be pulsed. A "0" indicates that the bit should be pulsed; a "1" indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port). In PS/2 mode, bits P22 and P23 are not pulsed.

IDE Bus Interface Control
Integrated Drive Electronics bus interface control signals are provided by the VL82C108 Combo chip. The timing and drive for these lines are consistent with the Conner Peripherals CP342 Integrated Hard Disk Manual.

A set of signals are used for this interface when the VL82C108 Combo chip is configured to support the IDE interface via IDE_EN, bit 5 of Control Register 1.

The Combo chip monitors bit 1 of the I/O address 03F6H and uses this bit to enable the interrupts received on IRQI when IDE_EN=1.

Input Signals:

IDINT — This signal indicates an interrupt request to the system from the IDE. It is used to generate IRQI.

Output Signals:

–CS3 — Chip Select 3. This signal is used as the floppy disk chip select. The default decode is 03F4H-03F5H. The IDE_EN control bit of Control Register 1 has no effect on this signal.

–CS4 — Chip Select 4. This signal is used as the –HOST CS0 of the IDE bus. The default decode is 01F0H-01F7H. The IDE_EN control bit of Control Register 1 has no effect on this signal.

–HCS1 — This signal is active (low) for address 03F6H-03F7H if IDE_EN=1 and is used as –HOST CS1 of the IDE bus.

–IDENH — This signal is used to drive the –OE pin of an external 74LS245 buffering bits 8-15 of the IDE data bus to the SD bus. It is active (low) when:

–CS4 is active AND SA2-SA0 = 000 AND IDE_EN=1.

–IDENL — This signal is used to drive the –OE pin of an external 74LS245 buffering bits 0-6 of the IDE data bus. It is active (low) when:

IDE_EN=1 AND –CS4 is active OR SA0-SA9 = 3F6H OR 3F7H.

This allows a simple implementation for an IDE bus that includes both the hard disk controller and the floppy disk controller.

IRQI — This is the three-state interrupt request to the CPU. It is normally tied directly to the IRQ14 signal of the system. When enabled it reflects the state of the IDINT input. It is enabled by writing bit 1 of I/O 3F6H with a zero (0) and setting IDE_EN=1. When disabled, it is three-stated.

–IOCS16 — This output signal is used to indicate to the system that the peripheral being accessed is a 16-bit device. It is set active (low) when the address of 1F0H is decoded and IDE_EN is set to a "1". This signal becomes active on the leading edge of ALE and inactive on the trailing edge of –IOW or –IOR.

Bidirectional Signals:

IDB7 — The control for the transceiver between IDB7 and SD7 is as follows:

IDB7 –> SD7 when:

–IOR is active AND (–CS4 is active OR SA0-SA9 = 3F6) is active AND IDE_EN=1.

SD7 is three-stated when:

–IOR is active AND IDE_EN=1 AND SA0-SA9=3F7H.

SD7 –> IDB7 at all other times when IDE_EN=1, three-stated (with internal pull-up) if IDE_EN=0.

Combo Chip Control Ports
Contained in the VL82C108 are two registers used for programming peripheral chip select base addresses and enabling options.

Default Chip Selects
The VL82C108 Combo chip also has several hard-wired default chip selects for the serial port, line printer port, floppy disk chip selects and hard disk chip select. The chip selects are:

Select/ Device	Address
COMA	3F8H-3FFH (Bit 3 of Port 102H) (Default) 2F8H-2FFH (Bit 3 of Port 102H =0)
LPT	03BCH-03BFH [Bit 5, 6 of Port 102H = 0, 0 (Default)] 0378H-037BH (Bit 5, 6 of Port 102H = 1, 0) 0278H-027BH (Bit 5, 6 of Port 102H = 0, 1)
–CS3	03F4H-03F5H
–CS4	01F0H-01F7H
–CS5	03F2H AND FDCS EN = 1
–CS6	03F7H AND FDCS EN = 1

Control Register 0 (I/O PORT 102H) Bits
This register contains bits that enable or disable functionality of the internal components of the Combo chip. The bits of this register are defined to be consistent with definitions used in the PS/2-50 family. This explains the unusual utilization of bits and control states.

The contents of the register are detailed below:

Bit	Usage	Value After Reset (–RES)
0	SYS BD EN	Enabled (1)
1	FDCS EN (CS3)	Enabled (1)
2	COMA EN (CS1)	Enabled (1)
3	COMA DEF	COM1 (1)
4	LPT EN (CS2)	Enabled (1)
5	LPT DEF 0	Parallel Port Add. (0)
6	LPT DEF 1	Parallel Port Add. (0)
7	–EMODE	Compat. Mode (1)

Bit 0 - System Board Enable (SYS BD EN) Control bit - When set (1), allows bits 1, 2, and 4 to enable and disable their respective devices. When reset (0), the floppy disk chip select (CS3), COMA (CS1), and the LPT port (CS2) are disabled regardless of the contents of bits 1, 2, and 4.

Bit 1 - Floppy Disk CS Enable (FDCS EN) Control bit - When set (1), allows the FD CS signal (CS3, CS4 and CS5) to be asserted to an external floppy disk controller chip. When reset (0), prevents the assertion of this chip select.

Bit 2 - Communications Port Enable (COMA EN) Control bit - When set (1), allows the internal COMA (CS1) port to be accessed. When reset (0), COMA is disabled.

Bit 3 - Communications Port Default Address (COMA DEF) Control bit when set (1), forces the hard-wired default base address to COMA to correspond to (3F8H-3FBH). Reset (0) forces the COMA hard-wired address to (2F8H-2FBH).

Bit 4 - Line Printer Port Enable (LPT EN) Control bit, when set (1) enables the LPT port (CS2). Reset (0) disables the LPT port.

Bit 5 & 6 - Line Printer Default bits 0 and 1 (LPT DEF 0 and 1) Control bits, set the Line Printer Base hard-wired address defaults as shown below:

Bit 6	Bit 5	Address Range
0	0	03BCH-03BFH
0	1	0378H-037BH
1	0	0278H-027BH
1	1	Reserved

Setting bit 3 of I/O Port 102H changes the base address to that set in the program address registers for LPT (CS3).

Bit 7 - Line Printer Extended Mode (LPT –EMODE) Control bit - When set (1), disables the Extended Mode and forces PC/AT compatibility. When reset (0), the Extended Mode is enabled allowing the printer port direction to be controlled and the interrupt status to be latched.

Bit	Usage	Value After Reset
0	POWERDOWN	Disabled (0)
1	AT/PS2_KBD	AT (1)
2	PRIV_EN	Enabled (1)
3	KB_RST	Enabled (0)
4	HDCS_EN	Enabled (1)
5	IDE_EN	Enabled (1)
6	MISCOUT1	PS/2 Mode Only (1)
7	MISCOUT2	PS/2 Mode Only (1)

Control Register 1 (I/O Port 103H) Bits

This register is used to control peripheral chip selects that are not included in Control Register 0. The bits in this register are defined as follows:

Bit 0 - Power Down Enable. A "1" will stop the oscillator until this bit either resets (0), or a falling edge occurs on the –WAKEUP input pin.

Bit 1 - AT or PS/2-Compatible Keyboard. A "1" selects PC/AT type keyboard controller functions, while a "0" places the keyboard controller in PS/2 mode.

Bit 2 - Private Controls Enable. When in AT mode (AT/PS2_KBD = 1), this bit is used to latch the values of the keyboard controller's output signals KHSE, KSRE, and IRQM to the VL82C108 output pins. When "1", these outputs follow the keyboard controller's outputs. When "0", these outputs are held at that value regardless of the keyboard controller's outputs.

When in PS/2 mode (AT/PS2_KBD = 0), this bit has no effect on the KHSE, KSRE, and IRQM output pins. The Combo chip outputs follow the keyboard controller's outputs.

Bit 3 - KB_RST. This bit is used to reset the keyboard controller. Setting this bit places the keyboard controller into a reset mode which is identical to the mode during power-on reset. Clearing this bit enables the keyboard controller.

Bit 4 - Hard Disk Chip Select Enable. A "1" enables the Hard Disk Chip Select signal (–CS4), while a "0" disables the chip select.

Bit 5 - Integrated Drive Electronics Enable. A "1" enables the IDE functions of outputs –IDENH, –IDENL, IRQI, –IOCS16, and IDB7 as described in IDE Bus Interface Control section.

Bit 6 - Miscellaneous Output 1. This bit is directed to pin 79 (KI0) when the AT/PS2_KBD (bit 2) of this register is set to a "0" (PS/2 mode). Setting MISCOUT1 to a "1" while in the PS/2 mode, will cause pin 79 to be set high. Setting this bit to a "0" will cause pin 79 to be set to a low level. When the AT/PS2_KBD bit is set to a "1" (AT mode), setting MISCOUT1 to a "1" or a "0" has no effect.

Bit 7 - Miscellaneous Output 2. This bit is directed to pin 78 (KI1) when the AT/PS2_KBD (bit 1) of this register is set to a "0" (PS/2 mode). Setting MISCOUT2 to a "1" while in the PS/2 mode, will cause pin 78 to be set to a low level. When the AT/PS2_KBD bit is set to a "1" (AT mode), setting MISCOUT2 to a "1" or a "0" has no effect.

Miscellaneous Control Signals

–XDRDIN This input signal is active (low) when data is transferred from the XD bus to the SD bus, i.e., interrupt acknowledge cycles and I/O read accesses to addresses 000H-0FFH.

–XDRDOUT This output signal is to control the direction pin of a transceiver between the XD bus and the SD bus. This signal is set inactive

(high) when the Combo's keyboard controller chip select is active or when the –XDRDIN input is high.

–WAKEUP This input is used to turn the on-chip oscillator on after it has been shut down under software control. A high to low transition on this input restarts the oscillator. This pin may be tied to the keyboard clock line for automatic wakeup on any keystroke.

XTAL1 This pin is the input to the on-board 18.432 MHz crystal oscillator. This pin may also be driven by an external CMOS clock signal at 18.432 MHz.

XTAL2 This pin is the output pin of the internal crystal oscillator and should be left open and unloaded if an external clock signal is applied to the XTAL1 pin. This pin is capable of driving one CMOS external load other than the crystal.

–TRI This pin is used for in-circuit testing. When low, all outputs and I/O pins are placed in the high impedance state.

–ICT This pin, when strobed low, places the VL82C108 into test mode determined by the data on the SD0 through SD3 pins. The chip will remain in this mode until RES is asserted. Test mode may be changed by strobing this pin low again with different data on the SD0-SD3 pins.

Test Modes

Test modes are to be defined by design. They should include boundary scan or I/O mapping for in-circuit test mode and allow the muxing of the megacells and other circuit logic to package pins.

SD3	SD2	SD1	SD0	Test Mode
0	1	0	1	COMA
0	1	0	0	Reserved
1	1	0	0	LPT
1	0	1	0	Keyboard Controller
0	1	1	1	Chip Select Logic
0	0	1	1	Bypass Dividers on Clocks
0	1	1	0	ICT Mux

COMBO ICT MUX CONNECTIONS

Output Pins		to Input Pins	
Name	Number	Name	Number
PD0	49	PE	58
PD1	48	BUSY	57
PD2	47	SLCT	56
PD3	46	–ERR	55
PD4	44	–CTS	64
PD5	43	SA9	27
PD6	42	SA4	22
PD7	41	SA3	21
SD0	94	KI0	79
SD1	93	KI1	78
SD2	90	KI2	77
SD3	89	KI3	76
SD4	88	KI5	75
SD5	87	KRSEL	74
SD6	85	KKSW	73
SD7	84	IDB7	97
–STB	51	–ACK	59
KCLK	82	–DSR	63
SOUT	39	–DSR	63
KSRE	80	–ERR	55
–CS3	9	–IOR	13
–CS4	10	–IOW	14
–RTS	37	–RI	61
KA20	71	–RI	61
–DTR	38	–DCD	62
–SLIN	54	–WAKEUP	36
–IOCS16	95	–XDRDIN	98
–CS5	11	AEN	15
–CS6	12	ALE	16
–HCS1	1	BUSY	57
IRQ1	28	IDINT	99
KDAT	83	KCM	72
–IDENL	7	KI2	77
–IDENH	6	KI3	76
–INIT	53	KI5	75
–XDRDOUT	8	SA0	18
IRQK	29	SA1	19
IRQM	30	SA2	20
IRQC	32	SA5	23
IRQP	33	SA6	24
–IRQE	34	SA7	25
–OUT2	35	SA9	26
–AFD	52	SIN	60
KRES	70	SIN	60
KHSE	81	SLCT	56
XTAL2	68	XTAL1	67

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write Figures 8, 9					
tSU1	Address Setup Time	55		ns	
tH2	Address Hold Time	20		ns	
tSU3	AEN Setup Time	55		ns	
tH4	AEN Hold Time	20		ns	
t5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL=200 pF
tH9	Read Data Hold	5	60	ns	CL=50 pF
Chip Select Timing Figures 10, 11					
tD11	Chip Select Delay from Address		35	ns	CL=50 pF
tD12	–CS5, –CS6 Delay from –IOW		30	ns	CL=50 pF
tD13	–IOCS16 Active from Address		60	ns	CL=200 pF
–IOCS16 Timing Figure 11					
tD17	–IOCS16 Inactive from Command		55	ns	CL=200 pF
t21	ALE Pulse Width High	40		ns	
IDE Interface Timing Figure 12					
tD18	IRQI Delay from IDINT		40	ns	CL=100 pF
tD19	–IDENH/–IDENL Delay from Address		60	ns	CL=50 pF
tD20	IDB7 Delay from SD7 Input		40	ns	CL=200 pF
tD21	SD7 Delay from IDB7 Input		40	ns	CL=200 pF
tD23	SD7 Delay from –IOR During IDE Access	0	85	ns	CL=200 pF
tH24	SD7 Hold from –IOR Inactive	5	60	ns	CL=50 pF
tD25	IDB7 Delay from –IOR Inactive	0	85	ns	CL=200 pF
tH26	IDB7 Hold from –IOR Active	5	60	ns	CL=50 pF
XDATA Control Timing Figure 13					
tD27	–XDRDOUT Delay from –XDRDIN		30	ns	CL=50 pF
tD28	–XDRDOUT Delay from –IOR		30	ns	CL=50 pF

Note: –IOCS16 is an open-drain output with an active pull-up for approximately 10 ns. These parameters are measured at VOH = 1.5 V with a 300 ohm pull-up. Actual performance will vary depending on system configuration.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
SERIAL PRINTER					
Transmitter Figure 15					
tHR1	Delay from Rising Edge of –IOW (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from THRE Reset to Transmit Start		16	CLK Cycles	Note1
tSI	Delay from Write to THRE	8	24	CLK Cycles	Note 1
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 1
tIR	Delay from –IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control Figure 16					
tMDO	Delay from –IOW (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –IOR (RS MSR)		250	ns	100 pF Load
Receiver Figure 14					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 1
tRINT	Delay from –IOR (RD RBR/RDLSR) to Reset Interrupt		1	µs	100 pF Load
Parallel Port Figure 17					
tDT	Data Time	1		µs	Software Controller
tSB	Strobe Time	1	500	µs	Software Controller
tAD	Acknowledge Delay (Busy Start to Acknowledge)			µs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			µs	Defined by Printer
tAK	Acknowledge Duration Time			µs	Defined by Printer
tBSY	Busy Duration Time			µs	Defined by Printer
tBSD	Busy Delay Time			µs	Defined by Printer

Note: 1. CLK cycle refers to external 18.432 MHz clock divided by 10, e.g. 1.8432 MHz.

FIGURE 8. BUS INTERFACE TIMING WRITE CYCLE

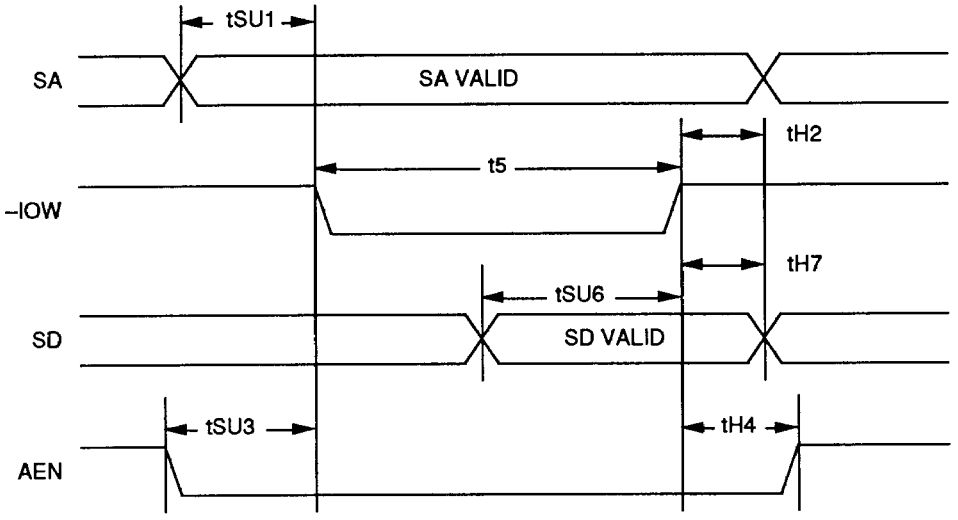


FIGURE 9. BUS INTERFACE TIMING READ CYCLE

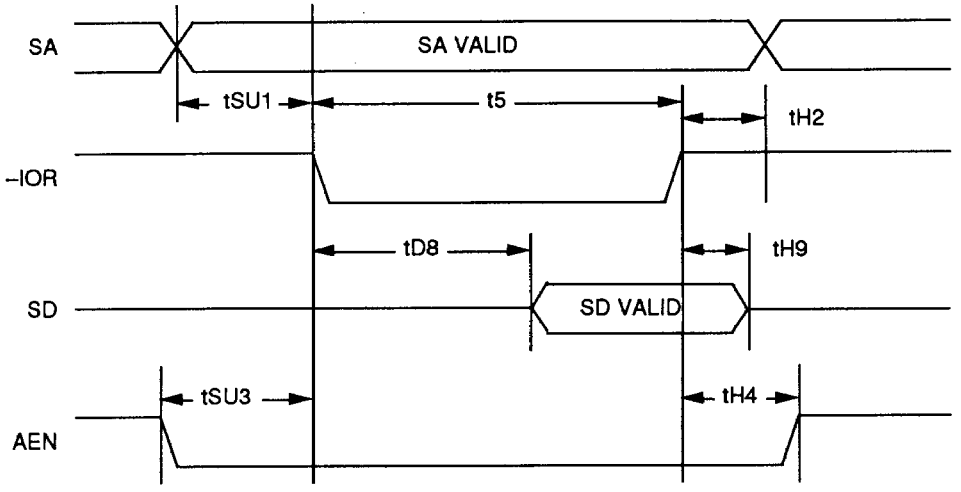


FIGURE 10. CHIP SELECT TIMING

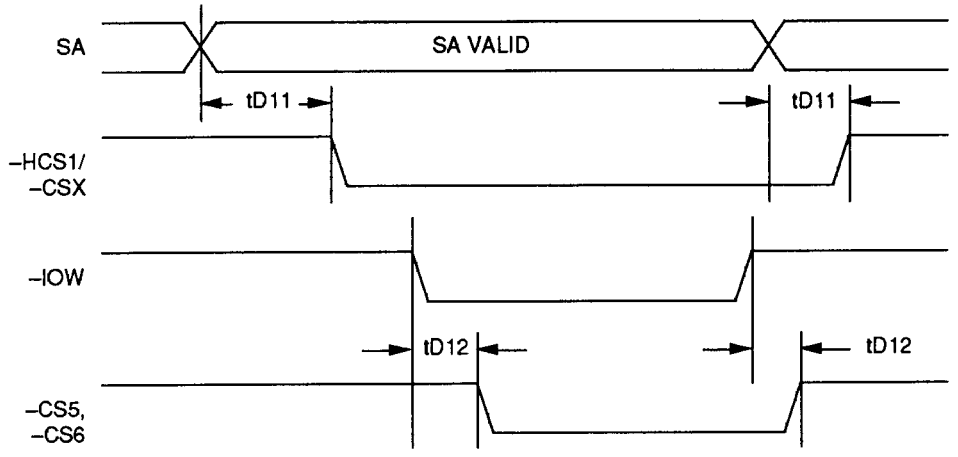


FIGURE 11. IOCS16 TIMING

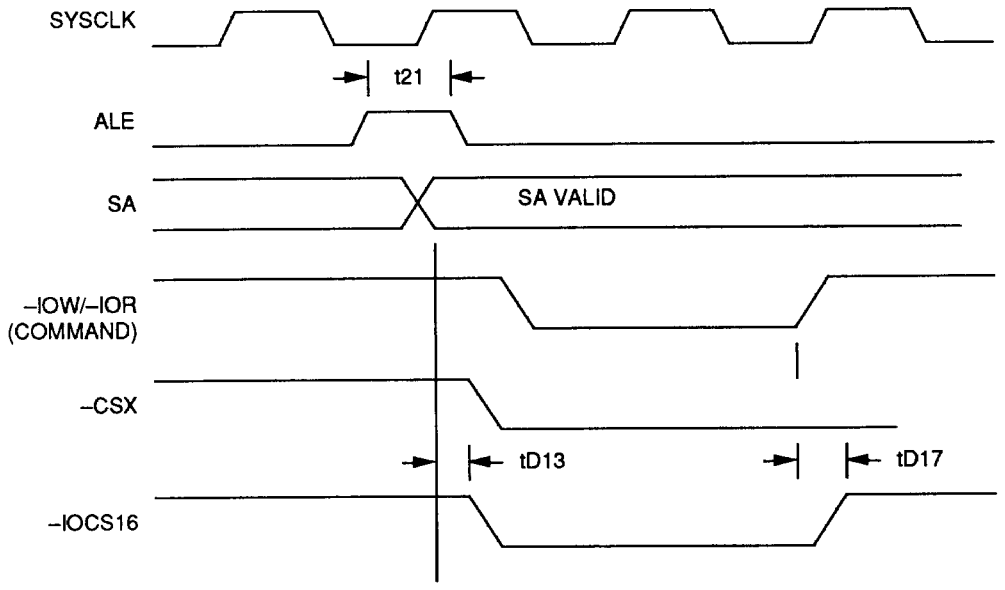


FIGURE 12. IDE INTERRFACE TIMING

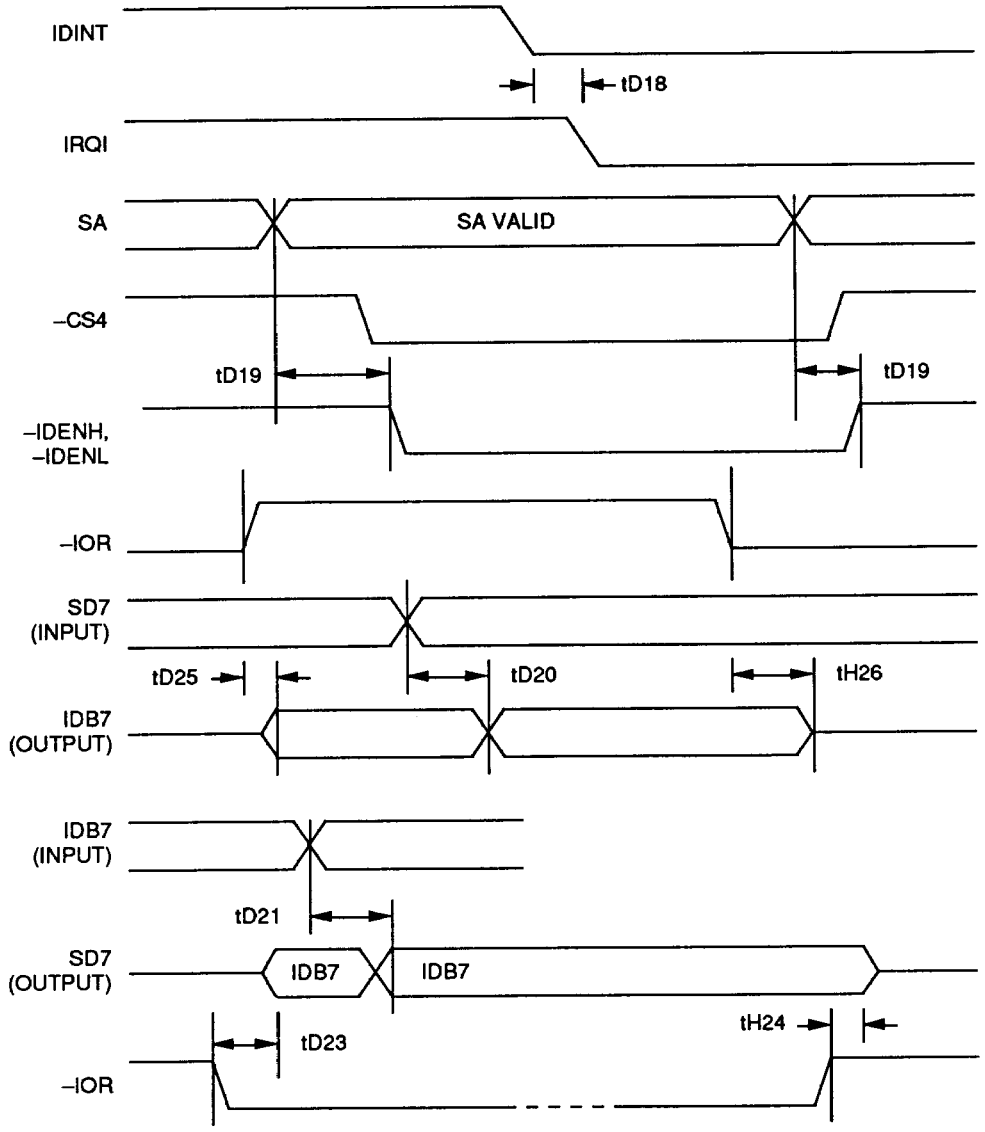


FIGURE 13. XDATA CONTROL TIMING

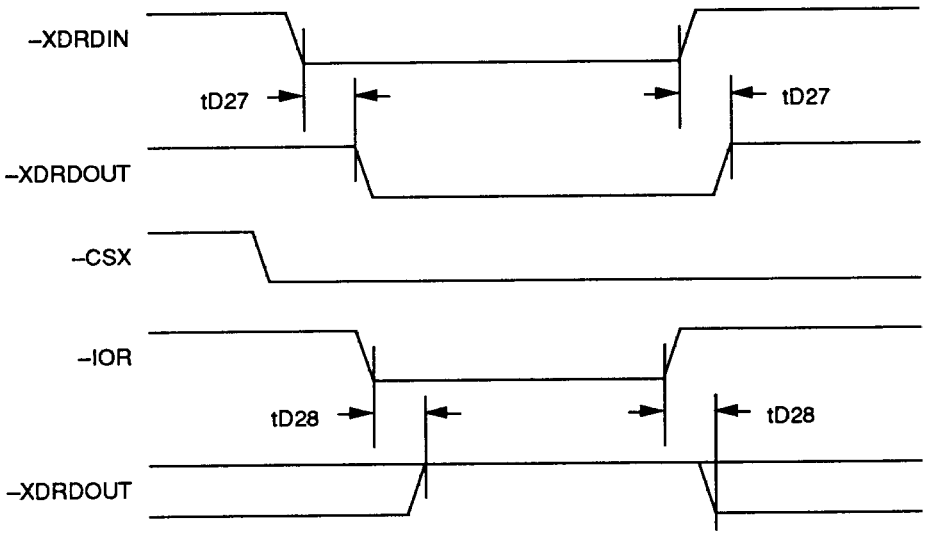


FIGURE 14. RECEIVER TIMING

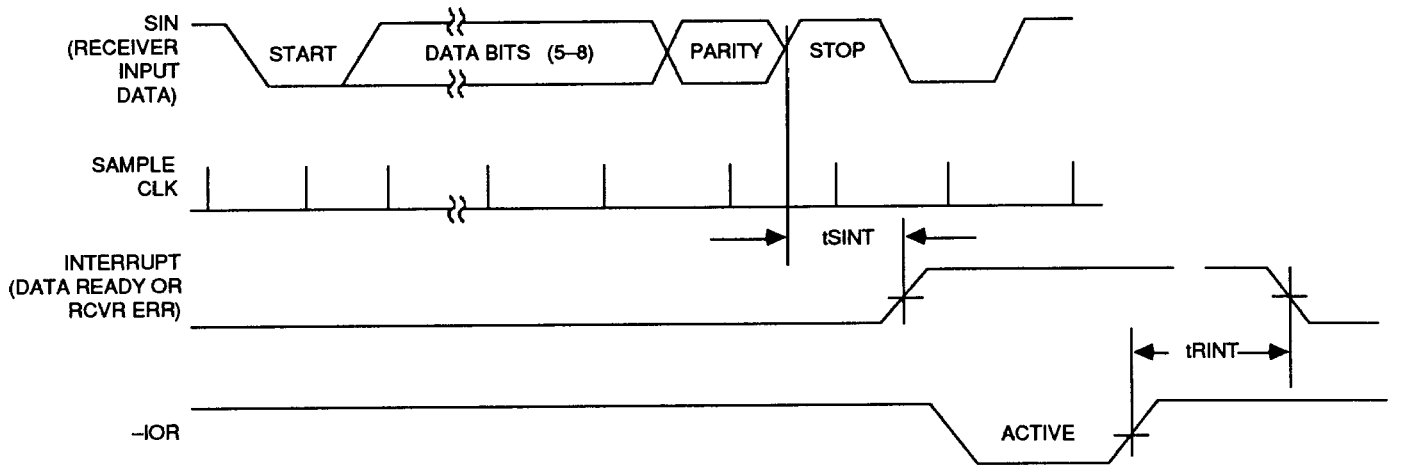


FIGURE 15. TRANSMITTER TIMING

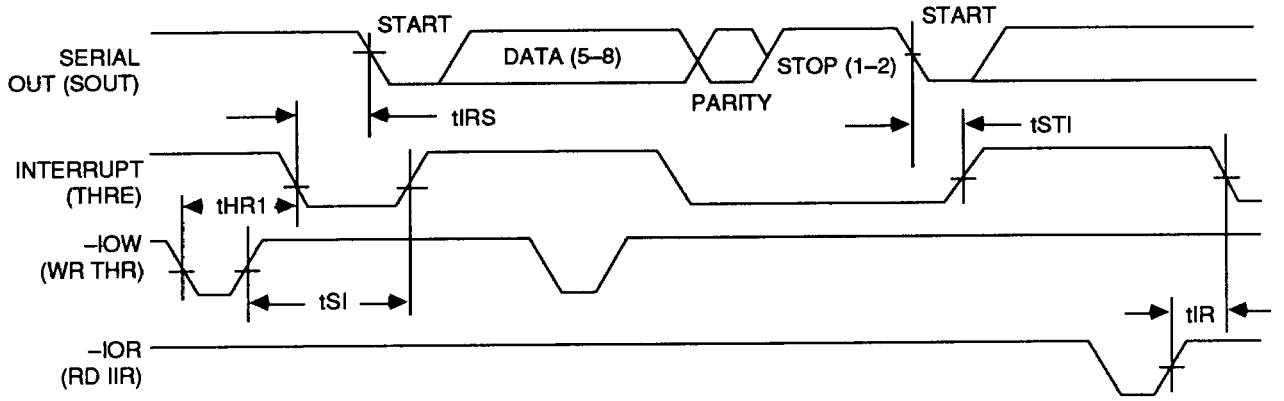


FIGURE 16. MODEM TIMING

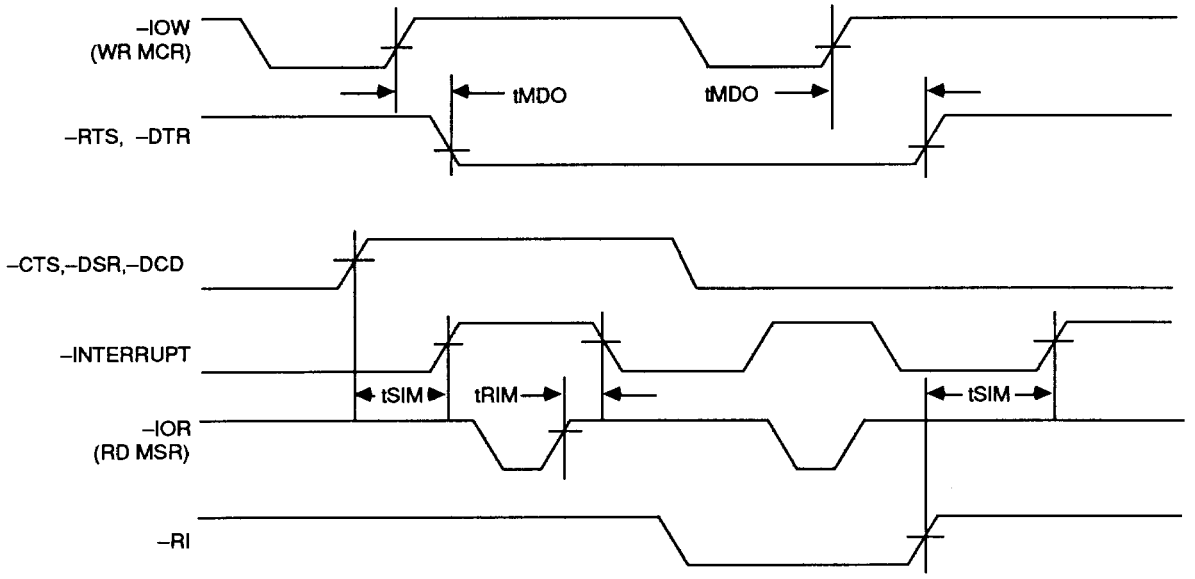


FIGURE 17. PARALLEL PORT TIMING

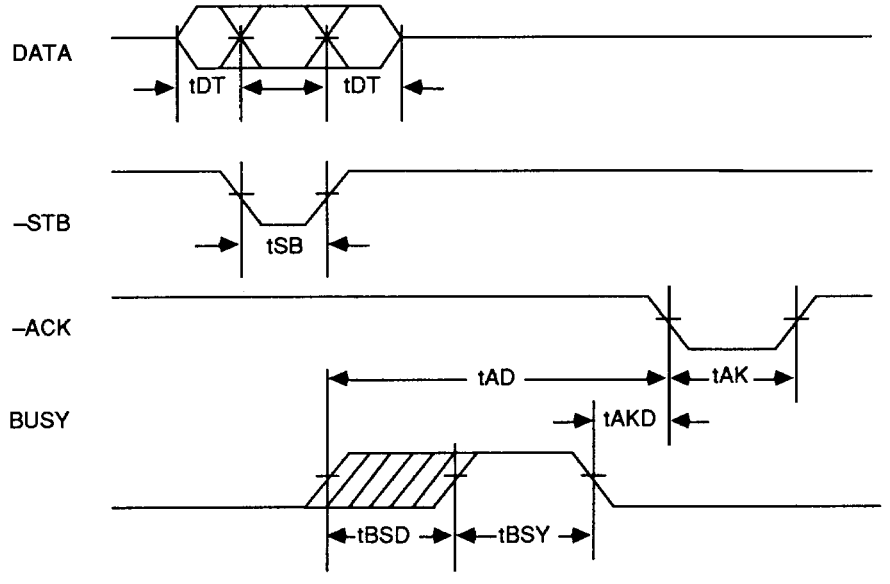
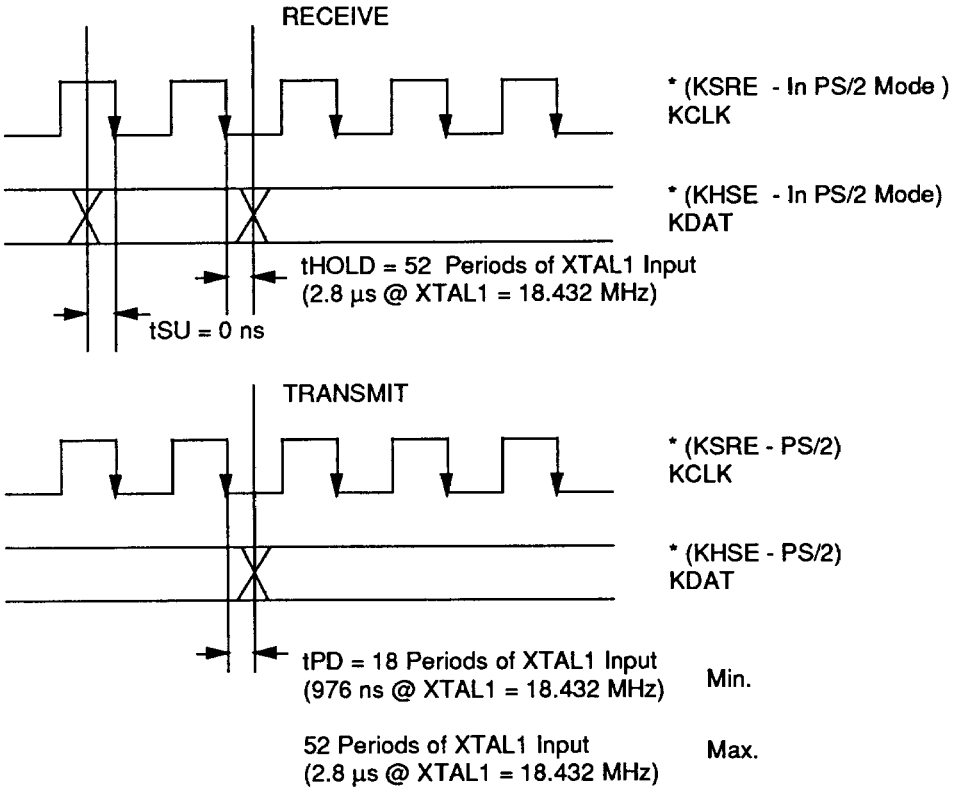
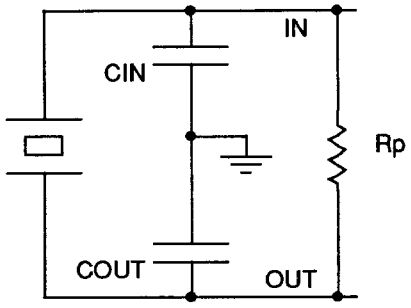


FIGURE 18. KEYBOARD CONTROLLER INTERFACE TIMING



*** Note:** Specifications are identical for KHSE with respect to KSRE in PS/2 Mode.

FIGURE 19. CRYSTAL OSCILLATOR CONFIGURATIONS



18.432 MHz

CIN = 10 pF
CCOUT = 30 pF
Rp = 10 MΩ

RECOMMENDED CRYSTAL PARAMETERS

Rs ≤ 50 Ω
Co ≤ 7 pF
Ci ≤ 20 pF
Parallel Resonance

ABSOLUTE MAXIMUM RATING

Ambient Temperature	–10°C to +70°C
Storage Temperature	–65°C to 150°C
Supply Voltage to Ground Potential	–0.5 V to VDD +0.3 V
Applied Output Voltage	–0.5 V to VDD +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

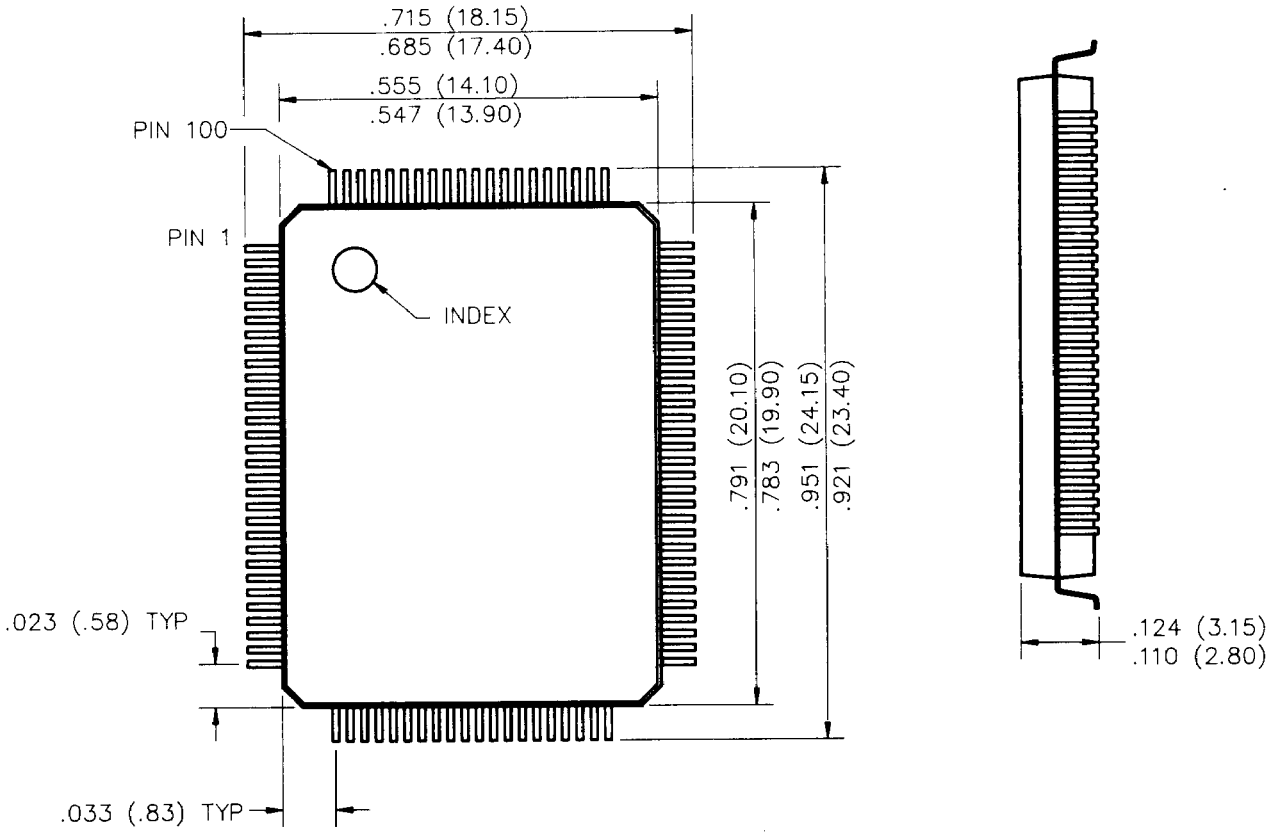
DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

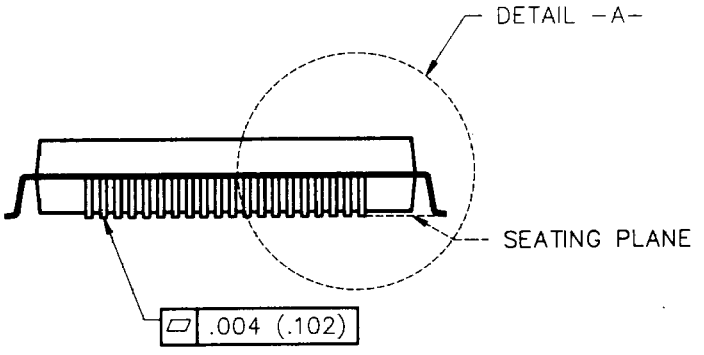
Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage				
	Input Types (All except I2)	–0.5	0.8	V	
	Input Type I2	–0.5	VDD* 0.2	V	
VIH	Input High Voltage				
	Input Types I1, I3, I4, IO2, IO4, IO5, IO6	2.0	VDD+0.5	V	
	Input Type I2	VDD* 0.7	VDD+0.5	V	
	Input Type I5	2.4	VDD+0.5	V	
VOL	Output Low Voltage				
	Output Type 01		0.4	V	IOL = 2.0 mA
	Output Type 06		0.4	V	IOL = 4.0 mA
	Output Type 04, I04, I05		0.4	V	IOL = 12.0 mA
	Output Type 02, 07, 08, IO2, I06		0.4	V	IOL = 24.0 mA
VOH	Output High Voltage				
	Output Type 01,06	2.4		V	IOH = –0.8 mA
	Output Type I05	2.4		V	IOH = –2.0 mA
	Output Type 02, I02, I06	2.4		V	IOH = –2.4 mA
IIH	Input High Current				
	Input Types I1, I3, I4, I5		10	µA	VIN = VDD
IIL	Input Low Current				
	Input Types I1, I5	–10		µA	VIN = VSS + 0.2
	Input Types I4, IO6	–500	–50	µA	VIN = 0.8 V All other pins floating.
ILOL	Three-State Leakage Current				
	I/O Output Types 06, 07,	–50		µA	VSS + 0.2
	I02, I04, I05		50	µA	VDD
IODL	Open-Drain Off Current				
	I/O Output Type 04	–5.0	–1.0	mA	V = 0.8 V
CO	Output Capacitance		8	pF	
CI	Input		8	pF	
CIO	Input/Output Capacitance		16	pF	
IDD	Operating Supply Current		40	mA	

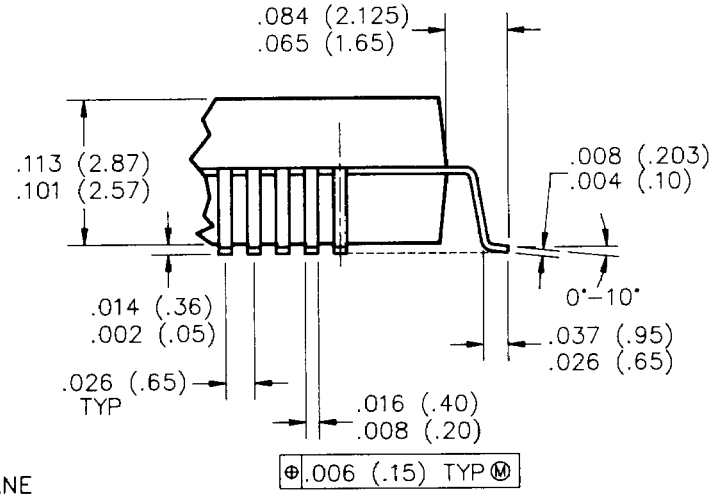
Note: For pin types, refer to the Legend and Pin Descriptions on pages 4-7 of this data sheet.

PACKAGE OUTLINE

100-LEAD PLASTIC QUAD FLAT PACK







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