VL82C106

PC/AT® COMBINATION I/O CHIP

FEATURES

- Combines the following PC/AT peripheral chips:
  VL16C450B UART - COM 1:
  VL16C450B UART - COM 2:
  Parallel printer port - LPT 1:
  Keyboard/mouse ctrl. - KBD
  Real-time clock - RTC
- Serial ports 100% 16C450B-compatible
- Bidirectional Line Printer Port (LPT)
- Software control of PS/2®-compatible enhancements (mouse)
- CMOS direct drive of Centronics-type parallel interface
- PC/AT- or PS/2-compatible keyboard and mouse controller
- 146818A-compatible real-time clock (RTC)
- 16 bytes of additional standby RAM (66 bytes total)
- IDE bus control signals included (two external 74LS245 and one 74ALS244, or equivalent, buffers are required)
- Seven battery-backed programmable chip select registers for auto configuration
- Preprogrammed default chip select registers
- Programmable wait state generation
- 5 µA standby current for RTC, RAM, and chip select registers
- Single 128-lead plastic quad flatpack

DESCRIPTION

The VL82C106 Combination chip replaces with a single 128-lead chip, several of the commonly used peripherals found in PC/AT-compatible computers. This chip when used with the VLSI PC/AT-compatible chip set allows designers to implement a very cost-effective, minimum chip count motherboard containing functions that are common to virtually all PCs.

The on-chip UARTs are completely software compatible with the VL16C450B ACE.

The bidirectional parallel port provides an AT and PS/2 software compatible interface between a Centronics-type printer and the VL82C106. Direct drive is provided so that all that is necessary to interface to the line printer port is a resistor - capacitor network. The bidirectional feature (option) is software programmable for backwards PC/AT-compatibility.

The keyboard/mouse controller is selectable as PC/AT- or PS/2-compatible.

The real-time clock is 146818A-compatible and offers a standby current drain of 5 µA at 3.0 V. Minimum battery voltage is 2.4 V.

Included is the control logic necessary for the support of the Integrated Drive Electronics (IDE) hard disk bus interface.

The Combination I/O chip also includes seven programmable chip selects, three internal and four external. Each chip select has a programmable 16-bit base address and a mask register that allows the number of bytes corresponding to each chip select to be programmed (e.g. 3F8H-3FFH has a base address of 3F8H and a range of 8 bytes). Each chip select can be programmed for number of wait states (0-7) and 8- or 16-bit operation. 16-bit decoding is used for all I/O addresses. A default fixed decode is provided on reset for the on-chip serial ports, printer port, and off-chip floppy and hard disk controllers, which may be changed to battery-backed programmable chip selects via a control bit.

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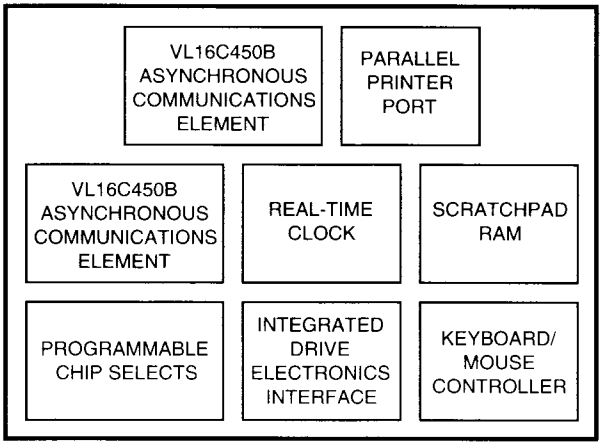
ORDER INFORMATION

Part Number	Package
VL82C106-FC	Plastic Quad Flatpack

Note: Operating temperature range is 0°C to +70°C.

INTERNAL FUNCTIONAL DIAGRAM



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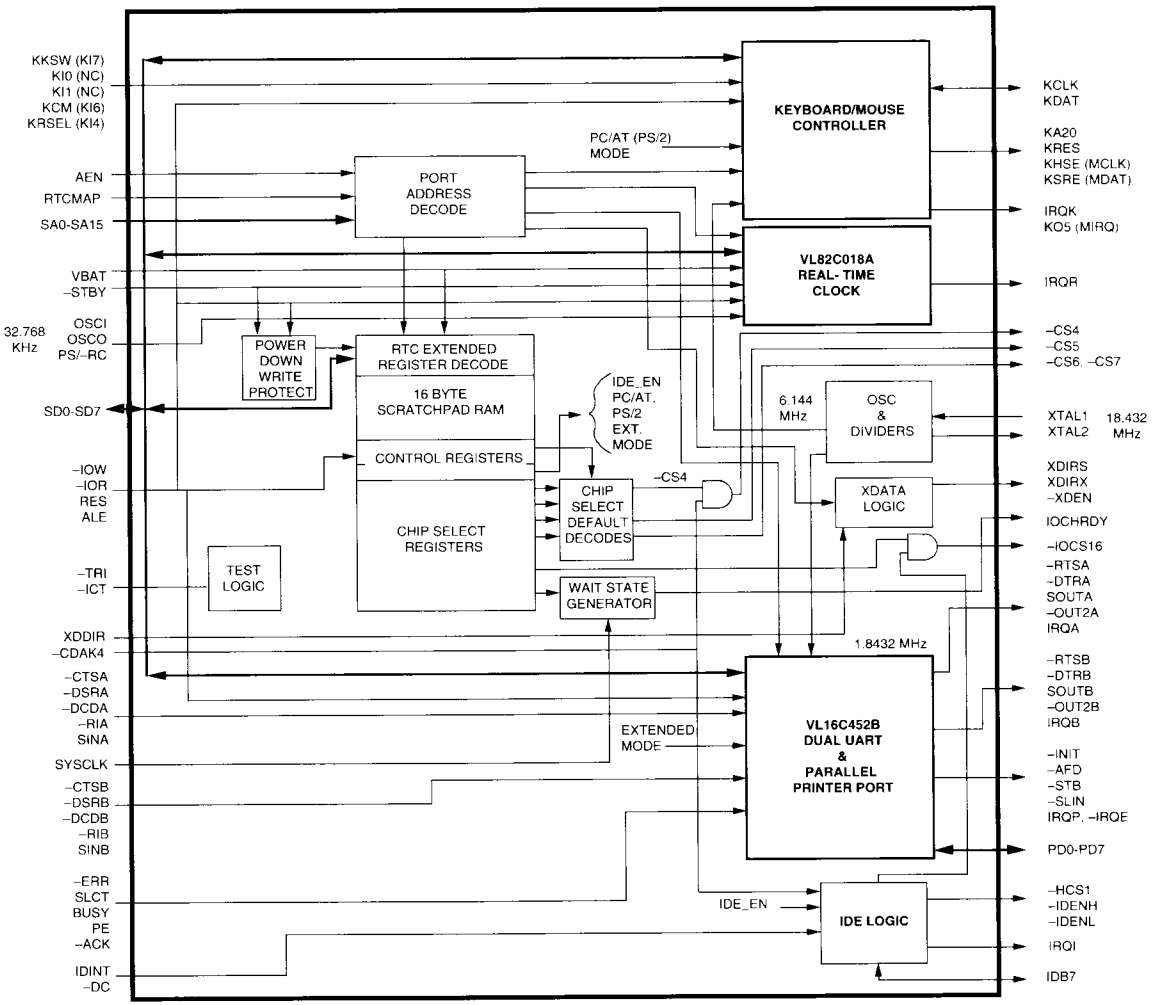
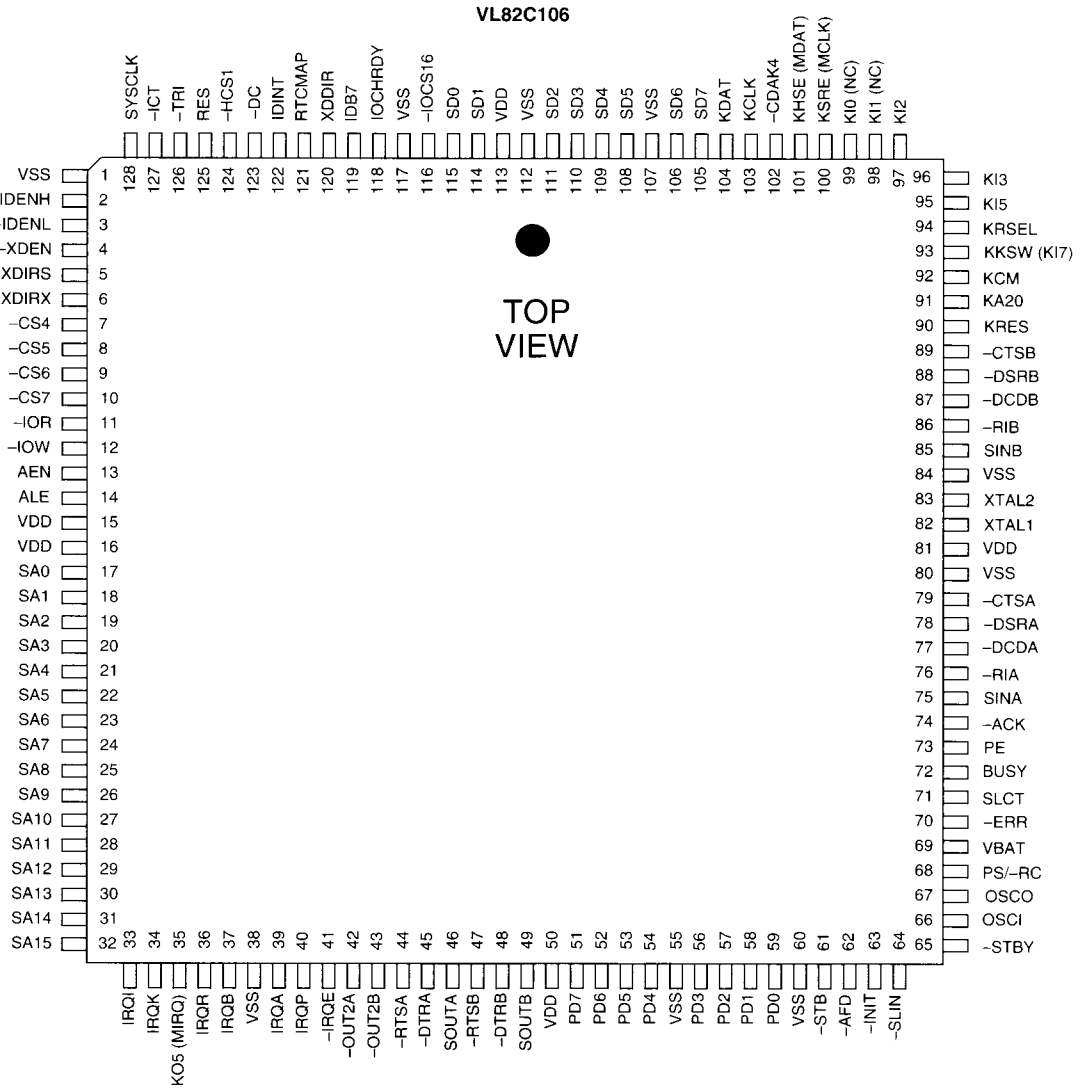
BLOCK DIAGRAM



Note: Items in parentheses () are signal names when the Keyboard Controller is in PS/2 mode.

PIN DIAGRAM



Note: Items in parentheses () are signal names when the Keyboard Controller is in PS/2 mode.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
COMMUNICATIONS PORT A			
–RTSA	44	O1	Request to Send, Port A
–DTRA	45	O1	Data Terminal Ready, Port A
SOUTA	46	O1	Serial Data Output, Port A
–CTSA	79	I4	Clear to Send, Port A
–DSRA	78	I4	Data Set Ready, Port A
–DCDA	77	I4	Data Carrier Detect, Port A
–RIA	76	I4	Ring Indicator, Port A
SINA	75	I4	Serial Input, Port A
IRQA	39	O6	Interrupt Request, Port A
–OUT2A	42	O1	Output 2, Port A
COMMUNICATIONS PORT B			
–RTSB	47	O1	Request to Send, Port B
–DTRB	48	O1	Data Terminal Ready, Port B
SOUTB	49	O1	Serial Data Output, Port B
–CTSB	89	I4	Clear to Send, Port B
–DSRB	88	I4	Data Set Ready, Port B
–DCDB	87	I4	Data Carrier Detect, Port B
–RIB	86	I4	Ring Indicator, Port B
SINB	85	I4	Serial Input, Port B
IRQB	37	O6	Interrupt Request, Port B
–OUT2B	43	O1	Output 2, Port B
PARALLEL PRINTER PORT			
PD0	59	IO5	Printer Data Port, Bit 0
PD1	58	IO5	Printer Data Port, Bit 1
PD2	57	IO5	Printer Data Port, Bit 2
PD3	56	IO5	Printer Data Port, Bit 3
PD4	54	IO5	Printer Data Port, Bit 4
PD5	53	IO5	Printer Data Port, Bit 5
PD6	52	IO5	Printer Data Port, Bit 6
PD7	51	IO5	Printer Data Port, Bit 7
–INIT	63	O4	Initialize Printer Signal
–AFD	62	O4	Autofeed Printer Signal
–STB	61	O4	Data Strobe to Printer
–SLIN	64	O4	Select Signal to Printer
–ERR	70	I4	Error Signal from Printer
SLCT	71	I4	Select Signal from Printer
BUSY	72	I4	Busy Signal from Printer

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
PE	73	I4	Paper Error Signal from Printer
–ACK	74	I4	Acknowledge Signal from Printer
IRQP	40	O6	Printer Interrupt Request - Asserted following the –ACK signal from the printer. PIRQ is internally connected to –ACK and PIRQ will go high in the rising edge of the –ACK signal. This signal is enabled/three-stated by setting the Interrupt Enable Bit (bit 4) in the Printer Control Register. This signal is suitable for directly driving the interrupt on the slot bus of the PC/AT. The PIRQ handling is controlled by RTC Control Register 1, (index 6Ah) bit 1, "AT/PS2". When AT/PS2 is set to 1, the PIRQ is internally connected to –ACK, this causes a pulsed PIRQ typically used in AT slot bus designs. When AT/PS2 is set to 0, the PIRQ is latched high on the rising edge of –ACK and held in the active state until the Printer Status Register is read creating a PS/2 style interrupt.
–IRQE	41	O1	Printer Interrupt Request Enabled
REAL-TIME CLOCK PORT			
VBAT	69	NA	Standby Power - Normally 2.4 V to 5.0 V, battery-backed.
–STBY	65	I5	Power Down Control
OSCI	66	NA	Crystal Connection Input - 32 KHz
OSCO	67	NA	Crystal Connection Output - 32 KHz
PS/–RC	68	I5	Power Sense /RAM Clear
IRQR	36	O1	Real-Time Clock Interrupt Request
RTCMAP	121	I4	Real-Time Clock Map - When high, the RTC input signal is mapped to 70H and 71H, when low, it is mapped to 170H and 171H. This signal requires a 30k ohm pull-up resistor.
KEYBOARD CONTROLLER PORT			
KCLK	103	IO4	Keyboard Clock (Keyboard Controller output port P2, bit 6) - An I/O signal that is internally inverted and fed back into the Keyboard Controller input TEST0 pin, such that it is capable of direct connection to the keyboard clock signal. This open drain signal requires an external pull-up resistor and bypass capacitor. This pin does not change function with AT/PS2 Mode setting.
KDAT	104	IO4	Keyboard Data (Keyboard Controller output port P2, bit 7) - This signal is capable of direct connection to the keyboard connector. It is an open drain signal that requires an external pull-up resistor and a 47 pF bypass capacitor. In PC/AT Mode, the VL82C106 internally inverts and routes bit 7 of port P2 to the Keyboard Controller's TEST1 input. In PS/2 Mode, this signal is internally inverted and routed to the Keyboard Controller's bit 0 of port P1 input for feedback. Thus, this same signal is used in both AT and PS/2 Mode.
KCM	92	I4	Color/Monochrome (Keyboard Controller input port P1 bit 6) - A general purpose input that is normally a color/monochrome jumper indicator. This pin does not change function when in AT/PS2 Mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
KKSW (KI7)	93	I4	KKSW - Keyboard Keyswitch (Keyboard Controller input port P1 bit 7) - When in AT Mode, this pin serves as the keyboard keyswitch input to the Keyboard Controller. When KKWS is active (low) and the mode register bit for INHIBIT (via the Keyboard Controller Mode Register) is enabled, it will cause the controller to discard incoming keyboard character scan codes. When KKSW is inactive (high) or when the INHIBIT is disabled, incoming keyboard character scan codes are passed through to the system. (KI7) - General Purpose Input - In PS/2 Mode, this input's value is reflected in the Keyboard Controller Status Register. Changes in the value of KI7 do not affect incoming SCAN codes in PS/2 mode.
KA20	91	O1	A20 Gate - (Keyboard Controller output port P2, bit 1) A general purpose output, normally A20 Gate. This pin does not change function with AT/PS2 Mode setting.
KRES	90	O1	CPU Reset (Keyboard Controller output port P2, bit 0) - A general purpose output, normally CPU Reset. This pin does not change function with AT/ PS2 Mode setting.
KHSE (MDAT)	101	O1 (IO4)	Speed Select (Keyboard Controller output port P2, bit 2) - When in PC/AT Mode, this pin serves as a general purpose output, normally speed select "TURBO" output. (Mouse Data) - In PS/2 Mode, this pin is the mouse data I/O signal capable of direct connection to the PS/2 style mouse data signal. It is an open drain signal that requires an external pull-up resistor and a bypass capacitor. It is internally inverted and connected to the P1[1] input port therefore, P1[1] is reserved and unusable via KI0 (Pin 99).
KSRE (MCLK)	100	O1 (IO4)	Shadow RAM Enable (Keyboard Controller output port P2, bit 3) In PC/AT mode, this pin serves as a general purpose output, normally shadow RAM enable. (Mouse Clock) - In PS/2 mode, this pin is the mouse clock I/O signal capable of direct connection to the PS/2 style mouse clock signal. MCLK is internally fed back into the controller Test 1 input. It is an open drain signal that requires an external pull-up resistor and a bypass capacitor.
IRQK	34	O1	Keyboard Interrupt Request (Keyboard Controller output port P2, bit 4) - This signal is enabled by a bit in the Keyboard Controller Mode Register. It does not change function with AT/PS2 Mode setting.
KO5 (MIRQ)	35	O1	General Purpose Output, Bit 5 (Keyboard Controller output port P2, bit 5) - In PC/AT Mode, this pin is a general purpose output signal from the Keyboard Controller. (Mouse Interrupt Request) - In PS/2 Mode, this pin is the the mouse interrupt signal. It is normally connected to the ISA bus signal IRQ12. It is enabled via the Keyboard Controller Mode Register.
KRSEL (KI4)	94	I4	RAM Select (Keyboard Controller input port P1, bit 4) - A general purpose input, normally RAM Select. This pin does not change function with AT/ PS2 Mode setting.
KI0 (NC)	99	I4 (NC)	(General Purpose Input, Bit 0) (Keyboard Controller input port P1, bit 0) - In PC/AT Mode, this pin is a general purpose input signal. (No Connect) - In PS/2 Mode, this pin is a a "no connect" because bit 0 of input port P1 is internally routed as the KDAT input for keyboard communication feedback.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
KI1 (NC)	98	I4 (NC)	General Purpose Input, Bit 1 (Keyboard Controller input port P1, bit 1) - In PC/AT Mode, this pin is a general purpose input signal. (No Connect) - In PS/2 Mode, this pin is a "no connect" because bit 1 of input port P1 is internally routed as the MDAT input for mouse communication.
KI2	97	I4	General Purpose Input, Bit 2 (Keyboard Controller input port P1, bit 2). This pin does not change function with AT/PS2 Mode setting.
KI3	96	I4	General Purpose Input, Bit 3 (Keyboard Controller input port P1, bit 3). This pin does not change function with AT/PS2 Mode setting.
KI5	95	I4	General Purpose Input, Bit 5 (Keyboard Controller input port P1, bit 5). This pin does not change function with AT/PS2 Mode setting.
IDE BUS I/O			
–IDENH	2	O1	IDE Bus Transceiver High Byte Enable
–IDENL	3	O1	IDE Bus Transceiver Low Byte Enable
IDINT	122	I4	IDE Bus Interrupt Request
IDB7	119	IO6	IDE Bus Data Bit 7
–DC	123	I4	Floppy Disk Change
–HCS1	124	O1	IDE Host Chip Select 1
IRQI	33	O6	IDE Interrupt Request
COMMON BUS I/O			
SD0	115	IO2	System Bus Data, Bit 0
SD1	114	IO2	System Bus Data, Bit 1
SD2	111	IO2	System Bus Data, Bit 2
SD3	110	IO2	System Bus Data, Bit 3
SD4	109	IO2	System Bus Data, Bit 4
SD5	108	IO2	System Bus Data, Bit 5
SD6	106	IO2	System Bus Data, Bit 6
SD7	105	IO2	System Bus Data, Bit 7
SA0	17	I1	System Bus Address, Bit 0
SA1	18	I1	System Bus Address, Bit 1
SA2	19	I1	System Bus Address, Bit 2
SA3	20	I1	System Bus Address, Bit 3
SA4	21	I1	System Bus Address, Bit 4
SA5	22	I1	System Bus Address, Bit 5
SA6	23	I1	System Bus Address, Bit 6
SA7	24	I1	System Bus Address, Bit 7
SA8	25	I1	System Bus Address, Bit 8
SA9	26	I1	System Bus Address, Bit 9
SA10	27	I1	System Bus Address, Bit 10
SA11	28	I1	System Bus Address, Bit 11

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SA12	29	I1	System Bus Address, Bit 12
SA13	30	I1	System Bus Address, Bit 13
SA14	31	I1	System Bus Address, Bit 14
SA15	32	I1	System Bus Address, Bit 15
XTAL1	82	NA	Crystal/Clock Input - 18.432 MHz
XTAL2	83	NA	Crystal/Clock Output - 18.432 MHz
–IOR	11	I1	System Bus I/O Read
–IOW	12	I1	System Bus I/O Write
RES	125	I5	System Reset
AEN	13	I1	System Bus Address Enable
ALE	14	I1	System Bus Address Latch Enable
–IOCS16	116	O8	System Bus I/O Chip Select 16
IOCHRDY	118	O8	System Bus I/O Channel Ready
SYSCLK	128	I1	System Clock - Processor clock divide by 2.
–CS4	7	O1	Chip Select 4 - This signal is reserved for an external floppy disk controller. It is controlled by the RTC Control Register 0, bit 1 - the "FDCS EN". This Control Register bit is also coupled to gating the disk change (–DC) signal on SD7 for I/O reads of 3F7. Therefore, –CS4 is strongly associated with external floppy disk control.
–CS5	8	O1	Chip Select 5 - Normally –HCS0 for IDE, but can be used as a general purpose chip select.
–CS6	9	O1	Chip Select 6 - Normally for use by an external floppy disk controller, but can be used as a general purpose chip select.
–CS7	10	O1	Chip Select 7 - Normally for use by an external floppy disk controller, but can be used as a general purpose chip select.
–CDAK4	102	I1	DMA Acknowledge forces –CS4 active.
XDDIR	120	I1	X Data Bus Transceiver Direction
XDIRS	5	O1	Modified X Data Bus Transceiver Direction Control Signal - Excludes real-time clock and Keyboard Controller decodes.
XDIRX	6	O1	X Data Bus Transceiver Control Signal - Includes all CS decodes generated on chip.
–XDEN	4	O1	X Data Bus Transceiver Enable
–TRI	126	I4	Three-state Control - Used for all outputs to isolate chip for board tests.
–ICT	127	I4	In-Circuit Test Mode Control
POWER, GROUND, & UNCOMMITTED			
VDD	15, 16, 50, 81, 113	PWR	System Power: +5 V
VSS	1, 38, 55, 60, 80, 84, 107, 112, 117	GND	System Ground

SIGNAL TYPE LEGEND

	mA	Type	Comment
O1	2	TTL	
O4	12	TTL-OD	Open drain, weak pull-up, no VDD diode
O6	4	TTL-TS	Three-state
O8	24	TTL-OD	Open drain, fast active pull-up
I1	–	TTL	
I2	–	CMOS	
I4	–	TTL	30k Ω pull-up resistor
I5	–	TTL	Schmitt-trigger
I6	–	TTL	30k Ω pull-up resistor, no VDD diode
IO2	24	TTL-TS	Three-state
IO4	12	TTL-OD	Open drain, slow turn-on
IO5	12	TTL-TS	Three-state
IO6	24	TTL-TS	Three-state, 30k Ω pull-up resistor

FUNCTIONAL DESCRIPTION

Below is a detailed explanation of each of the major building blocks of the VL82C106 Combination I/O chip. The following functional blocks are covered:

- 16C450B serial ports
- Parallel printer port
- 146818A-compatible real-time clock
- Keyboard Controller
- Control and chip selects
- IDE interface

SERIAL COMMUNICATIONS PORTS

The chip contains two UARTs, based on the VL16C450B megacell core. Each of these UARTs share a common baud-rate clock, which is the XTAL1 input (18.432 MHz) divided by ten. The 18.432 MHz signal is shared with the Keyboard Controller, which divides it by three to get an approximate 6 MHz reference clock. Please refer to the VL16C452B data sheet for the register descriptions and timing parameters for the UARTs.

COMA is accessed via internally generated CS1, while COMB uses internally generated CS2.

LINE PRINTER PORT

The Line Printer Port contains the functionality of the port included in the VL16C452B, but offers a software programmable Extended Mode, which includes a Direction Control Bit and Interrupt Status Bit. These features are disabled on initial power-up, but may be turned on by clearing the –EMODE bit of Control Register 0 (RTC Register 69H in AT or PS/2 Mode or I/O Port 102H in PS/2 Mode). When the –EMODE bit is set, the part functions exactly as a PC/AT-compatible printer port.

The Line Printer Port is accessed via internally generated programmable chip select CS3.

Register 0 - Line Printer Port Data

The Line Printer (LPT) Port is either uni- or bidirectional, depending on the state of the Extended Mode and Data Direction Control bits.

Compatibility Mode (–EMODE bit = 1) - Read operations to this register return the last data that was written to the LPT Port. Write operations immediately output data to the LPT Port.

Extended Mode (–EMODE bit = 0) - Read operations return either the data last written to the LPT Data Register if the Direction Bit is set to output (0) or the data that is present on the pins of the LPT Port if the direction is set to input (1). Write operations latch data into the output register, but only drive the LPT Port when the Direction Bit is set to output.

In either case, the bits of the LPT Data Register are defined as follows:

Bit	Description
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

Register 1 - LPT Port Status
The LPT Status Register is a read-only register that contains interrupt status and real-time status of the LPT connector pins. The bits are described as follows:

Bit	Description
0	Reserved
1	Reserved
2	–IRQ
3	–ERROR
4	SLCT
5	PE
6	–ACK
7	–BUSY

Bits 0 and 1 - Reserved. Read as 1's.

Bit 2 - Interrupt Request Status Bit. This bit is enabled/disabled by bit 4 of the Printer Control Register. When enabled, it is latched low when –ACK is deasserted, indicating that the printer has acknowledged the previous transfer. The –IRQ status bit is cleared to a high level upon a read of the LPT Port status Register.

When in AT mode (bit 1 of RTC Register 6AH = 1), the IRQP output follows the –ACK input, if enabled. IRQP is set during the inactive transition of the –ACK signal. When in PS/2 mode, IRQP is set during the deassertion of the –ACK input, if enabled, and cleared following a read of the LPT status register.

Bit 3 - Error Status Bit. A 0 indicates that the printer has had an error. A 1 indicates normal operation. This bit follows the state of the –ERR pin.

Bit 4 - Select Status Bit. Indicates the current status of the SLCT signal from the printer. A 0 indicates the printer is currently not selected (off-line). A 1 means the printer is currently selected.

Bit 5 - Paper Empty Status Bit. A 0 indicates normal operation. A 1 indicates that the printer is currently out of paper. This bit follows the state of the PE pin.

Bit 6 - Acknowledge Status Bit. A 0 indicates that the printer has received a character and is ready to accept another. A 1 indicates that the last operation to the printer has not been completed yet. This bit follows the state of the –ACK pin.

Bit 7 - Busy Status Bit. A 0 indicates that the printer is busy and can not receive data. A 1 indicates that the printer is ready to accept data. This bit is the inversion of the BUSY pin.

Register 2 - LPT Port Control
This port is a read/write port that is used to control the LPT direction as well as the Printer Control lines driven from the port. Write operations set or reset these bits, while read operations return the status of the last write operation to this register. The bits in this register are defined as follows:

Bit	Description
0	–STB
1	–AFD
2	–INIT
3	–SLIN
4	IRQ EN
5	DIR
6	Reserved
7	Reserved

Bit 0 - Printer Strobe Control Bit. When set (1), the –STB signal is asserted on the LPT interface, causing the printer to latch the current data. When reset (0), the signal is negated.

Bit 1 - Autofeed Control Bit. When set (1), the –AFD signal will be asserted on the LPT interface, causing the printer to automatically generate a line feed at the end of each line. When reset (0), the signal is negated.

Bit 2 - Initialize Printer Control Bit output. When Bit 2 is set (1), the –INIT pin is negated (high). When Bit 2 is reset (0), the –INIT pin is asserted to the printer, forcing a reset.

Bit 3 - Select Input Control Bit. When set (1), the –SLIN signal is asserted, causing the printer to go "on-line". When reset (0), the signal is negated.

Bit 4 - Interrupt Request Enable Control Bit. When set (1), enables interrupts from the LPT Port whenever the –ACK signal is asserted by the printer. When reset (0), interrupts are disabled.

Bit 5 - When –EMODE = 0, Direction (DIR) Control Bit. When set (1), the output buffers in the LPT Port are disabled, allowing data driven from external sources to be read from the LPT Port. When reset (0), the output buffers are enabled, forcing the LPT buffers to drive the LPT pins. The power-on reset value of this is cleared (0). When –EMODE = 1, this write-only bit has no effect and should be read as 1.

Bits 6 and 7 - Reserved. Read as 1's.

REAL-TIME CLOCK

The Real-Time Clock (RTC) is the equivalent of the Motorola MC146818A Real-Time Clock component. It is also compatible with the Dallas Semiconductor DS1287A RTC when an external battery and crystal are provided. Clock functions include the following:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- Programmable square-wave output
- 50 bytes of user RAM
- User RAM preset feature

RTC PROGRAMMERS MODEL

The RTC memory consists of ten RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 50 general purpose RAM bytes. The address map of the real-time clock is shown below.

Add.	Function	Range
00-09	Time Regs.	0-99
0A	RTC Register A	(R/W)
0B	RTC Register B	(R/W)
0C	RTC Register C	(R-O)
0D	RTC Register D	(R-O)
0E-3F	User RAM (Standby)	

All 64 bytes are directly readable and writable by the processor program except for the following:

1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.

The RTC is normally accessed via internally decoded port 070H (RTC register address) and port 071H (RTC data read/write).

The RTC address and data ports can be moved to port 170H, port 171H by pulling the RTCMAP pin (121) to ground. This pin can be left unconnected or tied high for normal port addressing.

The RTC address map also includes additional standby RAM, plus control registers for Combination chip configuration and chip select control. The RAM and Chip Select Control Registers are powered via the VBAT power supply for battery-backed operation. The total address map is shown below:

Add. (HEX)	Function
00-0D	Time Portion of RTC
0E-3F	RAM Portion of RTC
40-4F	Additional Standby RAM
50-68	Reserved - No RAM
69-7F	Chip Select Control Registers

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

TIME OF DAY REGISTER

The contents of the Time of Day registers can be either in Binary or BCD format. They are relatively straightforward, but are detailed here for completeness. The address map of these registers is shown next:

Add.	Function	Range
0	Seconds (Time)	0-59
1	Seconds (Alarm)	0-59
2	Minutes (Time)	0-59
3	Minutes (Alarm)	0-59
4	Hours (Time)	1-12, 12 Hr Mode
4	Hours (Time)	0-23, 24 Hr Mode
5	Hours (Alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99

Address 0 - Seconds (Time): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 1 - Seconds (Alarm): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 2 - Minutes (Time): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 3 - Minutes (Alarm): The range of this register is 0-59 in BCD mode and 0-3BH in Binary mode.

Address Range 4 - Hours (Time): The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01H-0CH	Binary	AM
81H-8CH	Binary	PM

Address 5 - Hours (Alarm): The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01H-0CH	Binary	AM
81H-8CH	Binary	PM

Address 6 - Day of Week: The range of this register is 1-7 in BCD mode, and 1-7H in Binary mode.

Address 7 - Date: The range of this register is 1-31 in BCD mode, and 1-1FH in Binary mode.

Address 8 - Month: The range of this register is 1-12 in BCD mode, and 1-0CH in Binary mode.

Address 9 - Year: The range of this register is 0-99 in BCD mode, and 0-63H in Binary mode.

RTC CONTROL REGISTER

The RTC has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Add.	Function	Type
0A	RTC Register A	R/W
0B	RTC Register B	R/W
0C	RTC Register C	R O
0D	RTC Register D	R O
0E-3F	User RAM (Standby)	R/W

Register A

This register contains control bits for the selection of Periodic Interrupt, Input Divisor, and the Update In Progress Status bit. The bits in the register are defined as follows:

Bit	Description	Abbr.
0	Rate Select Bit 0	RS0
1	Rate Select Bit 1	RS1
2	Rate Select Bit 2	RS2
3	Rate Select Bit 3	RS3
4	Divisor Bit 0	DV0
5	Divisor Bit 1	DV1
6	Divisor Bit 2	DV2
7	Update In Progress	UIP

Bits 0 to 3 - The four rate selection bits (RS0 to RS3) select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by RESET. The Periodic Interrupt Rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate
0	None
1	3.90625 ms
2	7.8125 ms
3	122.070 µs
4	244.141 µs
5	488.281 µs
6	976.562 µs
7	1.953125 ms
8	3.90625 ms
9	7.8125 ms
0AH	15.625 ms
0BH	31.25 ms
0CH	62.5 ms
0DH	125 ms
0EH	250 ms
0FH	500 ms

Bits 4 to 6 - The three Divisor Selection bits (DV0 to DV2) are fixed to provide for only a five-state divider chain, which would be used with a 32 KHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed, the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, Divider Running
6	Reset Mode, Divider in Reset State

Bit 7 - The Update In Progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1", the update cycle is in progress or will soon begin. When UIP is a "0", the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is "0". The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in Register B to a "1" will inhibit any update cycle and then clear the UIP status bit.

Register B

Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr.
0	Daylight Savings Enable	DSE
1	24/12 Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Not Used	
4	Update End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 - The Daylight Savings Enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

Bit 1 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode ("1") or the 12-hour mode ("0"). This is a read/write bit, which is affected only by software.

Bit 2 - The Data Mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

Bit 3 - This bit is unused in this version of the RTC, but is used for Square Wave Enable in the Motorola MC146818.

Bit 4 - The UIE (Update End Interrupt Enable) bit is a read/write bit which enables the Update End Interrupt Flag (UF) bit in Register C to assert an IRQ. The reset pin being asserted or the SET bit going high clears the UIE bit.

Bit 5 - The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a "1" permits the Alarm Interrupt Flag (AF) bit in Register C to assert an IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of 11XXXXXXb). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal. The reset pin clears AIE to "0". The internal functions do not affect the AIE bit.

Bit 6 - The Periodic Interrupt Enable (PIE) bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the IRQ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A "0" in PIE blocks IRQ from being initiated by a periodic interrupt, but the Periodic Interrupt Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal functions, but is cleared to "0" by a reset.

Bit 7 - When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

Register C

Register C contains status information about interrupts and internal operation of the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr.
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Update End Interrupt Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	IRQ Pending Flag	IRQF

Bits 0 to 3 - The unused bits of Status Register 1 are read as "0's", and cannot be written.

Bit 4 - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting IRQ. UF is cleared by a Register C read or a reset.

Bit 5 - A "1" in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the IRQ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A reset or a read of Register C clears AF.

Bit 6 - The Periodic Interrupt Flag (PF) is a read only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an IRQ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a reset or a software read of Register C.

Bit 7 - The Interrupt Request Pending Flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a "1", the IRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the reset pin is asserted.

Register D

This register contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr.
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Vaild RAM Data and Time	VRT

Bits 0 to 6 - The remaining bits of Register D are unused. They cannot be written, but are always read as "0's".

Bit 7 - The Valid RAM Data and Time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the reset pin. The VRT bit can only be set by reading Register D.

Pulling the PS/–RC pin low for a minimum of 2 µs also sets all RAM bytes from address OE through 3F to all ones.

CMOS STANDBY RAM

The 66 general purpose RAM bytes are not dedicated within the RTC. They can be used by the processor program, and are fully available during the update cycle.

GENERAL RTC NOTES

Set Operation

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the Data Mode (DM) bit of Register B. All ten time, calendar, and alarm bytes must use the same Data Mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the RTC makes all updates in the selected Data Mode. The Data Mode cannot be changed without reinitializing the ten data bytes.

BCD vs Binary Format

The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high-order bit of the hours byte represents PM when it is a "1".

Update Operation

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 KHz time base. The Update Cycle section shows how to accommodate the Update Cycle in the processor program.

Alarm Operation

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the Alarm Interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any byte from 0C0H to 0FFH. An Alarm Interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The Alarm Interrupt may be programmed to occur at rates from one-per-second to one-a-day. The Periodic Interrupt may be selected for rates from half-a-second to 30.517 µs. The Update Ended Interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control

The Divider Control bits are fixed for only 32.768 KHz operation. The divider chain may be held in reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half a second later. The Divider Control bits are also used to facilitate testing the RTC.

Periodic Interrupt Selection

The Periodic Interrupt allows the IRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The Periodic Interrupt is separate from the Alarm Interrupt which may be output from once-per-second to once-per-day.

Update Cycle

The RTC executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV2-DV0 divider is not clear, and the SET bit in Register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the second byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 KHz time base update cycle takes 1984 µs, during which, the time, calendar, and alarm bytes are not accessible by the processor program, protecting the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update is progress (UIP) status bit is set during the interval.

Three methods of accommodating non-availablity during update are usable by the program. In discussing the three methods, it is assumed that at random points, user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update in progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. After the UIP bit goes high, the update cycle begins 244

µs later. Therefore, if a low is a read in the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

KEYBOARD CONTROLLER

The Keyboard Controller on-chip ROM contains the code that is required to support the PC/AT and PS/2 command sets and 128 bytes of conversion code.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simplify error handling in software. This logic is duplicated for the mouse interface.

User RAM support is provided. The program writes a command 20-3FH (read) or 60-7FH (write) with the lower five bits representing the RAM address. Data from a read or for a write are accessed through port 60H DBB.

Parallel Port 1 (input) is provided and Parallel Port 2 (output) has defined functions depending on whether the controller is in PC/AT or PS/2 Mode.

Support for Port 60H DBB (reads and writes) and Status Register (reads and writes) is provided in hardware for interface to the PC host.

KEYBOARD CONTROLLER INTERFACE TO PC/AT

The interface to the PC/AT consists of one register pair (Port 60H/64H) for the keyboard and mouse.

The Port 60H read operations output the contents of the Output Buffer to D0-D7 and clears the status of the Output Buffer Full (OBF/Status Register bit 0) bit.

Status read operations output the contents of the Status Register to D0-D7. No status is changed as a result of the read operation.

The Port 60H write operations cause the Input Buffer DBB to be changed. The state of the C/D bit is cleared (Status Register bit 3, 0 indicates data) and the Input Buffer Full (IBF/Status Register bit 1) bit is set (1).

Command write operations are to Port 64H. The C/D bit will be set to (1) when a valid command has been written to Port 64H.

KEYBOARD PORT INTERFACE PROTOCOL

Data transmission between the controller, the keyboard, and mouse consist of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start Bit (Always 0)
2	Data Bit 0 (LSB)
3-8	Data Bits 1-6
9	Data Bit 7 (MSB)
10	Parity Bit (Odd)
11	Stop Bit (Always 1)

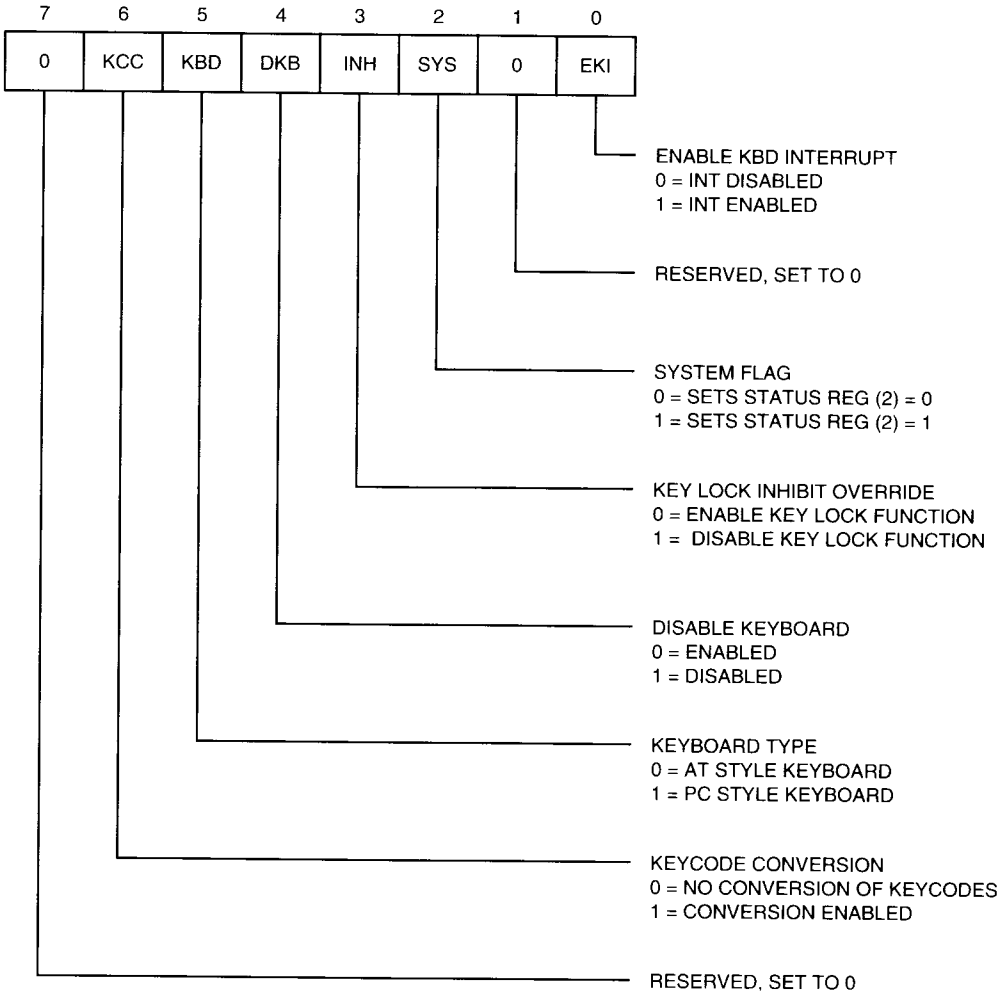
PROGRAMMER INTERFACE

The programmer interface to the Keyboard Controller is quite simple, consisting of four registers:

Register	R/W	I/O
Status	R	64H
Command	W	64H
Output Buffer	R	60H
Input Buffer	W	60H

The behavior of these registers differ according to the mode of operation (PC/AT or PS/2). There exists only one Mode Register and one Status Register with different bit definitions for PC/AT Mode and PS/2 Mode.

FIGURE 1. PC/AT MODE REGISTER (READ PORT 60H AFTER WRITE COMMAND 20H TO PORT 64H)



PC/AT MODE REGISTER

Bit 0 - Enable Keyboard Interrupt (EKI), when set ("1") causes the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Bit 1 - Reserved, should be written as "0".

Bit 2 - System Flag (SYS), when set ("1") writes the System Flag bit of the Status Register to "1". This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Inhibit Override (INH), when set ("1") disables the keyboard lock function (KKSW Input).

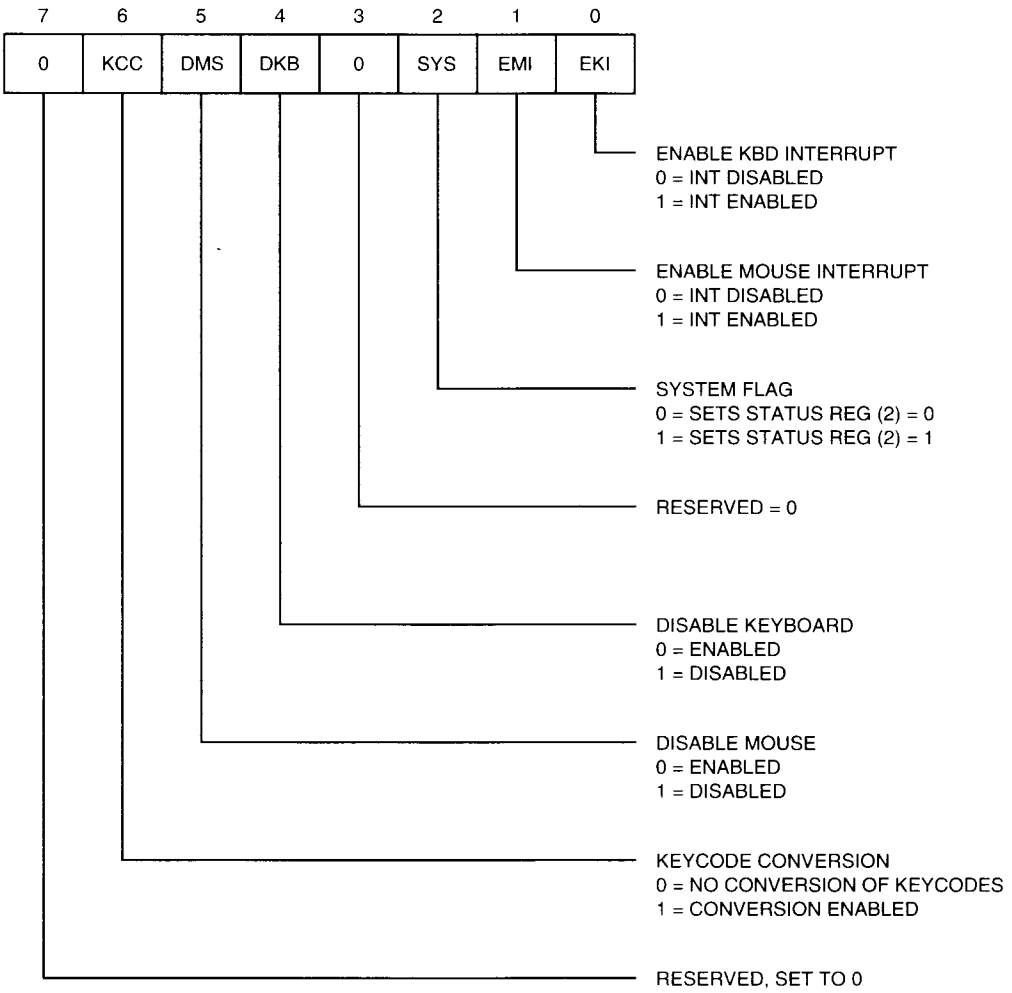
Bit 4 - Disable Keyboard (DKB), when set ("1") disables the keyboard by holding the –KCKOUT line low.

Bit 5 - Keyboard Type (KBD), when set ("1") allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.

Bit 6 - Keycode Conversion (KCC), when set ("1") causes the controller to convert the scan codes to PC format. When reset, the codes (AT keyboard) are passed along unconverted.

Bit 7 - Reserved, should be written as "0".

FIGURE 2. PS/2 MODE REGISTER (READ PORT 60H AFTER WRITE COMMAND 20H TO PORT 64H)



PS/2 MODE REGISTER

Bit 0 - Enable Keyboard Interrupt (EKI), when set ("1") causes the controller to generate a keyboard interrupt whenever data (keyboard or command) is written into the output buffer.

Bit 1 - Enable Mouse Interrupt (EMI), when set ("1") allows the controller to generate a mouse interrupt when mouse data is available in the output register.

Bit 2 - System Flag (SYS), when set ("1") writes the System Flag bit of the Status Register to "1". This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Reserved, "0".

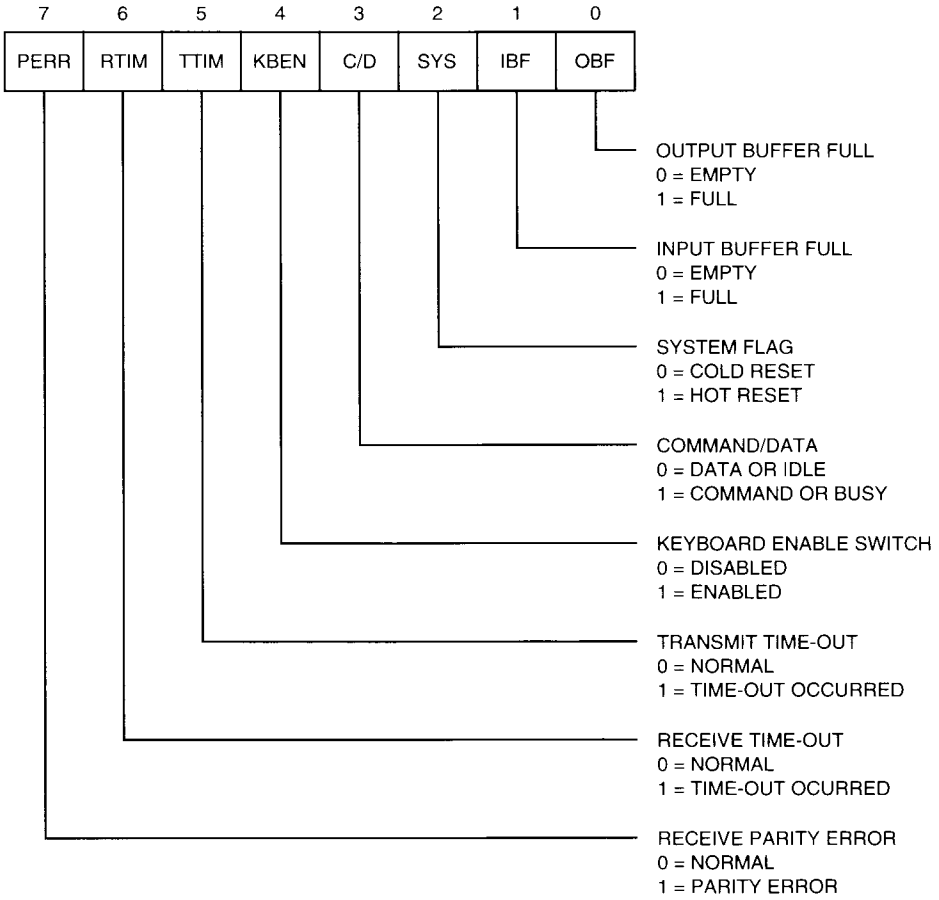
Bit 4 - Disable Keyboard (DKB), when set ("1") disables the keyboard by holding the –KCKOUT low.

Bit 5 - Disable Mouse (DMS), when set ("1") disables the mouse by deasserting the Mouse clock.

Bit 6 - Keycode Conversion (KCC), when set ("1") causes the controller to convert the scan codes to PC format. When reset, the codes (PS/2 keyboard) are passed along unconverted.

Bit 7 - Reserved, "0".

FIGURE 3. PC/AT STATUS REGISTER (READ-ONLY - PORT 64H)



PC/AT Status Register

Bit 0 - Output Buffer Full (OBF), when set ("1") indicates that data is available in the controller Data Bus Buffer, and that the CPU has not read the data yet. CPU reads to PORT 60H to reset the state of this bit.

Bit 1 - Input Buffer Full (IBF), when set ("1") indicates that data has been written to PORT 60H or 64H, and the controller has not read the data.

Bit 2 - System Flag (SYS), when set ("1") indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (CD), when set ("1") indicates that a command has been placed into the Input Data Buffer of the controller. The controller uses this bit to determine if the byte written is a command to be executed.

Bit 4 - Keyboard Enable (KBEN), indicates the state of the "keyboard inhibit" switch input (KKSW). "0" indicates the keyboard is inhibited.

Bit 5 - Transmit Time-out (TTIM), when set ("1") indicates that a transmission to the keyboard was not completed before the controller's internal timer timed-out.

Bit 6 - Receive Time-out (RTIM), when set ("1") indicates that a transmission from the keyboard was not completed before the controller's internal timer timed-out.

Bit 7 - Parity Error (PERR), when set ("1") indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the KIRQ pin is set ["1" if the EKI bit/ Mode Register bit 0 is set ("1")].

FIGURE 4. PC/AT KEYBOARD SCAN CODE TRANSLATION TO PC/XT SCAN CODE

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
00	ff
01	43
02	41
03	3f
04	3d
05	3b
06	3c
07	58
08	64
09	44
0a	42
0b	40
0c	3e
0d	0f
0e	29
0f	59
10	65
11	38
12	2a
13	70
14	1d
15	10
16	02
17	5a
18	66
19	71
1a	2c
1b	1f
1c	1e
1d	11
1e	03
1f	5b
20	67
21	2e
22	2d
23	20
24	12
25	05
26	04
27	5c
28	68
29	39
2a	2f
2b	21
2c	14
2d	13
2e	06
2f	5d

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
30	69
31	31
32	30
33	23
34	22
35	15
36	07
37	5e
38	6a
39	72
3a	32
3b	24
3c	16
3d	08
3e	09
3f	5f
40	6b
41	33
42	25
43	17
44	18
45	0b
46	0a
47	60
48	6c
49	34
4a	35
4b	26
4c	27
4d	19
4e	0c
4f	61
50	6d
51	73
52	28
53	74
54	1a
55	0d
56	62
57	6e
58	3a
59	36
5a	1c
5b	1b
5c	75
5d	2b
5e	63
5f	76

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
60	55
61	56
62	77
63	78
64	79
65	7a
66	oe
67	7b
68	7c
69	4f
6a	7d
6b	4b
6c	47
6d	7e
6e	7f
6f	6f
70	52
71	53
72	50
73	4c
74	4d
75	48
76	01
77	45
78	57
79	4e
7a	51
7b	4a
7c	37
7d	49
7e	46
7f	54

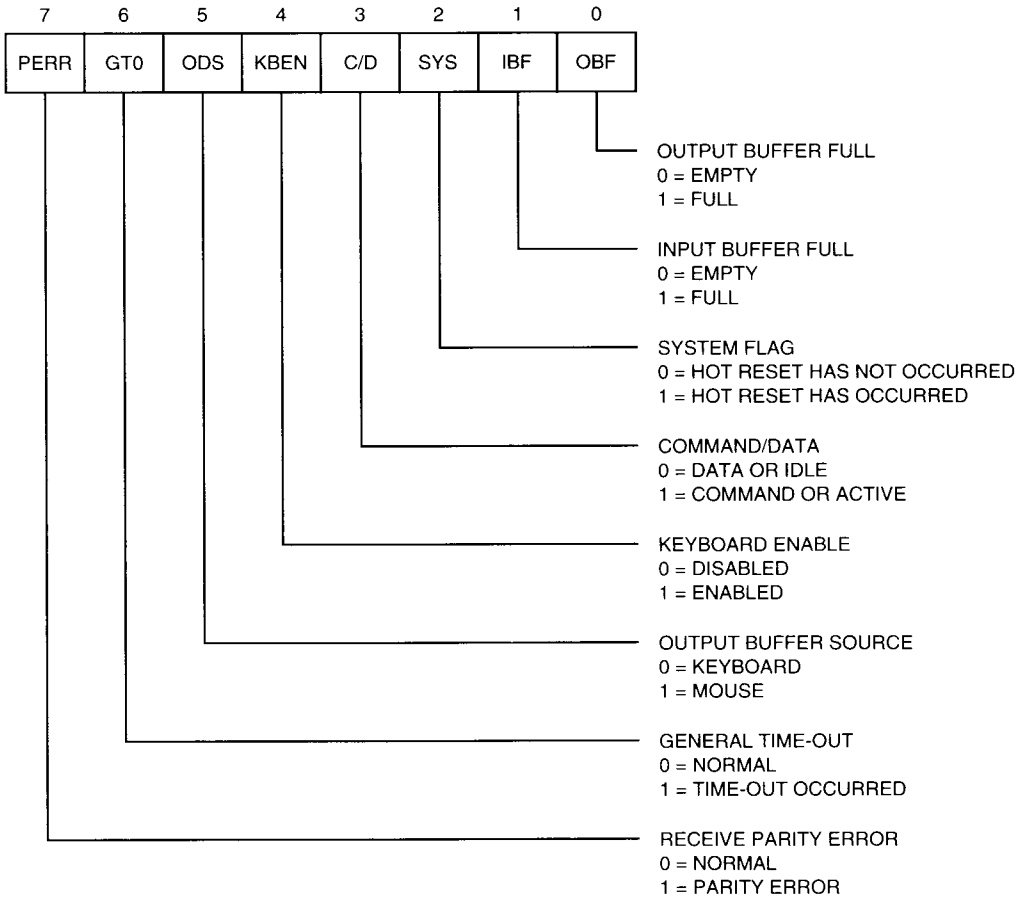
The following scan codes are converted by in-line code:

KEYBOARD SCAN CODE	SYSTEM SCAN CODE
83	41
84	54

Note: All other PC/AT scan codes are passed to the system untranslated.

5

FIGURE 5. PS/2 STATUS REGISTER (READ-ONLY - PORT 64H)



PS/2 Status Register

Bit 0 - Output Buffer Full (OBF), when set ("1") indicates that data is available in the controller Data Bus Buffer, and that the CPU has not read the data yet. The CPU reads to PORT 60H reset the state of this bit.

Bit 1 - Input Buffer Full (IBF), when set ("1") indicates that data has been written to PORT 60H or 64H, and the controller has not read the data.

Bit 2 - System Flag (SYS), when set ("1") indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (CD), when set ("1") indicates that a command has been placed into the Input Data Buffer of the controller. The controller uses this bit to determine if the byte written is a command to be executed. This bit is not reset until the command has completed its operation.

Bit 4 - Keyboard Enable (KBEN) indicates the state of the "keyboard inhibit" switch, KKSW (KI7), input port. This general purpose input has no other effect in PS/2 Mode.

Bit 5 - Output Buffer Data Source (ODS), when set ("1") indicates that the data in the output buffer is mouse data. When reset, it indicates the data is from the keyboard.

Bit 6 - Time-out Error (TERR), when set ("1") indicates that a transmission was started and that it did not complete within the normal time taken (approximately 11 KCKIN cycles). If the transmission originated from the controller, a FEH is placed in the output buffer. If the transmission originated from the keyboard, a FFH is placed in the output buffer.

Bit 7 - Parity Error (PERR), when set ("1") indicates that a parity error (even parity = error) occurred during the last transmission from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the KIRQ pin is set ["1" if the EKI bit/Mode Register bit 0 is set ("1")].

COMMAND SET

The command set supported by the keyboard controller supports two modes of operation, and a set of extensions to the AT command set for the PS/2. In both modes, the command is implemented by writing the command byte to port 64H. Any subsequent data is read from port 60H (see description of command 20) or written to port 60H (see description of command port 60H). The commands for each mode are shown in the table below:

PC/AT Mode:

Comm.	Description
20	Read Mode Register
60	Write Mode Register
AA	Self Test
AB	KBD Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port (P10-P17)
D0	Read Output Port (P20-P27)
D1	Write Output Port
E0	Read Test Inputs (T0, T1)
F0-FF	Pulse Output Port (P20-P27)

Note: If data is written to the data buffer (port 60H) and the command preceding it did not expect data from the port (port 60H) the data will be transmitted to the keyboard.

Added PS/2 Commands:

Comm.	Description
21-3F	Read Keyboard Controller RAM (Byte 1-31)
61-7F	Write Keyboard Controller RAM (Byte 1-31)
A4	Test Password
A5	Load Password
A6	Enable Password
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
C1	Poll in Port Low (P10-P13 -> S4-S7)
C2	Poll in Port High (P14-P17 -> S4-S7)
D1	Write Output Port
D2	Write Keyboard Output Buffer
D3	Write Mouse Output Buffer
D4	Write to Mouse

The following is a description of each command:

20 Read Keyboard Controller's Mode Register (PC/AT & PS/2)

The Keyboard Controller sends its current mode byte to the output buffer (accessed by a read of port 60H).

21-3F Read Keyboard Controller's RAM (PS/2 only)

Bits D4-D0 specify the address.

60 Write Keyboard Controller's Mode Register (PC/AT & PS/2)

The next byte of data written to the keyboard data port (port 60H) is placed in the controller's mode register.

61-7F Write Keyboard Controller's RAM (PS/2 only)

This command writes to the internal Keyboard Controller RAM with the address specified in bits D4-D0.

A4 Test Password Installed (PS/2 only)

This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and KIRQ is asserted (if the EKI bit is set). Test result - FAH means that the password is installed, and F1H means that it is not.

A5 Load Password (PS/2 only)

This command initiates the password load procedure. Following this command, the Controller will take data from the input buffer port (port 60H) until a 00h data byte is detected or a full 8 byte password is loaded into the password latches. Password data bytes are untranslated "make" scan codes. Break scan codes and "release" scan codes are not checked as part of the password validation.

A6 Enable Password (PS/2 only)

This command enables the security feature. The A6 command is valid only when the A5 Load Password command has been properly executed. All incoming keyboard "make" scan codes will be compared for a match, all keyboard data and mouse data will be discarded until the proper scan code sequence is entered via the keyboard. The Keyboard Controller will not accept and execute commands from the system while the password security is enabled.

A7 Disable Mouse (PS/2 only)

This command sets bit 5 of the Mode Register which disables the Mouse (–MCKOUT) clock signal.

A8 Enable Mouse (PS/2 only)

This command resets bit 5 of the Mode Register, thus enabling the Mouse clock (–MCKOUT).

A9 Mouse Interface Test (PS/2 only)

This command causes the Controller to test the mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the MIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Mouse Clock Line Stuck Low
02	Mouse Clock Line Stuck High
03	Mouse Data Line Stuck Low
04	Mouse Data Line Stuck High

AA Self Test command (PC/AT & PS/2)

This commands the Controller to perform internal diagnostic tests. A 55H is placed in the output buffer if no errors were detected. The OBF bit is set and KIRQ is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT & PS/ 2)

This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Keyboard Clock Line Stuck Low
02	Keyboard Clock Line Stuck High
03	Keyboard Data Line Stuck Low
04	Keyboard Data Line Stuck High

AC Diagnostic Dump (PC/AT only, Reserved on PS/2) - Sends 16 bytes of the controller's RAM, the current state of the input port, and current state of the output port to the system.

AD Keyboard Disable (PC/AT & PS/2)

This command sets bit 4 of the Mode Register to a 1. This disables the keyboard by disabling the clock line. Data will not be sent or received.

AE Keyboard Enable (PC/AT & PS/2)

This command resets bit 4 of the mode byte to a 0. This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT & PS/2)

This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port low (PS/2 only)

P1 bits 0-3 are written into Status Register bits 4-7 until a new command is issued to the Keyboard Controller.

C2 Poll Input Port high (PS/2 only)

P1 bits 4-7 are written into Status Register bits 4-7 until a new command is issued to the Keyboard Controller.

D0 Read Output Port (PC/AT & PS/2)

This command causes the Controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
0	P20	–RC	–RC
1	P21	A20 Gate	A20 Gate
2	P22	Speed Sel	–MDOUT
3	P23	Shadow Enable	–MCKOUT
4	P24	Output Buffer Full	KIRQ
5	P25		MIRQ
6	P26	–KCKOUT	–KCKOUT
7	P27	KDOUT	–KDOUT

Note: P22 (bit 2) is the speed control pin used by Award BIOS, and this is different from what is used by Phoenix and AMI, this bit is reserved by the keyboard controller in PS/2 Mode.

D1 Write Output Port (PC/AT & PS/2)

The next byte of data written to the keyboard data port (port 60H) will be written to the Controller's output port. The definitions of the bits are as defined above. In PC/AT Mode, P26 and P27 are not modified. In PS/2 Mode, P22, P23, P24, P25, P26 and P27 are not modified.

D2 Write Keyboard Output Buffer (PS/2 only)

The next byte written to the data buffer (port 60H) is written to the output buffer (60H) as if initiated by the keyboard [the OBF bit is set (1) and KIRQ will be set if the EKI bit is set (1)].

D3 Write Mouse Output Buffer (PS/2 only)

The next byte written to the data buffer (port 60H) is written to the output buffer as if initiated by the mouse [the OBF bit is set (1) and MIRQ will be set if the EMI bit is set (1)].

D4 Write to Mouse (PS/2 only)

The next byte written to the data buffer (port 60H) is transmitted to the mouse.

E0 Read Test Inputs (PC/AT & PS/2)

This command causes the Controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Keyboard Data	Keyboard Clock
1	Keyboard Clock	Mouse Clock
3-7	Read as 0's	Read as 0's

F0-FF Pulse Output Port (PC/AT & PS/2)

Bits 0-3 of the Controller's output port may be pulsed low for approximately 6 µs. Bits 0-3 of the command specify which bit will be pulsed. A 0 indicates that the bit should be pulsed; a 1 indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port). In PC/AT Mode, bits P26 and P27 are not pulsed. In PS/2 Mode, bits P26, P27, P22 and P23 are not pulsed.

IDE Bus Interface Control
Integrated Drive Electronics bus interface control signals are provided by the VL82C106 Combination chip. The timing and drive for these lines are consistent with the Conner Peripherals CP342 Integrated Hard Disk Manual.

A set of signals are used for this interface when the VL82C106 Combination chip is configured to support the IDE interface via IDE_EN, bit 5 of Control Register 1 (RTC Register 6AH).

The Combination chip has duplicated bit 1 of the "Fixed Disk Register" (I/O 3F6H) to enable IRQI.

Input Signals:

IDINT IDE Bus Interrupt Request
This signal indicates an interrupt request to the system. It is used to generate IRQI.

Output Signals:

–CS4 Chip Select 4
This signal is used as the floppy disk chip select. The default decode is 03F4H-03F5H, but may be redefined as described in the section on Combination Chip Control Registers. The IDE_EN control bit of Control Register 1 has no effect on this signal. –CS4 is also active when –CDAK4 is active.

When this chip select is enabled via FDCS_EN (RTC Control Register 0 bit 1), reads of 03F7h will cause the –DC input bit to be driven to the SD7 output bit.

–CS5 Chip Select 5
This signal is used as the –HOST CS0 of the IDE bus. The default decode is 01F0H-01F7H, but may be redefined as described in the section on Combination Chip Control Registers. The IDE_EN control bit of Control Register 1 has no effect on this signal.

–HCS1 Host Chip Select 1
This signal is active (low) for address 03F6H-03F7H and is used as –HOST CS1 of the IDE bus.

–IDENH IDE Bus Enable High Byte
This signal is used to drive the –OE pin of an external 74LS245 buffering bits 8-15 of the IDE data bus to the SD bus. It is active (low) when:

(–CS5 is active AND SA2-SA0 = 000) AND IDE_EN = 1 AND –IOR is active.

–IDENL IDE Bus Enable Low Byte
This signal is used to drive the –OE pin of an external 74LS245 buffering bits 0-6 of the IDE data bus. It is active (low) when:

(–CS5 is active OR SA0-SA9 = 3F6 OR 3F7) AND IDEN =1 and –IOR is active.

This allows a simple implementation for an IDE bus that includes both the hard disk controller and the floppy disk controller.

IRQI IDE Interrupt Request
This is the three-state interrupt request to the CPU. It is normally tied directly to the IRQ14 signal of the system. It reflects the state of the IDINT input and is enabled by writing bit 1 = 0 of I/O 3F6H as long as IDE_EN=1. Reset or disabling the IDE system three-states IRQI.

–IOCS16 I/O Chip Select 16
The VL82C106 has multiple sources for this signal. It is driven active (low) when:

(–CS5 is active AND SA0-SA2 = 000 AND IDE_EN = 1 AND {(CS_MODE = 0) OR (CS_MODE = 1 AND 16-bit operation selected for CS5)}) OR (any other CS is active with 16-bit operation selected AND CS_MODE = 1) OR (IDE_EN = 0 AND CS5 is active AND 16-bit operation is selected AND CS_MODE = 1).

Bidirectional Signals:

IDB7, –DC IDE Bus Data Bit 7
Floppy Disk Change
The control for the transceiver between IDB7, –DC, and SD7 is as follows:

IDB7 –> SD7 when:
–CS5 is active OR (SA0-SA9 = 3F AND –IOR is active AND IDE_EN = 1).

–DC –> SD7 when:
SA0-SA9 = 3F7H AND –IOR is active AND FDCS_EN = 1.

SD7 –> IDB7 at all other times when: IDE_EN = 1 and IDB7 is three-stated (with internal pull-up) if IDE_EN = 0.

Combination Chip Control Ports:
Contained in the VL82C106 are a set of 26 registers used for programming peripheral chip select base addresses, chip select address ranges, and enabling options. Each Base Address Register is a 16-bit register with bits corresponding to address bits A15-A0.

In addition to Base Address Registers, there is an Address Range Register that can be used to "don't-care" bits (A0-A4) used in the address range comparison, effectively controlling the address space occupied by the chip select from 1 to 32 bytes. There are also programmable bits to selectively generate wait states, and assert –IOCS16 whenever the corresponding address range is present. These registers are used in groups of three per chip select, and are defined as shown below:

Base Address Register (LSB):

Bit	Description
0	Base Address, Bit A0
1	Base Address, Bit A1
2	Base Address, Bit A2
3	Base Address, Bit A3
4	Base Address, Bit A4
5	Base Address, Bit A5
6	Base Address, Bit A6
7	Base Address, Bit A7

Base Address Register (MSB):

Bit	Description
0	Base Address, Bit A8
1	Base Address, Bit A9
2	Base Address, Bit A10
3	Base Address, Bit A11
4	Base Address, Bit A12
5	Base Address, Bit A13
6	Base Address, Bit A14
7	Base Address, Bit A15

Range Register:

Bit	Description
0	Don't Care, Bit A0
1	Dont' Care, Bit A1
2	Don't Care, Bit A2
3	Don't Care, Bit A3
4	Don't Care, Bit A4
5	Wait State 0
6	Wait State 1
7	8/16 Bit I/O

The only bits that need detailed descriptions are those contained in the Range Register. These bits are defined as follows:

Bits 0-4 - Don't Care Bits. When set (1), these bits cause that corresponding bit to be ignored during the chip select generation, effectively allowing the chip select signals to correspond to a range or ranges of addresses in the space from Base Address + 0 to Base Address + 31.

Bits 5, 6 - Wait State 0 and 1. These bits determine the number of wait states that will be generated whenever the corresponding chip select signal is generated. They generate wait states according to the following table:

WS1	WS0	Wait States*
0	0	0
0	1	1
1	0	3
1	1	7

* Number of wait states = number of SYSCLK cycles IOCHRDY is forced inactive (low) by the Combination chip.

Note: Programmed wait states can only extend the I/O cycle set by the system architecture.

Bit 7 - 8/16-Bit I/O. This bit is used to selectively assert –IOCS16 whenever the corresponding chip select signal is generated. When set (1), the access is defined as an 8-bit access, and –IOCS16 is not asserted.

Default Chip Selects

The VL82C106 Combination chip also has several hard-wired default chip selects for the serial ports, line printer port, floppy disk chip select and hard disk chip select. These default chip selects are used after a reset until the battery-backed programmable values are enabled via bit 3 of the second Control Register (RTC Register 6AH). The wait state and non IDE –IOCS16 values are also disabled in this mode. This allows the Combination chip to function normally without the need for programming. The default chip selects are:

Select/ Device	Address
COMA	3F8H-3FFH (Bit 3 of RTC Reg 69H = 1) 2F8H-2FFH (Bit 3 of RTC Reg 69H = 0)
COMB	2F8H-2FFH (Bit 3 of RTC Reg 69H = 1) 3F8H-3FFH (Bit 3 of RTC Reg 69H = 0)
LPT	03BCH-03BFH (Bit 5, 6 of RTC Reg 69H = 0, 0) 0378H-037BH (Bit 5, 6 of RTC Reg 69H = 1, 0) 0278H-027BH (Bit 5, 6 of RTC Reg 69H = 0,1)
–CS4	03F4H-03F5H
–CS5	01F0H-01F7H
–CS6	03F2H AND –IOW is Active
–CS7	03F7H AND –IOW is Active

Note: Note that on reset, COMA, COMB, LPT, and –CS4 through –CS7 are enabled and set to the hard-wired values. –CS6 and –CS7 are only qualified by –IOW when the hard-wired decodes are enabled. By writing values to Control Registers 7Ah through 7Fh and enabling these values via bit 3 of Control Register 1, the –IOW qualification is removed. –CS6 and –CS7 then become general purpose chip selects usable for read and write cycles.

Combination Chip Control Register

The VL82C106 Combination chip contains a number of programmable options, including peripheral base address and chip select "hole" size. The registers used to provide this control are located in the upper bytes of the RTC address space. They are defined as follows:

Addr	Usage
69	Control Register 0*
6A	Control Register 1*
6B	CS1 COMA Base Add LSB
6C	CS1 COMA Base Add MSB
6D	CS1 COMA Range
6E	CS2 COMB Base Add LSB
6F	CS2 COMB Base Add MSB
70	CS2 COMB Range
71	CS3 LPT Base Add LSB
72	CS3 LPT Base Add MSB
73	CS3 LPT Range
74	CS4 FDC Base Add LSB
75	CS4 FDC Base Add MSB
76	CS4 FDC Range
77	CS5 HDC Base Add LSB
78	CS5 HDC Base Add MSB
79	CS5 HDC Range
7A	CS6 Base Add LSB
7B	CS6 Base Add MSB
7C	CS6 Range
7D	CS7 Base Add LSB
7E	CS7 Base Add MSB
7F	CS7 Range

* Note: Control Register 0 and 1 are not battery-backed via the VBAT supply.

Control Register 0 (RTC Register 69H or I/O Port 102H) Bits:
This register contains bits that enable or disable functionality of the internal components of the Combination chip. The bits of this register are defined to be consistent with definitions used in the PS/2-50 family.

This register can also be accessed at address 102H, for PS/2 compatibility. The contents of the register are detailed below:

Bit	Usage	Value After Reset
0	SYS BD EN	Enabled (1)
1	FDCS EN (CS4)	Enabled (1)
2	COMA EN (CS1)	Enabled (1)
3	COMA DEF	COM1 (1)
4	LPT EN (CS3)	Enabled (1)
5	LPT DEF 0	Paralled Port 1 (0)
6	LPT DEF 1	Disabled (0)
7	–EMODE	Compat. Mode (1)

Bit 0 - System Board Enable (SYS BD EN) Control Bit. When set (1), allows bits 1, 2, and 4 to enable and disable their respective devices. When reset (0), the floppy disk chip select (CS4), COMA (CS1), and the LPT port (CS3) are disabled regardless of the contents of bits 1, 2, and 4.

Bit 1 - Floppy Disk CS Enable (FDCS EN) Control Bit. This control register when set 1, will enable –DC --> SD7 bit generation on I/O reads of 3F7H. When reset 0, SD7 will be three-stated on I/O reads of 3F7H.

Bit 2 - Communications Port A Enable (COMA EN) Control Bit. When set (1) allows the internal COMA (CS1) port to be accessed. When reset (0) COMA is disabled.

Bit 3 - Communications Port A Default Address (COMA DEF) Control Bit. When set (1), it forces the hard-wired default base address to COMA to correspond to (3F8H-3FFH) and COMB to (2F8H-2FFH). When reset (0), it forces the COMA hard-wired address to (2F8H-2FFH) and COMB to (3F8H-3FFH). The base address will be the programmed values if bit 3 of Control Register 1 (RTC Register 6AH) is set.

Bit 4 - Line Printer Port Enable (LPT EN) Control Bit. When set (1), it enables the LPT Port (CS3). When reset (0), it disables the LPT Port.

Bit 5, 6 - Line Printer Default bits 0 and 1 (LPT DEF 0 and 1) Control Bits. Set the Line Printer Base hard-wired address defaults as shown below:

Bit 6	Bit 5	Address Range
0	0	03BCH-03BFH
0	1	0378H-037BH
1	0	0278H-027BH
1	1	Reserved

Setting bit 3 of RTC Register 6AH changes the base address to that set in the Program Address Registers for LPT (CS3).

Bit 7 - Line Printer Extended Mode (EMODE) Control Bit. When set (1), it disables the Extended Mode and forces PC/AT compatibility. When reset (0), the Extended Mode is enabled, allowing the printer port direction to be controlled.

Control Register 1 (RTC Register 6AH) Bits
This register is used to control peripheral chip selects that are not included in Control Register 0. The bits in this register are defined as follows:

Bit	Usage	Value After Reset
0	COMB EN	Enabled (1)
1	AT/PS2 KBD	AT (1)
2	PRIV EN	Enabled (1)
3	CS MODE	Hard-wire (0)
4	HDCS EN	Enabled (1)
5	IDE EN	Enabled (1)
6	CS6 EN	Enabled (1)
7	CS7 EN	Enabled (1)

Bit 0 - Communication Port B Enable. A 1 enables COMB (CS2). A 0 disables COMB.

Bit 1 - AT or PS/2 Compatible Keyboard. A 1 selects PC/AT type Keyboard Controller functions, while a 0 places the Keyboard Controller in PS/2 Mode.

Bit 2 - Private Controls Enable. When in AT Mode (AT/PS2_KBD = 1), this bit is used to latch the values of the Keyboard Controller's output signals KHSE, KSRE, and IRQM to the VL82C106 output pins. When 1, these outputs follow the Keyboard Controller's outputs. When 0, these outputs held at that value regardless of the Keyboard Controller's outputs.

When in PS/2 Mode (AT/PS2_KBD = 0), this bit has no effect on the KHSE, KSRE, and IRQM output pins. The Combination chip outputs follow the Keyboard Controller's outputs.

Bit 3 - Chip Select Decode Mode. When 0, CS1-CS7 decodes revert to the hard-wired address decoding and non IDE –IOCS16 and IOCHRDY generation is disabled. A 1 enables the address decoding, wait state generation and 8/16-bit operation as programmed into the RTC Registers 69H-7FH. (See sections on "Default Chip Selects" and "Combination Chip Control Register.")

Bit 4 - Hard Disk Chip Select Enable. A 1 enables the hard disk chip select signal (–CS5), while a 0 disables the chip select.

Bit 5 - Integrated Drive Electronics Enable. A 1 enables the IDE functions of outputs –IDENH, –IDENL, IRQI, –IOCS16, and IDB7 as described in "IDE Bus Interface Control" section.

Bit 6 - Chip Select 6 Enable. When 0, the –CS6 output is disabled. A 1 enables the address decoding, wait state generation and 8/16-bit operation as programmed into the RTC Registers 7A-7CH. (See sections on "Default Chip Selects" and "Combination Chip Control Registers.")

Bit 7 - Chip Select 7 Enable. When 0, the –CS7 output is disabled. A 1 enables the address decoding, wait state generation and 8/16-bit operation as programmed into the RTC registers

7D-7FH. (See sections "Default Chip Selects" and "Combination Chip Control Register.")

Miscellaneous Control Signals

XDDIR XD Bus Transceiver Direction Signal

This input signal is normally generated by the system. It is inactive (low) when data is transferred from the XD bus to the SD bus, i.e., interrupt acknowledge cycles and I/O read accesses to addresses 000H-0FFH.

XDIRS XD Bus Transceiver Direction Control Signal

This output signal is to control the direction pin of a transceiver between the XD bus and the SD bus when the Combination chip is on the SD bus. Since the architecture assumes the RTC and Keyboard Controller are on the XD bus, this signal is set active (high) when XDDIR is high or either the RTC or the Keyboard Controller is selected.

XDIRX XD Bus Transceiver Control Signal

This output signal is to control the direction pin of the transceiver between the XD bus and the SD bus when the Combination chip is on the XD bus. Since the architecture assumes the peripherals other than the RTC and Keyboard Controller are on the SD bus, this signal is inactive (low) when the XDDIR is low or when –IOR is low and any chip select (CS1-CS7) is generated.

–XDEN XD Bus Transceiver Enable Signal

–CDAK4 DMA Acknowledge Signal (forces –CS4 Active)

This input will directly produce an active low on –CS4 when active low itself and is used by the IDE logic.

–IOCS16 I/O Chip Select 16 Signal

This output signal is used to indicate to the system that the peripheral being accessed is a 16-bit device. It is set active (low) when a programmed chip select, which specifies 16-bit I/O, is decoded or for certain IDE functions. (See sections on "Combination Chip Control Ports" and "IDE Bus Interface Control.")

When 16-bit programmed chip select operation is selected, –IOCS16 becomes active on the leading edge of ALE and inactive on the trailing edge of –IOW or –IOR. For 8-bit operation or default chip select operation, –IOCS16 is inactive during –IOW or –IOR active.

IOCHRDY I/O Channel Ready Signal

This output signal is used to lengthen the I/O cycle to the peripheral being accessed. It is set inactive (low) for the programmed number of wait states when a programmed chip select, which specifies one, three, or seven wait states, is decoded. (See the section "IDE Bus Interface Control.")

IOCHRDY transitions inactive at the falling edge of –IOW or –IOW, if enabled, and returns high at the falling edge of SYSCLK after the appropriate number of wait states SYSCLK cycles).

Note: Programmed wait states can only extend the I/O cycle, i.e., if the system architecture provides four wait states for 8-bit I/O, programming 1 or 3 has no effect.

XTAL1 Crystal Clock Input Signal

This pin is the input to the on-board 18.432 MHz crystal oscillator. This pin may also be driven by an external CMOS clock signal at 18.432 MHz.

XTAL2 Crystal Clock Output Signal

This pin is the output pin of the internal crystal oscillator and should be left open and unloaded if an external clock signal is applied to the XTAL1 pin. This pin is not capable of driving external loads other than the crystal.

–TRI Three-State Control Signal

This pin is used for in-circuit testing. When low, all outputs and I/O pins are placed in the high impedance state.

–ICT In-Circuit Test Signal

This pin, when strobed low, places the VL82C106 into Test Mode, determined by the data on the SD0-SD3 pins. The chip will remain in this mode until RES is asserted. Test Mode may be changed by strobing this pin low again with different data on the SD0-SD3 pins.

IN-CIRCUIT TEST LOGIC

During In-Circuit Test (ICT), each output may be toggled by one or more of the inputs. This allows for a board level tester to check the solder connection of each pin. The sequence for enabling ICT is as follows:

1. Start with –ICT high, –TRI high, and RES low.
2. Tester drives –TRI low to minimize possibility of bus contention.
3. Tester drives the SD7-SD0 bus with a value of X6h.
4. Tester drives the –ICT pin low, then high after 100 ns minimum.
5. Tester drives –TRI high.
6. Perform testing.
7. Tester drives RES pin in order to exit ICT mode.

The first table below shows the pins for which a one to one mapping occurs between an input and output. The second table shows signals for which one input is mapped to two outputs. In three instances, denoted by an asterisk, there is an inversion between the input and the output.

IN-CIRCUIT TEST INPUT TO OUTPUT MAPPING FOR THE VL82C106

ICT Input		ICT Output		ICT Input		ICT Output	
Sig. Name	**Pin #**	**Sig. Name**	**Pin #**	**Sig. Name**	**Pin #**	**Sig. Name**	**Pin #**
SA0	17	–XDIRS	5	–DSRA	78	SOUTA	46
SYSCLK	128	–XDIRX	6	–CTSA	79	–RTSB	47
–IOR	11	–CS4	7	–ERR	70	PD3	56
–IOW	12	–CS5	8	SLCT	71	PD2	57
AEN	13	–CS6	9	BUSY	72	PD1	58
ALE	14	–CS7	10	PE	73	PD0	59
SA1	18	IRQK	34	–ACK	74	–STB	61
SA2	19	IRQM	35	SINA	75	–AFD	62
SA3	20	IRQR	36	–STBY	65	–INIT	63
SA4	21	IRQB	37	–CDAK4	120	–SLIN	64
SA5	22	IRQA	39	OSCI	66	OSCO *	67
SA6	23	IRQP	40	XTAL1	82	XTAL2 *	83
SA7	24	IRQE	41	SINB	85	MCLK/KSRE	100
SA8	25	–OUT2A	42	–RIB	86	MDAT/KHSE	101
SA9	26	–OUT2B	43	–RLSDB	87	KA20	91
SA10	27	–DTRB	48	–DSRB	88	KRES	90
SA11	28	SOUTB	49	–CTSB	89	KCLK	103
SA12	29	PD7	51	KCM	92	KDAT	104
SA13	30	PD6	52	KKSW	93	SD6	106
SA14	31	PD5	53	KRSEL	94	SD5	108
SA15	32	PD4	54	KI1	98	SD1	114
IDINT	122	IRQI	33	XDDIR	120	–IOCS16	116
–RIA	76	–RTSA	44	RTCMAP	121	–HCS1	124
–RLSDA	77	–DTRA	45				

*Pins so marked have an inversion in the logic path.

VL82C106 INPUTS THAT ARE DIRECTLY CONNECTED TO TWO OUTPUTS

ICT Input		ICT Output		ICT Output	
Sig. Name	**Pin #**	**Sig. Name**	Pin #	**Sig. Name**	**Pin #**
K15	95	SD4	109	IOCHRDY	118
K13	96	SD3	110	–IDENH	2
K12	97	SD2	111	–IDENL	3
K10	99	SD0	115	–XDEN	4
–DC	123	IDB7	119	SD7	105

*Pins so marked have an inversion in the logic path.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write Figures 6, 7					
tSU1	Address Setup Time	55		ns	
tH2	Address Hold Time	20		ns	
tSU3	AEN Setup Time	55		ns	
tH4	AEN Hold Time	20		ns	
t5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL=200 pF
tH9	Read Data Hold	5	60	ns	CL=50 pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
Chip Select Timing (Hard-wired) Figures 8, 10					
tD11	Chip Select Delay from Address		35	ns	CL=50 pF
tD12	–CS6, –CS7 Delay from –IOW		30	ns	CL=50 pF
tD13	–IOCS16 Active from Address		60	ns	CL=200 pF
tD14	–CS4 Delay from –CDAK4		25	ns	CL=50 pF
Chip Select Timing (Programmable) Figures 8, 10					
tD11	Chip Select Delay from Address		45	ns	CL=50 pF
tD13	–IOCS16 Active from Address		70	ns	CL=200 pF
tD14	–CS4 Delay from –CDAK4		25	ns	CL=50 pF
–IOCS16/IOCHRDY Timing Figures 9, 10					
tD15	IOCHRDY Inactive from Command		50	ns	CL=200 pF
tD16	IOCHRDY Active from SYSCLK		55	ns	CL=200 pF
tD17	–IOCS16 Inactive from Command		55	ns	CL=200 pF
SYSCLK/ALE Timing Figures 9, 10					
t18	SYSCLK Period	84		ns	
t19	SYSCLK Pulse Width Low	35		ns	
t20	SYSCLK Pulse Width High	35		ns	
t21	ALE Pulse Width High	40		ns	

Note: –IOCS16, IOCHRDY are open-drain outputs with an active pull-up for approximately 10 ns. These parameters are measured at VOH = 1.5 V with a 300 ohm pull-up. Actual performance will vary depending on system configuration.

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
IDE Interface Timing Figure 11					
tD18	IRQI Delay from IDINT		40	ns	CL=100 pF
tD19	IDENH/IDENL Delay from Address		60	ns	CL=50 pF
tD20	IDB7 Delay from SD7 Input		40	ns	CL=200 pF
tD21	SD7 Delay from IDB7 Input		40	ns	CL=200 pF
tD22	SD7 Delay from –DC Input		40	ns	CL=200 pF
tD23	SD7 Delay from –IOR During IDE Access	0	85	ns	CL=200 pF
tH24	SD7 Hold from –IOR Inactive	5	60	ns	CL=50 pF
tD25	IDB7 Delay from –IOR Inactive	0	85	ns	CL=200 pF
tH26	IDB7 Hold from –IOR Active	5	60	ns	CL=50 pF
XDATA Control Timing Figure 12					
tD27	–XDIRS/–XDIRX Delay from –XDDIR		30	ns	CL=50 pF
tD28	–XDIRX Delay from –IOR		30	ns	CL=50 pF
tD29	–XDEN Delay from Command		30	ns	CL=50 pF
Real Time Clock Timing Figure 18					
tPSPW	Power Sense Pulse Width	2		µs	
tPSD	Power Sense Delay	2		µs	
tVRTD	VRT Bit Delay		2	µs	
tSBPW	–STBY Pulse Width	2		µs	

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AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
SERIAL, PRINTER					
Transmitter Figure 13					
tHR1	Delay from Rising Edge of –IOW (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from THRE Reset to Transmit Start		16	CLK Cycles	Note 2
tSI	Delay from Write to THRE	8	24	CLK Cycles	Note 2
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 2
tIR	Delay from –IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control Figure 14					
tMDO	Delay from –IOW (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –IOR (RS MSR)		250	ns	100 pF Load
Receiver Figure 12					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 2
tRINT	Delay from –IOR (RD RBR/RDLSR) to Reset Interrupt		1	µs	100 pF Load
Parallel Port Figure 15					
tDT	Data Time	1		µs	Software Controller
tSB	Strobe Time	1	500	µs	Software Controller
tAD	Acknowledge Delay (Busy Start to Acknowledge)			µs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			µs	Defined by Printer
tAK	Acknowledge Duration Time			µs	Defined by Printer
tBSY	Busy Duration Time			µs	Defined by Printer
tBSD	Busy Delay Time			µs	Defined by Printer

Notes: 1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. CLK cycle refers to external 18.432 MHz clock divided by 10, e.g. 1.8432 MHz.

BUS TIMING

FIGURE 6. WRITE CYCLE

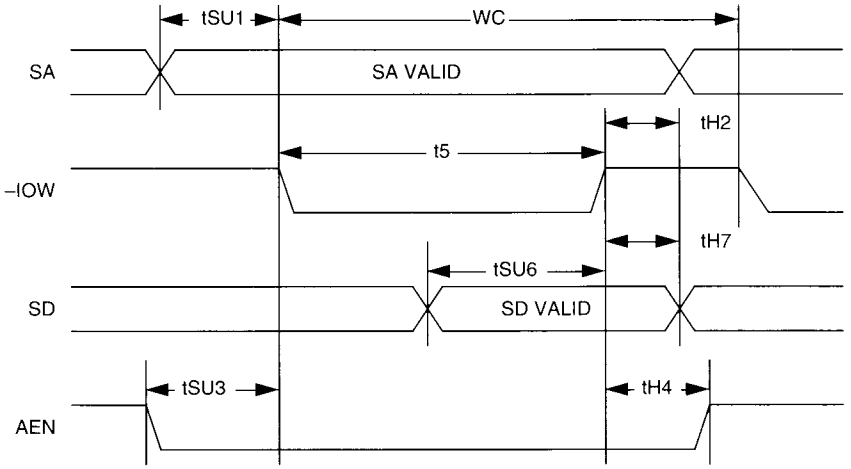
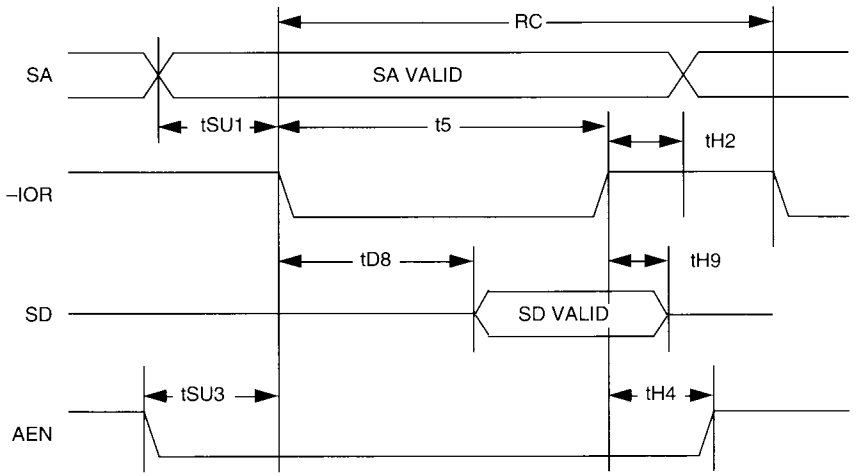


FIGURE 7. READ CYCLE



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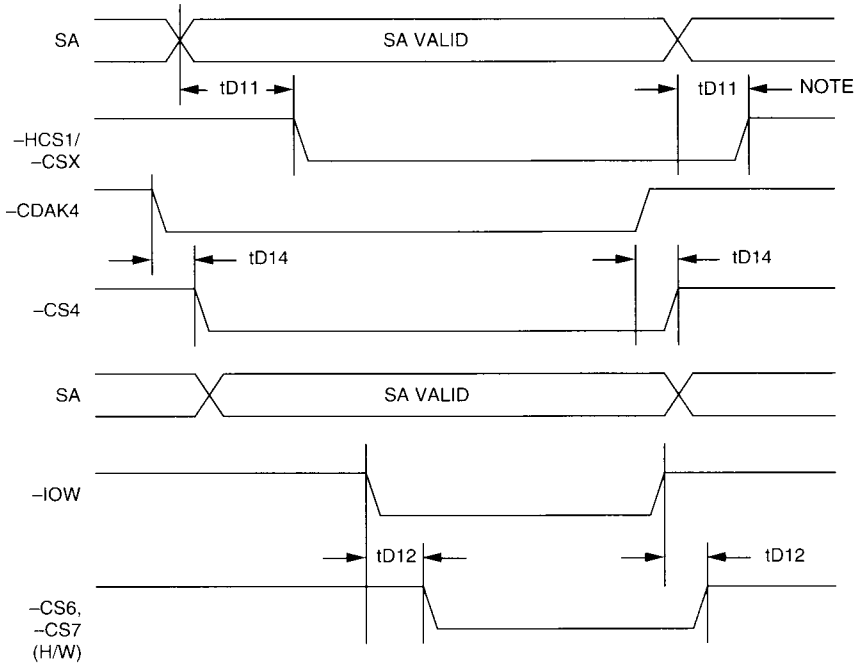
CHIP SELECT TIMING

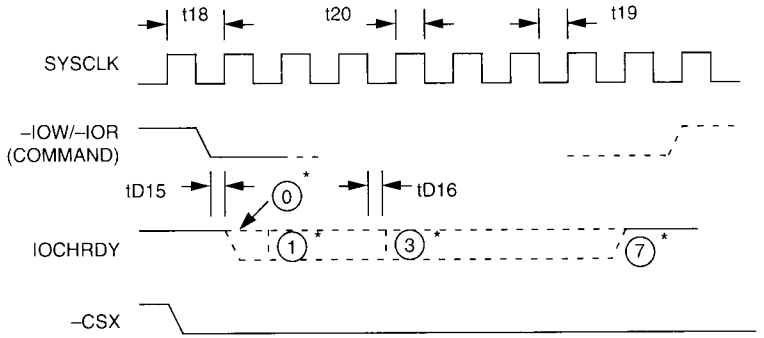
FIGURE 8.



Note: Except –CS6, –CS7 hard-wired.

IOCHRDY TIMING

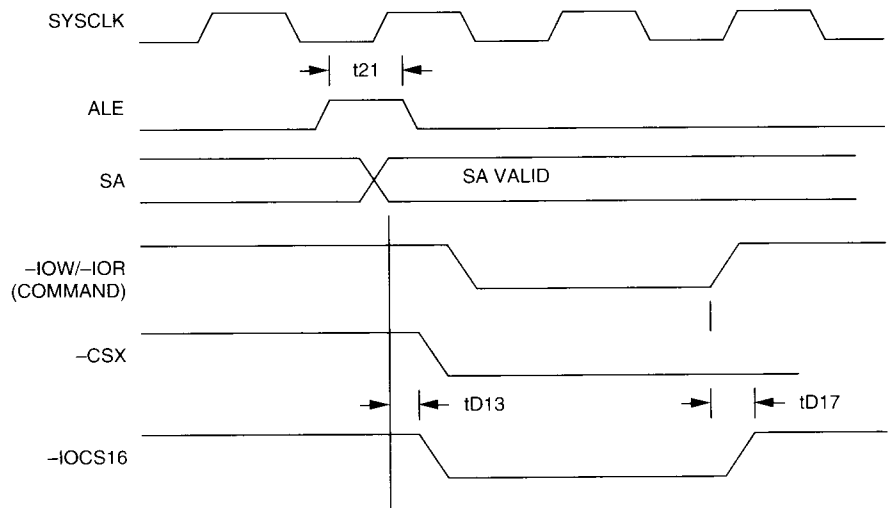
FIGURE 9.



* Programmed number of wait states. 0 = 0 wait state, 1 = 1 wait states, etc.

IOCS16 TIMING

FIGURE 10.



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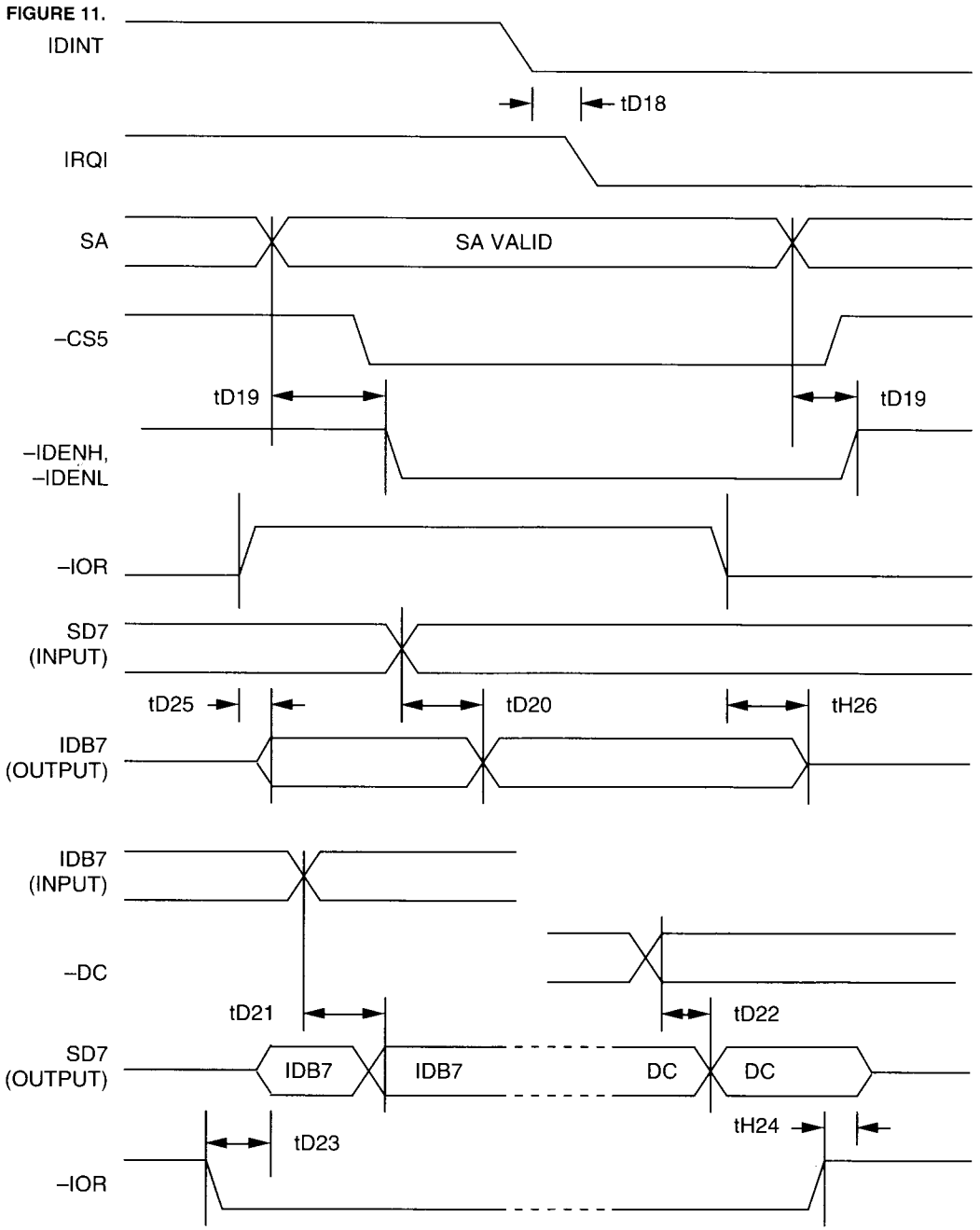
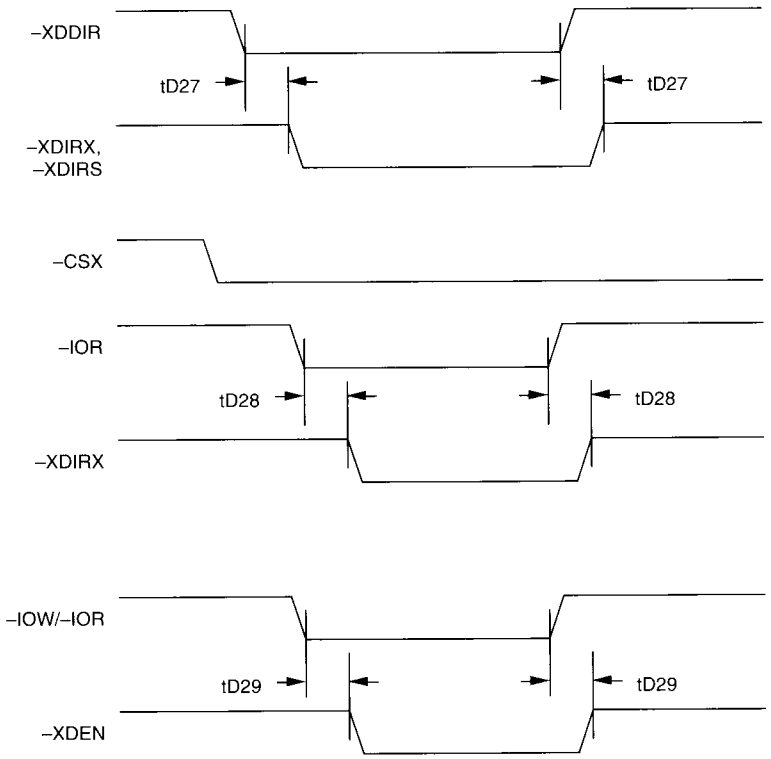
IDE INTERFACE TIMING

FIGURE 11.



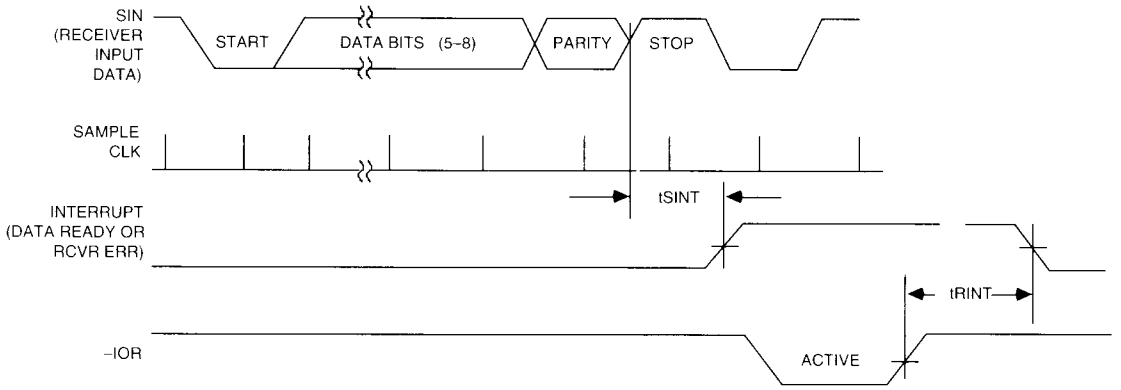
XDATA CONTROL TIMING

FIGURE 12.



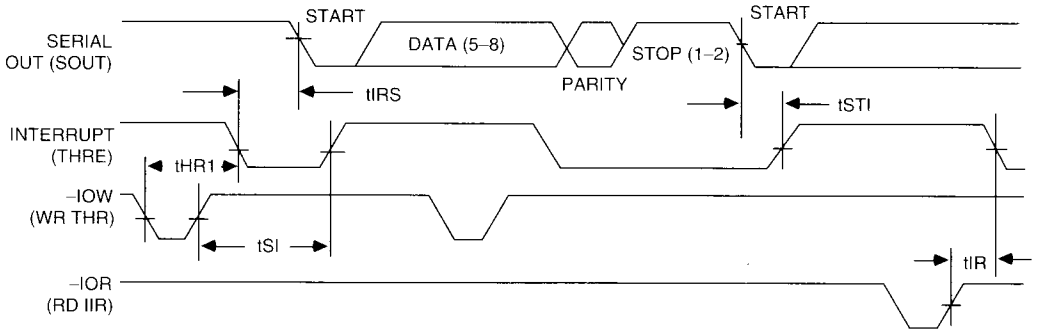
RECEIVER TIMING

FIGURE 13.



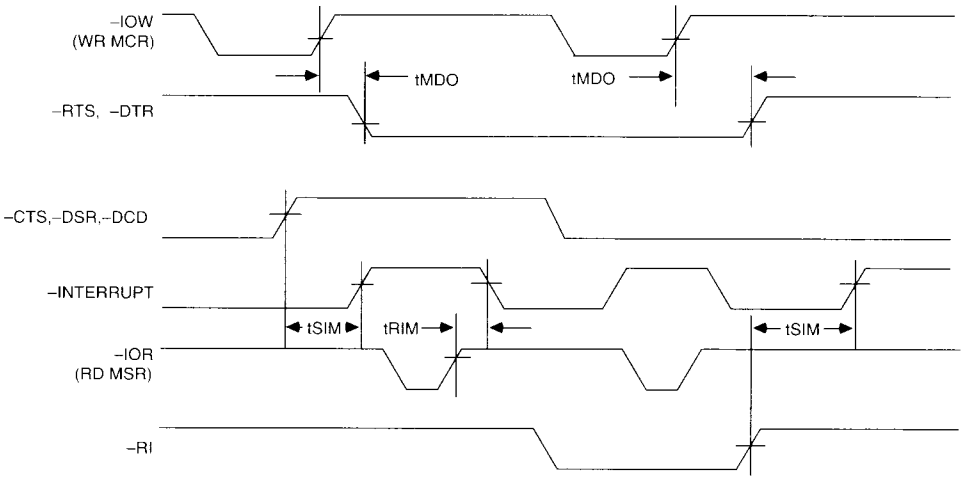
TRANSMITTER TIMING

FIGURE 14.



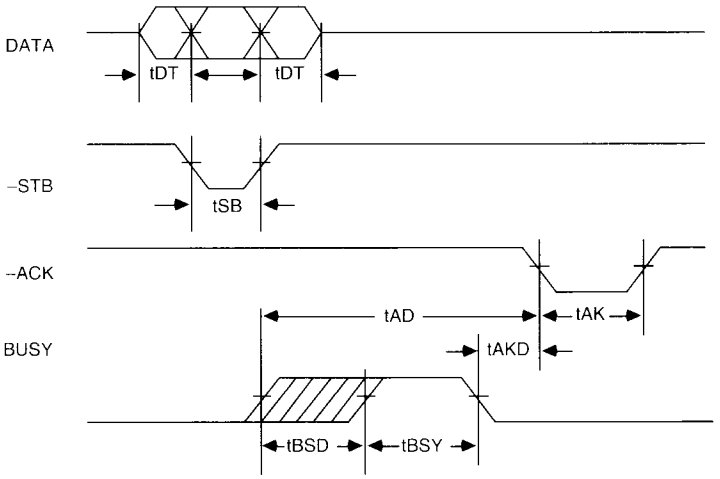
MODEM TIMING

FIGURE 15.



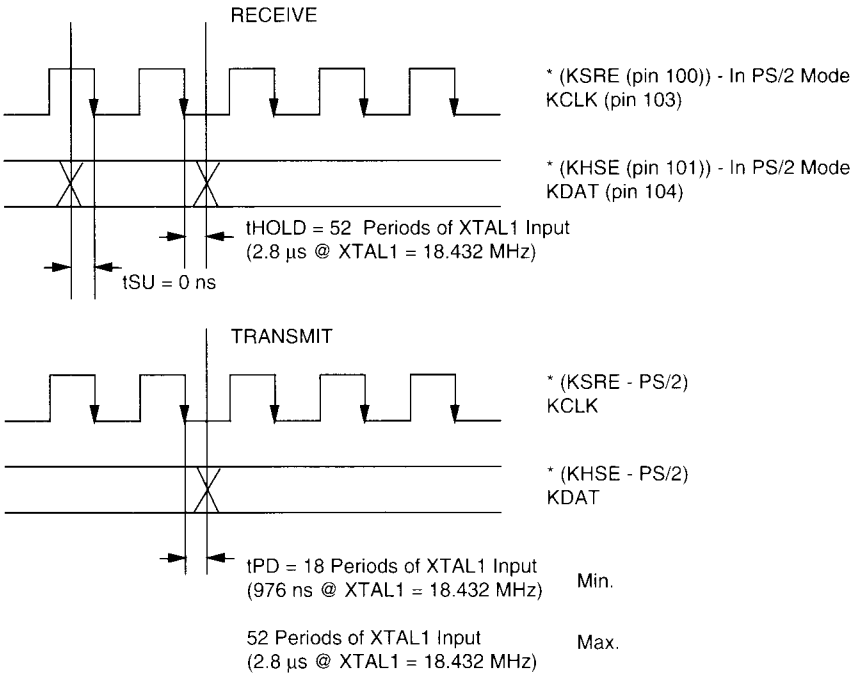
PARALLEL PORT TIMING

FIGURE 16.



KEYBOARD CONTROLLER TIMING

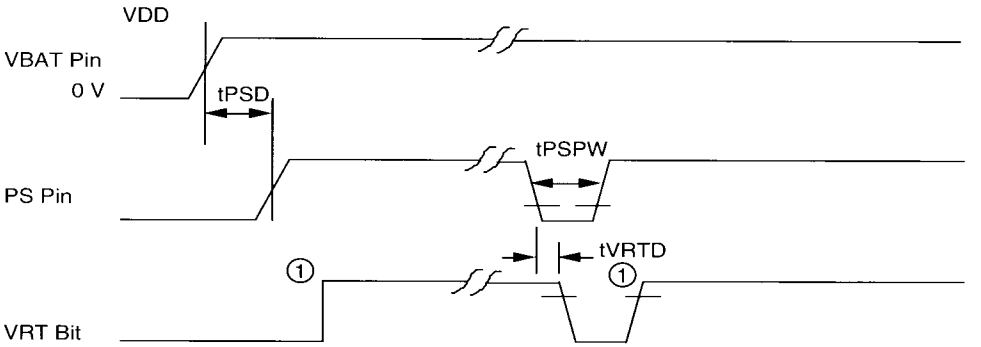
FIGURE 17.



*** Note:** Specifications are identical for KHSE (pin 101) with respect to KSRE (pin 100) in PS/2 Mode.

REAL-TIME CLOCK TIMING

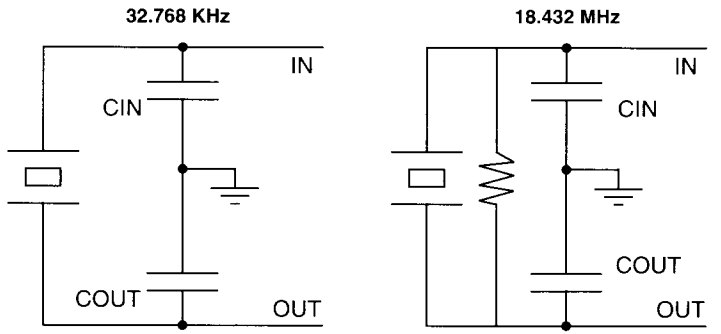
FIGURE 18.



① The VRT bit is set to a "1" by reading Register D. The VRT bit can only be cleared by pulling the PS pin low (see REGISTER D ($0D)).

CRYSTAL OSCILLATOR CONFIGURATIONS

FIGURE 19.



32.768 KHz

CIN = COUT = 10-22 pF
CIN may be a trimmer for precision timekeeping applications.

18.432 MHz

CIN = 10 pF
COUT = 30 pF
Kp = 10 Meg ohm

RECOMMENDED CRYSTAL PARAMETERS

Rs (max) ≤ 40k Ω
Co (max) ≤ 1.7 pF
CI (max) ≤ 12.5 pF
Parallel Resonance

Rs ≤ 50 Ω
Co ≤ 7 pF
CI ≤ 20 pF
Parallel Resonance

ABSOLUTE MAXIMUM RATING

Ambient Temperature	−10°C to +70°C
Storage Temperature	−65°C to 150°C
Supply Voltage to Ground Potential	−0.5 V to VDD +0.3 V
Applied Output Voltage	−0.5 V to VDD +0.3 V
Applied Input Voltage	−0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

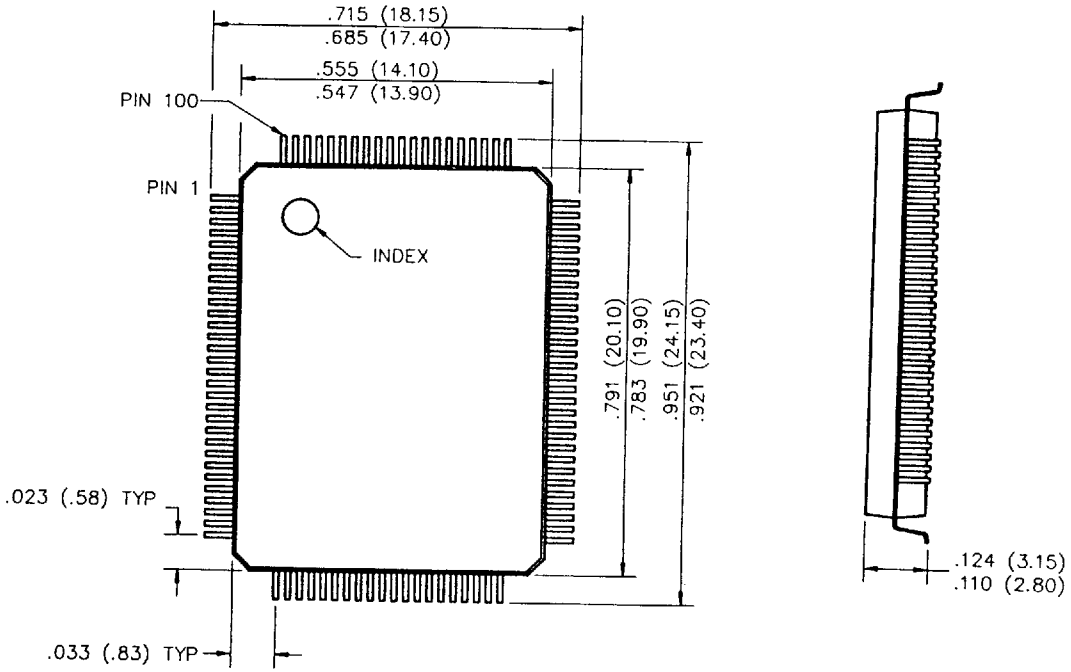
DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

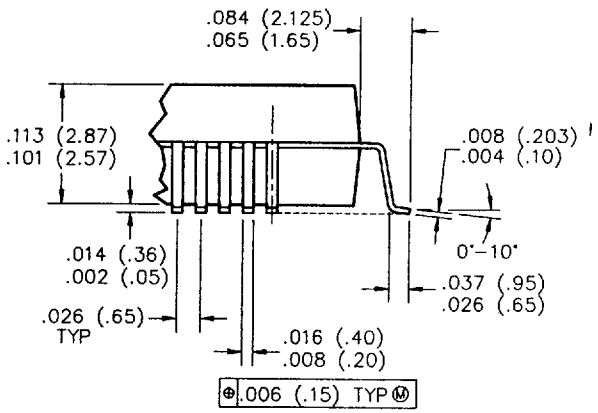
Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage				
	Input Types (All except I2)	−0.5	0.8	V	
	Input Type I2	−0.5	VDD + 0.2	V	
VIH	Input High Voltage				
	Input Types I1, I3, I4, IO2, IO4, IO5, IO6	2.0	VDD + 0.5	V	
	Input Type I2	VDD + 0.7	VDD + 0.5	V	
	Input Type I5	2.4	VDD + 0.5	V	
VOL	Output Low Voltage				
	Output Type 01		0.4	V	IOL = 2.0 mA
	Output Type 06		0.4	V	IOL = 4.0 mA
	Output Type 04, I04, I05		0.4	V	IOL = 12.0 mA
	Output Type 02, 07, 08, IO2, I06		0.4	V	IOL = 24.0 mA
VOH	Output High Voltage				
	Output Type 01,06	2.4		V	IOH = −0.8 mA
	Output Type I05	2.4		V	IOH = −2.0 mA
	Output Type 02, I02, I06	2.4		V	IOH = −2.4 mA
IIH	Input High Current				
	Input Types I1, I3, I4, I5		10	µA	VIN = VDD
IIL	Input Low Current				
	Input Types I1, I5	−10		µA	VIN = VSS + 0.2
	Input Types I4, IO6	−500	−50	µA	VIN = 0.8 V All other pins floating.
ILOL	Three-State Leakage Current				
	I/O Output Types 06, 07,	−50		µA	VSS+0.2
	I02, I04, I05		50	µA	VDD
IODL	Open-Drain Off Current				
	I/O Output Type 04	−5.0	−1.0	mA	V = 0.8 V
CO	Output Capacitance		8	pF	
CI	Input		8	pF	
CIO	Input/Output Capacitance		16	pF	
IDD	Operating Supply Current		40	mA	
IBAT	VBAT Supply Current, Standby Mode		5.0	µA	VBAT = 3.0 V
			50.0	µA	VBAT = 5.0 V
VBAT	Battery Supply Voltage, Standby Mode	2.4		V	IBAT is not tested

Note: For pin types, refer to the Signal Descriptions and Signal Legend on pages 5-6 through 5-11 of this data sheet.

100-PIN PLASTIC QUAD FLAT PACK

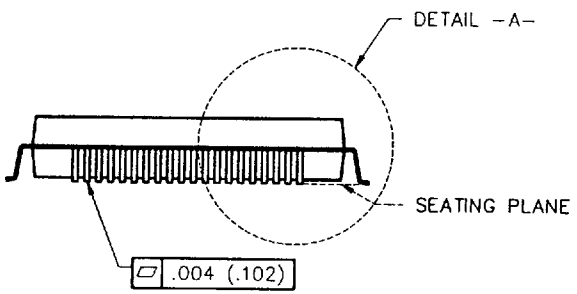
V L S I TECHNOLOGY INC





DETAIL –A–

NOTES:
1. CONTROLLING DIMENSION IS MM.



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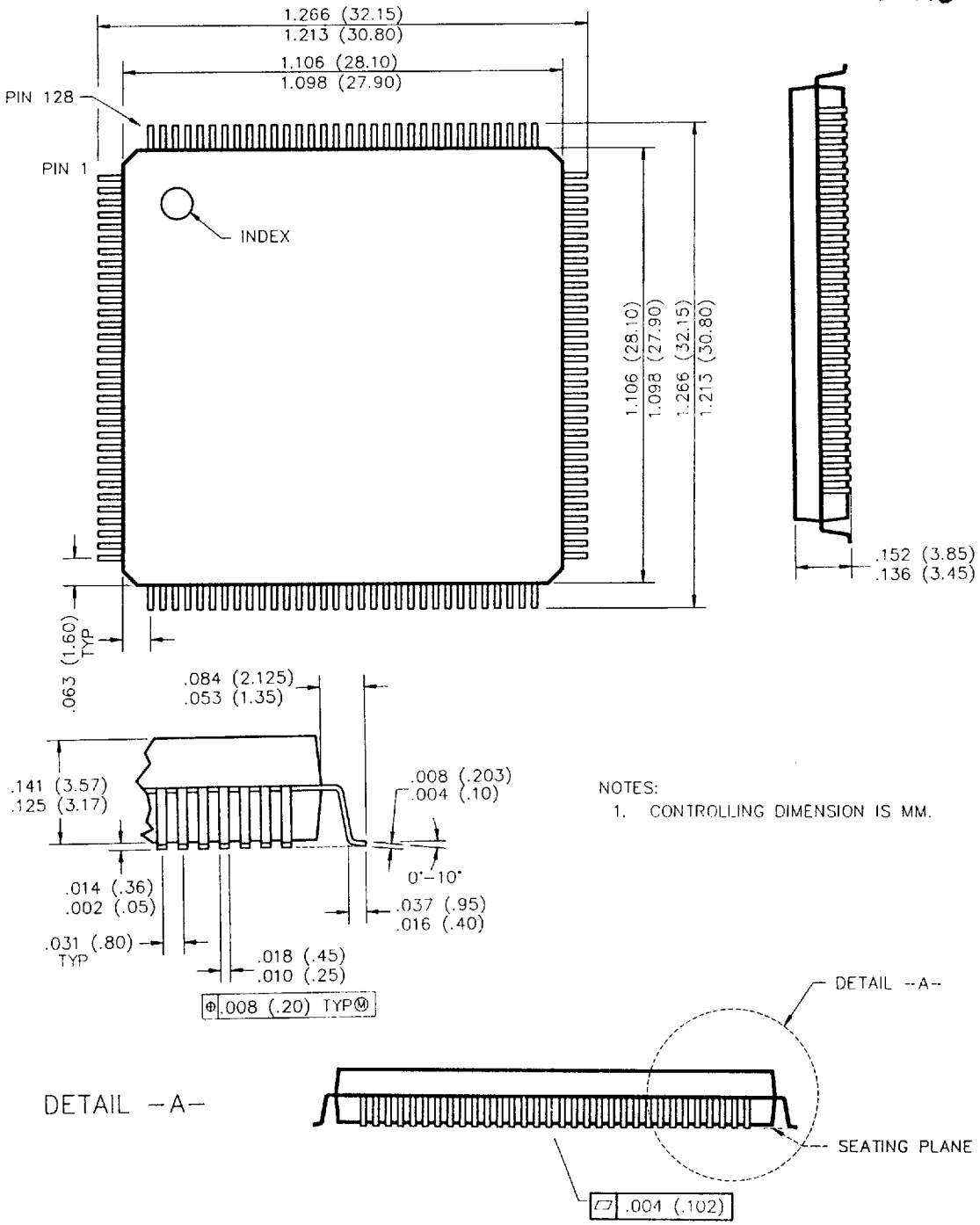
128-PIN PLASTIC FLAT PACK

V L S I TECHNOLOGY INC T-90-20

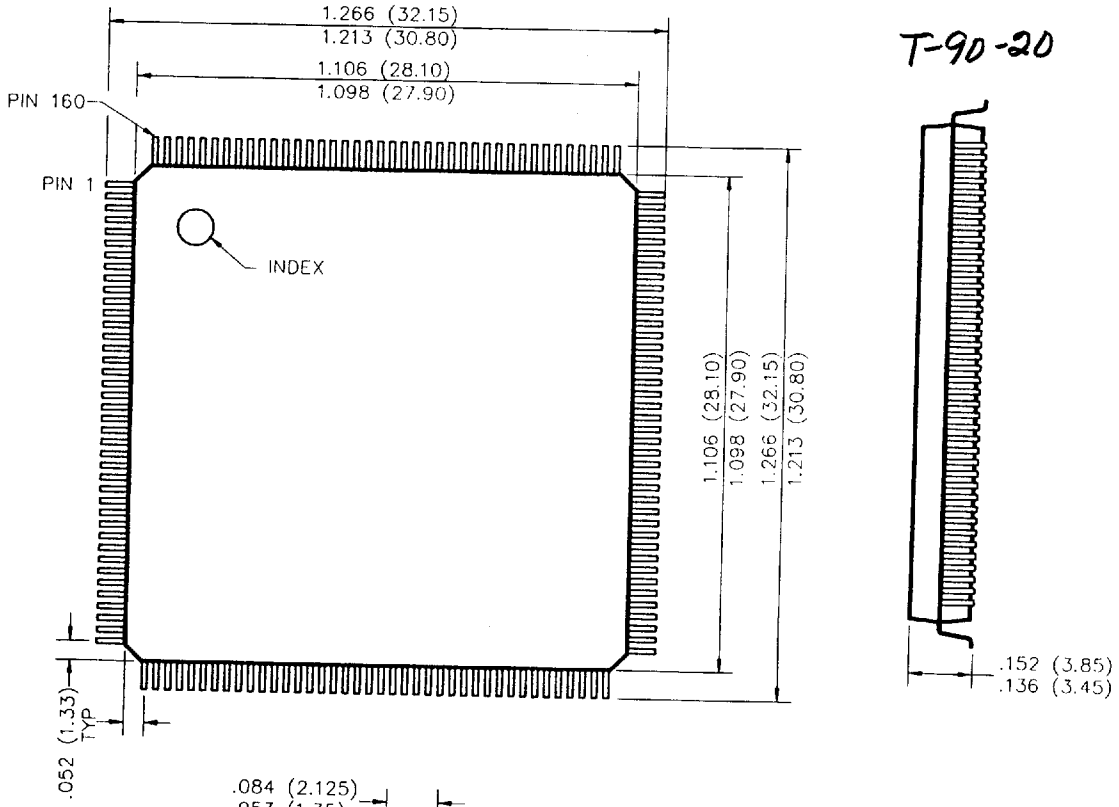


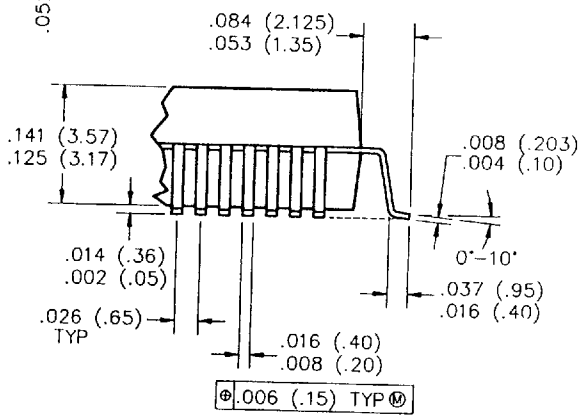
NOTES:
1. CONTROLLING DIMENSION IS MM.

160-PIN PLASTIC QUAD FLAT PACK

V L S I TECHNOLOGY INC

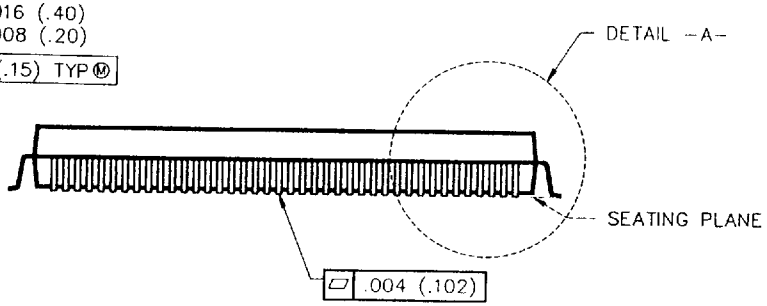
T-90-20





NOTES:
1. CONTROLLING DIMENSION IS MM.

DETAIL –A–



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