



VT82C598MVP

Apollo MVP3

66 / 75 / 83 / 100 MHz

**Single-Chip Socket-7 / Super-7 North Bridge
for Desktop and Mobile PC Systems
with AGP and PCI
plus Advanced ECC Memory Controller
supporting SDRAM, EDO, and FPG**

Preliminary Revision 1.0
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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	9/22/97	Initial release	DH
0.2	10/3/97	Updated pinouts & fixed pin definitions: DRAM, Power Management, Power Cleaned up AC Timing figures & fixed miscellaneous signal name typos Renamed ADS[1:0]# as GDS[1:0]# to reduce confusion with ADS# Renamed DCLKI / DCLKO as MCLKI / MCLKO	DH
0.3	10/9/97	Changed pinouts to be pin compatible with VT82C597 Apollo VP3 with the following differences: TA8 is changed to REQ4#, TA9 is changed to GNT4#, reserved pin is SUSCLK, reserved pin is SUSST#, GPAR is GPAR/CKRUN#. New CKE0-3# functions are shared on RAS4#, RAS5#, MAB0, and MAB1.	DH
0.4	10/10/97	Updated pinout definitions (rev 0.3 pin change was incomplete)	DH
0.5	11/7/98	Updated feature bullets and overview; added mobile system block diagram Added references and connection information for VT82C596 Mobile South Fixed typographical errors (0.35 micron technology not 0.5) Clarified power pin functions & fixed power plane naming Removed VTT function from VT82C598 (VT82C598AT feature only) Added HA25-27 strapping options and 2.5x and 3x clock mode descriptions Fixed typo in timing figure "2bank PBRAM Read 3111-2111" NA# signal Updated register definitions to reflect internal MVP3 register document rev 0.7 <ul style="list-style-type: none"> • Added I/O Port 22 • - Rx04[9] changed to RO - Rx50[4-3] 9 and 10-bit tag removed - COAST module detection table removed - Rx53[1-0] new bits added - Rx58[0, 4, 12] virtual channel support bits added - Rx63[1-0] "10", Rx68[4] changed to reserved - Rx68[1-0] changed to dipswitch read of system CPU bus frequency - Rx69 added (DRAM Clock Select) - Rx6C[5] added (MD-to-HD Pop) for 100MHz timing improvement - Rx6C[6] added (DRAM Start Cycle control) - Rx70[5-4, 2-1] bits changed/added, bit-0 changed to reserved - Rx71[5] added (CPU-to-IDE Posting), bit-5 changed to reserved - Rx72[7] changed wording to clarify function, bit-0 changed to reserved - Rx73[7], Rx78 (PMU Control), Rx88[2] added - Rx80[6-4] changed reserved bits to "always program to 0" - RxAC[3] added to allow RW of RxA4[1] - RxAC[1] added (AGP Arbitration Parking), bit-0 changed - RxFC and RxFE added (Back Door Control and Back Door Device ID) - Device 1 - Added Rx40[4-3, 1-0], Rx41[6, 1], Rx42[4] 	DH
0.6	12/5/97	Updated AC Electrical Specifications Fixed typos and clarified wording in pin descriptions: TA0-7, GCLK Removed incorrect note at start of "Device 0 Config Regs - Host Bridge" Removed incorrect notes at end of registers 68 and 6B (device 0)	DH
1.0	7/26/98	Removed 598 pinouts and renamed 598AT as 598MVP Removed DDR SDRAM-II, ESDRAM, & Virtual Chan from feature bullets Updated feature bullets and pin descriptions to correspond to production parts Updated AGP spec support from 1.0 to 2.0 (1x and 2x transfer modes) Fixed register definition errors: Device 0 Rx70[4], Rx73[0,4,7] Updated AC Elec Specs - HA & TA setup times for 100MHz CPU interface Removed DDR SDRAM timing Moved functional timing diagrams to separate document Fixed other miscellaneous typographical and formatting errors	DH

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VIA VT82C598MVP APOLLO MVP3

66 / 75 / 83 / 100 MHz

Single-Chip Socket-7 / Super-7 North Bridge
for Desktop and Mobile PC Systems
with AGP and PCI
plus Advanced ECC Memory Controller
supporting SDRAM, EDO, and FPG

- **AGP / PCI / ISA Mobile and Deep Green PC Ready**

- Supports 3.3V and sub-3.3V interface to CPU
- Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
- PC-97 compatible using VIA VT82C586B (208-pin PQFP) south bridge chip with ACPI Power Management for cost-efficient desktop applications
- Modular power management and clock control for mobile system applications
- Combine with VIA VT82C596 (Intel PIIIX4 pin compatible 324-pin BGA) “Mobile South” south bridge chip for state-of-the-art mobile applications

- **High Integration**

- Single chip implementation for 64-bit Socket-7-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
- **Apollo MVP3** Chipset: **VT82C598MVP** system controller and **VT82C586B** PCI to ISA bridge
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip

- **High Performance CPU Interface**

- Supports all Socket-7 processors including 64-bit Intel Pentium™ / Pentium™ with MMX™, AMD 6_K86™ (K6™), Cyrix/IBM 6_X86™ / 6_X86MX™, and IDT/Centaur C6 CPUs
- 66 / 75 / 83 / 100 MHz CPU external bus speed (internal 300MHz and above)
- Built-in deskew DLL (Delay Lock Loop) circuitry for optimal skew control within and between clocking regions
- Cyrix/IBM 6_X86 linear burst support
- AMD 6_K86™ write allocation support
- System management interrupt, memory remap and STPCLK mechanism

- **Advanced Cache Controller**

- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support
- Flexible cache size: 0K / 256K / 512K / 1M / 2MB
- 32 byte line size to match the primary cache
- Integrated 8-bit tag comparator
- 3-1-1-1-1-1-1 back to back read timing for PBSRAM access up to 100 MHz
- Tag timing optimized (less than 4ns setup time) to allow external tag SRAM implementation for most flexible cache organization
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM & PCI bus post write buffers up to 100 MHz
- Supports CPU single read cycle L2 allocation
- System and video BIOS cacheable and write-protect
- Programmable cacheable region

• Full Featured Accelerated Graphics Port (AGP) Controller

- Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

<u>PCI</u>	<u>AGP</u>	<u>CPU</u>	<u>DRAM</u>	<u>Mode</u>	
33 MHz	66 MHz	100 MHz	100 MHz	3x synchronous	(DRAM uses CPU clock)
33 MHz	66 MHz	83 MHz	83 MHz	2.5x pseudo-synchronous	(DRAM uses CPU clock)
30 MHz	60 MHz	75 MHz	75 MHz	2.5x pseudo-synchronous	(DRAM uses CPU clock)
33 MHz	66 MHz	66 MHz	66 MHz	2x synchronous	(DRAM uses CPU clock)
33 MHz	66 MHz	100 MHz	66 MHz	3x synchronous	(DRAM uses AGP clock)
33 MHz	66 MHz	83 MHz	66 MHz	2.5x pseudo-synchronous	(DRAM uses AGP clock)
30 MHz	60 MHz	75 MHz	66 MHz	2.5x pseudo-synchronous	(DRAM uses AGP clock)
33 MHz	66 MHz	66 MHz	66 MHz	2x synchronous	(DRAM uses AGP clock)
- AGP v2.0 compliant (1x and 2x transfer modes)
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
- Supports 133MHz 2X mode for AD and SBA signalling
- Pipelined split-transaction long-burst transfers up to 533 MB/sec
- Eight level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (128 bytes)
- Sixteen level (quadwords) write data FIFO (64 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)
 - One level TLB structure
 - Sixteen entry fully associative page table
 - LRU replacement scheme
 - Independent GART lookup control for host / AGP / PCI master accesses
- Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support

• Concurrent PCI Bus Controller

- PCI buses are synchronous / pseudo-synchronous to host CPU bus
- 33 MHz operation on the primary PCI bus
- 66 MHz PCI operation on the AGP bus
- PCI-to-PCI bridge configuration on the 66MHz PCI bus
- Supports up to five PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- PCI master snoop ahead and snoop filtering
- Six levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
- Supports L1/L2 write-back merged with PCI master post-write to minimize DRAM utilization
- Delay transaction from PCI master reading DRAM
- Read caching for PCI master reading DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**

- DRAM interface synchronous with host CPU (66/75/83/100 MHz) or AGP (66MHz) for most flexible configuration
- Concurrent CPU and AGP access
- FP, EDO, and SDRAM
 - 66MHz and 100MHz (PC100) SDRAM support
- Different DRAM types may be used in mixed combinations
- Different DRAM timing for each bank
- Dynamic Clock Enable (CKE) control for SDRAM power reduction in mobile and desktop systems
- Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
- 6 banks up to 768MB DRAMs
- Flexible row and column addresses
- 64-bit data width only
- 3.3V DRAM interface with 5V-tolerant inputs
- Programmable I/O drive capability for MA, command, and MD signals
- Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support
- Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
- Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
- Four quadwords of CPU/cache to DRAM read prefetch buffers
- Concurrent DRAM writeback
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- 5-2-2-2-2-2-2-2 back-to-back accesses for EDO DRAM
- 6-1-1-1-2-1-1-1 back-to-back accesses for SDRAM
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate and refresh on populated banks only
- CAS before RAS or self refresh

- **Mobile System Support**

- Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
- PCI and AGP bus clock run and clock generator control
- VTT suspend power plane preserves memory data
- Suspend-to-DRAM and Self-Refresh operation
- New VIA BGA VT82C596 “Mobile South” south bridge chip available soon for support of new mobile features
- Dynamic clock gating for internal functional blocks for power reduction during normal operation
- Low-leakage I/O pads

- **Built-in NAND-tree pin scan test capability**

- **3.3V, 0.35um, high speed / low power CMOS process**

- **35 x 35 mm, 476 pin BGA Package**

OVERVIEW

The *Apollo MVP3* is a high performance, cost-effective and energy efficient chip set for the implementation of AGP / PCI / ISA desktop and notebook personal computer systems from 66 MHz to 100 MHz based on 64-bit Socket-7 (Intel Pentium and Pentium MMX; AMD K6; Cyrix / IBM 6_x86 / 6_x86MX, and IDT / Centaur C6/WinChip) super-scalar processors.

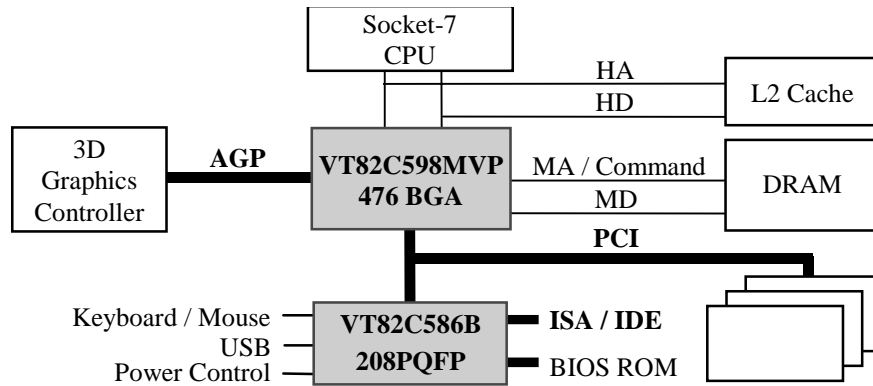


Figure 1. Apollo MVP3 System Block Diagram Using the VT82C586B South Bridge

The Apollo-MVP3 chip set consists of the VT82C598MVP system controller (476 pin BGA) and the VT82C586B PCI to ISA bridge (208 pin PQFP). The system controller provides superior performance between the CPU, optional synchronous cache, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation. For pipelined burst synchronous SRAMs, 3-1-1-1-1-1-1 timing can be achieved for both read and write transactions at 100 MHz. Tag timing is specially optimized internally (less than 4 nsec setup time) to allow implementation of L2 cache using an external tag for the most flexible cache organization (0K / 256K / 512K / 1M / 2M). Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers with concurrent write-back capability are included on chip to speed up cache read and write miss cycles.

The VT82C598MVP supports six banks of DRAMs up to 768MB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, and Synchronous DRAM (SDRAM) in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 100 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM Controller can run at either the host CPU bus frequency (66 / 75 / 83 / 100 MHz) or at the AGP bus frequency (66 MHz) with built-in deskew DLL timing control. The VT82C598MVP allows implementation of the most flexible, reliable, and high-performance DRAM interface.

The VT82C598MVP also supports AGP v2.0 compatibility for maximum bus utilization including 2x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU/AGP/PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT82C598MVP supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The VT82C586B PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C586B also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter and gather capability and extension to UltraDMA-33 / ATA-33 for 33MB/sec transfer rate, integrated USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface. Using the low-cost 208-pin PQFP-packaged VT82C586B south bridge chip, a complete main board can be implemented with only four TTLs.

For sophisticated notebook implementations, the VT82C598MVP provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the 324-pin Ball Grid Array VT82C596 "Mobile South" chip, a complete notebook PC main board can be implemented with no external TTLs.

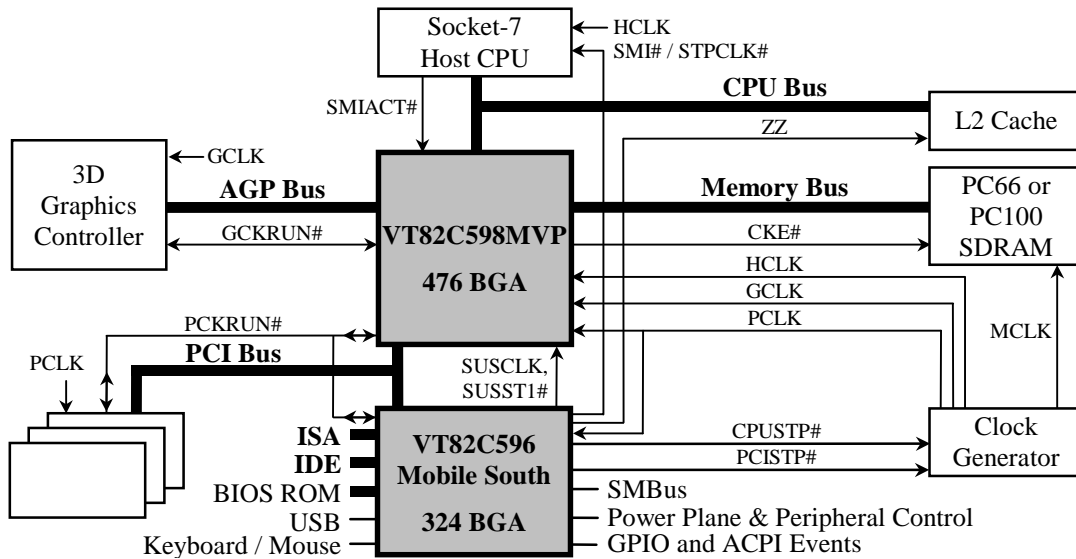


Figure 2. Apollo MVP3 System Block Diagram Using the VT82C596 Mobile South Bridge

The Apollo MVP3 chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / ISA computer systems.

PINOUTS – VT82C598MVP

Figure 3. VT82C598MVP Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	SBA5	SBA3	GPIPE#	GREQ#	PCRUN#	SBA0	MD0	MD33	MD35	MD37	MD39	MD41	MD12	MD46	MECC4	SCASC#	CAS0#	SRASC#	MAB1	MA5	MA9	MA13	RAS4#	RAS1#	CAS2#	CAS3#
B	SBA6	SBS#	GRBF#	ST1	GGNT#	GCRUN#	MD32	MD2	MD4	MD6	MD8	MD10	MD44	MD15	MECC1	SCASB#	CAS4#	SRASB#	MA2	MA6	MA10	MAA0	RAS3#	RAS0#	CAS6#	CAS7#
C	GD31	SBA7	SBA1	ST0	SBA2	SUST#	MD1	MD34	MD36	MD38	MD40	MD42	MD13	MD47	MECC5	SCASA#	CAS5#	SRASA#	MA3	MA7	MA11	MAA1	RAS2#	SWEC#	SWEB#	SWEA#
D	GD28	GD30	GD29	GCLK	SBA4	SUCLK	MD3	GND	MD5	MD7	MD9	MD11	MD45	MECC0	DS0#	DS2#	CAS1#	MAB0	MA4	MA8	MA12	RAS5#	MECC7	MECC3	MECC6	MECC2
E	GD24	GD26	GDS1#	GD27	VCCI	GND	GND	ST2	VCC	VCC	VCC	MD43	MD14	GND	GND	GND	VCC	VCC	VCC	MVREF	5VREF	GND	MD49	MD17	MD48	MD16
F	GBE3#	GD25	GD21	GD23	GVREF	VCCI	GND	VTT	9	10	11	12	13	14	15	16	17	18	VTT	GND	GND	VCCI	MD51	MD19	MD50	MD18
G	GD20	GD22	GBE2#	GD17	VCC	GND	G7	8	Total = 476 Pins						Data	Control			Address	Control	GND	DS1#	MD53	MD21	MD52	MD20
H	GD16	GD18	GD19	GDSEL#	VCC	VCC	H	9	10	11	12	13	14	15	16	17	18	Data	VTT	DS3#	MD55	MD23	MD54	MD22		
J	GTRDY#	GIRDY#	GFRM#	GBE1#	VCC	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	VCC	MD57	MD25	MD56	MD24
K	GD13	GD15	GSTOP#	GD14	AVCC	K	AGP Pins	K	K10	11	12	13	14	15	16	K17	K	Mem Pins	K	VCC	MD59	MD27	MD58	MD26		
L	GD9	GD12	GD11	GD10	GND	L	L	L	L	GND	GND	GND	GND	GND	GND	L	L	L	L	VCC	MD61	MD29	MD60	MD28		
M	GD6	GD8	GBE0#	GDS0#	GND	M	M	M	M	GND	GND	GND	GND	GND	GND	M	M	M	M	TA2	MD63	MD31	MD62	MD30		
N	GD2	GD4	GD7	GD5	AGND	N	N	N	N	GND	GND	GND	GND	GND	GND	N	N	N	N	TA5	TA4	TA3	TA0	TA1		
P	GD3	GD1	GD0	GNT3#	HCLK	P	P	P	P	GND	GND	GND	GND	GND	GND	P	P	P	Cache	P	GND	REQ4#	TWE#	TA6	TA7	
R	GNT1#	REQ2#	GNT2#	REQ3#	VCC	R	R	R	R	GND	GND	GND	GND	GND	GND	R	R	R	R	R	GND	BWE#	CCS1#	COE1#	GNT4#	
T	LOCK#	REQ0#	GNT0#	REQ1#	VCC	T	PCI Pins	T	T	GND	GND	GND	GND	GND	GND	T	T	T	T	T	HD1	HD0	CADV#	CADS#	GWE#	
U	AD28	AD29	AD30	AD31	VCC	U	U	U	U10	11	12	13	14	15	16	U17	U	U	Data	U	HVCC	HD5	HD4	HD3	HD2	
V	AD24	AD25	AD26	AD27	VCC	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	HVCC	HD9	HD8	HD7	HD6	
W	AD21	AD22	AD23	CBE3#	PCLK	GND	W	9	10	11	12	13	14	15	16	17	18	W	GND	HD14	HD13	HD12	HD11	HD10		
Y	AD17	AD18	AD19	AD20	GND	GND	Y7	8	Control	Address	CPU Pins					Byte Enables	19	Y20	GND	HD19	HD18	HD17	HD16	HD15		
AA	IRDY#	FRM#	CBE2#	AD16	GND	VCCI	VCC	VCC	9	10	11	12	13	14	15	16	17	18	GND	GND	GND	GND	HD23	HD22	HD21	HD20
AB	STOP#	DSEL#	TRDY#	SERR#	VCCI	VCC	VCC	5VREF	HVCC	HVCC	HA25	HA30	GND	GND	HA8	BE5#	HVCC	HVCC	HVCC	HD52	VCCI	GND	HD27	HD26	HD25	HD24
AC	CBE1#	PAR	AD15	AD14	AD2	PREQ#	RESET#	BRDY#	M/IO#	HA27	HA28	HA17	HA14	HA3	HA7	BE6#	BE1#	HD61	HD57	HD53	HD48	HD44	HD31	HD30	HD29	HD28
AD	AD13	AD12	AD11	AD5	AD1	PGNT#	ADS#	NA#	CACHE#	HA26	HA29	HA18	HA15	HA11	HA6	BE7#	BE2#	HD62	HD58	HD54	HD49	HD45	HD41	HD38	HD33	HD32
AE	AD10	AD9	AD7	AD4	AD0	EADS#	D/C#	BOFF#	AHOLD	HA24	HA31	HA19	HA16	HA12	HA5	HA10	BE3#	HD63	HD59	HD55	HD50	HD46	HD42	HD39	HD36	HD34
AF	AD8	CBE0#	AD6	AD3	HLOCK#	W/R#	HITM#	SMIACK#	KEN#	HA23	HA21	HA22	HA20	HA13	HA4	HA9	BE4#	BE0#	HD60	HD56	HD51	HD47	HD43	HD40	HD37	HD35

Figure 4. VT82C598MVP Pin List (Numerical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A01	I SBA5	D03	IO GD29	H03	IO GD19	P03	IO GD00	Y03	IO AD19	AD03	IO AD11
A02	I SBA3	D04	I GCLK	H04	IO GDSEL#	P04	O GNT3#	Y04	IO AD20	AD04	IO AD05
A03	I GPIPE#	D05	I SBA4	H05	P VCC	P05	I HCLK	Y05	P GND	AD05	IO AD01
A04	I GREO#	D06	I SUCLK	H06	P VCC	P11	P GND	Y06	P GND	AD06	O PGNT#
A05	IO PCKRUN#	D07	IO MD03	H21	P VTT	P12	P GND	Y21	P GND	AD07	IO ADS#
A06	I SBA0	D08	P GND	H22	O DS3#(Reserved)	P13	P GND	Y22	IO HD19	AD08	O NA#
A07	IO MD00	D09	IO MD05	H23	IO MD55	P14	P GND	Y23	IO HD18	AD09	I CACHE#
A08	IO MD33	D10	IO MD07	H24	IO MD23	P15	P GND	Y24	IO HD17	AD10	IO HA26
A09	IO MD35	D11	IO MD09	H25	IO MD54	P16	P GND	Y25	IO HD16	AD11	IO HA29
A10	IO MD37	D12	IO MD11	H26	IO MD22	P22	P GND	Y26	IO HD15	AD12	IO HA18
A11	IO MD39	D13	IO MD45	J01	IO GTRDY#	P23	I REO4#	AA01	IO IRDY#	AD13	IO HA15
A12	IO MD41	D14	IO MECC0	J02	IO GIRDY#	P24	O TWE#	AA02	IO FRAME#	AD14	IO HA11
A13	IO MD12	D15	O DS0#(Reserved)	J03	IO GFRM#	P25	IO TA6	AA03	IO CBE2#	AD15	IO HA06
A14	IO MD46	D16	O DS2#(Reserved)	J04	IO GBE1#	P26	IO TA7	AA04	IO AD16	AD16	IO BE7#
A15	IO MECC4	D17	O CAS1# / DOM1#	J05	P VCC	R01	O GNT1#	AA05	P GND	AD17	IO BE2#
A16	O SCASC#	D18	O MAB0	J22	P VCC	R02	I REO2#	AA06	P VCCI	AD18	IO HPD62
A17	O CAS0# / DOM0#	D19	O MA04	J23	IO MD57	R03	O GNT2#	AA07	P VCC	AD19	IO HD58
A18	O SRASC#	D20	O MA08	J24	IO MD25	R04	I REO3#	AA08	P VCC	AD20	IO HD54
A19	O MAB1	D21	O MA12	J25	IO MD56	R05	P VCC	AA19	P GND	AD21	IO HD49
A20	O MA05	D22	O RAS5# / CS5#	J26	IO MD24	R11	P GND	AA20	P GND	AD22	IO HD45
A21	O MA09	D23	IO MECC7	K01	IO GD13	R12	P GND	AA21	P GND	AD23	IO HD41
A22	O MA13	D24	IO MECC3	K02	IO GD15	R13	P GND	AA22	P GND	AD24	IO HD38
A23	O RAS4# / CS4#	D25	IO MECC6	K03	IO GSTOP#	R14	P GND	AA23	IO HD23	AD25	IO HD33
A24	O RAS1# / CS1#	D26	IO MECC2	K04	IO GD14	R15	P GND	AA24	IO HD22	AD26	IO HD32
A25	O CAS2# / DOM2#	E01	IO GD24	K05	P AVCC	R16	P GND	AA25	IO HD21	AE01	IO AD10
A26	O CAS3# / DOM3#	E02	IO GD26	K22	P VCC	R22	P GND	AA26	IO HD20	AE02	IO AD09
B01	I SBA6	E03	IO GDS1#	K23	IO MD59	R23	O BWE#	AB01	IO STOP#	AE03	IO AD07
B02	I SBS#	E04	IO GD27	K24	IO MD27	R24	O CCS1#	AB02	IO DEVSEL#	AE04	IO AD04
B03	I GRBF#	E05	P VCCI	K25	IO MD58	R25	O COE1#	AB03	IO TRDY#	AE05	IO AD00
B04	O ST1	E06	P GND	K26	IO MD26	R26	O GNT4#	AB04	IO SERR#	AE06	O EADS#
B05	O GGNT#	E07	P GND	L01	IO GD09	T01	IO LOCK#	AB05	P VCCI	AE07	IO D/C#
B06	IO GCKRUN#	E08	O ST2	L02	IO GD12	T02	I REO0#	AB06	P VCC	AE08	O BOFF#
B07	IO MD32	E09	P VCC	L03	IO GD11	T03	O GNT0#	AB07	P VCC	AE09	O AHOLD
B08	IO MD02	E10	P VCC	L04	IO GD10	T04	I REO1#	AB08	P SVREF	AE10	IO HA24
B09	IO MD04	E11	P VCC	L05	P GND	T05	P VCC	AB09	P HVCC	AE11	IO HA31
B10	IO MD06	E12	IO MD43	L11	P GND	T11	P GND	AB10	P HVCC	AE12	IO HA19
B11	IO MD08	E13	IO MD14	L12	P GND	T12	P GND	AB11	IO HA25	AE13	IO HA16
B12	IO MD10	E14	P GND	L13	P GND	T13	P GND	AB12	IO HA30	AE14	IO HA12
B13	IO MD44	E15	P GND	L14	P GND	T14	P GND	AB13	P GND	AE15	IO HA05
B14	IO MD15	E16	P GND	L15	P GND	T15	P GND	AB14	P GND	AE16	IO HA10
B15	IO MECC1	E17	P VCC	L16	P GND	T16	P GND	AB15	IO HA08	AE17	IO BE3#
B16	O SCASB#	E18	P VCC	L22	P VCC	T22	IO HD01	AB16	IO BE5#	AE18	IO HD63
B17	O CAS4# / DOM4#	E19	P VCC	L23	IO MD61	T23	IO HD00	AB17	P HVCC	AE19	IO HD59
B18	O SRASB#	E20	P MVREF	L24	IO MD29	T24	O CADV#	AB18	P HVCC	AE20	IO HD55
B19	O MA02	E21	P SVREF	L25	IO MD60	T25	O CADS#	AB19	P HVCC	AE21	IO HD50
B20	O MA06	E22	P GND	L26	IO MD28	T26	O GWE#	AB20	IO HD52	AE22	IO HD46
B21	O MA10	E23	IO MD49	M01	IO GD06	U01	IO AD28	AB21	P VCCI	AE23	IO HD42
B22	O MAA0	E24	IO MD17	M02	IO GD08	U02	IO AD19	AB22	P GND	AE24	IO HD39
B23	O RAS3# / CS3#	E25	IO MD48	M03	IO GBE0#	U03	IO AD30	AB23	IO HD27	AE25	IO HD36
B24	O RAS0# / CS0#	E26	IO MD16	M04	IO GDS0#	U04	IO AD31	AB24	IO HD26	AE26	IO HD34
B25	O CAS6# / DOM6#	F01	IO GBE3#	M05	P GND	U05	P VCC	AB25	IO HD25	AF01	IO AD08
B26	O CAS7# / DOM7#	F02	IO GD25	M11	P GND	U22	P HVCC	AB26	IO HD24	AF02	IO CBE0#
C01	IO GD31	F03	IO GD21	M12	P GND	U23	IO HD05	AC01	IO CBE1#	AF03	IO AD06
C02	I SBA7	F04	IO GD23	M13	P GND	U24	IO HD04	AC02	IO PAR	AF04	IO AD03
C03	I SBA1	F05	P GVREF	M14	P GND	U25	IO HD03	AC03	IO AD15	AF05	I HLOCK#
C04	O ST0	F06	P VCCI	M15	P GND	U26	IO HD02	AC04	IO AD14	AF06	IO W/R#
C05	I SBA2	F07	P GND	M16	P GND	V01	IO AD24	AC05	IO AD02	AF07	I HITM#
C06	I SUST#	F08	P VTT	M22	IO TA2	V02	IO AD25	AC06	I PREQ#	AF08	I SMIAC#
C07	IO MD01	F19	P VTT	M23	IO MD63	V03	IO AD26	AC07	I RESET#	AF09	O KEN#
C08	IO MD34	F20	P GND	M24	IO MD31	V04	IO AD27	AC08	IO BRDY#	AF10	IO HA23
C09	IO MD36	F21	P GND	M25	IO MD62	V05	P VCC	AC09	IO M/IO#	AF11	IO HA21
C10	IO MD38	F22	P VCCI	M26	IO MD30	V22	P HVCC	AC10	IO HA27	AF12	IO HA22
C11	IO MD40	F23	IO MD51	N01	IO GD02	V23	IO HD09	AC11	IO HA28	AF13	IO HA20
C12	IO MD42	F24	IO MD19	N02	IO GD04	V24	IO HD08	AC12	IO HA17	AF14	IO HA13
C13	IO MD13	F25	IO MD50	N03	IO GD07	V25	IO HD07	AC13	IO HA14	AF15	IO HA04
C14	IO MD47	F26	IO MD18	N04	IO GD05	V26	IO HD06	AC14	IO HA03	AF16	IO HA09
C15	IO MECC5	G01	IO GD20	N05	P AGND	W01	IO AD21	AC15	IO HA07	AF17	IO BE4#
C16	O SCASA#	G02	IO GD22	N11	P GND	W02	IO AD22	AC16	IO BE6#	AF18	IO BE0#
C17	O CAS5# / DOM5#	G03	IO GBE2#	N12	P GND	W03	IO AD23	AC17	IO BE1#	AF19	IO HD60
C18	O SRASA#	G04	IO GD17	N13	P GND	W04	IO CBE3#	AC18	IO HD61	AF20	IO HD56
C19	O MA03	G05	P VCC	N14	P GND	W05	I PCLK	AC19	IO HD57	AF21	IO HD51
C20	O MA07	G06	P GND	N15	P GND	W06	P GND	AC20	IO HD53	AF22	IO HD47
C21	O MA11	G21	P GND	N16	P GND	W21	P GND	AC21	IO HD48	AF23	IO HD43
C22	O MAA1	G22	O DS1#(Reserved)	N22	IO TA5	W22	IO HD14	AC22	IO HD44	AF24	IO HD40
C23	O RAS2# / CS2#	G23	IO MD53	N23	IO TA4	W23	IO HD13	AC23	IO HD31	AF25	IO HD37
C24	O SWEC# / MWE#	G24	IO MD21	N24	IO TA3	W24	IO HD12	AC24	IO HD30	AF26	IO HD35
C25	O SWEB# / MWEB#	G25	IO MD52	N25	IO TA0	W25	IO HD11	AC25	IO HD29		
C26	O SWEA# / MWEA#	G26	IO MD20	N26	IO TA1	W26	IO HD10	AC26	IO HD28		
D01	IO GD28	H01	IO GD16	P01	IO GD03	Y01	IO AD17	AD01	IO AD13		
D02	IO GD30	H02	IO GD18	P02	IO GD01	Y02	IO AD18	AD02	IO AD12		

Figure 5. VT82C598MVP Pin List (Alphabetical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
E21	P 5VREF	P03	IO GD00	R14	P GND	Y26	IO HD15	B08	IO MD02	B23	O RAS3# / CS3#
AB08	P 5VREF	P02	IO GD01	R15	P GND	Y25	IO HD16	D07	IO MD03	A23	O RAS4# / CS4#
AE05	IO AD00	N01	IO GD02	R16	P GND	Y24	IO HD17	B09	IO MD04	D22	O RAS5# / CS5#
AD05	IO AD01	P01	IO GD03	R22	P GND	Y23	IO HD18	D09	IO MD05	T02	I REQ0#
AC05	IO AD02	N02	IO GD04	T11	P GND	Y22	IO HD19	B10	IO MD06	T04	I REQ1#
AF04	IO AD03	N04	IO GD05	T12	P GND	AA26	IO HD20	D10	IO MD07	R02	I REQ2#
AE04	IO AD04	M01	IO GD06	T13	P GND	AA25	IO HD21	B11	IO MD08	R04	I REQ3#
AD04	IO AD05	N03	IO GD07	T14	P GND	AA24	IO HD22	D11	IO MD09	P23	I REQ4#
AF03	IO AD06	M02	IO GD08	T15	P GND	AA23	IO HD23	B12	IO MD10	AC07	I RESET#
AE03	IO AD07	L01	IO GD09	T16	P GND	AB26	IO HD24	D12	IO MD11	A06	I SBA0
AF01	IO AD08	L04	IO GD10	W06	P GND	AB21	IO HD25	A13	IO MD12	C03	I SBA1
AE02	IO AD09	L03	IO GD11	W21	P GND	AB24	IO HD26	C13	IO MD13	C05	I SBA2
AE01	IO AD10	L02	IO GD12	Y05	P GND	AB23	IO HD27	E13	IO MD14	A02	I SBA3
AD03	IO AD11	K01	IO GD13	Y06	P GND	AC26	IO HD28	B14	IO MD15	D05	I SBA4
AD02	IO AD12	K04	IO GD14	Y21	P GND	AC25	IO HD29	E26	IO MD16	A01	I SBA5
AD01	IO AD13	K02	IO GD15	AA05	P GND	AC24	IO HD30	E24	IO MD17	B01	I SBA6
AC04	IO AD14	H01	IO GD16	AA19	P GND	AC23	IO HD31	F26	IO MD18	C02	I SBA7
AC03	IO AD15	G04	IO GD17	AA20	P GND	AD26	IO HD32	F24	IO MD19	B02	I SBS#
AA04	IO AD16	H02	IO GD18	AA21	P GND	AD25	IO HD33	G26	IO MD20	C16	O SCASA#
Y01	IO AD17	H03	IO GD19	AA22	P GND	AE26	IO HD34	G24	IO MD21	B16	O SCASB#
Y02	IO AD18	G01	IO GD20	AB13	P GND	AF26	IO HD35	H26	IO MD22	A16	O SCASC#
Y03	IO AD19	F03	IO GD21	AB14	P GND	AE25	IO HD36	H24	IO MD23	AB04	IO SEERR#
Y04	IO AD20	G02	IO GD22	AB22	P GND	AF25	IO HD37	J26	IO MD24	AF08	I SMIACK#
W01	IO AD21	F04	IO GD23			AD24	IO HD38	J24	IO MD25	C18	O SRASA#
W02	IO AD22	E01	IO GD24	T03	O GNT0#	AE24	IO HD39	K26	IO MD26	B18	O SRASB#
W03	IO AD23	F02	IO GD25	R01	O GNT1#	AF24	IO HD40	K24	IO MD27	A18	O SRASC#
V01	IO AD24	E02	IO GD26	R03	O GNT2#	AD23	IO HD41	L26	IO MD28	C04	O ST0
V02	IO AD25	E04	IO GD27	P04	O GNT3#	AE23	IO HD42	L24	IO MD29	B04	O ST1
V03	IO AD26	D01	IO GD28	R26	O GNT4#	AF23	IO HD43	M26	IO MD30	E08	O ST2
V04	IO AD27	D03	IO GD29	A03	I GPIPE#	AC22	IO HD44	M24	IO MD31	AB01	IO STOP#
U01	IO AD28	D02	IO GD30	B03	I GRBF#	AD22	IO HD45	B07	IO MD32	D06	I SUCLK
U02	IO AD29	C01	IO GD31	A04	I GREQ#	AE22	IO HD46	A08	IO MD33	C06	I SUST#
U03	IO AD30	M04	IO GDS0#	K03	IO GSTOP#	AF22	IO HD47	C08	IO MD34	C26	O SCASA# / MWEA#
U04	IO AD31	E03	IO GDS1#	J01	IO GTRDY#	AC21	IO HD48	A09	IO MD35	C25	O SWEBS# / MWEB#
AD07	IO ADS#	H04	IO GDSEL#	F05	P GVREF	AD21	IO HD49	C09	IO MD36	C24	O SWEC# / MWECS#
N05	P AGND	J03	IO GFRM#	T26	O GWE#	AE21	IO HD50	A10	IO MD37	N25	IO TA0
AE09	O AHOLD	B05	O GGNT#	AC14	IO HA03	AF21	IO HD51	C10	IO MD38	N26	IO TA1
K05	P AVCC	J02	IO GIRDY#	AF15	IO HA04	AB20	IO HD52	A11	IO MD39	M22	IO TA2
AF18	IO BE0#	D08	P GND	AE15	IO HA05	AC20	IO HD53	C11	IO MD40	N24	IO TA3
AC17	IO BE1#	E06	P GND	AC15	IO HA07	AD20	IO HD54	A12	IO MD41	N23	IO TA4
AD17	IO BE2#	E07	P GND	AB15	IO HA08	AE20	IO HD55	C12	IO MD42	N22	IO TA5
AE17	IO BE3#	E14	P GND	AF16	IO HA09	AF20	IO HD56	E12	IO MD43	P25	IO TA6
AF17	IO BE4#	E15	P GND	AE16	IO HA10	AC19	IO HD57	B13	IO MD44	P26	IO TA7
AB16	IO BE5#	E16	P GND	AD14	IO HA11	AD19	IO HD58	D13	IO MD45	AB03	IO TRDY#
AC16	IO BE6#	E22	P GND	AE14	IO HA12	AE19	IO HD59	A14	IO MD46	P24	O TWE#
AD16	IO BE7#	F07	P GND	AF14	IO HA13	AF19	IO HD60	C14	IO MD47	E09	P VCC
AE08	O BOFF#	F20	P GND	AC13	IO HA14	AC18	IO HD61	E25	IO MD48	E10	P VCC
AC08	IO BRDY#	F21	P GND	AD13	IO HA15	AD18	IO HD62	E23	IO MD49	E11	P VCC
R23	O BWE#	G06	P GND	AE13	IO HA16	AE18	IO HD63	F25	IO MD50	E17	P VCC
AD09	I CACHE#	G21	P GND	AC12	IO HA17	AF07	I HITM#	F23	IO MD51	E18	P VCC
T25	O CADS#	L05	P GND	AD12	IO HA18	AF05	I HLOCK#	G25	IO MD52	E19	P VCC
T24	O CADV#	L11	P GND	AE12	IO HA19	U22	P HVCC	G23	IO MD53	G05	P VCC
A17	O CAS0# / DQM0#	L12	P GND	AF13	IO HA20	V22	P HVCC	H25	IO MD54	H05	P VCC
D17	O CAS1# / DQM1#	L13	P GND	AF11	IO HA21	AB09	P HVCC	H23	IO MD55	H06	P VCC
A25	O CAS2# / DQM2#	L14	P GND	AF12	IO HA22	AB10	P HVCC	J25	IO MD56	J05	P VCC
A26	O CAS3# / DQM3#	L15	P GND	AF10	IO HA23	AB17	P HVCC	J23	IO MD57	J22	P VCC
B17	O CAS4# / DQM4#	L16	P GND	AE10	IO HA24	AB18	P HVCC	K25	IO MD58	K22	P VCC
C17	O CAS5# / DQM5#	M05	P GND	AB11	IO HA25	AB19	P HVCC	K23	IO MD59	L22	P VCC
B25	O CAS6# / DQM6#	M11	P GND	AD10	IO HA26	AA01	IO IRDY#	L25	IO MD60	R05	P VCC
B26	O CAS7# / DQM7#	M12	P GND	AC10	IO HA27	AF09	O KEN#	L23	IO MD61	T05	P VCC
AF02	IO CBE0#	M13	P GND	AC11	IO HA28	T01	IO LOCK#	M25	IO MD62	U05	P VCC
AC01	IO CBE1#	M14	P GND	AD11	IO HA29	AC09	IO M/IO#	M23	IO MD63	V05	P VCC
AA03	IO CBE2#	M15	P GND	AB12	IO HA30	B19	O MA02	D14	IO MECC0	AA07	P VCC
W04	IO CBE3#	M16	P GND	AE11	IO HA31	C19	O MA03	B15	IO MECC1	AA08	P VCC
R24	O CCS1#	N11	P GND	P05	I HCLK	D19	O MA04	D26	IO MECC2	AB06	P VCC
R25	O COE1#	N12	P GND	T23	IO HD00	A20	O MA05	D24	IO MECC3	AB07	P VCC
AE07	IO D/C#	N13	P GND	T22	IO HD01	B20	O MA06	A15	IO MECC4	E05	P VCCI
AB02	IO DEVSEL#	N14	P GND	U26	IO HD02	C20	O MA07	C15	IO MECC5	F06	P VCCI
D15	O DS0# (Reserved)	N15	P GND	U25	IO HD03	D20	O MA08	D25	IO MECC6	F22	P VCCI
G22	O DS1# (Reserved)	N16	P GND	U24	IO HD04	A21	O MA09	D23	IO MECC7	AA06	P VCCI
D16	O DS2# (Reserved)	P11	P GND	U23	IO HD05	B21	O MA10	E20	P MVREF	AB05	P VCCI
H22	O DS3# (Reserved)	P12	P GND	V26	IO HD06	C21	O MA11	AD08	O NA#	AB21	P VCCI
AE06	O EADS#	P13	P GND	V25	IO HD07	D21	O MA12	AC02	IO PAR	F08	P VTT
AA02	IO FRAME#	P14	P GND	V24	IO HD08	A22	O MA13	A05	IO PCKRUN#	F19	P VTT
M03	IO GBE0#	P15	P GND	V23	IO HD09	B22	O MAA0	W05	I PCLK	H21	P VTT
J04	IO GBE1#	P16	P GND	W26	IO HD10	C22	O MAA1	AD06	O PGNT#	AF06	IO W/R#
G03	IO GBE2#	P22	P GND	W25	IO HD11	D18	O MAB0	AC06	I PREQ#		
F01	IO GBE3#	R11	P GND	W24	IO HD12	A19	O MAB1	B24	O RAS0# / CS0#		
B06	IO GCKRUN#	R12	P GND	W23	IO HD13	A07	IO MD00	A24	O RAS1# / CS1#		
D04	I GCLK	R13	P GND	W22	IO HD14	C07	IO MD01	C23	O RAS2# / CS2#		

PIN DESCRIPTIONS

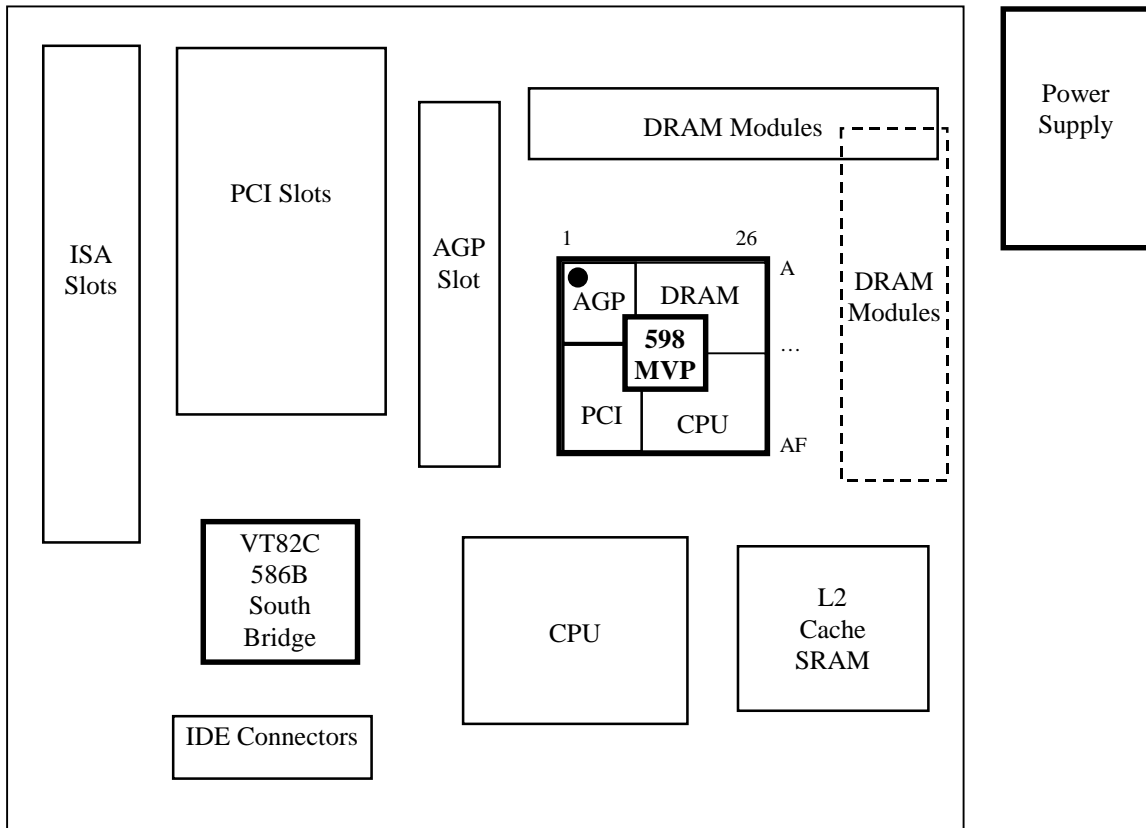
Table 1. VT82C598MVP Pin Descriptions

CPU Interface			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
ADS#	AD7	B	Address Strobe. The CPU asserts ADS# in T1 of the CPU bus cycle to initiate a command
M/IO#	AC9	B	Memory / IO Command Indicator
W/R#	AF6	B	Write / Read Command Indicator
D/C#	AE7	B	Data / Control Command Indicator
BRDY#	AC8	B	Bus Ready. The VT82C598MVP asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
EADS#	AE6	O	External Address Strobe. Asserted by the VT82C598MVP to inquire the L1 cache when serving PCI master accesses to main memory.
KEN# / INV	AF9	O	Cache Enable / Invalidate. KEN# / INV functions as both the KEN# signal during CPU read cycles and the INV signal during L1 cache snoop cycles.
HITM#	AF7	I	Hit Modified. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	AF5	I	Host Lock. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
CACHE#	AD9	I	Cacheable Indicator. Asserted by the CPU during a read cycle to indicate the CPU can perform a burst line fill. Asserted by the CPU during a write cycle to indicate that the CPU will perform a burst write-back cycle.
AHOLD	AE9	O	Address Hold. The VT82C598MVP asserts AHOLD when a PCI master is accessing main memory. AHOLD is held for the duration of the PCI burst transfer.
NA#	AD8	O	Next Address Indicator.
BOFF#	AE8	O	Back Off. Asserted by the VT82C598MVP when required to terminate a CPU cycle that was in progress.
SMIACT#	AF8	I	System Management Interrupt Active. This is asserted by the CPU when it is in system management mode as a result of SMI.
BE[7:0]#	AD16, AC16, AB16, AF17, AE17, AD17, AC17, AF18	B	Byte Enables. The CPU byte enables indicate which byte lane the current CPU cycle is accessing.
HA[31:3]	(see pinout tables)	B	Host Address Bus. HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the VT82C598MVP during cache snooping operations. HA25-27 are also used for power-up strapping options (sampled on the RESET# rising edge): HA27-26 Rx68[1-0] System Frequency (00,10=2x, 01=3x, 11=2.5x) HA25 Rx69[7] Memory Frequency (0=CPU, 1=AGP)
HD[63:0]	(see pinout tables)	B	Host CPU Data. These signals are connected to the CPU data bus.

Note: Clocking of the CPU and cache interfaces is performed with HCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

Cache Control			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
CADS#	T25	O	Cache Address Strobe. Assertion causes the burst SRAM to load the address register from address pins. Connected to all cache SRAMs.
CADV#	T24	O	Cache Advance. Assertion causes the burst SRAM to advance to the next Quadword in the cache line. Connected to all cache SRAMs.
COE1#	R25	O	Cache Output Enable. Typically connected to all cache SRAMs.
CCS1#	R24	O	Cache Chip Select. Typically connected to all cache SRAMs.
TA[7:0]	P26, P25, N22, N23, N24, M26, N26, N25	B	Tag Address. TA0-7 are inputs during CPU accesses and outputs during L2 cache line fills and L2 line invalidates during inquire cycles.
TWE#	P24	O	Tag Write Enable. When asserted, new state and tag addresses are written into the external tag. Connected to all cache SRAMs.
GWE#	T26	O	Global Write Enable. Connected to all cache SRAMs.
BWE#	R23	O	Byte Write Enable. Connected to all cache SRAMs.

Note: The VT82C598MVP pinouts were defined assuming the Baby AT PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (ATX, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface			
Signal Name	Pin #	I/O	Signal Description
MD[63:0]	(see pinout tables)	B	Memory Data. These signals are connected to the DRAM data bus. Note: MD0 is internally pulled up for use in EDO memory type detection.
MECC[7:0]	D23, D25, C15, A15, D24, D26, B15, D14	B	DRAM ECC or EC Data
MA[13:2], MAA[1:0], MAB[1:0] / CKE[3:2]#	A22, D21, C21, B21, A21, D20, C20, B20, A20, D19, C19, B19, C22, B22, A19, D18	O	Memory Address. DRAM address lines. MA0-1 are duplicated for better drive. The second copy (MAB0-1) can optionally be configured for use as clock enables 2-3 for notebook configurations to power down the SDRAMs (see Rx78[0]).
RAS5# / CS5# / CKE1#, RAS4# / CS4# / CKE0#, RAS3# / CS3#, RAS2# / CS2#, RAS1# / CS1#, RAS0# / CS0#	D22, A23, B23, C23, A24, B24	O	Multifunction Pins 1. FPG/EDO DRAM: Row Address Strobe of each bank. 2. Synchronous DRAM: Chip select of each bank. 3. Alternate function: RAS[5-4]# may be used as clock enables 1-0 for powering down the SDRAMs in notebook applications.
CAS#[7:0] / DQM#[7:0]	B26, B25, C17, B17, A26, A25, D17, A17	O	Multifunction Pins 1. FPG/EDO DRAM: Column Address Strobe of each byte lane. 2. Synchronous DRAM: Data mask of each byte lane.
SRASA#, SRASB#, SRASC#	C18, B18, A18	O	Row Address Command Indicator. For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1), and "C" controls banks 4-5 (module 2).
SCASA#, SCASB#, SCASC#	C16, B16, A16	O	Column Address Command Indicator. For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1), and "C" controls banks 4-5 (module 2).
SWEA# / MWEA#, SWEB# / MWEB#, SWEC# / MWEC#	C26, C25, C24	O	Write Enable Command Indicator. For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). Multifunction pins, used as MWE# pins for FPG/EDO memory. "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1), and "C" controls banks 4-5 (module 2).
DS[3:0]#	H22, D16, G22, D15	O	Data Strobes. (Reserved for future use)

Note: Clocking of the memory subsystem is synchronous with the CPU clock (HCLK); see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

PCI Bus Interface			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
FRAME#	AA2	B	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	(see pinout tables)	B	Address/Data Bus. The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	W4, AA3, AC1, AF2	B	Command/Byte Enable. Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	AA1	B	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	AB3	B	Target Ready. Asserted when the target is ready for data transfer.
STOP#	AB1	B	Stop. Asserted by the target to request the master to stop the current transaction.
DEVSEL#	AB2	B	Device Select. This signal is driven by the VT82C598MVP when a PCI initiator is attempting to access main memory. It is an input when the VT82C598MVP is acting as a PCI initiator.
PAR	AC2	B	Parity. A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	AB4	B	System Error. VT82C598MVP will pulse this signal when it detects a system error condition.
LOCK#	T1	B	Lock. Used to establish, maintain, and release resource lock.
PREQ#	AC6	I	South Bridge Request. This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	AD6	O	South Bridge Grant. This signal driven by the VT82C598MVP to grant PCI access to the South Bridge.
REQ[4:0]#	P23, R4, R2, T4, T2	I	PCI Master Request. PCI master requests for PCI.
GNT[4:0]#	R26, P4, R3, R1, T3	O	PCI Master Grant. Permission is given to the master to use PCI.

Note: Clocking of the PCI interface is performed with PCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

AGP Bus Interface			
Signal Name	Pin #	I/O	Signal Description
GFRM#	J3	B	Frame (PCI transactions only). Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GDS0#	M4	B	Bus Strobe 0 (AGP transactions only). Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1#	E3	B	Bus Strobe 1 (AGP transactions only). Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GD[31:0]	(see pinout tables)	B	Address/Data Bus. The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GBE[3:0]#	F1, G3, J4, M3	B	Command/Byte Enable. AGP: These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. PCI: Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GIRDY#	J2	B	Initiator Ready AGP: For write operations, the assertion of this pin indicates that the master is ready to provide <i>all</i> write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is <i>never</i> allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. PCI: Asserted when the initiator is ready for data transfer.
GTRDY#	J1	B	Target Ready: AGP: Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. PCI: Asserted when the target is ready for data transfer.
GSTOP#	K3	B	Stop (PCI transactions only). Asserted by the target to request the master to stop the current transaction.
GDSEL#	H4	B	Device Select (PCI transactions only). This signal is driven by the VT82C598MVP when a PCI initiator is attempting to access main memory. It is an input when the VT82C598MVP is acting as PCI initiator. Not used for AGP cycles.

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock input pins.

Note: PCB Layout Guidelines (reference from AGP specification)

- Total motherboard trace length 10" max, trace impedance = 65 ohms \pm 15 ohms, minimize signal crosstalk
- Trace lengths within groups matched to within 2 inches or better
 Groups are:
 - GDS0#, GD15-0, GBE1-0#
 - GDS1#, GD31-16, GBE3-2#
 - SBS#, SBA7-0
- Ground isolation should be provided around GDS0# and GDS1# to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

AGP Bus Interface (continued)			
Signal Name	Pin #	I/O	Signal Description
GPIPE#	A3	I	Pipelined Request. Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target VT82C598MVP. The master enqueues one request each rising edge of GCLK while PIPE# is asserted. When PIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	B3	I	Read Buffer Full. Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When RBF# is asserted, the VT82C598MVP will not return low priority read data to the master.
SBA[7:0]	C2, B1, A1, D5, A2, C5, C3, A6	I	SideBand Address. Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT82C598MVP). These pins are ignored until enabled.
SBS#	B2	I	Sideband Strobe. Provides timing for SBA[7:0] (driven by the master)
ST[2:0]	E8, B4, C4	O	Status (AGP only). Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT82C598MVP and inputs to the master.
GREQ#	A4	I	Request. Master request for AGP.
GGNT#	B5	O	Grant. Permission is given to the master to use AGP.
GPAR / GCKRUN#	B6	IO O	Rx78[1]=0: AGP Parity. A single parity bit is provided over GD[31:0] and GBE[3:0]. Rx78[1]=1: AGP Clock Run. Used to stop the AGP bus clock to reduce bus power usage.
GSERR# / PCKRUN#	A5	IO O	Rx78[1]=0: AGP System Error. The VT82C598MVP will pulse this signal when it detects a system error condition. Rx78[1]=1: PCI Clock Run. Used to stop the PCI bus clock to reduce bus power usage.

Note: For PCI operation on the AGP bus, the following pins are not required:

- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: PIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the 598MVP has an internal pullup on RBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

Clock / Reset Control																																																																											
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>																																																																								
HCLK	P5	I	Host Clock. This pin receives the host CPU clock. This clock is used by all logic in the host CPU domain. The memory interface logic will also use this clock if selected (memory system timing can alternately be selected to use the AGP bus clock).																																																																								
GCLK	D4	I	AGP Clock. This pin receives the AGP bus clock. This clock is used by all logic in the AGP clock domain. The AGP clock must be synchronous / pseudo-synchronous to the host CPU clock (selectable as shown in the table below). The CPU clock needs to lead the AGP clock by 0.2 ± 0.5 nsec.																																																																								
PCLK	W5	I	<p>PCI Clock. This pin receives a buffered host clock divided-by-2, 2.5, or 3 See strapping options on HA27-25 (strapping options can be read back in configuration registers 68 and 69). This clock is used by all of the VT82C598MVP logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous / pseudo-synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 2:1, 2.5:1, or 3:1 as shown in the table below. The PCI clock needs to be controlled to within 1.5 ± 0.5 nsec relative to the host CPU clock (CPU leads).</p> <p><u>Typical Clock Frequency Combinations (DRAM synchronous to CPU)</u></p> <table border="1"> <thead> <tr> <th>HA[27-25]</th> <th>Mode</th> <th>Host Clock</th> <th>DRAM Clock</th> <th>AGP Clock</th> <th>PCI Clock</th> </tr> </thead> <tbody> <tr> <td>100</td> <td>2x</td> <td>60 MHz</td> <td>60 MHz</td> <td>60 MHz</td> <td>30 MHz</td> </tr> <tr> <td>100</td> <td>2x</td> <td>66 MHz</td> <td>66 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> <tr> <td>110</td> <td>2.5x</td> <td>75 MHz</td> <td>75 MHz</td> <td>60 MHz</td> <td>30 MHz</td> </tr> <tr> <td>110</td> <td>2.5x</td> <td>83 MHz</td> <td>83 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> <tr> <td>010</td> <td>3x</td> <td>100 MHz</td> <td>100 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> </tbody> </table> <p><u>Typical Clock Frequency Combinations (DRAM synchronous to AGP)</u></p> <table border="1"> <thead> <tr> <th>HA[27-25]</th> <th>Mode</th> <th>Host Clock</th> <th>DRAM Clock</th> <th>AGP Clock</th> <th>PCI Clock</th> </tr> </thead> <tbody> <tr> <td>101</td> <td>2x</td> <td>60 MHz</td> <td>60 MHz</td> <td>60 MHz</td> <td>30 MHz</td> </tr> <tr> <td>101</td> <td>2x</td> <td>66 MHz</td> <td>66 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> <tr> <td>111</td> <td>2.5x</td> <td>75 MHz</td> <td>60 MHz</td> <td>60 MHz</td> <td>30 MHz</td> </tr> <tr> <td>111</td> <td>2.5x</td> <td>83 MHz</td> <td>66 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> <tr> <td>011</td> <td>3x</td> <td>100 MHz</td> <td>66 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> </tbody> </table>	HA[27-25]	Mode	Host Clock	DRAM Clock	AGP Clock	PCI Clock	100	2x	60 MHz	60 MHz	60 MHz	30 MHz	100	2x	66 MHz	66 MHz	66 MHz	33 MHz	110	2.5x	75 MHz	75 MHz	60 MHz	30 MHz	110	2.5x	83 MHz	83 MHz	66 MHz	33 MHz	010	3x	100 MHz	100 MHz	66 MHz	33 MHz	HA[27-25]	Mode	Host Clock	DRAM Clock	AGP Clock	PCI Clock	101	2x	60 MHz	60 MHz	60 MHz	30 MHz	101	2x	66 MHz	66 MHz	66 MHz	33 MHz	111	2.5x	75 MHz	60 MHz	60 MHz	30 MHz	111	2.5x	83 MHz	66 MHz	66 MHz	33 MHz	011	3x	100 MHz	66 MHz	66 MHz	33 MHz
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RESET#	AC7	I	Reset. When asserted, this signal resets the VT82C598MVP and sets all register bits to the default value. This signal also connects to the PCI bus, to the AGP bus, and (through an inverter) to the ISA bus (if implemented). The rising edge of this signal is used to sample all power-up strap options (see HA25-27).																																																																								
SUSCLK	D6	I	Suspend Clock. For implementation of the Suspend-to-DRAM feature. Ground this pin to disable.																																																																								
SUSTAT#	C6	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.																																																																								
GCKRUN# / GPAR	B6	O IO	AGP Clock Run (Rx78[1]=1). For implementation of AGP bus clock control for very low-power AGP bus operation. Refer to the AGP Specification for additional information.																																																																								
PCKRUN# / GSERR#	A5	O IO	PCI Clock Run (Rx78[1]=1). For implementation of PCI bus clock control for very low-power PCI bus operation. Refer to the PCI Mobile Design Guidelines document for additional information.																																																																								

Power and Ground			
Signal Name	Pin #	I/O	Signal Description
VTT	F8, F19, H21	P	Suspend Power (3.3V ±5%). Power for SWEA-C#, RAS[5-0]#, CAS[7-0]#, SUSTAT#, SUSCLK.
VCCI	E5, F6, F22, AA6, AB5, AB21	P	Power for Internal Logic (3.3V ±5%).
HVCC	U22, V22, AB9-10, AB17-19	P	Power for CPU Interface (2.5V to 3.3V ±5%).
VCC	E9-11, E17-19, G5, H5-6, J5, J22, K22, L22, R5, T5, U5, V5, AA7-8, AB6-7	P	Power for Memory, PCI, and AGP Interfaces (3.3V ±5%).
AVCC	K5	P	Analog Power (3.3V ±5%). For internal clock logic.
AGND	N5	P	Analog Ground. For internal clock logic. Connect to main ground plane.
GND	D8, E6-E7, E14-E16, E22, F7, F20-21, G6, G21, L5, L11-L16, M5, M11-M16, N11-N16, P11-P16, P22, R11-R16, R22, T11-T16, W6, W21, Y5-6, Y21, AA5, AA19-22, AB13-14, AB22	P	Ground
5VREF	E21, AB8	P	5V Reference (5V ±5%). Used to provide 5V input tolerance.
GVREF	F5	P	AGP Voltage Reference. 0.39 GVCC to 0.41 GVCC. Typical value is 1.32V (0.40 times 3.3V). This can be provided with a resistive divider on GVCC using 270 ohm and 180 ohm (2%) resistors.
MVREF	E20	P	DRAM Voltage Reference. 1.5V for SDRAM, 1.0V for DDR SDRAM (±5%)

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C598MVP. These tables also document the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), “—” for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1’s to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 2. VT82C598MVP Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0598	RO
5-4	Command	0006	RW
7-6	Status	0290	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	0000 0008	RW
14-27	-reserved- (base address registers)	00	—
28-2F	-reserved- (unassigned)	00	—
33-30	-reserved- (expan ROM base addr)	00	—
37-34	Capability Pointer	0000 00A0	RO
34-3B	-reserved- (unassigned)	00	—
3C-3D	-reserved- (interrupt line & pin)	00	—
3E-3F	-reserved- (min gnt and max latency)	00	—

Device-Specific Registers

Offset	Cache Control	Default	Acc
50	Cache Control 1	00	RW
51	Cache Control 2	00	RW
52	Non-Cacheable Control	00	RW
53	System Performance Control	00	RW
55-54	Non-Cacheable Region #1	0000	RW
57-56	Non-Cacheable Region #2	0000	RW

Offset	DRAM Control	Default	Acc
59-58	MA Map Type	0000	RW
5A-5F	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[29:22])	01	RW
5B	Bank 1 Ending (HA[29:22])	01	RW
5C	Bank 2 Ending (HA[29:22])	01	RW
5D	Bank 3 Ending (HA[29:22])	01	RW
5E	Bank 4 Ending (HA[29:22])	01	RW
5F	Bank 5 Ending (HA[29:22])	01	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for Banks 0,1	EC	RW
65	DRAM Timing for Banks 2,3	EC	RW
66	DRAM Timing for Banks 4,5	EC	RW
67	-reserved- (unassigned)	00	RW
68	DRAM Control	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	01	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	RO

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	RW
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78	PMU Control	00	RW
79-7D	-reserved-	00	—
7E-7F	DLL Test Mode (do not program)	00	RW
80-FF	-reserved-	00	—

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved- (unassigned)	00	—
8B-88	Gr. Aperture Translation Table Base	0000 0000	RW
8C-8F	-reserved- (unassigned)	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	02	RO
A1	AGP Next Item Pointer	00	RO
A2	AGP Specification Revision	10	RO
A3	-reserved- (unassigned)	00	—
A7-A4	AGP Status	0700 0203	RO
AB-A8	AGP Command	0000 0000	RW
AC	AGP Control	00	RW
AD-AF	-reserved- (unassigned)	00	—

Offset	Miscellaneous Control	Default	Acc
B0-FB	-reserved- (unassigned)	00	—
FD-FF	Reserved (do not program)	0000 0000	RW

Device 1 - PCI-to-PCI Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	8598	RO
5-4	Command	0007	RW
7-6	Status	0220	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	04	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	01	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved- (base address registers)	00	—
18	Primary Bus Number	00	RW
19	Secondary Bus Number	00	RW
1A	Subordinate Bus Number	00	RW
1B	-reserved- (secondary latency timer)	00	—
1C	I/O Base	F0	RW
1D	I/O Limit	00	RW
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	FFF0	RW
23-22	Memory Limit (Inclusive)	0000	RW
25-24	Prefetchable Memory Base	FFF0	RW
27-26	Prefetchable Memory Limit	0000	RW
28-3D	-reserved- (unassigned)	00	—
3F-3E	PCI-to-PCI Bridge Control	00	RW

Device-Specific Registers

Offset	PCI Bus #2 Control	Default	Acc
40	CPU-to-PCI Flow Control 1	00	RW
41	CPU-to-PCI Flow Control 2	00	RW
42	PCI Master Control	00	RW
43-4F	-reserved- (unassigned)	00	—

Miscellaneous I/O

One I/O port is defined in the VT82C598MVP: Port 22.

Port 22 – PCI Arbiter Disable RW

- 7-2 **Reserved** always reads 0
- 1 **PCI #2 (AGP) Arbiter Disable**
 - 0 Respond to GREQ# signal default
 - 1 Do not respond to GREQ# signal
- 0 **PCI #1 Arbiter Disable**
 - 0 Respond to all REQ# signals default
 - 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the VT82C598MVP (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

- 31 **Configuration Space Enable**
 - 0 Disabled default
 - 1 Convert configuration data port writes to configuration cycles on the PCI bus
- 30-24 **Reserved** always reads 0
- 23-16 **PCI Bus Number**
 - Used to choose a specific PCI bus in the system
- 15-11 **Device Number**
 - Used to choose a specific device in the system (devices 0 and 1 are defined)
- 10-8 **Function Number**
 - Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined).
- 7-2 **Register Number (also called the "Offset")**
 - Used to select a specific DWORD in the configuration space
- 1-0 **Fixed** always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID.....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID.....RO

15-0 ID Code (0598h to identify the VT82C598MVP)

Device 0 Offset 5-4 - Command.....RW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RO
 - 0 Fast back-to-back transactions only allowed to the same agentdefault
 - 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable**..... RO
 - 0 SERR# driver disableddefault
 - 1 SERR# driver enabled
 (SERR# is used to report parity errors if bit-6 is set).
- 7 Address / Data Stepping** RO
 - 0 Device never does steppingdefault
 - 1 Device always does stepping
- 6 Parity Error Response**.....RW
 - 0 Ignore parity errors & continuedefault
 - 1 Take normal action on detected parity errors
- 5 VGA Palette Snoop** RO
 - 0 Treat palette accesses normallydefault
 - 1 Don't respond to palette accesses on PCI bus
- 4 Memory Write and Invalidate Command**..... RO
 - 0 Bus masters must use Mem Writedefault
 - 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring** RO
 - 0 Does not monitor special cyclesdefault
 - 1 Monitors special cycles
- 2 Bus Master** RO
 - 0 Never behaves as a bus master
 - 1 Can behave as a bus masterdefault
- 1 Memory Space**..... RO
 - 0 Does not respond to memory space
 - 1 Responds to memory spacedefault
- 0 I/O Space** RO
 - 0 Does not respond to I/O spacedefault
 - 1 Responds to I/O space

Device 0 Offset 7-6 - Status RWC

- 15 Detected Parity Error**
 - 0 No parity error detected default
 - 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6).write one to clear
- 14 Signaled System Error (SERR# Asserted)**
 - always reads 0
- 13 Signaled Master Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the master write one to clear
- 12 Received Target Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the target..... write 1 to clear
- 11 Signaled Target Abort**..... always reads 0
 - 0 Target Abort never signaled
- 10-9 DEVSEL# Timing**
 - 00 Fast
 - 01 Medium..... always reads 01
 - 10 Slow
 - 11 Reserved
- 8 Data Parity Error Detected**
 - 0 No data parity error detected default
 - 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT82C598MVP was initiator of the operation in which the error occurred....write one to clear
- 7 Fast Back-to-Back Capable** always reads 1
- 6 Reserved** always reads 0
- 5 66MHz Capable**..... always reads 0
- 4 Supports New Capability list** always reads 1
- 3-0 Reserved** always reads 0

Device 0 Offset 8 - Revision ID RO

7-0 VT82C598MVP Chip Revision Code

Device 0 Offset 9 - Programming Interface RO

7-0 Interface Identifier always reads 00

Device 0 Offset A - Sub Class Code..... RO

7-0 Sub Class Codereads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code..... RO

7-0 Base Class Code..reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer RW

Specifies the latency timer value in PCI bus clocks.

- 7-3 Guaranteed Time Slice for CPU**..... default=0
- 2-0 Reserved** (fixed granularity of 8 clks) .. always read 0
 - Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type.....RO

7-0 Header Type Codereads 00: single function

Device 0 Offset F - Built In Self Test (BIST).....RO

7 BIST Supportedreads 0: no supported functions

6-0 Reserved always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base.....RW

31-28 Upper Programmable Base Address Bits..... def=0

27-20 Lower Programmable Base Address Bits def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 1 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
<u>7</u>	<u>6</u>	<u>5</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>	<u>0</u>	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 37-34 - Capability Pointer.....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointeralways reads A0h

Device 0 Configuration Registers - Host Bridge

Cache Control

Device 0 Offset 50 - Cache Control 1.....RW

- 7-6 Cache Enable / Initialize**
 - 00 Cache disabledefault
 - 01 Cache Initialize - always does L2 fill
 - 10 Cache enable (normal operation)
 - 11 Reserved (do not use)
- 5 Linear Burst**
 - 0 Disabledefault
 - 1 Enable
- 4-3 Tag Configuration**
 - 00 8+0 - 8 Tag bits, no alt (dirty) bit.....default
 - 01 7+1 - 7 Tag bits + alternate (dirty) bit
 - 1x Reserved
- 2-0 Reserved**always read 0

Device 0 Offset 51 - Cache Control 2.....RW

- 7-6 Reserved (no function)**..... RW
- 5 Backoff CPU**
Set to one to backoff CPU when non-streaming access to fill L2 cache. Used when register 52h bit-2 is set for "L2 fill when CACHE# is inactive". This bit should normally be set to 0 for best performance, but performance differences are typically not significantly noticeable at the system level.
 - 0 Defer ready return until L2 is filled.....default
 - 1 Backoff CPU until L2 is filled
- 4 Reserved** always reads 0
- 3 SRAM Banks**.....(default set from inverse of HA29)
 - 0 1 Bank
 - 1 2 Banks
- 2 Reserved** always reads 0
- 1-0 Cache Size** (bit-0 default set from inverse of HA31)
 - 00 256K
 - 01 512K
 - 10 1M
 - 11 2M

Device 0 Offset 52 - Non-Cacheable Control..... RW

- 7 C0000-C7FFF Cacheable & Write-Protect**def=0
- 6 D0000-DFFFF Cacheable & Write-Protect** ...def=0
- 5 E0000-EFFFF Cacheable & Write-Protect**def=0
- 4 F0000-FFFFF Cacheable & Write-Protect**def=0
- 3 Reserved**always reads 0
- 2 L2 Fill on Single Read**
 - 0 Normal L2 cache fill default
 - 1 Force the requested data to be filled into the L2 cache (provided that L2 cache is enabled), even if the CPU does a read cycle with CACHE# de-asserted. Setting this bit significantly improves performance.
- 1 Reserved**always reads 0
- 0 L2 Write Thru/Write-Back**
 - 0 Write-Back default
 - 1 Write-Thru

Device 0 Offset 53 - System Performance Control..... RW

- 7 Read Around Write**
 - 0 Disable..... default
 - 1 Enable
- 6 Cache Read Pipeline Cycle**
 - 0 Disable..... default
 - 1 Enable
- 5 Cache Write Pipeline Cycle**
 - 0 Disable..... default
 - 1 Enable
- 4 DRAM Read Pipeline Cycle**
 - 0 Disable..... default
 - 1 Enable
- 3-0 Reserved**always reads 0

Device 0 Offset 55-54 - Non-Cacheable Region #1RW

- 15-3 Base Address - A<28:16>..... default=0**
 As noted below, the base address must be a multiple of the region size.
- 2-0 Range (Region Size)**
- 000 Disabledefault
 - 001 64K
 - 010 128K (Base Address A16 must be 0)
 - 011 256K (Base Address A16-17 must be 0)
 - 100 512K (Base Address A16-18 must be 0)
 - 101 1M (Base Address A16-19 must be 0)
 - 110 2M (Base Address A16-20 must be 0)
 - 111 4M (Base Address A16-21 must be 0)

Device 0 Offset 57-56 - Non-Cacheable Region #2..... RW

- 15-3 Base Address MSBs - A<28:16>..... default=0**
 As noted below, the base address must be a multiple of the region size.
- 2-0 Range (Region Size)**
- 000 Disable..... default
 - 001 64K
 - 010 128K (Base Address A16 must be 0)
 - 011 256K (Base Address A16-17 must be 0)
 - 100 512K (Base Address A16-18 must be 0)
 - 101 1M (Base Address A16-19 must be 0)
 - 110 2M (Base Address A16-20 must be 0)
 - 111 4M (Base Address A16-21 must be 0)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies 82C598MVP BIOS porting guide for details).

Table 3. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys	1MB	—	00100000-DRAM Top	Can have hole
Bus	D Top		DRAM Top-FFFEFFFF	
Init	4G-64K	64K	FFFEFFFF-FFFFFFF	000Fxxxx alias

Device 0 Offset 59-58 - DRAM MA Map Type.....RW

- 15-13 Bank 5/4 MA Map Type (EDO/FPG)**
 - 000 8-bit Column Address
 - 001 9-bit Column Address
 - 010 10-bit Column Addressdefault
 - 011 11-bit Column Address
 - 100 12-bit Column Address (64Mb)
 - 101 Reserved
 - 11x Reserved
- Bank 5/4 MA Map Type (SDRAM)**
 - 0xx 16Mbit SDRAM.....default
 - 100 64Mbit SDRAM (x4, x8, x16, 4-bank x32)
 - 101 Reserved
 - 11x Reserved
- 12 Bank 5/4 Virtual Channel Enable..... default=0**
- 11-8 Reserved always reads 0**
- 7-5 Bank 1/0 MA Map Type (see above)**
 - 4 Bank 1/0 Virtual Channel Enable..... default=0**
- 3-1 Bank 3/2 MA Map Type (see above)**
 - 0 Bank 3/2 Virtual Channel Enable..... default=0**

Device 0 Offset 5A-5F – DRAM Row Ending Address:

All of the registers in this group default to 01h:

- Offset 5A – Bank 0 Ending (HA[30:23])..... RW**
- Offset 5B – Bank 1 Ending (HA[30:23])..... RW**
- Offset 5C – Bank 2 Ending (HA[30:23])..... RW**
- Offset 5D – Bank 3 Ending (HA[30:23])..... RW**
- Offset 5E – Bank 4 Ending (HA[30:23])..... RW**
- Offset 5F – Bank 5 Ending (HA[30:23])..... RW**

Note :BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type RW

- 7-6 Reserved always reads 0**
- 5-4 DRAM Type for Bank 5/4**
 - 00 Fast Page Mode DRAM (FPG)..... default
 - 01 EDO DRAM (EDO)
 - 10 SDRAM Double Data Rate (DDR SDRAM-II)
 - 11 SDRAM Single Data Rate (SDR SDRAM)
- 3-2 DRAM Type for Bank 3/2.....default=FPG**
- 1-0 DRAM Type for Bank 1/0.....default=FPG**

Table 4. Memory Address Mapping Table

EDO/FP DRAM

MA:	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8-bit Col (000)		23	22	21	11	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
9-bit Col (001)		24	23	22	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
10-bit Col (010)		25	24	23	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
11-bit Col (011)		26	25	23	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
12-bit Col (100)		27	25	23	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits

SDRAM

MA:	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
16Mb (0xx)			11	11	10	9	8	7	6	5	4	3	2	1	0	Row Bits Col Bits
64Mb (100)	24	13	12	22	21	20	19	18	17	16	15	14	11	23	x4: 10 col x8: 9 col x16: 8 col x32: 8 col	

"PC" = "Precharge Control" (refer to SDRAM specifications)

- 16Mb 11x10, 11x9, and 11x8 configurations supported
- 64Mb x4: 12x10 4bank, 13x10 2bank
- x8: 12x9 4bank, 13x9 2bank
- x16: 12x8 4bank, 13x8 2bank
- x32: 11x8 4bank

Device 0 Offset 61 - Shadow RAM Control 1RW

- 7-6 CC000h-CFFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 5-4 C8000h-CBFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 3-2 C4000h-C7FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 1-0 C0000h-C3FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2RW

- 7-6 DC000h-DFFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 5-4 D8000h-DBFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 3-2 D4000h-D7FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 1-0 D0000h-D3FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3..... RW

- 7-6 E0000h-EFFFFh**
 00 Read/write disable default
 01 Write enable
 10 Read enable
 11 Read/write enable
- 5-4 F0000h-FFFFFFh**
 00 Read/write disable default
 01 Write enable
 10 Read enable
 11 Read/write enable
- 3-2 Memory Hole**
 00 None default
 01 512K-640K
 10 15M-16M (1M)
 11 14M-16M (2M)
- 1-0 SMI Mapping Control**
 00 Disable SMI Address Redirection default
 01 Allow access to DRAM Axxxx-Bxxxx for both normal and SMI cycles
 10 Reserved
 11 Allow SMI Axxxx-Bxxxx DRAM access

Note: The A0000-BFFFF address range is reserved for use by VGA controllers for system access to the VGA frame buffer. Since frame buffer accesses are normally directed to the system VGA controller (with its separate memory subsystem), system DRAM locations in the A0000-BFFFF range would normally be unused. Setting the above bits appropriately allows this block of system memory to be used by directing Axxxx-Bxxxx accesses to corresponding memory addresses in system DRAM instead of directing those accesses to the PCI bus for VGA frame buffer access.

Device 0 Offset 64 - DRAM Timing for Banks 0,1RW

Device 0 Offset 65 - DRAM Timing for Banks 2,3RW

Device 0 Offset 66 - DRAM Timing for Banks 4,5RW

FPG / EDO Settings for Registers 64-66

- 7 RAS Precharge Time**
 - 0 3T
 - 1 4Tdefault
- 6 RAS Pulse Width**
 - 0 4T
 - 1 5Tdefault
- 5-4 CAS Read Pulse Width**
 - 00 1T
 - 01 2T
 - 10 3Tdefault
 - 11 4T

Note: EDO will not automatically reduce the CAS pulse width. For EDO type DRAMs, use 00 if CAS width = 1 is to be used.
- 3 CAS Write Pulse Width**
 - 0 1T
 - 1 2Tdefault
- 2 MA-to-CAS Delay**
 - 0 1T
 - 1 2Tdefault
- 1 RAS to MA Delay**
 - 0 1Tdefault
 - 1 2T
- 0 Reserved** always reads 0

SDRAM Settings for Registers 64-66

- 7 Precharge Command to Active Command Period**
 - 0 TRP = 2T
 - 1 TRP = 3T default
- 6 Active Command to Precharge Command Period**
 - 0 TRAS = 5T
 - 1 TRAS = 6T default
- 5-4 CAS Latency**

	SDRAM	SDRAM-II
00	1T	n/a
01	2T	n/a
10	3T	2T, 2.5T default
11	n/a	3T
- 3 DDR Write Enable (SDRAM-II Only)**
 - 0 Disable
 - 1 Enable default
- 2 ACTIVE Command to CMD Command Period**
 - 0 2T
 - 1 3T default
- 1-0 Bank Interleave**
 - 00 No Interleave default
 - 01 2-way
 - 10 4-way
 - 11 Reserved

Device 0 Offset 68 - DRAM Control.....RW

- 7 SDRAM Open Page Control**
 - 0 Always precharge SDRAM banks when accessing EDO/FPG DRAMs.....default
 - 1 SDRAM banks remain active when accessing EDO/FPG banks
- 6 Bank Page Control**
 - 0 Allow only pages of the same bank active... def
 - 1 Allow pages of different banks to be active
- 5 EDO Pipeline Burst Rate**
 - 0 X-2-2-2-2-2-2.....default
 - 1 X-2-2-2-3-2-2-2
- 4 Reserved (do not program)..... default = 0**
- 3 EDO Test Mode**
 - 0 Disabledefault
 - 1 Enable
- 2 Burst Refresh**
 - 0 Disabledefault
 - 1 Enable (burst 4 times)
- 1-0 System Frequency Divider RO**
 - x0 CPU/PCI Frequency Ratio = 2x (66 MHz)
 - 01 CPU/PCI Frequency Ratio = 3x (100 MHz)
 - 11 CPU/PCI Frequency Ratio = 2.5x (75/83 MHz)

These bits are latched from HA27-26 at the rising edge of RESET#.

Note: MD0 is internally pulled up for EDO detection.

Device 0 Offset 69 – DRAM Clock Select.....RW

- 7 DRAM Operating Frequency RO**
 - 0 Same as CPU Frequency (66/75/83/100 MHz)
 - 1 Same as AGP Frequency (66 MHz)

This bit is latched from HA25 at the rising edge of RESET#.
- 6-0 Reserved always reads 0**

Device 0 Offset 6A - Refresh Counter RW

- 7-0 Refresh Counter (in units of 16 CPUCLKs)**
 - 00 DRAM Refresh Disabled..... default
 - 01 32 CPUCLKs
 - 02 48 CPUCLKs
 - 03 64 CPUCLKs
 - 04 80 CPUCLKs
 - 05 96 CPUCLKs
 -

The programmed value is the desired number of 16-CPUCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control..... RW

- 7-6 Arbitration Parking Policy**
 - 00 Park at last bus owner default
 - 01 Park at CPU side
 - 10 Park at AGP side
 - 11 Reserved
- 5-1 Reserved always reads 0**
- 0 Multi-Page Open**
 - 0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
 - 1 Enable default

Device 0 Offset 6C - SDRAM Control.....RW

- 7 Reserved** always reads 0
- 6 DRAM Start Cycle**
 - 0 Concurrent with cache hit detection
(for 66MHz operation)default
 - 1 After cache hit detection
(for 100MHz operation)
- 5 MD-to-HD Pop**
 - 0 Normaldefault
 - 1 Add 1T latency to improve MD setup time at
100 MHz
- 4 DDR Write-to-Read Turnaround**
 - 0 1T Turnaround (i.e., 3T from Write command
to Read command)default
 - 1 2T Turnaround
- 3 Single RW Burst Stop Command**
 - 0 Disabledefault
 - 1 Enable BST command to SDRAM to allow
fast single-cycle pipeline
- 2-0 SDRAM Operation Mode Select**
 - 000 Normal SDRAM Modedefault
 - 001 NOP Command Enable
 - 010 All-Banks-Precharge Command Enable
(CPU-to-DRAM cycles are converted
to All-Banks-Precharge commands).
 - 011 MSR Enable
CPU-to-DRAM cycles are converted to
commands and the commands are driven on
MA[13:0]. The BIOS selects an appropriate
host address for each row of memory such that
the right commands are generated on
MA[13:0].
 - 100 CBR Cycle Enable (if this code is selected,
CAS-before-RAS refresh is used; if it is not
selected, RAS-Only refresh is used)
 - 101 Reserved
 - 11x Reserved

Device 0 Offset 6D - DRAM Drive Strength..... RW

- 7 Reserved** always reads 0
- 6-5 Delay DRAM Read Latch**
 - 00 Disable default
 - 01 0.5 ns
 - 10 1.0 ns
 - 11 2.0 ns
- 4 MD Drive**
 - 0 8 mA default
 - 1 6 mA
- 3 SDRAM Command Drive (SRAS#, SCAS#, SWE#)**
 - 0 16mA default
 - 1 24mA
- 2 MA[2:13] / WE# Drive**
 - 0 16mA default
 - 1 24mA
- 1 CAS# Drive**
 - 0 8 mA default
 - 1 12 mA
- 0 RAS# Drive**
 - 0 16mA default
 - 1 24mA

Device 0 Offset 6E - ECC ControlRW

- 7 ECC / EMode Select**
 - 0 ECC Checking and Reportingdefault
 - 1 ECC Checking, Reporting, and Correcting
- 6 Reserved** always reads 0
- 5 Enable SERR# on ECC / EC Multi-Bit Error**
 - 0 Don't assert SERR# for multi-bit errors..... def
 - 1 Assert SERR# for multi-bit errors
- 4 Enable SERR# on ECC / EC Single-Bit Error**
 - 0 Don't assert SERR# for single-bit errors..... def
 - 1 Assert SERR# for single-bit errors
- 3 Reserved** always reads 0
- 2 ECC / EC Enable - Bank 5/4 (DIMM 2)**
 - 0 Disable (no ECC or EC for banks 5/4)...default
 - 1 Enable (ECC or EC per bit-7)
- 1 ECC / EC Enable - Bank 3/2 (DIMM 1)**
 - 0 Disable (no ECC or EC for banks 3/2)...default
 - 1 Enable (ECC or EC per bit-7)
- 0 ECC / EC Enable - Bank 1/0 (DIMM 0)**
 - 0 Disable (no ECC or EC for banks 1/0)...default
 - 1 Enable (ECC or EC per bit-7)

Device 0 Offset 6F - ECC Status..... RWC

- 7 Multi-bit Error Detected**..... write of '1' resets
- 6-4 Multi-bit Error DRAM Bank**..... default=0
Encoded value of the bank with the multi-bit error.
- 3 Single-bit Error Detected**..... write of '1' resets
- 2-0 Single-bit Error DRAM Bank** default=0
Encoded value of the bank with the single-bit error.

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

<u>Bit-7</u>	<u>Bits 2-0</u>	<u>RMW</u>	<u>Error Checking</u>	<u>Error Correction</u>
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

PCI Bus #1 Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer ControlRW

- 7 CPU to PCI Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 6 PCI Master to DRAM Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 5 CPU-to-PCI Prefetch**
 - 0 Disabledefault
 - 1 Enable
- 4 PCI Master to DRAM Prefetch Disable**
 - 0 Enable.....default
 - 1 Disable
- 3 Reserved** (do not program)..... default = 0
- 2 PCI Master Read Caching**
 - 0 Disabledefault
 - 1 Enable
- 1 Delay Transaction**
 - 0 Disabledefault
 - 1 Enable
- 0 Reserved** (do not program)..... default = 0

Device 0 Offset 71 - CPU to PCI Flow Control 1..... RW

- 7 Dynamic Burst**
 - 0 Disable..... default
 - 1 Enable (see note under bit-3 below)
- 6 Byte Merge**
 - 0 Disable..... default
 - 1 Enable
- 5 Reserved** (do not program)..... default = 0
- 4 PCI I/O Cycle Post Write**
 - 0 Disable..... default
 - 1 Enable
- 3 PCI Burst**
 - 0 Disable..... default
 - 1 Enable (bit7=1 will override this option)
- bit-7 bit-3 Operation**
 - 0 0 Every write goes into the write buffer and no PCI burst operations occur.
 - 0 1 If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
 - 1 x Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.
- 2 PCI Fast Back-to-Back Write**
 - 0 Disable..... default
 - 1 Enable
- 1 Quick Frame Generation**
 - 0 Disable..... default
 - 1 Enable
- 0 1 Wait State PCI Cycles**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset 72 - CPU to PCI Flow Control 2.....RWC

- 7 Retry Status**
 - 0 Retry occurred less than retry limitdefault
 - 1 Retry occurred more than x times (where x is defined by bits 5-4) **write 1 to clear**
- 6 Retry Timeout Action**
 - 0 Retry Forever (record status only).....default
 - 1 Flush buffer for write or return all 1s for read
- 5-4 Retry Limit**
 - 00 Retry 2 timesdefault
 - 01 Retry 16 times
 - 10 Retry 4 times
 - 11 Retry 64 times
- 3 Clear Failed Data and Continue Retry**
 - 0 Flush the entire post-write bufferdefault
 - 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting
- 2 CPU Backoff on PCI Read Retry Failure**
 - 0 Disabledefault
 - 1 Backoff CPU when reading data from PCI and retry fails
- 1 Reduce 1T for FRAME# Generation**
 - 0 Disabledefault
 - 1 Enable
- 0 Reserved** (do not program)..... default = 0

Device 0 Offset 73 - PCI Master Control 1..... RW

- 7 Reserved** always reads 0
- 6 PCI Master 1-Wait-State Write**
 - 0 Zero wait state TRDY# response default
 - 1 One wait state TRDY# response
- 5 PCI Master 1-Wait-State Read**
 - 0 Zero wait state TRDY# response default
 - 1 One wait state TRDY# response
- 4 Prefetch Disable**
 - 0 Enable default
 - 1 Disable
- 3 Assert STOP# after PCI Master Write Timeout**
 - 0 Disable default
 - 1 Enable
- 2 Assert STOP# after PCI Master Read Timeout**
 - 0 Disable default
 - 1 Enable
- 1 LOCK# Function**
 - 0 Disable default
 - 1 Enable
- 0 PCI Master Broken Timer Enable**
 - 0 Disable default
 - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant. Does not apply to south bridge PREQ# input

Device 0 Offset 74 - PCI Master Control 2..... RW

- 7 PCI Master Read Prefetch by Enhance Command**
 - 0 Always Prefetch default
 - 1 Prefetch only if Enhance command
- 6 PCI Master Write Merge**
 - 0 Disable default
 - 1 Enable
- 5-0 Reserved** always reads 0

Device 0 Offset 75 - PCI Arbitration 1RW

- 7 Arbitration Mechanism**
 - 0 PCI has prioritydefault
 - 1 Fair arbitration between PCI and CPU
- 6 Arbitration Mode**
 - 0 REQ-based (arbitrate at end of REQ#)...default
 - 1 Frame-based (arbitrate at FRAME# assertion)
- 5-4 Latency Timer** read only, reads Rx0D bits 2:1
- 3-0 PCI Master Bus Time-Out**
(force into arbitration after a period of time)
 - 0000 Disabledefault
 - 0001 1x32 PCICLKs
 - 0010 2x32 PCICLKs
 - 0011 3x32 PCICLKs
 - 0100 4x32 PCICLKs
 -
 - 1111 15x32 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2RW

- 7 PCI #2 Master Access PCI #1 Retry Disconnect**
 - 0 Disable (PCI #2 will not be disconnected until access finishes).....default
 - 1 Enable (PCI #2 will be disconnected if max retries are attempted without success)
- 6 CPU Latency Timer Bit-0**..... RO
 - 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
 - 1 CPU has no time slot
- 5-4 Master Priority Rotation Control**
 - 00 Disabled (arbitration per Rx75 bit-7)default
 - 01 Grant to CPU after every PCI master grant
 - 10 Grant to CPU after every 2 PCI master grants
 - 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).
- 3-0 Reserved** always reads 0

Device 0 Offset 77 - Chip Test ModeRW

- 7-6 Reserved (no function)**..... always reads 0
- 5-0 Reserved (do not use)**..... default=0

Device 0 Offset 78 - PMU Control..... RW

- 7 I/O Port 22 Access**
 - 0 CPU access to I/O address 22h is passed on to the PCI bus default
 - 1 CPU access to I/O address 22h is processed internally
- 6 Suspend Refresh Type**
 - 0 CBR Refresh..... default
 - 1 Self Refresh
- 5 Normal Refresh**
 - 0 Suspend refresh using SUSCLK default
 - 1 Normal refresh
- 4 Dynamic Clock Control**
 - 0 Normal (clock is always running) default
 - 1 Clock to various internal functional blocks is disabled when those blocks are not being used
- 3 GCKRUN# De-assertion**
 - 0 GCKRUN# always low..... default
 - 1 GCKRUN# could be high due to PCKRUN#
- 2 Reserved**always reads 0
- 1 PCKRUN# / GCKRUN# Pin Control**
 - 0 Disable (A21=GPAR,C20=GSERR#) ... default
 - 1 Enable (A21=GCKRUN#, C20=PCKRUN#)
- 0 Memory Clock Enable (CKE) Function**
 - 0 CKE Disable (pins T1, R4, M2, M3 used for normal DRAM signals)..... default
 - 1 CKE Enable (pins T1, R4, M2, M3 used for CKE# signals)

Device 0 Offset 7E – DLL Test Mode..... RW

- 7-6 Reserved (status)**RO
- 5-0 Reserved (do not use)**default=0

Device 0 Offset 7F – DLL Test Mode..... RW

- 7-0 Reserved (do not use)** default=0

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT82C598MVP.

This scheme is shown in the figure below.

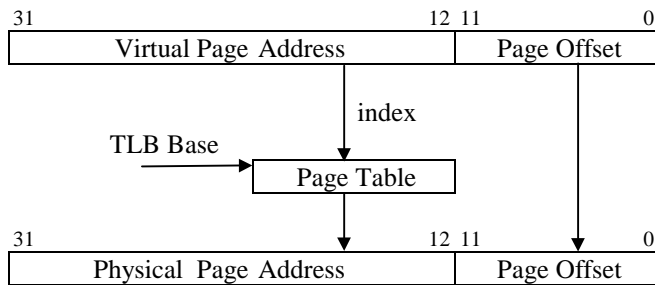


Figure 6. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the 82C598MVP contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control.....RW

- 31-16 Reserved always reads 0
- 15-8 Reserved (test mode status)..... RO

- 7 Flush Page TLB
 - 0 Disabledefault
 - 1 Enable

- 6-4 Reserved (always program to 0) RW

- 3 PCI#1 Master Address Translation for GA Access
 - 0 Addresses generated by PCI #1 Master accesses of the Graphics Aperture will not be translateddefault
 - 1 PCI #1 Master GA addresses will be translated
- 2 PCI#2 Master Address Translation for GA Access
 - 0 Addresses generated by PCI #2 Master accesses of the Graphics Aperture will not be translateddefault
 - 1 PCI #2 Master GA addresses will be translated
- 1 CPU Address Translation for GA Access
 - 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated def
 - 1 CPU GA addresses will be translated
- 0 AGP Address Translation for GA Access
 - 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated def
 - 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size..... RW

- 7-0 Graphics Aperture Size
 - 11111111 1M
 - 11111110 2M
 - 11111100 4M
 - 11111000 8M
 - 11110000 16M
 - 11100000 32M
 - 11000000 64M
 - 10000000 128M
 - 00000000 256M
- 3-0 Reserved always reads 0

Offset 8B-88 - GA Translation Table Base..... RW

- 31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).
- 11-3 Reserved always reads 0
- 2 PCI Master Directly Accesses DRAM if in GART Range
 - 0 Disable default
 - 1 Enable
- 1 Graphics Aperture Enable
 - 0 Disable default
 - 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

- 0 Translation Table Noncachable
 - 0 Cachable default
 - 1 Non-cachable

Note: Setting this bit will make the address range programmed in bits 31-12 of this register non-cachable to L1/L2 with the following bits masked per the Graphics Aperture Size (offset 84 described above):

- Address bit 17 masked if Size bit-7 = 0
- Address bit 16 masked if Size bit-6 = 0
- Address bit 15 masked if Size bit-5 = 0
- Address bit 14 masked if Size bit-4 = 0
- Address bit 13 masked if Size bit-3 = 0
- Address bit 12 masked if Size bit-2 = 0
- Address bit 11 masked if Size bit-1 = 0
- Address bit 10 masked if Size bit-0 = 0

Note: If TLB miss, the TLB table is fetched by the address:

Gr Ap Trans Table Base [31:12] + A[27:22], A[21:12], 2'b00

AGP Control

Device 0 Offset A3-A0 - AGP Capability IdentifierRO

- 31-24 Reserved** always reads 00
- 23-20 Major Specification Revision** always reads 0001
Major revision # of AGP spec device conforms to
- 19-16 Minor Specification Revision** always reads 0000
Minor revision # of AGP spec device conforms to
- 15-8 Pointer to Next Item**..... always reads 00 (last item)
- 7-0 AGP ID** .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status.....RO

- 31-24 Maximum AGP Requests** always reads 07
Max # of AGP requests the device can manage (8)
- 23-10 Reserved**always reads 0s
- 9 Supports SideBand Addressing** always reads 1
- 8-2 Reserved**always reads 0s
- 1 2X Rate Supported**
Value returned can be programmed by writing to RxAC[3]
- 0 1X Rate Supported**..... always reads 1

Device 0 Offset AB-A8 - AGP Command RW

- 31-24 Request Depth** (reserved for target).. always reads 0s
- 23-10 Reserved** always reads 0s
- 9 SideBand Addressing Enable**
0 Disable..... default
1 Enable
- 8 AGP Enable**
0 Disable..... default
1 Enable
- 7-2 Reserved** always reads 0s
- 1 2X Mode Enable**
0 Disable..... default
1 Enable
- 0 1X Mode Enable**
0 Disable..... default
1 Enable

Device 0 Offset AC - AGP ControlRW

- 7-4 **Reserved**always reads 0s
- 3 **2X Rate Supported** (read also at RxA4[1])
 - 0 Not supported.....default
 - 1 Supported
- 2 **LPR In-Order Access (Force Fence)**
 - 0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests.....default
 - 1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.
- 1 **AGP Arbitration Parking**
 - 0 Disabledefault
 - 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)
- 0 **Arbitration Priority Between CPU-to-PCI Post Write and PCI Master Request After PCI Master Access**
 - 0 CPU-to-PCI write buffer has prioritydefault
 - 1 PCI master has priority

Device 0 Offset FD-FC – Reserved..... RW

- 15-1 **Reserved** always reads 0s
- 0 **Reserved (Do Not Program)** default = 0

Device 0 Offset FF-FE – Reserved RW

- 15-0 **Reserved** default = 00

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID.....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID.....RO

15-0 ID Code (reads 8598h to identify the VT82C598MVP PCI-to-PCI Bridge device)

Device 1 Offset 5-4 - Command.....RW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RO
 - 0 Fast back-to-back transactions only allowed to the same agentdefault
 - 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable**..... RO
 - 0 SERR# driver disableddefault
 - 1 SERR# driver enabled
 (SERR# is used to report parity errors if bit-6 is set).
- 7 Address / Data Stepping** RO
 - 0 Device never does steppingdefault
 - 1 Device always does stepping
- 6 Parity Error Response**.....RW
 - 0 Ignore parity errors & continuedefault
 - 1 Take normal action on detected parity errors
- 5 VGA Palette Snoop** RO
 - 0 Treat palette accesses normallydefault
 - 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)
- 4 Memory Write and Invalidate Command**..... RO
 - 0 Bus masters must use Mem Writedefault
 - 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring** RO
 - 0 Does not monitor special cyclesdefault
 - 1 Monitors special cycles
- 2 Bus Master**RW
 - 0 Never behaves as a bus master
 - 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interfacedefault
- 1 Memory Space**.....RW
 - 0 Does not respond to memory space
 - 1 Enable memory space accessdefault
- 0 I/O Space**RW
 - 0 Does not respond to I/O space
 - 1 Enable I/O space accessdefault

Device 1 Offset 7-6 - Status (Primary Bus)..... RWC

- 15 Detected Parity Error** always reads 0
- 14 Signaled System Error (SERR#)** always reads 0
- 13 Signaled Master Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... write 1 to clear
- 12 Received Target Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the target with Target-Abort write 1 to clear
- 11 Signaled Target Abort**..... always reads 0
- 10-9 DEVSEL# Timing**
 - 00 Fast
 - 01 Medium..... always reads 01
 - 10 Slow
 - 11 Reserved
- 8 Data Parity Error Detected** always reads 0
- 7 Fast Back-to-Back Capable** always reads 0
- 6 User Definable Features**..... always reads 0
- 5 66MHz Capable**..... always reads 1
- 4 Supports New Capability list**..... always reads 0
- 3-0 Reserved** always reads 0

Device 1 Offset 8 - Revision ID..... RO

7-0 VT82C598MVP Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier always reads 00

Device 1 Offset A - Sub Class Code..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer RO

7-0 Reserved always reads 0

Device 1 Offset E - Header Type RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) RO

- 7 BIST Supported** reads 0: no supported functions
- 6 Start Test** write 1 to start but writes ignored
- 5-4 Reserved** always reads 0
- 3-0 Response Code**.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus NumberRW
7-0 Primary Bus Number..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus NumberRW
7-0 Secondary Bus Number..... default = 0

Note: PCI#2 must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus NumberRW
7-0 Primary Bus Number..... default = 0

Note: PCI#2 must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1C - I/O BaseRW
7-4 I/O Base AD[15:12]..... default = 1111b
3-0 I/O Addressing Capability..... default = 0
Device 1 Offset 1D - I/O Limit.....RW
7-4 I/O Limit AD[15:12]..... default = 0
3-0 I/O Addressing Capability..... default = 0
Device 1 Offset 1F-1E - Secondary Status RO
15-0 Reserved always reads 0000
Device 1 Offset 21-20 - Memory Base RW
15-4 Memory Base AD[31:20] default = 0FFFh
3-0 Reserved always reads 0
Device 1 Offset 23-22 - Memory Limit (Inclusive)..... RW
15-4 Memory Limit AD[31:20] default = 0
3-0 Reserved always reads 0
Device 1 Offset 25-24 - Prefetchable Memory Base..... RW
15-4 Prefetchable Memory Base AD[31:20] def = 0FFFh
3-0 Reserved always reads 0
Device 1 Offset 27-26 - Prefetchable Memory Limit RW
15-4 Prefetchable Memory Limit AD[31:20].....
..... default = 0
3-0 Reserved always reads 0

Device 1 Offset 3F-3E – PCI-to-PCI Bridge ControlRW

- 15-4 Reserved** always reads 0
- 3 VGA-Present on AGP**
 - 0 Forward VGA accesses to PCI Bus #1 ...default
 - 1 Forward VGA accesses to PCI Bus #2 / AGP

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
- 2 Block / Forward ISA I/O Addresses**
 - 0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)default
 - 1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.
- 1-0 Reserved** always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

PCI Bus #2 Control

Device 1 Offset 40 - CPU-to-PCI #2 Flow Control 1..RW

- 7 CPU-PCI #2 Post Write**
0 Disabledefault
1 Enable
- 6 CPU-PCI #2 Dynamic Burst**
0 Disabledefault
1 Enable
- 5 CPU-PCI #2 One Wait State Burst Write**
0 Disabledefault
1 Enable
- 4 PCI #2 to DRAM Prefetch**
0 Disabledefault
1 Enable
- 3 PCI Master Allowed Before CPU-to-PCI Post Write Buffer is not Flushed**
0 Disabledefault
1 Enable
This option is always enabled for PCI #1
- 2 MDA Present on PCI #2**
0 Forward MDA accesses to AGP.....default
1 Forward MDA accesses to PCI #1
Note: Forward despite IO / Memory Base / Limit
Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.
Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).
- 1 PCI #2 Master Read Caching**
0 Disabledefault
1 Enable
- 0 PCI #2 Delay Transaction**
0 Disabledefault
1 Enable

Table 5. VGA/MDA Memory/IO Redirection

<u>3E[3]</u> <u>VGA</u> <u>Pres.</u>	<u>40[2]</u> <u>MDA</u> <u>Pres.</u>	<u>VGA</u> <u>is</u> <u>on</u>	<u>MDA</u> <u>is</u> <u>on</u>	<u>Axxxx,</u> <u>B8xxx</u> <u>Access</u>	<u>B0000</u> <u>-B7FFF</u> <u>Access</u>	<u>3Cx,</u> <u>3Dx</u> <u>I/O</u>	<u>3Bx</u> <u>I/O</u>
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-PCI #2 Flow Control 2 .. RWC

- 7 Retry Status**
0 No retry occurred..... default
1 Retry Occurredwrite 1 to clear
- 6 Retry Timeout Action**
0 No action taken except to record status def
1 Flush buffer for write or return all 1s for read
- 5-4 Retry Count**
00 Retry 2, backoff CPU default
01 Retry 4, backoff CPU
10 Retry 16, backoff CPU
11 Retry 64, backoff CPU
- 3 Post Write Data on Abort**
0 Flush entire post-write buffer on target-abort or master abort..... default
1 Pop one data output on target-abort or master-abort
- 2 CPU Backoff on PCI #2 Read Retry Timeout**
0 Disable..... default
1 Enable
- 1 CPU to PCI #2 I/O Write Posting**
0 Disable..... default
1 Enable
- 0 Reserved**always reads 0

Device 1 Offset 42 - PCI #2 Master Control..... RW

- 7 Read Prefetch for Enhance Command**
0 Always Perform Prefetch..... default
1 Prefetch only if Enhance Command
- 6 PCI #2 Master One Wait State Write**
0 Disable..... default
1 Enable
- 5 PCI #2 Master One Wait State Read**
0 Disable..... default
1 Enable
- 4 Extend PCI #2 Internal Master for Efficient Handling of Dummy Request Cycles**
0 Disable..... default
1 Enable
This bit is normally set to 1.
- 3 PCI #2 Master Write Timeout Asserts STOP#**
0 Disable..... default
1 Enable
- 2 PCI #2 Master Read Timeout Asserts STOP#**
0 Disable..... default
1 Enable
- 1-0 Reserved**always reads 0

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	°C
Storage temperature	-55	125	°C
Input voltage	-0.5	5.5	Volts
Output voltage ($V_{CC} = 3.1 - 3.6V$)	-0.5	$V_{CC} + 0.5$	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA=0-70°C, $V_{CC}=5V \pm 5\%$, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output low voltage	-	0.45	V	$I_{OL}=4.0mA$
V_{OH}	Output high voltage	2.4	-	V	$I_{OH}=-1.0mA$
I_{IL}	Input leakage current	-	+/-10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45 < V_{OUT} < V_{CC}$
I_{CC}	Power supply current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 6. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (VCC, VCCI, VTT, AVCC, HVCC)	3.135	3.465	Volts
5V Reference (5VREF)	4.75	5.25	Volts
Temperature	0	70	°C

Drive strength for each output pin is programmable. See Rx6D for details.

Table 7. AC Characteristics – 66/75/83/100 MHz CPU Cycle Timing

Parameter				Min	Max	Unit	Notes
ADS#	Setup Time	to	HCLK Rising	3.5		ns	0pf
WR#	Setup Time	to	HCLK Rising	3.3		ns	
M/IO#	Setup Time	to	HCLK Rising	1.7		ns	
D/C#	Setup Time	to	HCLK Rising	1.0		ns	
HITM#	Setup Time	to	HCLK Rising	3.6		ns	
CACHE#	Setup Time	to	HCLK Rising	1.6		ns	
LOCK#	Setup Time	to	HCLK Rising	3.1		ns	
BE[7:0]#	Setup Time	to	HCLK Rising	2.8		ns	
HA[31:3]	Setup Time	to	HCLK Rising	2.5		ns	
HD[63:0]	Setup Time	to	HCLK Rising	1.6		ns	
ADS#	Hold Time	from	HCLK Rising	0		ns	
WR#	Hold Time	from	HCLK Rising	0		ns	
MIO#	Hold Time	from	HCLK Rising	0		ns	
DC#	Hold Time	from	HCLK Rising	0		ns	
HITM#	Hold Time	from	HCLK Rising	0		ns	
CACHE#	Hold Time	from	HCLK Rising	0		ns	
BE[7:0]#	Hold Time	from	HCLK Rising	0		ns	
HA[31:3]	Hold Time	from	HCLK Rising	0		ns	
HD[63:0]	Hold Time	from	HCLK Rising	0		ns	
BRDY#	Valid Delay	from	HCLK Rising	0.9	1.7	ns	
NA#	Valid Delay	from	HCLK Rising	0.9	1.7	ns	
AHOLD	Valid Delay	from	HCLK Rising	0.8	1.7	ns	
BOFF#	Valid Delay	from	HCLK Rising	1.0	2.0	ns	
EADS#	Valid Delay	from	HCLK Rising	1.2	2.5	ns	
KEN# / INV#	Valid Delay	from	HCLK Rising	1.0	1.9	ns	
BE[7:0]#	Valid Delay	from	HCLK Rising	2.9	3.6	ns	
HA[31:3]	Valid Delay	from	HCLK Rising	1.2	3.8	ns	
HD[63:0]	Valid Delay	from	HCLK Rising	0.9	2.2	ns	

Table 8. AC Characteristics – 66/75/83/100 MHz L2 Cache Timing

Parameter				Min	Max	Unit	Notes
COE#	Valid Delay	from	HCLK Rising	1.8	3.6	ns	0pf
TA[7:0]	Valid Delay	from	HCLK Rising	1.7	4.3	ns	
TWE#	Valid Delay	from	HCLK Rising	1.0	2.2	ns	
GWE#	Valid Delay	from	HCLK Rising	0.8	1.6	ns	
BWE#	Valid Delay	from	HCLK Rising	0.8	1.6	ns	
CADS#	Valid Delay	from	HCLK Rising	0.9	1.8	ns	
CADV#	Valid Delay	from	HCLK Rising	0.9	1.8	ns	
TA[7:0]	Setup Time	to	HCLK Rising	3.7		ns	
TA[7:0]	Hold Time	from	HCLK Rising	0.0		ns	

Table 9. AC Characteristics – 66/75/83/100 MHz DRAM Interface Timing

Parameter				Min	Max	Unit	Notes
RAS[5:0]#	Valid Delay	from	GCLK / HCLK [†] Rising (EDO)		4.3	ns	0pf
CS[5:0]#	Valid Delay	from	GCLK / HCLK [†] Rising (SDRAM)		1.6	ns	
CAS[7:0]#	Valid Delay	from	GCLK / HCLK [†] Rising (EDO)		1.8	ns	
DQM[7:0]#	Valid Delay	from	GCLK / HCLK [†] Rising (SDRAM)		1.8	ns	
SRAS[A,B,C]#	Valid Delay	from	GCLK / HCLK [†] Rising (SDRAM)		7.4	ns	
SCAS[A,B,C]#	Valid Delay	from	GCLK / HCLK [†] Rising (SDRAM)		8.2	ns	
SWE[A,B,C]#	Valid Delay	from	GCLK / HCLK [†] Rising (SDRAM)		8.9	ns	
SWE[A,B,C]#	Valid Delay	from	GCLK / HCLK [†] Rising (EDO)		5.6	ns	
MA[11:2]	Valid Delay	from	GCLK / HCLK [†] Rising (first clock after RAS# asserts)		5.8	ns	
MA[1:0]	Valid Delay	from	GCLK / HCLK [†] Rising (Burst)		4.2	ns	
MD[63:0]	Valid Delay	from	GCLK / HCLK [†] Rising (EDO / SDRAM Write)		2.8	ns	
MD[63:0]	Setup Time	before	GCLK / HCLK [†] Rising (SDRAM Read)	1.7		ns	
MD[63:0]	Hold Time	after	GCLK / HCLK [†] Rising (SDRAM Read)	0.4		ns	

[†] Note: Memory system timing may be programmed to be synchronous with either the CPU (HCLK) or the AGP bus (GCLK).

Table 10. AC Characteristics - PCI Bus Cycle Timing

Parameter				Min	Max	Unit	Notes
AD[31:0]	Setup Time	to	PCLK Rising	7		ns	50pf
CBE[3:0]#	Setup Time	to	PCLK Rising	7		ns	
FRAME#	Setup Time	to	PCLK Rising	7		ns	
TRDY#	Setup Time	to	PCLK Rising	7		ns	
IRDY#	Setup Time	to	PCLK Rising	7		ns	
STOP#	Setup Time	to	PCLK Rising	7		ns	
DEVSEL#	Setup Time	to	PCLK Rising	7		ns	
REQ[3:0]#	Setup Time	to	PCLK Rising	12		ns	
AD[31:0]	Hold Time	from	PCLK Rising	1		ns	
CBE[3:0]#	Hold Time	from	PCLK Rising	1		ns	
FRAME#	Hold Time	from	PCLK Rising	1		ns	
TRDY#	Hold Time	from	PCLK Rising	1		ns	
IRDY#	Hold Time	from	PCLK Rising	1		ns	
STOP#	Hold Time	from	PCLK Rising	1		ns	
DEVSEL#	Hold Time	from	PCLK Rising	1		ns	
REQ[3:0]#	Hold Time	from	PCLK Rising	1		ns	
AD[31:0]	Valid Delay	from	PCLK Rising (Address Phase)	2	11	ns	
AD[31:0]	Valid Delay	from	PCLK Rising (Data Phase)	2	11	ns	
CBE[3:0]#	Valid Delay	from	PCLK Rising	2	11	ns	
FRAME#	Valid Delay	from	PCLK Rising	2	11	ns	
TRDY#	Valid Delay	from	PCLK Rising	2	11	ns	
IRDY#	Valid Delay	from	PCLK Rising	2	11	ns	
STOP#	Valid Delay	from	PCLK Rising	2	11	ns	
DEVSEL#	Valid Delay	from	PCLK Rising	2	11	ns	
GNT[3:0]#	Valid Delay	from	PCLK Rising	2	11	ns	
CBE[3:0]#	Float Delay	from	PCLK Rising	2	11	ns	
FRAME#	Float Delay	from	PCLK Rising	2	11	ns	
TRDY#	Float Delay	from	PCLK Rising	2	11	ns	
IRDY#	Float Delay	from	PCLK Rising	2	11	ns	
STOP#	Float Delay	from	PCLK Rising	2	11	ns	
DEVSEL#	Float Delay	from	PCLK Rising	2	11	ns	

Table 11. AC Characteristics – AGP Bus PCI Slave Cycle Timing

Parameter				Min	Max	Unit	Notes
GD[31:0]	Setup Time	to	GCLK Rising	5		ns	0 pF
GBE[3:0]#	Setup Time	to	GCLK Rising	5		ns	
GFRM#	Setup Time	to	GCLK Rising	5		ns	
GTRDY#	Setup Time	to	GCLK Rising	5		ns	
GIRDY#	Setup Time	to	GCLK Rising	5		ns	
GSTOP#	Setup Time	to	GCLK Rising	5		ns	
GDSEL#	Setup Time	to	GCLK Rising	5		ns	
GD[31:0]	Hold Time	from	GCLK Rising	1		ns	
GBE[3:0]#	Hold Time	from	GCLK Rising	1		ns	
GFRM#	Hold Time	from	GCLK Rising	1		ns	
GTRDY#	Hold Time	from	GCLK Rising	1		ns	
GIRDY#	Hold Time	from	GCLK Rising	1		ns	
GSTOP#	Hold Time	from	GCLK Rising	1		ns	
GDSEL#	Hold Time	from	GCLK Rising	1		ns	
GD[31:0]	Valid Delay	from	GCLK Rising (Address Phase)	1.5	6	ns	
GD[31:0]	Valid Delay	from	GCLK Rising (Data Phase)	1.5	6	ns	
GBE[3:0]#	Valid Delay	from	GCLK Rising	1.5	6	ns	
GFRM#	Valid Delay	from	GCLK Rising	1.5	6	ns	
GTRDY#	Valid Delay	from	GCLK Rising	1.5	6	ns	
GIRDY#	Valid Delay	from	GCLK Rising	1.5	6	ns	
GSTOP#	Valid Delay	from	GCLK Rising	1.5	6	ns	
GDSEL#	Valid Delay	from	GCLK Rising	1.5	6	ns	

Table 12. AC Characteristics - AGP Bus 1X Mode (PCI-66) Cycle Timing

Parameter				Min	Max	Unit	Notes
GD[31:0]	Setup Time	to	GCLK Rising (Request Phase)	5		ns	0 pf
GBE[3:0]#	Setup Time	to	GCLK Rising	5		ns	
GPIPE#	Setup Time	to	GCLK Rising	5		ns	
SBA[7:0]	Setup Time	to	GCLK Rising	5		ns	
GIRDY#	Setup Time	to	GCLK Rising	5		ns	
GRBF#	Setup Time	to	GCLK Rising	5		ns	
GREQ#	Setup Time	to	GCLK Rising	5		ns	
GD[31:0]	Hold Time	from	GCLK Rising (Data Phase)	0		ns	
GBE[3:0]#	Hold Time	from	GCLK Rising	0		ns	
GPIPE#	Hold Time	from	GCLK Rising	0		ns	
SBA[7:0]	Hold Time	from	GCLK Rising	0		ns	
GIRDY#	Hold Time	from	GCLK Rising	0		ns	
GRBF#	Hold Time	from	GCLK Rising	0		ns	
GREQ#	Hold Time	from	GCLK Rising	0		ns	
GD[31:0]	Valid Delay	from	GCLK Rising (Data Phase)		1.8	ns	
ST[2:0]	Valid Delay	from	GCLK Rising	1.5	4.6	ns	
GTRDY#	Valid Delay	from	GCLK Rising	1.5	4.6	ns	
GGNT#	Valid Delay	from	GCLK Rising	1.5	6	ns	

Table 13. AC Characteristics – AGP Bus 2X Mode Cycle Timing

Parameter				Min	Max	Unit	Notes
GD[31:0]	Setup Time	to	GDS[1:0]#	0.6		ns	0 pf
GBE[3:0]#	Setup Time	to	GDS[1:0]#	0.6		ns	
SBA[7:0]	Setup Time	to	SBS#	0.8		ns	
GDS[1:0]#	Setup Time	to	GCLK Rising (T2)	5		ns	
SBS#	Setup Time	to	GCLK Rising	4		ns	
GD[31:0]	Hold Time	from	GDS[1:0]# Falling	0.5		ns	
GBE[3:0]#	Hold Time	from	GDS[1:0]# Falling	0.5		ns	
SBA[7:0]	Hold Time	from	SBS# Falling	0		ns	
GDS[1:0]#	Hold Time	from	GCLK Rising (T2)	0		ns	
SBS#	Hold Time	from	GCLK Rising	0		ns	
GD[31:0]	Valid Delay	before	GDS[1:0]#		2.9	ns	
GD[31:0]	Valid Delay	from	GDS[1:0]#		3.6	ns	
GD[31:0]	Active Delay	from	Float		7.9	ns	
GD[31:0]	Float Delay	from	Active		8.1	ns	
GDS[1:0]#	Falling Delay	from	GCLK Rising		11.4	ns	
GDS[1:0]#	Rising Delay	from	GCLK Rising		19.4	ns	

MECHANICAL SPECIFICATIONS

Figure 9. Mechanical Specifications - 476-Pin Ball Grid Array Package

