VT82C580VPX

APOLLO VPX

Low-Cost Pentium / PCI North Bridge with 66/75MHz CPU Support and SDRAM / EDO / FPG Interface for Green PC Desktop Computers

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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
Preliminary	1/2/97	Original release based on VT82C595 Apollo VP2 data sheet revision 0.4 (VPX register set is more like Apollo VP2 than like VT82C580 Apollo VP) • Changed intro and features list to reflect Apollo VPX • Added pinouts, electrical, and mechanical specs from 580VP data sheet • Added tables of pins in alphabetical order for both chips • Changed pinouts to reflect VPX - Removed UMA (added CPURSTI and CPURSTO on MREQ0/1#) - Added 64Mb DRAM support (added MA12/13 opt on MBEN/RAS5) - Improved SDRAM support (added SWEC#/SCASC# on WE/Mgnt) • Changed registers to reflect VPX - Removed ECC registers (no pins for ECC in PQFP package) - Added Rx50[2], Rx65[2], Rx66[5], Rx68[3], Rx6B[2] - Swapped bytes of Rx54-55 & 56-57 to match silicon (same in VP2)	DH

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VIA VT82C580 APOLLO VPX

LOW-COST PENTIUM / PCI NORTH BRIDGE WITH 66/75MHZ CPU SUPPORT AND SDRAM / EDO / FPG INTERFACE FOR GREEN PC DESKTOP COMPUTERS

- **Flexible CPU Interface**
  - Supports 64-bit Pentium™, AMD 5_K86™ , AMD 6_K86™ and Cyrix 6_X86™ CPUs
  - CPU external bus speed up to 75 MHz (asynchronous) or 66MHz (synchronous) (internal 200Mhz and above)
  - Supports CPU internal write-back cache
  - System management interrupt, memory remap and STPCLK mechanism
  - Cyrix 6_X86 linear burst support
  - CPU NA# / Address pipeline capability
- **Low Cost**
  - PQFP packaging for low-cost implementation of 64-bit Pentium-CPU, 64-bit system memory, and 32-bit PCI
  - VT82C580 Apollo VPX Chipset: **VT82C585VPX** system controller and **VT82C587VP** Data Buffers
  - **VT82C586B** includes UltraDMA-33 EIDE, USB, and Keyboard / Mouse Interfaces plus RTC / CMOS
  - Six TTLs for a complete main board implementation
- **PCI/ISA Green PC Ready**
  - Supports 3.3V or 5V interface to CPU, system memory, and / or PCI bus
  - Supports CPUs with internal voltages below 3.3V
  - PC-97 compatible using VT82C586B South Bridge with ACPI Power Management
- **Advanced Cache Controller**
  - Direct map write back or write through secondary cache
  - Pipelined burst synchronous SRAM (PBSRAM) cache support
  - Flexible cache size: 0K/256K/512K/1M/2MB
  - 32 byte line size to match the primary cache
  - Integrated 10-bit tag comparator
  - 3-1-1-1 read/write timing for PBSRAM access at 66/75 MHz
  - 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access at 66/75 MHz
  - Sustained 3 cycle write access for PBSRAM access or CPU to DRAM and PCI bus post write buffers at 66/75 MHz
  - Data streaming for simultaneous primary and secondary cache line fill
  - System and video BIOS cacheable and write-protect
  - Programmable cacheable region and cache timing

- **Fast DRAM Controller**
  - Fast Page Mode/EDO/Synchronous-DRAM support in a mixed combination
  - Mixed 1M/2M/4M/8M/16MxN DRAMs
  - 6 banks up to 512MB DRAMs
  - Flexible row and column addresses
  - 64-bit or 32-bit data width in arbitrary mixed combination
  - 3.3v and 5v DRAM without external buffers
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support (14 MA lines)
  - Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
  - Concurrent DRAM writeback
  - Speculative DRAM access
  - Read around write capability for non-stalled CPU read
  - Burst read and write operation
  - 4-2-2-2 on page, 7-2-2-2 start page and 9-2-2-2 off page timing for EDO DRAMs at 50/60 MHz
  - 5-2-2-2 on page, 8-2-2-2 start page and 11-2-2-2 off page timing for EDO DRAMs at 66 MHz
  - 6-1-1-1 on page, 8-1-1-1 start page and 10-1-1-1 off page for SDRAMs at 66 MHz
  - 5-2-2-2-3-1-2-2 back-to-back access for EDO DRAM at 66 MHz
  - 6-1-1-1-3-1-1-1 back-to-back access for SDRAM at 66 MHz
  - BIOS shadow at 16KB increment
  - Decoupled and burst DRAM refresh with staggered RAS timing
  - Programmable refresh rate, CAS-before-RAS refresh and refresh on populated banks only
- **Intelligent PCI Bus Controller**
  - 32 bit 3.3/5v PCI interface
  - Synchronous divide-by-two and asynchronous PCI bus interface
  - PCI master snoop ahead and snoop filtering
  - PCI master peer concurrency
  - Synchronous bus to CPU clock with divide-by-two from the CPU clock
  - Automatic detection of data streaming burst cycles from CPU to the PCI bus
  - Five levels (double-words) of CPU to PCI posted write buffers
  - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132Mbyte/sec
  - Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
  - Complete steerable PCI interrupts
  - Supports L1 write-back forward to PCI master read to minimize PCI read latency
  - Supports L1 write-back merged with PCI master post-write to minimize DRAM utilization
  - Provides transaction timer to fairly arbitrate between PCI masters
  - PCI-2.1 compliant
- **Built-in nand-tree pin scan test capability**
- **0.6um mixed voltage, high speed / low power CMOS process**
- **VT82C585VPX: 208-pin PQFP Package**
- **VT82C587VP: 100-pin PQFP Package**

OVERVIEW

The VT82C580VPX ***Apollo-VPX*** is a high performance, cost-effective and energy efficient chip set for implementation of PCI / ISA desktop and notebook personal computer systems based on 64-bit P54C/Pentium/K5/K6/M1 super-scalar processors. The CPU / cache connection is supported using an "asynchronous" interface up to 75Mhz CPU external bus speed (with CPU internal speed up to 200Mhz and above), with CPUs such as the "P200+" processors from Cyrix / IBM Microelectronics. The "asynchronous" interface allows the processor external bus frequency to be increased above 66MHz while still allowing the PCI bus to run at the specified top frequency of 33MHz. The chipset also supports CPU external bus speeds up to 66MHz in "synchronous" mode, so may also be used in boards designed around the popular VT82C580VP (Apollo VP) chipset. The 66MHz external bus speed is used primarily for Intel and AMD processors. The CPU, DRAM and PCI bus are all independently powered so that each of the bus can be run at 3.3v or 5v, independently. The ISA bus always runs at 5v.

The VT82C580VPX chip set consists of the VT82C585VPX system controller, the VT82C586B PCI to ISA bridge, and two instances of the VT82C587VP data buffers. The VT82C585VPX is the only different component in a VPX-based system from the chips used in an Apollo VP system: the same VT82C586B South Bridge chip may be used with all VIA North Bridge chips (Pentium and PentiumPro-based designs) and the VT82C587VP Data Buffer is the same chip as is used in Apollo VP designs.

The CPU bus is minimally loaded with only the CPU, secondary cache and the chip set. The VT82C587VP data buffers isolate the CPU bus from the DRAM and PCI bus so that CPU and cache operation may run reliably at the high frequencies demanded by today's processors. The VT82C585VPX contains multiple deep FIFOs to allow efficient concurrent operation and DRAM utilization. The VT82C586B PCI to ISA bridge includes integrated 206-style IPC (DMA, interrupt controller and timer), integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, ACPI-compatible Power Management subsystem, integrated master mode enhanced IDE / UltraDMA-33 disk controller with full scatter and gather capability, and integrated USB (universal serial bus) interface with root hub and two function ports with built-in physical layer transceivers (refer to the separate VT82C586B Data Sheet for additional information). A complete main board can be implemented with only six TTLs. Refer to Figure 1 for the system block diagram.

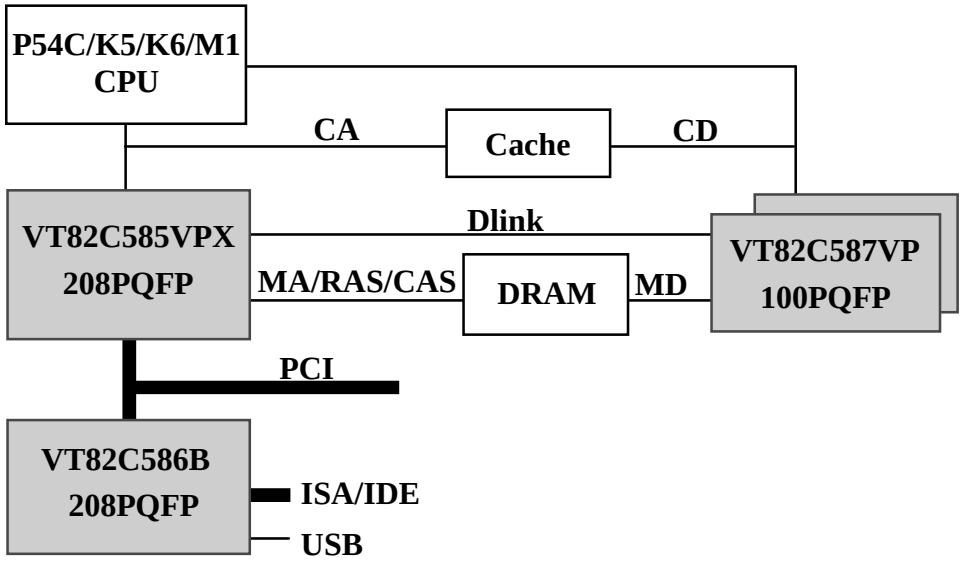

Figure 1. Apollo VPX System Block Diagram

The secondary (L2) cache is based on Burst Synchronous (Pipelined or non-pipelined) SRAM cache modules from 128KB to 2MB. For burst synchronous SRAMs, 3-1-1-1 timing can be achieved for both read and write transactions at 66Mhz. Four cache lines (16 quadwords) of CPU / cache to DRAM write buffers with concurrent write-back capability are included in the VT82C587VP data buffer chips to speed up cache read and write miss cycles.

The VT82C580VPX supports six banks of DRAMs up to 512KB. The DRAM controller supports Standard Page Mode DRAM, EDO-DRAM, and Synchronous DRAM in a flexible mixed/match manner. Synchronous DRAM allows zero wait state bursting between the DRAM and the VT82C587VP data buffers at 66/75Mhz. The six banks of DRAM are grouped into three pairs with

an arbitrary mixture of 256K/512K/1M/2M/4M/8M/16MxN DRAMs. Each bank may be populated with either 32bit or 64bit data width.

The VT82C580VPX supports the shadowing of the system, video and other BIOS to speed up access. The video and system BIOS can also be write-protected and made cacheable. Access cycles to either E , D or C segment can be programmed to be an on-board EPROM cycle to allow the combination of system and video BIOS for an all-in-one system board implementation. The VT82C580VPX can also be programmed to recognize write cycles as EPROM cycles to support field upgradability of flash EPROM BIOS.

The VT82C580VPX supports a 3.3/5v 32-bit PCI bus with 64-bit to 32-bit data conversion. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. Consecutive CPU addresses are converted into burst PCI cycles with byte merging capability for optimal CPU to PCI throughput. A 16-bit fast data link is established between the two VT82C587VP data units and the VT82C585VPX system controller so that the address, data and command information for CPU to PCI bus transactions is contained in the same chip. This arrangement, unique to the VT82C580VP and VT82C580VPX chipsets is crucial in achieving zero wait state buffer movement and implementing sophisticated and upgradable buffer management schemes such as the byte merging. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chipset also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, the chipset supports advanced features such as snoop ahead, snoop filtering, L1 write-back forward to PCI master and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. The VT82C586B PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delayed transactions to allow efficient PCI bus utilization and is PCI-2.1 compliant.

The integrated master mode IDE controller of the VT82C586B supports a dual-channel / four-device enhanced IDE bus with enhancements for UltraDMA-33 operation and has sixteen levels of double-word prefetch and write buffers. The data bus, control signals, write buffers and prefetch buffers are separated from those of the PCI bus so that performance and electrical loading are optimized. The command and recovery time of each IDE device can be individually programmed in units of PCI bus clocks to achieve optimal speed of the device up to 33MB/s. Other features of the IDE controller include interlaced dual channel commands, full scatter and gather capability, bus master programming interface for ATA controllers, SFF-8038 compliance and complete software driver support. The VT82C586B South Bridge also includes an integrated RTC with extended 256-byte CMOS, integrated keyboard controller, integrated USB (Universal Serial Bus) controller, and a sophisticated power management unit that is compliant with both APM 1.1 and ACPI 0.9 to allow design of PC systems that are fully PC-97 compliant.

The VT82C580VPX is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook PCI/ISA computer systems.

PINOUTS

VT82C585VPX Pinouts

Figure 2. VT82C585VPX Pin Diagram (Top View)

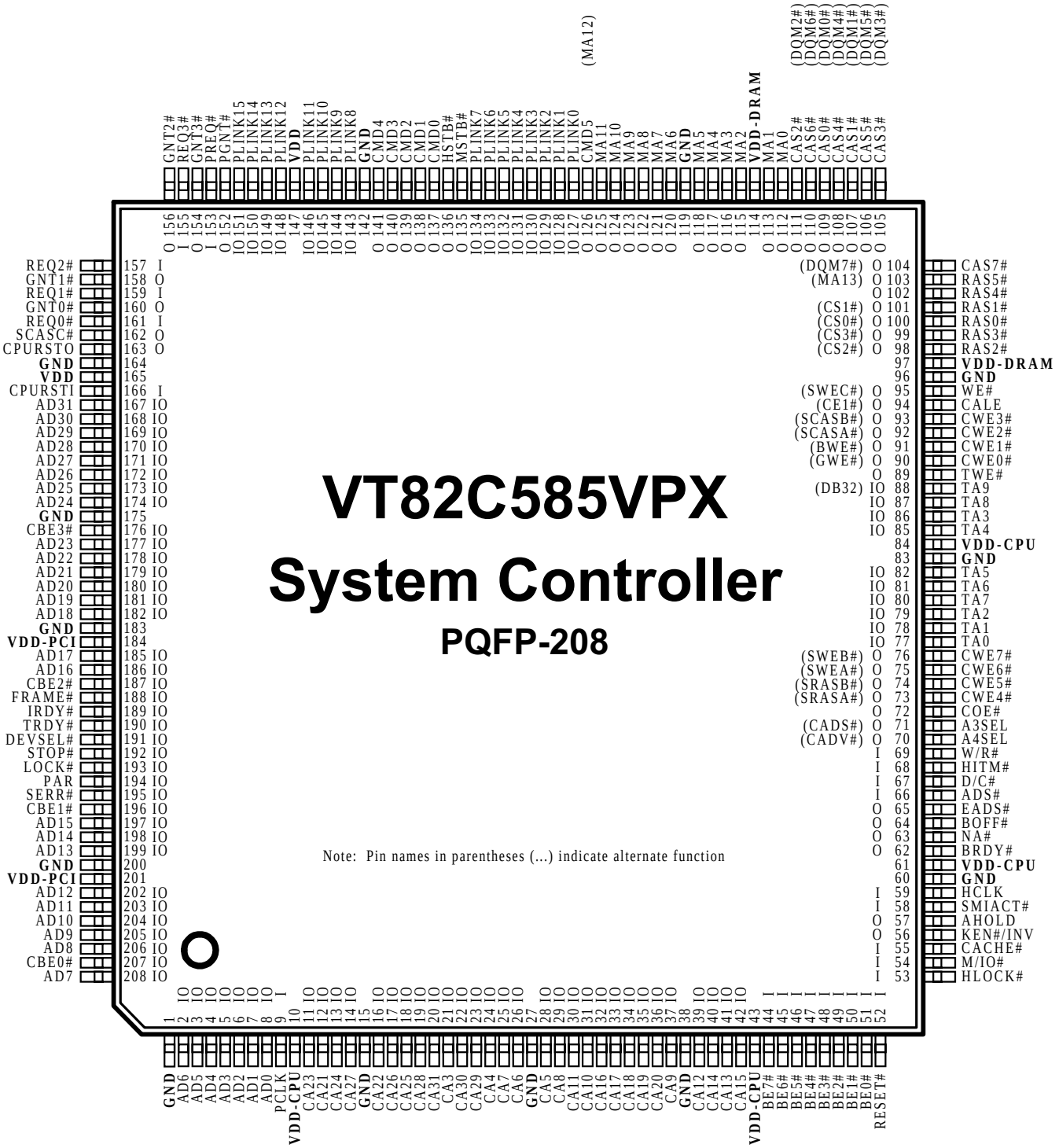

Figure 3. VT82C585VPX Pin List (Alphabetical Order)

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
71	A3SEL / CADS#	42	CA15	107	DQM1# / CAS1#	132	PLINK5
70	A4SEL / CADV#	32	CA16	111	DQM2# / CAS2#	133	PLINK6
8	AD0	33	CA17	105	DQM3# / CAS3#	134	PLINK7
7	AD1	34	CA18	108	DQM4# / CAS4#	143	PLINK8
6	AD2	35	CA19	106	DQM5# / CAS5#	144	PLINK9
5	AD3	36	CA20	110	DQM6# / CAS6#	145	PLINK10
4	AD4	12	CA21	104	DQM7# / CAS7#	146	PLINK11
3	AD5	16	CA22	65	EADS#	148	PLINK12
2	AD6	11	CA23	188	FRAME#	149	PLINK13
208	AD7	13	CA24	1	**GND**	150	PLINK14
206	AD8	18	CA25	15	**GND**	151	PLINK15
205	AD9	17	CA26	27	**GND**	153	PREQ#
204	AD10	14	CA27	38	**GND**	100	RAS0# / CS0#
203	AD11	19	CA28	60	**GND**	101	RAS1# / CS1#
202	AD12	23	CA29	83	**GND**	98	RAS2# / CS2#
199	AD13	22	CA30	96	**GND**	99	RAS3# / CS3#
198	AD14	20	CA31	119	**GND**	102	RAS4#
197	AD15	55	CACHE#	142	**GND**	103	RAS5# / MA13
186	AD16	71	CADS# / A3SEL	164	**GND**	161	REQ0#
185	AD17	70	CADV# / A4SEL	175	**GND**	159	REQ1#
182	AD18	94	CALE / CE1#	183	**GND**	157	REQ2#
181	AD19	109	CAS0# / DQM0#	200	**GND**	155	REQ3#
180	AD20	107	CAS1# / DQM1#	160	GNT0#	52	RESET#
179	AD21	111	CAS2# / DQM2#	158	GNT1#	92	SCASA# / CWE2#
178	AD22	105	CAS3# / DQM3#	156	GNT2#	93	SCASB# / CWE3#
177	AD23	108	CAS4# / DQM4#	154	GNT3#	162	SCASC#
174	AD24	106	CAS5# / DQM5#	90	GWE# / CWE0#	195	SERR#
173	AD25	110	CAS6# / DQM6#	59	HCLK	58	SMIACT#
172	AD26	104	CAS7# / DQM7#	68	HITM#	73	SRASA# / CWE4#
171	AD27	207	CBE0#	53	HLOCK#	74	SRASB# / CWE5#
170	AD28	196	CBE1#	136	HSTB#	192	STOP#
169	AD29	187	CBE2#	189	IRDY#	75	SWEA# / CWE6#
168	AD30	176	CBE3#	56	KEN#/INV	76	SWEB# / CWE7#
167	AD31	94	CE1# / CALE	193	LOCK#	95	SWEC# / WE#
66	ADS#	137	CMD0	54	M/IO#	77	TA0
57	AHOLD	138	CMD1	112	MA0	78	TA1
51	BE0#	139	CMD2	113	MA1	79	TA2
50	BE1#	140	CMD3	115	MA2	86	TA3
49	BE2#	141	CMD4	116	MA3	85	TA4
48	BE3#	126	CMD5 / MA12	117	MA4	82	TA5
47	BE4#	72	COE#	118	MA5	81	TA6
46	BE5#	166	CPURSTI	120	MA6	80	TA7
45	BE6#	163	CPURSTO	121	MA7	87	TA8
44	BE7#	100	CS0# / RAS0#	122	MA8	88	TA9 / DB32
64	BOFF#	101	CS1# / RAS1#	123	MA9	190	TRDY#
62	BRDY#	98	CS2# / RAS2#	124	MA10	89	TWE#
91	BWE# / CWE1#	99	CS3# / RAS3#	125	MA11	147	**VDD**
21	CA3	90	CWE0# / GWE#	126	MA12 / CMD5	165	**VDD**
24	CA4	91	CWE1# / BWE#	103	MA13 / RAS5#	10	**VDD-CPU**
28	CA5	92	CWE2# / SCASA#	135	MSTB#	43	**VDD-CPU**
26	CA6	93	CWE3# / SCASB#	63	NA#	61	**VDD-CPU**
25	CA7	73	CWE4# / SRASA#	194	PAR	84	**VDD-CPU**
29	CA8	74	CWE5# / SRASB#	9	PCLK	97	**VDD-DRAM**
37	CA9	75	CWE6# / SWEA#	152	PGNT#	114	**VDD-DRAM**
31	CA10	76	CWE7# / SWEB#	127	PLINK0	184	**VDD-PCI**
30	CA11	67	D/C#	128	PLINK1	201	**VDD-PCI**
39	CA12	88	DB32 / TA9	129	PLINK2	69	W/R#
41	CA13	191	DEVSEL#	130	PLINK3	95	WE# / SWEC#
40	CA14	109	DQM0# / CAS0#	131	PLINK4		

Table 1. VT82C585VPX Pin Descriptions

Signal Name	Pin No.	Power	I/O	Signal Description
Clock Control				
HCLK	59	CPU	I	**Host Clock.** This pin receives a buffered host clock which is used by all VT82C585VPX logic in the Host CPU clock domain. This pin should connect to the same clock net that is used to clock the CPU.
PCLK	9	CPU	I	**PCI Clock.** Used by all logic in the PCI clock domain. Typically host clock divided by two for 66MHz CPU operation but is not required to be synchronous with HCLK. Maximum 33MHz to meet PCI specifications.
Reset Control				
RESET#	52	PCI	I	**Reset.** Resets the chip and sets all register bits to their default values.
CPURSTI	166	PCI	I	**CPU Reset In.** Used to synchronize the CPURST signal from the south bridge chip to the CPU (required for 75MHz operation, optional for 66).
CPURSTI	162	CPU	O	**CPU Reset Out.** Synchronized CPURST signal to the CPU.
CPU Interface				
ADS#	66	CPU	I	**Address Strobe.** The CPU asserts ADS# in T1 of the CPU bus cycle.
M/IO#	54	CPU	I	**Memory / IO**
W/R#	69	CPU	I	**Write / Read**
D/C#	67	CPU	I	**Data / Control**
BE#[7:0]	44-51	CPU	I	**Byte Enables.** Indicate byte lanes accessed in the current CPU cycle.
CA[31:3]	20, 22-23, 19, 14, 17-18, 13, 11, 16, 12, 36-32, 42, 40-41, 39, 30-31, 37, 29, 25-26, 28, 24, 21	CPU	B	**Address Bus.** CA[31:3] connect to the address bus of the CPU. During CPU cycles CA[31:3] are inputs. These signals are driven by the VT82C585VPX during cache snooping operations.
BRDY#	62	CPU	O	**Bus Ready.** The VT82C585VPX asserts BDRY# to indicate to the CPU that data is available on reads or has been received on writes.
EADS#	65	CPU	O	**External Address Strobe.** Asserted by the VT82C585VPX to inquire the L1 cache when serving PCI master accesses to main memory.
KEN#/INV	56	CPU	O	**Cache Enable / Invalidate.** KEN#/INV functions as both the KEN# signal during CPU read cycles and INV during L1 cache snoop cycles.
HITM#	68	CPU	I	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	53	CPU	I	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
CACHE#	55	CPU	I	**Cacheable.** Asserted by the CPU during a read cycle to indicate the CPU can perform a burst line fill. Asserted by the CPU during a write cycle to indicate that the CPU will perform a burst write-back cycle.
AHOLD	57	CPU	O	**Address Hold.** AHOLD is asserted while PCI masters are accessing main memory. AHOLD is held for the duration of PCI burst transfers.
NA#	63	CPU	O	**Next Address**
BOFF#	64	CPU	O	**Back Off.** Asserted by the VT82C585VPX when required to terminate a CPU cycle that was in progress.
SMIACT#	58	CPU	I	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of an SMI.

Cache Control				
COE#	72	CPU	O	**Cache SRAM Output Enable**
CWE#[7:0] / SWE#A-B, SRAS#A-B, SCAS#A-B, BWE#, GWE#	76-73, 93-90	CPU	O	**Multifunction Pins:** Global write option off (Rx50[2] = 0): **Cache SRAM Write Enables** for each byte. Global write option on (Rx50[2] = 1): **Synchronous DRAM Command** indicators and **BWE#/GWE#** for global write SRAM control.
TWE#	89	CPU	O	**Tag Write Enable.** When asserted , new state and tag addresses are written into the external tag.
A3SEL / CADS#	71	CPU	O	**Multifunction Pin:** Async SRAM: **Cache Address 3**. A3SEL is used to sequence through the Quad-words in a cache line during a burst operation. Sync SRAM: **Cache Address Strobe**. Assertion causes the burst SRAM to load the BSRAM address register from BSRAM address pin.
A4SEL / CADV#	70	CPU	O	**Multifunction Pin:** Async SRAM: **Cache Address 4.** A4SEL is used to sequence through the Quad-words in a cache line during a burst operation. Sync SRAM: **Cache Advance**. Assertion causes the burst SRAM to advance to the next Quad-word in the cache line.
TA[9] / DB32 TA[8:0]	88, 87, 80, 81, 82, 85, 86, 79-77	CPU	B	**Tag Address.** These are inputs during CPU accesses, outputs during L2 cache line fills, and L2 line invalidates during inquire cycles. TA9 is a multi-function pin and will act as **DB32** to the VT82C587VP chips when 32-bit DRAM mode is enabled.
CALE / CE1#	94	CPU	O	**Multifunction Pin:** Async SRAM: **Cache Address Latch.** CALE is used to control the cache address latches. Sync SRAM: **Chip Enable 1**. CE1# is used as chip-select 1 for BSRAM.

DRAM Control				
MA[11:0]	125-120, 118-115, 113-112	DRAM	O	**Memory Address.** DRAM address lines 0-11.
MA12 / CMD5	126	DRAM	O	Dual Function Pin: **Command 5.** This function is provided for backwards compatibility: In VT82C585VP-based designs (i.e., non-VPX), this pin (previously called "MBEN#) was connected to the VT82C587VP "CMD5" pin for UMA control. For compatibility with those systems, this pin may be programmed to remain high at all times. In new or modified designs, the VT82C587VP CMD5 input may be tied high so that this pin may be used to drive **Memory Address 12** for support of larger memory sizes.
RAS5# / MA13	103	DRAM	O	FPG/EDO/BEDO DRAM: **Row Address Strobe** for bank 5 or **Memory Address 13**. Synchronous DRAM: **Memory Address 13**
RAS4#	102	DRAM	O	FPG/EDO/BEDO DRAM: **Row Address Strobe** for bank 4 Synchronous DRAM: **Unused**
RAS[3:0]# / CS[3:0]#	99-98, 101-100	DRAM		FPG/EDO/BEDO DRAM: **Row Address Strobe** for each bank. Synchronous DRAM: **Chip Select** for each bank.
CAS[7:0]# / DQM[7:0]#	104, 110, 106, 108, 105, 111, 107, 109	DRAM	O	FPG/EDO/BEDO DRAM: **Column Address Strobe** for each byte lane. Synchronous DRAM: **Data Mask** for each byte lane.
SRASA#, SRASB#	73, 74	DRAM	O	FPG/EDO/BEDO DRAM: Inactive. Synchronous DRAM: **Row Address Command Indicators** (three identical copies for better drive).
SCASA#, SCASB#, SCASC#	92, 93	DRAM	O	FPG/EDO/BEDO DRAM: Inactive. Synchronous DRAM: **Column Address Command Indicators** (three identical copies for better drive).
SWEA#, SWEB#, SWEC# / WE#	75, 76, 95	DRAM	O	FPG/EDO/BEDO DRAM: **Write Enable** (pin 95). Pins 75-76 inactive. Synchronous DRAM: **Write Enable Command Indicators** (three identical copies for better drive).

VT82C587VP Interface				
PLINK[15:0]	151-148, 146-143, 134-127	DRAM	B	**PCI Link.** This is the data path between CPU / main memory and the PCI bus. PCI main memory reads and CPU-to-PCI writes are driven onto these pins by the VT82C587VP. CPU reads from PCI and PCI writes to main memory are received on this bus by the VT82C587VP. Each VT82C587VP is connected to one byte of this bus.
MSTB#	135	DRAM	O	**Memory Strobe.** Assertion causes data to be posted in the DRAM Write Buffer.
HSTB#	136	DRAM	O	**Host Strobe.** Assertion causes data to be posted in the CPU Read Buffer.
CMD[4:0]	141-137	DRAM	O	**Command.** The VT82C585VPX uses these signals to control the buffers in the VT82C587VP chips. See also pin 126 above for CMD5 function.

Table 2. VT82C585VP vs. VT82C585VPX Pinout Differences Summary

Pin #	VT82C585VP	VT82C585VPX
95	WE#	WE# / SWEC#
103	RAS5#	RAS5# / MA13
126	MBEN#	CMD5 / MA12
162	MGNT#	SCASC#
163	MREQ0#	CPURSTO
166	MREQ1#	CPURSTI

PCI Bus Interface				
FRAME#	188	PCI	B	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	167-174, 177-182, 185, 186, 197-199, 202-206, 208, 2-8	PCI	B	**Address / Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
C/BE#[3:0]	176, 187, 196, 207	PCI	B	**Command / Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	189	PCI	B	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	190	PCI	B	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	192	PCI	B	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	191	PCI	B	**Device Select.** This signal is driven by the VT82C585VPX when a PCI initiator is attempting to access main memory. It is an input when the VT82C585VPX is acting as a PCI initiator.
PAR	194	PCI	B	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	195	PCI	B	**System Error.** The VT82C585VPX will pulse this signal when it detects a system error condition.
LOCK#	193	PCI	B	**Lock.** Used to establish, maintain, and release resource lock on the PCI bus
PREQ#	153	PCI	I	**PCI Request.** This signal comes from the south bridge chip (VT82C586, 586A, or 586B). PREQ# is the south bridge chip's request for the PCI bus.
PGNT#	152	PCI	O	**PCI Grant.** This signal driven by the VT82C585VPX to grant PCI access to the VT82C586, 586A, or 586B south bridge.
REQ#[3:0]	155, 157, 159, 161	PCI	I	**Request.** PCI master requests for the PCI bus.
GNT#[3:0]	154, 156, 158, 160	PCI	O	**Grant.** Permission is given to the master to use the PCI bus.

Power and Ground				
VDD	147, 165	5V	I	**Power Supply for the internal logic of the VT82C585VPX chip (5v)**
VDD-CPU	10, 43, 61, 84	CPU	I	**Power Supply for the CPU Bus (3.3v or 5v)**
VDD-PCI	184, 201	PCI	I	**Power Supply for the PCI Bus (3.3v or 5v)**
VDD-DRAM	97, 114	DRAM	I	**Power Supply for the DRAM Bus (3.3v or 5v)**
GND	1, 15, 27, 38, 60, 83, 96, 119, 142, 164, 175, 183, 200	0V	I	**Ground**

VT82C587VP Pinouts

Figure 4. VT82C587VP Pin Diagram (Top View)

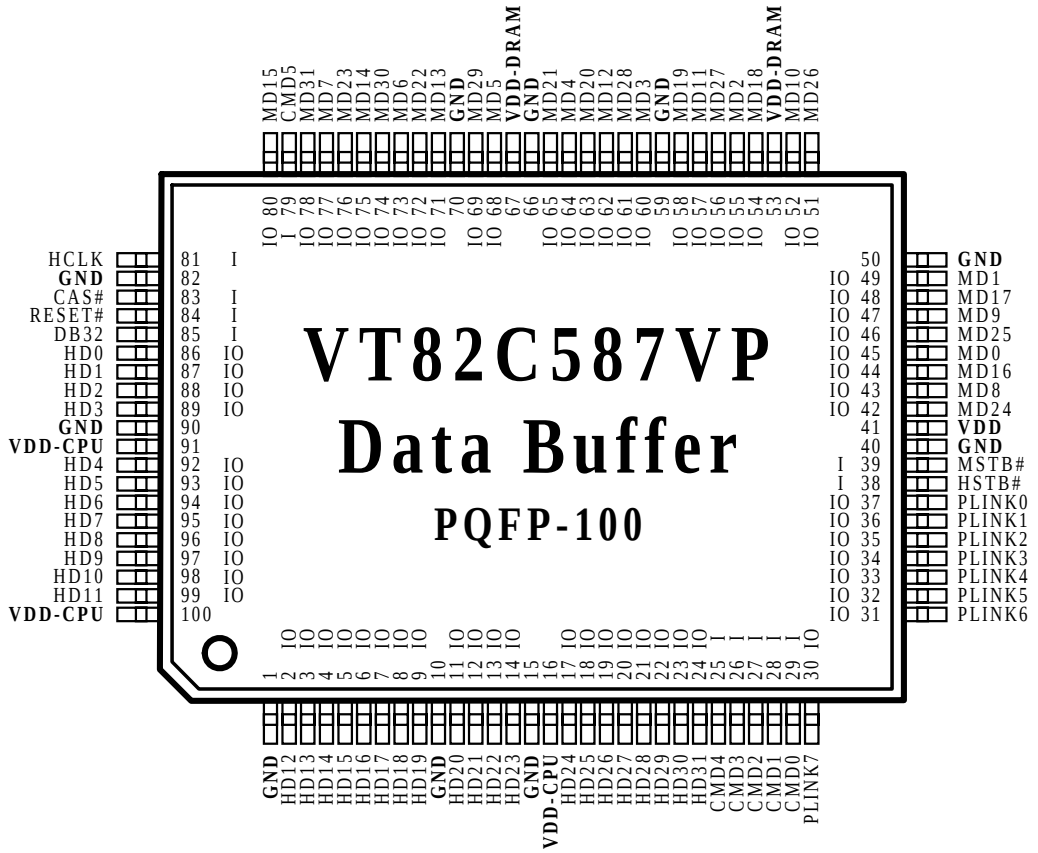

Figure 5. VT82C587VP Pin List (Alphabetical Order)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
83	CAS#	94	HD06	24	HD31	76	MD23
29	CMD0	95	HD07	38	HSTB#	42	MD24
28	CMD1	96	HD08	45	MD00	46	MD25
27	CMD2	97	HD09	49	MD01	51	MD26
26	CMD3	98	HD10	55	MD02	56	MD27
25	CMD4	99	HD11	60	MD03	61	MD28
79	CMD5	2	HD12	64	MD04	69	MD29
85	DB32	3	HD13	68	MD05	74	MD30
1	**GND**	4	HD14	73	MD06	78	MD31
10	**GND**	5	HD15	77	MD07	39	MSTB#
15	**GND**	6	HD16	43	MD08	37	PLINK0
40	**GND**	7	HD17	47	MD09	36	PLINK1
50	**GND**	8	HD18	52	MD10	35	PLINK2
59	**GND**	9	HD19	57	MD11	34	PLINK3
66	**GND**	11	HD20	62	MD12	33	PLINK4
70	**GND**	12	HD21	71	MD13	32	PLINK5
82	**GND**	13	HD22	75	MD14	31	PLINK6
90	**GND**	14	HD23	80	MD15	30	PLINK7
81	HCLK	17	HD24	44	MD16	84	RESET#
86	HD00	18	HD25	48	MD17	41	**VDD**
87	HD01	19	HD26	54	MD18	16	**VDD-CPU**
88	HD02	20	HD27	58	MD19	91	**VDD-CPU**
89	HD03	21	HD28	63	MD20	100	**VDD-CPU**
92	HD04	22	HD29	65	MD21	53	**VDD-DRAM**
93	HD05	23	HD30	72	MD22	67	**VDD-DRAM**

Table 3. VT82C587VP Pin Descriptions

Signal Name	Pin No.	Power	I/O	Signal Description
CPU Data Port				
HD[31:0]	24-17, 14-11, 9-2, 99-92, 89-86	CPU	B	**Host CPU Data**. These signals are connected to the CPU data bus. The CPU data bus is interleaved between the two VT82C587VP chips for every byte, effectively creating an even and odd 587VP.
DRAM Data Port				
MD[31:0]	78, 74, 69, 61, 56, 51, 46, 42, 76, 72, 65, 63, 58, 54, 48, 44, 80, 75, 71, 62, 57, 52, 47, 43, 77, 73, 68, 64, 60, 55, 49, 45	DRAM	B	**Memory Data**. These signals are connected to the DRAM data bus. The DRAM data bus is interleaved between the two VT82C587VP for every byte, effectively creating an even and odd VT82C587VP.
VT82C585VPX Interface				
DB32	85	DRAM	I	**DRAM Width**. This is used to control the width of the DRAM data bus
CMD[5:0]	79, 25-29	DRAM	I	**Command**. The buffers in the VT82C587VP are controlled by the VT82C585VPX through these command signals. The CMD5 input is used for UMA support only so may be tied high. The VT82C585VPX may be programmed to drive its CMD5 output high at all times for backwards compatibility with 82C585VP-based (non-VPX) designs.
HSTB#	38	DRAM	I	**Host Data Strobe**. Assertion causes data to be posted in the CPU read buffer
MSTB#	39	DRAM	I	**Memory Strobe**. Assertion causes data to be posted in the DRAM write buffer.
PLINK[7:0]	30-37	DRAM	B	**PCI Link**. These signals are connected to the PLINK data bus on the VT82C585VPX. This the data path between the VT82C585VPX and the VT82C587VP chips. Each VT82C587VP connects to one-byte of the 16-bit bus.
Clock and Miscellaneous Control				
HCLK	81	CPU	I	**Host Clock**. Primary clock input used to drive the part.
RESET#	84	CPU	I	**Host Reset**. Primary reset signal for the VT82C587VP.
CAS#	83	CPU	I	**DRAM CAS Synchronization**. Connects to any DRAM CAS signal to synchronize the clocks with DRAM CAS. Required for Burst EDO DRAM operation only; can be tied high if BEDO DRAMs will never be used in the system design. It is recommended to maintain same skew among the eight DRAM CAS# lines for Burst EDO operation.
Power and Ground				
VDD	41	5V	I	**Power Supply** for the **Internal Logic** of the chip (5v)
VDD-DRAM	53, 67	DRAM	I	**Power Supply** for the **DRAM** interface (3.3v or 5v)
VDD-CPU	16, 91, 100	CPU	I	**Power Supply** for the **CPU** bus (3.3v or 5v).
GND	1, 10, 15, 40, 50, 59, 66, 70, 79, 90	0V	I	**Ground**

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C585VPX. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 4. VT82C585VPX Registers

Configuration Space VT82C585VPX Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0585	RO
5-4	Command	0007	**RW**
7-6	Status	02A0	**WC**
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2F	-reserved- (unassigned)	00	—
30-33	-reserved- (expan ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (minimum grant)	00	—
3F	-reserved- (maximum latency)	00	—

Configuration Space VT82C585VPX-Specific Registers

Offset	Cache Control	Default	Acc
50	Cache Control 1	00	RW
51	Cache Control 2	00	RW
52	Non-Cacheable Control	02	RW
53	System Performance Control	00	RW
54	Non-Cacheable Region #1 High Byte	00	RW
55	Non-Cacheable Region #1 Low Byte	00	RW
56	Non-Cacheable Region #2 High Byte	00	RW
57	Non-Cacheable Region #2 Low Byte	00	RW

Offset	DRAM Control	Default	Acc
58	DRAM Configuration 1	40	RW
59	DRAM Configuration 2	05	RW
5A-5F	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[29:22])	01	RW
5B	Bank 1 Ending (HA[29:22])	01	RW
5C	Bank 2 Ending (HA[29:22])	01	RW
5D	Bank 3 Ending (HA[29:22])	01	RW
5E	Bank 4 Ending (HA[29:22])	01	RW
5F	Bank 5 Ending (HA[29:22])	01	RW
60	DRAM Type	00	RW
61	Shadow RAM Control C0000-CFFFF	00	RW
62	Shadow RAM Control D0000-DFFFF	00	RW
63	Shadow RAM Control E0000-FFFFF	00	RW
64	DRAM Reference Timing	AB	RW
65	DRAM Timing Control 1	00	RW
66	DRAM Timing Control 2	00	RW
67	32-Bit DRAM Width	00	RW
68	-reserved- (do not program)	00	RW
69	-reserved- (do not program)	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Refresh Control	00	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E-6F	-reserved-	00	—

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	**WC**
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	-reserved- (chip test - do not program)	00	RW
78-FF	-reserved-	00	—

Configuration Space I/O

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address .....RW

31 Configuration Space Enable
- 0 Disabled .....default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved ..... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number
Used to select a specific DWORD in the device's configuration space

1-0 Fixed ..... always reads 0

Port CFF-CFC - Configuration Data .....RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

PCI Configuration Space Header

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC.

Offset 1-0 - Vendor ID ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID ..... RO

15-0 ID Code (reads 585h to identify the VT82C585VPX)

Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RW
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RW
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space ..... RO
- 0 Does not respond to I/O space
- 1 Responds to I/O space ..... default

Offset 7-6 - Status ..... RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected. May be set even if error response is disabled (command register bit-6) .. .. write one to clear

14 Signaled System Error ..... always reads 0
- 1 SERR# asserted

13 Signaled Master Abort ..... always reads 0
- 1 Transaction aborted by the master

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target ..... write 1 to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 1

6 Reserved ..... always reads 0

5 66MHz Capable ..... always reads 1

4-0 Reserved ..... always reads 0

Offset 8 - Revision ID ..... RO

0-7 VT82C585VPX Chip Revision Code (00=First Silicon)

Offset 9 - Programming Interface ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

0-7 Interface Identifier ..... always reads 00

Offset A - Sub Class Code ..... RO

0-7 Sub Class Code ..... reads 00 to indicate Host Bridge

Offset B - Base Class Code ..... RO

0-7 Base Class Code .. reads 06 to indicate Bridge Device

Offset D - Latency Timer ..... RW

Specifies the latency timer value in PCI bus clocks. Bits 0-2 are fixed, resulting in a granularity of 8 clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved ..... always reads 0

Offset E - Header Type ..... RO

0-7 Header Type Code ..... reads 00: single function

Offset F - Built In Self Test (BIST) ..... RO

7 BIST Supported ..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved ..... always reads 0

3-0 Response Code ..... 0 = test completed successfully

VT82C585VPX-Specific Configuration Registers

Cache Control

Offset 50- Cache Control 1 .....RW

7-6 Cache Enable
- 00 Cache disable .....default
- 01 Cache Init - always does L2 fill
- 10 Cache enable (normal operation)
- 11 -reserved- (do not program)

5 Linear Burst Enable
- 0 Disable .....default
- 1 Enable

4-3 Tag Configuration
- 00 8+0 - 8 Tag bits, no alt (dirty) bit.....default
- 01 7+1 - 7 Tag bits + alternate (dirty) bit
- 10 10 - 10 Tag bits, no alt (dirty) bit
- 11 9+1 - 9 Tag bits + alternate (dirty) bit

2 SDRAM Interface Select

Selects the function of pins 90-93 and 73-76:
- 0 CWE[0-7]#.....default
- 1 GWE#, BWE#, SCASx#, SRASx#, SWEx#

1-0 SRAM Type
- 00 No SRAM.....default
- 01 Reserved
- 10 Burst SRAM
- 11 Pipeline Burst SRAM

Offset 51 - Cache Control 2 ..... RW

7-6 Reserved .....RW, default=0

5 Backoff CPU

Used when register 52h bit-2 is set for "L2 fill when CACHE# is inactive". This bit should normally be set to 0 for best performance, but performance differences are typically not significantly noticable at a system level.
- 0 Defer ready return until L2 is filled ..... default
- 1 Backoff CPU until L2 is filled

4 Reserved .....RW, default=0

3 SRAM Banks
- 0 1 Bank..... default
- 1 2 Banks

2 Reserved .....RW, default=0

1-0 Cache Size
- 00 256K ..... default
- 01 512K
- 10 1M
- 11 2M

Offset 52 - Non-Cacheable Control.....RW

7 **C0000-C7FFF Cacheable & Write-Protect** ... def=0
6 **D0000-DFFFF Cacheable & Write-Protect**... def=0
5 **E0000-EFFFF Cacheable & Write-Protect** ... def=0
4 **F0000-FFFFF Cacheable & Write-Protect**.... def=0
3 **Reserved (no function)**.....RW, default=0
2 **L2 Fill**
0 Normal L2 cache fill.....default
1 Force the requested data to be filled into the L2 cache (provided that L2 cache is enabled), even if the CPU does a read cycle with CACHE# de-asserted. Setting this bit significantly improves performance.
1 **Reserved (no function)**.....RW, default=0
0 **L2 Write Thru/Write-Back**
0 Write-Back .....default
1 Write-Thru

Offset 53 - System Performance Control.....RW

7 **Read Around Write**
0 Disable .....default
1 Enable
6 **Cache Read Pipeline Cycle**
0 Disable .....default
1 Enable
5 **Cache Write Pipeline Cycle**
0 Disable .....default
1 Enable
4 **DRAM Pipeline Cycle**
0 Disable .....default
1 Enable
3 **PCI Master Peer Concurrency**
0 Disable .....default
1 Enable
2-0 **Reserved** .....RW, default=0

Offset 54 - Non-Cacheable Region #1 High Byte ..... RW

15-8 **Base Address MSBs** - A<28:21> .....default=0
As noted below, the base address must be a multiple of the region size.

Offset 55 - Non-Cacheable Region #1 Low Byte ..... RW

7-3 **Base Address LSBs** - A<20:16> .....default=0
As noted below, the base address must be a multiple of the region size.
2-0 **Range (Region Size)**
000 Disable..... default
001 64K
010 128K (Base Address A16 must be 0)
011 256K (Base Address A16-17 must be 0)
100 512K (Base Address A16-18 must be 0)
101 1M (Base Address A16-19 must be 0)
110 2M (Base Address A16-20 must be 0)
111 4M (Base Address A16-21 must be 0)

Offset 56 - Non-Cacheable Region #2 High Byte ..... RW

15-8 **Base Address MSBs** - A<28:21> .....default=0
As noted below, the base address must be a multiple of the region size.

Offset 57 - Non-Cacheable Region #2 Low Byte ..... RW

7-3 **Base Address LSBs** - A<20:16> .....default=0
As noted below, the base address must be a multiple of the region size.
2-0 **Range (Region Size)**
000 Disable..... default
001 64K
010 128K (Base Address A16 must be 0)
011 256K (Base Address A16-17 must be 0)
100 512K (Base Address A16-18 must be 0)
101 1M (Base Address A16-19 must be 0)
110 2M (Base Address A16-20 must be 0)
111 4M (Base Address A16-21 must be 0)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies 82C580 BIOS porting guide for details).

Table 5. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Offset 58 - DRAM Configuration 1 .....RW

7-5 Bank 0/1 MA Map Type (EDO/FPG)
- 000 8-bit Column Address
- 001 9-bit Column Address
- 010 10-bit Column Address .....default
- 011 11-bit Column Address
- 100 12-bit Column Address
- 101 Reserved
- 11x Reserved

Bank 0/1 MA Map Type (SDRAM)
- 0xx 16Mbit SDRAM.....default
- 1xx 64Mbit SDRAM

4 Reserved .....RW, default=0

3-1 Bank 2/3 MA Map Type (EDO/FPG)
- 000 8-bit Column Address .....default
- 001 9-bit Column Address
- 010 10-bit Column Address
- 011 11-bit Column Address
- 100 12-bit Column Address
- 101 Reserved
- 11x Reserved

Bank 2/3 MA Map Type (SDRAM)
- 0xx 16Mbit SDRAM.....default
- 1xx 64Mbit SDRAM

0 Reserved .....RW, default=0

Offset 59 - DRAM Configuration 2..... RW

7-5 Bank 4/5 MA Map Type (EDO/FPG)
- 000 8-bit Column Address..... default
- 001 9-bit Column Address
- 010 10-bit Column Address
- 011 11-bit Column Address
- 100 12-bit Column Address
- 101 Reserved
- 11x Reserved

Bank 4/5 MA Map Type (SDRAM)
- 0xx 16Mbit SDRAM ..... default
- 1xx 64Mbit SDRAM

4-3 Reserved .....RW, default=0

2-0 Last Bank DRAM Populated
- 000 Bank 0
- 001 Bank 1
- 010 Bank 2
- 011 Bank 3
- 100 Bank 4
- 101 Bank 5..... default
- 11x Reserved

Offset 5A-5F - DRAM Row Ending Address:

All of the registers in this group default to 01h:

Offset 5A - Bank 0 Ending (HA[29:22]) ..... RW

Offset 5B - Bank 1 Ending (HA[29:22])..... RW

Offset 5C - Bank 2 Ending (HA[29:22]) ..... RW

Offset 5D - Bank 3 Ending (HA[29:22]) ..... RW

Offset 5E - Bank 4 Ending (HA[29:22])..... RW

Offset 5F - Bank 5 Ending (HA[29:22])..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Offset 60 - DRAM Type ..... RW

7-6 Reserved .....always reads 0

5-4 DRAM Type for Bank 4/5
- 00 Fast Page Mode DRAM (FPG)..... default
- 01 EDO DRAM (EDO)
- 10 Reserved
- 11 Synchronous DRAM (SDRAM)

3-2 DRAM Type for Bank 2/3.....default=FPG

1-0 DRAM Type for Bank 0/1.....default=FPG

Offset 61 - Shadow RAM Control 1.....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Offset 62 - Shadow RAM Control 2.....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Offset 63 - Shadow RAM Control 3 ..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1 SMI Redirect to A0000h-BFFFFh
- 0 Disable Redirection ..... default
- 1 Enable Redirection

0 DRAM A0000h-BFFFFh Access
- 0 Disable read write to A0000-B0000 ..... default
- 1 Enable read write to A0000-B0000 in DRAM

Note: A0000-BFFFF is reserved for use by VGA controllers for system access to the VGA frame buffer. Setting this bit directs accesses to Axxxx-Bxxxx to corresponding memory addresses in system DRAM instead of directing those accesses to the PCI bus for VGA frame buffer access.

Offset 64 - DRAM Reference Timing (FPG Only) .....RW

Defines basic timing for Fast Page (FPG) DRAMs. Timing for banks populated with EDO / SDRAM is defined per Rx65-66.

7-6 RAS Precharge Time
- 00 2T
- 01 3T
- 10 4T .....default
- 11 6T

5-4 RAS Pulse Width
- 00 3T
- 01 4T
- 10 5T .....default
- 11 6T

3-2 CAS Read Pulse Width
- 00 1T
- 01 2T (FPG), 1T (EDO)
- 10 3T (FPG), 2T (EDO).....default
- 11 4T (FPG), 3T (EDO)

1 CAS Write Pulse Width
- 0 1T
- 1 2T .....default

0 Column Address to CAS Delay (see also Rx67[7])
- 0 1T
- 1 2T .....default

Offset 65 - DRAM Timing Control 1 (EDO/SDRAM) ...RW

7-6 Page Mode Control
- 00 Page closes after access.....default
- 01 Reserved
- 10 Page stays open after access
- 11 Page closes if CPU is idle

5 Fast DRAM Decoding Enable
- 0 End of Second T2.....default
- 1 End of First T2 (recommended setting)

Determines the latch point for all DRAM-related decoding (bank, page-hit, MA address mux setup, etc). DRAM control signals (RAS#, CAS#, or SDRAM commands) are also activated at this point.

4 EDO DRAM Leadoff Cycle Reduction
- 0 Normal leadoff cycle (recommended)....default
- 1 Reduce leadoff cycle by 1T

3 DRAM Data Latch Delay.(recommended setting=0)
- 0 Latch DRAM data 1 cycle before CPU..... def
- 1 Latch DRAM Data ½ cycle before the CPU

2 Pin 88 Function Select
- 0 DB32 .....default
- 1 TA9

1 Reserved .....RW, default=0

0 Relaxed DRAM Read Cycle Latency ..... default=0

Used to relax the timing when Rx53[7] (read-around-write) and Rx65[5] (fast decoding) are both enabled.
- 0 No effect (DRAM decoding time is end of T2)
- 1 Add 1 cycle delay (DRAM decoding time is the end of the second T2) if the write-buffer is not empty (recommended setting).

Offset 66 - DRAM Timing Control 2 (EDO/SDRAM)... RW

7 EDO Test Mode Enable
- 0 Normal Mode..... default
- 1 EDO Test Mode

6 Reserved .....always reads 0

5 SDRAM CAS Latency.....default=0

The definition of this bit is the same as Rx6C bit-3 for backwards compatibility with Apollo VP (VT82C585VP). The two bits are OR'd: if either bit is set to one, a latency of 3 is selected; if both bits are 0 a latency of 2 is selected.

4 Reserved .....always reads 0

3 Turbo EDO Mode Enable (recommended setting=0)
- 0 -2-2-2 Two-Cycle Burst..... def
- 1 -1-1-1 One-Cycle Burst (only applicable to turbo EDO DRAMs)

2 MD to HD FIFO Control. (recommended setting=0)
- 0 -1-1-1 to pop the data from the DRAM-to-CPU FIFO to the CPU..... default
- 1 -2-2-2 to pop data from the FIFO to the CPU

1 SDRAM RAS-Precharge Reduction ..... (recommended setting=0)
- 0 Use Rx64[7-6] for RAS-Precharge time..... def
- 1 Reduce the above by 1T for SDRAM access

0 SDRAM RAS-to-CAS Delay Reduction .... (recommended setting=1)
- 0 Use Rx64[0] for Column Address to CAS delay for SDRAM) ..... default
- 1 Column Address to CAS delay is fixed at 1T for SDRAM

Offset 67 - 32-Bit DRAM Width..... RW

7 RAS to Column Address Delay

This bit determines the number of CPU clocks from RAS assertion to column address assertion.
- 0 1T (recommended setting)..... default
- 1 2T (only set this with heavily loaded DRAM)

6 NA# Delay
- 0 No NA# delay, 3-1-1-1-2-1-1-1 for L2 cache read hit (recommended setting) ..... default
- 1 Delay NA# 1T, 3-1-1-1-3-1-1-1

This bit only applies when 2 banks of PBSRAM is installed.

5 Bank 5 Width. 1=32-bit, 0= 64 bit.....default=64

4 Bank 4 Width. 1=32-bit, 0= 64 bit .....default=64

3 Bank 3 Width. 1=32-bit, 0= 64 bit .....default=64

2 Bank 2 Width. 1=32-bit, 0= 64 bit .....default=64

1 Bank 1 Width. 1=32-bit, 0 =64 bit .....default=64

0 Bank 0 Width. 1=32-bit, 0= 64 bit .....default=64

Offset 68 - Reserved (Do Not Program) .....RW

7-4 **Reserved** (do not program).....RW, default = 0

3 **Pin 126 Function Select**
- 0 Pin 126 remains high all the time (for backwards compatibility with VT82C585VP-based designs that drive the VT82C587VP "CMD5" input with pin 126).....default
- 1 Pin 126 is MA12 for 64Mb DRAM support

2-0 **Reserved** (do not program).....RW, default = 0

Offset 69 - Reserved (Do Not Program) .....RW

7-0 **Reserved** (do not program).....RW, default = 0

Offset 6A - Refresh Counter.....RW

7-0 **Refresh Counter** (in units of 16 CPUCLKs) .... def=0
note: When set to 00, DRAM refresh is disabled

Offset 6B - Refresh Control.....RW

7 **CBR (CAS-before-RAS) Refresh**
- 0 Disable CBR Refresh .....default
- 1 Enable CBR Refresh

6 **Burst Refresh (Burst 4 Times)**
- 0 Disable burst refresh.....default
- 1 Enable burst refresh

5-3 **Reserved** .....RW, default=0

2 **Extended Timing**
- 0 Normal Timing.....default
- 1 Force 2T from MA to RAS# and CAS# falling for all cases (use this setting for heavily loaded DRAM and direct drive)

1-0 **Reserved** .....always read 0

Offset 6C - SDRAM Control..... RW

7 **64Mbit SDRAM Interleave**
- 0 2-bank interleave for 64Mbit SDRAM .. default
- 1 4-bank interleave for 64Mbit SDRAM

Note: This bit is a don't-care for 16Mbit SDRAM

6 **SDRAM Burst Write**
- 0 Disabled..... default
- 1 Enabled

5 **SDRAM Bank Interleave Enable**
- 0 Disabled (bit-7 is a don't care) ..... default
- 1 Enabled
  16Mbit is 2-way only
  64Mbit is defined by bit-7 of this register

4 **Reserved** .....RW, default= 0

3 **SDRAM CAS Latency** (see also Rx66[5])
- 0 Cycle latency is 2 (RX66[5] must be 0). default
- 1 Cycle latency is 3

2-0 **SDRAM Operation Mode Select**
- 000 Normal SDRAM Mode..... default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable. CPU-to-DRAM cycles are converted to All-Banks-Precharge commands.
- 011 CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[11:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[11:0].
- 100 CBR Cycle Enable
- 101 Reserved
- 11x Reserved

Offset 6D - DRAM Control Drive Strength..... RW

7 **Bank Decoding Test**.....default=0

6 **MA[0:1] Drive**
- 0 12mA ..... default
- 1 24mA

5 **Duplicate Copy of MA[0:1]**

	Pin N17	Pin M17	Drive Control	
0	RAS5#	RAS4#	bit 0	default
1	MA1	MA0	bit 6	

4 **Force SMM Mode** .....default=0

3 **SDRAM Command Drive** (SRAS#, SCAS#, SWE#)
- 0 12mA ..... default
- 1 24mA

2 **MA[2:13] / WE# Drive**
- 0 12mA ..... default
- 1 24mA

1 **CAS# Drive**
- 0 8 mA ..... default
- 1 12 mA

0 **RAS# Drive**
- 0 12mA ..... default
- 1 24mA

PCI Bus Control

These registers are normally programmed once at system initialization time.

Offset 70 - PCI Buffer Control.....RW

7 CPU to PCI Post-Write
- 0 Disabled .....default
- 1 Enabled

6 PCI Master to DRAM Post-Write
- 0 Disabled .....default
- 1 Enabled

5 PCI Master to DRAM Prefetch
- 0 Disabled .....default
- 1 Enabled

4 Reserved .....RW, default= 0

3-2 Reserved ..... always reads 0

1 PCI Retry for CPU QW Access
- 0 Disabled .....default
- 1 Enabled

0 PCI Master Does Not Flush CPU to PCI Buffer
- 0 Master flushes CPU-to-PCI buffer .....default
- 1 Master does not flush CPU to PCI buffer

Offset 71 - CPU to PCI Flow Control 1.....RW

7 Dynamic Burst
- 0 Disabled .....default
- 1 Enabled (see note under bit-3 below)

6 Byte Merge
- 0 Disabled .....default
- 1 Enabled

5 Reserved ..... always reads 0

4 PCI I/O Cycle Post Write
- 0 Disabled .....default
- 1 Enabled

3 PCI Burst
- 0 Disabled .....default
- 1 Enabled (bit7=1 will override this option)

bit-7	bit-3	Operation
0	0	Every write goes into the write buffer and no PCI burst operations occur.
0	1	If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
1	x	Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.

2 Enable PCI Fast Back-to-Back Write .. def=0 (disa)

1 Enable Quick Frame Generation... def=0 (disabled)

0 Enable 1 Wait State PCI Cycles .... def=0 (disabled)

Offset 72 - CPU to PCI Flow Control 2 ..... RWC

7 Retry Status over 16 / 64 Times
- 0 No retry occurred..... default
- 1 Retry occurred ..... write 1 to clear

6 Retry Timeout Action
- 0 Retry Forever (record status only) ..... default
- 1 Flush buffer or return FFFFFFFF for read

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times, back off CPU ..... default
- 01 Retry 16 times
- 10 Retry 4 times, back off CPU
- 11 Retry 64 times

3 Clear Failed Data and Continue Retry
- 0 Disabled..... default
- 1 When data is posting and retry fails, pop the failed data if any, and keep posting

2 CPU Backoff on PCI Read Retry Failure
- 0 Disabled..... default
- 1 Backoff CPU when reading data from PCI and retry fails

1 Reduce 1T for FRAME# Generation
- 0 Disabled..... default
- 1 Enabled

0 Reduce 1T for CPU Read PCI Slave
- 0 Disabled..... default
- 1 Enabled (bypass TRDY# to LRDY#)

Offset 73 - PCI Master Control 1.....RW

7 Local Memory Decoding
- 0 Fast (address phase) .....default
- 1 Slow (first data phase)

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response .....default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response .....default
- 1 One wait state TRDY# response

4 Reserved ..... always reads 0

3 Assert STOP# after PCI Master Write Timeout
- 0 Disabled .....default
- 1 Enabled

2 Assert STOP# after PCI Master Read Timeout
- 0 Disabled .....default
- 1 Enabled

1 LOCK# Function
- 0 Disabled .....default
- 1 Enabled

0 PCI Master Broken Timer Enable
- 0 Disabled .....default
- 1 Enabled. Force into arbitration when there is no FRAME# 16 PCICLK's after the GRANT.

Offset 74 - PCI Master Control 2.....RW

7 PCI Enhance Command Support
- 0 Disabled .....default
- 1 Enabled

6 PCI Master Single Write Merge
- 0 Disabled .....default
- 1 Enabled

5-0 Reserved ..... always reads 0

Offset 75 - PCI Arbitration 1..... RW

7 Arbitration Mechanism
- 0 PCI has priority..... default
- 1 Fair arbitration between PCI and CPU

6 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) .. default
- 1 Frame-based (arbitrate at end of each FRAME#)

5-4 Reserved .....RW, default=0

3-0 PCI Master Bus Time-Out
(force into arbitration after a period of time)
- 0000 Disable..... default
- 0001 1x32 PCICLKs
- 0010 2x32 PCICLKs
- ... ...
- 1111 15x32 PCICLKs

Offset 76 - PCI Arbitration 2..... RW

7 Master Priority Rotation Enable
- 0 Disable (arbitration per Rx75 bit-7)..... default
- 1 Enable (arbitration per bits 5-4 of this register) (gives the CPU higher priority than either of the mechanisms defined by Rx75 bit-7)

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disabled (arbitration per Rx75 bit-7)..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-1 Reserved .....always reads 0

0 Reserved .....RW, default=0

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storage temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	Volts
Output voltage (V_{DD} = 3.1 - 3.6V)	-0.5	V_{DD} + 0.5	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA-0-70^{o}C, V_{DD}=5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
I_{CC}	Power supply current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 6. AC Timing Min / Max Conditions

	Min	Max
VDD-CPU, VDD-PCI, VDD-DRAM	5.25	3.135
VDD	5.25	4.75
Temperature	0	70

Pad load derating curve specifications are listed from 0pf to 80pf with 5pf resolution; above 80 pf use 20 pf resolution up to 200 pf. The following pads are provided:

Table 7. PAD Load Derating Curve (I/V curve)

External pad name	Voltage	Remark
vpad000	3.3	
vpad 001	3.3	
vpad 002	3.3	
vpad 005	3.3	24mA
vpad 007	3.3	12mA
vpad 009	3.3	12mA
vpad 011	3.3	8mA
vpad 012	3.3	
vpad 013	3.3	
vpad 014	3.3	

Table 8. AC Characteristics - CPU Cycle Timing

Parameter	Min	Max	Pad	Notes
ADS# Setup Time to CCLK Rising	5			
WR# Setup Time to CCLK Rising	5			
MIO# Setup Time to CCLK Rising	5			
DC# Setup Time to CCLK Rising	5			
BE[7:9[# Setup Time to CCLK Rising	5			
HITM# Setup Time to CCLK Rising	5			
CACHE# Setup Time to CCLK Rising	5			
HA[31:3] Setup Time to CCLK Rising	5			
ADS#,HITM#,WR#,MIO#,DC#,BE[7:0]#,CACHE# Hold Time from CCLK Rising	2			
HA[31:3] Hold Time from CCLK Rising	2			
BRDY# Valid Delay From CCLK Rising	3	8	vpad000	0 pf
NA# Valid Delay From CCLK Rising	3	7	vpad000	0 pf
AHOLD Valid Delay From CCLK Rising	3	7	vpad000	0 pf
BOFF# Valid Delay From CCLK Rising	3	7	vpad000	0 pf
EADS# Valid Delay From CCLK Rising	3	7	vpad000	0 pf
KEN#/INV# Valid Delay from CCLK Rising	3	7	vpad000	0 pf
BE[7:0]# Valid Delay from CCLK Rising	4	9	vpad002	0 pf
HA[31:3] Valid Delay from CCLK Rising	4	13	vpad002	0 pf
HA[31:3] Float Delay from CCLK Rising	4	9		0 pf

Table 9. AC Characteristics - L2 Cache Timing

Parameter	Min	Max	Pad	Notes
COE# Valid Delay from CCLK Rising	2	6	vpad000	0 pf
TA[9:0] Valid Delay from CCLK Rising	3	9	vpad001	0 pf
TA[9:0] setup time to CCLK Rising	8			
TA[9:0] Hold Time from CCLK Rising	1			
TAGWE# Valid Delay from CCLK Rising	2	6	vpad000	0 pf
CWE[7:0]#/GWE#/BWE# Active Delay from CCLK Rising	2	6	vpad000	0 pf
CCS#(CALE) Valid Delay from CCLK Rising	2	6	vpad000	0 pf
CADS# Valid Delay from CCLK Rising	2	6	vpad000	0 pf
CADV# Valid Delay from CCLK Rising	2	6	vpad000	0 pf

Table 10. AC Characteristics - DRAM Interface Timing

Parameter	Min	Max	Pad	Notes
RAS[5:0] Valid Delay from CCLK Rising	4	9	vpad005	0 pf
CAS[7:0]# Valid Delay from CCLK Rising (EDO)	3	8	vpad007	0 pf
DQM[7:0]# Valid Delay from CCLK Rising (SDRAM)	3	7	vpad011	
SRAS# Valid Delay from CCLK Rising	3	7	vpad005	
SCAS# Valid Delay from CCLK Rising	3	7	vpad005	
SWE#,SWEB# Valid Delay from CCLK Rising	3	7	vpad005	
MA[11:2]# Valid Delay from CCLK Rising on first Clock after RAS# asserts	4	9	vpad005	startpage 0 pf
MA[1:0] Valid Delay from CCLK Rising (burst)	4	10	vpad005	0 pf
MA[11:0] Flow Through Delay from HA for first read cycle	4	10	vpad005	Leadoff, 0pf
MWE# Valid Delay from CCLK Rising	6	15	vpad005	0 pf

Table 11. AC Characteristics - PCI Cycle Timing

Parameter	Min	Max	Pad	Notes
AD[31:0] Valid Delay from PCLK Rising (address phase)	5	12	vpad012	0 pf
AD[31:0] Valid Delay from PCLK Rising (data phase)	5	11		
AD[31:0] Setup Time to PCLK	7			
AD[31:0] Hold Time	2			
CBE[3:0]#,FRAME#,TRDY#,IRDY#,STOP#,DEVSEL# Valid Delay from PCLK Rising	3	8	vpad013	0 pf
CBE[3:0]#,FRAME#,TRDY#,IRDY#,STOP#,DEVSEL# Float Delay from CCLK Rising		10		
CBE[3:0]#,FRAME#,TRDY#,IRDY#,STOP#,DEVSEL# Setup Time to CCLK Rising	7			
CBE[3:0]#,FRAME#,TRDY#,IRDY#,STOP#,DEVSEL# Hold Time from CCLK Rising	2			
PHLD#,REQ[3:0]# Setup Time to PCLK Rising	7			
GNT[3:0]#,PGNT# Valid Delay from PCLK Rising	2	6		

Table 12. AC Characteristics - Data Timing

Parameter	Min	Max	Fig.	Notes
HD Valid Delay from CCLK Rising	3	7	vpad001	0 pf
HD Setup Time to CCLK Rising	2			
HD Hold Time from CCLK Rising	2			
MD Valid Delay from CCLK Rising (SDRAM)	3	8	vpad001	0 pf
MD Valid Delay from CCLK Falling (EDO/FP)	4	14		
MD Setup Time to CCLK Rising (SDRAM)	2			
MD Setup Time to CCLK Falling (EDO)	2			
MD Hold Time from CCLK Rising (SDRAM)	3			
MD Hold Time from CCLK Falling (EDO)	3			

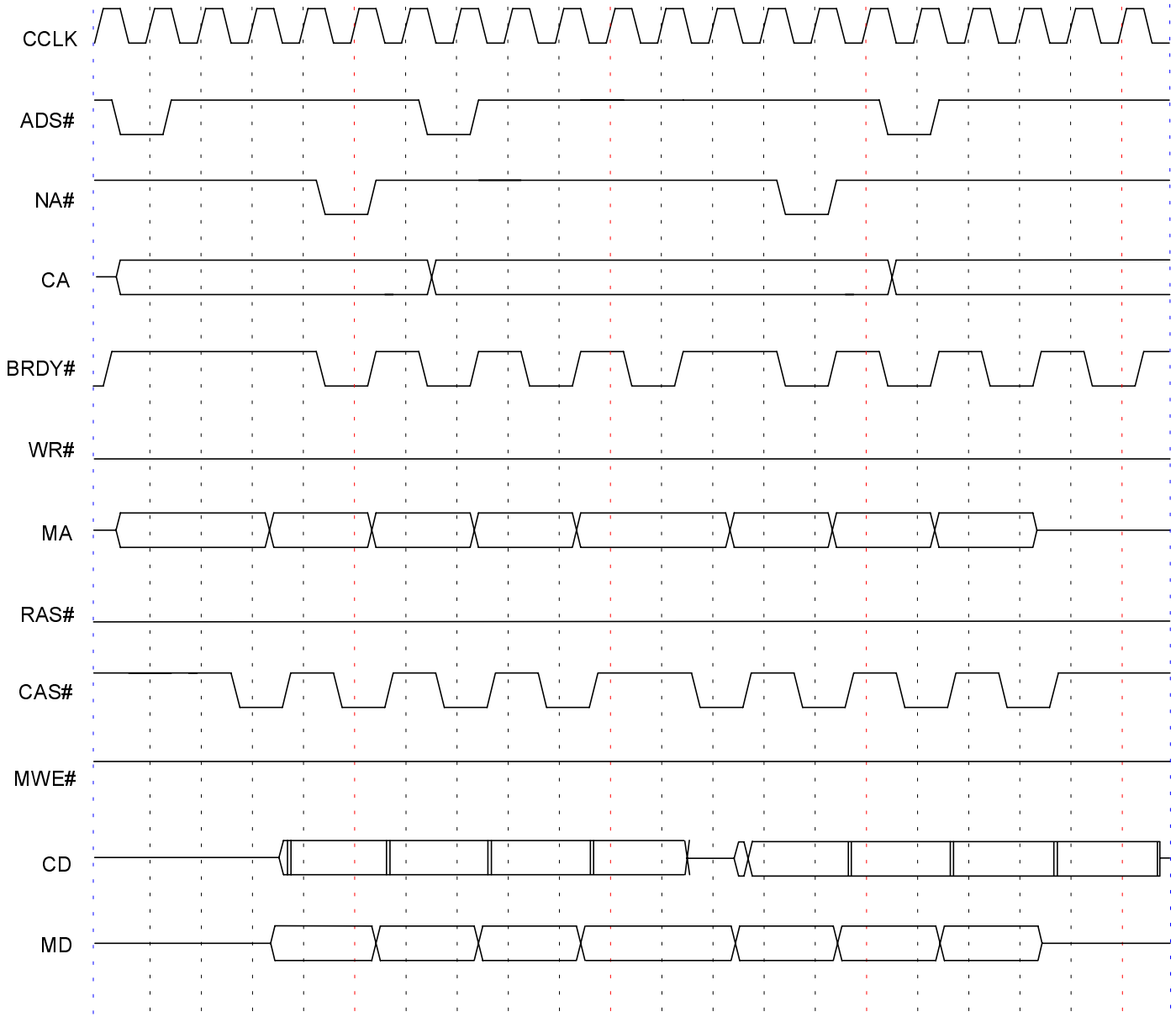

Figure 6. DRAM READ PIPE LINE EDO 5-2-2-2, 3-2-2-2

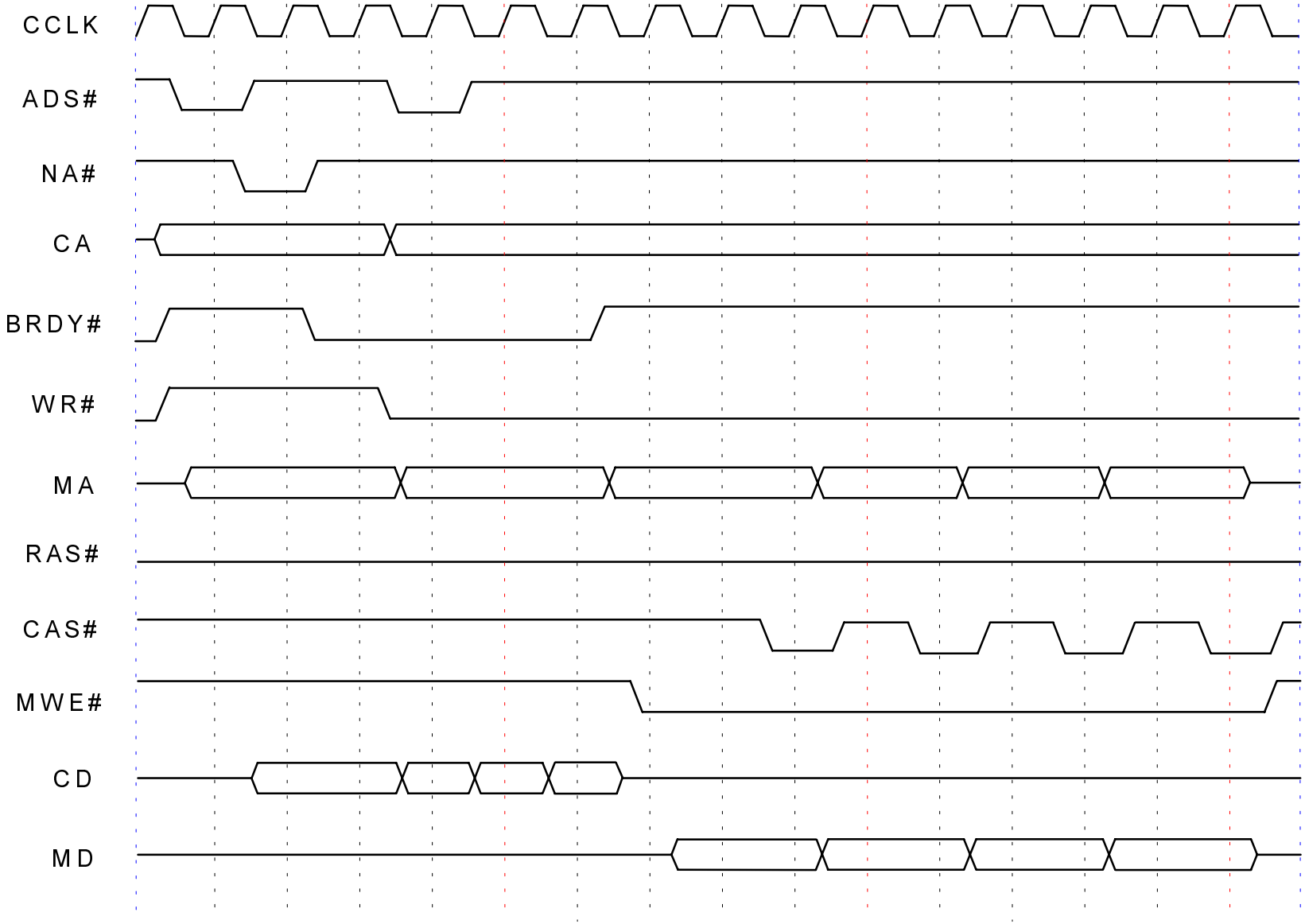

Figure 7. POST WRITE 3111,DRAM EDO 2222

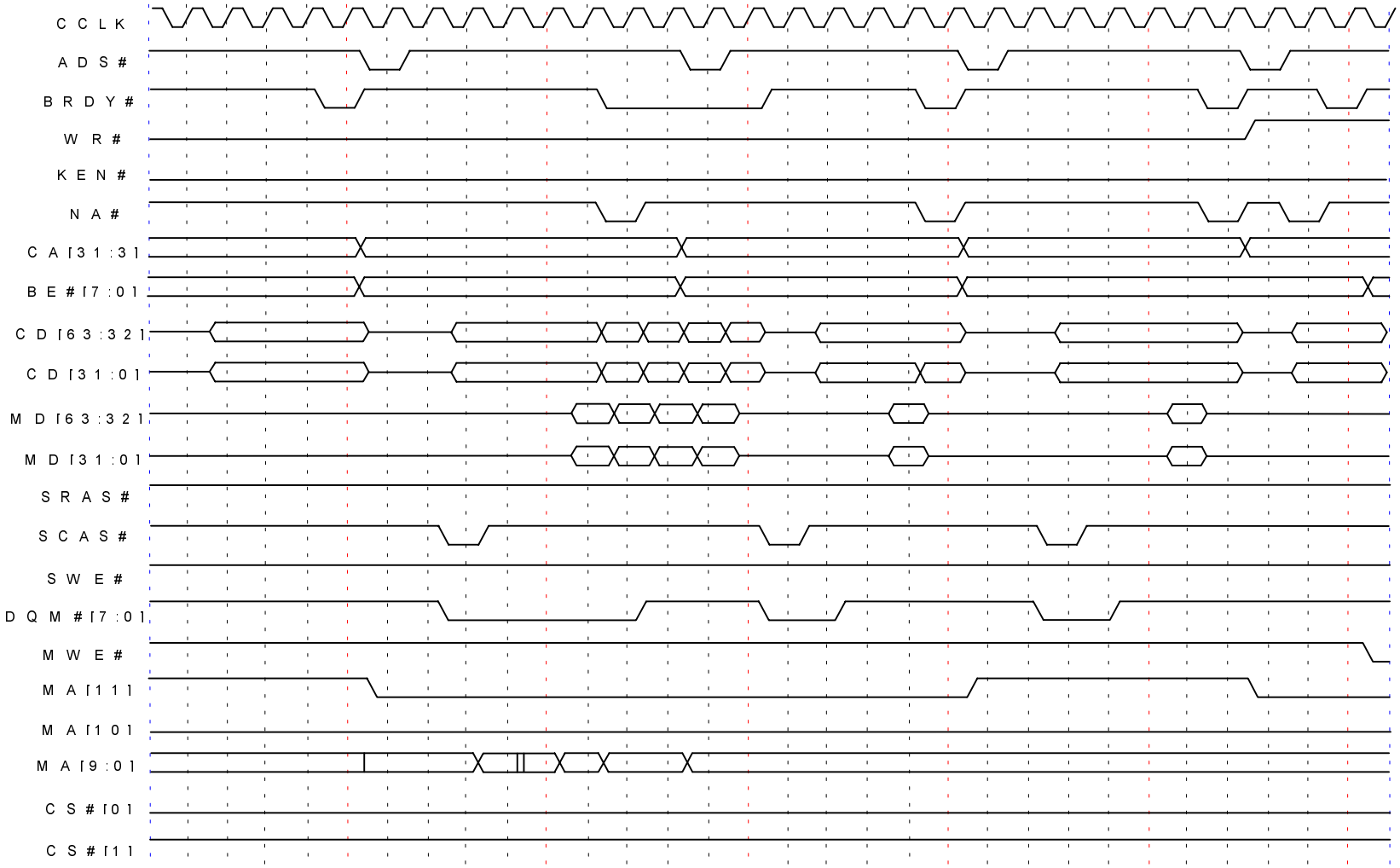

Figure 8. SDRAM READ CYCLE (BANK INTERLEAVE, CAS LATENCY=3)

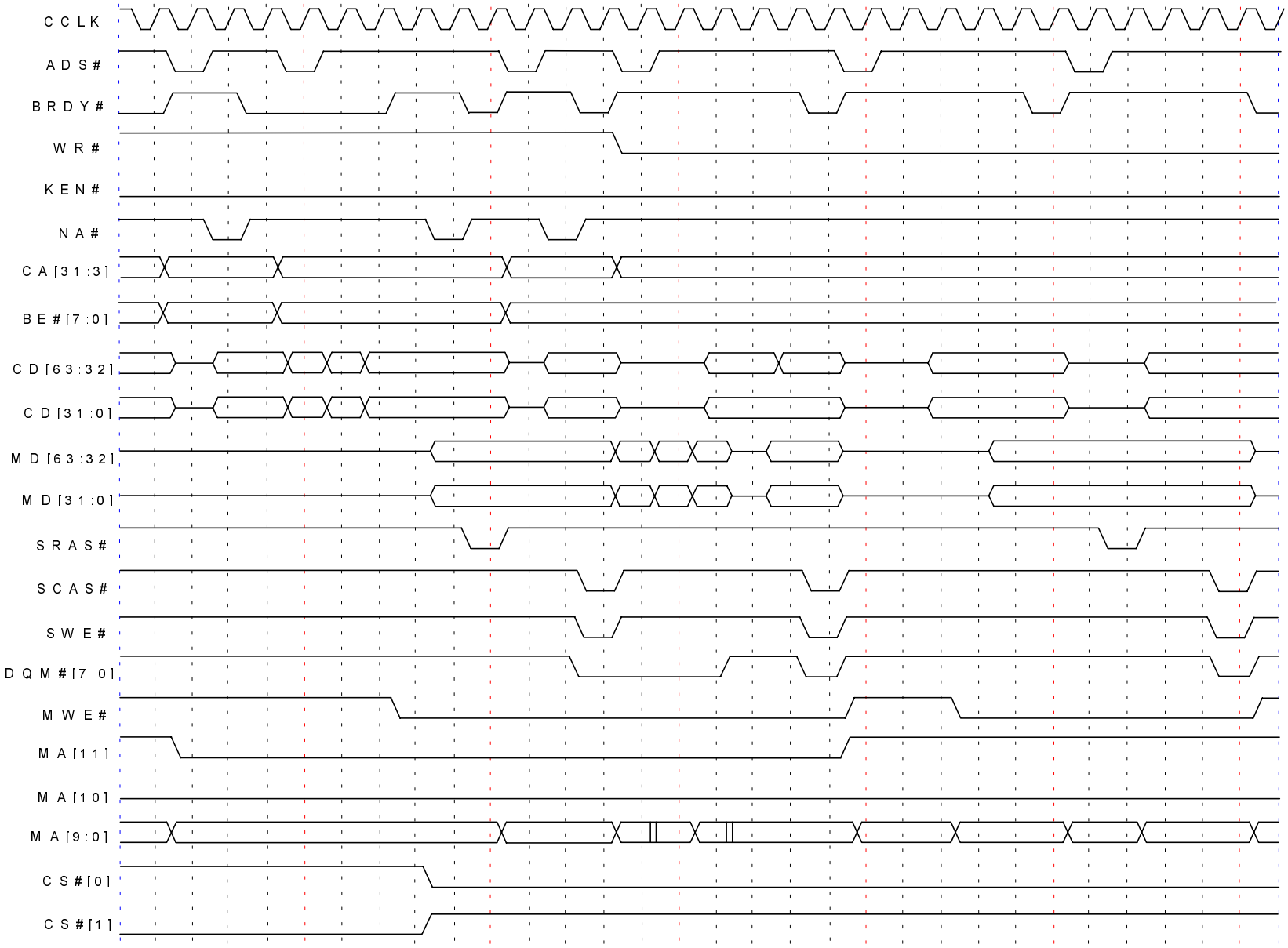

Figure 9. SDRAM WRITE CYCLE (BANK INTERLEAVE)

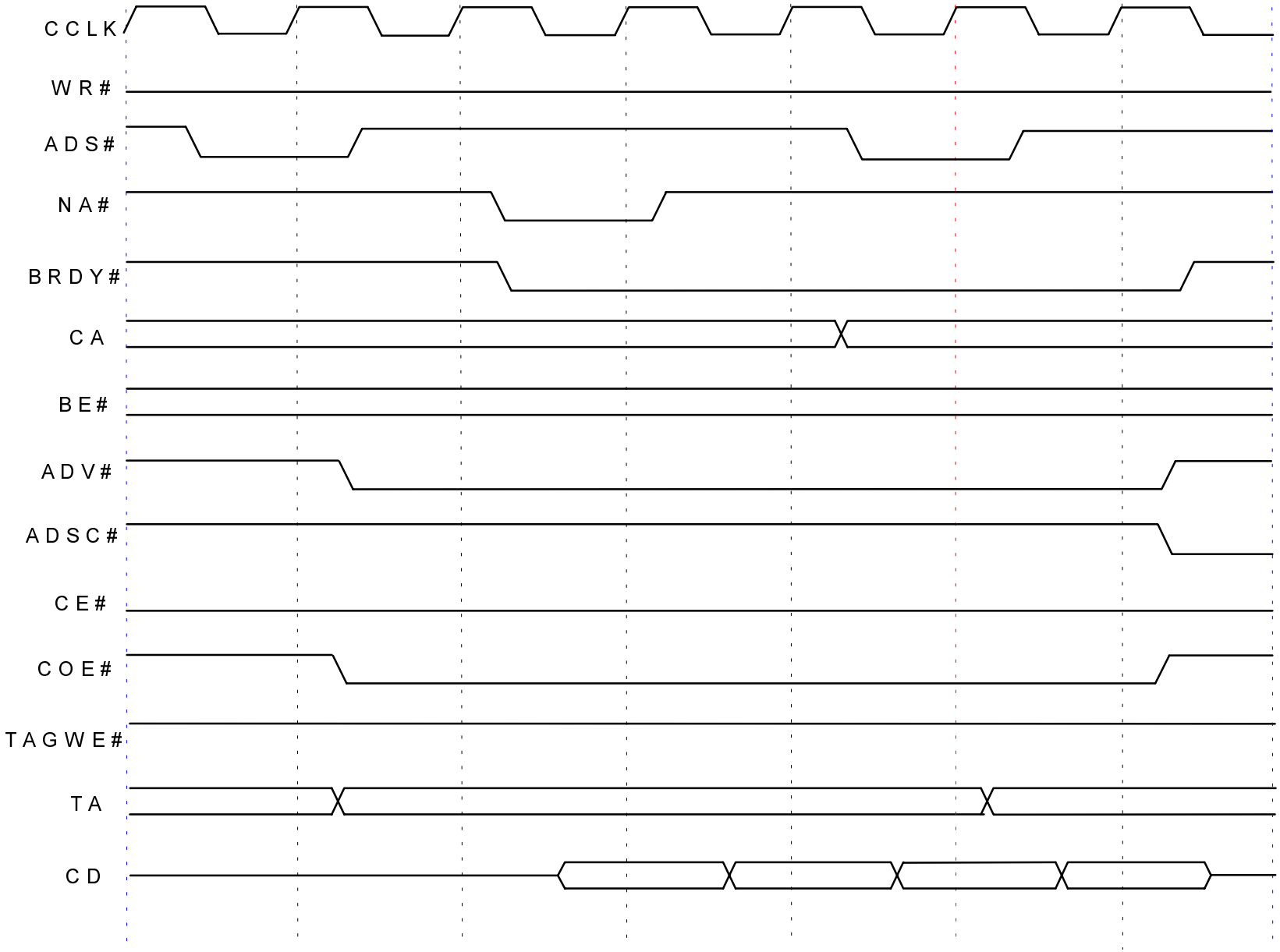

Figure 10. CPU READ HIT SYNCHRONOUS SRAM 3111

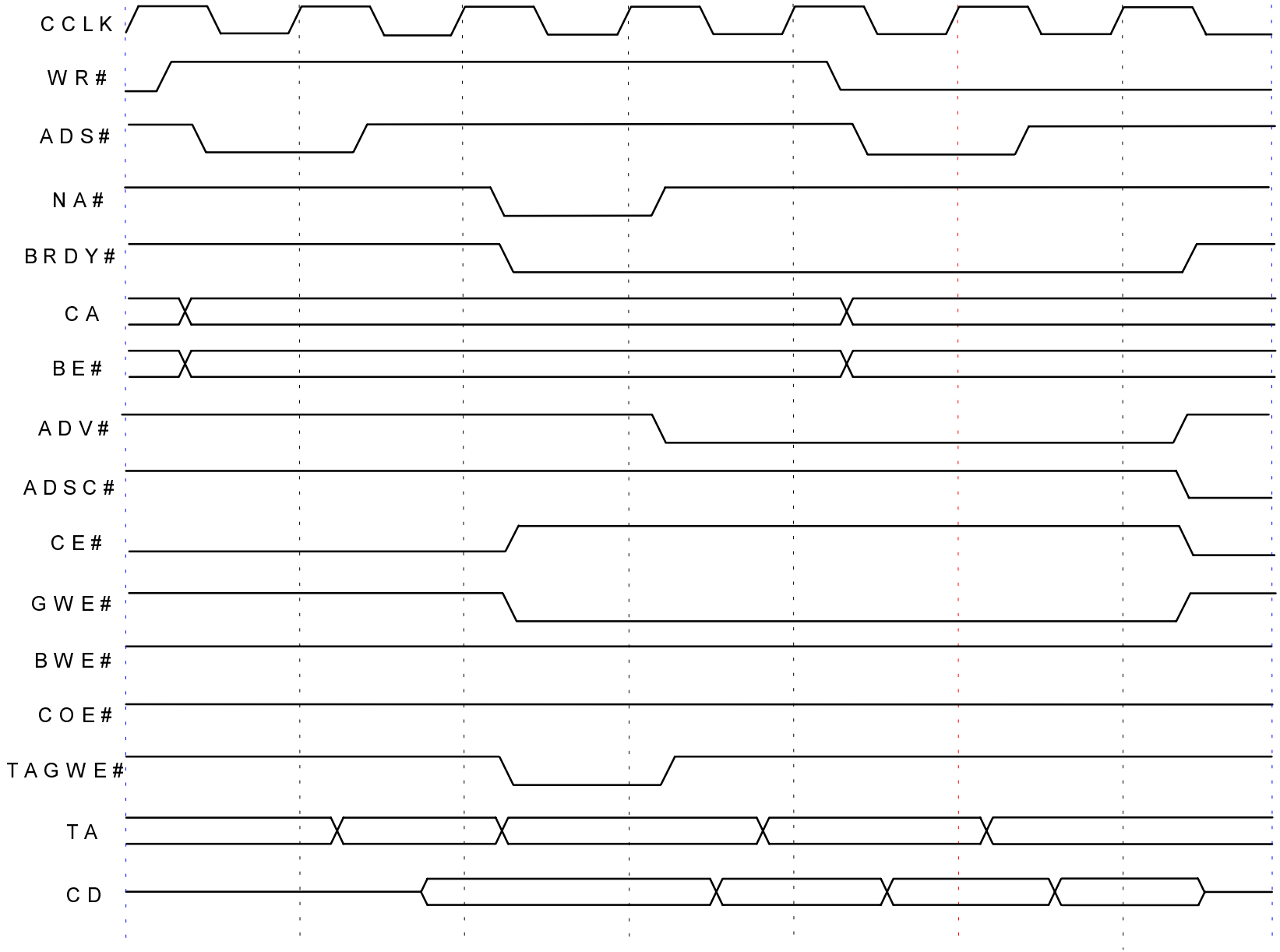

Figure 11. CPU WRITE HIT SYNCHRONOUS SRAM 3111

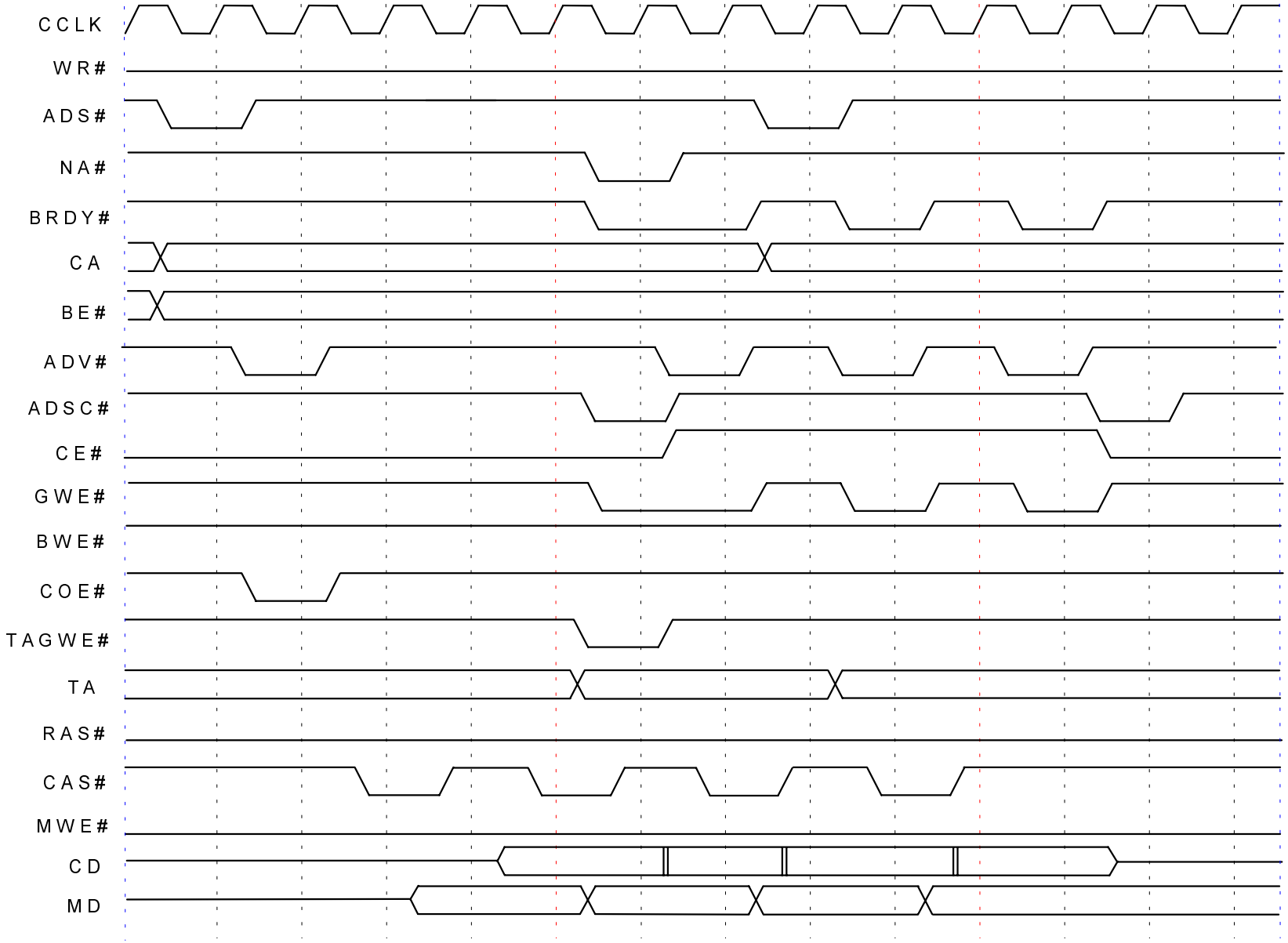

Figure 12. CPU READ MISS FILL SYNCHRONOUS SRAM

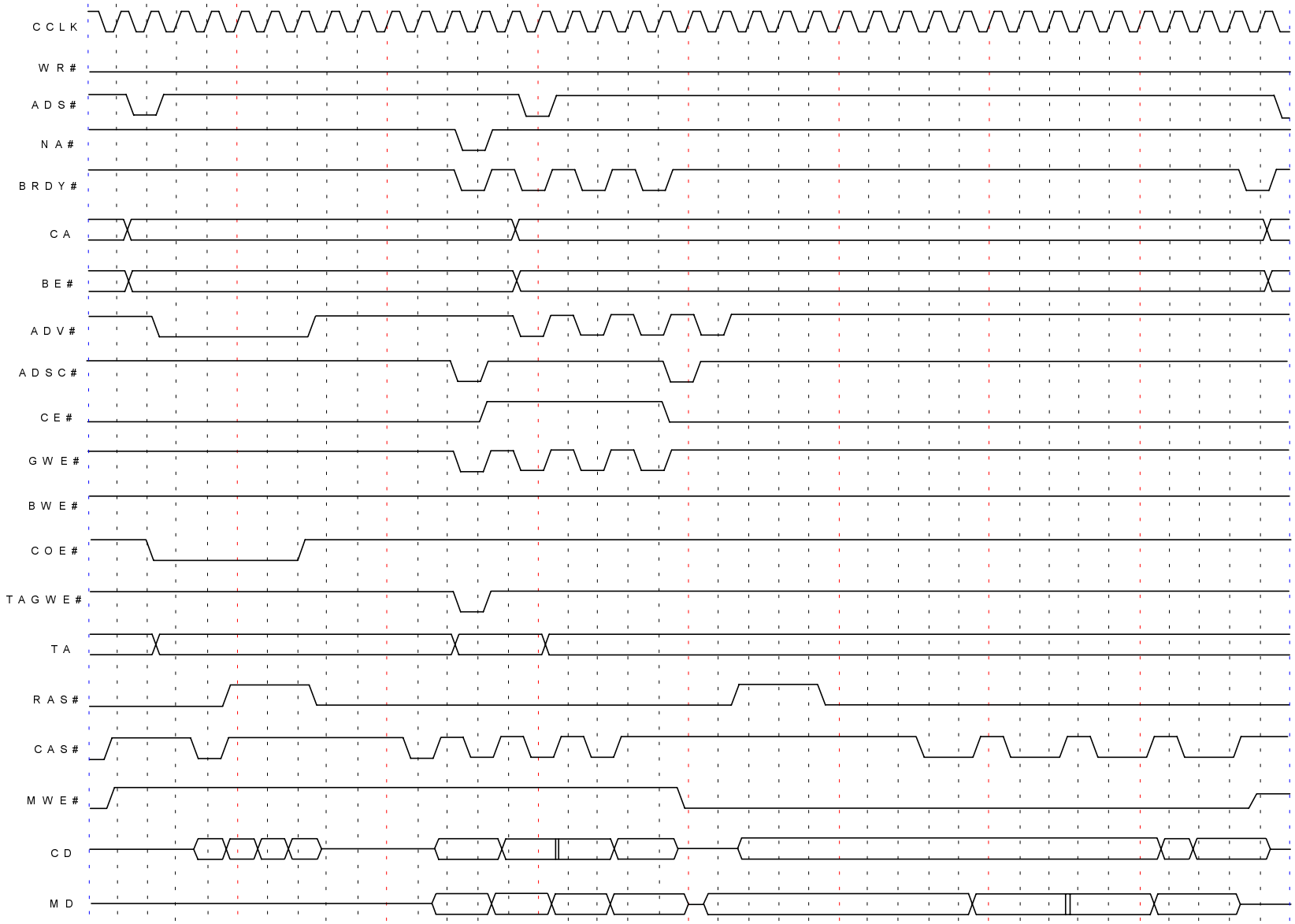

Figure 13. CPU READ MISS DIRTY L2 WRITE BACK FILL

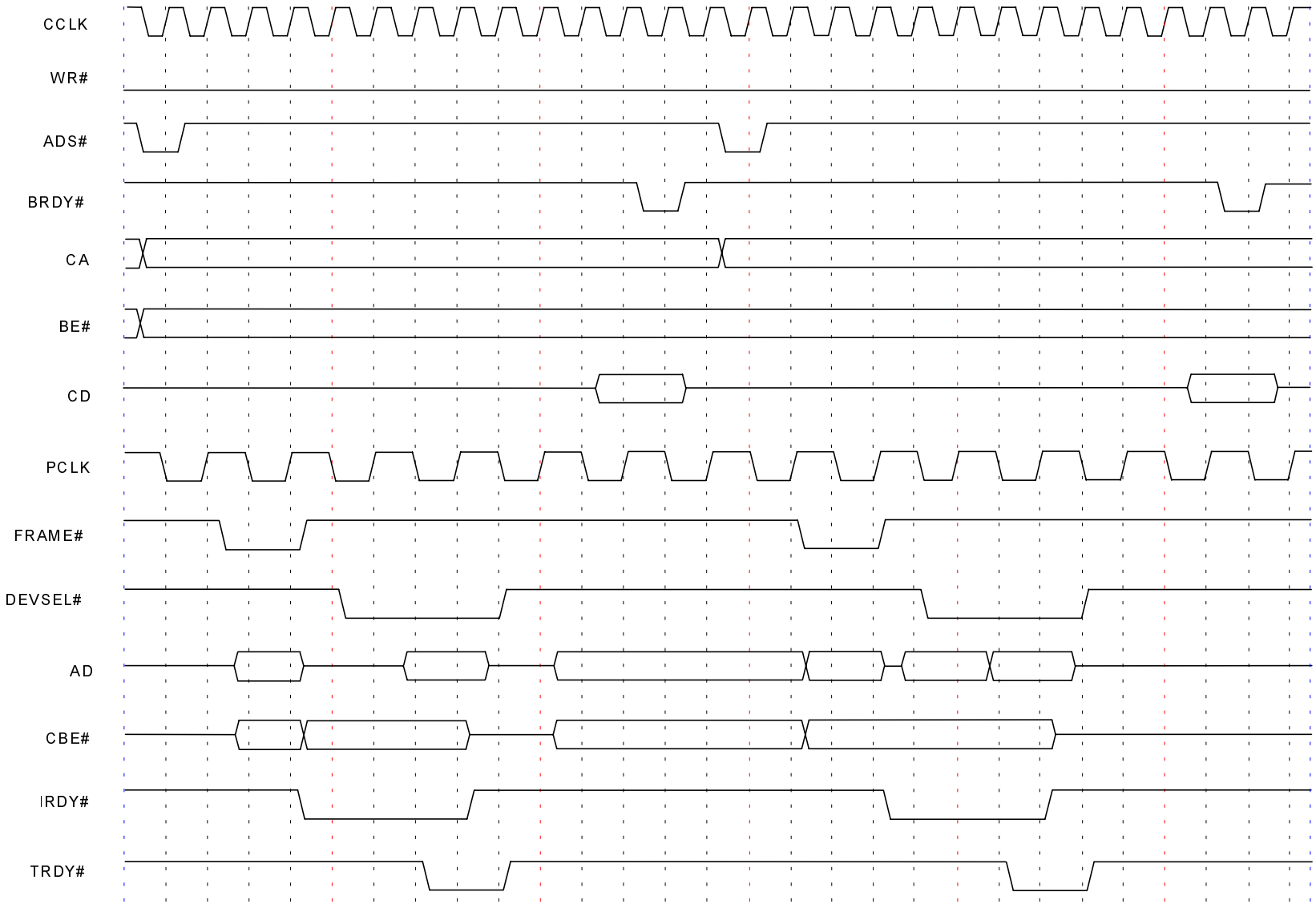

Figure 14. CPU READ PCI SLAVE

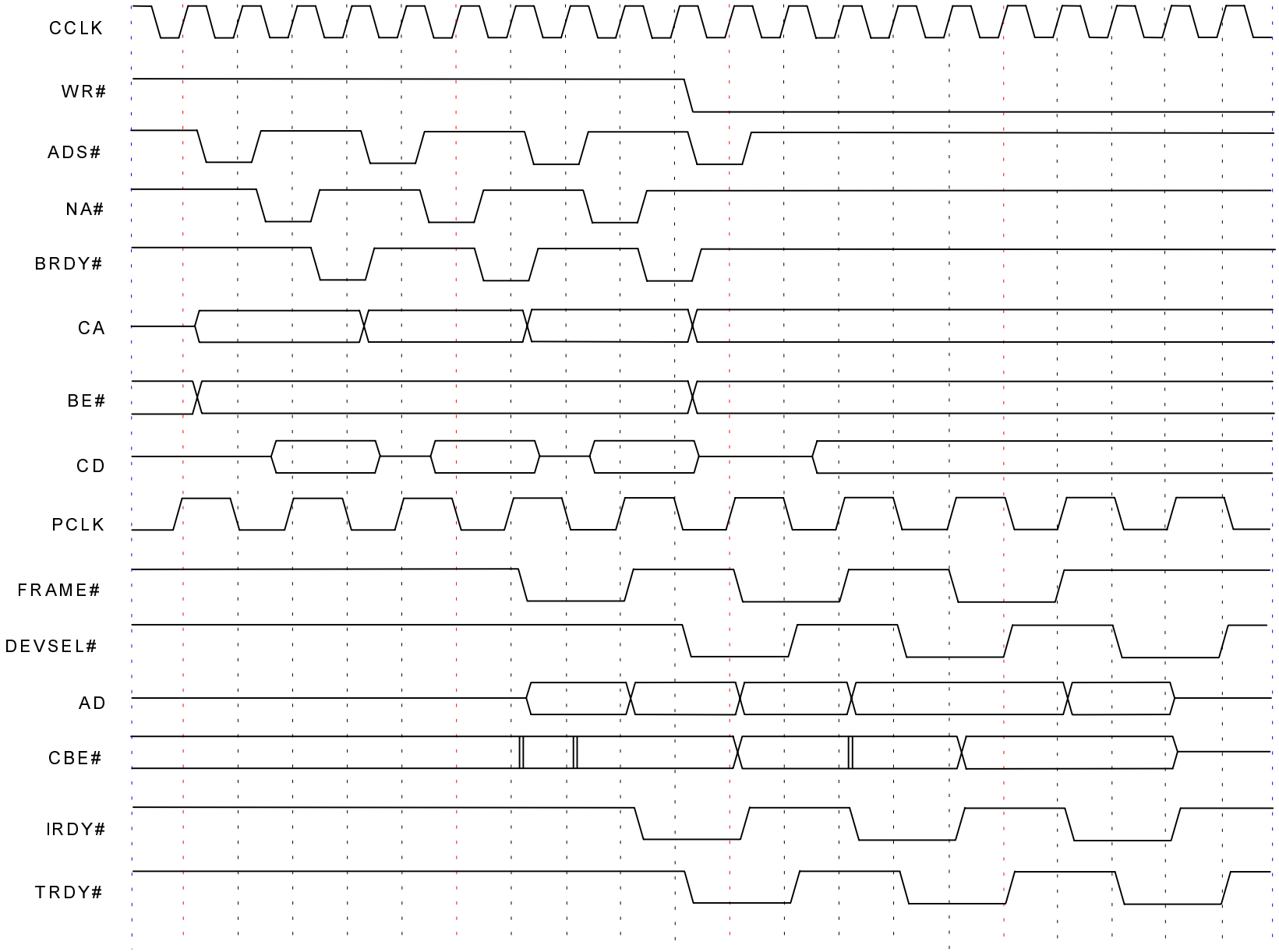

Figure 15. CPU WRITE PCI SLAVE WRITE BUFFER ON FAST BACK TO BACK

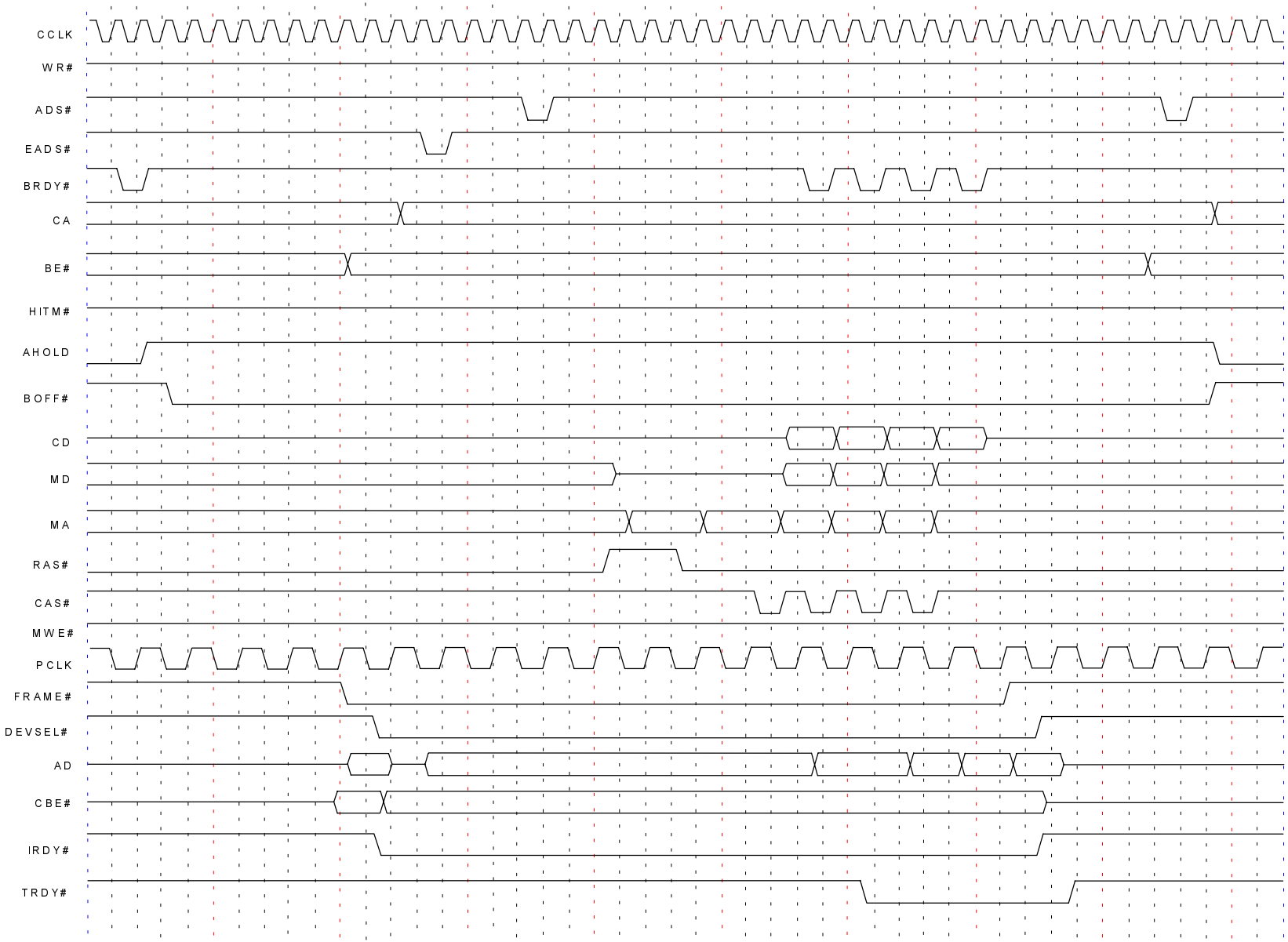

Figure 16. PCI MASTER READ HIT DRAM

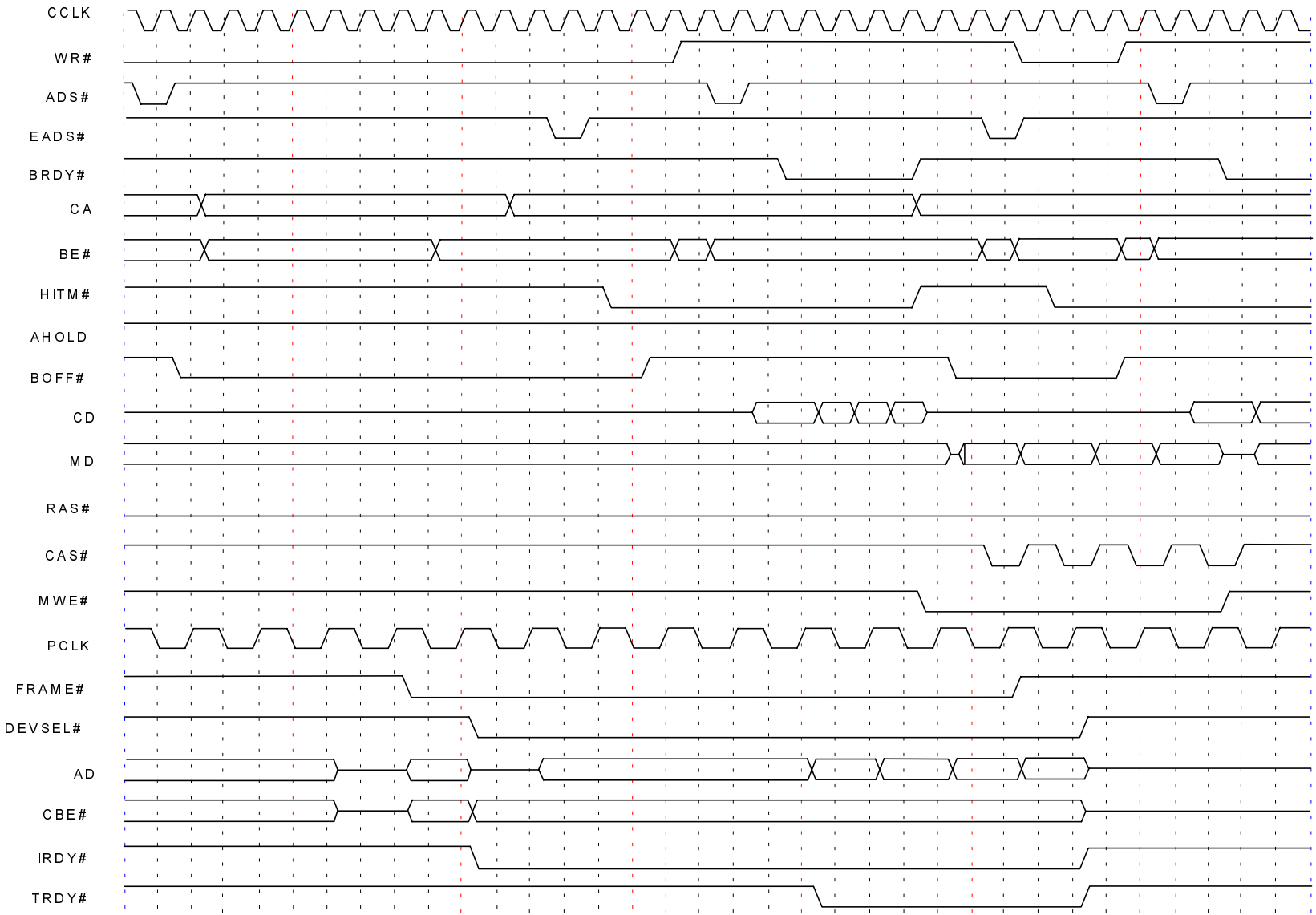

Figure 17. PCI MASTER READ L1 SNOOP TO DRAM

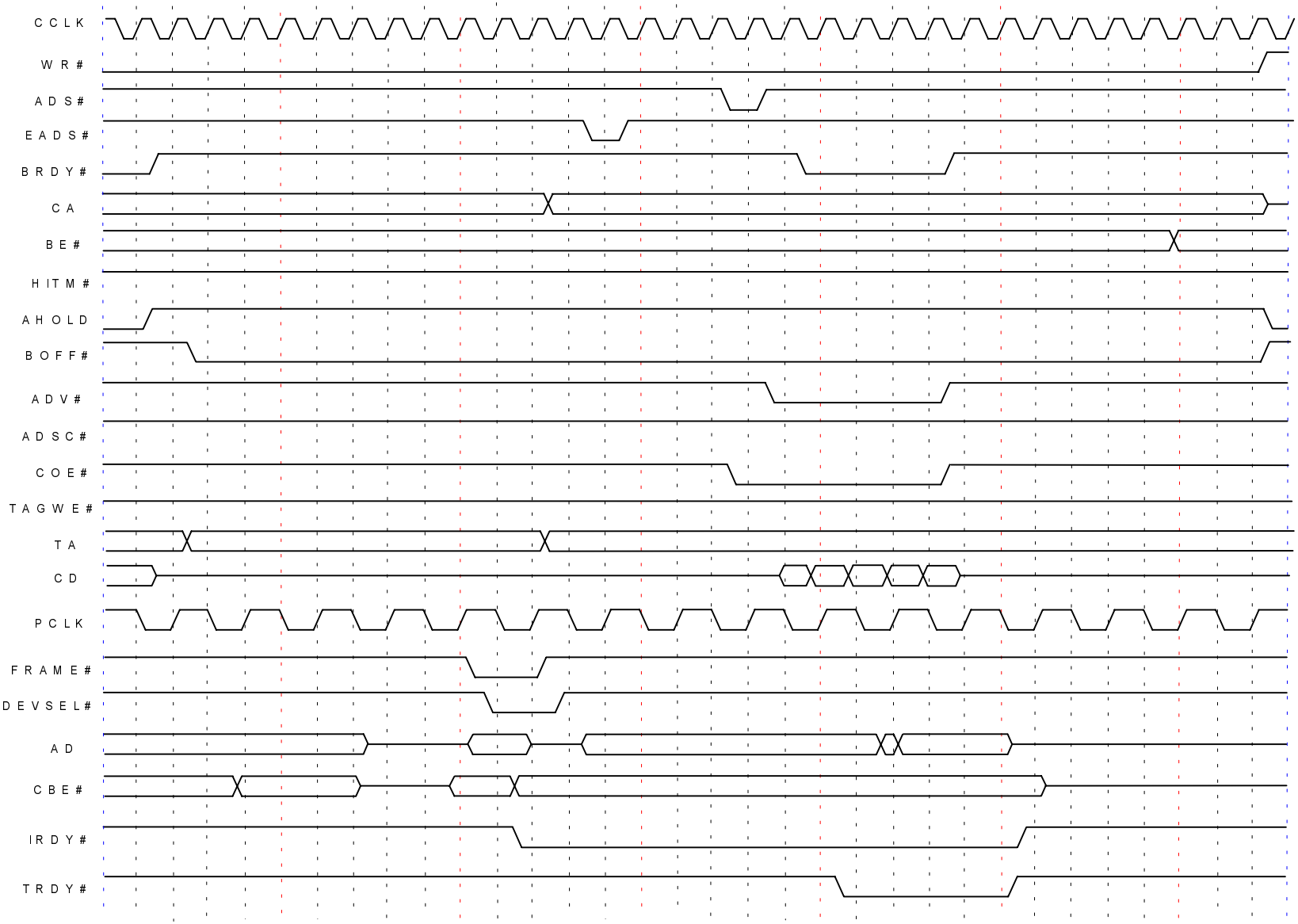

Figure 18. PCI MASTER READ HIT L2

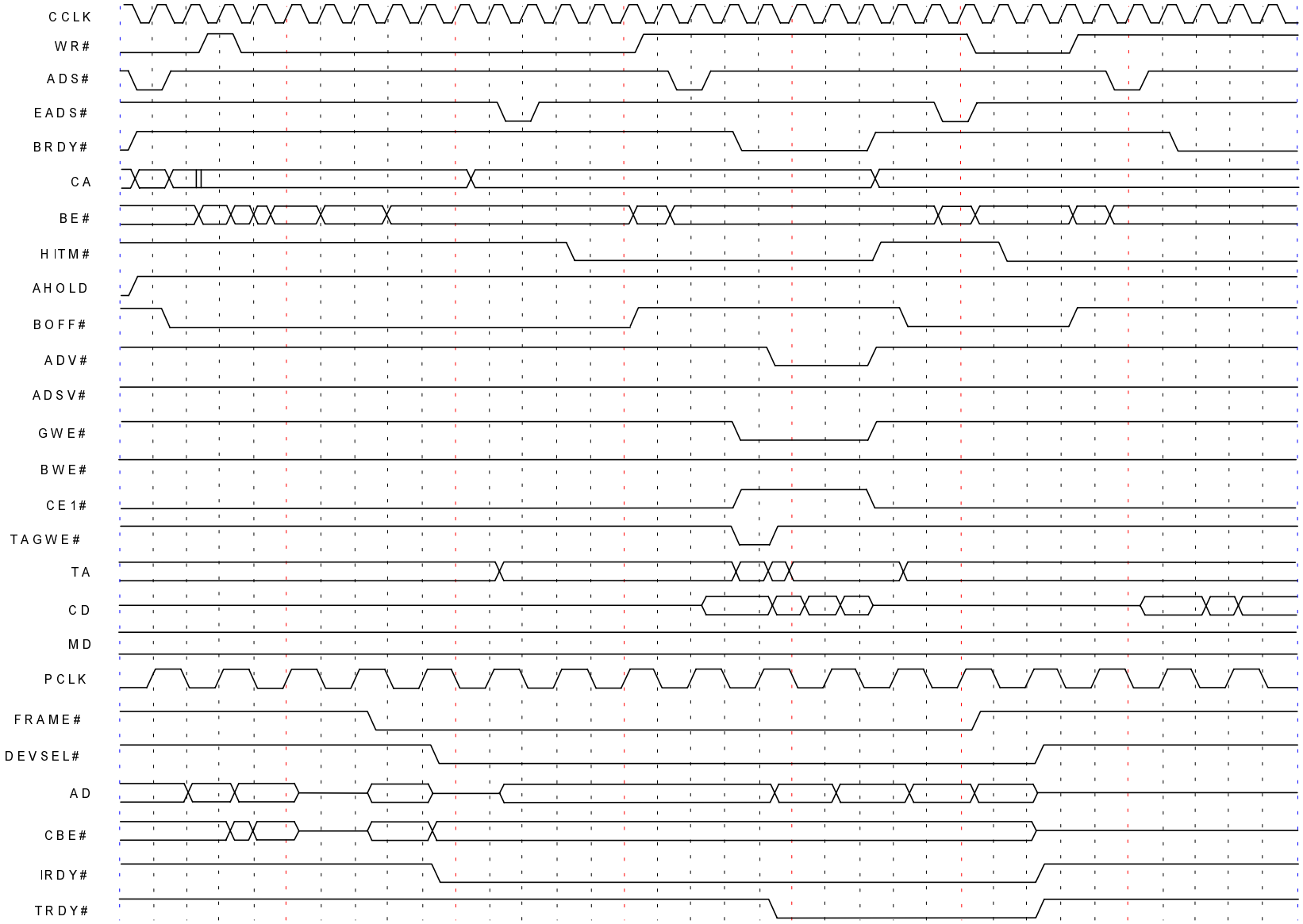

Figure 19. PCI MASTER READ L1 SNOOP TO L2

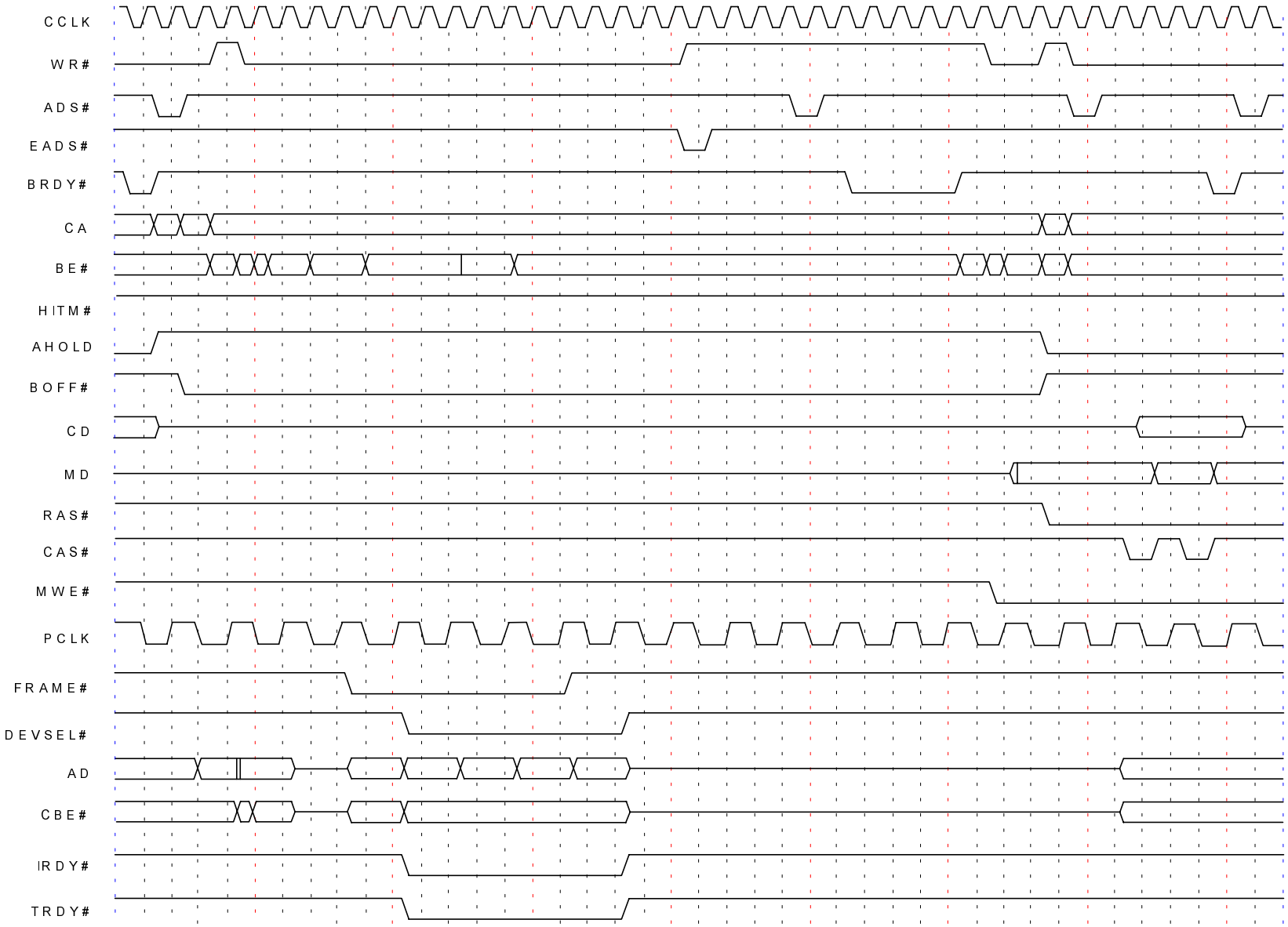

Figure 20. PCI MASTER WRITE DRAM

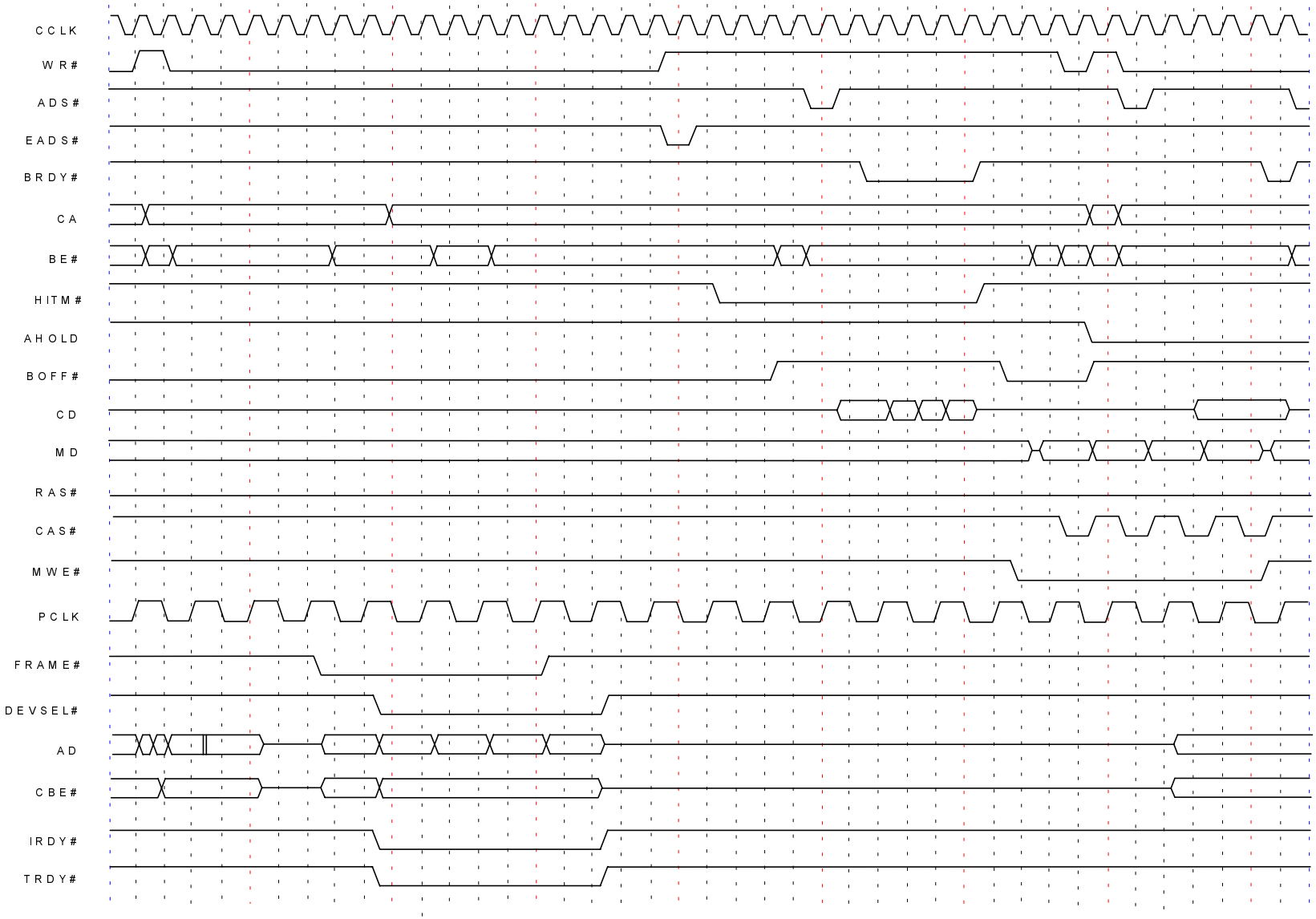

Figure 21. PCI MASTER WRITE HIT L1 SNOOP TO DRAM

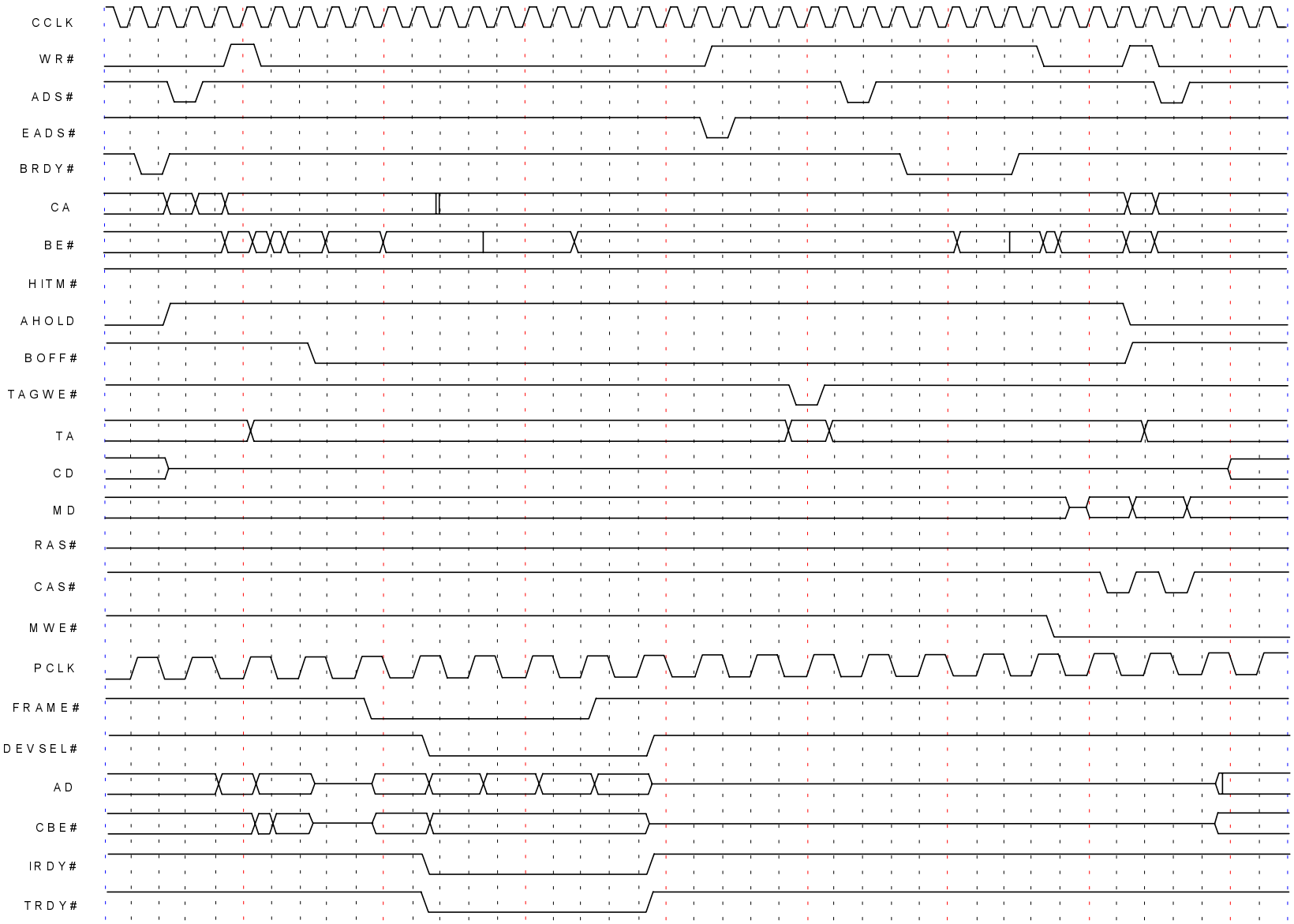

Figure 22. PCI MASTER WRITE HIT L2

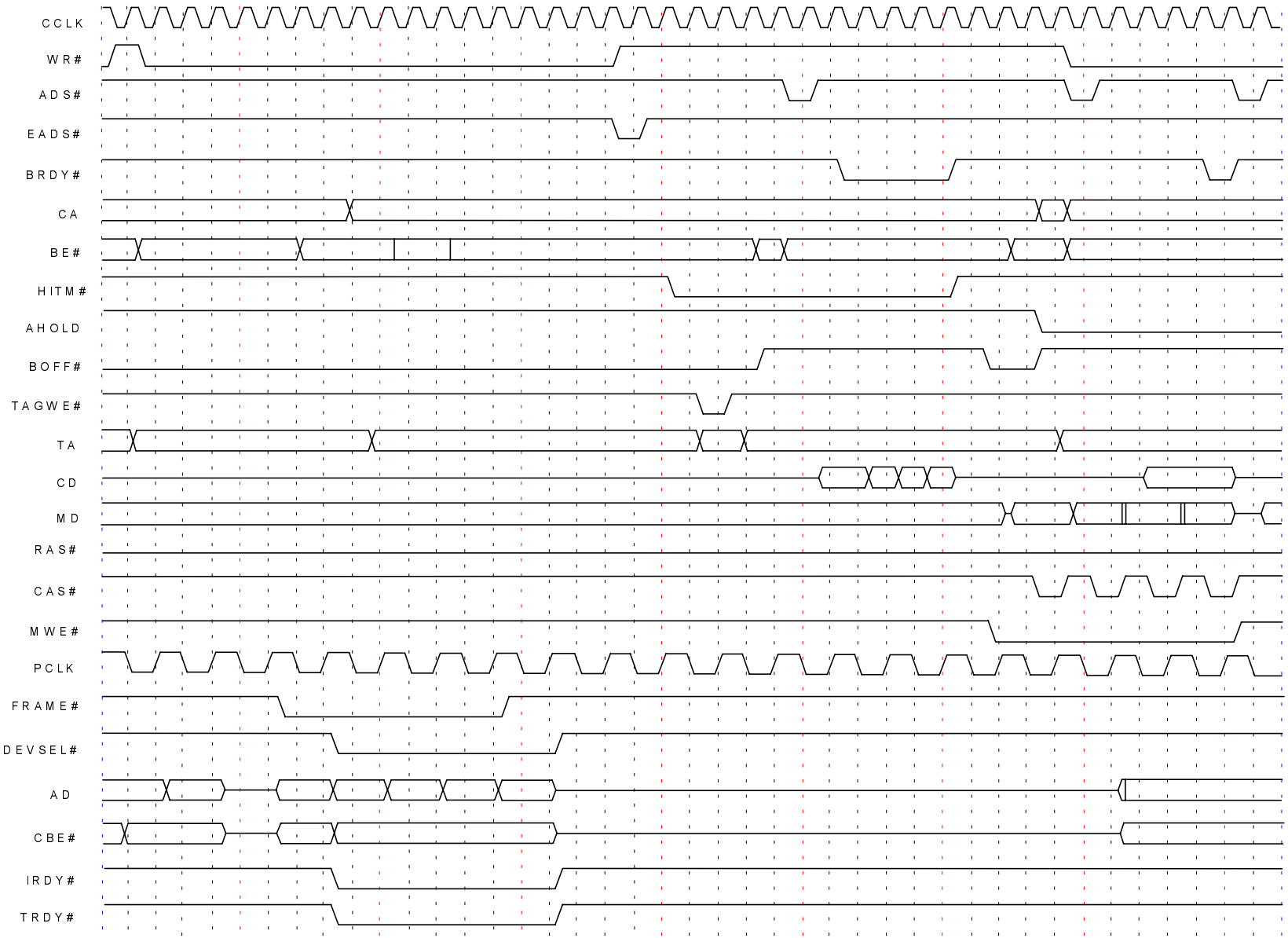

Figure 23. PCI MASTER WRITE HIT L2, L1 HITM

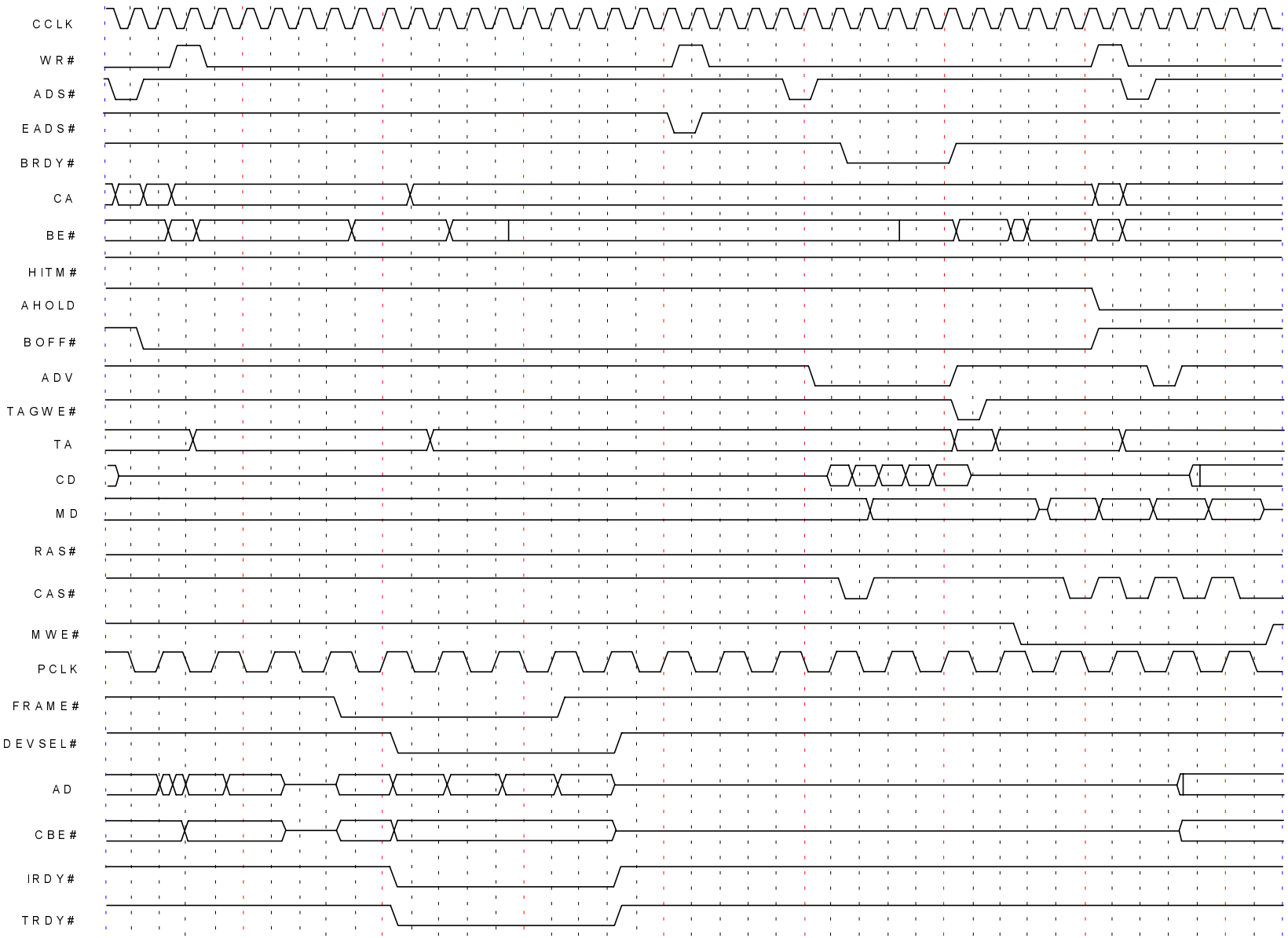

Figure 24. PCI MASTER WRITE HIT L2 & DIRTY

PACKAGE MECHANICAL SPECIFICATIONS

PQFP-208

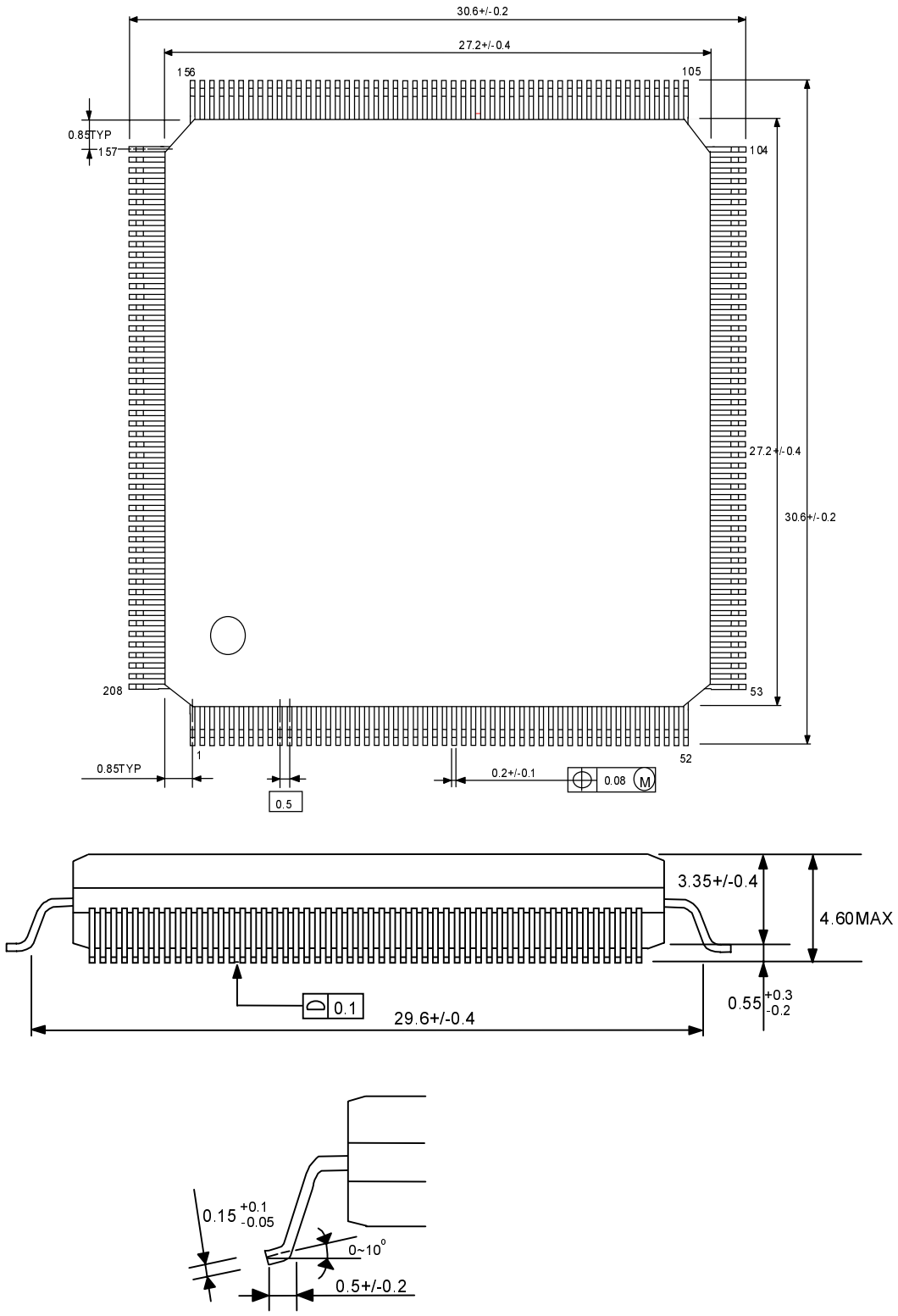

Figure 25. Mechanical Specifications - 208-Pin Plastic Flat Package

PQFP-100

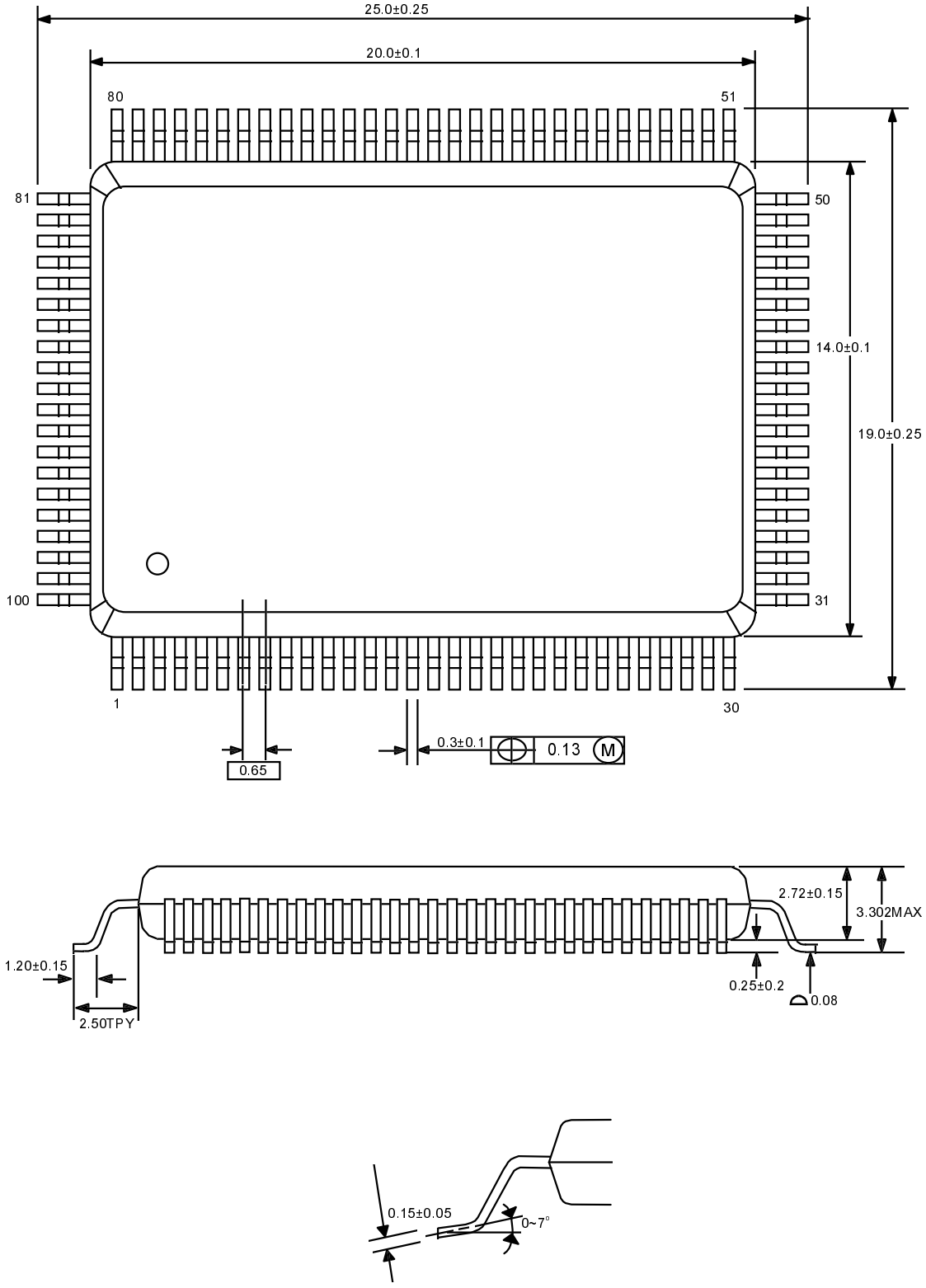

Figure 26. Mechanical Specifications - 100-Pin Plastic Flat Package