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Configuration Registers of VT82C425MV

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Two ports are provided for the access of configuration registers, first by write 8 bit index to port A8H and then by read or write 8 bit from/to data port A9H.

RX00: Chip and revision ID (read only)

bit 7-4 = Chip ID
bit 3-0 = Revision ID

Chipset	Chipset ID	Revision ID
VT82C425MV-D	1001	0001

RX01: XD bus switch register

Bit 0-1 reflects XD bus XD0-1 power-on jumper setting, 1 reflects pull high, 0 reflects pull low.

bit 7-6 = reserved.
bit 5 = reserved, must be 1.
bit 4-2 = reserved
bit 1-0 = CPU type
00 : 80386SX
01 : 80486LP
10 : 80386DX
11 : 80486

RX02: Slow counter. Pulse width of STPCLK# throttling is controlled by bit 6-0 (default is 02H)

bit 7 = 1/0 : enable/disable slow function.
bit 6 = reserved.
bit 5 = reserved.
bit 4 = set throttling clock time base.
1 : 1.7 msec
0 : 3.35 usec.
bit 3-0 = STPCLK# duty cycle. (from 1/16 to 15/16, default is 4/16, 0 means disable.)

RX03: ISA bus control (default is 00H)

bit 7 = 1/0 : extra/normal ISA command delay.
bit 6 = 1/0 : 0/1 ROM wait state.
bit 5 = 1/0 : 5/4 ISA slave wait state.
bit 4 = 1/0 : 4/2 chipset register wait state.
bit 3 = 1/0 : enable/disable I/O recovery time.
bit 2 = 1/0 : enable/disable extend BALE
bit 1 = reserved, must be 0.
bit 0 = 1/0 : enable/disable decouple refresh.

RX04: ISA bus control (default is 00H)

bit 7 = reserved, must be 0.
bit 6 = 1/0 : enable/disable internal XRDY when slow down CPU clock.
bit 5 = 1/0 : enable/disable Port 92H fast reset.
bit 4 = 1/0 : enable/disable turbo pin for deturbo function.
bit 3 = reserved, must be 0.
bit 2 = reserved, must be 0.
bit 1 = reserved.
bit 0 = 1/0 : enable/disable LOCAL# pin used for PCI bridge function.

RX10: 80387 and DMA clock

bit 7 = 1/0 : 80387 present/not exist. Automatically checked from 80387 ERROR# pin. (Read only)
bit 6 = 1/0 : DMA clock = ISA bus clock/half ISA bus clock.

RX11: ISA bus clock rate (default is 00H)

bit 7 = 1/0 : enable/disable SA16 reversal for FLASH EPROM.
bit 6 = 1/0 : enable/disable ROM write for FLASH ROM.
bit 5 = 1/0 : enable/disable PS/2 mouse lock.
bit 4 = 1/0 : enable/disable A0 command.
bit 3 = 1/0 : enable/disable ISA CLK selection of bit 2-0. If disabled, ISA CLK=CLKIN/8.
bit 2-0 = 000 : CLKIN/3
001 : CLKIN/2
010 : CLKIN/4
011 : CLKIN/6
100 : CLKIN/5
101 : CLKIN/10
110 : CLKIN/12
111 : OSC/2 (14.318MHz/2=7.159MHz)

Note : Procedure for ISA bus clock switching.
1. Set bit 3 = 0.
2. Change value of bit 2-0.
3. Set bit 3 = 1.

RX20: DRAM configuration (default is 30H)

bit 7-5 = bank 0 number of column address
000 : disable
001 : 9-bit (256K-bit DRAM)
010 : 10-bit (1M-bit DRAM)
011 : 11 bit (4M-bit DRAM)
100 : 12 bit (16M-bit DRAM)
others: illegal
bit 4 = 1/0 : enable/ disable DRAM page mode
bit 3-1 = bank 1 number of column address
000 : disable
001 : 9-bit (256K-bit DRAM)
010 : 10-bit (1M-bit DRAM)
011 : 11 bit (4M-bit DRAM)
100 : 12 bit (16M-bit DRAM)
others: illegal
bit 0 = reserved.

RX21: DRAM configuration (default is 0EH)

bit 7-5 = bank 2 number of column address
- 000 : disable
- 001 : 9-bit (256K-bit DRAM)
- 010 : 10-bit (1M-bit DRAM)
- 011 : 11 bit (4M-bit DRAM)
- 100 : 12 bit (16M-bit DRAM)
- others: illegal

bit 4 = reserved.

bit 3-1 = bank 3 number of column address
- 000 : disable
- 001 : 9-bit (256K-bit DRAM)
- 010 : 10-bit (1M-bit DRAM)
- 011 : 11 bit (4M-bit DRAM)
- 100 : 12 bit (16M-bit DRAM)
- others: illegal

bit 0 = 1/0 : enable/disable fast 2X mode

Note :. Fast 2X is available only when second level cache is disabled, which asserts CAS# in the middle of T2 state.

RX22: DRAM timing (default is 44H)

bit 7-6 = RAS# precharge width
- 00 : 1 cycle
- 01 : 2 cycles
- 10 : 3 cycles
- 11 : 4 cycles

bit 5-4 = RAS# pulse width
- 00 : 2 cycle
- 01 : 3 cycles
- 10 : 4 cycles
- 11 : 5 cycles

bit 3-2 = Read cycle CAS# pulse width
- 00 : 1 cycle
- 01 : 2 cycles
- 10 : 3 cycles
- 11 : 4 cycles

bit 1 = Write cycle CAS# pulse width
- 0 : 1 cycle
- 1 : 2 cycles

bit 0 = RAS# to column address and column address to CAS#
- 0 : 1 cycle
- 1 : 2 cycles

RX30: C segment shadow control (default is 00H)

bit 7 = 1/0 : enable/disable CC000-CFFFF shadow area read operation.
bit 6 = 1/0 : enable/disable CC000-CFFFF shadow area write operation.
bit 5 = 1/0 : enable/disable C8000-CBFFF shadow area read operation.
bit 4 = 1/0 : enable/disable C8000-CBFFF shadow area write operation.
bit 3 = 1/0 : enable/disable C4000-C7FFF shadow area read operation.
bit 2 = 1/0 : enable/disable C4000-C7FFF shadow area write operation.
bit 1 = 1/0 : enable/disable C0000-C3FFF shadow area read operation.

bit 0 = 1/0 : enable/disable C0000-C3FFF shadow area write operation.

RX31: D segment shadow control (default is 00H)

bit 7 = 1/0 : enable/disable DC000-DFFFF shadow area read operation.
bit 6 = 1/0 : enable/disable DC000-DFFFF shadow area write operation.
bit 5 = 1/0 : enable/disable D8000-DBFFF shadow area read operation.
bit 4 = 1/0 : enable/disable D8000-DBFFF shadow area write operation.
bit 3 = 1/0 : enable/disable D4000-D7FFF shadow area read operation.
bit 2 = 1/0 : enable/disable D4000-D7FFF shadow area write operation.
bit 1 = 1/0 : enable/disable D0000-D3FFF shadow area read operation.
bit 0 = 1/0 : enable/disable D0000-D3FFF shadow area write operation.

RX32 E/F segment shadow and DRAM burst control (default is 00H)

bit 7 = 1/0 : enable/disable E0000-EFFFF shadow area read operation.
bit 6 = 1/0 : enable/disable E0000-EFFFF shadow area write operation.
bit 5 = 1/0 : enable/disable F0000-FFFFF shadow area read operation.
bit 4 = 1/0 : enable/disable F0000-FFFFF shadow area write operation.
bit 4 = reserved.
bit 2 = 1/0 : enable/disable 1MB hole at top of 16MB, start from 0F00000H.
bit 1 = 1/0 : enable/disable DRAM burst read.
bit 0 = reserved, must be 0.

RX33: ROM decoding and DRAM relocation (default is 00H).

bit 7 = 1/0 : C8000-CFFFF is decoded as ROM/ISA cycle.
bit 6 = 1/0 : C0000-C7FFF is decoded as ROM/ISA cycle.
bit 5 = 1/0 : E8000-EFFFF is decoded as ROM/ISA cycle.
bit 4 = 1/0 : E0000-E8FFF is decoded as ROM/ISA cycle.
bit 3-2 = 256K/384K relocation
    00 : no relocation
    01 : illegal
    10 : 256K relocation
    11 : 384K relocation
bit 1-0 = reserved, must be 0.

RX38: ROM cacheable (default is 00H)

bit 7 = 1/0 : enable/disable C0000-C7FFF to be cacheable and write protect.
bit 6 = 1/0 : enable/disable F0000-FFFFF to be cacheable and write protect.
bit 5 = 1/0 : enable/disable E0000-EFFFF to be cacheable and write protect.
bit 4 = reserved.
bit 3 = 1/0 : enable/disable CAS before RAS refresh.
bit 2 = 1/0 : enable/disable fast ISA master command sampling.
bit 1-0 = delay of CAS# during DMA write cycle.
    00: disable
    01 : 1 CPU clock
    10 : 2 CPU clocks
    11 : 3 CPU clocks

RX39: Non-cacheable area base address

bit 7-0 = A26-A19

RX3A: Non-cacheable area base address/size (default is 00H)

bit 7-5 = A18-A16
bit 4 = 1/0 : enable/disable IOCHRDY# for ISA master DRAM access.
bit 3-1 = non-cacheable area size
000 : disable
001 : 64KB
010 : 128KB
011 : 256KB
100 : 512KB
101 : 1MB
110 : 2MB
111 : 4MB
bit 0 = 0/1, enable/disable synchronous of local bus ready. If enabled, LRDY# is synchronous by 1 CPU clock and then pass to READY#.

RX3B: DRAM size and SIMM type (default: 00H)

bit 7-5 = DRAM size of bank 0
000 : 512KB
001 : 1MB
010 : 2MB
011 : 4MB
100 : 8MB
101 : 16MB
110 : 32MB
111 : 64MB
bit 4 = 1/0 : double/single side SIMM for bank 0
bit 3-1 = DRAM size of bank 1
000 : 512KB
001 : 1MB
010 : 2MB
011 : 4MB
100 : 8MB
101 : 16MB
110 : 32MB
111 : 64MB
bit 0 = 1/0 : double/single side SIMM for bank 1

RX3C: DRAM size and SIMM type (default: 00H)

bit 7-5 = DRAM size of bank 2
000 : 512KB
001 : 1MB
010 : 2MB
011 : 4MB
100 : 8MB
101 : 16MB
110 : 32MB
111 : 64MB
bit 4 = 1/0 : double/single side SIMM for bank 2
bit 3-1 = DRAM size of bank 3
000 : 512KB
001 : 1MB

010 : 2MB
011 : 4MB
100 : 8MB
101 : 16MB
110 : 32MB
111 : 64MB
bit 0 = 1/0 : double/single side SIMM for bank 3

RX40: Port 70H shadow register.

This register is a shadow of port 70H.

RX41: Port 2F8H shadow register.

This register is a shadow of port 2F8H.

RX42: Port 3F8H shadow register.

This register is a shadow of port 3F8H.

RX43: Port 372H shadow register.

This register is a shadow of port 372H.

RX44: Port 377H shadow register.

This register is a shadow of port 377H.

RX45: Port 171H shadow register.

This register is a shadow of port 171H.

RX46: Port 177H shadow register.

This register is a shadow of port 177H.

RX47: Port 376H shadow register.

This register is a shadow of port 376H.

RX48: Port 1F1H shadow register.

This register is a shadow of port 1F1H.

RX49: Port 1F7H shadow register.

This register is a shadow of port 1F7H.

RX4A: Port 3F6H shadow register.

This register is a shadow of port 3F6H.

RX4B: General IO port direction control (default: 00H)

bit 7-5 : reserved.
bit 4-0 : GPIO4-0 direction
1/0 = output/input

RX4C: General IO port value control

bit 7 : DPC4 output value
bit 4-0 : GPIO4-0 port value (read for input ports and read/write for output ports)

RX50: SLOWIN function and debounce control (default: 00H)

bit 7-5 : reserved
bit 4 = 1/0 : debounce clock select 512ms/8ms
bit 3 = 1/0 : SLOWIN/CONSERVE mode
0 : clock stretching
1 : clock throttling
bit 2 = 1/0 : SLOWIN event status: occurred/not occurred
bit 1 = 1/0 : SLOWIN active high/low
bit 0 = 1/0 : SLOWIN pin enable/disable

RX51: Pulse width modulation control (default: 00H)

bit 7-6 = period of PWM0 (GPIO0)
00 : 1/64 sec
01 : 1/16 sec
10 : 1 sec
11 : 4 sec
bit 5-4 = duty cycle percentage of PWM0
00 : 0 (PWM0 function disabled and GPIO0 used as a general IO port)
01 : 1/4
10 : 1/2
11 : 3/4
bit 3-2 = period of PWM1 (GPIO1)
00 : 1/64 sec
01 : 1/16 sec
10 : 1 sec
11 : 4 sec
bit 1-0 = duty cycle percentage of PWM1
00 : 0 (PWM1 function disabled and GPIO1 used as a general IO port)
01 : 1/4
10 : 1/2
11 : 3/4

RX52: Primary activity detector control (reload primary idle timer)

bit 7 = 1/0 : enable/disable detection of keyboard access, R/W port 60H.
bit 6 = 1/0 : enable/disable detection of serial port, R/W port 3F8-3FF, 2F8-2FF, 3E8-3EF, 2E8-2EF.
bit 5 = 1/0 : enable/disable detection of parallel port, R/W port 378-37F, 278-27F.
bit 4 = 1/0 : enable/disable detection of video access, R/W port 3B0-3DF, memory A and B segment.
bit 3 = 1/0 : enable/disable detection of IDE and floppy access. R/W port 1F0-1F7, 170-177, 3F5.
bit 2 = 1/0 : enable/disable detection of programmable IO port (RX6D-6E)
bit 1 = 1/0 : enable/disable detection of sound/speaker R/W port 43, 220.
bit 0 = 1/0 : enable/disable detection of DRQ/LREQ#, positive edge for DRQ, negative edge for LREQ#.

Note : RX52 is used with RX54 bit 5 to control the source of power management interrupt.

RX53: Primary activity status

bit 7 = 1/0 : keyboard activity exist/not exist, (R/W port 60H).
bit 6 = 1/0 : serial port activity exist/not exist, (R/W port 3F8-3FF, 2F8-2FF, 3E8-3EF, 2E8-2EF).
bit 5 = 1/0 : parallel port activity exist/not exist, (R/W port 378-37F, 278-27F).
bit 4 = 1/0 : video activity exist/not exist, (R/W port 3B0-3DF, memory A and B segment).
bit 3 = 1/0 : IDE and floppy activity exist/not exist, (R/W port 1F0-1F7, 3F7).
bit 2 = 1/0 : programmable I/O port activity exist/not exist, (as defined by RX6D-6E).
bit 1 = 1/0 : sound/speaker activity exist/not exist, (R/W 43, 220).
bit 0 = 1/0 : DRQ/LREQ# activity exist/not exist, (positive edge for DRQ, negative edge for LREQ#.

Note :

1. RX53 is not controlled by RX52, it will be latched with or without enable RX52.
2. RX53 is also used to generate power management interrupt if RX54 bit 5 is enabled. The status of primary activities can only be cleared by write 1 to individual bit, and it is recommended to clear RX53 before enable RX52 and RX54 bit 5.

RX54: Power management interrupt (PMI) event control

bit 7 = 1/0 : enable/disable idle timer time out to trigger PMI.
bit 6 = 1/0 : enable/disable GP timer time out to trigger PMI.
bit 5 = 1/0 : enable/disable primary activity to trigger PMI.
bit 4 = 1/0 : enable/disable primary interrupt to trigger PMI.

Note : Each IRQ can be individually controlled to trigger PMI, please refer to RX60 and RX61.

bit 3 = 1/0 : enable/disable turbo pin to trigger PMI.
bit 2 = 1/0 : enable/disable DRQ/LREQ# to trigger PMI.
bit 1 = 1/0 : enable/disable extended PMI to trigger PMI (extended in RX6B)
bit 0 = write 1 to this bit generates a software PMI.

Note : RX53 is used to generate power management interrupt if RX54 bit 5 is enabled. The status of primary activities can only be cleared by write 1 to individual bit, and it is recommended to clear RX53 before enable RX52 or RX54 bit 5.

RX55: Power management interrupt (PMI) status

bit 7 = idle timer time out.
bit 6 = GP timer time out.
bit 5 = primary activity.
bit 4 = primary interrupt.
bit 3 = turbo pin.
bit 2 = DRQ/LREQ# pulse.
bit 1 = extended PMI (extended in RX6C).
bit 0 = software PMI.

Note : The status of power management interrupt can only be cleared by write 1 to individual bit

RX56: CPU clock control

bit 7-5 = clock selection
000 : CLKIN (Full-on mode)
001 : CLKIN/4 (Doze mode)
010 : CLKIN/8 (Doze mode)

011 : CLKIN/16 (Doze mode)
100 : CLKIN/32 (Doze mode)
101 : CLKIN/64 (Doze mode)
110 : CLKIN/2 (Doze mode)
111 : Stop clock (Suspend mode)

bit 4 = reserved.

bit 3-0 = clock generator selection of 82C406MV

bit 2	bit 1	bit 0	bit 3=1	bit 3=0
0	0	0	8Mhz	16Mhz
0	0	1	20Mhz	40Mhz
0	1	0	25Mhz	50Mhz
0	1	1	40Mhz	80Mhz
1	0	0	33.3Mhz	66.6Mhz
1	0	1	50Mhz	100Mhz
1	1	0	4Mhz	8Mhz
1	1	1	30Mhz	60Mhz

Note : Procedure to change clock.
1. Write clock selection value to RX56 bit 7-5.
2. Set RX5D bit 7 to 1.

RX57: 1st peripheral timer count value (time base is bit 1-0 of RX66)

RX58: General purpose (GP) timer count value (time base is bit 7-6 of RX59)

RX59: Timer control (default: 00H)

bit 7-6 = GP timer time base (timer is RX58)
00 : disable
01 : 32.768K
10 : 1 second
11 : 1 minute

bit 5-4 = STPCLK# recovery time or auto stop grant delay time

bit5,4	STPCLK# recovery time (RX5D bit 3 = 0)	Auto stop grant delay time (RX5D bit 3 = 1)
00	immediately	immediately
01	1ms	0.5ms
10	0.375 ms	0.1875ms
11	0.125 ms	0.0625ms

bit 3-1= primary idle timer time out value
000 : disable
001 : 2 second
010 : 8 second
011 : 32 second
100 : 2 minute
101 : 8 minute
110 : 16 minute
111 : 32 minute

Note : Primary idle timer time out is not re-triggerable, the correct procedure to use idle timer is:
1. Load idle timer value into RX59 bit 3-1.
2. Set RX54 bit 7 to 1, start counting.
3. After time out, reload idle timer value (RX59 bit 3-1) and set RX54 bit 7 again.

bit 0 : reserved.

RX5A: General purpose output ports (default: FFH)

bit 7-4 = PC3-0 output value (by MA and PCWE#).
bit 3-0 = DPC3-0 direct output value.

Note: DPC3-0 have two sets register, power down mode and normal mode, which are selected by RX5D bit 0. DPC3-0 for power down will be sent out during power down mode, and DPC3-0 for normal mode will be sent out when resume from power down.

RX5B: SMM control (default: 00H)

bit 7 = 1/0 : enable/disable power management mode.
bit 6 = CPU type for SMM protocol.
0 : Intel
1 : AMD/Cyrix
bit 5 = PMI connection
0 : PMI directly output to pin 141 SMI#.
1 : PMI internal connect to IRQ15 of interrupt controller.
bit 4 = 1/0 : enable/disable of SMM address remap to A0000-BFFFF.
(Intel : 30000-4FFFF, AMD/Cyrix : 60000H-7FFFF)
bit 3 = 1/0 : enable/disable to access DRAM A0000-BFFFF.
bit 2 : reserved.
bit 1 = 1/0 : enable/disable force SMM mode, which forces access of 30000-4FFFF remap to A0000-BFFFF.
bit 0 = 1/0 : enable/disable STPCLK# throttling mode, the STPCLK# will periodically be asserted to reduce power consumption of CPU. STPCLK# pulse width is controlled by RX02.

RX5C: Misc.

bit 7 = wait for HALT cycle to start clock change.
0 : immediately
1 : wait for HALT
bit 6 = wait for acknowledge response when clock change.
0 : do not wait
1 : wait for acknowledge (For INTEL S-Series, it is STOP GRANT cycle. For Cyrix, it is SUSPA#.)
bit 5 = CPU type for change clock protocol.
0 : Cyrix SUSPA# protocol
1 : Intel STPCLK# protocol or Cyrix SUSP# protocol

Note: Following is an example table to use bit 7,6,5.

CPU	Bit 7,6,5	Description
INTEL S series	011	INTEL stop grant protocol
Cyrix CPU	110	Support SUSPA# input signal only, BIOS must use HALT instruction to go into suspend mode.

Cyrix CPU	011	Support SUSP# output signal only, RX5D bit 3 auto stop grand can be used to go to suspend mode.

bit 4 = reserved.
bit 3 = turbo pin status. (read only)
bit 2 = reserved, must be 0.
bit 1 = 1/0 : enable/disable soft reset for write back CPU and INTEL S series CPU (default: 0)
bit 0 = 1/0 : enable/disable 1 wait delay for local master write cycle.

RX5D: Change CPU clock and misc. control

bit 7 = write 1 to start change CPU clock operation.
bit 6 = 1/0 : enable/disable PMI to automatically wakeup clock.
bit 5 = 1/0 : enable/disable SMI# active until SMIADS#.
bit 4 = 1/0 : enable/disable turbo pin to be used as keyboard lock, (low active).
bit 3 = write 1 to enable auto stop grand protocol. (for Cyrix CPU)
bit 2 = reserved.
bit 1 = 1/0 : enable/disable DRAM power down leakage control
bit 0 = 1/0 : enable/disable power down leakage control

Note: RX5D bit 0 can be used to select two sets register of RX5A bit 3-0. To go into power down mode, set RX5D bit 0 =1 and change CPU clock to 0MHz. To exit power down mode, use signal EXTSMI0.

RX5E: Misc. (default: 10H)

bit 7 = 1/0 : enable/disable Write-Back CPU mode.
bit 6 = 1/0 : reserved
bit 5 = CACHE# and BLAST# signal sharing for data streaming.
0 : BLAST# is used on pin 72.
1 : CACHE# is used.
bit 4 = 1/0 : enable/disable snoop filtering for ISA master.
bit 3 = 1/0 : enable/disable one CPU clock delay of ISA bus ready.
bit 2 = 1/0 : enable/disable two times longer slow refresh.
bit 1 = reserved
bit 0 = write 1 to this bit asserts STPCLK# signal and force CPU goes into suspend without change clock.

RX5F: Conserve and secondary event mode control (default: 00H)

bit 7-6 = conserve mode time out value
00 : 1/16 sec
01 : 1/8 sec
10 : 1 second
11 : 1 minute

Note : This value is the time elapsed to go into conserve mode if there is no primary activity.

bit 5 = 1/0 : enable/disable conserve mode.(write)
: status of conserve mode. (read)
bit 4 = conserve mode clock select
0 : CLKIN/2
1 : CLKIN/4
bit 3-2 = secondary event timer value

00 : 2 ms
01 : 16 ms
10 : 64 ms
11 : after EOI (IO write to port 20H) plus 0.125ms

Note : System will wake up (go to secondary event mode) when secondary event is coming, and then automatically exit from secondary event mode after this time value is elapsed.

bit 1 = 1/0 : enable/disable secondary event mode. (write)
: status of secondary event mode. (read)
bit 0 = secondary event mode clock select
0 : CLKIN (full speed)
1 : CLKIN/2

RX60: Interrupt event/activity detection control (default: FEh)

bit 7 = 1/0 : set IRQ7 as primary/secondary event.
bit 6 = 1/0 : set IRQ6 as primary/secondary event.
bit 5 = 1/0 : set IRQ5 as primary/secondary event.
bit 4 = 1/0 : set IRQ4 as primary/secondary event.
bit 3 = 1/0 : set IRQ3 as primary/secondary event.
bit 2 = 1/0 : set IRQ1 as primary/secondary event.
bit 1 = 1/0 : set IRQ0 as primary event.
bit 0 = 1/0 : enable/disable IRQ to reload idle timer.

Note :

1. Primary event can be used to reload idle timer or generate PMI.
2. Secondary event is used to go into secondary event mode.
3. RX60 bit 0 must be used with RX60 bit 7-1 and RX61 bit 7-0 to control IRQ reload idle timer.
4. RX54 bit 4 must be used with RX60 bit 7-1 and RX61 bit 7-0 to control IRQ positive edge to trigger PMI.
5. Use RX62 bit 1 to set IRQ0 as secondary event.

RX61: Interrupt event/activity detection control (default: FFH)

bit 7 = 1/0 : set IRQ15 as primary/secondary event.
bit 6 = 1/0 : set IRQ14 as primary/secondary event.
bit 5 = 1/0 : set IRQ13 as primary/secondary event.
bit 4 = 1/0 : set IRQ12 as primary/secondary event.
bit 3 = 1/0 : set IRQ11 as primary/secondary event.
bit 2 = 1/0 : set IRQ10 as primary/secondary event.
bit 1 = 1/0 : set IRQ9 as primary/secondary event.
bit 0 = 1/0 : set IRQ8 as primary event.

RX62: Level trigger interrupt control (default: 06H)

bit 7 = 1/0 : enable/disable IRQ7 as a level trigger interrupt.
bit 6 = 1/0 : enable/disable IRQ6 as a level trigger interrupt.
bit 5 = 1/0 : enable/disable IRQ5 as a level trigger interrupt.
bit 4 = 1/0 : enable/disable IRQ4 as a level trigger interrupt.
bit 3 = 1/0 : enable/disable IRQ3 as a level trigger interrupt.
bit 2 = 1/0 : enable/disable IRQ8 as secondary event.
bit 1 = 1/0 : enable/disable IRQ0 as secondary event.

bit 0 = 1/0 : enable/disable level trigger interrupt.

Note : RX62 bit 0 must be used with RX62 bit 7-3 and RX63 to control level trigger interrupt.

RX63: Level trigger interrupt control (default: 00H)

bit 7 = 1/0 : enable/disable IRQ15 as a level trigger interrupt.
bit 6 = 1/0 : enable/disable IRQ14 as a level trigger interrupt.
bit 5 = 1/0 : enable/disable DMA/interrupt/timer controller shadow read.
bit 4 = 1/0 : enable/disable IRQ12 as a level trigger interrupt.
bit 3 = 1/0 : enable/disable IRQ11 as a level trigger interrupt.
bit 2 = 1/0 : enable/disable IRQ10 as a level trigger interrupt.
bit 1 = 1/0 : enable/disable IRQ9 as a level trigger interrupt.
bit 0 = 1/0 : enable/disable 1 clock ADS# delay.

RX64: Power on switch setting.

bit 7 = 1/0 : disable/enable 1 clock BRDY# delay for burst write cycle.
bit 6 = 1/0 : enable/disable EADS# asserted at the beginning of SMI#, to flush CPU.
bit 5 = 1/0 : enable/disable DRAM burst write.
bit 4 = 1/0 : enable/disable always return READY# in SMI# cycle, for AMD and UMC CPU.
bit 3 = switch setting of MA3.
bit 2 = switch setting of MA2.
bit 1 = switch setting of MA1.
bit 0 = switch setting of MA0.

RX65: Peripheral and secondary event timer control

bit 7 = 1/0 : enable/disable keyboard access to reload 1st peripheral timer, R/W port 60H.
bit 6 = 1/0 : enable/disable serial port to reload 1st peripheral timer, R/W port 3F8-3FF, 2F8-2FF, 3E8-3EF, 2E8-2EF.
bit 5 = 1/0 : enable/disable video access to reload 1st peripheral timer, R/W port 3B0-3DF, memory A and B segment.
bit 4 = 1/0 : enable/disable IDE and floppy access to reload 1st peripheral timer, R/W port 1F0-1F7, 170-177, 3F5.
bit 3 = 1/0 : enable/disable parallel port access to reload 2nd peripheral timer, R/W port 378-37F, 278-27F.
bit 2 = 1/0 : enable/disable programmable IO port to reload 2nd peripheral timer, R/W.
bit 1 = 1/0 : enable/disable speaker/sound port access to reload 2nd peripheral timer, R/W port 43 and 220.
bit 0 = 1/0 : enable/disable IDE and floppy access to reload 2nd peripheral timer, R/W port 1F0-1F7, 170-177, 3F5.

RX66: Peripheral timer control

bit 7-4 : reserved
bit 3-2 = 2nd peripheral timer select (timer is RX67)
  00 : disable
  01 : 32.768K
  10 : 1 second
  11 : 1 minute
bit 1-0 = 1st peripheral timer select (timer is RX57)
  00 : disable
  01 : 32.768K
  10 : 1 second

11 : 1 minute

RX67: 2nd peripheral timer count value (time base is bit 1-0 of RX66)

RX68: External PMI signal falling enable (default: 00H)

bit 7 = enable PMI for EXTSMI0 falling
bit 6 = enable PMI for EXTSMI1 falling
bit 5 = enable PMI for DOCKIN falling
bit 4 = enable PMI for CSWITCH falling
bit 3 = enable PMI for AC falling
bit 2 = enable PMI for BL falling
bit 1 = enable PMI for BW falling
bit 0 = enable PMI for BVL falling

RX69: External PMI signal rising enable (default: 00H)

bit 7 = enable PMI for EXTSMI0 rising
bit 6 = enable PMI for EXTSMI1 rising
bit 5 = enable PMI for DOCKIN rising
bit 4 = enable PMI for CSWITCH rising
bit 3 = enable PMI for AC rising
bit 2 = enable PMI for BL rising
bit 1 = enable PMI for BW rising
bit 0 = enable PMI for BVL rising

RX6A: External PMI status (write 1 to clear)

bit 7 : EXTSMI0 triggered PMI
bit 6 : EXTSMI1 triggered PMI
bit 5 : DOCKIN triggered PMI
bit 4 : CSWITCH triggered PMI
bit 3 : AC triggered PMI
bit 2 : BL triggered PMI
bit 1 : BW triggered PMI
bit 0 : BVL triggered PMI

RX6B: Extended PMI enable (default: 00H)

bit 7-4 : reserved
bit 3 = 1/0 : enable/disable 1st peripheral timer time out to trigger PMI
bit 2 = 1/0 : enable/disable 2nd peripheral timer time out to trigger PMI
bit 1 = 1/0 : enable/disable secondary event timer time out to trigger PMI
bit 0 = 1/0 : enable/disable external PMI pin to trigger PMI

RX6C: Extended PMI status

bit 7-4 : reserved
bit 3 : 1st peripheral timer time out
bit 2 : 2nd peripheral timer time out
bit 1 : secondary event timer time out
bit 0 : external PMI pin triggering

RX6D: General IO port address

bit 7-0: IO address A<7:0>

RX6E: General IO port address and mask

bit 7-2 : IO address compare mask A<5:0>
individual bit set to 1 means the bit will be compared (not masked)
bit 1-0 : IO address A<9:8>

RX6F: Hot key control (default : 00H)

bit 7 = 1/0 : enable/disable hot key code
bit 6 = 1/0 : hot key length equals 6/4 bits
bit 5-0 : hot key code

RX71: VL IDE configuration register (default: 00H)

bit 7 = 1 : transparent from IDE IRQ to ISA IRQ14.
0 : temporary hold IDE IRQ when prefetch buffer is full.
bit 6 = 1 : VL IDE located at 17xH and 376H.
0 : VL IDE located at 1FxH and 3F6H.
bit 5 = 1/0 : enable/disable write buffer to VL IDE.
bit 4 = 1/0 : enable/disable prefetch read buffer from VL IDE.
bit 3 = LRDY# timing of write buffer.
1 : asserted at first T2.
0 : asserted at second T2.
bit 2 = LRDY# timing of prefetch read buffer.
1 : asserted at first T2.
0 : asserted at second T2.
bit 1 = data present timing of prefetch read buffer.
1 : asserted at first T2.
0 : asserted at second T2.
bit 0 = 1/0 : enable/disable VL IDE module.

RX72: Non 1F0 timing control

bit 7-4 = number of clock for command active time. (default is 0F)
bit 3-0 = number of clock for command recovery time. (default is 0F)

RX73: Drive 0 data port 1F0 read cycle timing control

bit 7-4 = number of clock for command active time. (default is 0F)
bit 3-0 = number of clock for command recovery time. (default is 0F)

RX74: Drive 0 data port 1F0 write cycle timing control

bit 7-4 = number of clock for command active time. (default is 0F)
bit 3-0 = number of clock for command recovery time. (default is 0F)

RX77: Drive 0 address setup time.

bit 1-0 = number of clock before command asserted.

RX78: Drive 1 data port 1F0 read cycle timing control

bit 7-4 = number of clock for command active time. (default is 0F)
bit 3-0 = number of clock for command recovery time. (default is 0F)

RX79: Drive 1 data port 1F0 write cycle timing control

bit 7-4 = number of clock for command active time. (default is 0F)

bit 3-0 = number of clock for command recovery time. (default is 0F)

RX7C: Drive 1 address setup time.

bit 1-0 = number of clock before command asserted.

RX7F: Misc.

bit 4 = reserved, must be 1.
bit 3 = state machine decision making point.
1 : at first T2 risin g edge..
0 : at second T2 rising edge..
bit 2 = reserved, must be 0.