SL9350
80386DX Page Mode Memory Controller
PRELIMINARY

FEATURES

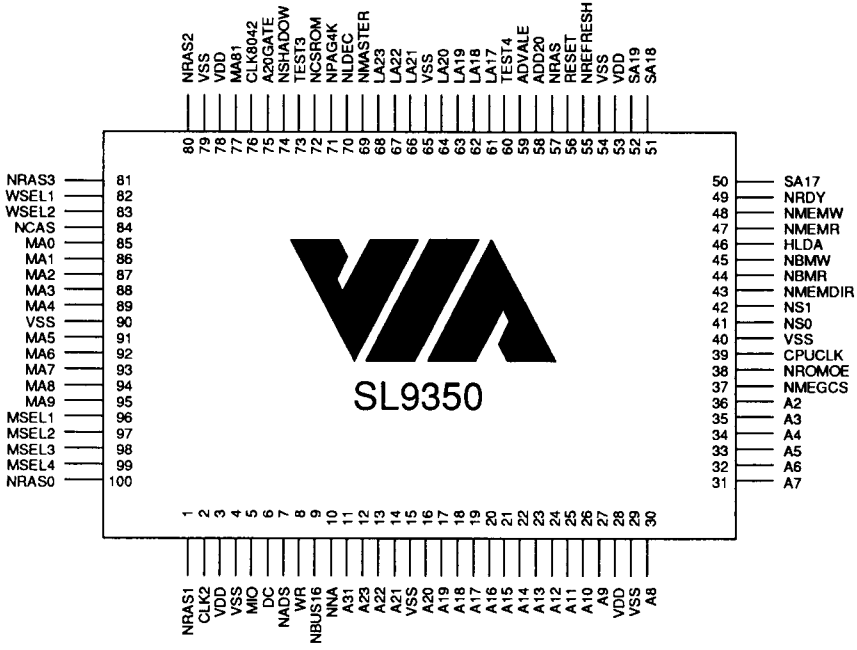
- Supports 80386DX based AT Designs.
- Up to 25 MHz Performance.
- Enhanced Fast Page Mode DRAM Controller.
- Supports 16 M byte of on Board Memory.
- Shadow RAM Feature.
- Programmable Wait State Options.
- Can use 256K or 1 Meg DRAMs or a mix.
- Supports 100 ns DRAMs at 16 MHz and 80 ns at 20 MHz.
- Selectable Wait State Option for Faster DRAMs.
- Switchable remapping of 640K - 1 M RAM to Top of the Address Space.
- Advanced CMOS Technology.
- 100 pin Flatpack.

DESCRIPTION

The SL9350 Memory Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

The SL9350 is part of the Personalized AT Logic chips that implements the Page Mode Memory Control functions which is specific to the 80386DX based PC/AT design and supports up to 25 MHz performance. Other members of the Personalized AT Logic chips include Page Interleave Memory Controller SL9151 and Page Mode Memory Controller SL9250 that are specific to 80286 and 80386SX-based PC/AT designs respectively.
It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

PINOUT


NRAS2 80
VSS 79
VDD 78
MA81 77
CLK8042 76
A20GATE 75
NSHADOW 74
TEST3 73
NCSROM 72
NPAG4K 71
NLDEC 70
NMASTER 69
LA23 68
LA22 67
LA21 66
VSS 65
LA20 64
LA19 63
LA18 62
LA17 61
TEST4 60
ADVALE 59
ADD20 58
NRAS 57
RESET 56
NREFRESH 55
VSS 54
VDD 53
SA19 52
SA18 51
NRAS3 81
WSEL1 82
WSEL2 83
NCAS 84
MA0 85
MA1 86
MA2 87
MA3 88
MA4 89
VSS 90
MA5 91
MA6 92
MA7 93
MA8 94
MA9 95
MSEL1 96
MSEL2 97
MSEL3 98
MSEL4 99
NRAS0 100
50 SA17
49 NRDY
48 NMEMW
47 NMEMR
46 HLDA
45 NBMW
44 NBMR
43 NMEMDIR
42 NS1
41 NS0
40 VSS
39 CPUCLK
38 NROMOE
37 NMEGCS
36 A2
35 A3
34 A4
33 A5
32 A6
31 A7
SL9350
1 NRAS1
2 CLK2
3 VDD
4 VSS
5 MIO
6 DC
7 NADS
8 WR
9 NBUS16
10 NNA
11 A31
12 A23
13 A22
14 A21
15 VSS
16 A20
17 A19
18 A18
19 A17
20 A16
21 A15
22 A14
23 A13
24 A12
25 A11
26 A10
27 A9
28 VDD
29 VSS
30 A8

ROM/RAM DECODE

The device provides all necessary circuitry to decode on board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column DRAMs.

The system can be configured for 512K Bytes to 16M Bytes. The bank selection code & sizes are as follows:

Msel4	Msel3	Msel2	Msel1	RAS0/CAS0	RAS1/CAS1	RAS2/CAS2	RAS3/CAS3	
0	0	0	0	0-640/1M-1M+384K				
0	0	0	1	0-640/2M-2M+384K	1M-2M			
0	0	1	0	0-640/3M-3M+384K	1M-2M	2M-3M		
0	0	1	1	0-640/4M-4M+384K	1M-2M	2M-3M	3M-4M	
0	1	0	0	0-640/1M-1M+384K				256K DRAMs
0	1	0	1	0-640/2M-2M+384K	1M-2M			1M DRAMs
0	1	1	0	0-640/6M-6M+384K	1M-2M	2M-6M		
0	1	1	1	0-640/10M-10M+384K	1M-2M	2M-6M	6M-10M	
1	1	0	0	0-640/1M-4M/4M-4M+384K				
1	1	0	1	0-640/1M-4M/8M-8M+384K	4M-8M			
1	1	1	0	0-640/1M-4M/12M-12M+384K	4M-8M	8M-12M		
1	1	1	1	0-640/1M-4M	4M-8M	8M-12M	12M-16M	

Table 1

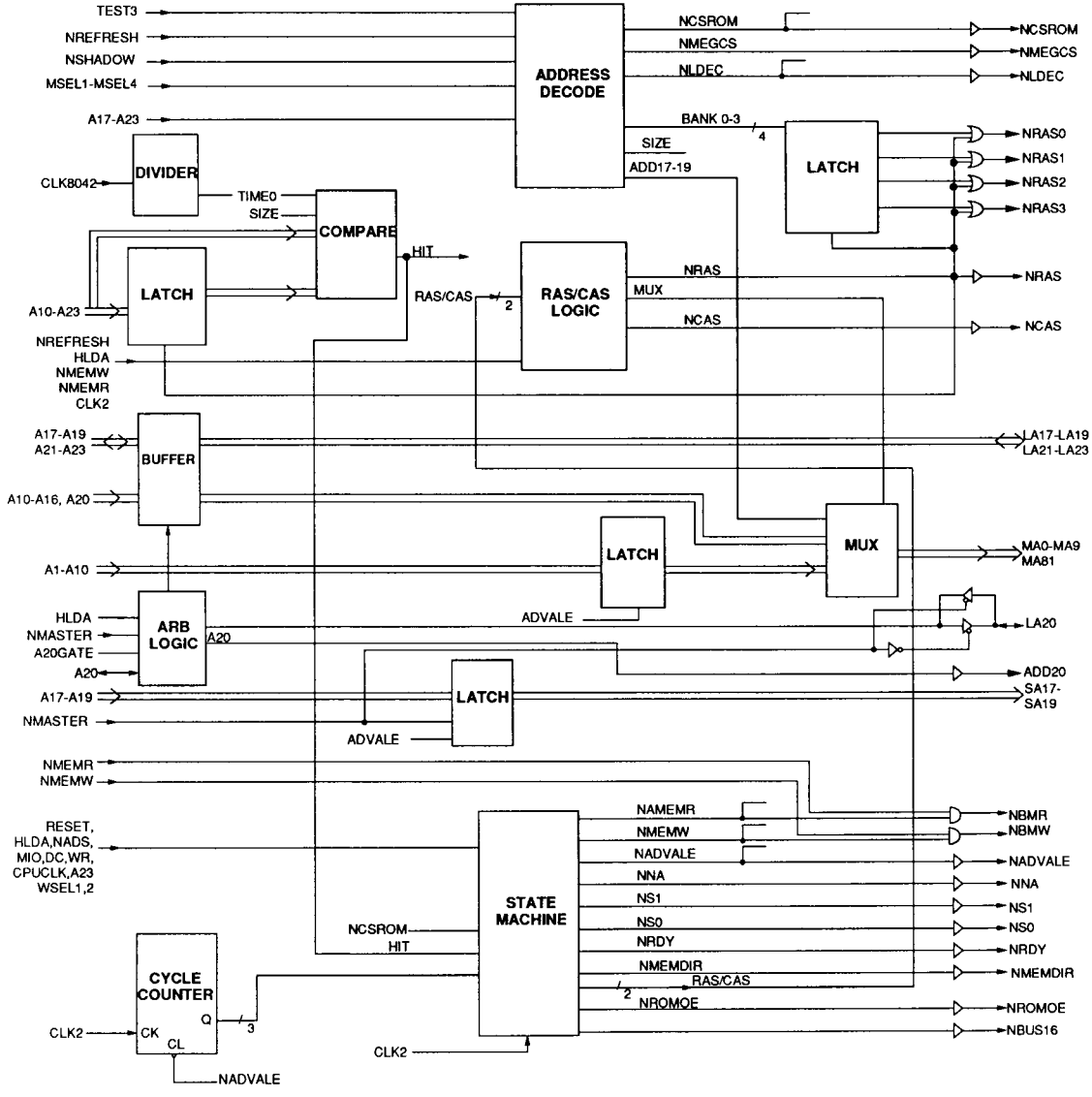
When Test3 input is tied low, the 384K Re-map to the top of the memory space is disabled.

Page is sized to 2KB if any 256K DRAMs are used and to 4KB if only 1M DRAMs are used, by tying NPAG4K High (256K) or Low (1Meg).

When CPU accesses the memory for the first time, the controller runs a one wait state memory cycle and asserts RAS & CAS low at appropriate times (Table 1). RAS is left low, CAS is returned high at the end of the cycle and the current row address is stored in an internal register. During all subsequent cycles, row addresses are compared with previous value stored in the register. If a match (hit) is detected, then the RAS is held low and CAS is strobed immediately after ADVALE goes low for read cycles, and for write cycles, CAS is asserted 1 CPUCLK later. If a mismatch (miss) is detected then RAS is pulled high for 3 CLK2 cycles before reasserting low, and new row address is stored in the row address register. The controller will now run a 1 or 2 wait state memory cycle depending on the switch setting WSEL1 and WSEL2 (Table 3).

CPU Addresses A11-A21, A31 are passed onto MA0-9 as unlatched row addresses whereas A2-A11 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. RAS, MUX, and CAS are separated by one CLK2 period as shown in the timing diagram. This latching of column addresses allows use of static column DRAMs as well.

BLOCK DIAGRAM SL9350



ROM/ RAM CONTROL (Cont'd.)

The SL9350 Memory Controller provides all the circuitry needed to generate RAM/ROM controls. RAM controls for Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS), RAM Read Write (NBMW, NBMR), Ready from 32 bit on board RAM read write (NRDY), next CPU address (NNA), and non on-board memory cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

MIO	DC	WR	ADDRESS	CYCLE TYPE
1	0	0		MEM CODE READ
1	0	1	2/0	HALT/SHUTDOWN
1	1	0		MEM DATA READ
1	1	1		MEM DATA WRITE
0	0	0		INTA
0	0	1		NOT POSSIBLE
0	1	0		I/O DATA READ
0	1	1		I/O DATA WRITE

Table 2

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 32 bit, on board, memory miss can be set using the following table.

CPU SPEED	WSEL1	WSEL2	WAIT STATES READ	WAIT STATES WRITE	MEMORY SPEED (ns)
16	0	0	2	2	-10
	1	0	2	1	-10*
	1	1	1	1	-8*
20	0	0	2	2	-8
	1	0	2	1	-8*
	1	1	1	1	-6*

* Page Mode CAS write time ≤ 1 CLK2 period.

Table 3

ROM controls NCSROM & NROMOE are asserted low at appropriate time when address 0E0000h-0FFFFFh (low) or FE0000h-FFFFFFh (high) is decoded during a memory cycle. The timing relationship is shown in the timing diagram. These will be disabled if Shadow RAM option is used. When Shadow RAM option is used by pulling NSHADOW pin low, the ROM code is copied in the corresponding RAM location by BIOS and the subsequent ROM code reads will be decoded as RAM reads and will be much faster. BIOS can be customized to activate this option at boot. The NSHADOW option affects the 128K region immediately below 1 Meg.

REFRESH SUPPORT

The SL9350 provides support for DRAM refresh. During refresh NRAS0-3 are asserted low, NCAS is inhibited high, the current bus state is ignored, and a refresh address generated by the SL9025 Address Controller is passed from A Bus to MA Bus.

BLOCK DIAGRAM SL9350

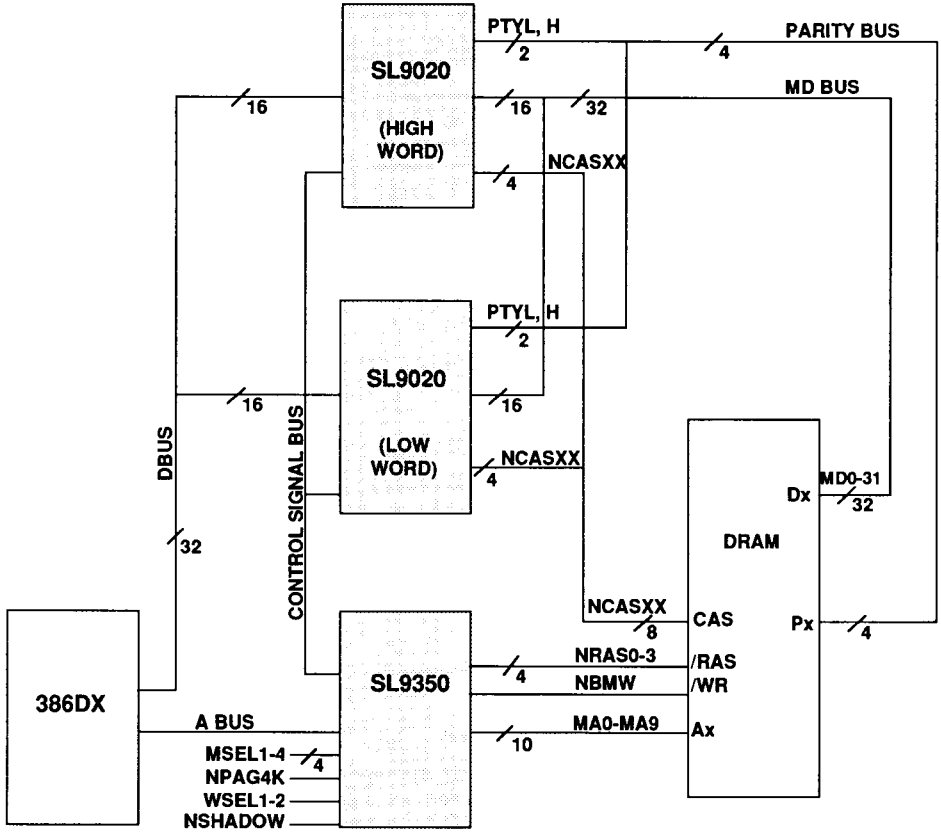


Fig. 1 386DX RAM BLOCK DIAGRAM

RAM

System RAM is added as shown in Fig. 1. 32 Bit memory data is connected to the MD Bus. Memory data flow is from/to the MD Bus and to/from Dbus via two each SL9020 (high word and low word) Data Controllers. Parity data is generated and checked in the SL9020 through parity byte bits PTYL and PTYH. The SL9020's output memory CAS strobes are: NCASA02, NCASA13, NCASB02, NCASB13.

RAM address is passed or latched internally in the SL9350 as necessary from A Bus to memory MA Bus (10 Bit). The MA Bus features 12ma drive capability. The SL9350 provides 24ma direct drive lines for memory RAS (NRAS0-NRAS3) as well as memory Write (NBMW). Eleven signals are output by the SL9350 to facilitate system control during RAM transfers. Their function and destination are covered in Table 4.

SIGNAL	DESTINATION	FUNCTION
ADVALE	SL9025 Address Controller	Used to latch the 386 address bus A1-A16 to the system address bus SA1-SA16.
	Internal	Used to latch the 386 address bus A17-A19 to the system address bus SA17-SA19. Transfers and latches 10 Bit CAS address (MA0-MA9) and NLDEC. Clears cycle counter.
NBMR	SL9025 Address Controller	Trailing edge used to latch parity error.
NBMW	SL9011 System Controller	Used to gate CPURST.
NCAS	SL9020 Data Controller	Used to gate SL9020 CAS output drivers: CASLA, CASLB, CASHA and CASHB. Trailing edge used to latch parity error.
NMEMDIR	SL9020 Data Controller	Sets MDBUS/DBUS direction. HI = D→MD
NLDEC	SL9011 System Controller	Indicates a local RAM/ROM decode.
MEGCS	SL9011 System Controller	Indicates a local RAM/ROM decode less than 1Meg address.
NRDY	SL9011 System Controller	Indicates the memory is ready with data.
NNA	386	Pipeline request to 386.
NS0-NS1	SL9011 System Controller	286 compatible status signal indicating a Read, Write, interrupt acknowledge or idle state.

Table 4. SL9350 Control Signal Function

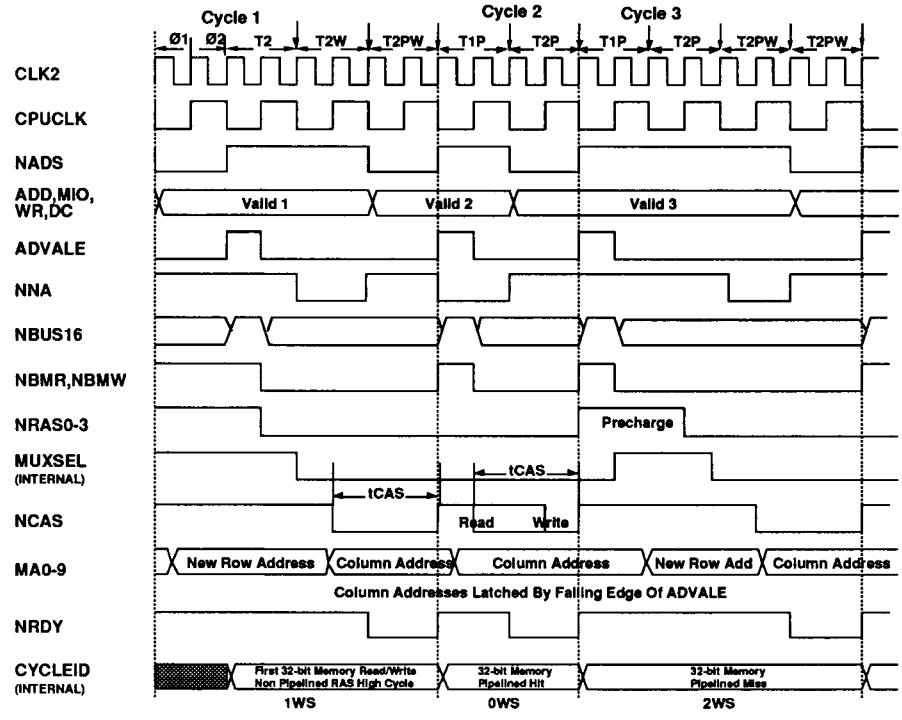


Fig. 2 32-Bit Memory (On Board) Timing Diagram

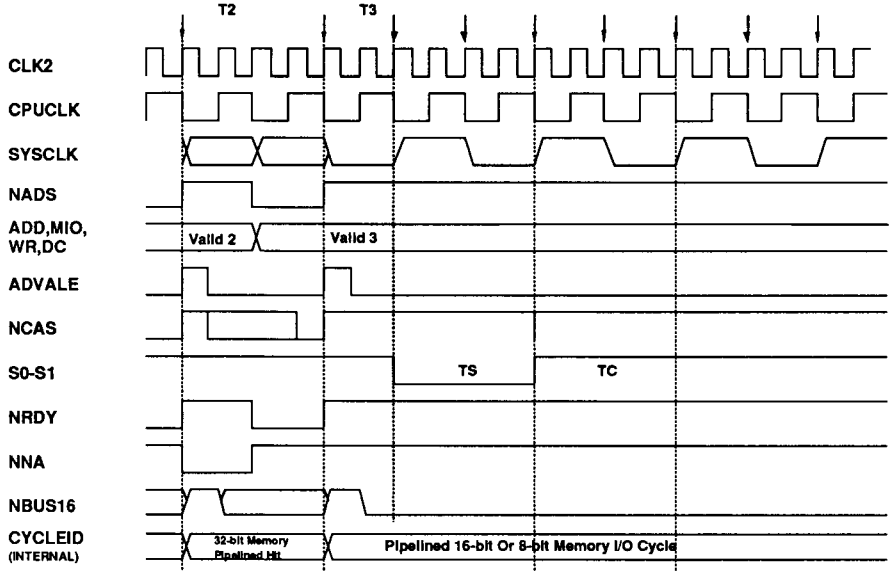


Fig. 3 Timing Diagram for Non 32-Bit Cycles

RAM (Cont'd)

A local memory cycle (cycle1 in Fig.2), begins during T1 when the 386 asserts NADS, MIO, and DC. SL9350 output NLDEC asserts, indicating a memory decode within the range specified by memory select jumpers Msel1-Msel4, as shown in Table 1. If the present address is within the lower 1 meg range, then MEGCS will also assert at this time. "ROW" addresses A11 through A20 are passed directly through the SL9350 into MA0-MA9. ADVALE is asserted during 01 (Phase 1, CPUCLK low) of T2. If the cycle is a Write, the start of T2 02 (Phase 2) brings NBMW valid, thus setting RAM WE. At this time, a RAS line will assert (NRAS0-NRAS3) strobing the MA0-MA9 address into the appropriate bank. ADVALE negates at 02, latching A1 through A10 in the SL9350. T2W 01 enables latched column address on MA0-MA9, and sets NNA to the 386 requesting the next cycle to be pipelined. T2W 02 asserts NCAS to the SL9020 Data Controllers, where the appropriate CAS line CASLA, LB, HA or HB is asserted, thus strobing the RAM column address and enabling RAM data output. NRDY to CPU (via SL9011) asserts at T2PW, signaling CPU to latch RAM data at end of T2PW 02. NADS also asserts, indicating a valid pipeline cycle in response to the previous NNA. T2WP 02 ends with CPUCLK dropping low, finishing the first cycle: NBMW, NCAS NRDY, and NADS negate, RAM data latches in the 386 CPU.

The next cycle, (cycle 2 in Fig. 3), T1P, asserts ADVALE, which enables a new column address on MA1-MA9. NNA is asserted, requesting the next cycle to be pipelined. AT T1P 02 advale negates, latching column addresses, asserts NBMR or NBMW as appropriate, and NCAS. NCAS assertion gives rise to the assertion of the appropriate RAM CAS line CASLA, LB, HA, or HB. T2P 01 negates NNA and asserts NRDY, signaling a page hit. The 386 asserts NADS indicating a new pipeline cycle. T2P 02 end latches RAM data in the 386 and negates NADS.

Cycle 3 begins in state T1P01 with NADS, NBMW, NRDY, NBUS, NNA NCAS and NRAS negated. ADVALE is asserted. Since NRAS is negated, a page miss is indicated. 02 negates ADVALE, asserts NBMW, and sets internal muxsel high. The mux is now driving a new row address on MA0-MA9. T2P 02 asserts the appropriate NRAS0-NRAS3 strobe, latching DRAM row address. T2P02 end drops internal muxsel, presenting as new column address on MA0-MA9. T2PW02 negates NCAS, thus strobing a new column address into DRAM and enabling DRAM output. The second wait state T2PW01 drops NRDY. Data for cycle 3 will then be latched in the CPU at the end of 02.

ROM

System ROM is enabled from 0E0000H to 0FFFFFH, or from FE0000H to FFFFFFH. 2 wait states are forced for any ROM access. If shadowing is selected, by asserting NSHADOW high on SL9350, then NROMOE and NCSROM signals are not asserted during the 386 Read cycle, and a RAM cycle is started instead.

System ROM is added as shown in Fig.4. 16 Bit ROM data out is connected to the MD Bus. 15 Bit ROM address input is connected directly to the 386 A Bus. Rom enable signals OE and CE are connected to the SL9350 output signals NROMOE and NCSROM. Data path is from MD Bus to 386D Bus via the SL9020 Data Controller. (Low word)

A Read cycle is started when the 386 asserts MIO, D/C and NADS. The "cycle" is latched internally on the rising edge of CLK2, when CPUCLK is high and a valid ROM address is on A17-A23 and A31. NCSROM is first asserted when a valid ROM address is decoded at T1A. When CPUCLK goes low and CLK2 rises high, (T2A), NBUS16 is asserted for the duration of CPUCLK low, indicating to the 386 a 16 bit cycle. Next CLK0, CPUCLK goes high and CLK2 rising high (T2B), NROMOE asserts, thus enabling ROM outputs. NMEMDIR asserts at this time, as well, signaling the SL9020 Data Controller to switch the memory data path from MDBus to DBus. After 2 wait states, on CLK2 rising high at T2W2B, NRDY asserts, signaling the SL9011 Controller that data is ready. The SL9011 drops NCPURDY, the CPU latches Bus data, and enters the second 16 Bit cycle by negating BE0, BE1, and NADS at T12 A. The second cycle repeats as the first. After the last ROM access, a valid ROM address will not be decoded and thus NCSROM, NRDMOE, and NMEMDIR will be negated in T1 A.

BLOCK DIAGRAM SL9350

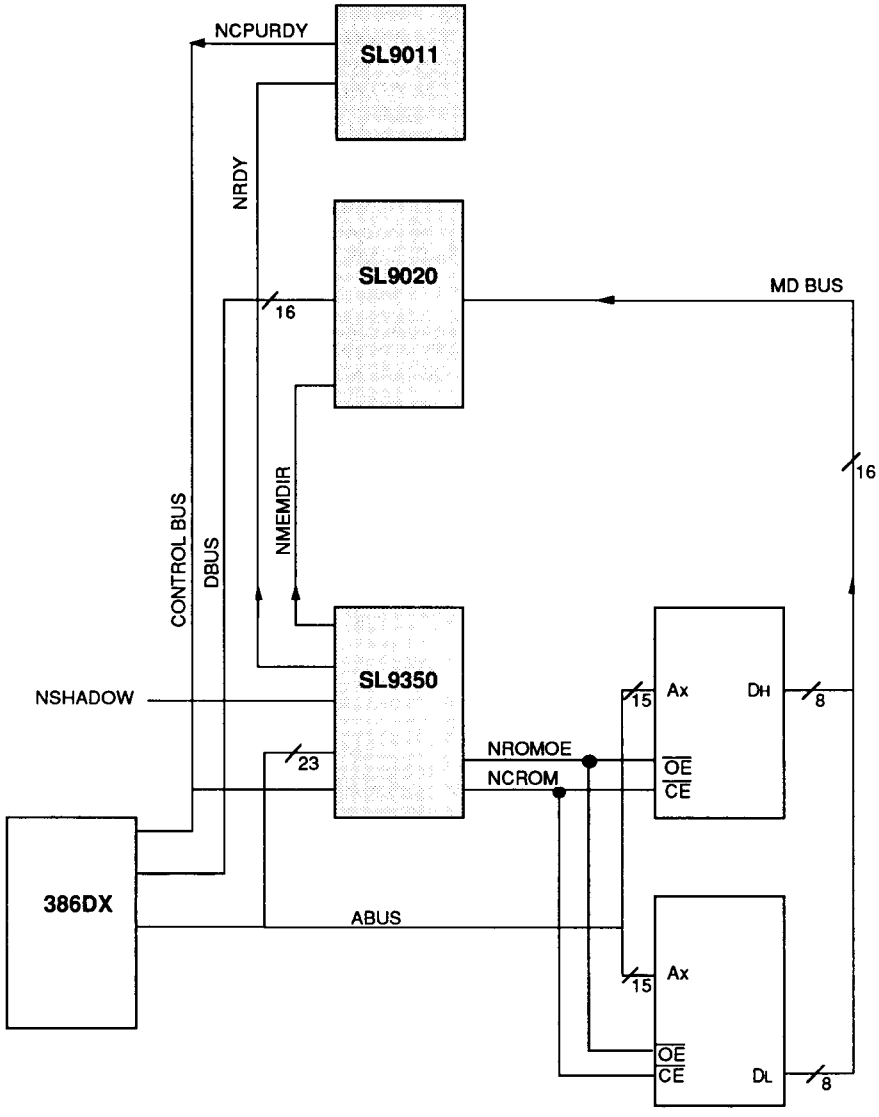


Fig. 4 386DX ROM BLOCK DIAGRAM

AC TIMING DIAGRAMS SL9350

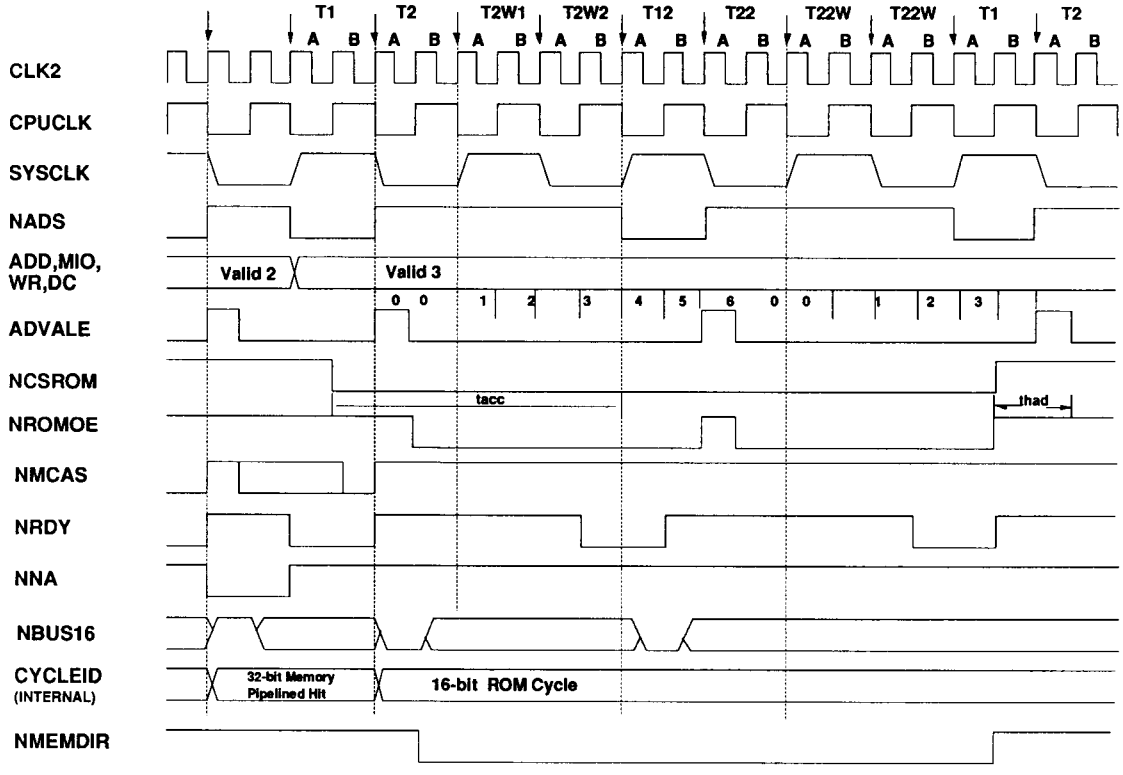


Fig. 5 Timing Diagram for BIOS ROM cycle (16-bit memory)

PIN DESCRIPTION SL9350

SYMBOL	PIN	TYPE	DESCRIPTION
A2-A16	36,35,34,33, 32,31,30,27, 26,25,24,23, 22,21,20	I	CPU Address Bus.
A17-A23	19,18,17,16, 14,13,12	I/O	CPU Address Bus.
A31	11	I/O	CPU Address Bus.
A20GATE	75	I	CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH.
ADD20	58	O	Decoded 20-bit address bit used to generate address decode for 1 M RAMs.
ADVALE	59	O	Advanced Address Latch Enable from memory controller. It latches local bus address for the system bus.
CLK2	2	I	Input Clock used to clock internal state machine. It is 2 times the frequency of the CPUCLK.
CLK8042	76	I	7 MHz clock input. It is used to internally generate a RAS time out. (Page mode.)
CPUCLK	39	I	Input Clock simulating 386 internal clock. It is CLK1 divided by two.
DC	6	I	CPU Status Signal. Differentiates between Data and Control instructions.
HLDA	46	I	CPU Output Signal, asserted to signal that the CPU has relinquished control of the bus to the device requesting MASTER or DMA. It is used to tri-state SLOT addresses during master.
LA17-LA23	61,62,63,64, 66,67,68	I/O	Local address bus. Directly drives AT-SLOT signals LA17-LA23.
MA0-MA9	85,86,87,88, 89,91,92,93, 94,95	O	RAM Address Bus Output. Directly drives DRAM address inputs.
MA81	77	O	RAM Address pin for 1M RAMs. Used in place of MA8 for 1M DRAMs.

PIN DESCRIPTION SL9350 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
MIO	5	I	CPU output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle. It is being used by the state machine to generate memory and I/O signals for the system.
MSEL1-4	96,97,98,99	I	On-board Fast RAM memory size and type select. They are set as indicated in Table 1. The setting will determine the appropriate RAS and CAS outputs. Internally pulled down.
NADS	7	I	CPU output control signal, asserted when Address Bus outputs are valid.
NBMR	44	O	Buffered Memory Read signal. Used to latch addresses in the SL9025 Address Controller chip.
NBMW	45	O	Buffered Memory Write signal. Used to directly drive DRAM write input.
NBUS16	9	O	CPU control input signal, Bus size 16. Activates 16-bit data bus operation; data is transferred on the lower 16 bits of the data bus and an extra cycle is provided for transfers of more than 16 bits.
NCSROM	72	O	LOW assert ROM Chip Select. Connects directly to system ROM CS.
NLDEC	70	O	Decode signal for on-board local HIGH-speed RAM. Indicates a local DRAM transfer is in process.
NMASTER	69	I	Asserted when an external device has control of the AT Bus at slot card output. Used to set address direction from SLOT to system.
NCAS	84	O	Memory column address strobe. Asserted when either CPU or DMA is accessing the memory. Used to drive SL9020 NCAS input.
NMEGCS	37	O	Select Decode for lower 1M of memory. Used to drive SL9011 NMEGCS input.
NMEMDIR	43	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is used to drive SL9020 NMEMDIR input.
NMEMR	47	I	Read Memory command from SL9011/SLOT.

PIN DESCRIPTION SL9350 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NMEMW	48	I	Write Memory command from SL9011/SLOT.
NNA	10	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
NPAG4K	71	I	Active LOW Page size = 4K option; when 1M DRAMs are used. Left HIGH for 256Ks or mixes.
NRAS	57	O	LOW assert Row address strobe. Not used in normal operation.
NRAS0-3	100,1,80,81	O	Row address strobes for Banks 0,1,2 & 3 for the on-board memory. Generated during CPU or DMA cycle for memory access. Used to directly drive DRAM RAS inputs.
NRDY	49	O	Asserted one clock cycle after NNA is asserted at the end of a local memory cycle. Used to signal SL9011 that data is ready.
NREFRESH	55	I	On-board RAM refresh signal. Generated from REFREQ input.
NROM0E	38	O	Enables ROM output during ROM read cycles. Connects directly to ROMOE pin.
NS0,1	41,42	O	80286 compatible status signals for the AT System Controller SL9011.
NSHADOW	74	I	Selectable option for Shadow RAMs. LOW enables Shadow RAM feature.
RESET	56	I	Active HIGH Reset from system controller.
SA17-19	50,51,52	O	System Address Bus.
TEST3	73	I	Optional disable for 684K - 1M [384K] remap.
TEST4	60	I	Test Pin - Not connected.
VDD	3,28,53,78	-	+5V. Power.
VSS	4,15,29,40, 54,65,79,90	-	0V. Ground.
WR	8	I	CPU output control signal Write.
WSEL1,2	82,83	I	Wait-state Select options. Refer to Table 3 for proper setting. Internally pulled up.

AC TIMING DIAGRAMS SL9350

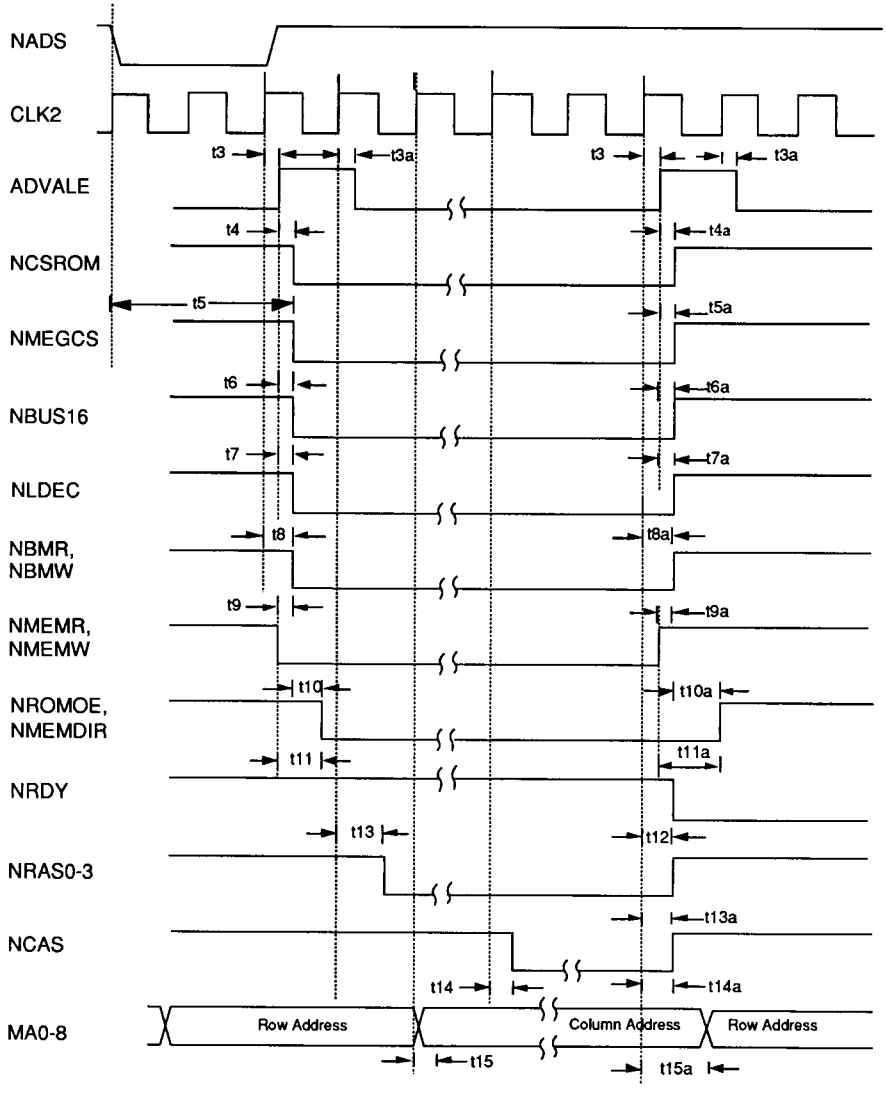


Fig. 6 Set-up and Hold Times

ABSOLUT MAXIMUM RATINGS SL9350 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current *note 2	I_{OS}	-40	+40	mA
Output Current *note 3	I_{OS}	-40	+80	mA
Output Current *note 4	I_{OS}	-60	+120	mA
Output Current *note 5	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. ADVALE, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NNA, NRDY, NROMOE, NS0, NS1.
3. A17 - A23, A31.
4. ADD20, MA0-MA9, MA81, LA17 - LA23, NRAS, SA17 - SA19.
5. NBMW, NRAS0 - NRAS3.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9350

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	CONDITIONS
Power Supply Current	IDDS	TBD	TBD	mA	20 MHz
Power Supply Current	IDDS	0	100	µA	Steady state
Output High Voltage *note 1	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output *note 2	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output NBMW, NRAS0-NRAS3	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output *note 3	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output A17-A23, A31	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output *note 4	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output NBMW, NRAS0-NRAS3	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for All Inputs	VIH	2.2		V	
Input Low Voltage for All Inputs	VIL		0.8	V	
Input Leakage Current *note 5	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current, Tristate *note 6	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = Vss
Input Current, Pull-up *note 7	IILU	-33.5	-204	µA	VI = .4V
Input Current, Pull-up *note 8	IIHU	-13.5	-124	µA	VI = 2.4V
Input Current, Pull-down MSEL1-MSEL4	IILD	4	26	µA	VI = .4V
Input Current, Pull-down MSEL1-MSEL4	IIHD	14	106	µA	VI = 2.4V

NOTES:
1. ADVALE, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1, A17-A23, A31
2. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
3. ADVALE, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1
4. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
5. A2-A16, A20 GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, NREFRESH, RESET, WR
6. A17-A23, A31, LA17-LA23, SA17-SA19
7. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2
8. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2

AC CHARACTERISTICS SL9350

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	CLK2 Period	25	-	ns
t2	CLK2 High Duration	7	-	ns
t2a	CLK2 Low Duration	7	-	ns
t3	CLK2 to ADVALE (Low to High)	5	20	ns
t3a	CLK2 to ADVALE (High to Low)	5	20	ns
t4	ADVALE to NCSROM (High to Low)	5	15	ns
t4a	ADVALE to NCSROM (Low to High)	5	15	ns
t5	NADS to NMEGCS (High to Low)	5	15	ns
t5a	NADS to NMEGCS (Low to High)	5	15	ns
t6	ADVALE to NBUS16 (High to Low)	5	15	ns
t6a	ADVALE to NBUS16(Low to High)	5	15	ns
t7	ADVALE to NLDEC (High to Low)	5	15	ns
t7a	ADVALE to NLDEC (Low to High)	5	15	ns
t8	CLK2 to NBMR, NBMW (High to Low)	5	12	ns
t8a	CLK2 to NBMR, NBMW (Low to High)	5	12	ns
t9	NMEMR, NMEMW to NBMR, NBMW (High to Low)	5	10	ns
t9a	NMEMR,NMEMW to NBMR, NBMW (Low to High)	5	10	ns
t10	NBMR to NROMOE (High to Low)	0	12	ns
t10a	NBMR to NROMOE (Low to High)	0	12	ns
t11	NMEMR to NROMOE (High to Low)	5	15	ns
t11a	NMEMR to NROMOE (Low to High)	5	15	ns
t12	CLK2 to NRDY	5	12	ns
t13	CLK2 to NRAS0-NRAS3 (High to Low)	5	12	ns
t13a	CLK2 to NRAS0-NRAS3 (Low to High)	5	12	ns
t14	CLK2 to NCAS (High to Low)	5	12	ns
t14a	CLK2 to NCAS (Low to High)	5	12	ns
t15	CLK2 to MA0-MA8 Delay	5	15	ns

(TA = 25 ° C, VDD = V1 = 5V, fo = 1MHz)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	NOTES
Input Pin Capacitance	CIN	---	16	Pf	note 1
Input Pin Capacitance	CIN	---	TBD	Pf	note 2
Output Pin Capacitance	COUT	---	16	Pf	note 3
Output Pin Capacitance	COUT	---	18	Pf	note 4
I/O Pin Capacitance	CI/O	---	16	Pf	note 5
I/O Pin Capacitance	CI/O	---	23	Pf	note 6

NOTES:
1. A2-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, REFRESH, RESET, WR
2. NSHADOW, MSEL1-MSEL4, NPAG4K, TEST 3, TEST 4, WSEL1, WSEL2
3. ADVALE, ADD20, MA0-MA9, MA81, NBMR, NBUS16, NCSROM, NLDEC, NMEGCS, NMEMDIR, NNA, NRDY, NRAS, NROMOE, NS0, NS1
4. NBMW, NRAS0-NRAS3
5. A17-A23, A31, LA17-LA23, SA17-SA19
6. NBMW, NRAS0-NRAS3