FEATURES

- Supports 80386SX based AT Designs.
- Up to 25 MHz Performance.
- Enhanced Fast Page Mode/Page Interleave.
- Supports 8 M bytes of on Board Memory.
- Shadow RAM Feature
  - 16K granularity
  - 8 remap options
  - System, video, LAN BIOS
- Programmable Memory Options
  - ROM chip select in 16K granularity
  - Wait states for 16 Bit ROM
  - Hit wait states (0-3)
  - Miss wait states (1-4)
  - RAS and CAS precharge
- Programmable Memory Partitioning
  - Disable (on board) memory to 0K in 128K resolution
  - 512 X 512 split
  - Memory backfill
- Can use 256K x 1, 1 M x 1 and 256K x 4 DRAMs or a mix.
- Staggered RAS Refresh.
- Supports Pipeline and Non-Pipeline Modes.
- Fast Gate A20 and Fast Reset.
- Backward Compatible to SL9250.
- Advanced, Low Power CMOS Technology for Laptops.
- 100 pin Flatpack.

DESCRIPTION

The SL9251 Memory Controller supports PC/AT systems based on Intel's 80386SX microprocessor. It is a member of VIA's FlexSet family which utilizes the same core logic across the entire PC/AT spectrum. The SL9251 is backward compatible with existing memory controllers for the 80386SX (SL9250). Boards designed using the SL9250 can be used with the new SL9251 without modifications and with existing BIOS. In order to take advantage of the SL9251's many new programmable features, minor board modification and a modified BIOS is required for enhanced performance.

The SL9251 offers the advanced memory control functions and features needed to develop high performance PC/AT systems without using external TTL Logic. The SL9251 supports two-way and 4-way page interleave mode for 80386SX based designs. The Page interleave option can be enabled or disabled using the configuration registers. All memory banks which are interleaved use the same type of memory. Designers can enable the staggered RAS option during refresh, which minimizes power surge. Both pipeline and non-pipeline modes are supported by enabling or disabling the next address controls, and providing ready at the correct time.

RAM & ROM OPTIONS

The programmable RAM options supported by the SL9251, offer a very high level of design flexibility to the PC/AT system designer. DRAM page 'HIT' wait states are programmable from 0 to 3, and the DRAM page 'MISS' wait states are programmable from 1 to 4. This allows systems designers to design PC/AT systems capable of handling a wide range of DRAM speeds with wide variety of CPU speeds including 33 MHz Cache based systems. The 'MISS' wait states for write operation can be programmed to one less than the Read cycle. A minimum of one wait state is forced if a 'MISS' cycle is detected. The RAS precharge time is also programmable, typically a multiple of the CLK2 (2 to 5). Start of CAS can be independently programmed for HIT, read MISS and write MISS cycles. RAS to address is programmable in steps and 1/2 CLK2 increments.

In addition to the RAM, programming options for ROM are also supported. ROM chip select is programmable in 16K granularity. For ROM, 1 to 10 programmable wait states are supported.

REMAP

In order to enhance the system and video performance, the SL9251 has been designed to support advanced shadow RAM features. The memory address space from '00A0000' to 00FFFFF' can be shadowed in 16K granularity, for system, video, LAN and other types of BIOS. This memory space is write protected in 16K granularity. The chip also supports Read/Write for local RAM using the 'backfill' option. By disabling the local RAM, the SL9251 allows system designers to Read and Write to the system bus. The local memory from 0 to 640K can be disabled with 128K granularity. The SL9251 offers many memory remap options which are listed in Table 1.

DESCRIPTION (cont'd.)

Table 1. Remap Options

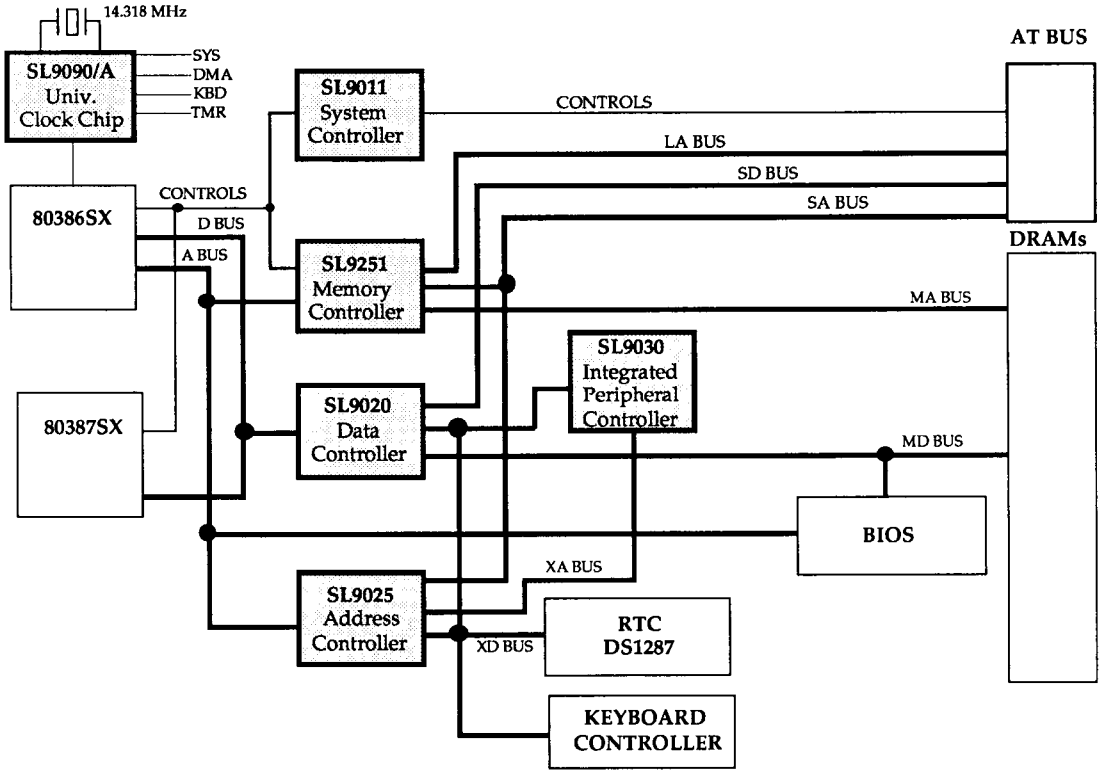
NO REMAP
512K (512 X 512 SPLIT)
128K (384K - 256K (SYSROM + ALL OPTION ROM)
256K (384K - 128K LOCAL ROM)
288K (384K - LOCAL SYS ROM + VIDEO ROM)
320K (384K - 64K LOCAL ROM)
352K (384K - 32K LOCAL ROM)
384K REMAPPED FULLY. (NO SHADOW)

ADDITIONAL FEATURES

OS/2 performance is enhanced significantly by using the Fast GATEA20 and Fast CPU Reset features offered by the SL9251. Port 92, defined in the IBM PS/2 technical manual, is used to provide faster performance.

Configuration registers are used to program these features during the system set up.

The SL9251 is available in a 100 pin plastic flat pack. It has been designed using advanced 1.2 micron double layer metal CMOS technology.



FlexAT/386SX System Block Diagram