SL9250 80386SX Page Mode Memory Controller

FEATURES

- Supports 80386SX based AT Designs.

- Up to 20 MHz Performance.

- Enhanced Fast Page Mode DRAM Controller.

- Supports 8 M byte of On-Board Memory.

- Shadow RAM Feature.

- Programmable Wait State Options.

- Can use 256K or 1 Meg DRAMs or a mix.

- Supports 100 ns DRAMs at 16 MHz and 80 ns at 20 MHz.

- Selectable Wait State Option for Faster DRAMs.

- Switchable remapping of 640K - 1 M RAM to the Top of the Address Space.

- Advanced CMOS Technology.
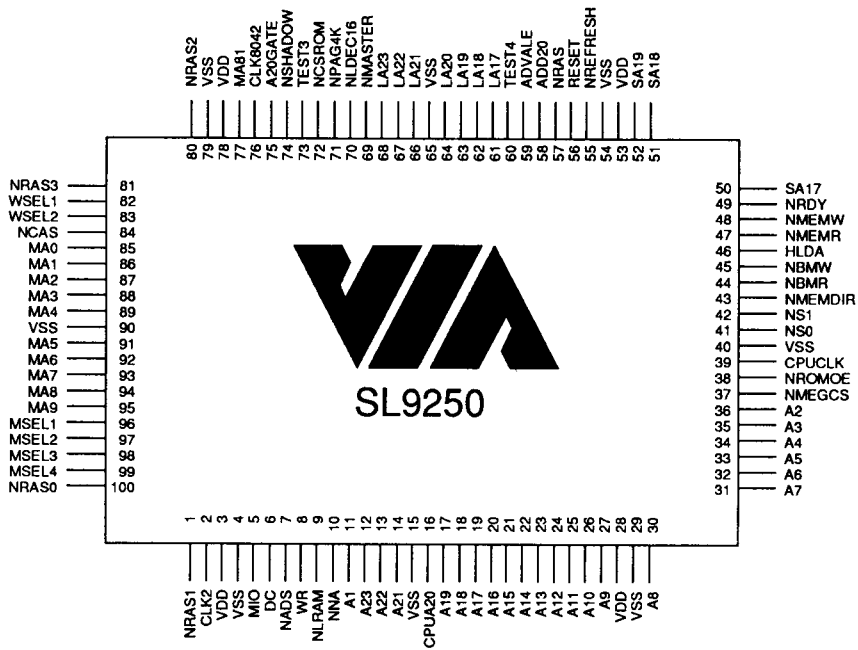
- 100 pin Flatpack.

DESCRIPTION

The SL9250 Memory Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

The SL9250 is part of the Personalized AT Logic chipset that implements the Page Mode Memory Control functions which is specific to the 80386SX based PC/AT design and supports up to 20 MHz performance. Other members of the Personalized AT Logic chips include the SL9151 Page Interleave Memory Controller and the SL9350 Page Mode Memory Controller that are specific to 80286 and 80386DX-based PC/AT designs respectively.

It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

PINOUT

```
                              N V V M C A N T N N N L L L V L L L L T A A N R N V V S S
                              R S D A L 2 S E C P L A A A S A A A E D D R E E S D A A
                              A S D 8 K 0 H S P A D 2 2 2 S 2 2 1 S V D M S E D 1 1 1
                              S   1 8 G T S T S G E 3 2 1   0 9 8 T A 2 E F   9 8
                              2     0 A A O 3 R O 4 C       1     4 L 0 T R     S
                                      4 T D   O M 1         1     E E   E E     S
                                      2 E W     M 6               6 0   T S
                                                                          H

                              80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51

         NRAS3 ─── 81                                                                                    50 ─── SA17
         WSEL1 ─── 82                                                                                    49 ─── NRDY
         WSEL2 ─── 83                                                                                    48 ─── NMEMW
          NCAS ─── 84                                                                                    47 ─── NMEMR
           MA0 ─── 85                                                                                    46 ─── HLDA
           MA1 ─── 86                                                                                    45 ─── NBMW
           MA2 ─── 87                                                                                    44 ─── NBMR
           MA3 ─── 88                                                                                    43 ─── NMEMDIR
           MA4 ─── 89              ███████ SL9250 ███████                                                42 ─── NS1
           VSS ─── 90                                                                                    41 ─── NS0
           MA5 ─── 91                                                                                    40 ─── VSS
           MA6 ─── 92                                                                                    39 ─── CPUCLK
           MA7 ─── 93                                                                                    38 ─── NROMOE
           MA8 ─── 94                        SL9250                                                      37 ─── NMEGCS
           MA9 ─── 95                                                                                    36 ─── A2
         MSEL1 ─── 96                                                                                    35 ─── A3
         MSEL2 ─── 97                                                                                    34 ─── A4
         MSEL3 ─── 98                                                                                    33 ─── A5
         MSEL4 ─── 99                                                                                    32 ─── A6
         NRAS0 ─── 100                                                                                   31 ─── A7

                              1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

                              N C V V M D W N N A A A A V C A A A A A A A A A A A A A V V A
                              R L D S I C R L N 1 2 2 2 S P 1 1 1 1 1 1 1 1 1 1 1 1 0 D S 8
                              A K D S O   R R A   3 2 1 S U 9 8 7 6 5 4 3 2 1 0     D S
                              S 2           A N     0     A         0             S
                              1             M M     2                 9
                                                        0
```

ROM /RAM DECODE

The device provides all necessary circuitry to decode on-board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column DRAMs.

The system can be configured for 512K Bytes to 16M Bytes. The bank selection code & sizes are as follows:

Msel4	Msel3	Msel2	Msel1	RAS0/CAS0	RAS1/CAS1	RAS2/CAS2	RAS3/CAS3	
0	0	0	0	0-640/1M-1M+384K				
0	0	0	1	0-640/2M-2M+384K	1M-2M			
0	0	1	0	0-640/3M-3M+384K	1M-2M	2M-3M		
0	0	1	1	0-640/4M-4M+384K	1M-2M	2M-3M	3M-4M	
0	1	0	0	0-640/1M-1M+384K				256K DRAMs
0	1	0	1	0-640/2M-2M+384K	1M-2M			1M DRAMS
0	1	1	0	0-640/6M-6M+384K	1M-2M	2M-6M		
0	1	1	1	0-640/10M-10M+384K	1M-2M	2M-6M	6M-10M	
1	1	0	0	0-640/1M-4M/4M-4M+384K				
1	1	0	1	0-640/1M-4M/8M-8M+384K	4M-8M			
1	1	1	0	0-640/1M-4M/12M-12M+384K	4M-8M	8M-12M		
1	1	1	1	0-640/1M-4M	4M-8M	8M-12M	12M-16M	

Table 1

When Test3 input is tied low, the 384K Re-map to the top of the memory space is disabled.

The page size is 2KB if any 256K DRAMs are used and 4KB if only 1M DRAMs are used, by tying NPAG4K High (256K) or Low (1Meg).

When CPU accesses the memory for the first time, the controller runs a one wait state memory cycle and asserts RAS & CAS low at appropriate times (Table 1). RAS is kept asserted while the CAS is deasserted at the end of the cycle and the current row address is stored in an internal register. During all subsequent cycles, row addresses are compared with the previous value stored in the register. If a match (hit) is detected, the RAS is held low and CAS is strobed immediately after ADVALE goes low for read cycles, and for write cycles, CAS is asserted 1 CPUCLK later. If a mismatch (miss) is detected then RAS is pulled high for 3 CLK2 cycles before being reasserted and new row address is stored in the row address register. The controller will now run a 1 or 2 wait state memory cycle depending on the switch setting WSEL1 and WSEL2 (Table 3).

CPU Addresses A11-A21 and A1 are passed onto MA0-9 as unlatched row addresses whereas A2-A11 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. RAS, MUX, and CAS are separated by one CLK2 period as shown in the timing diagram. This latching of column addresses allows use of static column DRAMs as well.

BLOCK DIAGRAM SL9250
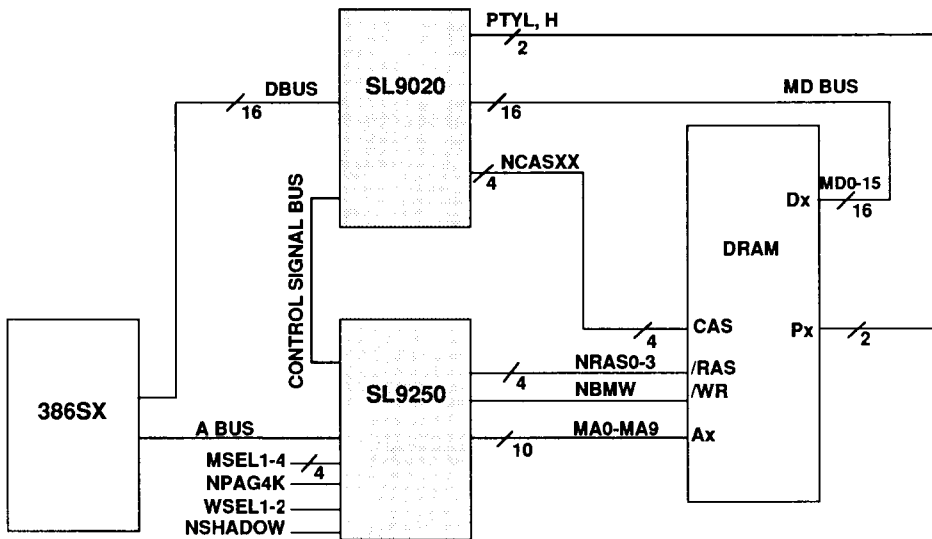
Fig. 1 386SX RAM BLOCK DIAGRAM

ROM/ RAM CONTROL (Cont'd.)

The SL9250 Memory Controller provides all the circuitry needed to generate RAM/ROM controls. RAM controls for Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS), RAM Read Write (NBMW, NBMR), Ready from 16 bit on board RAM read write (NRDY), next CPU address (NNA), and non on-board memory cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

MIO	DC	WR	ADDRESS	CYCLE TYPE
1	0	0		MEM CODE READ
1	0	1	2/0	HALT/SHUTDOWN
1	1	0		MEM DATA READ
1	1	1		MEM DATA WRITE
0	0	0		INTA
0	0	1		NOT POSSIBLE
0	1	0		I/O DATA READ
0	1	1		I/O DATA WRITE

Table 2

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 16 bit, on board, memory miss can be set using the following table.

CPU SPEED	WSEL1	WSEL2	WAIT STATES READ	WRITE	MEMORY SPEED (ns)
16	0	0	2	2	-10
	1	0	2	1	-10*
	1	1	1	1	-8*
20	0	0	2	2	-8
	1	0	2	1	-8*
	1	1	1	1	-6*

* Page Mode CAS write time ≤ 1 CLK2 period.

Table 3

ROM controls NCSROM & NROMOE are asserted low at appropriate time when address 0E0000h-0FFFFFh (low) or FE0000h-FFFFFFh (high) is decoded during a memory cycle. The timing relationship is shown in the timing diagram. These will be disabled if Shadow RAM option is used. When Shadow RAM option is used by pulling NSHADOW pin low, the ROM code is copied in the corresponding RAM location by BIOS, and the subsequent ROM code reads will be decoded as RAM reads & will be much faster. BIOS can be customized to activate this option at boot. The NSHADOW option affects the 128K region immediately below 1 Meg.

REFRESH SUPPORT

The SL9250 provides support for DRAM refresh. During refresh NRAS0-3 are asserted low, NCAS is inhibited high, the current bus state is ignored, and a refresh address generated by the SL9025 Address Controller is passed from A Bus to MA Bus.

BLOCK DIAGRAM SL9250

TEST3 → ADDRESS DECODE

NREFRESH →

NSHADOW →

MSEL1-MSEL4 →

A1, A17-A19, A21-A23, CPUA20 →

CLK8042 → DIVIDER

TIME0

SIZE

A10-A19 A21-A23 CPUA20 → LATCH

COMPARE → HIT

NREFRESH HLDA NMEMW NMEMR CLK2

RAS/CAS → RAS/CAS LOGIC

2

A17-A19 A21-A23 → BUFFER

A10-A16, A20 →

A1-A10 →

HLDA NMASTER A20GATE CPUA20 → ARB LOGIC

A20

A17-A19 →

NMASTER →

ADVALE

NMEMR →
NMEMW →

RESET, HLDA,NADS, MIO,DC,WR, CPUCLK,A23 WSEL1,2 →

NCSROM →

HIT →

CLK2 → CK Q CYCLE COUNTER CL

3

NADVALE

CLK2 →

STATE MACHINE

LATCH

LATCH

MUX

LATCH

ADDRESS DECODE outputs:
NCSROM → NCSROM
NMEGCS → NMEGCS
NLDEC16 → NLDEC16
→ NLRAM
BANK 0-3   4
SIZE
ADD17-19

LATCH → NRAS0
NRAS1
NRAS2
NRAS3

NRAS
MUX → NRAS
NCAS → NCAS

LA17-LA19
LA21-LA23

MA0-MA9
MA8I

LA20
ADD20
SA17-SA19

NAMEMR → NBMR
NMEMW → NBMW
NADVALE → NADVALE
NNA → NNA
NS1 → NS1
NS0 → NS0
NRDY → NRDY
NMEMDIR → NMEMDIR
RAS/CAS   2
NROMOE → NROMOE

RAM

System RAM is added as shown in Fig. 1. 16 Bit memory data is connected to the MD Bus. Memory data flow is from/to the MD Bus and to/from Dbus via the SL9020 Data Controller. Parity data is generated and checked in the SL9020 through parity byte bits PTYL and PTYH. The SL9020's output memory CAS strobes are: NCASA02, NCASA13, NCASB02, NCASB13.

RAM address is passed or latched internally in the SL9250 as necessary from A Bus to memory MA Bus (10 Bit). The MA Bus features 12ma drive capability. The SL9250 provides 24ma direct drive lines for memory RAS (NRAS0-NRAS3) as well as memory Write (NBMW). Eleven signals are output by the SL9250 to facilitate system control during RAM transfers. Their function and destination are covered in Table 4.

SIGNAL	DESTINATION	FUNCTION
ADVALE	SL9025 Address Controller	Used to latch the 386SX address bus A1-A16 to the system address bus SA1-SA16.
	Internal	Used to latch the 386SX address bus A17-A19 to the system address bus SA17-SA19. Transfers and latches 10 Bit CAS address (MA0-MA9) and NLDEC16. Clears cycle counter.
NBMR	SL9025 Address Controller	Trailing edge used to latch parity error.
NBMW	SL9011 System Controller	Used to gate CPURST and drive WE for RAM.
NCAS	SL9020 Data Controller	Used to gate SL9020 CAS output drivers: CASLA, CASLB, CASHA and CASHB. Trailing edge used to latch parity error.
NMEMDIR	SL9020 Data Controller	Sets MDBUS/DBUS direction. HI = D→MD
NLDEC16	SL9011 System Controller	Indicates a local RAM/ROM decode.
MEGCS	SL9011 System Controller	Indicates a local RAM/ROM decode less than 1Meg address.
NRDY	SL9011 System Controller	Indicates the memory is ready with data.
NNA	386SX	Pipeline request to 386SX.
NS0-NS1	SL9011 System Controller	286 compatible status signal indicating a Read, Write, interrupt acknowledge or idle state.

Table 4. SL9250 Control Signal Function
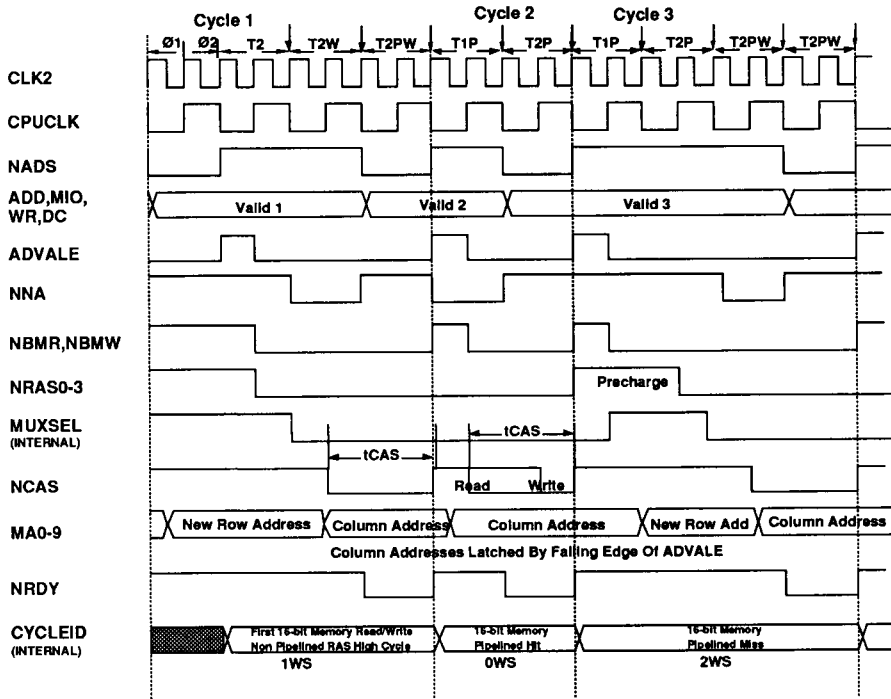
Fig. 2 On-Board Memory Timing Diagram
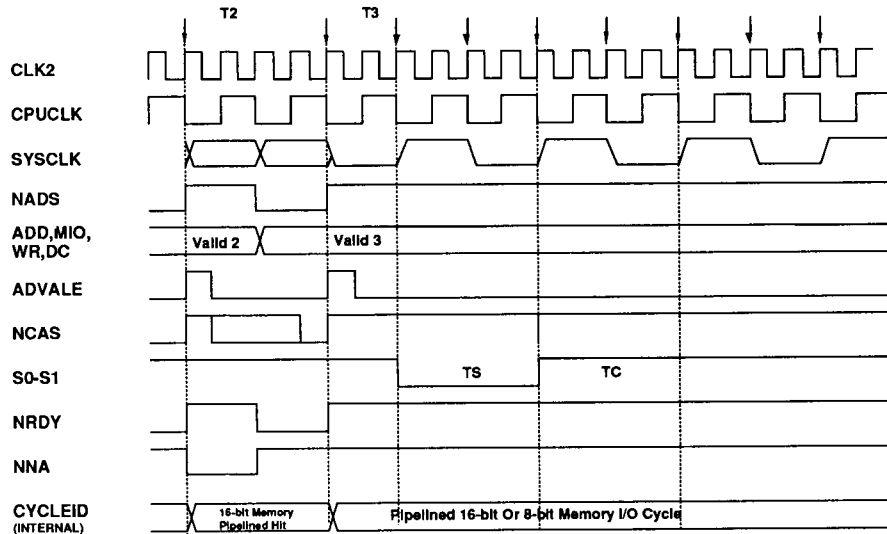
Fig. 3 Off-Board Memory Timing Diagram

RAM (Cont'd)

A local memory cycle (cycle1 in Fig.2), begins during T1 when the 386SX asserts NADS, MIO, and DC. SL9250 output NLDEC16 asserts, indicating a memory decode within the range specified by memory select jumpers MSEL1-MSEL4, as shown in Table 1. If the present address is within the lower 1 meg range, then MEGCS will also assert at this time. "ROW" addresses A11-A19 and CPUA20 are passed directly through the SL9250 into MA0-MA9. ADVALE is asserted during 01 (Phase 1, CPUCLK low) of T2. If the cycle is a Write, the start of T2 02 (Phase 2) brings NBMW valid, thus setting RAM WE. At this time, a RAS line will assert (NRAS0-NRAS3) strobing the MA0-MA9 address into the appropriate bank. ADVALE negates at 02, latching A1 through A10 in the SL9250. T2W 01 enables latched column address on MA0-MA9, and sets NNA to the 386SX requesting the next cycle to be pipelined. T2W 02 asserts NCAS to the SL9020 Data Controller, where the appropriate CAS line CASLA, LB, HA or HB is asserted, thus strobing the RAM column address and enabling RAM data output. NRDY to CPU (via SL9011) asserts at T2PW, signaling CPU to latch RAM data at end of T2PW 02. NADS also asserts, indicating a valid pipeline cycle in response to the previous NNA. T2WP 02 ends with CPUCLK dropping low, finishing the first cycle: NBMW, NCAS, NRDY and NADS negate, RAM data latches in the 386SX CPU.

The next cycle, (cycle 2 in Fig. 3), T1P, asserts ADVALE, which enables a new column address on MA1-MA9. NNA is asserted, requesting the next cycle to be pipelined. AT T1P 02 advale negates, latching column addresses, asserts NBMR or NBMW as appropriate, and NCAS. NCAS assertion gives rise to the assertion of the appropriate RAM CAS line CASLA, LB, HA, or HB. T2P 01 negates NNA and asserts NRDY, signaling a page hit. The 386SX asserts NADS indicating a new pipeline cycle. T2P 02 end latches RAM data in the 386SX and negates NADS.

Cycle 3 begins in state T1P01 with NADS, NBMW, NRDY, NBUS, NNA NCAS and NRAS negated. ADVALE is asserted. Since NRAS is negated, a page miss is indicated. 02 negates ADVALE, asserts NBMW, and sets internal muxsel high. The mux is now driving a new row address on MA0-MA9. T2P 02 asserts the appropriate NRAS0-NRAS3 strobe, latching DRAM row address. T2P02 end drops internal muxsel, presenting as new column address on MA0-MA9. T2PW02 negates NCAS, thus strobing a new column address into DRAM and enabling DRAM output. The second wait state T2PW01 asserts NRDY. Data for cycle 3 will then be latched in the CPU at the end of 02.

ROM

System ROM is enabled from 0E0000H to 0FFFFFH, or from FE0000H to FFFFFFH. Two wait states are forced for any ROM access. If shadowing is selected, by asserting NSHADOW high on SL9250, NROMOE and NCSROM signals are not asserted during the 386SX Read cycle and a RAM cycle is started instead.

System ROM is added as shown in Fig.4. 16 Bit ROM data out is connected to the MD Bus. 15 Bit ROM address input is connected directly to the 386SX A Bus. ROM enable signals OE and CE are connected to the SL9250 output signals NROMOE and NCSROM. Data path is from MD Bus to 386SX D Bus via the SL9020 Data Controller.

A Read cycle is started when the 386SX asserts MIO, D/C and NADS. The "cycle" is latched internally on the rising edge of CLK2, when CPUCLK is high and a valid ROM address is on A1, A17-A19, A21-A23, and CPUA20. NCSROM is first asserted when a valid ROM address is decoded at T1A. When CPUCLK goes low and CLK2 rises high, (T2A), NBUS16 is asserted for the duration of CPUCLK low, indicating to the 386SX a 16 bit cycle. Next CLK0, CPUCLK goes high and CLK2 rising high (T2B), NROMOE asserts, thus enabling ROM outputs. NMEMDIR asserts at this time, as well, signaling the SL9020 Data Controller to switch the memory data path from MDBus to DBus. After 2 wait states, on CLK2 rising high at T2W2B, NRDY asserts, signaling the SL9011 Controller that data is ready. The SL9011 drops NCPURDY, the CPU latches Bus data, and enters the second 16 Bit cycle by negating BE0, BE1, and NADS at T12 A. The second cycle repeats as the first. After the last ROM access, a valid ROM address will not be decoded and thus NCSROM, NROMOE, and NMEMDIR will be negated in T1 A.
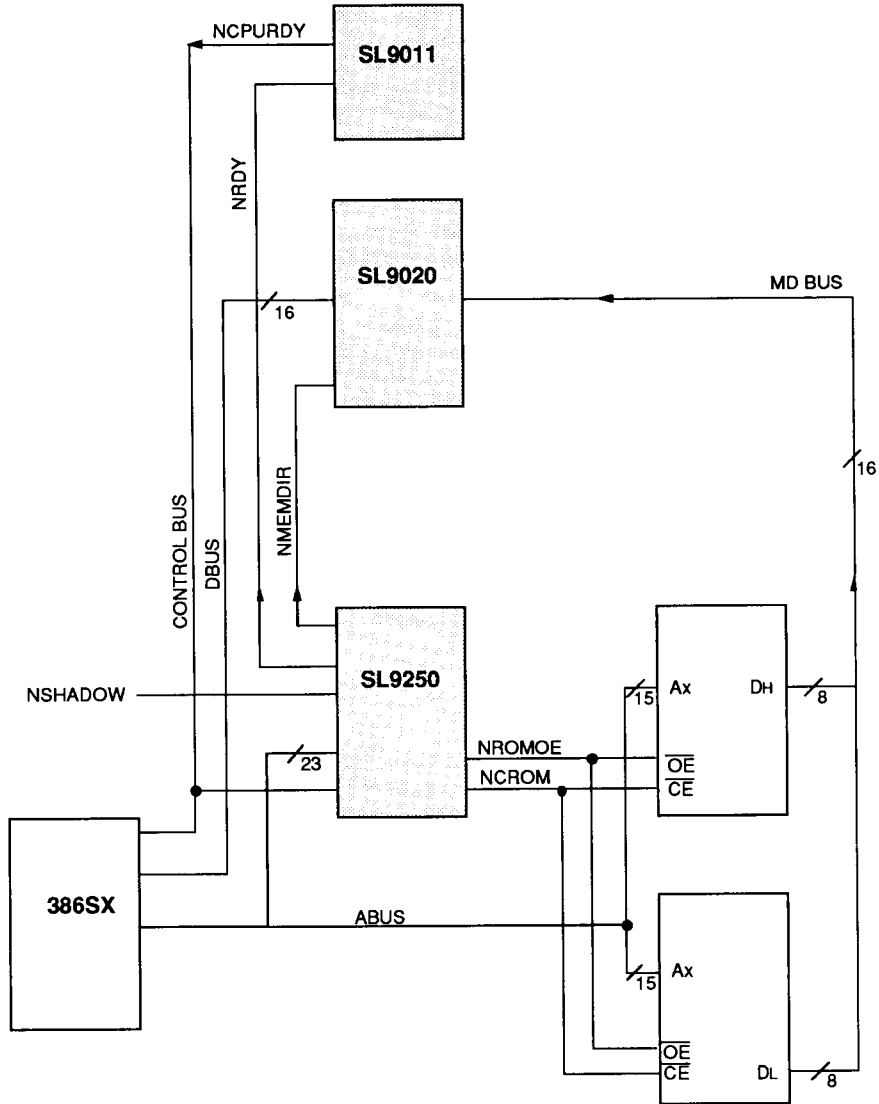
BLOCK DIAGRAM SL9250

Fig. 4 386SX ROM BLOCK DIAGRAM
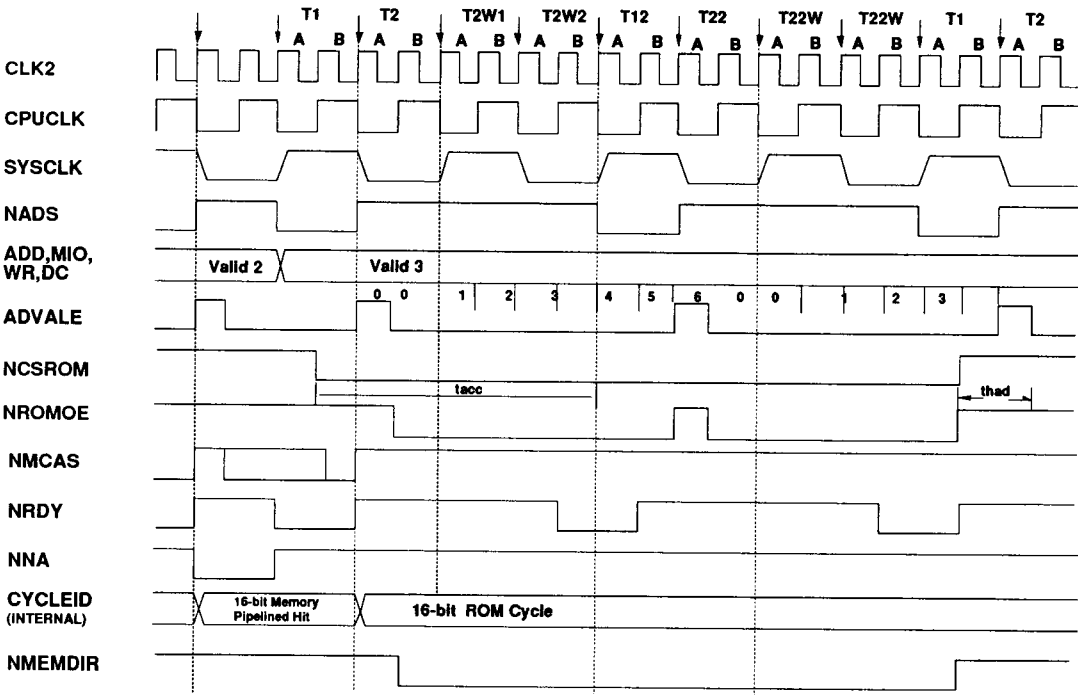
AC TIMING DIAGRAMS SL9250

Fig. 5 Timing Diagram for BIOS ROM cycle (16-bit memory)

PIN DESCRIPTION SL9250

SYMBOL	PIN	TYPE	DESCRIPTION
A1-A16	11,36,35,34,33, 32,31,30,27, 26,25,24,23, 22,21,20	I	CPU Address Bus.
A17-A19 A21-23	19,18,17, 14,13,12	I/O	CPU Address Bus.
A20GATE	75	I	CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH.
ADD20	58	O	Decoded 20-bit address bit used to generate address decode for 1 M RAMs.
ADVALE	59	O	Advanced Address Latch Enable from memory controller. It latches local bus address for the system bus.
CLK2	2	I	Input Clock used to clock internal state machine. It is 2 times the frequency of the CPUCLK.
CLK8042	76	I	7 MHz clock input. It is used to internally generate a RAS time out. (Page mode.)
CPUA20	16	I/O	CPU Address Bus.
CPUCLK	39	I	Input Clock simulating 386SX internal clock. It is CLK1 divided by two.
DC	6	I	CPU Status Signal. Differentiates between Data and Control instructions.
HLDA	46	I	CPU Output Signal, asserted to signal that the CPU has relinquished control of the bus to the requesting device: MASTER or DMA. It is used to tri-state SLOT addresses during master.
LA17-LA23	61,62,63,64, 66,67,68	I/O	Local address bus. Directly drives AT-SLOT signals LA17-LA23.
MA0-MA9	85,86,87,88, 89,91,92,93, 94,95	O	RAM Address Bus Output. Directly drives DRAM address inputs.
MA81	77	O	RAM Address pin for 1M RAMs. Used in place of MA8 for 1M DRAMs.

PIN DESCRIPTION SL9250 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
MIO	5	I	CPU output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle. It is being used by the state machine to generate memory and I/O signals for the system.
MSEL1-4	96,97,98,99	I	On-board Fast RAM memory size and type select. They are set as indicated in Table 1. The setting will determine the appropriate RAS and CAS outputs. Internally pulled down.
NADS	7	I	CPU output control signal, asserted when Address Bus outputs are valid.
NBMR	44	O	Buffered Memory Read signal. Used to latch addresses in the SL9025 Address Controller chip.
NBMW	45	O	Buffered Memory Write signal. Used to directly drive DRAM write input.
NCSROM	72	O	LOW assert ROM Chip Select. Connects directly to system ROM CS.
NLDEC16	70	O	Decode signal for on-board local HIGH-speed RAM. Indicates a local DRAM transfer is in process.
NLRAM	9	O	Decode for on-board external HIGH speed 16 Bit RAM.
NMASTER	69	I	Asserted when an external device has control of the AT Bus at slot card output. Used to set address direction from SLOT to system.
NCAS	84	O	Memory column address strobe. Asserted when either CPU or DMA is accessing the memory. Used to drive SL9020 NCAS input.
NMEGCS	37	O	Select Decode for lower 1M of memory. Used to drive SL9011 NMEGCS input.
NMEMDIR	43	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is used to drive SL9020 NMEMDIR input.
NMEMR	47	I	Read Memory command from SL9011/SLOT.

PIN DESCRIPTION SL9250 (Cont'd.)

| SYMBOL	PIN	TYPE	DESCRIPTION
NMEMW	48	I	Write Memory command from SL9011/SLOT.
NNA	10	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
NPAG4K	71	I	Active LOW Page size = 4K option; when 1M DRAMs are used. Left HIGH for 256Ks or mixes.
NRAS	57	O	LOW assert Row address strobe. Not used in normal operation.
NRAS0-3	100,1,80,81	O	Row address strobes for Banks 0,1,2 & 3 for the on-board memory. Generated during CPU or DMA cycle for memory access. Used to directly drive DRAM RAS inputs.
NRDY	49	O	Asserted one clock cycle after NNA is asserted at the end of a local memory cycle. Used to signal SL9011 that data is ready.
NREFRESH	55	I	On-board RAM refresh signal. Generated from REFREQ input.
NROM0E	38	O	Enables ROM output during ROM read cycles. Connects directly to ROMOE pin.
NS0,1	41,42	O	80286 compatible status signals for the AT System Controller SL9011.
NSHADOW	74	I	Selectable option for Shadow RAMs. LOW enables Shadow RAM feature.
RESET	56	I	Active HIGH Reset from system controller.
SA17-19	50,51,52	O	System Address Bus.
TEST3	73	I	Optional disable for 684K - 1M [384K] remap.
TEST4	60	I	Test Pin - Not connected.
VDD	3,28,53,78	-	+5V. Power.
VSS	4,15,29,40, 54,65,79,90	-	0V. Ground.
WR	8	I	CPU output control signal Write.
WSEL1,2	82,83	I	Wait-state Select options. Refer to Table 3 for proper setting. Internally pulled up.

AC TIMING DIAGRAMS SL9250
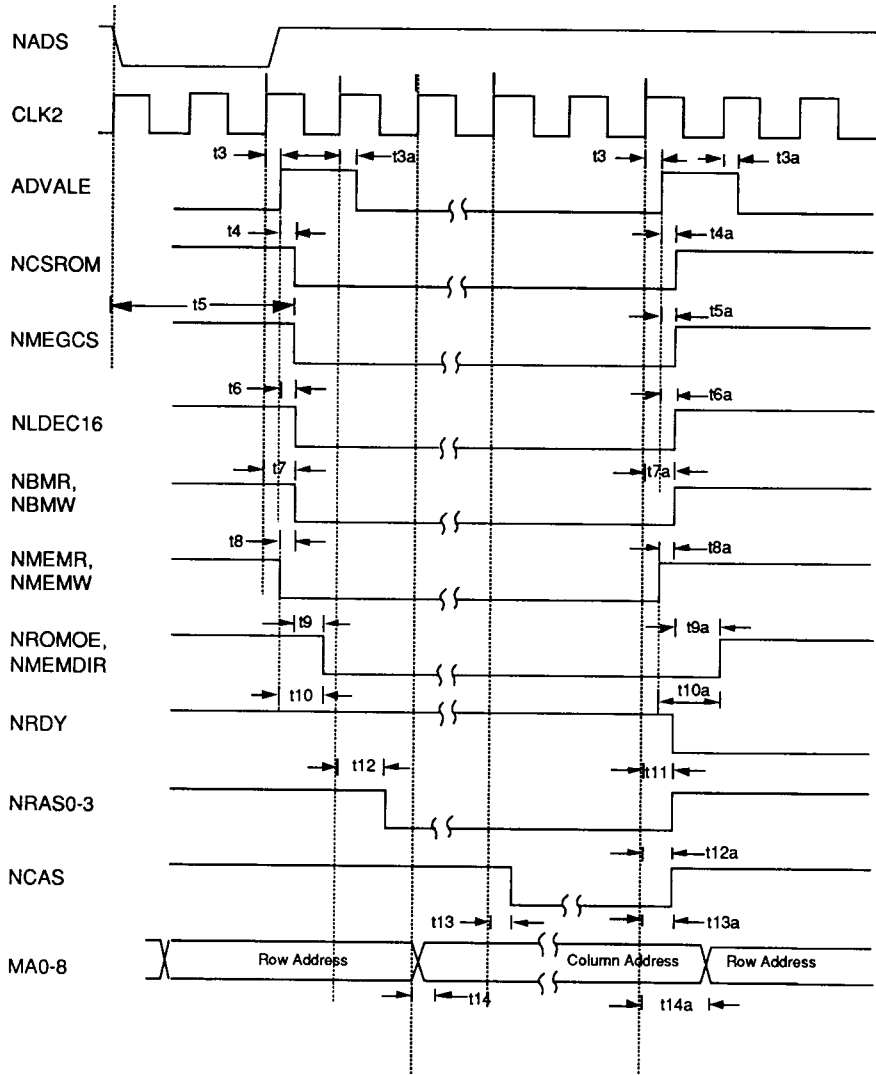
Fig. 6 Set-up and Hold Times

ABSOLUT MAXIMUM RATINGS   SL9250 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	VDD	-.5	6.0	V
Input Voltage	V1	-.5	VDD+.5	V
Output Voltage	V0	-.5	VDD+.5	V
Output Current *note 2	IOS	-40	+40	mA
Output Current *note 3	IOS	-40	+80	mA
Output Current *note 4	IOS	-60	+120	mA
Output Current *note 5	IOS	-90	+180	mA
Storage Temp.	TSTL	-40	+125	°C
Storage Temp.	TBIOS	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.

2. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NNA, NRDY, NROMOE, NS0, NS1.

3. A1, A17 - A19, A21-23, CPUA20.

4. ADD20, MA0-MA9, MA81, LA17 - LA23, NRAS, SA17 - SA19.

5. NBMW, NRAS0 - NRAS3.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	VDD	4.75	5.25	V
Temperature	TA	0	70	°C

DC CHARACTERISTICS   SL9250

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	CONDITIONS
Power Supply Current	IDDS	TBD	TBD	mA	20 MHz
Power Supply Current	IDDS	0	100	μA	Steady state
Output High Voltage *note 1	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output *note 2	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output NBMW, NRAS0-NRAS3	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output *note 3	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output A1, A17-A19, A21-23, CPUA20	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output *note 4	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output NBMW, NRAS0-NRAS3	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for All Inputs	VIH	2.2		V	
Input Low Voltage for All Inputs	VIL		0.8	V	
Input Leakage Current *note 5	ILI	-10	10	μA	VI = 0 - VDD
Input Leakage Current, Tri-state *note 6	ILZ	-10	10	μA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = Vss
Input Current, Pull-up *note 7	IILU	-335	-204	μA	VI = .4V
Input Current, Pull-up *note 8	IIHU	-135	-124	μA	VI = 2.4V
Input Current, Pull-up MSEL1-MSEL4	IILD	TBD	26	μA	VI = .4V
Input Current, Pull-up MSEL1-MSEL4	IIHD	14	106	μA	VI = 2.4V

NOTES:
1. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1, A1, A17-A19, A21-23, CPUA20
2. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
3. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1
4. ADD20, LA17-LA23, MA0-MA9, MA81, NRAS, SA17-SA19
5. A1-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, NREFRESH, RESET, WR
6. A1, A17-A19, A21-A23, CPUA20, LA17-LA23, SA17-SA19
7. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2
8. NSHADOW, NPAG4K, TEST3, TEST4, WSEL1, WSEL2

AC CHARACTERISTICS SL9250
(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	CLK2 Period	25	-	ns
t2	CLK2 High Duration	7	-	ns
t2a	CLK2 Low Duration	7	-	ns
t3	CLK2 to ADVALE (Low to High)	5	20	ns
t3a	CLK2 to ADVALE (High to Low)	5	20	ns
t4	ADVALE to NCSROM (High to Low)	5	15	ns
t4a	ADVALE to NCSROM (Low to High)	5	15	ns
t5	NADS to NMEGCS (High to Low)	5	15	ns
t5a	NADS to NMEGCS (Low to High)	5	15	ns
t6	ADVALE to NLDEC16 (High to Low)	5	15	ns
t6a	ADVALE to NLDEC16 (Low to High)	5	15	ns
t7	CLK2 to NBMR, NBMW (High to Low)	5	12	ns
t7a	CLK2 to NBMR, NBMW (Low to High)	5	12	ns
t8	NMEMR, NMEMW to NBMR, NBMW (High to Low)	5	10	ns
t8a	NMEMR,NMEMW to NBMR, NBMW (Low to High)	5	10	ns
t9	NBMR to NROMOE (High to Low)	0	12	ns
t9a	NBMR to NROMOE (Low to High)	0	12	ns
t10	NMEMR to NROMOE (High to Low)	5	15	ns
t10a	NMEMR to NROMOE (Low to High)	5	15	ns
t11	CLK2 to NRDY	5	12	ns
t12	CLK2 to NRAS0-NRAS3 (High to Low)	5	12	ns
t12a	CLK2 to NRAS0-NRAS3 (Low to High)	5	12	ns
t13	CLK2 to NCAS (High to Low)	5	12	ns
t13a	CLK2 to NCAS (Low to High)	5	12	ns
t14	CLK2 to MA0-MA8 Delay	5	15	ns

(TA = 25 ° C, VDD = V1 = 5V, fo = 1MHz)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	NOTES
Input Pin Capacitance	CIN	---	16	Pf	note 1
Input Pin Capacitance	CIN	---	TBD	Pf	note 2
Output Pin Capacitance	COUT	---	16	Pf	note 3
Output Pin Capacitance	COUT	---	18	Pf	note 4
I/O Pin Capacitance	CI/O	---	16	Pf	note 5
I/O Pin Capacitance	CI/O	---	23	Pf	note 6

NOTES:
1. A2-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, REFRESH, RESET, WR
2. NSHADOW, MSEL1-MSEL4, NPAG4K, TEST 3, TEST 4, WSEL1, WSEL2
3. ADVALE, ADD20, MA0-MA9, MA81, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NNA, NRDY, NRAS, NROMOE, NS0, NS1
4. NBMW, NRAS0-NRAS3
5. A1, A17-A19, A21-A23, CPUA20, LA17-LA23, SA17-SA19
6. NBMW, NRAS0-NRAS3