SL9151 80286 Page Interleave Memory Controller

PRELIMINARY

FEATURES

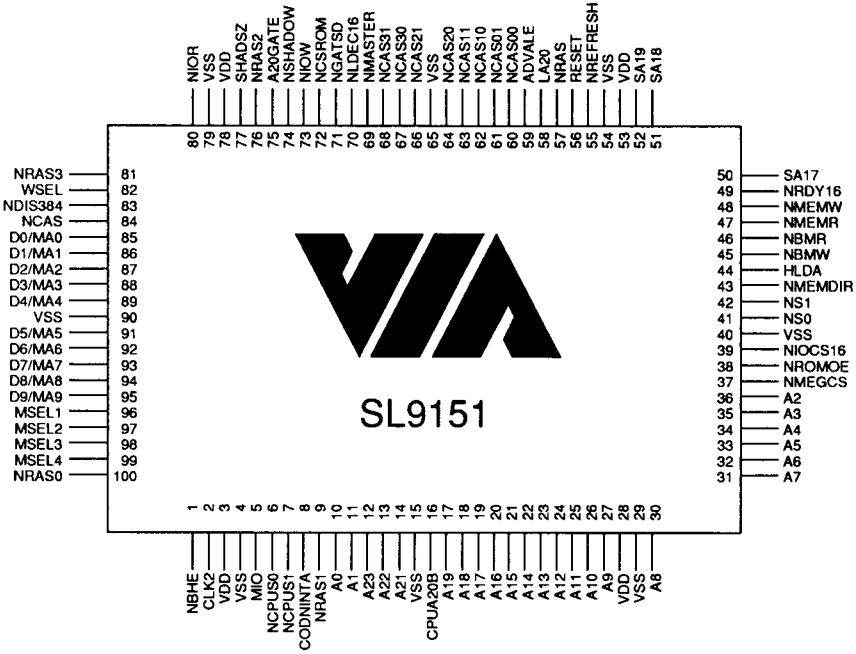
- Supports 80286 based designs.
- 16, 20 or 25 MHz Options.
- Enhanced Fast Page Mode/Page Interleave DRAM Controller.
- Hardware support for EMS LIM 4.0 standard and EEMS.
- Supports up to 8 M byte of on board memory.
- Programmable Shadow RAM feature of 128K or 256K.
- Programmable 2 or 4 way Memory Interleaving Option.
- Programmable Wait State Options.
- Can use 256K x 1, 256K x 4, and 1 M x 1 DRAMs or a mix.
- Supports 120ns and 80ns DRAMs at 16 MHz, 80ns and 60ns at 20 MHz and 60ns and 40ns at 25MHz.
- Programmable Registers for changing switch settings.
- Selectable Wait States for Slower DRAMs.
- Selectable remapping of 640K - 1 M RAM to top of the address space.
- Advanced CMOS Technology.
- 100 pin Flatpack.

DESCRIPTION

The SL9151 Memory Controller is a second generation integration of the most popular 80286 system level features. Both EMS LIM 4.0 and EEMS are now available on the chip. Programmable registers are available for controlling 2 or 4 way memory interleave options. In addition, earlier features have been expanded and optimized for higher performance.

The SL9151, along with the SL925X and SL935X provide complete PC/AT solutions by utilizing the same core logic chips. It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

PINOUT


NIOR 80
VSS 79
VDD 78
SHADSZ 77
NRAS2 76
A20GATE 75
NSHADOW 74
NIOW 73
NCSROM 72
NGATSD 71
NLDEC16 70
NMASTER 69
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NCAS11 63
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ADVALE 59
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D0/MA0 85
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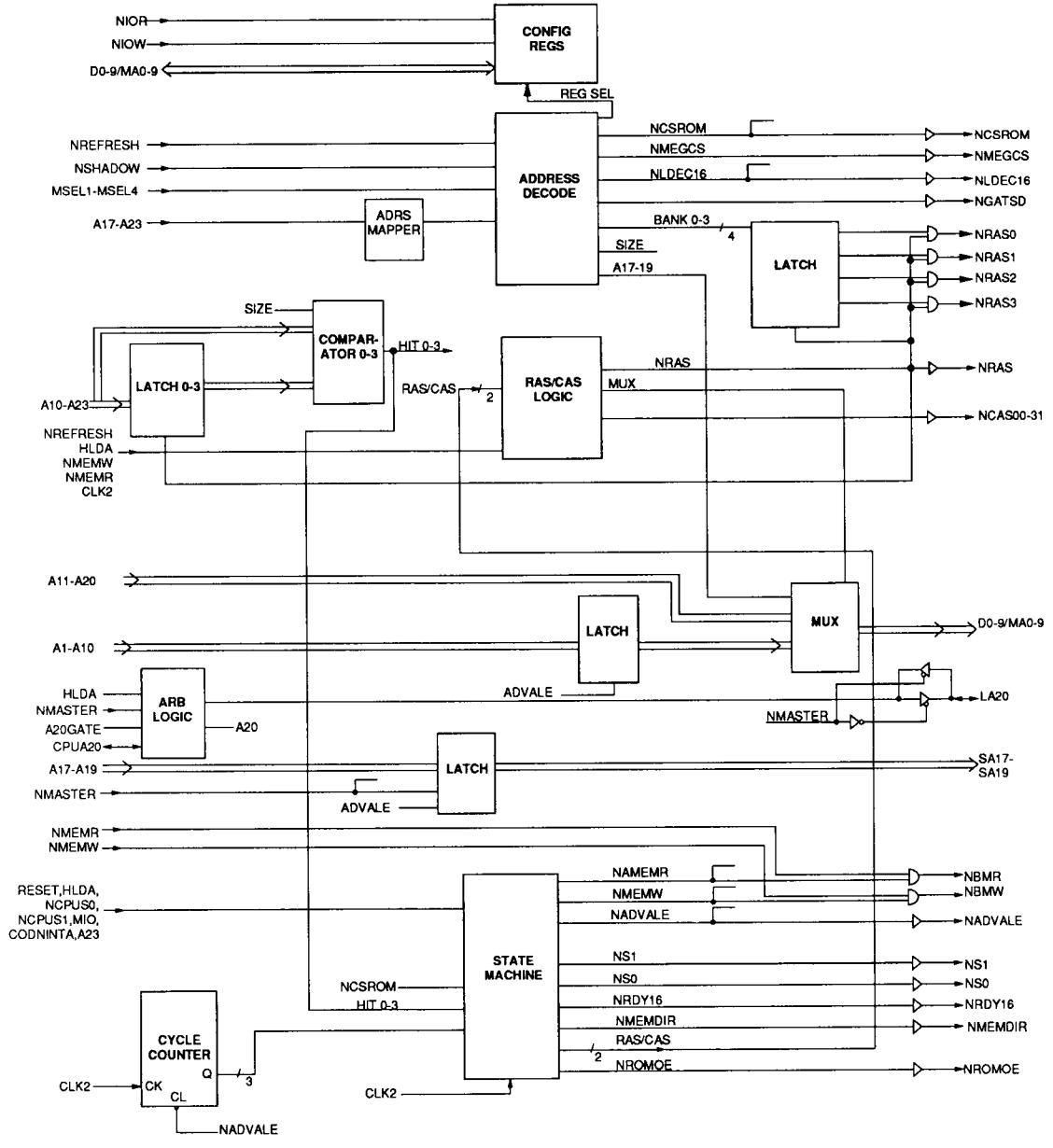
D6/MA6 92
D7/MA7 93
D8/MA8 94
D9/MA9 95
MSEL1 96
MSEL2 97
MSEL3 98
MSEL4 99
NRAS0 100
50 SA17
49 NRDY16
48 NMEMW
47 NMEMR
46 NBMR
45 NBMW
44 HLDA
43 NMEMDIR
42 NS1
41 NS0
40 VSS
39 NIOCS16
38 NROMOE
37 NMEGCS
36 A2
35 A3
34 A4
33 A5
32 A6
31 A7
SL9151
1 NBHE
2 CLK2
3 VDD
4 VSS
5 MIO
6 NCPUS0
7 NCPUS1
8 CODNINTA
9 NRAS1
10 A0
11 A1
12 A23
13 A22
14 A21
15 VSS
16 CPUA20B
17 A19
18 A18
19 A17
20 A16
21 A15
22 A14
23 A13
24 A12
25 A11
26 A10
27 A9
28 VDD
29 VSS
30 A8

BLOCK DIAGRAM SL9151



DESCRIPTION

ROM/RAM DECODE

The device provides all necessary circuitry to decode on board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column or Fast Page DRAMs.

The system can be configured for 512K Bytes to 8M Bytes. The bank selection code & sizes are as follows:

Total On Board Memory	Memory in Each Bank				Switch Selection				Operation Mode
	Bank3	Bank2	Bank1	Bank0	MseI4	MseI3	MseI2	MseI1	
512K				512K	0	0	0	0	Non Interleaved
1M			512K	512K	0	0	0	1	Non Interleaved
1.5M		512K	512K	512K	0	0	1	0	Non Interleaved
2M	512K	512K	512K	512K	0	0	1	1	Non Interleaved
3M		2M	512K	512K	0	1	1	0	Non Interleaved
5M	2M	2M	512K	512K	0	1	1	1	Non Interleaved
2M				2M	1	1	0	0	Non Interleaved
4M			2M	2M	1	1	0	1	Non Interleaved
6M		2M	2M	2M	1	1	1	0	Non Interleaved
8M	2M	2M	2M	2M	1	1	1	1	Non Interleaved
									Interleaved:
1M			512K	512K	1	0	0	0	2 Way
2M	512K	512K	512K	512K	1	0	0	1	4 Way
4M			2M	2M	1	0	1	0	2 Way
8M	2M	2M	2M	2M	1	0	1	1	4 Way

Table 1

When NDIS384 input is tied low, the 384K remap to the top of the memory space is disabled.

When CPU accesses the memory for the first time, the controller runs a page miss memory cycle and asserts RAS and CAS low at appropriate times (Fig. 1). RAS is left low, CAS is returned high at the end of the cycle and the current row address is stored in an internal register. During all subsequent cycles, row addresses are compared with previous value stored in the register. If a match (hit) is detected, then the RAS is held low and CAS is strobed immediately. If a mismatch (miss) is detected then RAS is brought high for 3 CLK2 cycles before reasserting low, and new row address is stored in the row address register. The controller will now run an 0/2 or 1/3 wait state memory cycle depending on the switch setting WSEL1 (Fig. 1, Fig. 2).

Page is automatically sized to 2KB if any 256K DRAMs are used and to 4KB if only 1M DRAMs are used.

CPU Addresses A11-A20 are passed onto MA0-9 as latched row addresses whereas A1-A10 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. NRAS, MUXSEL (internal), and NCAS00-31 are separated by one CLK2 period as shown in the timing diagram (fig.1). This latching of column addresses allows the use of static column DRAMs as well.

ROM/RAM CONTROL

SL9151 provides all the circuitry needed to generate RAM/ROM controls. Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS00-31), RAM Read/Write (NBMR, NBMW) ready for 16 bit on board RAM read/write (NRDY16) and non on-board memory/IO cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

MIO	CODNINTA	CPUNS0	CPUNS1	ADDRESS	CYCLE TYPE
1	0	0	1	_____	MEM CODE READ
1	0	0	0	_____	HALT/SHUTDOWN
1	1	1	0	_____	MEM DATA READ
1	1	0	1	_____	MEM DATA WRITE
0	0	0	0	_____	INTA
0	1	1	0	_____	I/O DATA READ
0	1	0	1	_____	I/O DATA WRITE

Table 2

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 16 bit memory miss can be set using the following table.

CPU SPEED	WSEL1	WAIT STATES		MEMORY SPEED (NS)
		Page Miss	Page Hit	
16	1	3	1	120
	0	2	0	80
20	1	3	1	80
	0	2	0	60
25	1	3	1	60
	0	2	0	40

Table 3

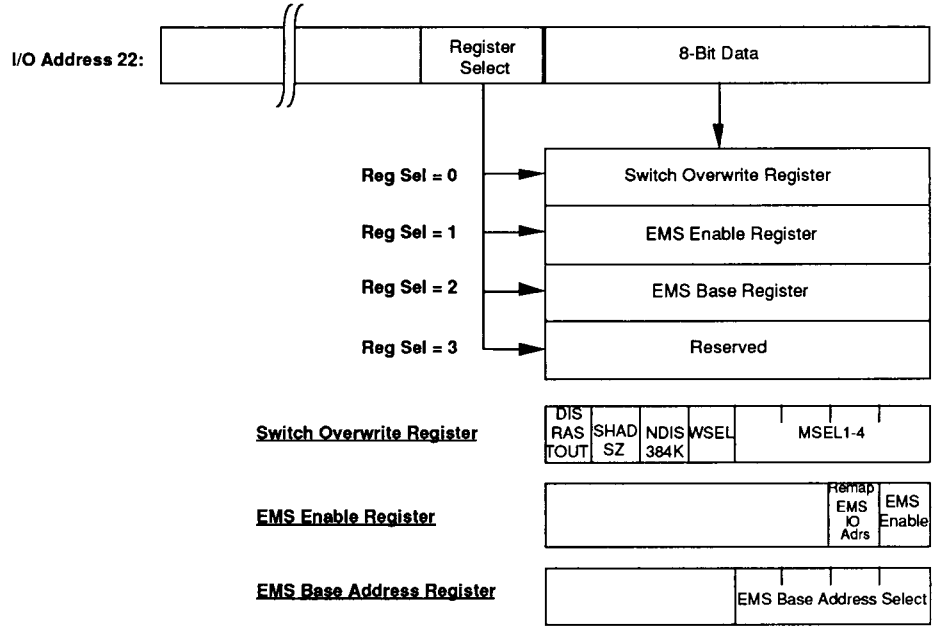
ROM controls, NCSROM and NROMOE, are asserted low at appropriate time when address 0E0000h-0FFFFFh or FE0000h-FFFFFFh is decoded during a memory cycle. The timing relationship is shown in the timing diagram. If Shadow RAM option is used by strapping NSHADOW pin low, the subsequent ROM code reads will be treated as RAM reads and ROM controls are disabled. BIOS customization is required to activate this option at boot time. NSHADOW option only affects the 128K/256K region immediately below 1 Meg, depending on the state of SHADSZ pin.

REFRESH

The SL9151 provides support for DRAM refresh. During refresh NRAS0-3 are deasserted and then asserted low, NCAS is inhibited high, the current bus state is ignored, and a refresh address generated by SL9025 Address Controller are passed from A Bus to MA Bus.

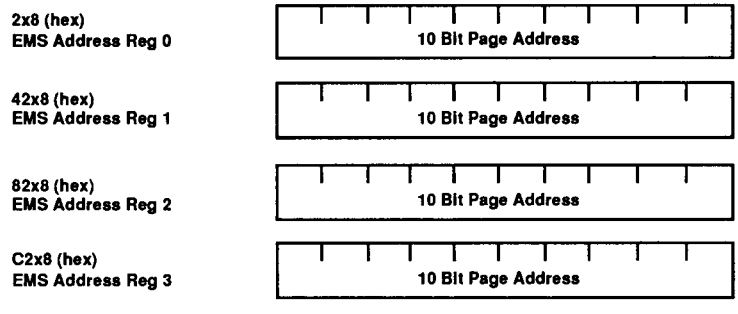
INTERNAL REGISTERS

16 Bit I/O write to address 22 writes a byte of data to one of 4 registers as selected by Data Bits 8 and 9.



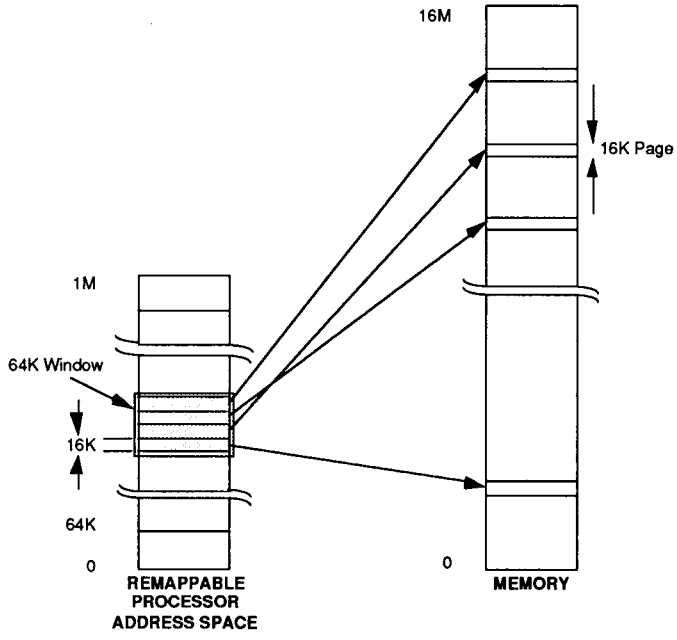
There are 4 EMS address registers of 10 bits width each, at the addresses: 2x8, 42x8, 82x8 and C2x8. X is 0 or 1 as defined by EMS Enable Register Bit 1. They each contain the Page Address for EMS Remapped Page.

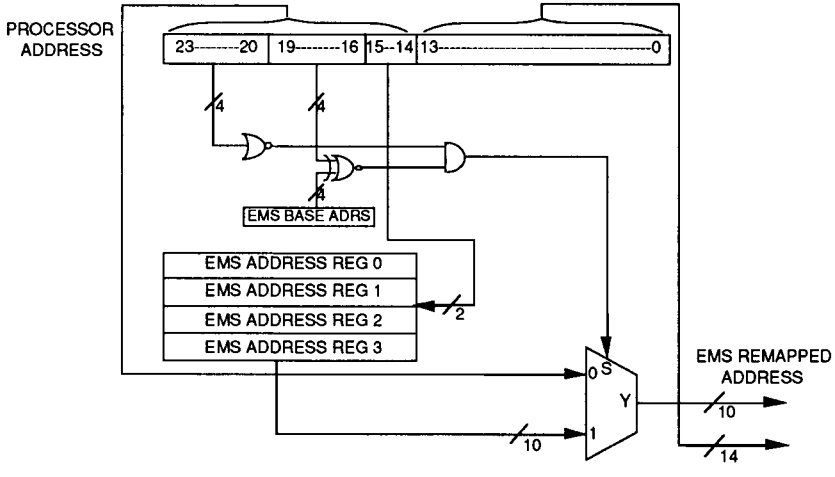
The remapping is shown in the diagrams.



EMS REMAPPING

EMS Base Address can be set to any 64K boundary in the first 1 Meg address space of the processor.
Then four 16K pages above that (base-address) can be mapped to any 16K boundary in the 16 Meg space.





PIN DESCRIPTION SL9151

SYMBOL	PIN	TYPE	DESCRIPTION
A1-A16	11,36,35,34, 33,32,31,30, 27,26,25,24, 23,22,21,20	I	CPU Address Bus.
A17-A23	19,18,17,14, 13,12	I	CPU Address Bus.
A20GATE	75	I	CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH.
ADVALE	59	O	Advanced Address Latch Enable. It latches local bus address for the system bus.
CLK2	2	I	CLK2 from SL9011 System Controller. CPU should get inverted CLK2.
CODNINTA	8	I	CPU status signal.
CPUA20B	16	I/O	CPU Address 20 or LA20.
D0-9/MA0-9	85,86,87,88, 89,91,92,93, 94,95	I/O	DRAM address bus. Data Bus for writing to the programmable registers for EMS and option select registers.
HLDA	44	I	Asserted to signal that the CPU has relinquished control of the bus to the requesting device.
LA20	58	I/O	Decoded 20-bit address bit used to generate address decode for 1 M RAMs.
MIO	5	I	CPU Output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle. It is used to generate memory and I/O signals for the system.
MSEL1-4	96,97,98,99	I	On-board DRAM memory size and type select. Internally pulled down. See Table 1.
NBMR	46	O	Buffered Memory Read signal.
NBMW	45	O	Buffered Memory Write signal.
NCAS	84	O	Logical Or of all CAS00-31 signals.
NCAS00,01, 10, 11,20, 21 30, 31	60-64, 66-68	O	Memory Column Address Strobe. Asserted LOW when either CPU or DMA is accessing the memory.

PIN DESCRIPTION SL9151 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NCPUS0,1	6,7	I	CPU status signal.
NCSROM	72	O	LOW assert Read Only Memory Chip select.
NDIS384	83	I	Optional Disable for 684K - 1M [384K] remap. When LOW disables remap.
NGATSD	71	O	Control for an external data buffer used for writing from XD Bus to XD/MA inputs only during I/O write cycles. This signal may be used to enable a 74245 type device. When LOW the 74245 may enable this data.
NIOCS16	39	I/O	16 Bit I/O cycle indication.
NIOR	80	I/O	Input/Output Read is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle.
NIOW	73	I/O	Input/Output Write is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle.
NSHADOW	74	I	Selectable Option for Shadow RAMs. When LOW enables Shadow RAM feature.
NLDEC16	70	O	Decode for on-board high speed 16-bit RAM.
NMASTER	69	I	Asserted when an external device has control of the AT Bus.
NMEGCS	37	O	Decode for lower 1M of RAM.
NMEMDIR	43	O	Direction select between D Bus and MD Bus. Read when LOW, generated by SL9011 System Controller.
NMEMR	47	I	LOW assert Memory Read signal from SL9011 System Controller.
NMEMW	48	I	LOW assert Memory Write signal from SL9011 System Controller.
NRAS	57	O	LOW assert Row Address Strobe.
NRAS0-3	100,9,76,81	O	Row Address Strobes for Banks 0, 1, 2 and 3 for the on-board memory. Asserted LOW during CPU or DMA cycle for memory access.

PIN DESCRIPTION SL9151 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NRDY16	49	O	Asserted LOW to signal the end of 16 bit on board memory cycle.
NREFRESH	55	I	On-board RAM refresh signal.
NROMOE	38	O	Enables ROM Output during ROM read cycles.
NS0,1	41,42	O	80286 compatible status signals for the SL9011 System Controller.
RESET	56	I	Active HIGH reset from system controller.
SA17,18,19	50,51,52	O	System Address Bus.
SHADSZ	77	I	Selects Shadow Memory Size. 0 = 128K. 1 = 256K.
WSEL	82	I	Wait-state Select Options. Internally pulled up. See Table 3.
VDD	3,28,53,78	-	+5V. Power.
VSS	4,15,29,40, 54,65,79,90	-	0V. Ground.

AC TIMING DIAGRAMS SL9151

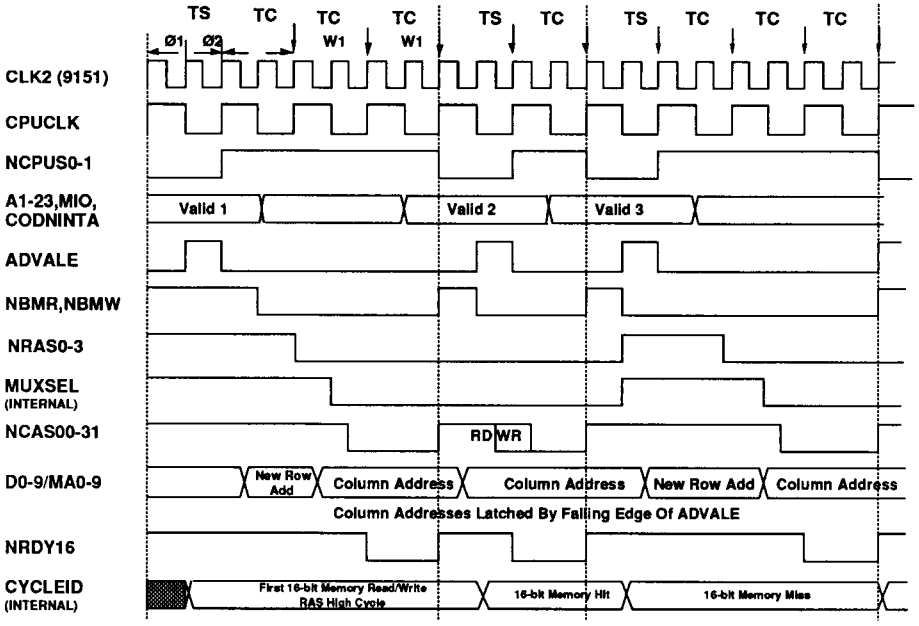


Fig. 1 16 Bit On Board/Local Memory Cycles Timing Diagram

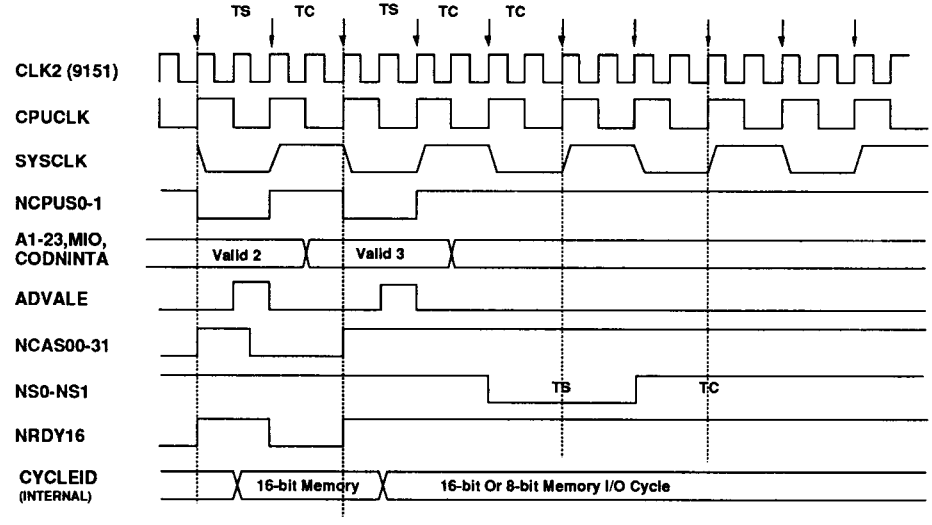


Fig. 2 Timing Diagram for I/O and Off Board Memory Cycles

AC TIMING DIAGRAMS SL9151

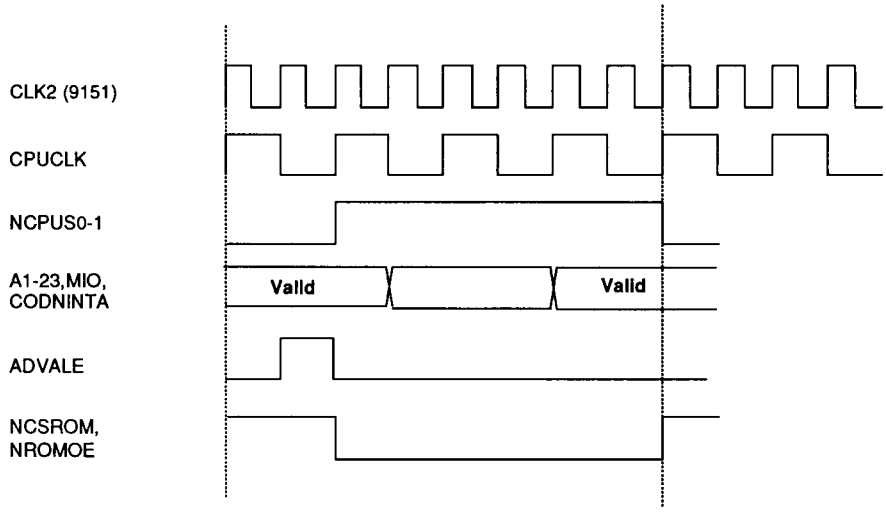


Fig. 3. ROM Cycle

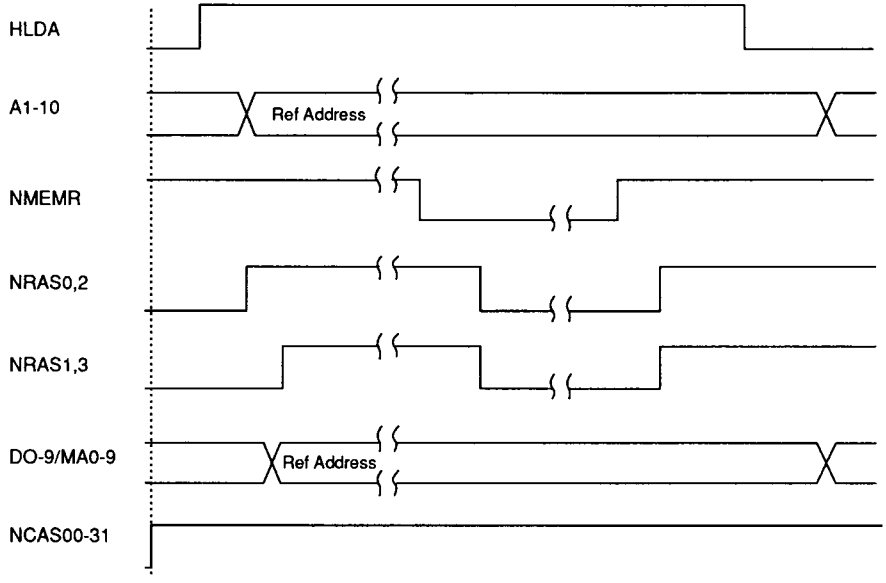


Fig. 4. Refresh Cycle

ABSOLUT MAXIMUM RATINGS SL9151 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current	I_{OS}	-40	+40	mA
Output Current	I_{OS}	-40	+80	mA
Output Current	I_{OS}	-60	+120	mA
Output Current	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9151

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2	---	V	
Input Low Voltage for Normal Input	VIL	---	0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL	---	0.3VDD	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = Vss

NOTES:

* VIH = VDD, VIL = Vss

RAS0-RAS3, NBMR, NBMW, SA17-SA19	= 24 mA	(typical)
LA17-LA23, MA0-MA9	= 12 mA	
A1-A16, A17-A23	= 8 mA	

AC CHARACTERISTICS SL9151

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	CLK2 Period	25	-	ns
t2	CLK2 High Duration	7	-	ns
t2a	CLK2 Low Duration	7	-	ns
t3	CLK2 to ADVALE (Low to High)	5	20	ns
t3a	CLK2 to ADVALE (High to Low)	5	20	ns
t4	ADVALE to NCSROM (High to Low)	5	15	ns
t4a	ADVALE to NCSROM (Low to High)	5	15	ns
t5	ADVALE to NMEGCS (High to Low)	5	15	ns
t5a	ADVALE to NMEGCS (Low to High)	5	15	ns
t6	ADVALE to NGATSD (High to Low)	5	15	ns
t6a	ADVALE to NGATSD (Low to High)	5	15	ns
t7	ADVALE to NLDEC16 (High to Low)	5	15	ns
t7a	ADVALE to NLDEC16 (Low to High)	5	15	ns
t8	CLK2 to NBMR, NBMW (High to Low)	5	12	ns
t8a	CLK2 to NBMR, NBMW (Low to High)	5	12	ns
t9	NMEMR, NMEMW to NBMR, NBMW (High to Low)	5	10	ns
t9a	NMEMR,NMEMW to NBMR, NBMW (Low to High)	5	10	ns
t10	NBMR to NROMOE (High to Low)	0	12	ns
t10a	NBMR to NROMOE (Low to High)	0	12	ns
t11	NMEMR to NROMOE (High to Low)	5	15	ns
t11a	NMEMR to NROMOE (Low to High)	5	15	ns
t12	CLK2 to NRDY16	5	12	ns
t13	CLK2 to NRAS0-NRAS3 (High to Low)	5	12	ns
t13a	CLK2 to NRAS0-NRAS3 (Low to High)	5	12	ns
t14	CLK2 to NCAS00-31 (High to Low)	5	12	ns
t14a	CLK2 to NCAS00-31 (Low to High)	5	12	ns
t15	CLK2 to MA0-MA9 Delay	5	15	ns

AC TIMING DIAGRAMS SL9151