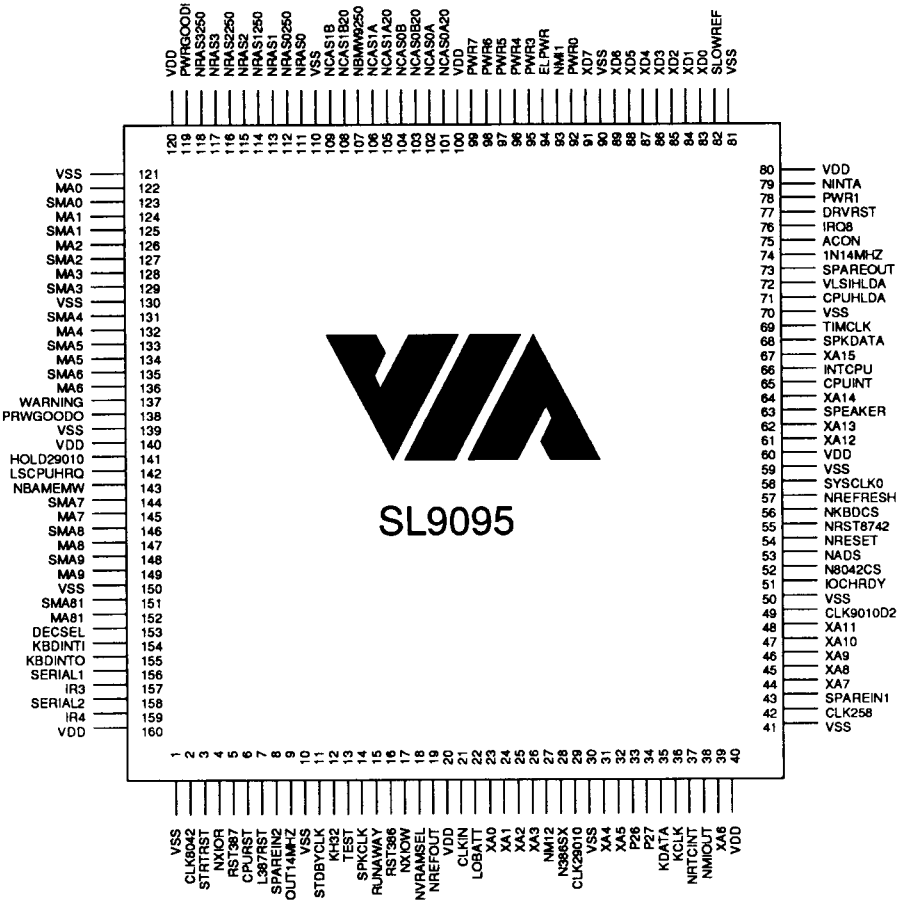
FEATURES

- Supports 80286, 80386SX, 80386DX, and 80486 Page Mode or Cache-based Laptop designs.
- IBM PC/AT Compatible.
- Software Programmable Power Management Unit. Provides Individual On/Off Control.
- Compatible with all CPU Clock Rates.
- Supports Suspend and Resume Modes.
- Auto Power On Capability.
- Supports Slow Refresh DRAMs.
- Sleep Mode.
- Generates all the necessary PC/AT Clock Signals.
- Advanced CMOS Technology.
- 160 pin Plastic Flatpack.

DESCRIPTION

The SL9095 is an integrated CMOS Power Mangement Unit (PMU) which minimizes the power consumption and maximizes the battery life in laptop designs. The PMU is a single chip addition to the FlexSet PC/AT core logic chip set. The FlexSet provides all of the core logic required for any Intel microprocessor based designs (80286, 80386SX, 80386DX and 80486). This approach provides minimum chip count, low power dissipation, low cost and maximizes upward design compatibility.

PINOUT


SL9095
1 VSS
2 CLK8042
3 STRTRST
4 NXIOR
5 RST387
6 CPURST
7 L387RST
8 SPAREIN2
9 OUT14MHZ
10 VSS
11 STDBYCLK
12 KH32
13 TEST
14 SPKCLK
15 RUNAWAY
16 RST386
17 NXIOW
18 NVRAMSEL
19 NREFOUT
20 VDD
21 CLKIN
22 LOBATT
23 XA1
24 XA2
25 XA3
26 NMI2
27 N386SX
28 CLK29010
29 VSS
30 XA4
31 XA5
32 P26
33 P27
34 KDATA
35 KCLK
36 NRTCINT
37 NMIOUT
38 XA6
39 VDD
40
41 VSS
42 CLK258
43 SPAREIN1
44 XA7
45 XA8
46 XA9
47 XA10
48 XA11
49 CLK9010D2
50 VSS
51 IOCHRDY
52 N8042CS
53 NADS
54 NRESET
55 NRST8742
56 NKBDCS
57 NREFRESH
58 SYSCLK0
59 VSS
60 VDD
61 XA12
62 XA13
63 SPEAKER
64 XA14
65 CPUINT
66 INTCPU
67 XA15
68 SPKDATA
69 TIMCLK
70 VSS
71 CPUHLDA
72 VLSIHLDA
73 SPAREOUT
74 1N14MHZ
75 ACON
76 IRQ8
77 DRVRST
78 PWR1
79 NINTA
80 VDD
81 VSS
82 SLOWREF
83 XD0
84 XD1
85 XD2
86 XD3
87 XD4
88 XD5
89 XD6
90 VSS
91 XD7
92 PWR0
93 NMI
94 ELPWR
95 PWR3
96 PWR4
97 PWR5
98 PWR6
99 PWR7
100 VDD
101 NCAS0A20
102 NCAS0A
103 NCAS0B20
104 NCAS0B
105 NCAS1A20
106 NCAS1A
107 NBMW8250
108 NCAS1B20
109 NCAS1B
110 VSS
111 NRAS0
112 NRAS0250
113 NRAS1
114 NRAS1250
115 NRAS2
116 NRAS2250
117 NRAS3
118 NRAS3250
119 PWRGOOD1
120 VDD
121 VSS
122 MA0
123 SMA0
124 MA1
125 SMA1
126 MA2
127 SMA2
128 MA3
129 SMA3
130 VSS
131 SMA4
132 MA4
133 SMA5
134 MA5
135 SMA6
136 MA6
137 WARNING
138 PRWGOODO
139 VSS
140 VDD
141 HOLD29010
142 LSCPUHRQ
143 NBAMEMW
144 SMA7
145 MA7
146 SMA8
147 MA8
148 SMA9
149 MA9
150 VSS
151 SMA81
152 MA81
153 DECSEL
154 KBDINTI
155 KBDINTO
156 SERIAL1
157 IR3
158 SERIAL2
159 IR4
160 VDD

GENERAL OPERATION

The SL9095 Power Management Unit supports three modes of operation, sleep mode, auto power off and suspend/resume. As an option, slow refresh DRAMs can be used to further reduce power during these various power down modes.

SLEEP MODE:

When the CPU is not executing a program or I/O operation and waiting for a keyboard input, a programmable counter is initialized in the PMU. If an interrupt does not occur within the programmed time limit (2 seconds to 8 minutes), the PMU will initiate a sleep mode. During sleep mode, the Real Time Clock interrupt is blocked, the CPU is halted and the clock is stopped for the 80286 and SL9011 PC/AT System Controller. Power is turned off for the SL9025 Address Controller, SL9250 Memory Controller, SL9020 Data Controller, EPROM, RS232C, EL or LCD display and SCSI Hard Disk Controller. The clock is slowed down for 80386SX and 80386DX, such that the CPU consumes a minimum amount of power. Following a keyboard entry, the power is turned back on and the CPU resumes execution . The memory is refreshed by the Power Management Unit while in the sleep mode. At the next keyboard entry, mouse or modem interrupt the PMU initiates "auto power on" allowing the CPU to continue at the same step where it was previously halted.

AUTO POWER OFF:

The Power Management Unit provides a programmable timeout counter to monitor the activity of a power hungry device. For example, the power to a electro-luminescent display can be automatically shut off if "no activity" has been detected for the programmed interval.

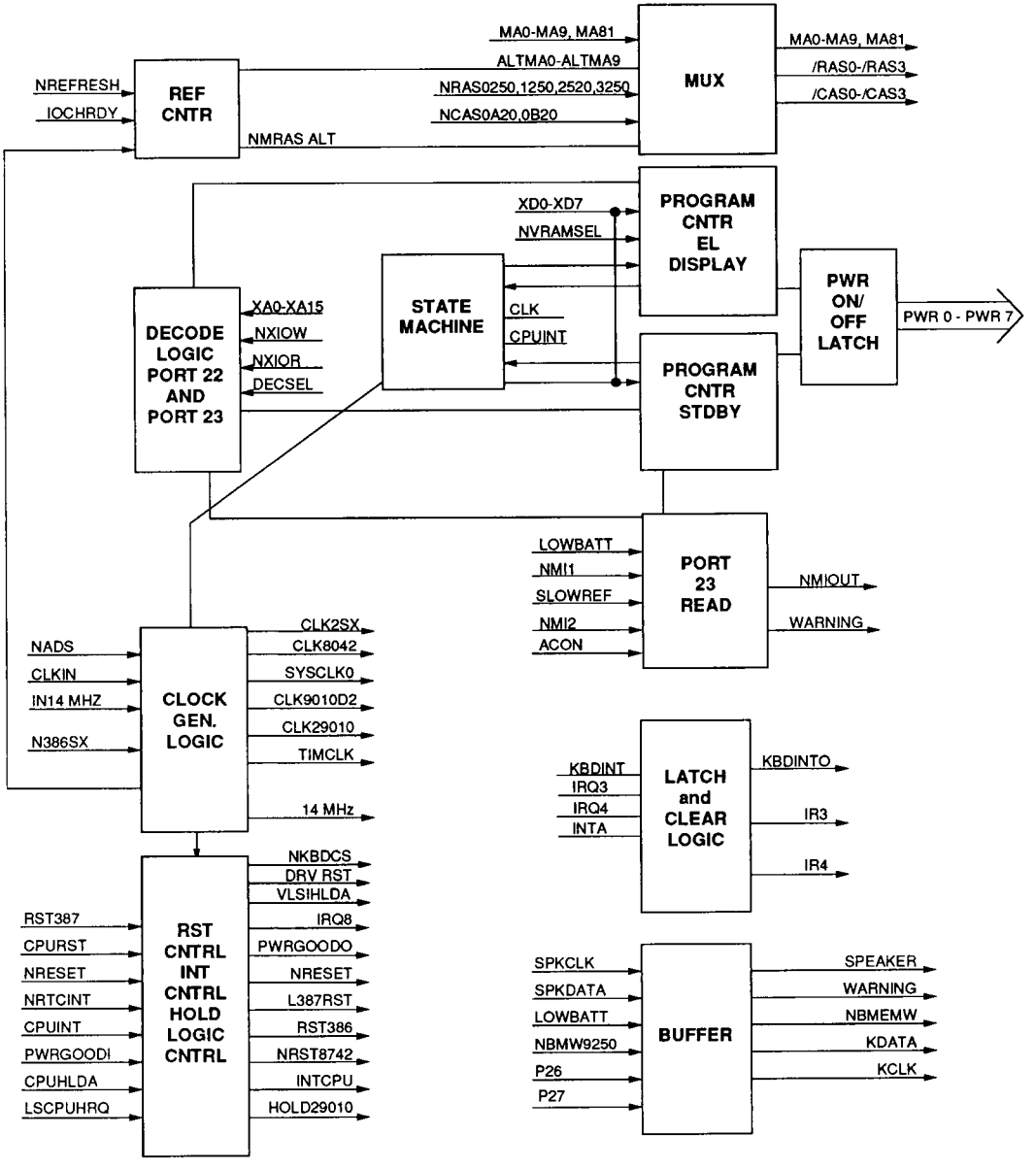
SUSPEND / RESUME:

The Suspend / Resume feature is a system option that enables a user to turn the system off (suspend) and save the current application. When power is turned back on (resume), the application continues from the point where it was suspended. The contents of all registers are stored in the battery backed up memory space or disk when power is turned off. If they were copied to disk, they will get copied back to the registers when power is turned back on. In order to accomplish this, all registers are read / writeable. During the power off sequence, if the resume option is enabled, BIOS is required to set check sum flags in memory. When the power is turned on again, the BIOS should always check the flags to see whether the data stored in the memory was valid while the system was in standby. If the flags are not valid then the BIOS will start the system as a cold start. The BIOS software must implement the suspend/resume feature for the PMU to operate.

SLOW REFRESH OPTION:

In order to use slow refresh DRAMs, the status bit on port 23 must be switched high. During power up, the system BIOS will check this status bit and set the SL9030 IPC refresh parameters.

BLOCK DIAGRAM SL9095



BLOCK DIAGRAM DESCRIPTION

1. REFRESH COUNTER: Generates refresh addresses during standby. Address generation during normal operations is handled by the SL9250.

2. MUX: Multiplexes memory addresses from the memory controller and the SL9095 refresh counter depending on the operating mode. DRAM selection should comprehend a small additional delay from MUX.

3. PROGRAMMABLE COUNTER, EL DISPLAY: Controls power supply and timing for an EL or LCD display.

4. PROGRAMMABLE STANDBY: Controls power supply and timing on power pins P0-P7.

5. STATE MACHINE: Generates the timing to control the programmable counters.

6. PORT 23 READ: Controls all status signals for machine operability.

7. CLOCK GENERATOR LOGIC: Generates all clocks required for PC/AT by using two oscillators.

8. RESET CONTROLLER: Generates all reset signals to ensure device operation during standby.

9. LATCH and CLEAR LOGIC: Latches keyboard, modem and mouse interrupts during standby.

PIN DESCRIPTION SL9095

SYMBOL	PIN	TYPE	DESCRIPTION
ACON	75	I	Active HIGH it indicates that the AC switch is ON.
CLKIN	21	I	Clock Input from an oscillator. It's frequency is twice that of the processor speed.
CLK258	42	O	Clock Output for the CPU. It's frequency is twice that of the processor speed and it is connected to the CPU.
CLK29010	29	O	Clock output for the PC/AT System Controller. It's frequency is twice that of the CPU speed and it is connected to the PC/AT SL9011 System Controller.
CLK8042	2	O	7MHz Keyboard Controller clock which is half the frequency of IN14MHZ frequency.
CLK9010D2	49	O	Clock output for the PC/AT SL9011 System Controller. It's frequency is equal to the frequency of the internal processor clock.
CPUHLDA	71	I	CPU hold acknowledge input. It is active HIGH when a bus cycle is granted in response to a hold request.
CPUINT	65	I	Active HIGH, interrupt from the Interrupt Controller, when asserted, will wake up the system from Sleep Mode.
CPURST	6	I	Active High from Sleep Mode. CPU reset signal input from the PC/AT System Controller SL9011.
DECSEL	153	I	This signal selects the port address for the SL9095 PMU. A HIGH maps the PMU SL9095 at port 22 and 23. A LOW maps the PMU SL9095 at port A4EA and A4EB.
DRVRST	77	O	The DRIVE RESET is an active HIGH output. This signal is not generated in STDBY. When active, it resets the system.
ELPWR	94	I	Display Power.
HOLD29010	141	O	This is the CPU Hold Request output. It is used to request control of the system bus.
IOCHRDY	51	I	The I/O Channel Ready is an active HIGH input from the AT bus. When active LOW, it indicates a not ready condition.

PIN DESCRIPTION SL9095 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
IN14MHZ	74	I	The CLK inputs from an oscillator are used to generate the clock signals OSC(14 MHz) , OSC/12 (TIMCLK) and the keyboard clock (CLK8042).
INTCPU	66	O	The INTCPU6 is an output used to interrupt the CPU. It is active HIGH.
IR3	157	O	This is the interrupt request output to the SL9030 Integrated Peripheral Controller. This active HIGH serial port2 interrupt request signal is latched in STANDBY.
IR4	159	O	This active HIGH interrupt request output to the SL9030 Integrated Peripheral Controller is latched in STANDBY.
IRQ8	76	O	Interrupt request output for the Real Time Clock interrupt.
KBDINTI	154	I	Active HIGH Keyboard Interrupt from Keyboard Controller 8742.
KBDINTO	155	O	Active HIGH Keyboard Interrupt output to the SL9030 Integrated Peripheral Controller is latched in STANDBY.
KCLK	36	O	Buffered Keyboard Clock output.
KDATA	35	O	Buffered Keyboard Data output.
KH32	12	I	This is the time base for the STANDBY counter. The clock is divided by 64K to generate STDBY CLK.
LOWBATT	22	I	A LOW signal on this input indicates that the battery is getting weak and needs to be recharged.
LSCPUHRQ	142	I	Active HIGH HOLDREQUEST input from the SL9030 Integrated Peripheral Controller.
L387RST	7	O	This output is latched RST387 and is not asserted when going into or coming out of STANDBY. It is connected to 80387SX coprocessor and it is active HIGH.
MA0 - MA9	122, 124, 126, 128, 132, 134, 136, 145, 147, 149	O	This is the RAM address bus.

PIN DESCRIPTION SL9095 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
MA81	152	O	This is the RAM address select pin for 1M DRAMs.
NADS	53	I	The address status is an input generated by the CPU. When asserted it indicates the start of a new cycle.
NBAMEMW	143	O	The Buffered Memory Write signal is active LOW.
NBMW9250	107	I	The Memory Write input from the Memory Controller is active LOW.
NCAS0A,1A	102, 106	O	CAS0 and CAS1 for bank A is active LOW.
NCAS0A20, 1A20	101, 105	I	CAS0 and CAS1 inputs from the SL9020 Data Controller for bank A is active LOW.
NCAS0B, 1B	104, 109	O	CAS0 and CAS1 for bank B is active LOW.
NCAS0B20, 1B20	103, 108	I	CAS0 and CAS1 inputs from the SL9020 Data Controller for bank B is active LOW.
NINTA	79	I	The interrupt acknowledge is an active LOW input from the PC/AT SL9011 System Controller.
NKBDCS	56	O	This active LOW signal is asserted to select the Keyboard Controller 8742.
NMI1	93	I	This is a Non Maskable Interrupt input from the PC/AT SL9011 System Controller.
NMI2	27	I	This pin can be used for any NMI source in order to generate NMI, e.g. power failure. It is active HIGH.
NMIOUT	38	O	NMI output connected to the CPU. It is active HIGH.
NRAS0-3	111, 113, 115, 117	O	Row address strobes for Banks 0, 1, 2 and 3 for the on board memory generated during the CPU or DMA cycles for memory access. It is active LOW.
NRAS0250-NRAS3250	112, 114, 116, 118	I	Row address strobes from the Memory Controller are active LOW.
NREFOUT	19	O	This active LOW signal is used to generate a refresh cycle for the DRAMs. This signal is not generated in the STANDBY wake up period.

PIN DESCRIPTION SL9095 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NREFRESH	57	I	Active LOW from the SL9030 Integrated Peripheral Controller. When asserted it indicates the DRAM refresh cycle.
NRESET	54	I	The NRESET is active LOW from the PC/AT SL9011 System Controller.
NRST8742	55	O	Active LOW Reset to 8742.
NRTCINT	37	I	This is the Real Time Clock input.
NVRAMSEL	18	I	This activates the ELPWR control pin. This will go HIGH for ELPWR to shutoff if Electroluminescence display is not accessed for the programmed time.
NXIOR	4	I	The peripheral bus input read is active LOW.
NXIOW	17	I	The peripheral bus output write is active LOW.
N386SX	28	I	This indicates if the CPU is 80286, 80386SX, or 80386DX. A LOW indicates a 80386SX or 80836DX.
N8042CS	52	I	This is the input signal from the SL9025 Address Controller. It is latched in STANDBY and active LOW.
OUT14MHZ	9	O	This Output has a buffered clock with the same frequency as the input IN14MHZ frequency.
PWRGOODI	119	I	The PWRGOODI is an active HIGH input from the power supply.
PWRGOODO	138	O	The PWRGOODO is an active HIGH output that generates the reset after STANDBY.
PWR0, PWR3-PWR7	92, 95 - 99	O	These outputs control the power supply of different device. They are active LOW in STANDBY. When active HIGH it indicates that the power is ON.
PWR1	78	O	This output controls the power on a device. It is active LOW in STANDBY. When active HIGH it indicates that the power is ON.
P26	33	I	This is the keyboard data input from the Keyboard Controller 8742.
P27	34	I	This is the keyboard data input from the Keyboard Controller 8742.

PIN DESCRIPTION SL9095 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
RST386	16	O	This is the CPU reset signal. It is not generated in STANDBY and it is active HIGH.
RST387	5	I	This input is active HIGH from the PC/AT SL9011 System Controller.
RUNAWAY	15	O	This output is generated if the CPU does not wake up after the sleep mode.
SERIAL 1	156	I	This is the interrupt from the first serial port.
SERIAL 2	158	I	This is the interrupt from the second serial port.
SLOWREF	82	I	Slow refresh DRAM. 1: Indicates that slow refresh DRAMs are used. 0: Indicates that regular DRAMs are used.
SMA0 - SMA9	123, 125, 127, 129, 131, 133, 135, 144, 146, 148	I	RAM address bus inputs from the SL9X5X Memory Controller.
SMA81	151	I	RAM address select input from the SL9X5X Memory Controller.
SPAREIN1	43	I	Spare input of the NAND Gate.
SPAREIN2	8	I	Spare input of the NAND Gate.
SPAREOUT	73	O	Spare output of the NAND Gate.
SPEAKER	63	O	This output is connected to the speaker.
SPKCLK	14	I	This CLK is used to generate an alarm.
SPKDATA	68	I	This is used with the SPKCLK to generate the speaker alarm.
STDBYCLK	11	O	This clock runs the programmable STDBY counter. (2 seconds)
STRTRST	3	I	This should be tied to VDD. This signal is used in simulation.
SYSCLK0	58	O	System clock out is a free running system clock generated by dividing CPUCLK by 2. It is conditioned by the NADS signal.

PIN DESCRIPTION SL9095 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
TEST	13	I	This signal is used to test the counters in simulation. This signal should be tied to VDD.
TIMCLK	69	O	This output has a buffered clock with a frequency 1/ 12th that of IN14MHZ (pin 74) frequency.
VDD	20, 40, 60, 80, 100, 120, 140, 160		+5V, Power.
VLSIHLDA	72	O	Active HIGH output which indicates that a bus cycle is granted in response to HOLD REQUEST.
VSS	1, 10,30, 41, 50 59, 70, 81, 90, 110, 121, 130, 139, 150		0V, Ground.
WARNING	137	O	This signal indicates low battery warning through either the speaker or LED.
XA0-XA15	23-26, 31, 32, 39, 44-48, 61, 62, 64, 67	I	Peripheral address bus inputs from the Address Controller SL9025.
XD0-XD7	83-89, 91	I/O	Peripheral Data Bus.

DC CHARACTERISTICS SL9095

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL	0.3VDD		V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = VS

NOTES:

* VIH = VDD, VIL = Vss

NRAS0 - NRAS3 = 24mA

CLK8042, OUT14MHz, MA0 - MA9, MA81
CLK29010, UDATA, KCLK, CLK2SX, CLK10D2
WARNING, TIMCLK, PWR0, ELPWR, PWR3-7, NCAS0A-NCAS1B = 12mA

RST386, LRST387, DRVRST, NRST8742 = 8mA

ALL OTHER OUTPUT = 3.2 mA

AC CHARACTERISTICS SL9095

(TA = 0° C to 70 ° C, VDD = 5V ± 5%)

Symbol	Description	Min.	Max.	Units
t1	CLK2 to CPUCLK (low to high)	1.1	3.8	ns
t2	CLK2 to CPUCLK (high to low)	1.1	3	ns
t3	CLK10D2 to SYSCLK (high to low)	3	5	ns
t4	CLK10D2 to SYSCLK (low to high)	2	5	ns
t5	NRAS0250-3250 to NRAS0-3 (high to low)		24	ns
t6	NRAS0250-3250 to NRAS0-3 (low to high)		16	ns
t7	NCAS(0A-1B) 9020 TO NCAS0A-1B (high to low)		14	ns
t8	NCAS(0A-1B) 9020 to NCAS0A-1B (low to high)		18	ns
t9	SMA0-SMA9 to MA0-MA9 Delay		18	ns
t10	CLK2SX to 386RST (high to low)	4	18	ns
t11	CLK2SX to L387RST (low to high)	4	18	ns
t12	CLK2SX to NDRVRST (low to high)	4	15	ns
t13	CLK2SX to NRST8742 (low to high)	4	15	ns
t14	SYSCLK to PERHLDA (low to high)	4	10	ns
t15	LSCPUHRQ to HOLD29010 (low to high)		14	ns
t16	LSCPUHRQ to HOLD9010 (high to low)		16	ns
t17	P26 to KCLK (low to high)		14	ns
t18	P26 to KCLK (high to low)		16	ns
t19	P27 to KDATA (low to high)		14	ns
t20	P27 to KDATA (high to low)		16	ns
t21	NBMW9250 to NBAMEMW (high to low)		18	ns
t22	NBMW9250 to NBAMEMW (low to high)		14	ns
t23	CLK Period	25		ns
t24	CLK High Duration	7		ns
t25	CLK Low Duration	7		ns
t26	XD_0-XD_7 Hold Time	8	20	ns

CONFIGURATION REGISTERS

The following registers are accessed by an indexing scheme, whereby the index value of the register to be accessed is written to I/O Port 22H, followed by the Data Information to I/O Port 23H. If the DEC SEL Pin is low, the I/O Port Address changes from Port 22H to Port A4EAH and from Port 23H to Port A4EBH.

INDEX: 02H - EL Counter Register or Backlit Power Register. (WRITE)

This register holds the counter value to turn off the DC-AC converter for the EL or to turn off the LCD Power and Backlit Power in case an LCD Display is being used.

D7	D6	D5	D4	D3	D2	D1	D0
EL CNT7	EL CNT6	EL CNT5	EL CNT4	EL CNT3	EL CNT2	EL CNT1	EL CNT0

BIT	FUNCTION
7-0	COUNTER VALUE (0-255) D0 = 1 Specifies 2 second Interval D0-7 = FF Specifies 8 Min. and 32 Secs. Intervals

INDEX: 03H - Standy Counter Register. (WRITE)

This register holds the counter value to turn off the PWR0-PWR7 signals when the system goes in stand-by.

D7	D6	D5	D4	D3	D2	D1	D0
STDBY CNT7							STDBY CNT0

BIT	FUNCTION
7-0	COUNTER VALUE (0-255) D0 = 1 Specifies 2 second Interval D0-7 = FF Specifies 8 Min. and 32 Secs. Intervals

CONFIGURATION REGISTERS

INDEX: 00 - Power Control Register. (WRITE)

This register holds the value of each power pin.

D7	D6	D5	D4	D3	D2	D1	D0
PWR 7							PWR 0

BIT	FUNCTION	
0	D0 = 0	PWR0 =OFF = 0
	D0 = 1	PWR0 = ON = 1
1	D1 = 0	PWR1 = OFF = 0
	D1 = 1	PWR1 = ON = 1
2	D2 = 0	DISPWR0 = OFF = 0
	D2 = 1	DISPWR1 = ON = 1
3	D3 = 0	PWR3 = OFF = 0
	D3 = 1	PWR3 = ON = 1
4	D4 = 0	PWR4 = OFF = 1
	D4 = 1	PWR4 = ON = 1
5	D5 = 0	PWR5 = OFF = 0
	D5 = 1	PWR5 = ON = 1
6	D6 = 0	PWR6 = OFF = 0
	D6 = 1	PWR6 = ON = 1
7	D7 = 0	PWR7 = OFF = 0
	D7 = 1	PWR7 = ON = 1

CONFIGURATION REGISTERS

INDEX: 01H - Start Count Register. (WRITE)

This register holds the value to start the count to turn off power pin PWR0-PWR7 in STANDBY.

D7	D6	D5	D4	D3	D2	D1	D0
TXD7	TXD6	TXD5	TXD4	TXD3	TXD2	TXD1	TXD0

0	D0 = 1	Starts down counting of EL Display or LCD Display counter register. DISPWR.
	DO = 0	No Down Count. DISP PWR = ON
1	D1 = 1	Starts down counting of stand-by counter. PWR0-PWR7 are turned off when counter reaches 0.
	D1 = 0	No DWN Counter. POWER = ON.
2	D2 = TXD2	SPARE.
3	D3 = TXD3 = NBLOCK	
	D3 = 1	Blocks the HOLD request to SL9010. (HOLD29010). When the Processor goes to HALT.
4	D4 = TXD4 = 1	PWR4 Pin will not be turned off in standby. PWR4 = 1
	D4 = TXD4=0	PWR4 Pin will be turned off in standby. PWR4 = 0.
5	D5 = TXD5 = 1	PWR5 Pin will not be turned off in standby. PWR5 = 1
	D5 = TXD5 = 0	PWR5 Pin will be turned off in standby.
6	D6 = TXD6 = 1	PWR6 Pin will not be turned off in standby.
	D6 = TXD6 = 0	PWR6 Pin will be turned off in standby.
7	D7 = TXD7 = 1	PWR7 Pin will not be turned off in standby.
	D7 = TXD7 = 0	PWR7 Pin turned off in standby.

CONFIGURATION REGISTERS

INDEX: 01H - Status Register. (READ)

This register holds the status of several pins.

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

XD0 = 1 **NMI2 is On. (Nonmaskable Interrupt)X**

XD1 = 2 **Slow Refresh DRAMs are used.**

XD2 = **Space.**

XD3= **Space.**

XD4=1 **AC Power On.**

XD5=0 **Battery Low.**

XD6=1 **EL Display Power is On.**

XD7=1 **Power 3 Pin is On (Hard Disk).**

AC TIMING DIAGRAMS SL9095

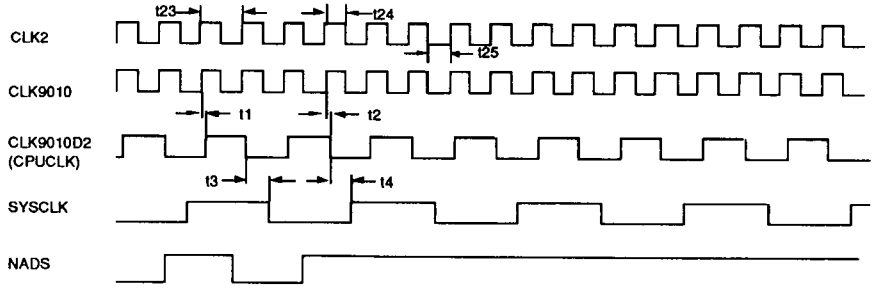


FIG. 1 CLK DURATION AND DELAYS FROM CLK2 OR CPUCLK.

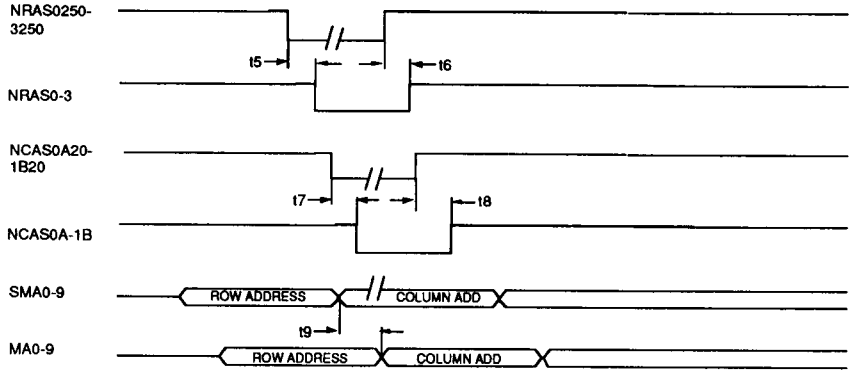


FIG. 2 OUTPUT SIGNAL DELAYS FROM INPUTS.

AC TIMING DIAGRAMS SL9095

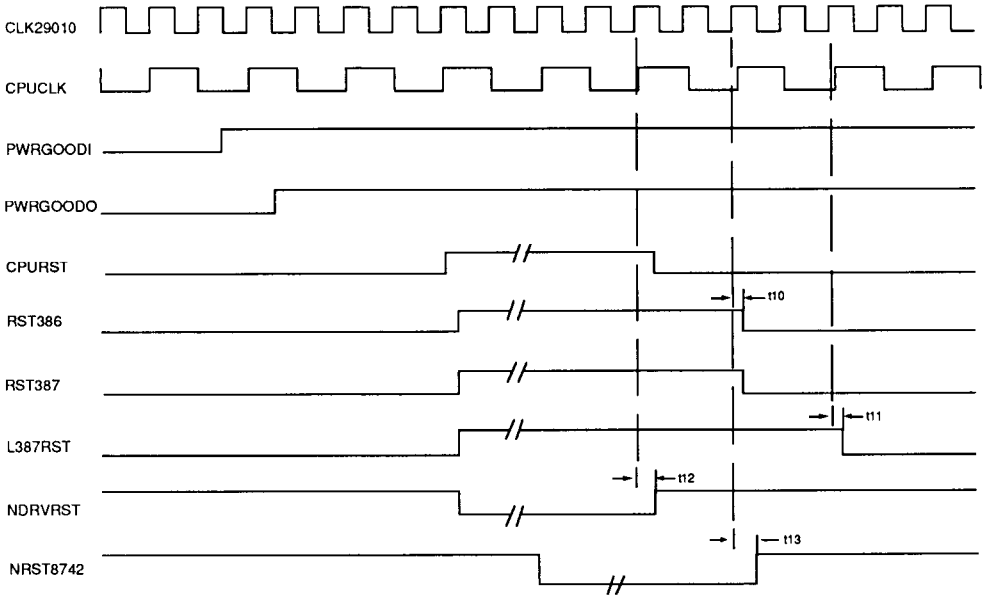


FIG. 3 RST386, L387RST andNRST8742 DELAYS FROM INPUTS AND CPUCLK

AC TIMING DIAGRAMS SL9095

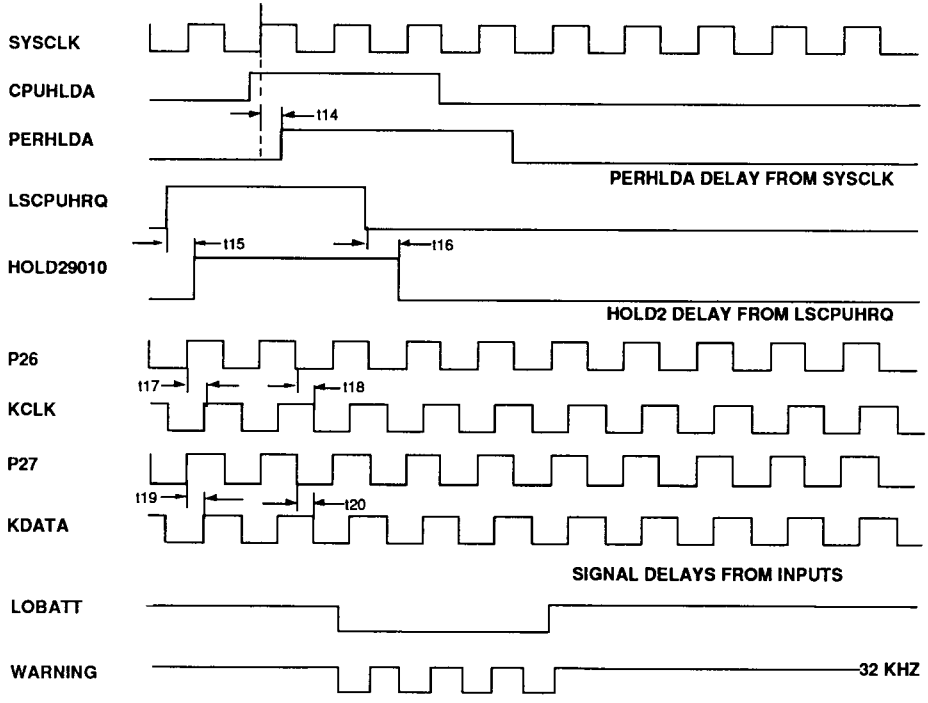


FIG. 4 WARNING SIGNAL TO SPEAKER

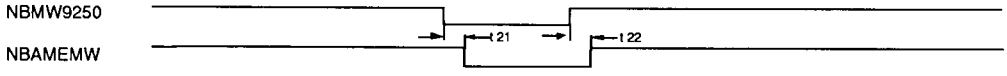


FIG. 5 NBAMEMW SIGNAL DELAYS FROM INPUT NBMW9250.

AC TIMING DIAGRAMS SL9095

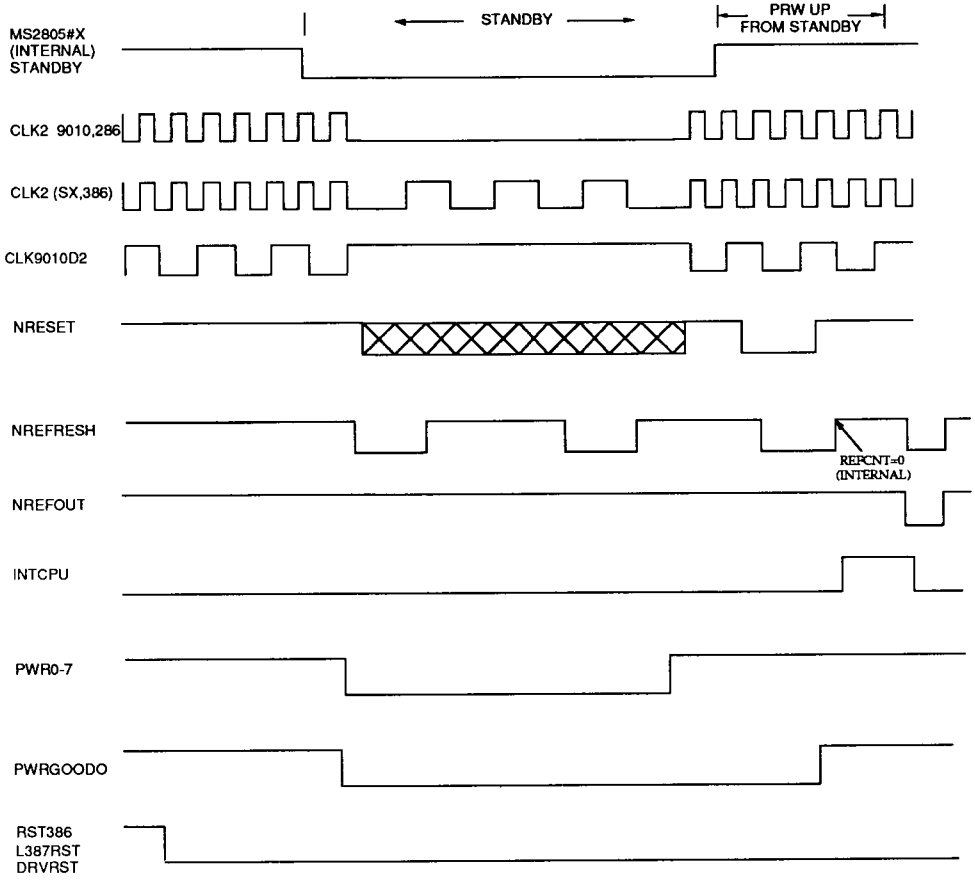


FIG. 6 STANDBY CYCLE TIMINGS

AC TIMING DIAGRAMS SL9095

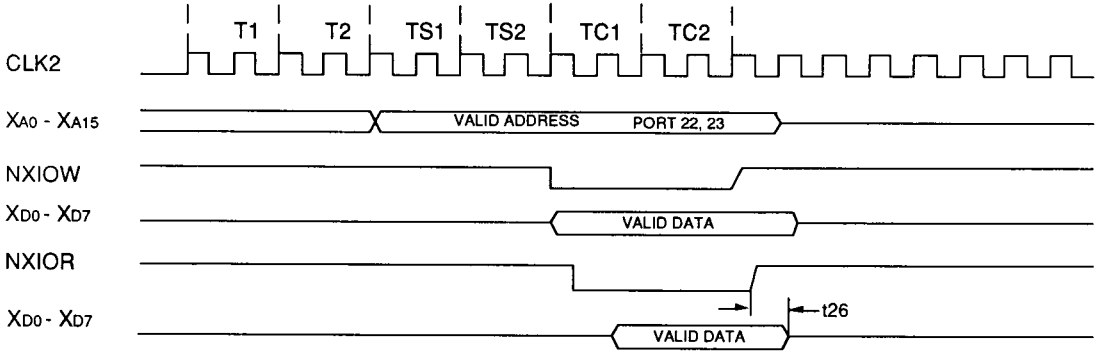


FIG. 7 EXTERNAL I/O CYCLE.