FEATURES

- **Supports 80286, 80386SX (P9), 80386DX, and 80486-based AT Designs.**
- **Address In to Address Out: 15 ns.**
- **Up to 25 MHz Performance.**
- **24 mA Buffers.**
- **Include SA & XA Buffers.**
- **Includes XD to XA Transfer Latches.**
- **Provides Refresh for 256K, 1M or 4Mbit DRAM Chips.**
- **Includes Port B, I/O Decode and NMI Logic.**
- **Advanced CMOS Technology.**
- **100 pin Flatpack.**

DESCRIPTION

The SL9025 Address Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

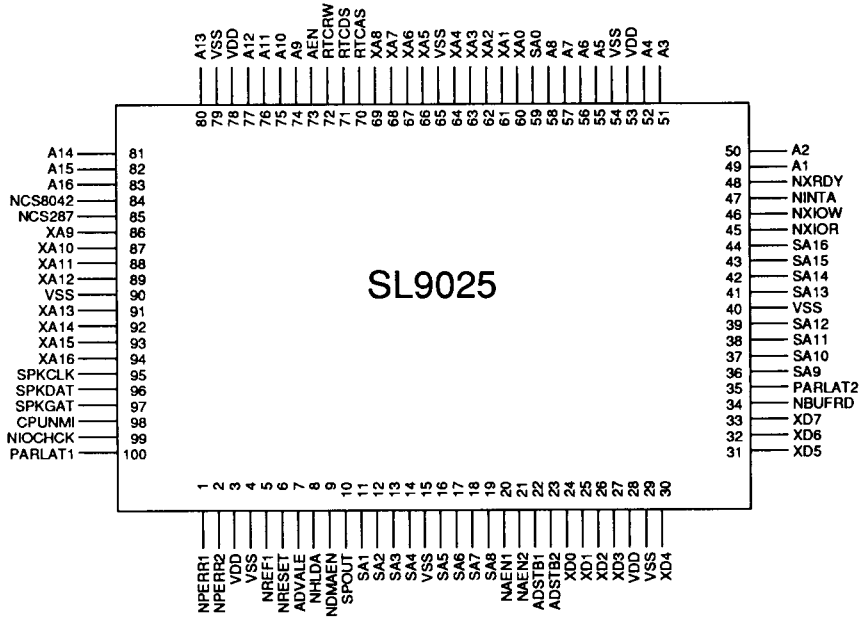
The SL9025 is part of the Core AT Logic chips that implement the system logic common to 80286, 80386SX, 80386DX and 80486-based PC/AT designs. It supports up to 25 MHz performance. In addition to the SL9025, the Core AT Logic chips consists of the SL9011 System Controller, the SL9020 Data Controller, the SL9030 Integrated Peripheral Controller and the 9X5X Memory Controller.

It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

SL9025 is a general purpose address controller for PC/AT. It can be used with 16 or 32 bit CPUs including 80286, 80386SX, 80386DX or 80486. The device includes all necessary latches, buffers, and drivers for CPU Address Bus (A-Bus), System Address Bus (SA-Bus), and Peripheral Address Bus (XA-Bus). In addition, Port-B, NMI, Parity Latch and I/O Decode Logic as well as Refresh for 256K, 1M or 4M DRAMs is provided. Optional XD to XA transfer latches are also provided.

High drive buffers (12mA-24mA) are provided for full PC/AT compatibility.

PINOUT


SL9025
1 NPERR1
2 NPERR2
3 VDD
4 VSS
5 NREF1
6 NRESET
7 ADVALE
8 NHLDA
9 NDMAEN
10 SPOUT
11 SA1
12 SA2
13 SA3
14 SA4
15 VSS
16 SA5
17 SA6
18 SA7
19 SA8
20 NAEN1
21 NAEN2
22 ADSTB1
23 ADSTB2
24 XD0
25 XD1
26 XD2
27 XD3
28 VDD
29 VSS
30 XD4
31 XD5
32 XD6
33 XD7
34 NBUFRD
35 PARLAT2
36 SA9
37 SA10
38 SA11
39 SA12
40 VSS
41 SA13
42 SA14
43 SA15
44 SA16
45 NXIOR
46 NXIOW
47 NINTA
48 NXRDY
49 A1
50 A2
51 A3
52 A4
53 VDD
54 VSS
55 A5
56 A6
57 A7
58 A8
59 SA0
60 XA0
61 XA1
62 XA2
63 XA3
64 XA4
65 VSS
66 XA5
67 XA6
68 XA7
69 XA8
70 RTCAS
71 RTCDS
72 RTCRW
73 AEN
74 A9
75 A10
76 A11
77 A12
78 VDD
79 VSS
80 A13
81 A14
82 A15
83 A16
84 NCS8042
85 NCS287
86 XA9
87 XA10
88 XA11
89 XA12
90 VSS
91 XA13
92 XA14
93 XA15
94 XA16
95 SPKCLK
96 SPKDAT
97 SPKGAT
98 CPUNMI
99 NIOCHCK
100 PARLAT1

PORT B AND NMI LOGIC

Port "B" at I/O address 64H is fully IBM compatible. Read/Write bit definitions are as shown below in Table 1.

BIT	R	W
0	Speaker Gate	Speaker Gate
1	Speaker Data	Speaker Data
2	XD2	Reset Parity Latch
3	XD3	Reset I/O Chck Latch
4	REFRESH 0	XD4
5	Speaker Clock	XD5
6	I/O Channel Check	XD6
7	Parity Error	NMI Enable

Table 1

Parity error signals NPERR1 and NPERR2 are logically ored together and latched by a low to high transition on PARLAT1 or PARLAT2 inputs. The parity latch is held reset by writing a 1 to Bit 2. Parity error inputs on Port B Bit 7.

I/O channel check (NIOCHCK) is latched on a low transition, and is held clear by writing a 1 to Bit 3. It is input on Bit 6.

Latched parity error and I/O channel check are ored together and gated out with write Bit 7 to produce a CPUNMI (CPU non-maskable interrupt).

DMA

8237 compatible DMA support logic is comprised of two 8 Bit latches and two 8 Bit multiplexers. Reference the DMA section of the Block Diagram.

A low to high transition on ADSTB1 latches 8 Bit DMA most significant address byte from XD Bus into XD8 latch. Likewise, a low to high transition on ADSTB2 latches 16 Bit DMA most significant address byte from SD bus into SD16 latch.

If the transfer is an 8 Bit DMA, input NAEN1 is asserted causing the DMA Mux to switch SD8 latch data onto the SA Bus Mux and the A Bus Mux. If the transfer is a 16 Bit DMA, input NAEN2 is asserted causing the DMA Mux to switch SD16 latch data onto the S Bus Mux and the A Bus Mux.

I/O DECODE LOGIC

The I/O decode logic provides the chip selects and strobes for the NPX, NMI, Port B, Keyboard Controller and the RTC. Reference the I/O Decode Logic portion of the Block Diagram. The direction enable signal NBUFRD, used by the SL9020 Data Controller, is also provided.

Input SPOUT is used to gate NXIOR onto NBUFRD. Address inputs XA0, 4, 5, 6, 7, 8, 9 and AEN are selectively used to decode the external selects NCS287 and NCS8042, the strobes RTCAS, RTCDS, RTCRW and NBUFRD, as well as the internal strobes NMICK, PBRD and PBWT. Input NXIOR strobes NBUFRD, RTCDS and PBRD. The input NXIOW strobes NMICK, RTCRW and PBWR. NXRDY qualifies NMICK and the output RTCAS.

BUS MULTIPLEXERS/DIRECTION CONTROL

The bus multiplexers and direction control logic provides the necessary gating and arbitration to:

1. The XA and SA Bus with system address during CPU I/O and memory operations
2. DMA address during DMA transfers
3. Refresh address to A and SA Buses at Refresh time

The direction control logic uses the inputs NHLDA, NDMAEN, NAEN1, NAEN2 and NREF1 to generate the I/O internal Mux selection and output buffer enable signals; X TO S, X TO A, S TO A, S TO X, A TO X, XR TO S, NENA, NENS, NENXL, NENXH. Refer to Table 2 for the allowed transfer directions.

REFRESH COUNTER/MULTIPLEXER

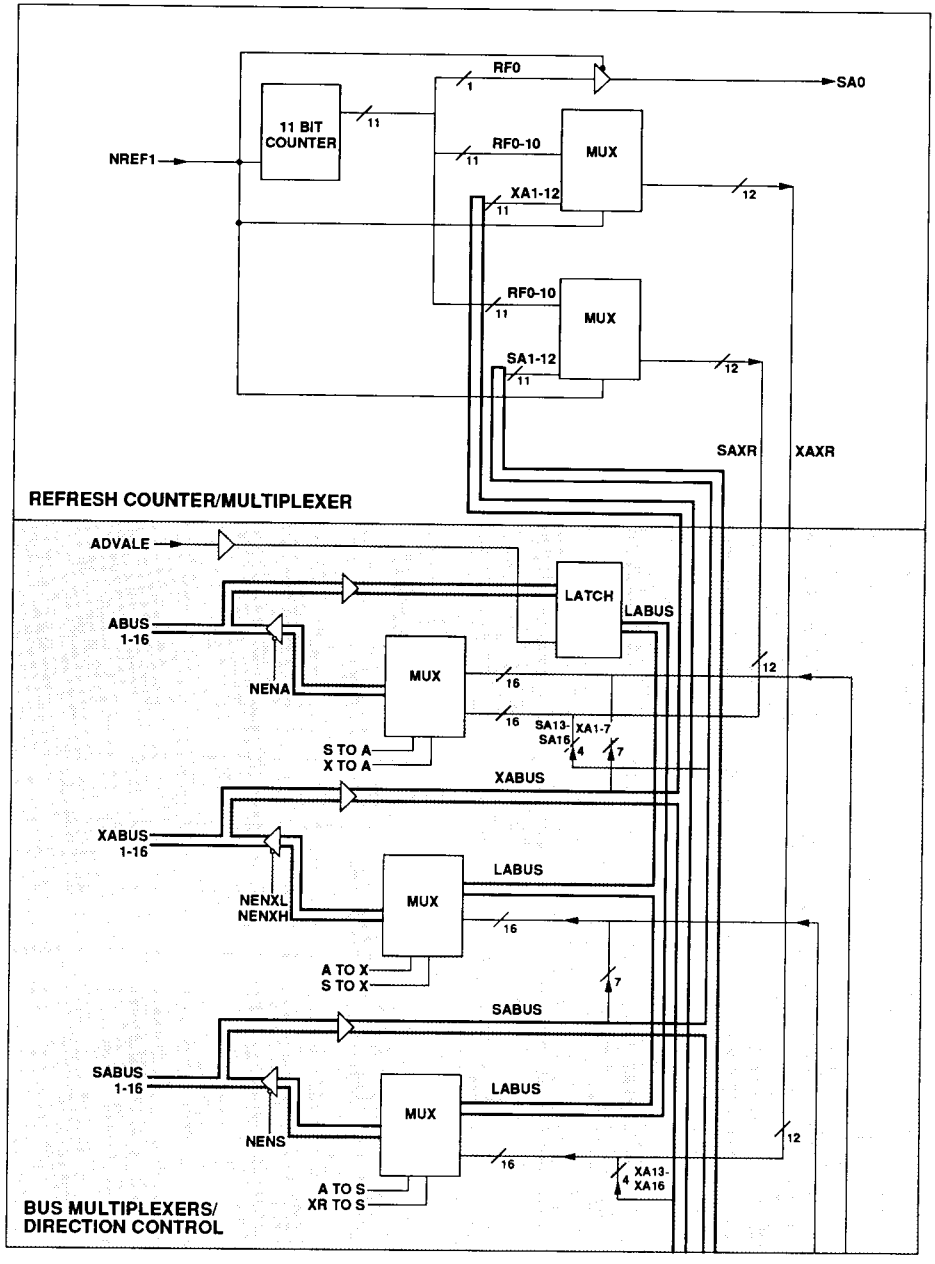
The Refresh Counter/Multiplexer consists of an eleven bit Counter and two 12 Bit Multiplexers.

When NREF1 is true, the 11 Bit Counter is advanced, and the output address is Muxed and enabled onto the A Bus and SA Bus.

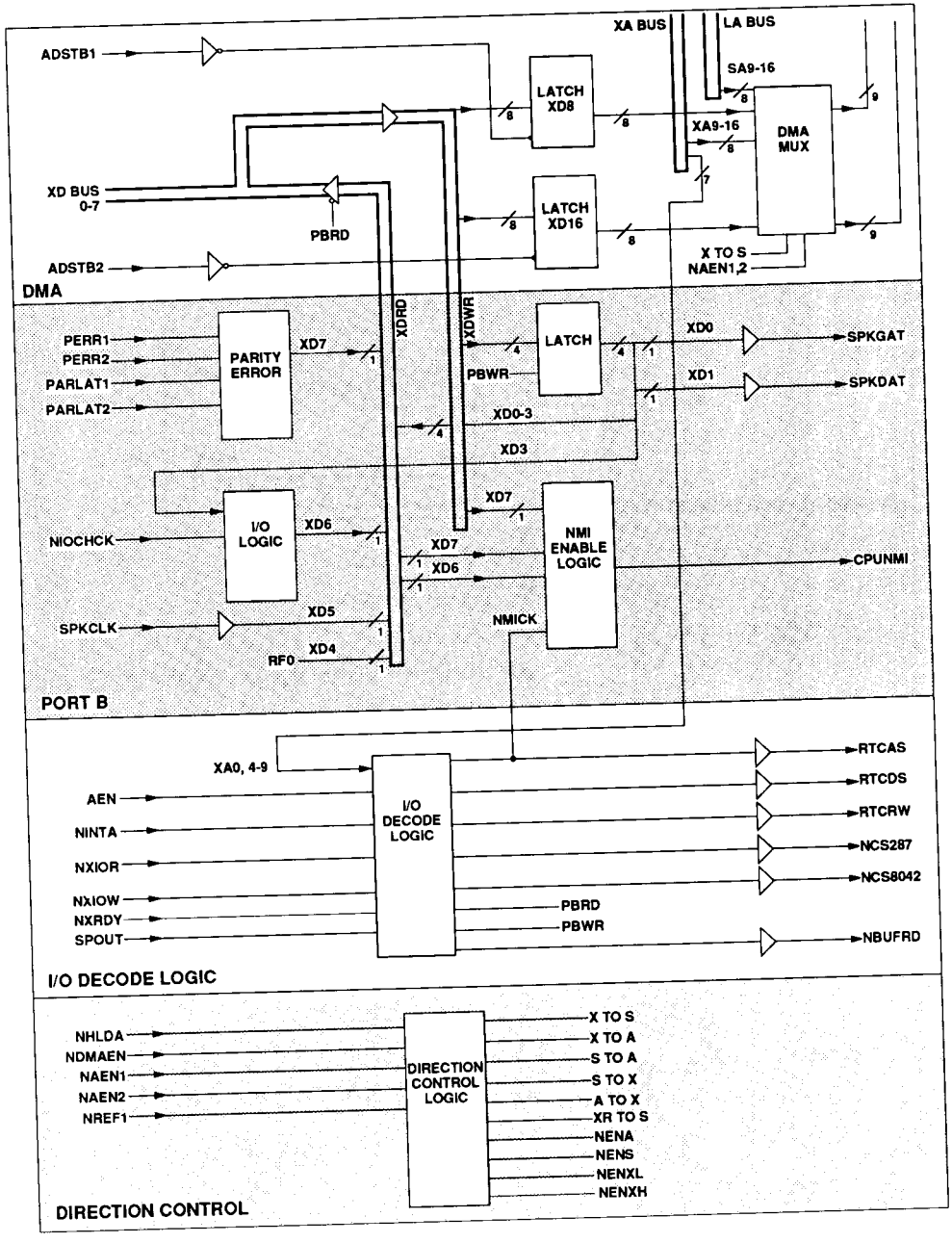
SYSTEM FUNCTION	NHLDA	NDMAEN	AEN1,2	REF1	NAENA	NENS	NENXL	NENXH	S TO A	A TO S	XR TO S	X TO S	S TO X	X TO A	A TO X
DMA	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0
I/O REFR	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0
LOC REFR	0	1	0	1	0	0	0	0	1	0	1	0	1	0	0
CPU R/W	1	1	0	0	1	0	0	0	0	1	0	0	1	0	1

Table 2

BLOCK DIAGRAM SL9025



BLOCK DIAGRAM SL9025 (Cont'd)



PIN DESCRIPTION SL9025

SYMBOL	PIN	TYPE	DESCRIPTION
A1-A16	49,50,51,52, 55,56,57,58, 74,75,76,77, 80,81,82,83	I/O	CPU Address Bus.
ADSTB1,2	22,23	I	Address Strobes to latch XD data from DMA controllers to XA Bus. ADSTB1 is active for 8-bit DMA transfers while ADSTB2 is active for 16-bit DMA transfers. Tied HIGH if the SL9030 Integrated Peripheral Controller is used.
ADVALE	7	I	Advance Address Latch Enable from memory controller. It latches local bus address for the system bus on the LOW to HIGH transition.
AEN	73	I	Address Enable, HIGH for DMA cycles. Prevents DMA from accessing on-board peripherals. When LOW, enables data buffers between XD Bus and SD Bus.
CPUNMI	98	O	CPU Non-Maskable Interrupt, generated from PERR or IOCHCK. Output to 80X86.
NAEN1,2	20,21	I	Address Enable 1 and 2, from discrete DMA controller. Assertion allows DMA XD data to tie to XA Bus. Tied HIGH if the SL9030 Integrated Peripheral Controller is used.
NBUFRD	34	O	Direction control for data buffer between SD Bus and XD Bus. Drives the SL9025 Data Controller signal NBUFRD.
NCS287	85	O	Active LOW Numeric Processor Chip Select to NXP.
NCS8042	84	O	Active LOW Keyboard Controller Chip Select to 8042.
NDMAEN	9	I	DMA Enable from the SL9011 System Controller. When LOW, indicates a DMA cycle: XA1-XA16 is gated onto SA1-SA16.
NHLDA	8	I	Hold Acknowledge. When asserted by CPU, indicates that the CPU has released the bus. It is used to direction address bits 1-16 to/from A Bus/SA Bus.
NINTA	47	I	Interrupt Acknowledge from the SL9011 System Controller. It is used to gate NBUFRD.
NIOCHCK	99	I	I/O Channel Check. Active LOW signal from the AT bus. When LOW it indicates an I/O channel fault.

PIN DESCRIPTION SL9025 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
NPERR1,2	1,2	I	Parity Error from lower and upper 16 bit RAM, from the SL9020 Data Controller.
NREF1	5	I	Refresh cycle clock from SL9011 pin REFCLK. It is used to clock RAM Row Address during Refresh.
NRESET	6	I	Systems Reset. Active LOW, from the SL9011 System Controller.
NXIOR	45	I	X Bus I/O Read.
NXIOW	46	I	X Bus I/O Write.
NXRDY	48	I	X Ready from the SL9011 System Controller. When LOW, indicates a peripheral bus cycle termination. (End of T2 data phase.) It is used to qualify RTCAS.
PARLAT1,2	100,35	I	Parity error is latched on rising edge of either PARLAT1 or PARLAT2 while the other is LOW. Connects to 9X5X pins NBMR and NCAS.
RTCAS	70	O	Active HIGH Real Time Clock Address Strobe to RTC.
RTCDS	71	O	Active HIGH Real Time Clock Data Strobe to RTC.
RTCRW	72	O	Active HIGH Real Time Clock Read Cycle/Write Cycle input to RTC.
SA0	59	O	System Bus Address A0.
SA1-SA16	11,12,13,14, 16,17,18,19, 36,37,38,39, 41,42,43,44	1/O	System Address Bus.
SPKCLK	95	I	Speaker Clock from the SL9030 Integrated Peripheral Controller.
SPKDAT	96	O	Speaker Data active HIGH output used to gate the timer tone signal to the speaker.
SPKGAT	97	O	Speaker Gate. Enables timer tone signal to the speaker.
SPOUT	10	I	Serial Parallel port decode. Usually tied LOW. A logical 1 in will enable NBUFRD during NXIOR.
VDD	3,28,53,78	-	+5V. Power.

PIN DESCRIPTION SL9025 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
VSS	4,15,29,40, 54,65,79,90	-	0V. Ground.
XA0	60	I	Peripheral Bus Address A0.
XA1-XA16	61,62,63,64, 66,67,68,69, 86,87,88,89, 91,92,93,94	I/O	Peripheral Address Bus.
XD0-XD7	24,25,26,27, 30,31,32,33	I/O	Peripheral Data Bus.

ABSOLUT MAXIMUM RATINGS SL9025 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current *note 2	I_{OS}	-40	+40	mA
Output Current *note 3	I_{OS}	-40	+80	mA
Output Current *note 4	I_{OS}	-60	+120	mA
Output Current *note 5	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. All others.
3. A1-A16.
4. XA1-XA16.
5. SA0-SA16.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9025

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL		0.3VDD	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = VSS

NOTES:

* VIH = VDD, VIL = Vss

SA0-SA16	= 24mA buffers	(typical)
XA1-XA16	= 12mA buffers	
A1-A16	= 8mA buffers	
All others	= 3.2 mA buffers	

AC CHARACTERISTICS SL9025

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	ADVALE to System Address Bus Delay	8	20	ns
t2	ADVALE to Peripheral Address Bus Delay (XA Bus)	8	20	ns
t4	System Address Bus to Peripheral Address Bus Delay (XA Bus)	8	15	ns
t5	System Address Bus to CPU Address Bus Delay	8	15	ns
t6	Peripheral Address Bus to System Address Bus Delay	8	15	ns
t7	Peripheral Address Bus to CPU Address Bus Delay	8	15	ns
t8	NREF1 Active to Peripheral Address Bus Valid Delay	8	40	ns
t9	NREF1 Active to System Address Bus Delay	8	40	ns
t10	NREF1 Active to Memory Address Bus Delay	8	40	ns
t11	NREF1 In-Active to System Address Bus Hi-Z Delay	8	20	ns
t12	NREF1 to SA0 Valid Delay	6	15	ns
t13	NREF1 to SA0 Hi-Z Delay	6	15	ns
t14	NAEN1,2 to Peripheral Address Bus Valid Delay	6	15	ns
t15	NAEN1,2 to Peripheral Address Bus Hi-Z Delay	6	15	ns
t16	Peripheral Data Bus to Peripheral Address Bus Delay	8	20	ns

AC TIMING DIAGRAMS SL9025