FEATURES

- **Supports 80286, 80386SX, 80386DX, and 80486-based AT Designs.**
- **Data In to Data Out: 15 ns.**
- **24 mA Output Buffers for SD Bus.**
- **Includes MD, SD & XD Buffers.**
- **16 bit Data Path can be Used as Low or High Buffer.**
- **Two SL9020 are Used in Tandem to Support 32 bit Data Bus.**
- **Low to High byte Transfer.**
- **Latches Provided for Cache Designs.**
- **Fast Memory to CPU Data Path.**
- **Advance CMOS Technology.**
- **100 pin Flatpack.**

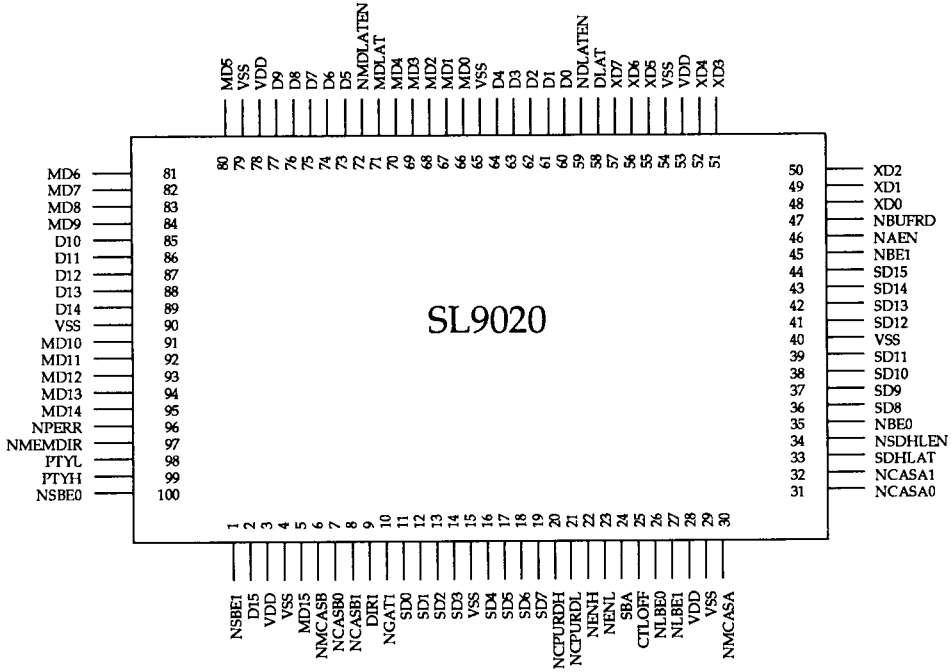
DESCRIPTION

The SL9020 Data Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system logic.

The SL9020 is part of the Core AT Logic chips that implement the system logic which is common to all microprocessors such as 80286, 80386SX, 80386DX and 80486-based PC/AT designs and supports up to 25 MHz performance. In addition to the SL9020, the Core AT Logic chips consists of the SL9011 System Controller, the SL9025 Address Controller, the SL9030 Integrated Peripheral Controller and the SL9X5X Memory Controller.

It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

PINOUT


SL9020
1 NSBE1
2 D15
3 VDD
4 VSS
5 MD15
6 NMCASB
7 NCASB0
8 NCASB1
9 DIR1
10 NGAT1
11 SD0
12 SD1
13 SD2
14 SD3
15 VSS
16 SD4
17 SD5
18 SD6
19 SD7
20 NCPURDH
21 NCPURDL
22 NENH
23 NENL
24 SBA
25 CTLOFF
26 NLBE0
27 NLBE1
28 VDD
29 VSS
30 NMCASA
31 NCASA0
32 NCASA1
33 SDHLAT
34 NSDHLEN
35 NBE0
36 SD8
37 SD9
38 SD10
39 SD11
40 VSS
41 SD12
42 SD13
43 SD14
44 SD15
45 NBE1
46 NAEN
47 NBUFRD
48 XD0
49 XD1
50 XD2
51 XD3
52 XD4
53 VDD
54 VSS
55 XD5
56 XD6
57 XD7
58 DLAT
59 NDLATEN
60 D0
61 D1
62 D2
63 D3
64 D4
65 VSS
66 MD0
67 MD1
68 MD2
69 MD3
70 MD4
71 MDLAT
72 NMDLATEN
73 D5
74 D6
75 D7
76 D8
77 D9
78 VDD
79 VSS
80 MD5
81 MD6
82 MD7
83 MD8
84 MD9
85 D10
86 D11
87 D12
88 D13
89 D14
90 VSS
91 MD10
92 MD11
93 MD12
94 MD13
95 MD14
96 NPERR
97 NMEMDIR
98 PTYL
99 PTYH
100 NSBE0

DESCRIPTION (Cont'd.)

The SL9020 provides the data buffer latches and drivers for a 16-bit data path for PC/AT using 80286 and 80386SX type processor. Two SL9020 can be used to construct a 32-bit data path for PC/AT's using an 80386DX microprocessor.

Control logic and drivers for the chip includes CPU Data Bus (D Bus), Memory Data Bus (MD Bus), System Data Bus (SD Bus) and Peripheral Data Bus (XD Bus). The SL9020 also performs parity generation/checking, low to high byte transfer on SD Bus and drivers for low and high byte Column Address Strobes (CAS) for two independent memory banks. Latched CPU Byte enable (BHE0 & BHE1) are also provided.

All Data bus outputs are capable of high drive (12-24mA) and have fast rise & fall times of 5ns.

Latches are also provided on D to MD, MD to D, and SD to D paths.

MD/D LOW BYTE BUFFER/LATCH

Data is transferred from MD0-7 to D0-7 or D0-7 to MD0-7 Bus via the MD/D low byte buffer/latch. The transfer direction is set MD to D by asserting NMEMDIR low. Deasserting NMEMDIR sets transfer directions D to MD. NSBE0 enables the MD or D bus low byte output buffers, and hence must be asserted to allow data to be driven onto the selected bus.

Transparent input data latches are provided on both D0-D7 and MD0-MD7 busses. Asserting DLAT high enables D0-D7 data to pass through latches. Deasserting DLAT latches D0-D7 data. Latched D0-D7 data or D0-D7 data is selected by asserting/deasserting NDLATEN. Similarly, asserting MDLAT high enables MD0-MD7 data to pass through latches. Deasserting MDLAT latches D0-D7 data. Latched MD0-MD7 data or MD0-MD7 data is selected by asserting/deasserting NMDLATEN.

MD/D HIGH BYTE BUFFER/LATCH

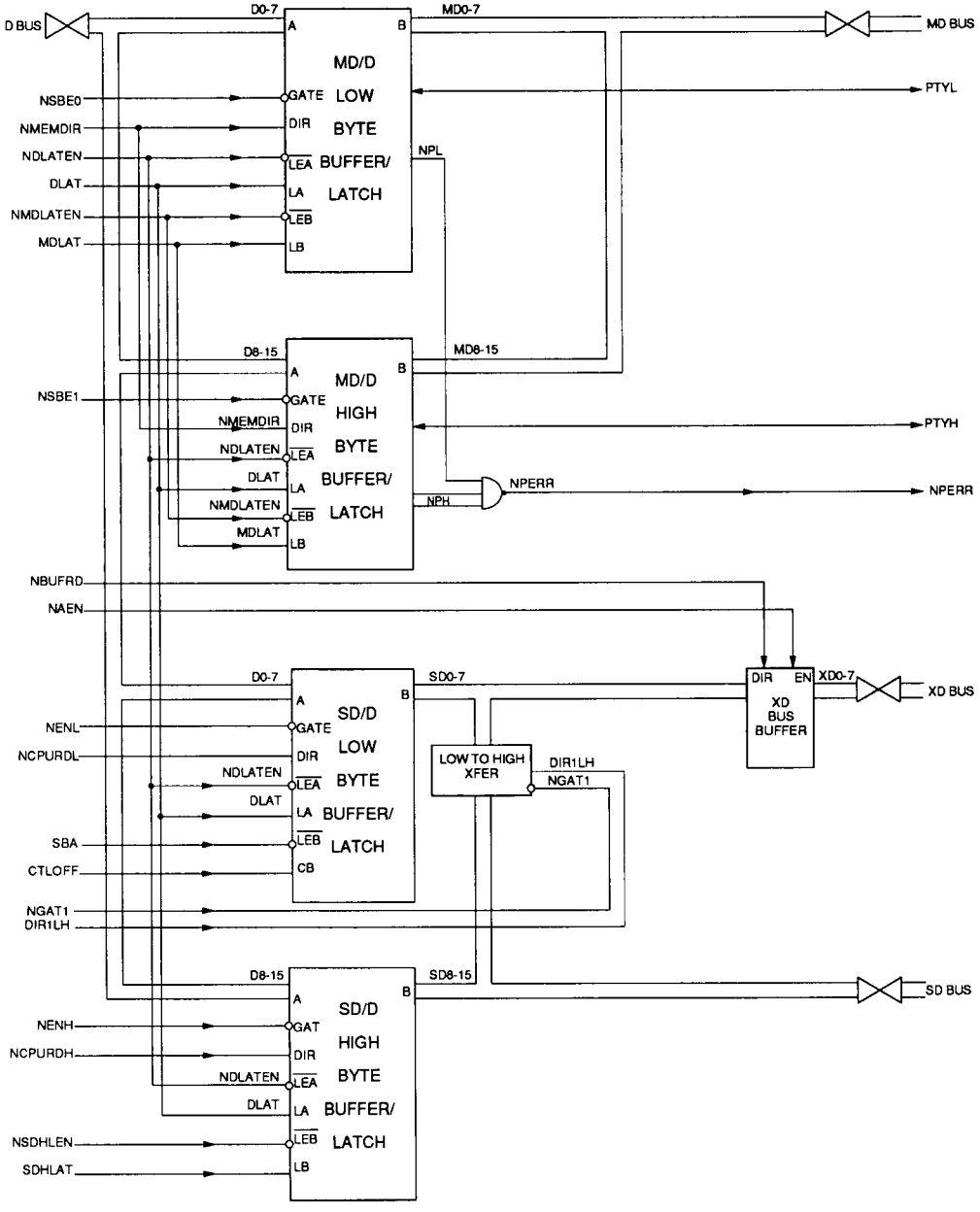
Data is transferred from the MD8-MD15 bus to the D8-D15 bus or from the D8-D15 bus to the MD8-MD15 bus via the MD/D high byte buffer/latch. Both direction (NMEMDIR) and latch controls (DLAT, NDLATEN, MDLAT, NMDLATEN) operate on high byte identically as they would on low byte. Reference MD/D low byte buffer latch. NSBE1 enables the MD or D bus high byte output buffers.

SD/D LOW BYTE BUFFER/LATCH

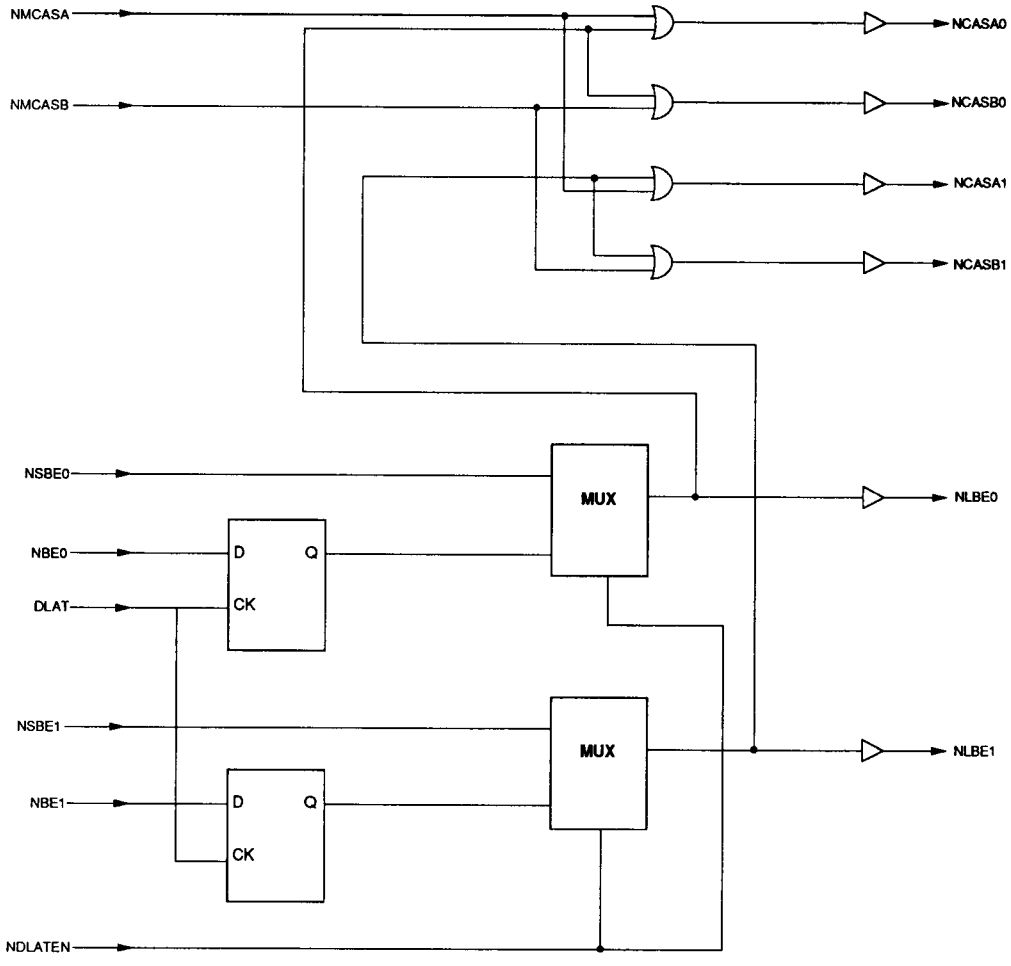
Data is transferred from SD0-SD7 bus to D0-D7 bus or from D0-D7 bus to SD0-SD7 bus via the SD/D low byte buffer/latch. The transfer direction is set SD to D by asserting NCPURDL low. Deasserting NCPURDL sets transfer direction D to SD. NENL enables the SD or D bus low byte output buffers, and hence must be asserted low to allow data to be driven onto the selected bus.

Input data latches are provided on both D0-D7 and SD0-SD7 busses. Asserting DLAT high enables D0-D7 data to pass though latches. Deasserting DLAT latches D0-D7 data. Latched D0-D7 data or D0-D7 data is selected by asserting/deasserting NDLATEN. Similarly, the low to high edge of CTLOFF latches SD0-SD7 data. Latched SD0-SD7 data or SD0-SD7 data is selected by asserting/negating SBA.

BLOCK DIAGRAM SL9020



BLOCK DIAGRAM SL9020 (Cont'd.)



CAS Buffer Logic

SD/D HIGH BYTE BUFFER/LATCH

Data is transferred from SD8-SD15 Bus to D8-D15 Bus or from D8-D15 Bus to SD8-SD15 Bus via the SD/D high byte buffer/latch. The transfer direction is set SD to D by asserting NCPURDH low. Deasserting NCPURDH sets transfer direction D to SD. NENH enables the SD or D bus high byte output buffers, and hence must be asserted low to allow data to be driven onto the selected bus.

Input data latches are provided on both D8-D15 and SD8-SD15 busses. Asserting DLAT high enables D8-D15 data to pass through latches. Deasserting DLAT latches D8-D15 data. Latched D8-D15 data or D8-D15 data is selected by asserting/deasserting NDLATEN. The low to high edge of SDHLAT latches SD8-SD15 data. Latched SD8-SD15 data or SD8-SD15 data is selected by negating/asserting NSDHLEN.

SD LOW BYTE TO SD HIGH BYTE TRANSFER

Low byte to high byte SD bus transfers (byte to word) are effected through the SD low byte to high byte transfer logic, asserting DIR1LH directs SD0-SD7 onto SD8-SD15. Asserting NGAT1 enables the SD buffers. If DIR1LH is deasserted, transfer will occur from high byte to low byte.

XD BUS BUFFER

Data is transferred from XD0-XD7 bus to SD0-SD7 bus or from SD0-SD7 bus to XD0-XD7 bus via the XD bus buffer. The transfer direction is set XD to SD bus by asserting NBUFRD low. Deasserting NBUFRD sets direction of transfer SD to XD bus. NAEN enables the XD or SD bus buffers and hence must be asserted low to allow data to be driven onto the selected bus.

CAS BUFFER LOGIC

The CAS Buffer Logic "demultiplexes" the NMCASA and NMCASB inputs from the memory controller, generating 24ma drive CAS lines for 2 Banks (A and B) high byte and low byte: NCASA0, NCASB0, NCASA1, NCASB1. Inputs NSBE0, NSBE1, NBE0, NBE1, NDLATEN, NMCASA and NMCASB are inputs to the CAS logic. NDLATEN, when asserted low, selects NBE0/NBE1 latched outputs to gate out NCASX0/NCASX1. NDLATEN is also used to gate NSBE0/NSBE1 or NBE0-NBE1 (latched with rising DLAT) into the outputs NLBE0/NLBE1. When NDLATEN is asserted low, it selects latched NBE0/NBE1 for outputs.

PARITY GENERATION/CHECK

The parity generation and checking logic is included within the low and high byte buffer/latches. Even parity is checked looking at MD0-MD7 and PTYL for the high byte, and looking at MD8-MD15 and PTYH for the high byte. The low byte/high byte parity check outputs NPL and NPH are gated with NBE0 and NBE1 respectively and logically ored together with NMDIRIN to produce the parity error output NPERR. Parity is generated during write cycles when NMEMDIR is negated high. The low byte output PTYL, is even parity generated from D0 through D7. Similarly, the high byte output, PTYH, is even parity generated from D8 through D15.

PIN DESCRIPTION SL9020

SYMBOL	PIN	TYPE	DESCRIPTION
CTLOFF	25	I/O	Rising edge clocks data from SD [7:0] to D[7:0] latches during Bus-conversion cycles.
D0-D15	60,61,62,63,64 73,74,75,76,77 85,86,87,88,89,2	I/O	16 Bit local data Bus.
DIR1	9	I	Direction 1. When asserted HIGH, directs data from SD[7:0] to SD[15:8]. DIR1 is enabled by NGAT1.
DLAT	58	I	Latches local bus data when Pulled LOW. Should be left un-connected for non-cache-based designs. Latches NBE0, NBE1.
MD0-MD15	66,67,68,69,70 80,81,82,83,84 91,92,93,94,95,5	I/O	16 Bit Memory data Bus.
MDLAT	71	I	Latches MD Bus data when pulled LOW. Should be left un-connected for non-cache-based designs.
NAEN	46	I	Asserting NAEN LOW enables data buffers between XD Bus & SD Bus.
NBE0,1	35,45	I	Active LOW Byte Enable signals. Inputs to BE0/BE1 latch for CAS demultiplexing. Not normally used in an AT structure, should be pulled-up.
NBUFRD	47	I	Direction control for XD Bus Buffer. When asserted LOW, transfer is from XD to SD.
NCASA0	31	O	CAS for bank A LS byte.
NCASA1	32	O	CAS for bank A MS byte.
NCASB0	7	O	CAS for bank B LS byte.
NCASB1	8	O	CAS for bank B MS byte.
NCPURDH	20	I	HIGH byte direction control between D Bus and SD Bus. When LOW, direction is from SD Bus to D Bus.
NCPURDL	21	I	LOW Byte direction control between D Bus and SD bus. When LOW, direction is from SD Bus to D Bus.

PIN DESCRIPTION SL9020 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
NDLATEN	59	I	Data Latch Enable. Selects latched D Bus/D Bus data when LOW/HIGH. It also selects NBE0,1 or NSBE0,1 for use in demultiplexing CAS inputs. Should be left un-connected for non-cache-based designs.
NENH	22	I	Active LOW. HIGH Byte data transfer enable between D Bus and SD Bus from SL9011 System Controller.
NENL	23	I	Active LOW. LOW Byte data transfer enable between D Bus and SD Bus from SL9011 System Controller.
NGAT1	10	I	When LOW, enables byte transfer between SD Bus' LOW and HIGH bytes.
NLBE0,1	26,27	O	Latched Byte enable outputs. When NDLATEN is asserted, the latched inputs NBE0/NBE1 (latched by LOW to HIGH transition on DLAT) are buffered out on NLBE0/NBLE1. When NDLATEN is negated, the inputs NSBE0/NSBE1 are buffered out on NLBE0/NLBE1.
NMCASA	30	I	Memory Column Address Strobe from SL9X50. Active LOW for DMA or CPU Memory Cycles for Bank A. Used to generate NCASA0,1 signals.
NMCASB	6	I	Memory Column Address Strobe from SL9X50. Active LOW for DMA or CPU Memory Cycles for Bank B. Used to generate NCASB0,1 signals.
NMDLATEN	72	I	Memory data latch enable. Selects latched MD Bus data when asserted LOW. Should be left un-connected for non-cache-based designs.
NMEMDIR	97	I	Data transfer direction between D Bus and MD Bus. When LOW, data path is from MD Bus to D Bus. (Read)
NPERR	96	O	When LOW it indicates Parity Error on the LOW or the HIGH Byte. Active on read cycles only.
NSBE0,1	100,1	I	Byte Enables. Asserting NSBE0/1 enables LOW/HIGH byte MD or D Bus Buffers.
NSDHLEN	34	I	Selects latched/unlatched SD data. When LOW it selects unlatched data from SD Bus.

PIN DESCRIPTION SL9020 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
PTYL,H	98,99	I/O	Parity Data Bus for LOW and HIGH bytes. Parity is generated for write cycles. Parity is checked for read cycles. Direction is controlled by NMEMDIR.
SBA	24	I	Select Data Buffers from the SL9011 System Controller. When HIGH it selects latched data from SD [7:0] to D [7:0]. When LOW it selects unlatched data from SD [7:0] to D [7:0].
SD0-SD15	11,12,13,14 16,17,18,19 36,37,38,39 41,42,43,44	I/O	16 Bit I/O channel Data Bus.
SDHLAT	33	I	SLOT Data Latch Strobe. A LOW to HIGH transition latches data from SD[15:8].
VDD	3,28,53,78	-	+5V Power.
VSS	4,15,29,40 54,65,79,90	-	0V Ground.
XD0-XD7	48,49,50,51 52,55,56,57	I/O	8 Bit peripheral Data Bus.

ABSOLUT MAXIMUM RATINGS SL9020 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current *note 2	I_{OS}	-40	+40	mA
Output Current *note 3	I_{OS}	-40	+80	mA
Output Current *note 4	I_{OS}	-60	+120	mA
Output Current *note 5	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. All other outputs.
3. XD0-XD15.
4. MD0-MD15, D0-D15.
5. SD0-SD15,NCASA,B,02,13.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9020

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for TTL Input	VIH	2.2		V	
Input Low Voltage for TTL Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL		0.3VDD	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = VSS

NOTES:

* VIH = VDD, VIL = Vss

SD0-SD15,NCASA,B,02,13	= 24mA buffers	(typical)
MD0-MD15, D0-D15	= 12mA buffers	
XD0-XD15	= 8mA buffers	
All other outputs	= 3.2 mA buffers	

AC CHARACTERISTICS SL9020

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	System Data Bus to Memory Bus Delay	8	17	ns
t2	System Data Bus to CPU Data Bus Delay	8	17	ns
t3	System Data Bus to Parity Bits Output	10	30	ns
t4	CPU Data Bus to Memory Data Bus Delay	8	15	ns
t5	CPU Data Bus to System Data Bus Delay	8	20	ns
t6	CPU Data Bus to Parity Bits PTYL,H Output	10	30	ns
t7	Memory Data Bus to CPU Data Bus Delay	8	15	ns
t8	Memory Data Bus to System Data Bus Delay	8	20	ns
t9	Memory Data Bus to Parity Error Output	10	24	ns
t10	System Data Bus Low Byte to High Byte Conversion	8	20	ns
t11	System Bus to CPU Data Bus Hi-Lo Byte Conversion	8	30	ns
t12	System Bus to Mem Data Bus Hi-Lo Byte Conversion	8	30	ns
t13	NSBE0,1 to CPU Data Bus Delay	8	29	ns
t14	NSBE0,1 to Memory Data Bus Hi-Z	8	26	ns
t15	NSBE0,1 to Memory Data Bus Valid	8	29	ns
t16	NGAT1 to SD8-SD15 Delay	--	29	ns
t17	SD Bus to CTLOFF setup time	10	-	ns
t18	AEN to XD,SD Hi-Z	8	20	ns
t19	NBUFRD to XD,SD Valid	8	20	ns
t20	DLAT, MDLAT, SDHLAT to Latched Data	8	20	ns
t21	NCASA,B or NSBE0,1 to NCASA02,13 or NCASB02,13	8	15	ns

AC TIMING DIAGRAMS SL9020