FEATURES

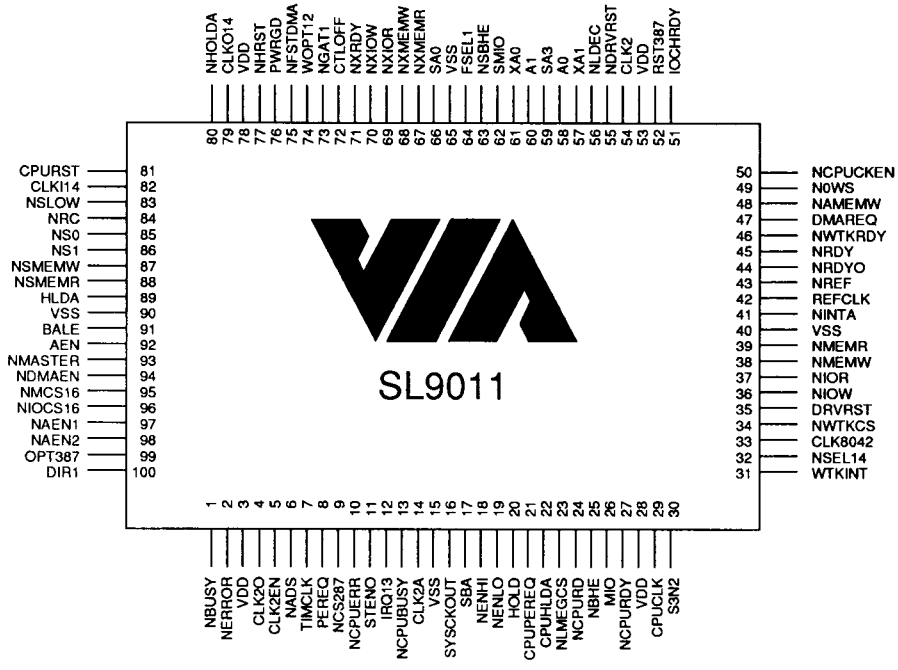
- AT System Control Logic.
- Supports 80286, 80386SX (P9), or 80386DX-based Designs.
- Up to 25 MHz Performance.
- Clock Switching and Reset Logic.
- Programmable Wait States for 8 Bit AT Cycles.
- Generates all Essential Clock Signals for PC's.
- Synchronous Options.
- Refresh/DMA Arbitration.
- Numerical Coprocessor Support for 80287, 80387SX, 80387DX and Weitek Coprocessor.
- Ready Generation Logic.
- Generates Data, Address, Direction and Enable Controls.
- Advanced ALE Generation.
- Advance CMOS Technology.
- 100 pin Flatpack.

DESCRIPTION

The SL9011 System Controller is a member of VIA's FlexSet family that efficiently integrates the PC/AT system control logic.

The SL9011 is part of the Core AT Logic that implements the system logic which is common to the microprocessors 80286, 80386SX and 80386DX. Up to 25 MHz performance is supported. In addition to the SL9011, the Core AT Logic chips consists of the SL9020 Data Controller, the SL9025 Address Controller, the SL9030 Integrated Peripheral Controller and the SL9X50/1 Memory Controller.

PINOUT


SL9011
1 NBUSY
2 NERROR
3 VDD
4 CLK2O
5 CLK2EN
6 NADS
7 TIMCLK
8 PEREQ
9 NCS287
10 NCPUERR
11 STENO
12 IRQ13
13 NCPUBUSY
14 CLK2A
15 VSS
16 SYSCKOUT
17 SBA
18 NENHI
19 NENLO
20 HOLD
21 CPUPEREQ
22 CPUHLDA
23 NLMEGCS
24 NCPURD
25 NBHE
26 MIO
27 NCPURDY
28 VDD
29 CPUCLK
30 S3N2
31 WTKINT
32 NSEL14
33 CLK8042
34 NWTKCS
35 DRVRST
36 NIOW
37 NIOR
38 NMEMW
39 NMEMR
40 VSS
41 NINTA
42 REFCLK
43 NREF
44 NRDYO
45 NRDY
46 NWTKRDY
47 DMAREQ
48 NAMEMW
49 NOWS
50 NCPUCKEN
51 IOCHRDY
52 RST387
53 VDD
54 CLK2
55 NDRVRST
56 NLDEC
57 XA1
58 A0
59 SA3
60 A1
61 XA0
62 SMIO
63 NSBHE
64 FSEL1
65 VSS
66 SA0
67 NXMEMR
68 NXMEMW
69 NXIOR
70 NXIOW
71 NXRDY
72 CTLOFF
73 NGAT1
74 WOPT12
75 NFSTDMA
76 PWRGD
77 NHRST
78 VDD
79 CLKO14
80 NHOLDA
81 CPURST
82 CLKI14
83 NSLOW
84 NRC
85 NS0
86 NS1
87 NSMEMW
88 NSMEMR
89 HLDA
90 VSS
91 BALE
92 AEN
93 NMASTER
94 NDMAEN
95 NMCS16
96 NIOCS16
97 NAEN1
98 NAEN2
99 OPT387
100 DIR1

DESCRIPTION (Cont'd.)

The SL9011 provides the AT System Control Logic. It generates all the major clocks for an AT compatible system design along with the command and control signals for both the system and peripheral busses. It interfaces with the CPU to determine the type of the bus cycle to execute, and generates the CPU READY signal. The SL9011 System Controller contains logic to make conversions between 16-bit and 8-bit data accesses. It also generates the control signals necessary for the 80287, 80387SX and 80387DX Numeric Processors.

The SL9011 controls all bus activity and provides arbitration between the CPU, DMA, External Master devices and the Refresh logic. It is designed using advanced 1.5 micron, double layer metal CMOS process and is offered in a 100 pin plastic flatpack package.

SL9011 operates in four basic modes. First and most common, is the CPU mode. This mode is active any time CPUHLDA is low.

The other modes can only be active when CPUHLDA is high. These modes are DMA mode, External Master Mode, or Refresh Mode. If the inputs NAEN1 or NAEN2 are active, the SL9011 is in DMA mode and the command bus is driven from the inputs on the peripheral bus.

FUNCTIONAL DESCRIPTION

The SL9011 AT System Controller consists of the following sub-modules as illustrated in the Block Diagram.

1. 80X87 Logic
2. Refresh Logic
3. Ready
4. 82288 Bus Controller
5. Reset Logic
6. FSel Logic
7. Bus Conversion Control Logic
8. Clock Control and Clock Generation

The SL9011 PC/AT Compatible System Controller functionally replaces an 82C288 Bus Controller and an 82C84A Clock Generator and Driver.

80X87 LOGIC

The 80X87 Logic supplies all the necessary glue logic to support the Intel 80287, 80387SX or 80387DX NPX and the Weitek 3167. The NPX I/O port address is 00F8 through 00FF, RST387 (from SL9025) is effected by an IO write to 00F1. The system signals SA0, SA3, MIO, NIOW, RESET and the SL9025 signal NCS287 are anded together to initiate a NPX reset. Reset logic will hold 387RST true and IOCHRDY false until the appropriate number of CPUCLK cycles have elapsed. The NPX output signal NBUSY is clocked into a "D" register by the NPX output NERROR. The register output is STENO, status enable. STENO is used to gate NPX output PEREQ into CPUPEREQ, as well as input WTKINT into IRQ13. STENO also gates either NBUSY or TIMCLK into NCPUBUSY, as determined by the input OPT387. STENO is true if NBUSY is false when the NPX asserts NERROR. If NBUSY is true when NERRROR is asserted, STENO is latched false and must then be cleared by an I/O write to 00F0.

NPX input NERROR is continuously gated into NCPUERR following the first NADS or NS1 after a CPURST.

REFRESH LOGIC

The refresh circuitry provides logic to perform the following five functions:

1. Provide REFCLK
2. Provide NMEMR
3. Hold off REFCLK and NMEMR with IOCHRDY
4. Drive NREF
5. Request a CPU hold

A refresh cycle is initiated when the input REFREQ is toggled low to high, causing the request to be latched. DMACLK relatches the request and causes a CPUHOLD request. The relatched request is again latched with SYSCLK. This latched output is anded with HLDA and used to drive NREF. NREF starts the State Machine which performs the following functions in order:

1. Enable REFCLK
2. Generate NMEMR
3. Hold for IOCHRDY
4. Reset Refresh
5. Stop

External refresh request logic may be utilized by tying REFREQ high, and connecting the NREF I/O pin to the external devices request pin. If an SL9030 IPC is used, the refresh line is called NREFRESH.

READY

The READY circuitry provides the basic function of oring peripheral and memory ready signals and passing them on to the CPU. Additionally, through the selection of the WOPT12 input, MEM/IO wait states may be added to IOCHRDY. See Table 1. IOCHRDY will extend any bus I/O, memory or refresh operation.

READY, Cont'd.

The three ready signals: NREAD0 from the NPX, NWTKRDY from the Weitek NPX, and NRDY from the memory controller, are ored together and gated out directly to NCPURDY. The SLOT signal N0WS is latched by CPUCLK, gated with NCNVRDY (no conversion in progress) relatched with NSYSCLK, then gated out to NCPURDY. The signal IOCHRDY from the SLOT bus is gated with the internal signals 1WS, CNVRDY and wait state counter outputs, such that the wait states per Table 1 are inserted. Delayed IOCHRDY is then latched by SYSCKOUT, relatched by CPUCLK, gated with internal conversion signals, latched by NSYSCKOUT and gated out to NCPURDY.

WOPT12	16 BIT	8BIT
0	2	6
1	1	4

Table 1

82288 BUS CONTROLLER

The 82288 Support Logic and 82288 work together to effect a system solution that is 82288 compatible.

Support logic uses the input signals S3N2 and MIO to distinguish between 386 or 286 operation. Inputs NS0, NS1 and MIO are decoded to product the basic outputs NINTA, NIOW, NIOR, NMEMW and NMEMR. NMCS16, XRDY, NDCONV, and ALE are used to generate CMDLY. The inputs HLDA and MASTER are used to generate AEN and disable the outputs for DMA operation.

RESET LOGIC

There are three Reset inputs and three Reset outputs. Two Reset functions are served, I/O and CPU.

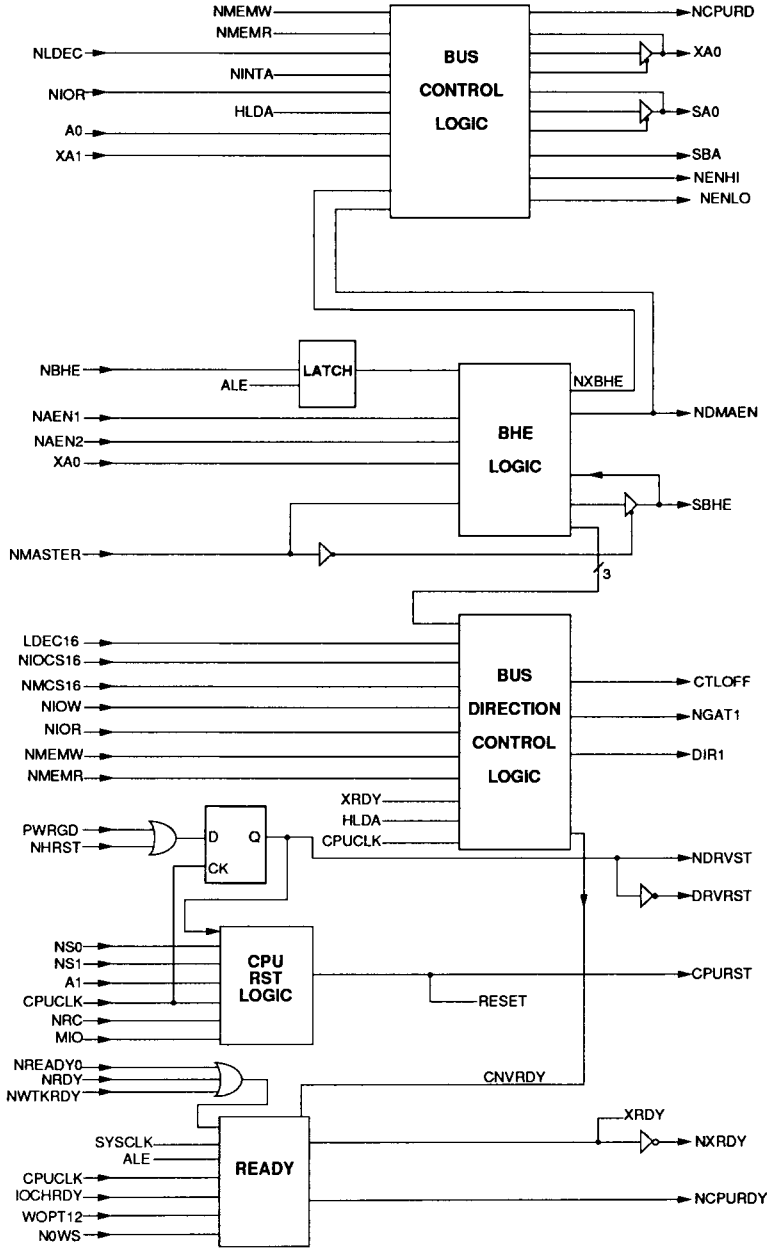
To effect a I/O Reset, inputs PWRGD and NHRST are ored and latched by CPUCLK. The latched output drives NDRVRST and its compliment, DRVRST. These signals are used to reset the slot I/O and keyboard controller. NHRST is a schmidt input and this may be driven with a mechanical switch.

To effect a CPU Reset, the inputs PWRGD and NHRST are ored and latched by CPUCLK. The latched signal is ored with NRC and conditioned with the CPU signals MIO NS0, NS1 and A1 such that the output signal CPURST is driven true synchronously with CPUCLK and is negated to meet the hold and release requirements of the processor.

FSEL LOGIC

FSel 1 output is used to drive the FSel Pin on SL9090A. When FSel1=0, the clock CPUCLK slows to 16MHz. When FSel1=1, the clock is selected fast (Reference the 9090A spec). When NFSTDMA is negated, NMASTER or NDMAEN (BUSMASTER or 8 or 16 bit DMA) will clock FSel1=0, and NS0 or NS1 (IO/MEM READ, IO/MEM WRITE) will reset FSel1=0. FSel1 will be set =1 by NADS or Reset. When NFSTDMA is asserted, NDMAEN and NMASTER have no affect on FSel1. NS0 and NS1 Reset FSel1=0 as above, and asserting NADS, RESET or HLDA will set FSel1=1.

BLOCK DIAGRAM SL9011



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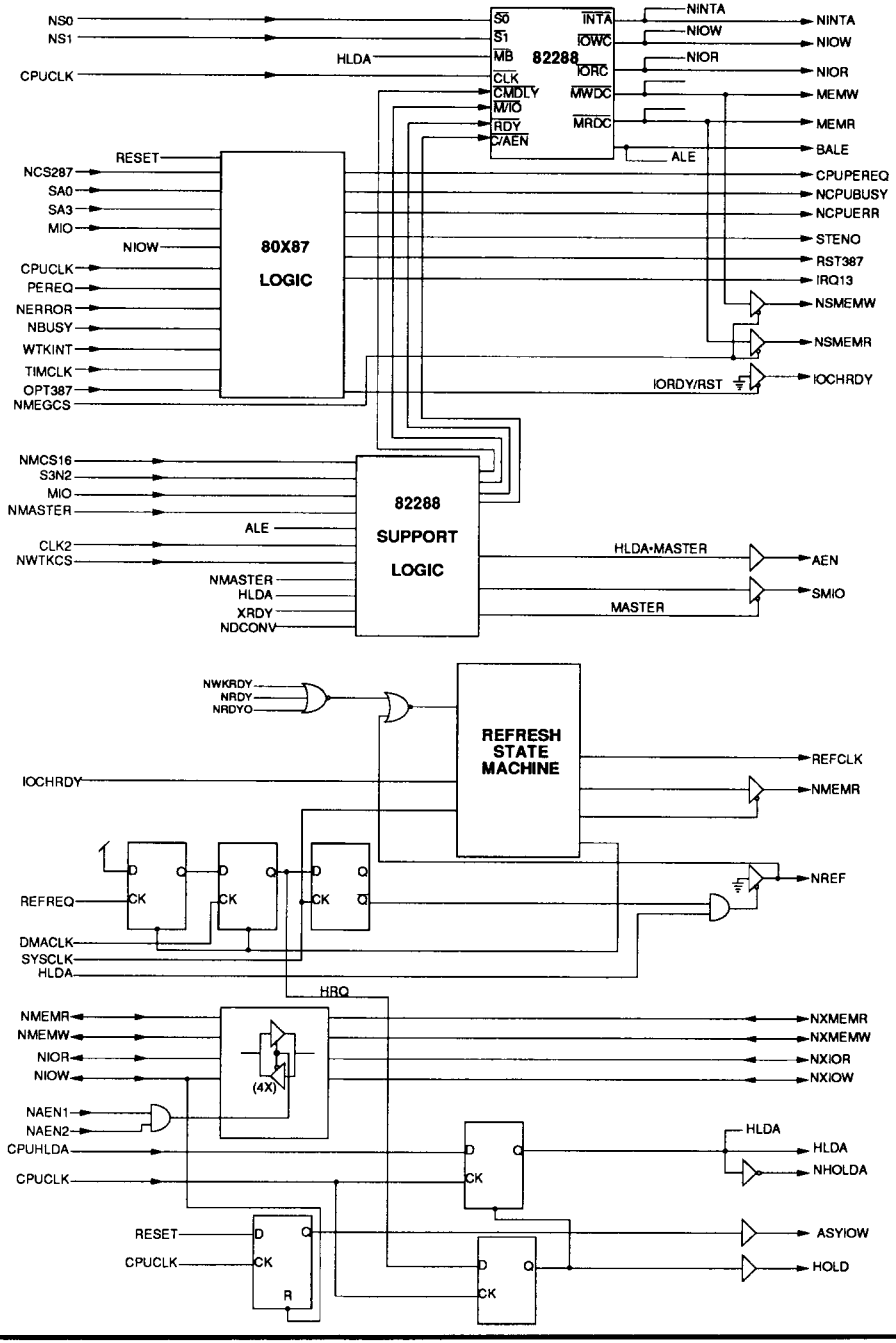

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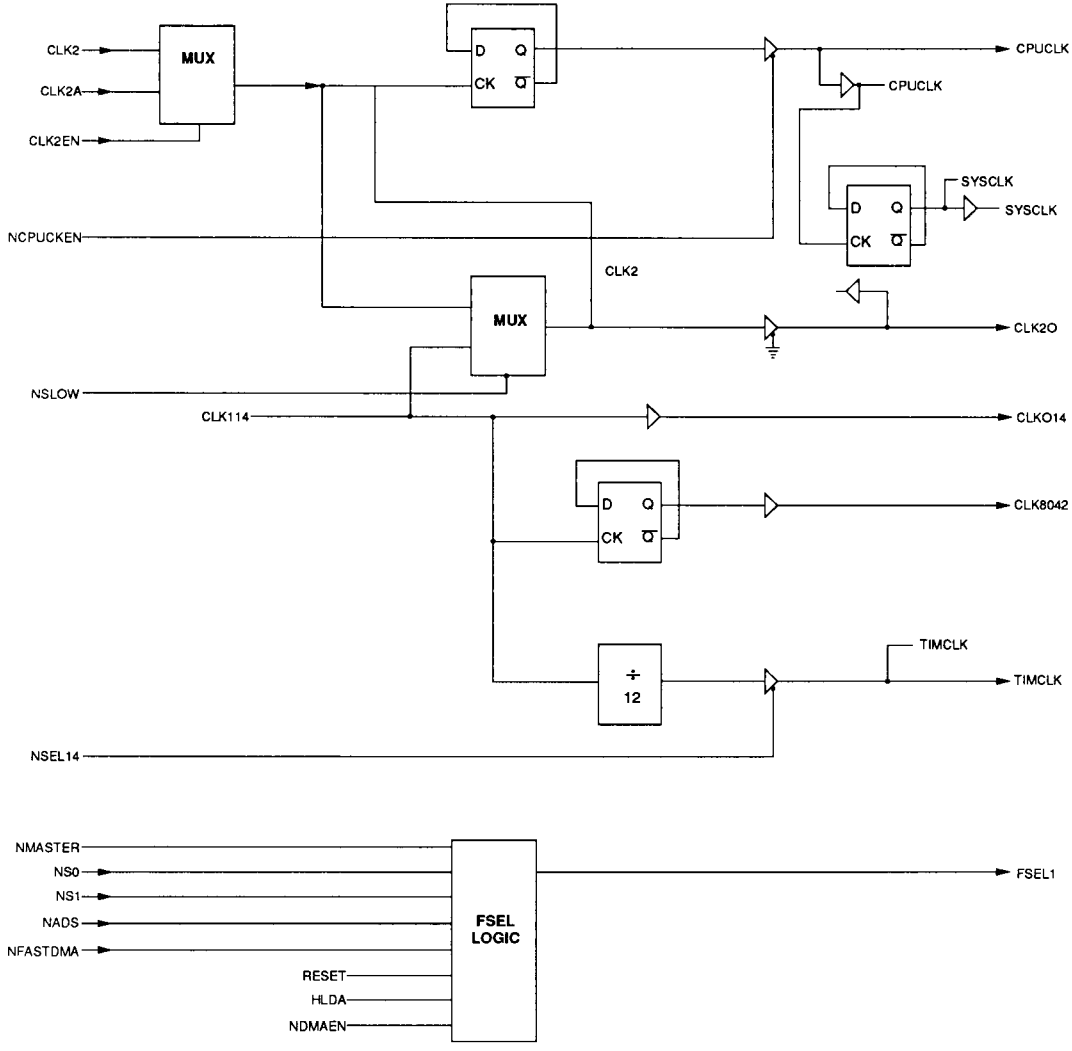


BUS CONVERSION CONTROL LOGIC

A State Machine for controlling the conversion between 16-bit data accesses from the CPU to 8-bit peripherals is contained in the SL9011. The state machine will generate the control signals DIR1, NGAT1 and CTLOFF to the SL9020 Data Buffer chip to route the data correctly for both read and write conversions. The conversion logic will signal the wait state logic to hold the CPU and start the read/write of the low byte. It will then latch the low byte for a read operation, negate the bus control signals, switch SA0 to high, and then perform read/write operations for the high data byte.

SL9011 also generates NGAT1 and DIR1 during 8-bit DMA cycles to route the lower byte on the system data bus to or from the high or low byte of the on-board memory.

CLOCK CONTROL AND CLOCK GENERATION

The SL9011 receives CLK2, CLK2A, and CLKI14 and uses them to generate CLKO14, CPUCLK, CLK8042, CLK2O, TIMCLK and SYSCKOUT. CLK2EN allows for switching between CLK2 and CLK2A. NCPUCKEN and NSEL14 also allow for CPUCLK and TIMCLK to be input externally. CLK2EN and NSLOW can be switched dynamically. SYSCKOUT is synchronized with NADS.

CLK2EN	NSLOW	CLK2O
X	0	14 MHz
X	0	14 MHz
0	1	CLK2
1	1	CLK2A

Table 2

PIN DESCRIPTION SL9011

SYMBOL	PIN	TYPE	DESCRIPTION
A0,1	58,60	I	Local bus least significant address inputs. A0-A1 are generated from CPU BE0-BE3. A0 is used to generate CPURST for shutdown cycle.
AEN	92	O	DMA Address Enable. When LOW, enables data buffers between XD Bus and SD Bus. It is HIGH during DMA cycles. It is used to drive SLOT AEN and the SL9025 Buffer Control.
BALE	91	O	Buffered Address Latch Enable. Directly drives AT SLOT signal BALE.
CLK2	54	I	TTL Level input from oscillator or clock chip. Has twice the frequency of the CPU clock. It is used to clock 82288 support logic.
CLK2A	14	I	Input from oscillator.
CLK2EN	5	I	Clock 2 Enable. Jumper input. When LOW CLK2A is input. When HIGH CLK2 is input.
CLK2O	4	O	Clock 2 Out. This pin is always output enabled. Depending on jumper combinations [CLK2EN], [NSLOW], CLK2O can be either CLK2, CLK2A or 14MHz.
CLK8042	33	O	CLK8042 is CLKI14 divided by two.
CLKI14	82	I	Clock In 14 MHz. 14 MHz being input from oscillator.
CLKO14	79	O	Clock Out 14 MHz. 14 MHz clock output from the chip.
CPUCLK	29	I/O	CPU Clock. It is half the frequency of CLK2 or CLK2A. Internally generated output or input from Clock Chip.
CPUHLDA	22	I	CPU Hold Acknowledge. It is active HIGH when a Bus cycle is granted in response to hold request (HOLD). It is used to generate HLDA and NHOLDA, as well as reset HOLD.
CPUPEREQ	21	O	CPU Processor Extension Request. When active (HIGH) it indicates to CPU that NPX is ready for data transfer to/from its data FIFO. When FIFO is empty, this signal is negated. CPUPEREQ connects directly to the PEREQ pin on the CPU.
CPURST	81	O	Reset Signal to the CPU is an active HIGH output. It is generated in response to any one of the following signals: NHRST, PWRGD and NRC.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
CTLOFF	72	O	Control Output Flag. Rising edge clocks data from SD[7:0] to D [7:0] latches during Bus-conversion cycles. Connects directly to the SL9020 pin CTLOFF.
DIR1	100	O	Direction 1. Controls data transfer direction between SD[7:0] and SD[15:8] in the SL9020 Data Controller. NGAT1 must be asserted. It is used during data conversions (8bit SLOT Read/Writes).
DMAREQ	47	I	DMA Request is asserted HIGH to request a DMA cycle. It initiates hold request (HOLD) to the CPU for a DMA cycle to begin.
DRVRST	35	O	Device Reset is an active HIGH output. When asserted it resets the AT System and the SL9350 Memory Controller. Directly drives the AT SLOT signal DRVRST.
FSEL1	64	O	Frequency Select 1. Jumper output. When asserted LOW (when SL9011 is used with SL9090A), SYSCKOUT is slowed down to 8MHz.
HLDA	89	O	Hold Acknowledge is an active HIGH output to the SL9X5X Memory Controller. When asserted it indicates that CPU has released its control on the local bus in favor of another bus master device (DMA external master). It is generated by resynchronizing CPUHLDA with CPUCLK.
HOLD	20	O	Hold is asserted HIGH whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU.
IOCHRDY	51	I/O	I/O Channel Ready is an active HIGH input from the AT bus. When LOW it indicates a not ready condition and inserts wait states in AT I/O or AT memory cycles. It is used to generate NCPURDY. It is an output during NPX reset cycle.
IRQ13	12	O	Interrupt Request 13 is an active HIGH output which indicates an interrupt from the numeric coprocessor. It connects to the SL9030 pin IRQ13.
MIO	26	I	Memory Input/Output signal from the CPU. When HIGH, it indicates a memory cycle, when LOW, it indicates an I/O cycle. It is used to synchronize Reset, drive SMIO, and enable 80X87 operations.
NADS	6	I	Address Status is an active LOW input generated by the CPU. When asserted it indicates the start of a new cycle.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NAEN1,2	97,98	I	DMA Enable 1,2 are active LOW inputs from the SL9030. When NAEN1 is asserted LOW it indicates an 8-bit DMA cycle. When NAEN2 is asserted LOW it indicates a 16-bit DMA cycle. When both are HIGH it indicates that a non-DMA device owns the system's bus controls. They can not be LOW at the same time. They are used to generate direction control signals NSBHE, SBA, NENHI and NENLO.
NAMEMW	48	I	Advance Memory Write is an active LOW input. It is asserted for local memory write cycles. It is used to enable CPU HOLD.
NBHE	25	I	Byte High Enable is an active LOW input signal which indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is used to generate NENHI.
NBUSY	1	I	Numerical Coprocessor (NPX) Busy is an active LOW input indicating that NPX is currently executing a command. It is used to generate busy signal to the CPU, NCPUBUSY.
NCPUBUSY	13	O	CPU Busy is an active LOW output to the CPU indicating that the NPX is busy executing a command. It connects to the CPU pin BUSY.
NCPUCKEN	50	I	CPU Clock Enable. Jumper input. When LOW CPUCLK is an output. When HIGH CPUCLK is an input.
NCPUERR	10	O	CPU Error is an active LOW output from the NPX to the CPU indicating that an unmasked error condition exists. NCPUERR connects to the ERROR input pin on the CPU.
NCPURD	24	O	CPU Read is an active LOW output to the SL9020 that sets the direction of data between D0-D15 and SD0-SD15. When asserted, the direction is from SD to D.
NCPURDY	27	O	CPU Ready is an active LOW output which goes to CPU's ready input. When asserted, CPU terminates its current bus cycle. IC or S memory, I/O and NPX Ready signals.
NCS287	9	I	NPX Chip Select is an active LOW input which is asserted for I/O port addresses 00F0 through 00FF. It is connected to the SL9025 Address Controller pin NCS287.
NDMAEN	94	O	DMA Enable is an active LOW output to the SL9025 Address Controller. When asserted it indicates a DMA cycle is in progress; either 8-bit or 16-bit. It gates XA1-XA16 onto SA1-SA16 for a DMA operation.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NDRVRST	55	O	Device Reset is an active LOW output. It is the compliment of DRVRST. It is used to reset the SL9025 Address Controller.
NENHI	18	O	Enable High byte to the SL9020 Data Controller, is asserted LOW to enable HIGH byte data transfer between D Bus and SD Bus.
NENLO	19	O	Enable Low byte to the SL9020 Data Controller, is asserted LOW to enable LOW byte data transfers between D Bus and SD Bus.
NERROR	2	I	NPX Error is an active LOW input from 80X87. When asserted it indicates that a non-maskable exception has occurred during the current command cycle. It is used to generate NCPUERR.
NFSTDMA	75	I	Fast DMA. Jumper input. When LOW slows down I/O, and external memory access only. SYSCLK is at one half of CPUCLK. When HIGH SYSCLK slows down for I/O, and external memory, DMA and NMASTER.
NGAT1	73	O	Gate 1 is asserted LOW to enable the data buffer between HIGH byte and LOW byte of SD Bus. It is used in bus conversion cycles to assemble 8 bit bytes into 16 bit words in the SL9020 Data Controller.
NHOLDA	80	O	When asserted NHOLDA indicates that CPU has released its buses and controls on the local bus in favor of another bus master device (DMA/External Master). It is used by the SL9025 to gate SA1-SA16 into A1-A16 during DMA. It is the compliment of HLDA.
NHRST	77	I	Forcing Hardware Reset LOW generates a systems reset (CPURST, DRVRST and NDRVRST). It is a schmidt input and may be connected to a mechanical switch.
NIOCS16	96	I/O	Input/Output Chip select 16 is an active LOW input. It is asserted from AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When HIGH it implies an 8-bit I/O transfer. It is used to control NGAT1.
NINTA	41	O	Interrupt Acknowledge is an active LOW output for the interrupt controller. It is also used to direct data from the XD bus to SD bus during an interrupt acknowledge cycle.
NIOR	37	I/O	Input/Output Read is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NIOW	36	I/O	Input/Output Write is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle. It is used for 80X87 support.
NLDEC	56	I	Local Decode is an active LOW input for the SL9X5X. When active it indicates a local memory transfer. It is used to determine NCPURD direction.
NLMEGCS	23	I	Lower 1 Meg Chip Select is an active LOW, when asserted it indicated that lower 1 meg memory is being selected. It is used to tri-state enable NSMEMR and NSMEMW.
NMASTER	93	I	External Master is an active LOW input from the AT bus. When asserted, indicates that an external master device is currently active.
NMCS16	95	I	Memory Chip Select 16 is an active LOW input from the AT bus. When asserted indicates a 16 bit memory cycle. When HIGH it implies an 8-bit memory transfer. It is used to control NGAT1.
NMEMR	39	I/O	Memory Read is an active LOW bi-directional pin on the AT System bus. It is an output during CPU, DMA and refresh cycles. It is an input when an external master is active on the AT bus.
NMEMW	38	I/O	Memory Write is an active LOW bi-directional pin on the AT System bus. It is an output during CPU and DMA cycles. It is an input when an external master is active on the AT bus.
N0WS	49	I	Zero Wait State is an active LOW input from the AT System bus. It causes termination of a bus cycle, at the first Tc 02 (286) or T2 02 (386).
NRC	84	I	External CPU Reset is an active LOW input. When asserted it resets the CPU by generating CPURST. It may come from a debounced switch.
NRDYO	44	I	Ready O is an active LOW input from the NPX to terminate an NPX bus cycle. It generates an NCPURDY.
NRDY	45	I	Ready is an active LOW input. It is asserted for 32-bit local memory cycles and 16-bit ROM cycles for 386 based systems. For 386SX or 286 it is asserted for 16-bit local memory cycles and 16-bit ROM cycles. It generates an NCPURDY.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NREF	43	I/O	Refresh is an active LOW bi-directional pin. It is input at all other times. It connects to the SL9350 pin NREFRESH and to the SL9030 pin NREFRESH.
NS0,1	85,86	I	Status1,0 are active LOW inputs from the memory controller. They are used by the system to determine the type of bus cycle. (Write, Read, Idle or INTA).
NSBHE	63	I/O	Byte High Enable is an active LOW bi-directional pin for the AT bus. It indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output for CPU and DMA cycles and an input for an external master cycle.
NSEL14	32	I	Select 14. Jumper input. When LOW [TIMCLK] is output. When HIGH [TIMCLK] is input.
NSLOW	83	I	Jumper input. When LOW selects 14 MHz and outputs that as [CLK2O]. When HIGH it outputs [CLK2] or [CLK2A] as [CLK2O].
NSMEMR	88	O	System Memory Read is an active LOW tri-state output for the AT bus. It is an output for CPU, DMA and refresh cycles. It goes to tri-state when lower 1 meg memory is accessed.
NSMEMW	87	O	System Memory Write is an active LOW tri-state output for the AT bus. It is an output for CPU and DMA cycles. It goes tri-state when lower 1 meg memory is accessed.
NWTKCS	34	I	Weitek Chip Select is an active LOW input. When asserted it disables AT bus controller to allow NPX enough time to complete an NPX bus cycle. It connects to the NPX pin - MCS.
NWTKRDY	46	I	Weitek Ready is an active LOW input to terminate an NPX bus cycle. It is used to generate NCPURDY.
NXIOR	69	I/O	Peripheral Bus Input/Output Read is an active LOW bi-directional pin. It is an output for CPU, refresh and external master cycles. It is an input for DMA cycles.
NXIOW	70	I/O	Peripheral Bus Input/Output Write is an active LOW bi-directional pin. It is an output for CPU, refresh and external master cycles. It is an input for DMA cycles.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NXMEMR	67	I/O	Peripheral Bus Memory Read is an active LOW input for DMA cycles. It is used to generate NSMEMR and NMEMR signals during DMA cycles. All other operations (CPU memory read, Refresh, MASTER) will output NMEMR on this line.
NXMEMW	68	I/O	Peripheral Bus Memory Write is an active LOW output for CPU, refresh and external master cycles. It is an input for DMA cycles.
NXRDY	71	O	Ready is an active LOW output to the SL9025 Address Controller. When asserted it indicates termination of a CPU/SLOT bus cycle. It also resets AT's bus cycle state machine.
OPT387	99	I	Option 387 is a jumper select input. When HIGH, allows the NPX NBUSY to pass through to NCPUBUSY. Else TIMCLK appears on NCPUBUSY.
PEREQ	8	I	NPX Peripheral Request is an active HIGH input from NPX. When asserted it causes CPUPEREQ to assert, indicating to the CPU that NPX is ready to transfer data to/from it's data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated.
PWRGD	76	I	Power Good is an active HIGH input from the power supply. Negating it will cause NDRVRST, DRVRST and CPURST to assert.
REFCLK	42	O	Refresh Clock is an active LOW output asserted during refresh cycle for three SYSCKOUT cycles. It drives the SL9025 pin NREF1.
RST387	52	O	Reset 387 is an active HIGH output. It is asserted when I/O port 00F1 is written onto. The signal is active for 96 CPUCLK cycles.
S3N2	30	I	386/286 Mode Select. It is a jumper option. It is HIGH for 386DX or 386SX based systems and LOW for 286 based systems.
SA0	66	I/O	System Bus Address 0-bit. It is a bi-directional pin. It is an output for CPU, Refresh and DMA operations, and an input for Master operation. It is used for 80X87 support.
SA3	59	I	System Bus Address 3-bit. It is used for 80X87 support.
SBA	17	O	Select Data Buffer Data. This signal drives the SL9020 Data Controller. When HIGH it selects latched SD Bus LOW byte data during bus conversions cycles. When HIGH, unlatched SD Bus LOW byte data will pass onto D Bus.

PIN DESCRIPTION SL9011 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
SMIO	62	I/O	Memory Input/Output for the System Bus. When HIGH it indicates a memory cycle. When LOW it indicates an I/O cycle. Tri-stated when master is asserted. This signal is not normally used in an AT.
STENO	11	O	Status Enable is an active HIGH output. This pin serves as a chip select for the 80X87. When inactive, it forces the NPX outputs NBUSY, PEREQ, NERROR and NRDY into floating state.
SYSCKOUT	16	O	System Clock Out is a free running system clock generated by dividing CPUCLK by 2. It uses NADS to synchronize itself to the CPUCLK upon power up during the first CPU cycle. Odd numbers of wait states will also cause SYSCKOUT to resynchronize in subsequent cycles.
TIMCLK	7	I/O	1.19 MHz Timer Clock is an input from the clock chip, or internally generated timer clock being output.
VDD	3,28,53,78	-	+5V. Power.
VSS	15,40,65,90	-	0V. Ground.
WOPT12	74	I	Wait State Option 1,2 is a jumper option. When HIGH it allows 1 wait state for 16-bit memory/IO and 4 wait states for 8-bit memory/IO cycles. When LOW it allows 2 wait states for 16-bit memory/IO and 6 wait states for 8-bit memory/IO cycles.
WTKINT	31	I	Weitek Interrupt is an active HIGH input which asserts IRQ13. It connects directly to NPX pin INTR.
XA0	61	I/O	Peripheral Bus Address Line 0 is a bi-directional pin. It is an output for CPU, refresh and external master cycles and an input for DMA cycles. It is gated onto the SA Bus during DMA operation.
XA1	57	I	Peripheral Bus Address Line 1 is an input used in generating NENLO and NENHI. It must be tied LOW for 386SX based systems.

ABSOLUT MAXIMUM RATINGS SL9011 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current *note 2	I_{OS}	-40	+40	mA
Output Current *note 3	I_{OS}	-40	+80	mA
Output Current *note 4	I_{OS}	-60	+120	mA
Output Current *note 5	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. All other outputs.
3. NINTA, NDRVRST, CPURST, SYSCKOUT, CLK2O, CPUCLK.
4. NMEMR/W, NIOR/W, NXMEMR/W, NXIOR/W, NSMEMW/R, HLDA, BALE, AEN, IOCHRDY, NREF, SMIO, NSBHE, XA0, SA0 .
5. DRVRST.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9011

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL	0.3VDD		V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD

NOTES:

* VIH = VDD, VIL = Vss

DRVRST	= 24mA
NMEMR/W, NIOR/W, NXMEMR/W, NXIOR/W, NSMEMW/R, HLDA, BALE, AEN, IOCHRDY, NREF, SMIO, NSBHE, XA0, SA0	= 12mA
NINTA, NDRVRST, CPURST, SYSCKOUT, CLK2O, CPUCLK	= 8mA
ALL OTHER OUTPUTS	= 3.2 mA

AC CHARACTERISTICS SL9011

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Symbol	Description	Min.	Max.	Units
t1	CLK2 Period	25	-	ns
t2	CLK2 High Duration	7	-	ns
t2a	CLK2 Low Duration	7	-	ns
t3	CPUCLK Period	50	-	ns
t4	CPUCLK High Duration	14	-	ns
t4a	CPUCLK Low Duration	14	-	ns
t5	CPUCLK Falling Edge to SYSCKOUT (High to Low)	-	9.5	ns
t5a	CPUCLK Falling Edge to SYSCKOUT (Low to High)	-	9.5	ns
t6	CLK2 High to NADVALE (Low)	-	4.0	ns
t6a	CLK2 High to NADVALE (High)	-	4.0	ns
t7	NS0,1 Set-up time to CPUCLK Falling Edge	7.0	-	ns
t8	CPUCLK Falling Edge to BALE (Low to High)	-	7.5	ns
t8a	CPUCLK Falling Edge to BALE (High to Low)	-	7.5	ns
t9	N0WS Set-up time to CPUCLK Rising Edge	5.7	-	ns
t10	CPUCLK Falling Edge to NMEMW (High to Low)	-	16.7	ns
t10a	CPUCLK Falling Edge to NMEMW (Low to High)	-	16.7	ns
t11	SYSCKOUT Falling Edge to NCPURDY (High to Low)	-	6.0	ns
t11a	CLK2 Rising Edge to NCPURDY (Low to High)	-	15.5	ns
t12	NMCS16 Set-up time to CPUCLK Rising Edge	7.5	-	ns
t13	IOCHRDY Set-up time to SYSCKOUT Rising Edge	10	-	ns
t13a	IOCHRDY Hold Time to SYSCKOUT Rising Edge	5	-	ns
t14	NIOCS16 Set-up time to CPUCLK Rising Edge	7.5	-	ns
t15	PWRGD Set-up time to CPUCLK Rising Edge	6.0	-	ns
t15a	NHRST Set-up time to CPUCLK Rising Edge	6.0	-	ns
t16	CPUCLK Rising Edge to CPURST (High)	-	12.0	ns
t16a	CPUCLK Rising Edge to CPURST (Low)	-	12.0	ns
t17	CPUCLK Rising Edge to RST387 (High)	-	9.0	ns
t17a	CPUCLK Rising Edge to RST387 (Low)	-	9.0	ns
t18	WTKINT to IRQ13 (Low to High)	-	5.0	ns
t18a	WTKINT to IRQ13 (High to Low)	-	5.0	ns
t19	CLK2 Rising Edge to SMIO (High to Low)	-	15.5	ns
t19a	CLK2 Rising Edge to SMIO (Low to High)	-	16.0	ns
t20	CLK2 Rising Edge to NSBHE (High to Low)	-	18.5	ns
t20a	CLK2 Rising Edge to NSBHE (Low to High)	-	19.0	ns
t21	CLK2 Rising Edge to SA0 (High to Low)	-	18.5	ns
t21a	CLK2 Rising Edge to SA0 (Low to High)	-	19.0	ns
t22	NADS Set-up time to CLK2 Rising Edge	9.0	-	ns
t23	DMAREQ Set-up time to CPUCLK Rising Edge	3.0	-	ns
t24	REFREQ Set-up time to CPUCLK Rising Edge	3.0	-	ns

AC CHARACTERISTICs SL9011 (Cont'd.)

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Symbol	Description	Min.	Max.	Units
t25	CPUCLK Rising Edge to NREF (Low to High)	-	20.0	ns
t25a	CPUCLK Rising Edge to NREF (High to Low)	-	20.0	ns
t26	NREF Set-up time to CPUCLK Rising Edge	5.0	-	ns
t27	CPUCLK Rising Edge to NXRDY (High to Low)	-	15.0	ns
t27a	CPUCLK Rising Edge to NXRDY (Low to High)	-	15.0	ns
t28	CPUCLK Falling Edge to CTLOFF (Low to High)	-	10.0	ns
t28a	CPUCLK Falling Edge to CTLOFF (High to Low)	-	10.0	ns
t29	NWTKCS Set-up time to CPUCLK Rising Edge	5.0	-	ns
t30	CPUCLK Falling Edge to NGAT1 (High to Low)	-	30.0	ns
t30a	CPUCLK Falling Edge to NGAT1 (Low to High)	-	30.0	ns
t31	CPUCLK Falling Edge to DIR1 (High to Low)	-	27.0	ns
t31a	CPUCLK Falling Edge to DIR1 (Low to High)	-	27.0	ns
t32	CPUCLK Falling Edge to NINTA (High to Low)	-	14.0	ns
t32a	CPUCLK Falling Edge to NINTA (Low to High)	-	14.0	ns
t33	CPUHLDA Set-up time to CPUCLK Falling Edge	6.0	-	ns
t34	CPUCLK Falling Edge to NSMEMW (High to Low)	-	19.0	ns
t34a	CPUCLK Falling Edge to NSMEMW (Low to High)	-	19.0	ns
t35	CPUCLK Falling Edge to NSMEMR (High to Low)	-	20.0	ns
t35a	CPUCLK Falling Edge to NSMEMR (Low to High)	-	20.0	ns
t36	CPUCLK Falling Edge to ASYIOW (High to Low)	-	10.0	ns
t36a	CPUCLK Falling Edge to ASYIOW (Low to High)	-	10.0	ns
t37	CPUCLK Falling Edge to HLDA (Low to High)	-	6.0	ns
t37a	CPUCLK Falling Edge to HLDA (High to Low)	-	6.0	ns
t38	CPUCLK Falling Edge to NHOLDA (High to Low)	-	6.6	ns
t38a	CPUCLK Falling Edge to NHOLDA (Low to High)	-	6.6	ns
t39	CPUCLK Rising Edge to DRVRST (Low to High)	-	11.0	ns
t39a	CPUCLK Rising Edge to DRVRST (High to Low)	-	11.0	ns
t40	CPUCLK Rising Edge to NDRVRST (High to Low)	-	12.0	ns
t40a	CPUCLK Rising Edge to NDRVRST (Low to High)	-	12.0	ns
t41	CPUCLK Rising Edge to NCPURD (High to Low)	-	22.0	ns
t41a	CPUCLK Rising Edge to NCPURD (Low to High)	-	22.0	ns
t42	CPUCLK Rising Edge to SBA (High to Low)	-	12.0	ns
t42a	CPUCLK Rising Edge to SBA (Low to High)	-	12.0	ns
t43	CPUCLK Rising Edge to NENHI (High to Low)	-	18.0	ns
t43a	CPUCLK Rising Edge to NENHI (Low to High)	-	18.0	ns

AC CHARACTERISTICS SL9011 (Cont'd.)

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Symbol	Description	Min.	Max.	Units
t44	CPUCLK Rising Edge to NENLO (High to Low)	-	20.0	ns
t44a	CPUCLK Rising Edge to NENLO (Low to High)	-	20.0	ns
t45	SYSCKOUT Rising Edge to REFCLK (High to Low)	-	12.0	ns
t45a	SYSCKOUT Rising Edge to REFCLK (Low to High)	-	12.0	ns
t46	NLMEGCS asserted Low to NSMEMW enable	-	7.0	ns
t46a	NLMEGCS asserted High to NSMEMW Tri-state	-	8.5	ns
t47	NLMEGCS asserted Low to NSMEMR enable	-	7.0	ns
t47a	NLMEGCS asserted High to NSMEMR Tri-state	-	8.5	ns
t48	NMASTER asserted Low to AEN (Low to High)	-	6.5	ns
t48a	NMASTER asserted High to AEN (High to Low)	-	6.5	ns
t49	NAEN1 asserted Low to NDMAEN (High to Low)	-	6.0	ns
t49a	NAEN1 asserted High to NDMAEN (Low to High)	-	6.0	ns
t50	NAEN2 asserted Low to NDMAEN (High to Low)	-	6.0	ns
t50a	NAEN2 asserted High to NDMAEN (Low to High)	-	6.0	ns
t51	SA0 to XA0 delay (High to Low)	-	10.0	ns
t51a	SA0 to XA0 delay (Low to High)	-	10.0	ns
t52	XA0 to NSBHE delay (High to Low)	-	12.0	ns
t52a	XA0 to NSBHE delay (Low to High)	-	12.0	ns
t53	NBUSY to NCPUBUSY delay (High to Low)	-	8.0	ns
t53a	NBUSY to NCPUBUSY delay (Low to High)	-	8.0	ns
t54	PEREQ to CPUPEREQ delay (Low to High)	-	7.0	ns
t54a	PEREQ to CPUPEREQ delay (High to Low)	-	7.0	ns
t55	NERROR to NCPUERR delay (High to Low)	-	7.0	ns
t55a	NERROR to NCPUERR delay (Low to High)	-	7.0	ns
t56	NERROR Rising Edge to STENO (High to Low)	-	10.0	ns
t57	NCS287 asserted Low to STENO delay (Low to High)	-	17.0	ns
t58	NRDYO asserted Low to NCPURDY (High to Low)	-	6.4	ns
t58a	NRDYO asserted High to NCPURDY (Low to High)	-	6.4	ns
t59	NRDY asserted Low to NCPURDY (High to Low)	-	7.0	ns
t59a	NRDY asserted High to NCPURDY (Low to High)	-	7.0	ns
t60	NWTKRDY asserted Low to NCPURDY (High to Low)	-	7.0	ns
t60a	NWTKRDY asserted High to NCPURDY (Low to High)	-	7.0	ns

AC TIMING DIAGRAMS SL9011

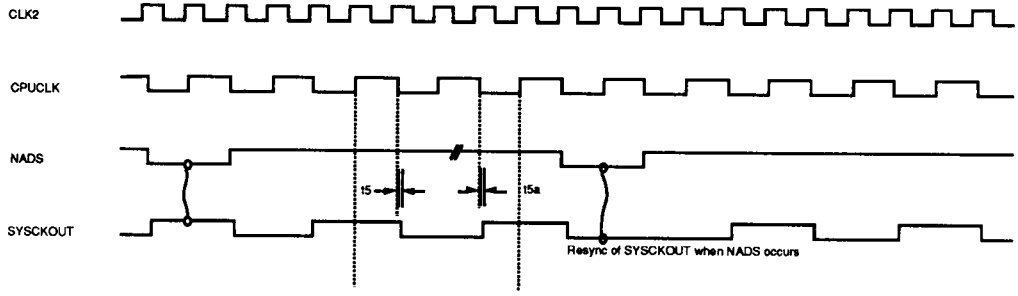
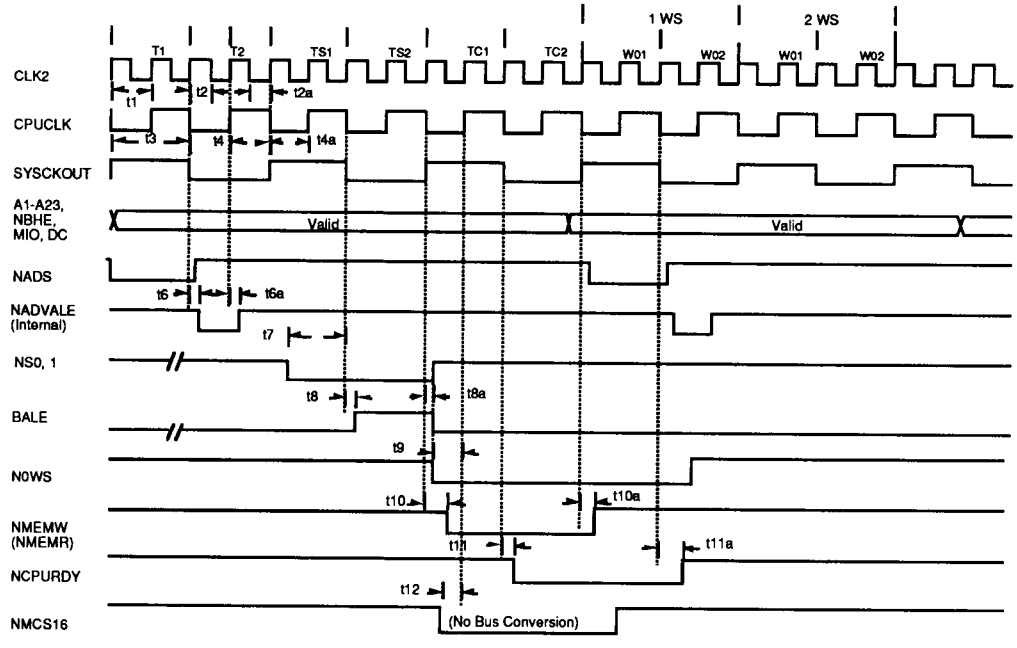


Figure 1. SYSKOUT and DMACLK Relationships with CPUCLK SYSCKOUT Synchronization with the Assertion of NADS



NOTES:

1. N0WS active setup to CPUCLK rising edge is to ensure AT (ISA) 0 wait state cycle.
2. NADVALE is internal to SL9011.
3. NMCS16 setup ensures that no Bus conversion cycle takes place.
4. NMEMR delay from CPUCLK falling edge is same as NMEMW (t10, t10a).
5. NMCS16 or NIOCS16 is not latched inside SL9011. It is sampled every rising edge of CPUCLK and must stay asserted for the duration of the ISA Bus cycle.
6. CMD DELAY is asserted for all 8 or 16 bit I/O cycles and 8 bit memory cycles.

Figure 2. 16 Bit External Memory Cycle, 0 Wait State Non-Pipelined

AC TIMING DIAGRAMS SL9011

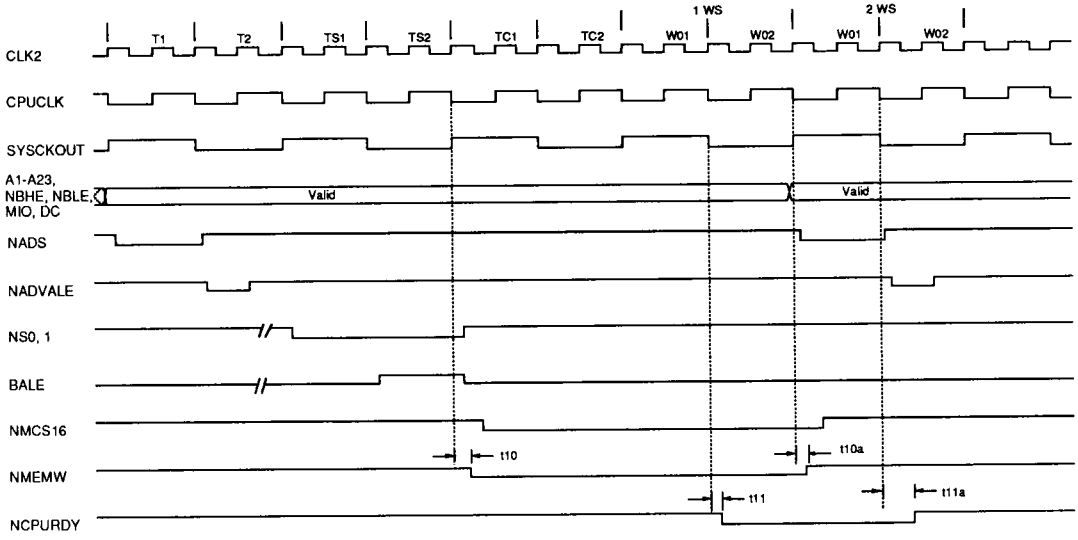


Figure 3. 16-Bit External Memory Cycle, 1 Wait State Non-Pipelined

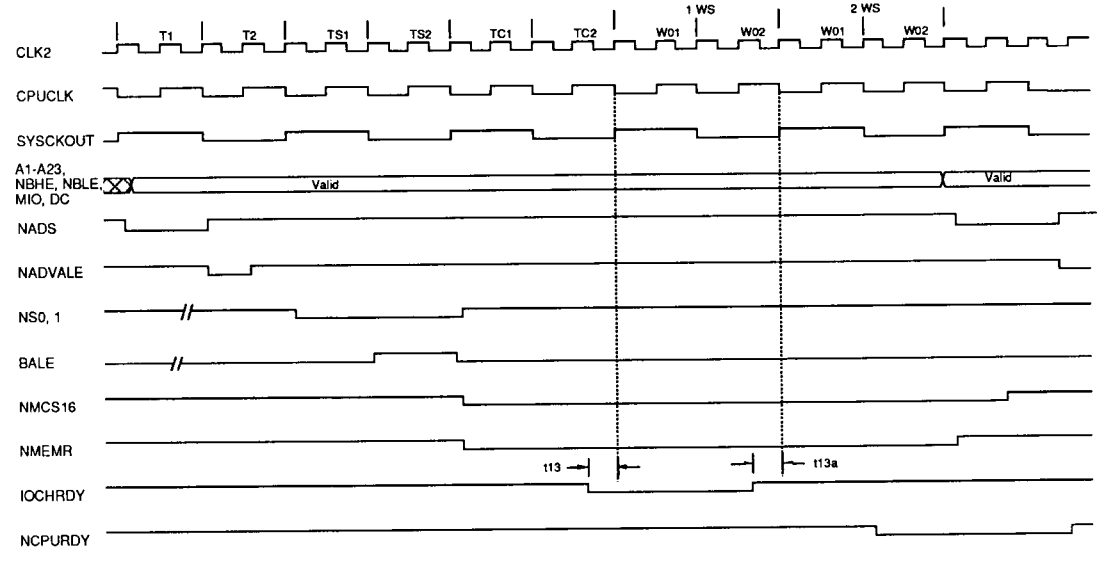


Figure 4. 16-Bit External Memory Cycle, 2 Wait State Using IOCHRDY to Extend the Cycle Non-Pipelined

AC TIMING DIAGRAMS SL9011

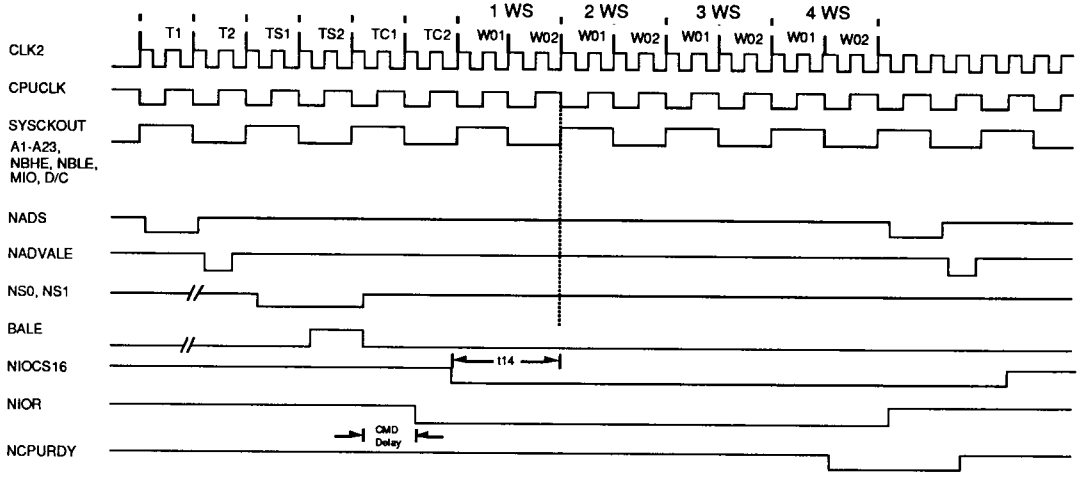


Figure 5. 16-Bit External I/O Cycle with 4 Wait States Non-Pipelined

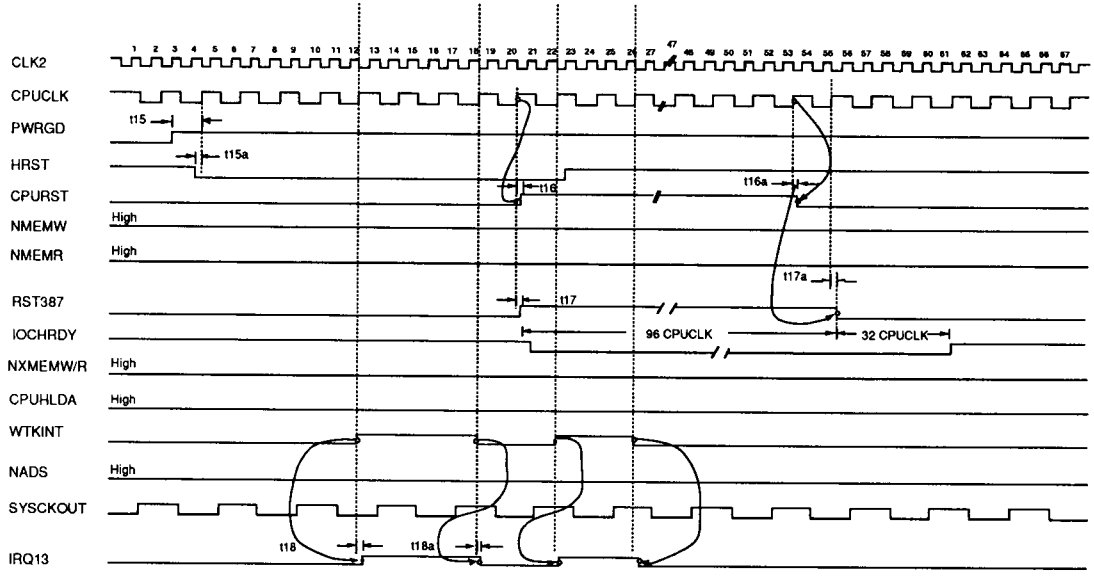


Figure 6. RESET, CPURST, DMACKOUT, SYSCKOUT TIMINGS WTKINT AND IRQ13 RELATIONSHIP

AC TIMING DIAGRAMS SL9011

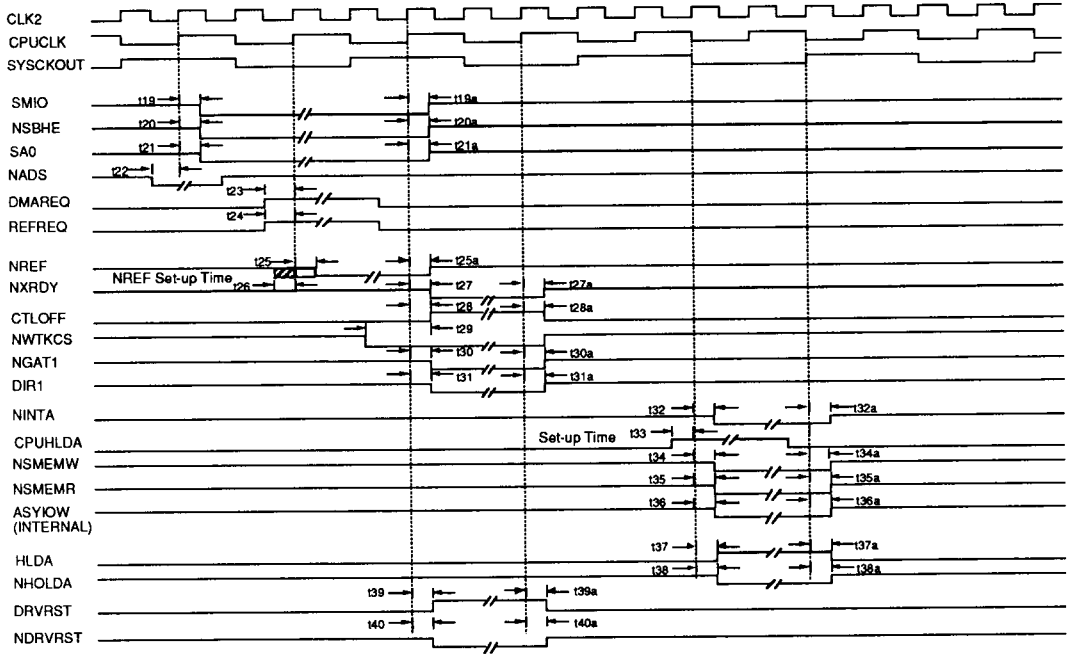


Figure 7. Set-Up Times and Output Signal Delays from CLK2 or CPUCLK

AC TIMING DIAGRAMS SL9011

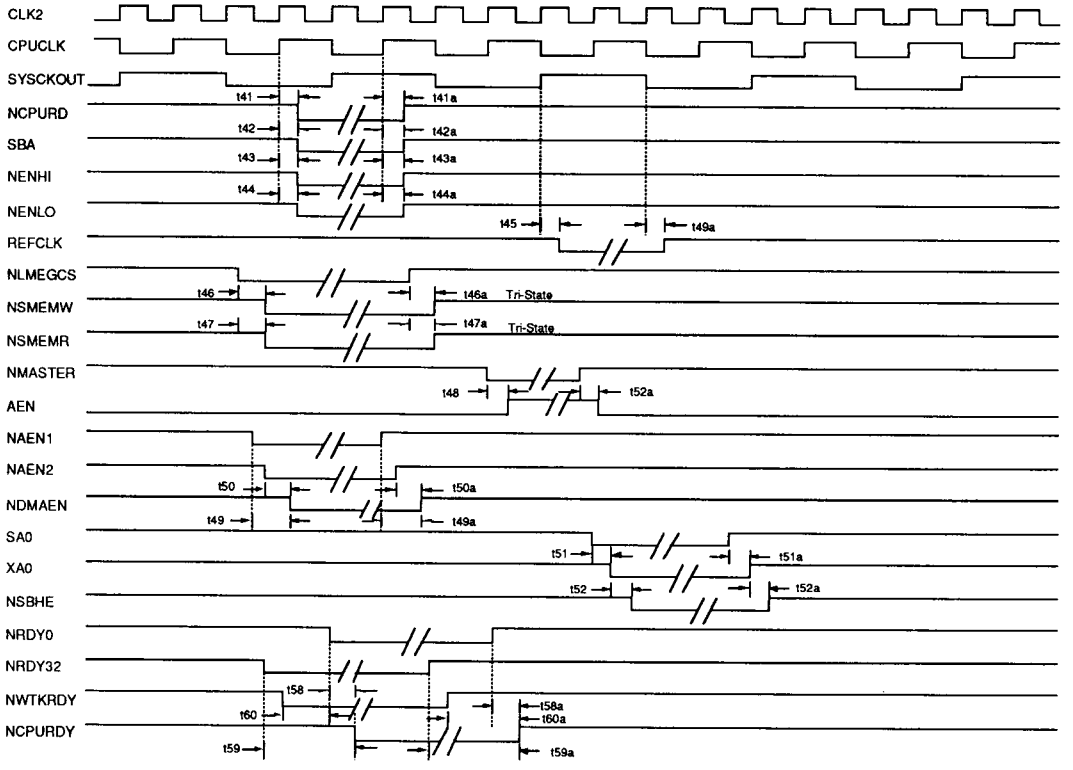


Figure 8. Output Signal Delays from CPUCLK and NCPURDY Delays

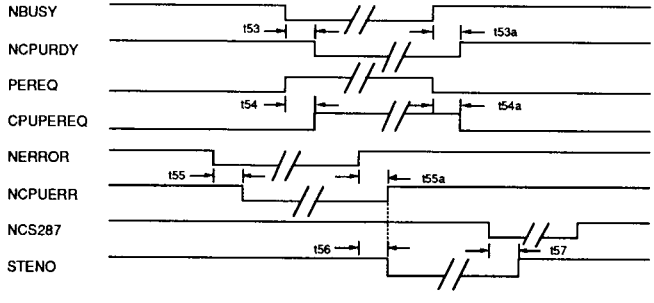
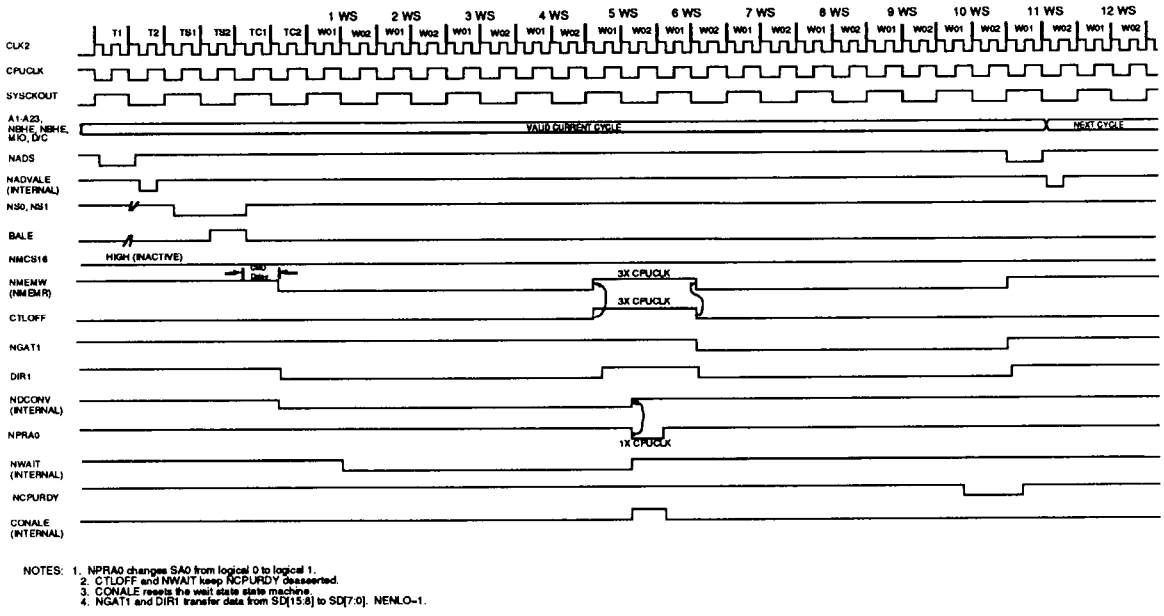


Figure 9. NPX Cycle Input to Output Signal Delays

AC TIMING DIAGRAMS SL9011



NOTES: 1. NPRA0 changes SA0 from logical 0 to logical 1.
2. CTLOFF and NWAIT keep NCPURDY deasserted.
3. CONALE resets the wait state state machine.
4. NGAT1 and DIR1 transfer data from SD[15:8] to SD[7:0]. NENLO=1.

Figure 10. 8 Bit External Memory Bus Conversion Cycles (non-pipelined)