The FlexSet™ PC/AT 80386SX System & Memory Controller SL9252

PRELIMINARY

FEATURES

- 100% PC/AT Compatible.
- Up to 20 MHz Performance.
- ISA Bus Control Logic.
  - Synchronous or Asynchronous System Control Operation.
  - Programmable Command Delays.
  - Numerical Co-processor Support.
  - Programmable Wait States for Local and Off-board Cycles.
  - Fast Gate A20 and Fast Reset.
  - IOCHRDY Timeout.
- Memory Control Logic
  - Enhanced Page Mode/2-Way Word and Multi-Page Interleave.
  - Supports up to 64M bytes of On-Board Memory.
  - Shadow RAM Feature for System, Video, LAN BIOS.
  - Can use 4M, 1M and 256K DRAMs or a mix.
  - Staggered RAS Refresh.
- Programmable Memory Options
  - User Selectable 8 or 16 bit ROM with Selectable wait states.
  - Selectable Hit (0-3) and Miss (1-4) wait states for DRAM access.
  - Mapping of Logical Banks to Physical Banks.
  - 512 X 512 Split.
  - Disable (On Board) Memory to 0K in 128K Resolution.
  - Memory Backfill.
  - EMS LIM 4.0 Mapping Registers
    - Up to 4 Sets of 4 Registers
    - Each Set Maps 64K Boundry
    - Each Register Maps 16K anywhere above 1M Memory
- Testability Features.
- Advanced, Low Power CMOS Technology for Laptops.
- 160 Pin Flatpack.

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860 East Arques Avenue
Sunnyvale, CA 94086

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BLOCK DIAGRAM SL9252

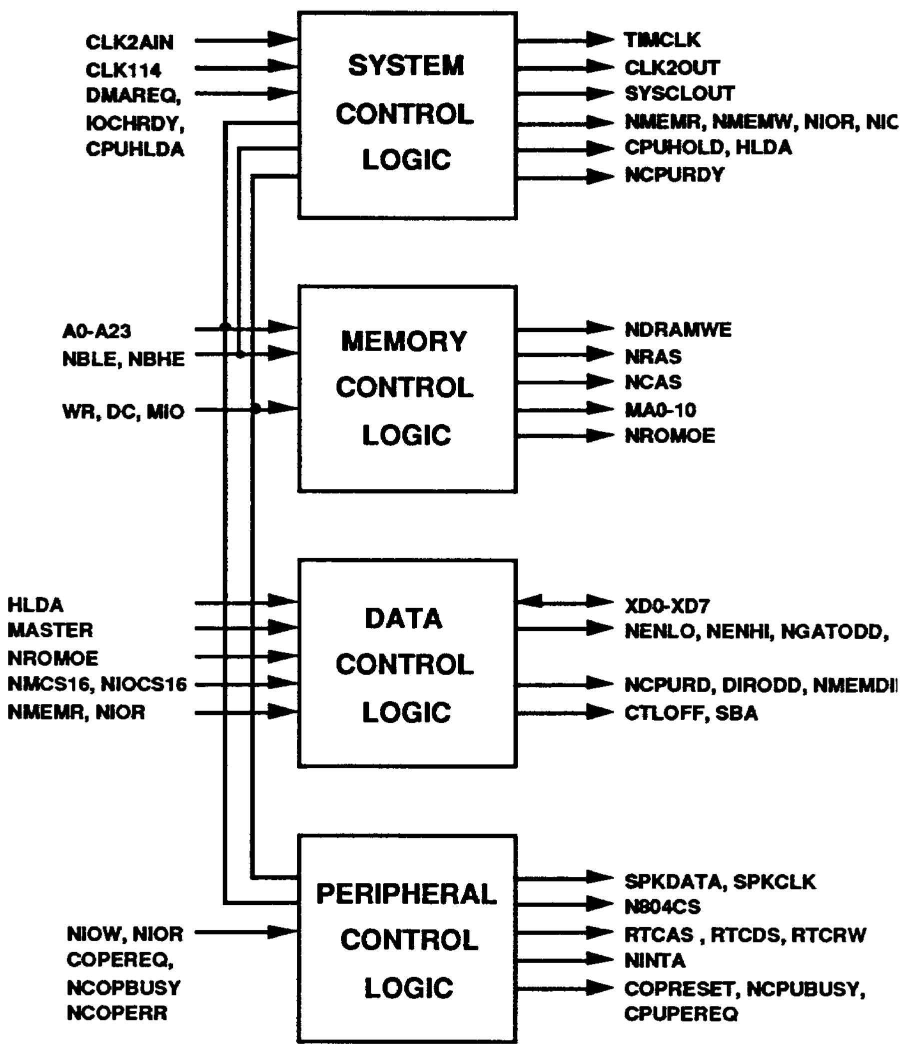


Fig. 1 Functional Block Diagram

I. DESCRIPTION

VIA's System and Memory Controller SL9252, has the logic for the System Control, Memory Control, Data Control and chip select for some of the peripherals used in an AT system. The device is fully configurable via software. No external hardware jumpers are needed to utilize its features. Default values are provided to boot any system configuration. On reset, BIOS routines are used to program the device, transparent to the user, to utilize its special features.

Four configuration registers in the System Control Logic control the AT bus and peripheral bus operations. Synchronous and asynchronous bus operations are supported. In synchronous mode, bus clock is derived from the processor's CLK2. In asynchronous mode, it is derived from an independent external bus clock pin.

Support for page mode and non-page mode operation with non-interleave or word/multi-page interleave, along with programmable memory timing, allow the system designer to get maximum performance for the chosen DRAMs. High drive for RAS, CAS, memory address, and write lines are provided to connect SL9252 directly to a large DRAM memory array without external buffering. In addition, CAS for all the banks in non-interleave and 2-way interleave are provided to reduce external gates.

Shadowing features are supported in 16K granularity from 640K to 1M. Remap options allow shadowing of eight different combinations of top of memory, Local ROM, and Video ROM to 640K to 1M region.

VIA's System and Memory Controller, SL9252, can be used with VIA's SL9020 Data Controller, or with discrete latches and buffers. Data direction and enable signals for the data controller are provided for both modes of operation.

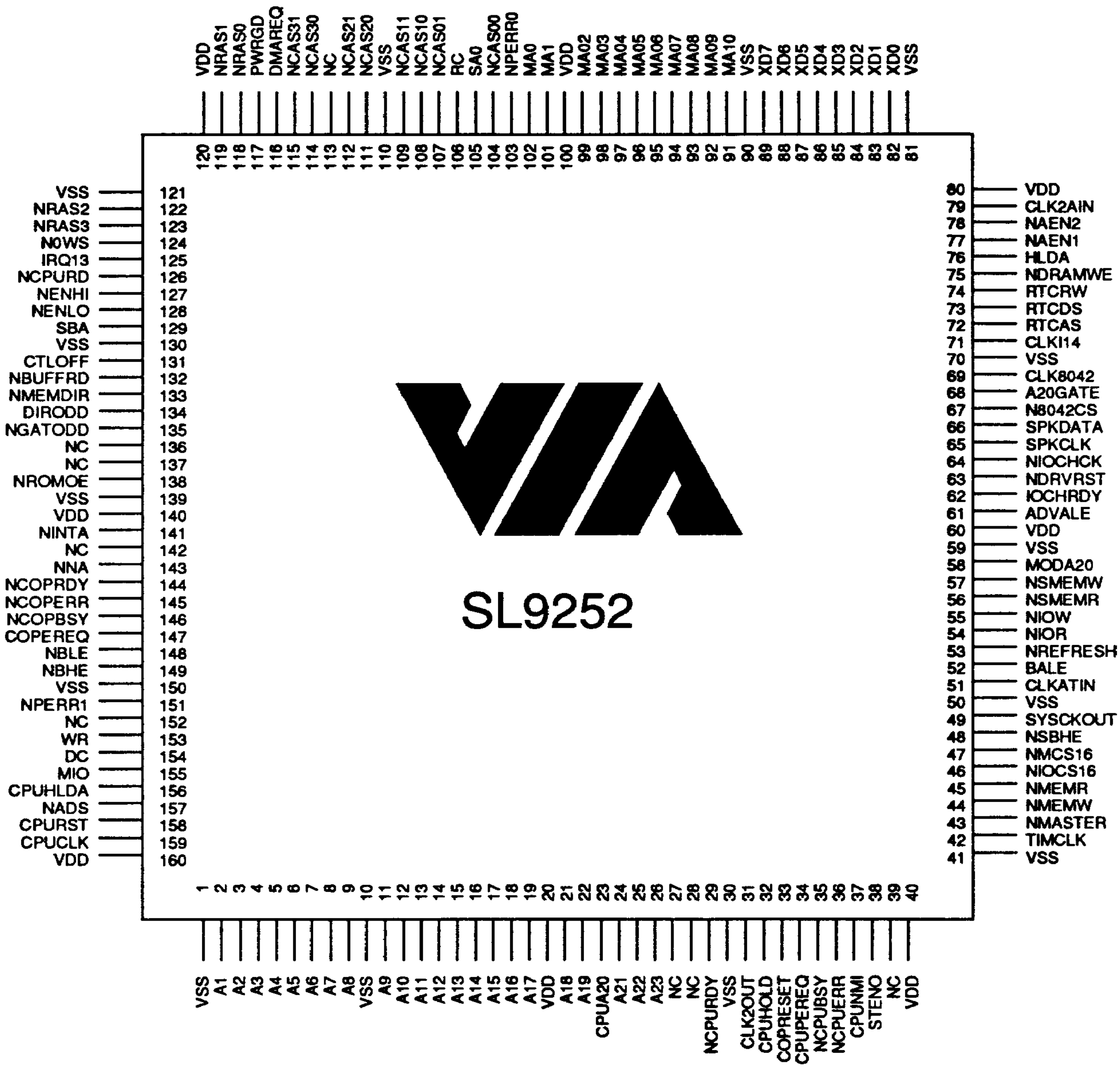
SL9252 provides decoding for the Real Time Clock and Keyboard Controller, thus avoiding external decoding gates. In addition, Port B logic, PS/2 Compatible Port 92 for fast reset, and A20GATE provide the necessary logic support for a one-chip solution.

Figure 1 shows the Functional Block Diagram of SL9252. It is logically divided into 4 blocks:

1. System Control Logic
2. Memory Control Logic
3. Data Control Logic.
4. Peripheral Control Logic

The following sections cover detailed operational descriptions of these four internal blocks.

PINOUT


SL9252
1 VSS
2 A1
3 A2
4 A3
5 A4
6 A5
7 A6
8 A7
9 A8
10 VSS
11 A9
12 A10
13 A11
14 A12
15 A13
16 A14
17 A15
18 A16
19 A17
20 VDD
21 A18
22 A19
23 CPUA20
24 A21
25 A22
26 A23
27 NC
28 NC
29 NCPURDY
30 VSS
31 CLK2OUT
32 CPUHOLD
33 COPRESET
34 CPUPEREQ
35 NCPUBSY
36 NCPUERR
37 CPUNMI
38 STENO
39 NC
40 VDD
41 VSS
42 TIMCLK
43 NMASTER
44 NMEMW
45 NMEMR
46 NIOCS16
47 NMCS16
48 NSBHE
49 SYSCKOUT
50 VSS
51 CLKATIN
52 BALE
53 NREFRESH
54 NIOR
55 NIOW
56 NSMEMR
57 NSMEMW
58 MODA20
59 VSS
60 VDD
61 ADVALE
62 IOCHRDY
63 NDRVRST
64 NIOCHCK
65 SPKCLK
66 SPKDATA
67 N8042CS
68 A20GATE
69 CLK8042
70 VSS
71 CLKI14
72 RTCAS
73 RTCDS
74 RTCRW
75 NDRAMWE
76 HLDA
77 NAEN1
78 NAEN2
79 CLK2AIN
80 VDD
81 VSS
82 XD0
83 XD1
84 XD2
85 XD3
86 XD4
87 XD5
88 XD6
89 XD7
90 VSS
91 MA10
92 MA09
93 MA08
94 MA07
95 MA06
96 MA05
97 MA04
98 MA03
99 MA02
100 VDD
101 MA1
102 MA0
103 NPERR0
104 NCAS00
105 SA0
106 RC
107 NCAS01
108 NCAS10
109 NCAS11
110 VSS
111 NCAS20
112 NCAS21
113 NC
114 NCAS30
115 NCAS31
116 DMAREQ
117 PWRGD
118 NRAS0
119 NRAS1
120 VDD
121 VSS
122 NRAS2
123 NRAS3
124 NOWS
125 IRQ13
126 NCPURD
127 NENHI
128 NENLO
129 SBA
130 VSS
131 CTLOFF
132 NBUFFRD
133 NMEMDIR
134 DIRODD
135 NGATODD
136 NC
137 NC
138 NROMOE
139 VSS
140 VDD
141 NINTA
142 NC
143 NNA
144 NCOPRDY
145 NCOPERR
146 NCOPBSY
147 COPEREQ
148 NBLE
149 NBHE
150 VSS
151 NPERR1
152 NC
153 WR
154 DC
155 MIO
156 CPUHLDA
157 NADS
158 CPURST
159 CPUCLK
160 VDD

II. PIN DESCRIPTION SL9252

SYMBOL	PIN	TYPE	DESCRIPTION
			CLOCK AND RESET SIGNALS
CLKI14	71	I	Clock In 14 MHz. 14.31818 MHz input from oscillator.
CLK2AIN	79	I	Input Clock used to generate CLK2 and clock internal state machine. It is twice the frequency of the CPU clock.
CLKATIN	51	I	Asynchronous AT Clock Input. Should be twice the BUSCLK frequency. Generated from the oscillator.
CLK2OUT	31	O	Clock 2 Output to CPU.
CLK8042	69	O	CLK8042 is CLKI14 divided by two. It is the keyboard controller clock.
COPRESET	33	O	Reset 387 is an active HIGH output. It is generated in response to any one of the following signals: PWRGD, RC, and PS/2 Fast Reset. It is also asserted when I/O port 00F1 is written to. The signal is active for 96 CPUCLK cycles.
CPURST	158	O	Reset Signal to the CPU is an active HIGH output. It is generated in response to any one of the following signals: PWRGD, RC and PS/2 fast reset.
NDRVRST	63	O	Device Reset is an active LOW output. It is used to reset the SL9025 Address Controller and Keyboard Controller.
PWRGD	117	I	Power Good is an active HIGH input from the power supply. A reset switch can be connected to this.
SYSCKOUT	49	O	System Clock Out is a free running system clock generated by dividing CPUCLK by 2. In synchronous mode this is synchronized with NADS. In asynchronous mode, this is generated from CLKATIN.
TIMCLK	42	O	1.19 MHz Timer Clock.
			CPU INTERFACE SIGNALS
A2-23	3,4,,5,6,7,8,9,11, 12,13,14,15,16,17 18,19,21,22,24, 25,26	I/O	These are inputs for CPU, DMA, and AT bus MASTER accesses and outputs during refresh cycle. A2 to A11 has the refresh address (all with MSB). A12 to A23 are LOW during refresh.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			CPU INTERFACE SIGNALS Cont'd
A20GATE	68	I	Internal Adress 20 is forced LOW when A20GATE is LOW and is same as generated by CPU when A20GATE is HIGH.
ADVALE	61	O	Advanced Address Latch Enable from the memory control logic. It latches local bus address for the system bus.
CPUA20	23	I/O	CPU Address Bus, bit 20. Output for AT bus MASTER accesses.
CPUCLK	159	O	Clock synchronized with 386SX internal clock. It is CLK2 divided by two.
CPUNMI	37	O	CPU Non-Maskable Interrupt, generated from PERR or IOCHCK. Output to 80386.
CPUPEREQ	34	O	CPU Processor Extension Request. When active (HIGH) it indicates to CPU that NPX is ready for data transfer to/from its data FIFO. When FIFO is empty, this signal is negated. CPUPEREQ connects directly to the PEREQ pin on the CPU.
DC	154	I	CPU Status Signal. Differentiates between Data and Control instructions.
MIO	155	I	Memory Input/Output signal from the CPU. When HIGH, it indicates a memory cycle, when LOW, it indicates an I/O cycle.
MODA20	58	I/O	CPU Address 20 gated with A20GATE.
NADS	157	I	Address Strobe is an active LOW input generated by the CPU. When asserted it indicates the start of a new cycle.
NNA	143	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
WR	153	I	CPU output control signal Write.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			MEMORY INTERFACE SIGNALS
MA0-MA10	102,101,99,98,97, 96,95,94,93,92,91	O	RAM Address Bus Output. Directly drives DRAM address inputs.
NCAS00	104	O	Memory column address strobe. Asserted when CPU, DMA or MASTER is accessing Bank 0, byte 0.
NCAS01	107	O	Memory Column Address Strobe for Bank 0, byte 1.
NCAS10	108	O	CAS for Bank 1, byte 0.
NCAS11	109	O	CAS for Bank 1, byte 1.
NCAS20	111	O	CAS for Bank 2, byte 0.
NCAS21	112	O	CAS for Bank 2, byte 1.
NCAS30	114	O	CAS for Bank 3, byte 0.
NCAS31	115	O	CAS for Bank 3, byte 1.
NCOPBSY	146	I	Numerical Coprocessor (NPX) Busy is an active LOW input indicating that NPX is currently executing a command. It is used to generate busy signal to the CPU, NCPUBUSY.
NDRAMWE	75	O	Active Low Memory Write signal. Used to drive DRAM write input.
NMEMDIR	133	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is used to drive SL9020 NMEMDIR input.
NPERR0	103	I	Parity Error to byte 0 (D0 - D7).
NPERR1	151	I	Parity Error to byte 1 (D8 - D15).
NRAS0-3	118,119,122,123	O	Row Address Strobes for Banks 0,1,2 and 3 for the on-board memory. Generated during CPU, DMA or MASTER cycle for memory access. Used to directly drive DRAM RAS inputsfor banks 0 - 3.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			MEMORY INTERFACE SIGNALS Cont'd
NROMOE	138	I/O	Bi-directional pin which enables ROM output during ROM read cycles. During power-up, this is an input, and if pulled LOW an 8 bit ROM is assumed. Connects directly to ROMOE pin.
			COPROCESSOR INTERFACE SIGNALS
COPEREQ	147	I	NPX Peripheral Request is an active HIGH input from NPX. When asserted it causes CPUPEREQ to assert, indicating to the CPU that NPX is ready to transfer data to/from its data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated.
IRQ13	125	O	Interrupt Request 13 is an active HIGH output which indicates an interrupt from the numeric coprocessor. It connects to the SL9030 pin IRQ13.
NCOPERR	145	I	NPX Error is an active LOW input from 80387SX. When asserted it indicates that a non-maskable exception has occurred during the current command cycle. It is used to generate NCPUERR.
NCOPRDY	144	I	Coprocessor Ready is an active LOW input from the NPX to terminate an NPX bus cycle.
NCPUBSY	35	O	CPU Busy is an active LOW output to the CPU indicating that the NPX is busy executing a command. It connects to the CPU pin BUSY.
NCPUERR	36	O	CPU Error is an active LOW output from the NPX to the CPU indicating that an unmasked error condition exists. NCPUERR connects to the ERROR input pin on the CPU.
STENO	38	O	Status Enable is an active HIGH output. This pin serves as a chip select for the 80387SX. When inactive, it forces the NPX outputs NBUSY, PEREQ, NERROR and NRDY into floating state.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			BUS CONTROL AND INTERFACE SIGNALS
A1	2	I/O	Input for CPU, DMA and AT bus MASTER. Output for Refresh cycles. During refresh cycles, refresh counter LSB is output on this.
ADVALE	61	O	Advanced Address Latch Enable from the memory control logic. It latches local bus address for the system bus.
BALE	52	O	Buffered Address Latch Enable. Directly drives AT slot signal BALE.
CTLOFF	131	O	Control Output Flag. Rising edge clocks data from SD [7:0] to D[7:0] latches during Bus-conversion cycles. Connects directly to the SL9020 pin CTLOFF.
DIRODD	134	O	Direction ODD. Controls data transfer direction between SD[7:0] and SD[15:8] in the SL9020 Data Controller. NGAT1 must be asserted. It is used during data conversion (8 bit SLOT Read/Writes) cycles.
IOCHRDY	62	I/O	I/O Channel Ready is an active HIGH input from the AT bus. When LOW it indicates a not ready condition and inserts wait states in AT bus or peripheral bus cycles. It is used to generate NCPURDY. It is an output during NPX reset cycle.
NAEN1,2	77,78	I	DMA Enable 1,2 are active LOW inputs from the SL9030. When NAEN1 is asserted LOW it indicates an 8-bit DMA cycle. When NAEN2 is asserted LOW it indicates a 16-bit DMA cycle. When both are HIGH it indicates that a non-DMA device owns the system's bus controls. They should not be LOW at the same time. They are used to generate direction control signals NSBHE, SBA, NENHI and NENLO.
NBLE	148	I	Active LOW Byte Enable 0 from CPU.
NBHE	149	I	Active LOW Byte Enable 1 from CPU.
NBUFFRD	132	O	Direction control for buffer between SD Bus and XD Bus.
NCPURD	126	O	CPU Read is an active LOW output to the SL9020 Data Controller that sets the direction of data between D0-D15 and SD0-SD15. When asserted, the direction is from SD to D.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			BUS CONTROL AND INTERFACE SIGNALS Cont'd
NCPURDY	29	O	Ready to CPU to terminate the cycle. Ready for local RAM, ROM (16 or 8 bit) accesses, on-chip I/O and AT bus accesses are generated in SL9252. External Coprocessor ready is input to 9252 and is OR'd with internal ready.
NENHI	127	O	Enable HIGH byte to the SL9020 Data Controller, is asserted LOW to enable HIGH byte data transfer between D8-D15 and SD8-SD15.
NENLO	128	O	Enable LOW byte to the SL9020 Data Controller, is asserted LOW to enable LOW byte data transfers between D0-D7 and SD0-SD7.
NGATODD	135	O	This is asserted LOW to enable the data buffer between HIGH byte and LOW byte of SD Bus. It is used in bus conversion cycles to assemble 8 bit bytes into 16 bit words in the SL9020 Data Controller.
NIOCHCK	64	I	I/O channel check. Active LOW signal from AT bus to assert CPUNMI.
NIOCS16	46	I	Peripheral I/O Chip select 16 is an active LOW input. It is asserted from AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When HIGH it implies an 8-bit I/O transfer. It is used to control NGATODD.
NIOR	54	I/O	Input/Output Read is an active LOW bi-directional signal. It is an output when CPU is reading peripheral or AT bus ports. It is an input for DMA and AT bus Master.
NIOW	55	I/O	Input/Output Write is an active LOW bi-directional signal. It is an output when CPU is writing to peripheral or AT bus ports. It is an input for DMA and AT bus Master.
NMASTER	43	I	External Master is an active LOW input from the AT bus. When asserted, indicates that an external master device is currently active.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			BUS CONTROL AND INTERFACE SIGNALS Cont'd
NMCS16	47	I	Memory Chip Select 16 is an active LOW input from the AT bus. When asserted indicates a 16 bit memory cycle. When HIGH it implies an 8 bit memory transfer. It is used to control NGATODD.
NMEMR	45	I/O	Memory Read is an active LOW bi-directional signal. It is an output when CPU is reading peripheral or AT bus memory, and during refresh cycle. It is an input for DMA and AT bus Master.
NMEMW	44	I/O	Memory Write is an active LOW bi-directional signal. It is an output when CPU is writing peripheral or AT bus memory. It is an input for DMA and AT bus Master.
N0WS	124	I	Zero Wait State is an active LOW input from the AT System bus. It causes termination of a bus cycle.
NSBHE	48	I/O	Byte HIGH Enable is an active LOW bi-directional pin for the AT bus. It indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output for CPU and DMA cycles and an input for an external master cycle.
NSMEMR	56	O	System Memory Read is active for a read access to lower 1 Meg memory. All other times it is tri-stated.
NSMEMW	57	O	System Memory Write is active for a write access to lower 1 Meg memory. All other times it is tri-stated.
SA0	105	I/O	System Bus Address 0-bit. It is a bi-directional pin. It is an output for CPU, Refresh and an input for DMA and AT bus Master.
SBA	129	O	Select Data Buffer Data. This signal drives the SL9020 Data Controller. When HIGH it selects latched SD Bus LOW byte data during bus conversions cycles. When LOW, unlatched SD Bus LOW byte data will pass onto D Bus.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			HOLD INTERFACE SIGNALS
CPUHLDA	156	I	CPU Hold Acknowledge. It is active HIGH when bus is granted in response to hold request (HOLD). It is used to generate HLDA.
CPUHOLD	32	O	Hold is asserted HIGH whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU.
DMAREQ	116	I	DMA Request is asserted HIGH to request a bus from CPU. It initiates hold request (HOLD) to the CPU for a DMA cycle to begin. Normally, SL9030 IPC's CPUHRQ is connected to this.
HLDA	76	O	Hold Acknowledge is an active HIGH output to the SL9030 Integrated Peripheral Controller. When asserted it indicates that CPU has released its control on the local bus in favor of another bus master device (DMA external master). It is generated by resynchronizing CPUHLDA with CPUCLK.
NREFRESH	53	I	On-board RAM refresh signal.
			PERIPHERAL INTERFACE SIGNALS
N8042CS	67	O	Active LOW keyboard controller chip select.
NINTA	141	O	Interrupt Acknowledge is an active LOW output for the interrupt controller. It is also used to direct data from the XD bus to SD bus during an interrupt acknowledge cycle.
RC	106	I	External CPU Reset is an active LOW input. When asserted it resets the CPU by generating CPURST. It is connected to the Keyboard Controller.
RTCAS	72	O	Active HIGH Real Time Clock Address Strobe.
RTCDS	73	O	Active LOW Real Time Clock Address Strobe.
RTCRW	74	O	Active LOW Real Time Clock Write Enable.
SPKCLK	65	O	Speaker clock.

PIN DESCRIPTION SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			PERIPHERAL INTERFACE SIGNALS Cont'd
SPKDATA	66	O	Active HIGH speaker data output. This is used to gate the timer tone signal to the speaker.
XD0-XD7	82,83,84,85, 86,87,88,89	I	Peripheral data bus to read/write SL9252 registers.
			POWER AND GROUND SIGNALS
VDD	20,40,60,80,100, 120,140,160	-	+5V. Power.
VSS	1,10,30,41,50,59, 70,81,90,110,121, 130,139,150	-	0V. Ground.
			UNCONNECTED PINS
NC	27,28,39,113,136, 137,142,152	-	No Connection

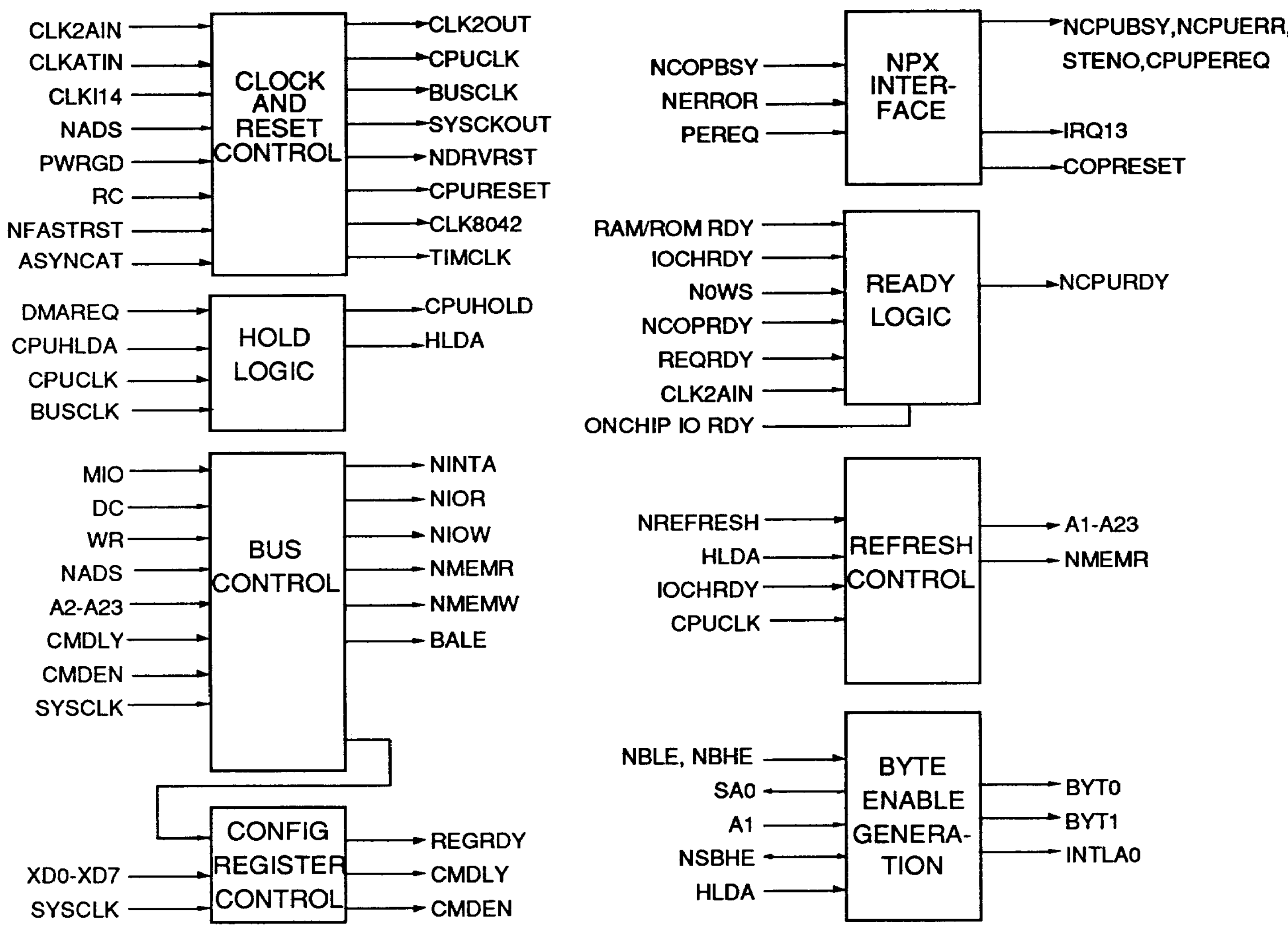


Fig. 2 System Control Logic Block Diagram

III. SYSTEM CONTROL LOGIC

Figure 2 shows the block diagram of System Control Logic. System Control is divided into nine sections:

a. Clock and Reset Control
b. Hold Logic
c. Bus Control Logic
d. Coprocessor Interface
e. Ready Logic
f. Refresh Counter Logic
g. Byte Enable Generation
h. PS/2 Compatible Port 92

a. Clock and Reset Control

The clock inputs to the chip are:

1. CLK2AIN
2. CLKI14.

The processor clock, CLK2, CPUCLK, and system clock SYSCKOUT are derived from CLK2AIN. In asynchronous mode SYSCKOUT is derived from CLKATIN. Asynchronous clock selection for the system clock is performed using the control bit ASYNCAT in register 18h. CLKI14 is the 14MHz clock used to derive CLK8042 and TIMCLK.

SL9252 generates CPU reset (CPURST), Coprocessor reset (COPRESET) and system bus reset (NDRVRST) from PWRGD, RC and PS/2 compatible port 92 fast reset. External reset through a switch can be provided by pulling PWRGD line low. RC is the keyboard controller output that generates software reset. CPURST will go active from 3 to 11 CPUCLKs after RC is asserted. It will go inactive either 16 CPUCLKs later or 16 CPUCLKs after RC is negated. An equivalent high speed reset can be generated through port 92 bit 0. As with RC and fast reset, CPURST will go active within 3 to 11 CPUCLKs of detecting the shutdown command and be negated 16 CPUCLKs later. CPURST is always asserted and negated at the beginning of Phase 1.

b. Hold Logic

The hold request to CPU and hold acknowledge to external devices (e.g. SL9030) are synchronized with CPUCLK and BUSCLK. External devices requesting the bus should assert DMAREQ and use HLDA as the hold acknowledge.

c. Bus Control Logic

SL9252 contains logic to generate bus command and control signals in four basic modes. The most commonly used is the CPU mode. This is active whenever there is no HLDA. The three other modes, DMA mode, MASTER mode and REFRESH mode, can be active only when HLDA is high.

During CPU mode the commands NMEMR, NMEMW, NIOR, NIOW are in output mode. One of these is asserted for an AT bus or peripheral bus access. The command delay can be programmed separately for read and write accesses through register 1Bh.

c. Bus Control Logic, cont'd

The bus activity and direction of the SL9252 pins depend on the mode. DMA is master when NAEN1 or NAEN2 (but not both) is asserted during HLDA. If NREFRESH is asserted during HLDA, it is in refresh mode. AT bus Master is master when NMASTER is asserted during HLDA. The following table lists the various signals and their direction for the modes mentioned above:

SIGNAL	MODE			
	CPU	DMA	AT Bus MASTER	REFRESH
NMEMR	O	I	I	O
NMEMW	O	I	I	I
NIOR	O	I	I	I
NIOW	O	I	I	I
SA0	O	I	I	I
NSBHE	O	O	I	O
A2 - A23	I	I	I	O
CPUA20	I	I	O	I
LA20	O	O	I	O

O = Output I = Input

Table 1 Signal Direction Descriptions

d. Coprocessor Interface

SL9252 generates reset for coprocessor 387 and is asserted whenever CPURST is asserted. It can also be activated through an I/O write to address 0F1h. It is active for 96 CPUCLK cycles. IOCHRDY will be asserted when COPRESET is active. It will be negated 95 CPUCLKs after COPRESET is negated.

From reset until the first CPU cycle, coprocessor error NERROR is routed to the CPU as NCPUERR. If coprocessor error is detected during coprocessor busy period, STENO is negated and interrupt request 13 is asserted. It also latches CPUBUSY. CPUBUSY is asserted to prevent the processor from accessing the co-processor until the error handling routine is completed. The interrupt handler clears the latched BUSY condition, by performing a dummy write to I/O port 0F0h. STENO and IRQ13 are also negated by writing to port 0F0h.

e. Ready Logic

SL9252 generates ready for DRAM, on-chip I/O and bus accesses. Wait states for DRAM accesses can be programmed separately for HIT and MISS cycles through register 08h. For the same number of wait states the pipeline mode ready will be one CPUCLK later compared to non-pipeline mode ready. On-chip I/O accesses have 1 wait state. The bus access wait states can be programmed separately for 16 bit and 8 bit devices. They can also be programmed separately for memory and I/O devices using registers 19h and 1Ah. IOCHRDY can be used to extend the cycle. Wait states are introduced until IOCHRDY is de-asserted. N0WS overides IOCHRDY and programmed wait states and the current cycle is terminated as soon as it is detected internally and synchronized to CPU CLK2. These three ready sources are combined with NCOPRDY (coprocessor ready) to generate the ready to the CPU.

f. Refresh Logic

SL9252 contains logic for refresh counter and refresh RAS generation. Refresh cycle starts when NREFRESH is asserted low and HLDA is active. Staggered refresh is enabled by setting the two stagger RAS control bits in register 12h. During refresh NRAS0-3 are asserted low, NCAS00 and NCAS31 are held high, and the current bus state is ignored. Refresh counter is incremented at the end of the refresh cycle. Refresh address is output on A1 to A11. NMEMR is asserted during the refresh cycle.

g. Byte Enable Generation

Four byte enable controls for asserting CAS are generated using the four byte enables from the CPU, A1, SA0 and NSBHE. In CPU mode the four byte enables from the CPU are selected. During DMA and MASTER address input A1 decides the word, and SA0 and NSBHE decide the low or high byte within a word. During DMA mode, NSBHE is generated internally by SL9252, based on 8 bit or 16 bit DMA.

h. PS/2 Compatible Port 92

PS/2 compatible port 92 to issue fast reset and fast A20GATE are provided in SL9252. On reset, fast reset logic is disabled. It can be enabled through bit 1 of register 13h.

SL9252's Memory Control Logic section provides the control interface between CPU, DMA, MASTER and local DRAM for non-interleave and interleave modes of operation in page mode and non page mode. In page mode both single page and multiple pages can be active simultaneously.

In page non-interleave mode there is only one page active. The page size is 2K bytes for 256K, 4K bytes for 1M and 8K bytes for 4M memories. It is doubled for 2-way word interleave and quadrupled for 4-way word interleave. For multiple page interleave there can be a maximum of four different pages: one page for each bank with four banks. Page size of each of these pages is the same as in page non-interleave mode.

IV. MEMORY CONTROL LOGIC

Figure 3 shows the block diagram of the Memory Control Logic. It is logically divided into six sections:

a. Address Decode
b. HIT/MISS Detection
c. RAS/CAS Logic
d. Memory Address Generation
e. Next Address and Ready Logic
f. ROM Data Conversion Logic

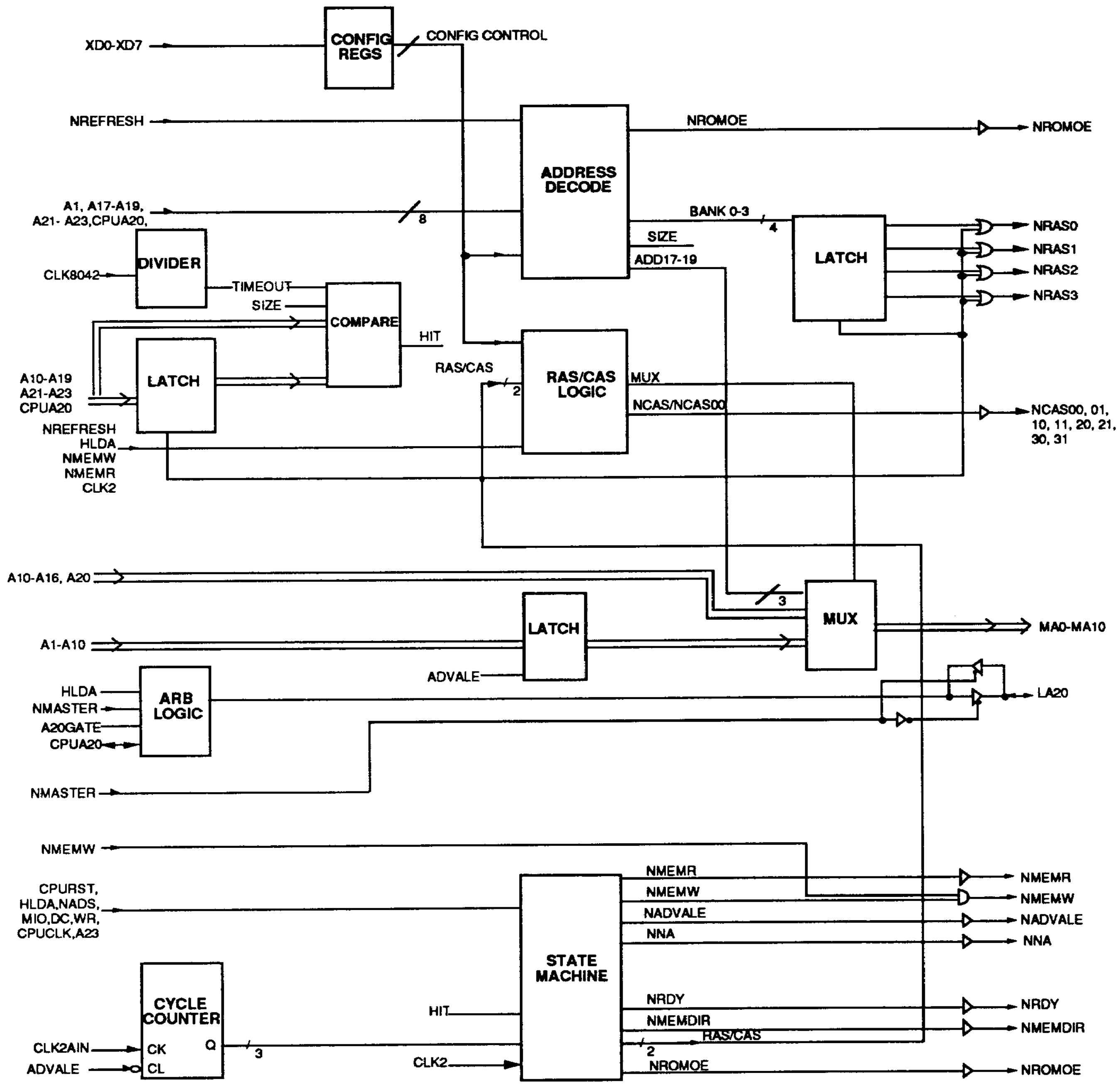


Fig. 3 Memory Control Logic Block Diagram

a. Address Decode

In addition to shadow and remap decoding, SL9252 provides all necessary circuitry to decode on-board RAM, ROM, and on-chip I/O. Sixteen memory type and select combinations can be chosen to support one to four banks using 256K, 1M, 4M or a mix of these using regular and static column DRAMs. The controller can be configured for 640K bytes to 64M bytes. The memory address range for different bank select codes for page mode (non-interleave and multi-page interleave) and non-page mode are shown in Table 2. The bank selection code is written to register 11h.

For page word interleave, the selection code and size are the same as shown in Table 2 except that the address range of the bank depends on address A2 for 2-way interleave and addresses A2 and A3 for 4-way interleave.

D3	D2	D1	D0	BANK 0	BANK 1	BANK 2	BANK 3	MEMORY
0	0	0	0	0-512K				512K
0	0	0	1	0-512K	512K-640K/SHDW			1M
0	0	1	0	0-512K	512K-640K/SHDW	1M-1M + 512K		1M + 512K
0	0	1	1	0-512K	512K-640K/SHDW	1M-1M + 512K	1M + 512K-2M	2M
0	1	0	0	0-512K	512K-640K/SHDW/1M-2M + 512KSHDW			3M
0	1	0	1	RESERVED				
0	1	1	0	0-512K	512K-640K/SHDW	1M-3M		3M
0	1	1	1	0-512K	512K-640K/SHDW	1M-3M	3M-5M	5M
1	0	0	0	0-512K/1M-8M/SHDW				8M
1	0	0	1	RESERVED				
1	0	1	0	RESERVED				
1	0	1	1	RESERVED				
1	1	0	0	0-640K/1M-4M/SHDW				2M
1	1	0	1	0-640K/1M-4M/SHDW	2M-4M			4M
1	1	1	0	0-640K/1M-4M/SHDW	2M-4M	4M-6M		6M
1	1	1	1	0-640K/1M-4M/SHDW	2M-4M	4M-6M	6M-8M	8M

Table 2 Bank Select Codes and Memory Address Range

'SHDW' corresponds to the 384K memory available from 640K to 1M. This area corresponds to the shadow address range or remap range. Shadow address range is decoded based on the bits set in registers 00h to 07h and the remap decoding is based on the remap register (09h) setting. Remap RAM address is always above the maximum DRAM memory specified in Table 2 for the selected memory select code. The programmer should make sure two or more address ranges do not overlap to the same physical area.

On reset, ROM is decoded from FE0000h to FFFFFFh and from 0F0000 to 0FFFFF. The second area can be disabled by resetting bits 0 and 1 in ROM control register 0Ch. Local ROM can be decoded from 0C0000 to 0EFFFF in 16k granularity by setting the control bits in ROM control register 0Ah and 0Bh. For the selected address range NROMOE is asserted active low.

b. Hit/Miss Detection

SL9252 supports both page non-interleave and page interleave modes of operation. In page mode, there is only one page active and the page size is 2K bytes for 256K, 4K bytes for 1M and 8K bytes for 4M memories. The page size is doubled for 2-way word interleave and quadrupled for 4-way word interleave. For multi-page interleave, there can be a maximum of four different pages, one page for each bank with four banks. Page size of each of these pages is the same as in page non-interleave mode.

After reset and after every HLDA cycle the first access to memory is treated as a MISS cycle asserting RAS and CAS as programmed in registers 0Dh, 0Eh, 0Fh, and 13h for MISS cycles. The page number is stored internally in a page register, and at the end of the cycle RAS is left low and CAS returned high. During all subsequent accesses, the access page number is compared with the stored page number and a HIT detected if they are same. If a mismatch (MISS) is detected, RAS is negated and asserted again after the programmed number of clocks for RAS precharge. The new page number is stored for subsequent cycle comparisons. For word page interleave on a MISS all bank RASes are negated and asserted together. For multiple page interleave only the bank for which there is a MISS will have its RAS negated. Thus, in multi-page interleave different banks can have different active pages. In non-page mode each access is treated as a MISS cycle.

c. RAS/CAS Logic

On-board memory timing is programmable as a multiple of CLK2. This gives unlimited flexibility in matching DRAM specifications to the CPU speed for optimal performance and cost. Four configuration registers are used for programming RAS and CAS precharge, and RAS to column address delay. These values can be different for HIT and MISS cycles and for read and write cycles. CAS is negated for every cycle and asserted after the specified number of CLK2's. RAS is negated for a MISS cycle and asserted after the specified number of CLK2's. The RAS and CAS access times are provided by programming the number of wait states correctly. The programmed values affect only CPU accesses. DMA, REFRESH and MASTER timings are fixed as shown in the timing diagrams. During refresh cycles, support for 1 or 2 CLK2 staggered refreshing is provided. During staggered refreshing, bank0 RAS is asserted first and bank3 RAS asserted last.

RAS timeout logic may be optionally enabled by setting bit 5 in register 10h to ensure that the RAS active time limit is not violated during page mode operation. If RAS remains active for a period greater than the selected period, RAS is negated during the next CPU access. The cycle is treated as a MISS cycle even if the access is to the same page.

d. Memory Address Generation

SL9252 provides the necessary circuitry to multiplex the access address as row address and column address. The physical address used for row and column depends on the memory size and mode of operation. Table 3 gives the address generation process. Row address hold time (RAS to column address) can be programmed through register 0Dh.

MODE	MEMORY		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10
NON-INTERLEAVE	256K	ROW	11	12	13	14	15	16	17	18	10		
		COL	1	2	3	4	5	6	7	8	9		
	1M	ROW	11	12	13	14	15	16	17	18	19	20	
		COL	1	2	3	4	5	6	7	8	9	10	
	4M	ROW	21	12	13	14	15	16	17	18	19	20	22
		COL	1	2	3	4	5	6	7	8	9	10	11
2-WAY INTERLEAVE	256K	ROW	11	12	13	14	15	16	17	18	19		
		COL	10	2	3	4	5	6	7	8	9		
	1M	ROW	21	12	13	14	15	16	17	18	19	20	
		COL	11	2	3	4	5	6	7	8	9	10	
	4M	ROW	21	22	13	14	15	16	17	18	19	20	23
		COL	11	2	3	4	5	6	7	8	9	10	12
4-WAY INTERLEAVE	256K	ROW	20	12	13	14	15	16	17	18	19		
		COL	10	11	3	4	5	6	7	8	9		
	1M	ROW	21	22	13	14	15	16	17	18	19	20	
		COL	11	12	3	4	5	6	7	8	9	10	
	4M	ROW	21	22	23	14	15	16	17	18	19	20	24
		COL	11	12	3	4	5	6	7	8	9	10	13

TABLE 3 Address Generation

e. Next Address and Ready Logic

SL9252 provides logic for pipeline mode and non-pipeline mode CPU operation. Setting bit 3 in register 12h disables pipeline operation. In pipeline mode the next address to CPU is asserted for on-board DRAM accesses before ready is asserted. For the same number of wait states the ready for non-pipeline operation will be one CPUCLK earlier than in pipeline operation. The number of wait states for HIT and MISS can be programmed separately. In addition, the wait state for write cycles can be one less than the read. Next address is not asserted for ROM on-chip I/O and bus accesses.

f. ROM Data Conversion Logic

With SL9252, the system designer has the flexibility to choose 8 bit or 16 bit ROM. If NROMOE is pulled low on reset, 8 bit ROM is assumed and SL9252 does the necessary data conversion cycles for ROM accesses. During word access to ROM, the low byte is accessed first (SA0 = 0) and latched. SA0 is then toggled to 1 and high byte is accessed. Ready to CPU is issued after the specified number of wait states for the second access. The first access also assumes the same number of wait states.

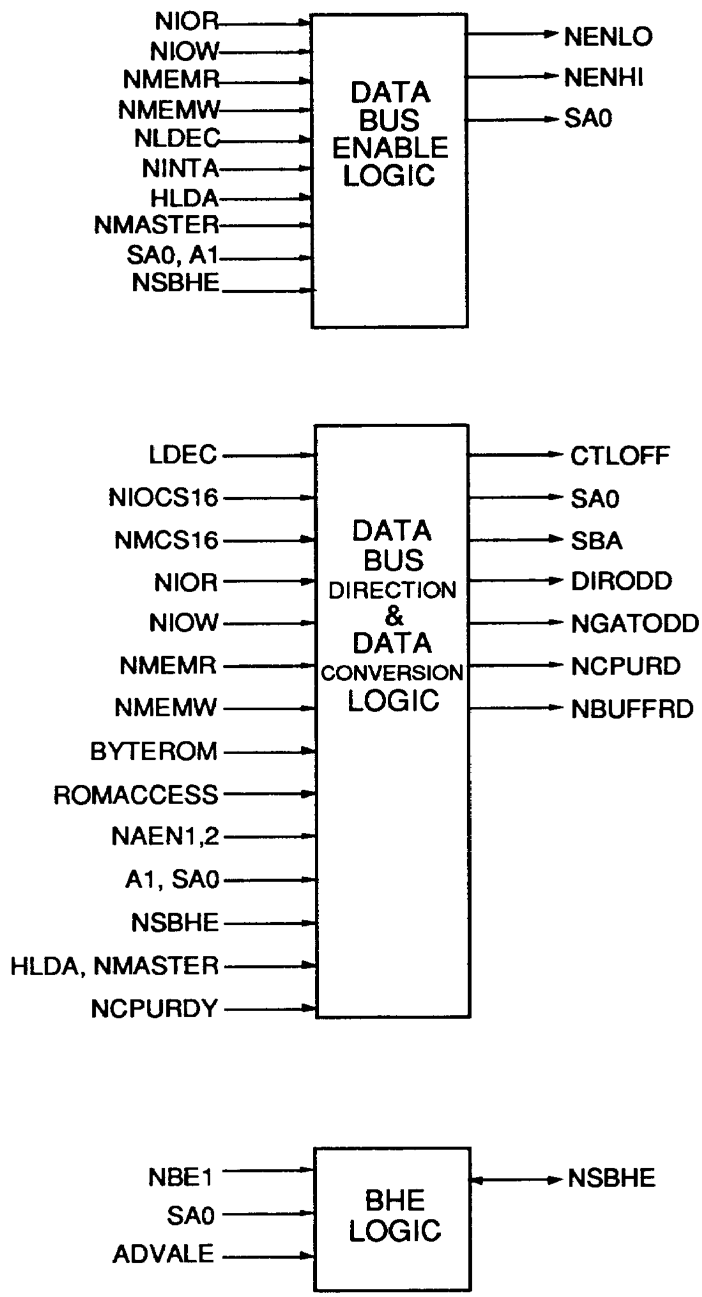


Fig. 4 Data Control Logic Block Diagram

V. DATA CONTROL LOGIC

Figure 4 shows the block diagram of the Data Control Logic. The three major blocks are:

a. Bus Enable Logic
b. Bus Direction and Data Conversion Logic
c. High Byte Enable Logic

a. Bus Enable Logic

SL9252 provides logic support for use of an external SL9020 Data Controller, or TTL buffers and latches. SL9252 generates necessary buffer enable controls for these two modes of operation. System control register 019h, bit 0 must be set if the SL9020 Data Controller is used with DRAM and ROM on MD bus. The following five enable controls are used to enable the buffers between D and SD bus. NENLO and NENHI enable the low word, low and high byte respectively. NGATODD enables the swap buffer between SD0-SD7 and SD8-SD15.

b. Bus Direction and Data Conversion Logic

The following signals control direction of AT bus and peripheral bus data buffers: NCPURD for low and high bytes of low word, DIRODD for the SD0-SD7 to SD8-SD15 swap buffer, and NBUFFRD for XD0-XD7 to SD0-SD7 buffer. NMEMDIR is used with SL9020 to direct data to and from memory data bus when local memory is on MD bus. The following table lists directions of the data bus signals:

Signal	Direction	
NCPURD	0	SD to D
	1	D to SD
DIRODD	0	SD8-SD15 to SD0-SD7
	1	SD0-SD7 to SD8-SD15
DIR2	0	SD to D
	1	D to SD
NBUFFRD	0	XD0-XD7 to SD0-SD7
	1	SD0-SD7 to XD0-XD7
NMEMDIR	0	MD to D
	1	D to MD

Table 4 Signal Directions

In addition to these enable and direction controls, SL9252 provides a clock and select signal for data conversion during word access to a byte port. CTLOFF is used to clock the low byte data, and SBA is used to select the latched data.

c. High Byte Enable Logic

NSBHE is AT bus byte high enable signal and is an input during MASTER mode and output at all other times. During CPU mode, this is asserted whenever CPU acceses high byte of either word. During 8 bit DMA it is of opposite polarity to SA0 and during 16 bit DMA it is low.

VI. PERIPHERAL CONTROL LOGIC

Figure 5 shows the block diagram of Peripheral Control Logic. It provides logic for the following:

a. Peripheral Address Decoding
b. Port B Logic

a. Peripheral Address Decoding

SL9252 provides address decoding logic to support the Real Time Clock and Keyboard Controller. RTCAS, RTCRW and RTCDS are generated for write access to 70h, 71h, and read access to 70h respectively. Keyboard controller chip select goes active for port 60h read and write accesses. The number of wait states for these accesses depends on the programmed number of wait states for bus accesses. These devices are to be located on XD bus.

b. Port B Logic

SL9252 also provides the port B (address 61h) logic for CPUNMI, and speaker data.

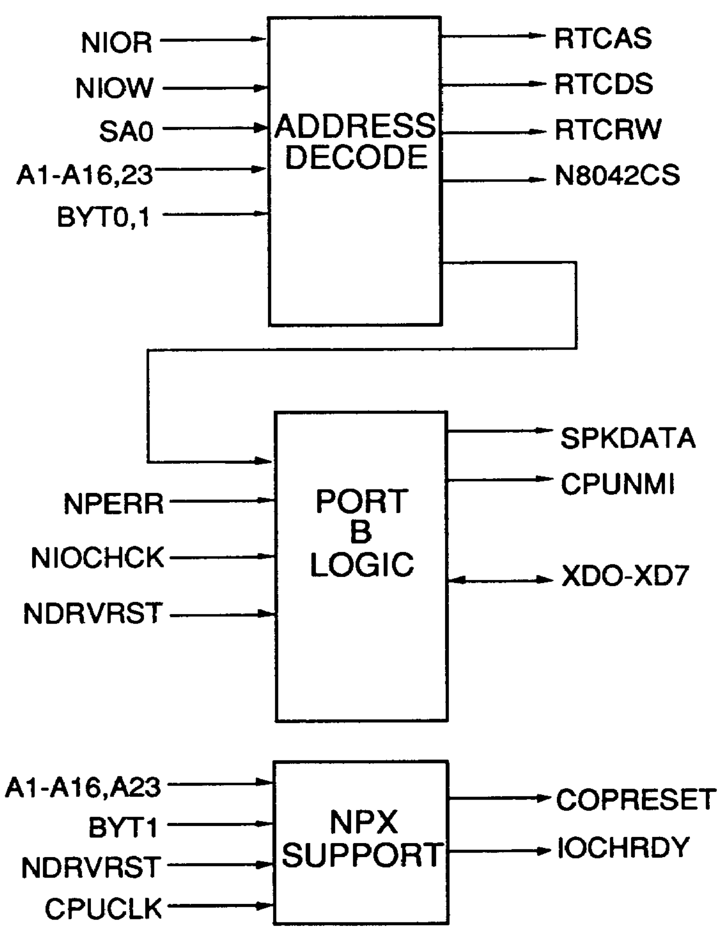


Fig. 5 Peripheral Control Logic Block Diagram

VII. CONFIGURATION REGISTERS

SL9252 provides 28 configuration registers for all programmable functions in the chip. All these registers are accessed through an index/data addressing scheme. Only one I/O address is used to access both index and data registers. The address defaults to 0122h after reset and can be remapped to any other unused I/O address (must be on byte 1 boundary) between 0000h and FFFFh by loading the new I/O address into the relocation registers. The addresses from these registers are transferred to a pipeline register, for comparing, with a write to configuration register 3 (using the unrelocated address i.e., 0122h) with bit 0 = 1. After this the temporary relocation registers are also in the new address space until the reset, when it defaults to 0122h.

The data registers are selected by writing their addresses in the index register. An internal pointer is used to determine whether the on-chip I/O write is for the index or data registers. After reset, the pointer points to the index register. Any write to the index register or data register will toggle the pointer. Only data registers can be read back and any read to the data registers will leave the pointer pointing to the index register.

The following table lists all the configuration registers by their index address, name and description:

INDEX ADDRESS	NAME	REGISTER
00	SDWREG0	Shadow control 0
01	SDWREG1	Shadow control 1
02	SDWREG2	Shadow control 2
03	SDWREG3	Shadow control 3
04	SDWREG4	Shadow control 4
05	SDWREG5	Shadow control 5
06	SDWREG6	Shadow control 6
07	SDWREG7	Shadow control 7
08	RAMWAIT	RAM wait state select
09	REMAP	Remap
0A	ROMCTL1	Local ROM control register 1
0B	ROMCTL2	Local ROM control register 2
0C	ROMCTL2	Local ROM control register 3
0D	RASTIM	RAS timing register
0E	CASTIM1	CAS timing register 1
0F	CASTIM2	CAS timing register 2
10	DISMEM	Disable to 0K
11	MEMTYPE	Memory type and size select
12	CONFIG1	Configuration register 1
13	CONFIG2	Configuration register 2
14	CONFIG3	Configuration register 3
15	IOMAPLOW	Relocation register low
16	IOMAPHI	Relocation register high
17	Reserved	
18	SYSCTL	System control register
19	WAIT16	System bus 16 bit device wait state select
1A	WAIT8	System bus 8 bit device wait state select
1B	CMDDLY	System bus command delay
1C	Reserved	
1D	Reserved	
1E	Reserved	
1F	RASMAP	RAS map register

Table 5 Configuration Registers

REGISTER BIT(S) DESCRIPTIONS

SHADOW CONTROL REGISTERS

Index address (hex) : 00 to 07

These 8 registers control the use of 640K - 1M byte in 16K granularity. All are read/write registers. The most significant 2 bits always read back as zeros. Two bits control one 16K region as defined below.

SDWRx	SDWWx	Function
0	0	Read/Write to system bus
0	1	Read system bus, write local DRAM
1	0	Read local DRAM, write system bus.
1	1	Read/Write local DRAM

(x : 00h to 17h)

Note: Local ROM is decoded from 0F0000 to 0FFFFF after reset. Local ROM should be disabled through ROM control register for shadowing ROM.

Shadow Control Register 0, Index 00h, R/W

Register 00h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWR2	SDWW2	SDWR1	SDWW1	SDWR0	SDWW0

- D1, D0: Shadow control for 0A0000 to 0A3FFF.
- D3, D2: Shadow control for 0A4000 to 0A7FFF.
- D5, D4: Shadow control for 0A8000 to 0ABFFF.
- D7, D6: Reserved for future use. Must be set to 0.

Shadow Control Register 1, Index 01h, R/W

Register 01h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWR5	SDWW5	SDWR4	SDWW4	SDWR3	SDWW3

- D1–D0: Shadow control for 0AC000 to 0AFFFF.
- D3–D2: Shadow control for 0B0000 to 0B3FFF.
- D5–D4: Shadow control for 0B4000 to 0B7FFF.
- D7–D6: Reserved for future use. Must be set to 0.

Shadow Control Register 2, Index 02h, R/W

Register 02h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWR8	SDWW8	SDWR7	SDWW7	SDWR6	SDWW6

- D1–D0: Shadow control for 0B8000 to 0BBFFF.
- D3–D2: Shadow control for 0BC000 to 0BFFFF.
- D5–D4: Shadow control for 0C0000 to 0CFFFF.
- D7–D6: Reserved for future use. Must be set to 0.

Shadow Control Register 3, Index 03h, R/W

Register 03h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWRB	SDWWB	SDWRA	SDWWA	SDWR9	SDWW9

- D1–D0: Shadow control for 0C4000 to 0C7FFF.
- D3–D2: Shadow control for 0C8000 to 0CBFFF.
- D5–D4: Shadow control for 0CC000 to 0CFFFF.
- D7–D6: Reserved for future use. Must be set to 0.

Shadow Control Register 4, Index 04h, R/W

Register 04h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWRE	SDWWE	SDWRD	SDWWD	SDWRC	SDWWC

- D1–D0: Shadow control for 0D0000 to 0D3FFF.
- D3–D2: Shadow control for 0D4000 to 0D7FFF.
- D5–D4: Shadow control for 0D8000 to 0DBFFF.
- D7–D6: Reserved for future use. Must be set to 0.

Shadow Control Register 5, Index 05h, R/W

Register 05h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWR11	SDWW11	SDWR10	SDWW10	SDWRF	SDWWF

- D1–D0: Shadow control for 0DC000 to 0DFFFF.
- D3–D2: Shadow control for 0E0000 to 0E3FFF.
- D5–D4: Shadow control for 0E4000 to 0E7FFF.
- D7–D6: Reserved for future use. Must be set to 0.

Shadow Control Register 6, Index 06h, R/W

Register 06h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWR14	SDWW14	SDWR13	SDWW13	SDWR12	SDWW12

- D1–D0: Shadow control for 0E8000 to 0EBFFF.
- D3–D2: Shadow control for 0EC000 to 0EFFFF.
- D5–D4: Shadow control for 0F0000 to 0F3FFF.
- D7–D6: Reserved for future use. Must be set to 0.

Shadow Control Register 7, Index 07h, R/W

Register 07h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	SDWR17	SDWW17	SDWR16	SDWW16	SDWR15	SDWW15

- D1–D0: Shadow control for 0F4000 to 0F7FFF.
- D3–D2: Shadow control for 0F8000 to 0FBFFF.
- D5–D4: Shadow control for 0FC000 to 0FFFFF.
- D7–D6: Reserved for future use. Must be set to 0.

Ram Wait State Select Register, Index 08h

Register 08h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	RDMSWT1	RDMSWT0	WRMSWT1	WRMSWT0	HITWTB1	HITWTB0

D1–D0: Wait states for page HIT

D1	D2	cycles
0	0	0
0	1	1
1	0	2
1	1	3

D3–D2: Wait states for MISS

D1	D2	write cycles
0	0	0
0	1	1
1	0	2
1	1	3

D5–D4: Wait states for MISS

D1	D2	read cycles
0	0	0
0	1	1
1	0	2
1	1	3

D7–D6: Reserved for future use. Must be set to 0.

Remap Register, Index 09h, R/W

Remap top RAM, local ROM and System ROM.

Register 09h

D2	D1	D0
RMPCD2	RMPCD1	RMPCD0

D2	D1	D0	TOP RAM	TOP ROM	LOCAL ROM ADDRESS	ROM	SYSTEM ROM ADDRESS
0	0	0	0	0K	0K		
0	0	1	512K	0K	0K		
0	1	0	128K	128K	(0E0000 - 0FFFFF)	128K	(0C0000 - 0DFFFF)
0	1	1	256K	128K	(0E0000 - 0FFFFF)	0K	
1	0	0	288K	64K	(0F0000 - 0FFFFF)	32K	(0C0000 - 0C3FFF)
1	0	1	320K	64K	(0F0000 - 0FFFFF)	0K	
1	1	0	352K	32K	(0F7FFF - 0FFFFF)	0K	
1	1	1	384K	0K		0K	

Local ROM Control Register 1, Index 0Ah, R/W

For each bit in this register, 0 is disable and 1 is enable.

Register 0Ah

D7	D6	D5	D4	D3	D2	D1	D0
0	0	D4TOD8	D0TOD4	CCTOD0	C8TOCC	C4TOC8	C0TOC4

- D0: ROM output enable for 0C0000h to 0C3FFFh.
- D1: ROM output enable for 0C4000h to 0C7FFFh.
- D2: ROM output enable for 0C8000h to 0CCFFFh.
- D3: ROM output enable for 0CC000h to 0CFFFFh.
- D4: ROM output enable for 0D0000h to 0D3FFFh.
- D5: ROM output enable for 0D4000h to 0D7FFFh.
- D7, D6: Reserved for future use. Must be set to 0.

Local ROM Control Register 2, Index 0Bh, R/W

For each bit in this register, 0 is disable and 1 is enable.

Register 0Bh

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ECTOFO0	E8TOEC	E4EOT8	E0TOE4	DCTOE0	D8TODC

Bit	Description
D0	ROM output enable for 0D8000h to 0DCFFFh.
D1	ROM output enable for 0DC000h to 0DFFFFh.
D2	ROM output enable for 0E000h0 to 0E3FFFh.
D3	ROM output enable for 0E4000h to 0E7FFFh.
D4	ROM output enable for 0E8000h to 0ECFFFh.
D5	ROM output enable for 0EC000h to 0EFFFFh.
D7, D6	Reserved for future use. Must be set to 0.

Local ROM Control Register 3, Index 0Ch, R/W

For bits 0 and 1 in this register, 0 is disable and 1 is enable.

Register 0Ch

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	PRMSW2	PRMSW1	PRMSW0	F8TOFF	F0TOF8

D0:
0 ROM output disable for 0F0000h to 0F7FFFh.
1 ROM output enable for 0F0000h to 0F7FFFh.

D1:
0 ROM output disable for 0F8000h to 0FFFFFh.
1 ROM output enable for 0F8000h to 0FFFFFh.

D4–D2:

D4	D3	D2	ROM Wait State Select
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
0	0	0	4
1	0	1	6
1	1	0	8
1	1	1	10

D7–D5: Reserved for future use. Must be set to 0.

RAS Timing Register, Index 0Dh, R/W

Register 0Dh

D7	D6	D5	D4	D3	D2	D1	D0
0	0	RTCBI	RTCBO	RSENDDLY	RSBGNDLY	RSPR1	RSPR0

D1–D0: RAS Precharge (2-5) CLK2 cycles)

D1	D0	RAS Precharge (2-5) CLK2 cycles)
0	0	2
0	1	3
1	0	4
1	1	5

D2:

0= RAS assertion as defined by bits RSPR1 - RSPR0.
1= RAS assertion as defined by bits RSPR1 - RSPR0 delayed by half CLK2 cycle.

D3:

0= RAS negation on T2 beginning.
1= RAS negation delayed by half CLK2 cycle.

D5–D4: RAS to Column Address Delay

D5	D4	RAS to Column Address Delay
0	0	Fast mode
0	1	1/2 CLK2
1	0	1 CLK2
1	1	1 1/2 CLK2

D7–D6: Reserved for future use. Must be set to 0.

CAS Timing Register 1, Index 0Eh, R/W

Register 0Eh

D7	D6	D5	D4	D3	D2	D1	D0
0	0	MSWRCSB2	MSWRCSB1	MSWRCSB0	MSRDCSB2	MSRDCSB1	MSRDCSB0

D2–D0: CAS start delay for MISS read cycles from T2 beginning (1 - 8 CLK2).

Bits 0 - 2 are coded in multiples of CLK2 cycles as shown below.

D2	D1	D0	Multiple
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D5–D3: CAS start delay for MISS write cycles from T2 beginning (1 - 8 CLK2).

Bits 3-5 are coded in multiples of CLK2 cycles as shown below.

D5	D4	D3	Multiple
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D7–D6: Reserved for future use. Must be set to 0.

CAS Timing Register 2, Index 0Fh, R/W

Register 0Fh

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CSENDDLY	HTWRCSB1	HTWRCSB0	HTRDCSB2	HTRDCSB1	HTRDCSB0

D2–D0: CAS start delay for HIT read cycles from T2 beginning (1 - 8 CLK2).

Bits 0 - 2 are coded in multiples of CLK2 cycles as shown below.

D2	D1	D0	Multiple
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D4–D3: CAS start delay for HIT write cycles (0-3 CLK2).

D4	D3	Start Delay
0	0	0
0	1	1
1	0	2
1	1	3

D5: CSENDDLY CAS negation delayed by half CLK2.

D7–D6: Reserved for future use. Must be set to 0.

Disable to OK Register, Index 10h, R/W

Register 10h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ENRSLMT	DI512	DI384	DI256	DI128	DI0

D0=0 Enable local DRAM from 0K to 128K .
D0=1 Disable local DRAM from 0K to 128K.

D1=0 Enable local DRAM from 128K to 256K.
D1=1 Disable local DRAM from 128K to 256K.

D2=0 Enable local DRAM from 256K to 384K.
D2=1 Disable local DRAM from 256K to 384K.

D3=0 Enable local DRAM from 384K to 512K.
D3=1 Disable local DRAM from 384K to 512K.

D4=0 Enable local DRAM from 512K to 640K.
D4=1 Disable local DRAM from 512K to 640K.

D5=0 Disable RAS timeout.
D5=1 Enable RAS timeout.

D7–D6: Reserved for future use. Must be set to 0.

Memory Type and Size Select Register, Index 11h, R/W

Register 11h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	>	Memory Type/Bank Selects		<

These bits define the type of memory devices to be used for each of the four banks.

D3	D2	D1	D0	BANK0	BANK1	BANK2	BANK3
0	0	0	1	256K	256K		
0	0	1	0	256K	256K	256K	
0	0	1	1	256K	256K	256K	256K
0	1	0	0	256K	1M		
0	1	0	1	Reserved			
0	1	1	0	256K	256K	1M	
0	1	1	1	256K	256K	1M	1M
1	0	0	0	4M			
1	0	0	1	4M	4M		
1	0	1	0	4M	4M	4M	
1	0	1	1	4M	4M	4M	4M
1	1	0	0	1M			
1	1	0	1	1M	1M		
1	1	1	0	1M	1M	1M	
1	1	1	1	1M	1M	1M	1M

Reserved for future use. Must be set to 0.

Configuration Register 1, Index 12h, R/W

Register 12h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	STGRS1	STGRS0	DISNA	SLOWWRT	NONPAGE	INTLV

D0=0 Non interleave mode.
D0=1 Interleave mode.

D1=0 Page mode.
D1=1 Non page mode.

D2=0 Write HIT wait state(s) 1 less than read HIT cycles.

D2=1 Write HIT wait state(s) same as for read HIT cycles.

D3=0 Enable pipeline mode.
D3=1 Disable pipeline mode.

Staggered refresh in CLK2 cycles.

D5	D4	
0	0	Disable
0	1	Reserved
1	0	1 CLK2 stagger
1	1	2 CLK2 staggers

D7, D6: Reserved for future use. Must be set to 0.

Configuration Register 2, Index 13h, R/W

Register 13h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	INTLVOK	FSTCLK	HTCSHFCK	MSCSHFCK	ENBFRST	1

- D0: Always read as 1.
- D1: D1=0 Disable fast reset. D1=1 Enable fast reset.
- D2: D2=0 MISS cycle CAS start as in CASTIM1. D2=1 MISS cycle CAS start delayed by 1/2 CLK2.
- D3: D3=0 HIT cycles CAS start as in CASTIM2. D3=1 HIT cycles CAS start delayed by 1/2 CLK2.
- D4: D4=0 Select CLK2 for RAS timeout. D4=1 Select CPUCLK for RAS timeout.
- D5: This is read only bit, set for valid interleave mode.
- D7–D6: Reserved for future use. Must be set to 0.

Configuration Register 3, Index 14h, R/W

Register 14h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	MULTPGIL	ALLCAS	SHRTCAS	XFRIOADS

D0=0 No action.
D0=1 Transfer relocation register to compare register.

D1=0 CAS negated at T2 beginning.
D1=1 CAS negated at end of ready.

D2=0 Only CAS00 active in non-interleave mode.
D2=1 All CAS active in non-interleave mode.

D3=0 Linear/page mode/ word interleave.
D3=1 Multipage interleave mode.

D7–D4: Reserved for future use. Must be set to 0.

Relocation Registers Low/High, Index 15h-16h R/W

These two registers are used to remap the SL9252 configuration registers. To remap the register, load registers 15 and 16 with the address (should be on a byte 2 boundary) and a write to configuration register 3 (014h) with bit 0=1. For example, to remap the configuration registers to address 162h, load register 16h with 01h, register 15h with 62h and set bit 0 in register 14h. All future accesses to configuration registers will then refer to the new address.

Register 15h

D7	D6	D5	D4	D3	D2	D1	D0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	0

Register 16h

D7	D6	D5	D4	D3	D2	D1	D0
AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

Example to indicate relocation (remap configuration registers to address 162h):

```
MOV     AX, 0122h
MOV     DX, AX
IN      AL, DX (dummy read ensures that pointer points to
                the address register)
MOV     AL, 15h
OUT     DX, AL
MOV     AL, 62h
OUT     DX, AL
MOV     AL, 16h
OUT     DX, AL
MOV     AL, 01h
OUT     DX, AL
MOV     AL, 14h
OUT     DX, AL
IN      AH, DX
OR      AH, 01h
OUT     DX, AH
IN      AH, DX
AND     AH, FEh
OUT     DX, AH
```

System Control Register, Index 18h, R/W

Register 18h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	ENATTMR	ASYNAT	LMEM-MD

- D0=0 Local DRAM and EPROM on D bus.
- D0=1 Local DRAM and EPROM on MD bus.
- D1=0 Synchronous AT bus operation.
- D1=1 Asynchronous AT bus operation.
- D2=0 Disable AT bus timeout.
- D1=1 Enable AT bus timeout.
- D7–D3: Reserved for future use. Must be set to 0.

System Bus 16-Bit Device Wait State Select Register, Index 19h, R/W

Register 19h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	IO16RY2	IO16RY1	IO16RY0	MEM16RY2	MEM16RY1	MEM16RY0

D2–D0: Wait state select for 16 bit memory devices.

Bits 0 - 2 are coded as shown below.

D2	D1	D0	#
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D5–D3: Wait state select for 16 bit I/O devices.

Bits 3-5 are coded as shown below.

D5	D4	D3	#
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D7–D6: Reserved for future use. Must be set to 0.

System Bus 8-Bit Device Wait State Select Register, Index 1Ah

Register 1Ah

D7	D6	D5	D4	D3	D2	D1	D0
0	0	IO8RY2	IO8RY1	IO8RY0	MEM8RY2	MEM8RY1	MEM8RY0

D2–D0: Wait state select for 8 bit memory devices.

Bits 0 - 2 are coded as shown below.

D2	D1	D0	#
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D5–D3: Wait state select for 8 bit I/O devices.

Bits 3-5 are coded as shown below.

D2	D1	D0	#
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D7–D6: Reserved for future use. Must be set to 0.

System Bus Command Delay Register, Index 1Bh

Register 1Bh

D7	D6	D5	D4	D3	D2	D1	D0
0	0	RCMDLY5	RCMDLY4	RCMDLY3	WRCMDLY2	WRCMDLY1	WRCMDLY0

D2–D0: Write command delay in CLK2 cycles.

Bits 0 - 2 are coded as shown below.

D2	D1	D0	#
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D5–D3: Read command delay in CLK2 cycles.

Bits 3-5 are coded as shown below.

D5	D4	D3	#
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D7–D6: Reserved for future use. Must be set to 0.

RAS Map Register, Index 1Fh

Register 1Fh

D7	D6	D5	D4	D3	D2	D1	D0
BNK3B1	BNK3B0	BNK2B1	BNK2B0	BNK1B1	BNK1B0	BNK0B1	BNK0B0

Selects bank 0 logical to physical mapping.

D1	D0	
0	0	LBNK0
0	1	LBNK1
1	0	LBNK2
1	1	LBNK3

Selects bank 1 logical to physical mapping.

D3	D2	
0	0	LBNK1
0	1	LBNK2
1	0	LBNK3
1	1	LBNK0

Selects bank 2 logical to physical mapping.

D5	D4	
0	0	LBNK2
0	1	LBNK3
1	0	LBNK0
1	1	LBNK1

Selects bank 3 logical to physical mapping.

D7	D6	
0	0	LBNK3
0	1	LBNK2
1	0	LBNK1
1	1	LBNK0

CONFIGURATION REGISTER, cont'd

Table 6 shows the default configuration values after reset.

ADDRESS	NAME	D7	D6	D5	D4	D3	D2	D1	D0
0	SDWREG0	0	0	0	0	0	0	0	0
1	SDWREG1	0	0	0	0	0	0	0	0
2	SDWREG2	0	0	0	0	0	0	0	0
3	SDWREG3	0	0	0	0	0	0	0	0
4	SDWREG4	0	0	0	0	0	0	0	0
5	SDWREG5	0	0	0	0	0	0	0	0
6	SDWREG6	0	0	0	0	0	0	0	0
7	SDWREG7	0	0	0	0	0	0	0	0
8	RAMWAIT	0	0	1	1	1	1	1	1
9	REMAP	0	0	0	0	0	0	0	0
A	ROMCTL0	0	0	0	0	0	0	0	0
B	ROMCTL1	0	0	0	0	0	0	0	0
C	ROMCTL2	0	0	0	1	1	1	1	1
D	RASTIM	0	0	0	1	0	0	1	1
E	CASTIM1	0	0	1	1	0	1	1	1
F	CASTIM2	0	0	0	0	1	0	0	1
10	DISMEM	0	0	0	0	0	0	0	0
11	MEMTYPE	0	0	0	0	0	0	0	0
12	CONFIG1	0	0	0	0	0	0	0	0
13	CONFIG2	0	0	R	0	0	0	0	0
14	CONFIG3	0	0	0	0	0	0	0	W
15	IOMAPLOW	0	0	1	0	0	0	1	0
16	IOMAPHI	0	0	0	0	0	0	0	1
18	SYSCTL	0	0	0	0	0	0	0	0
19	WAIT16	0	0	0	0	1	0	0	1
1A	WAIT8	0	0	0	1	1	0	1	1
1B	CMDDLY	0	0	0	0	0	0	0	1
1F	RASMAP	0	0	0	0	0	0	0	0

Table 6 Configuration Values

W : Write only bit(s). See Configuration register description.
R : Read only bit(s) See CONFIG2 register description.

PORT92

Port 92

D1	**D0**
A20GATE	FSTRST

D0 (FSTRST):

- 0 to 1 — Generate fast reset.
- 1 to 0 — No action.

D1 (A20GATE):

- D1=1 — Pass CPU A20.
- D1=0 — Force 0 on internal A20 if A20GATE from keyboard controller = 0.

VIII. AC TIMING DIAGRAMS SL9252

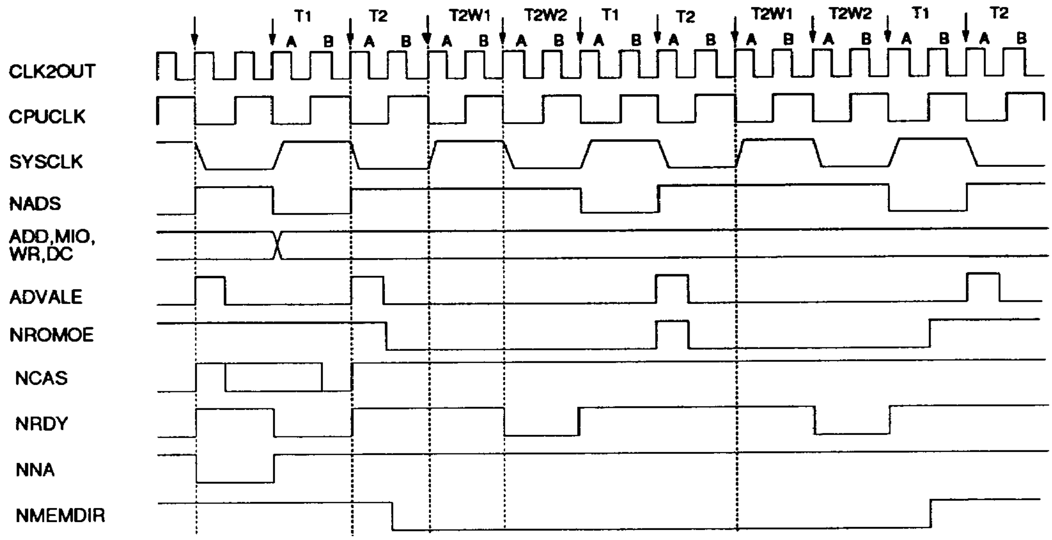


Fig. 6 Local Memory Cycles

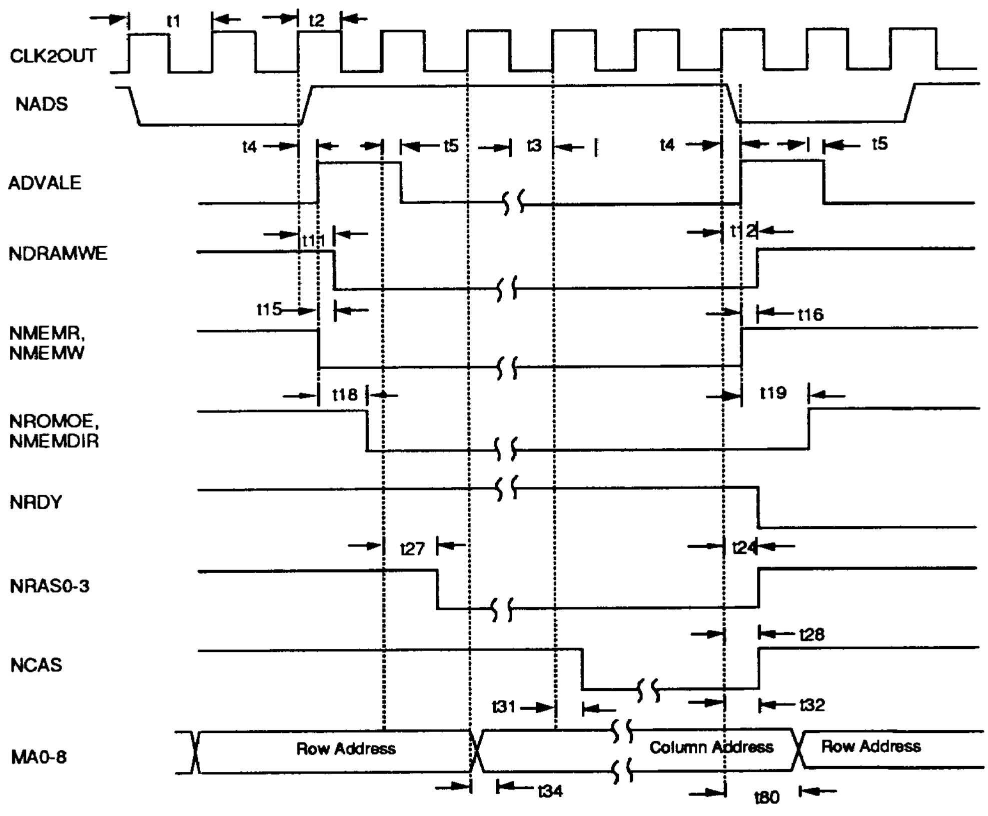


Fig. 7 Local Memory Cycle Timing Specification

AC TIMING DIAGRAMS SL9352

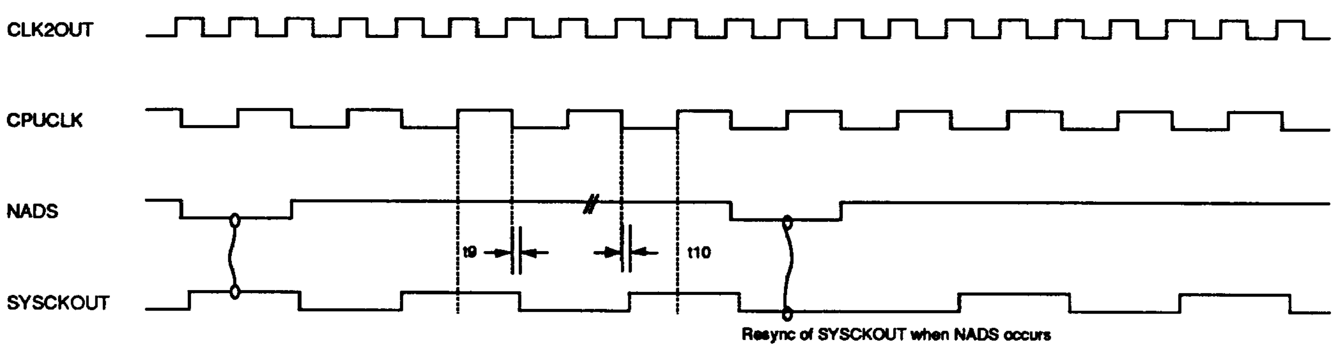
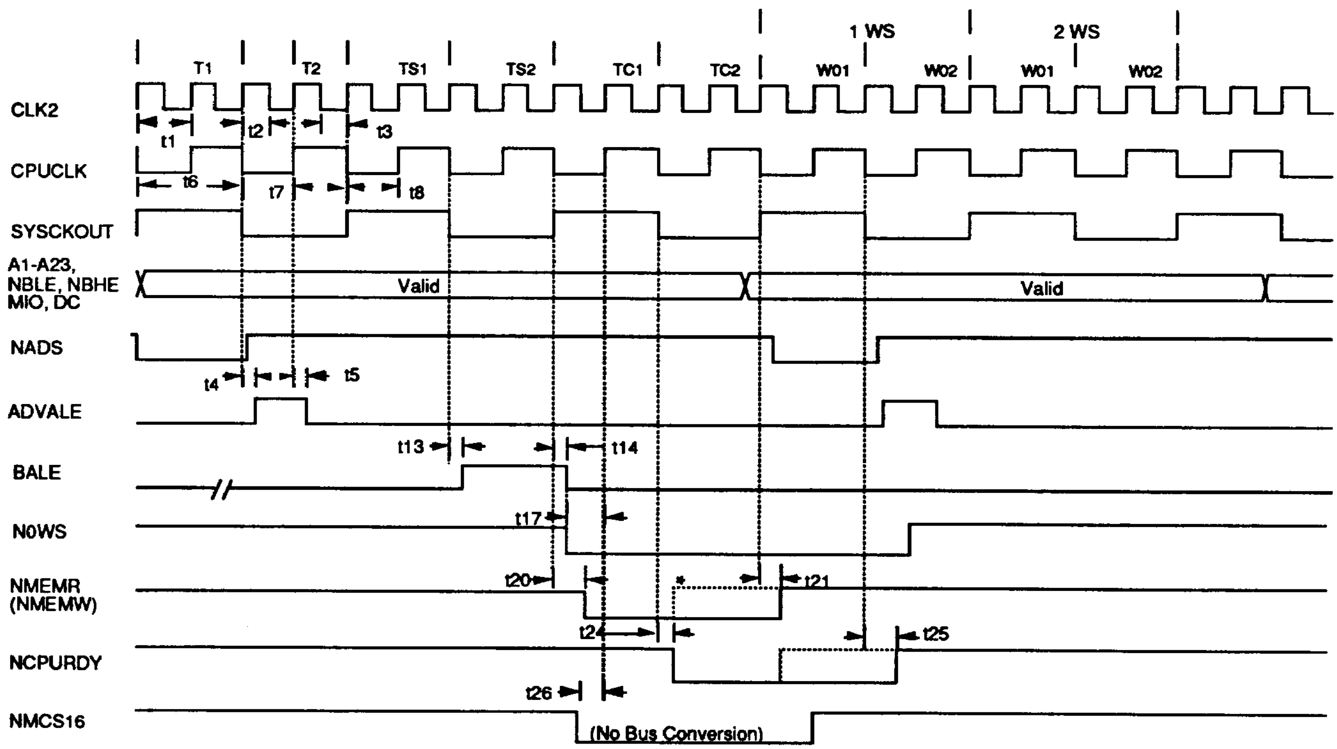


Fig. 8 SYSCKOUT and DMACLK Relationships with CPUCLK SYSCKOUT Synchronization with Assertion of NADS



NOTES:
* NMEMW
1. N0WS active setup to CPUCLK rising edge is to ensure AT (ISA) 0 wait state cycle.
2. NMCS16 setup ensures that no Bus conversion cycle takes place.
3. NMEMR delay from CPUCLK falling edge is same as NMEMW (t10, t10a).
4. NMCS16 or NIOCS16 is not latched inside SL9352. It is sampled every rising edge of CPUCLK and must stay asserted for the duration of the ISA Bus cycle.
5. NMEMW is negated with NCPURDY assertion.

FIG. 9 16-Bit External Memory Cycle, 0 Wait State Non-Pipelined

AC TIMING DIAGRAMS SL9352

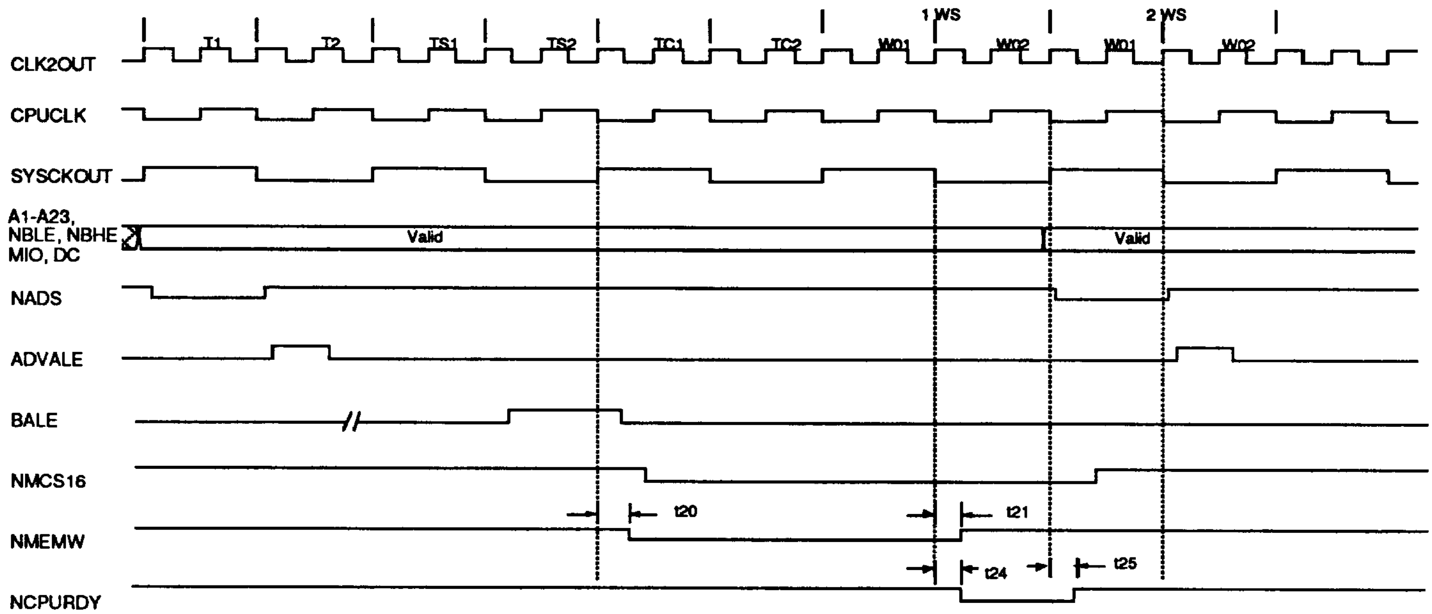


Fig. 10 16-Bit External Memory Cycle, 1 Wait State Non-Pipelined

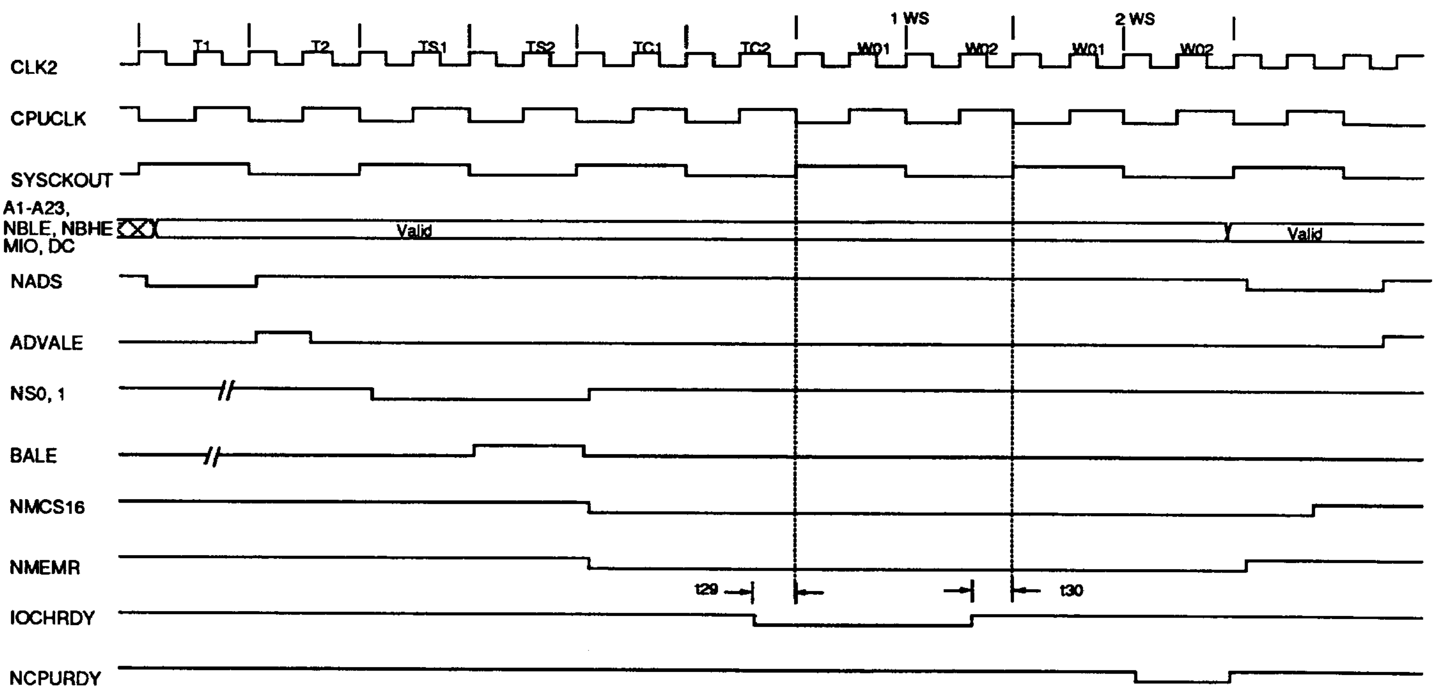


Fig. 11 16-Bit External Memory Cycle, 2 Wait State Using IOCHRDY to Extend the Cycle Non-Pipelined

AC TIMING DIAGRAMS SL9252

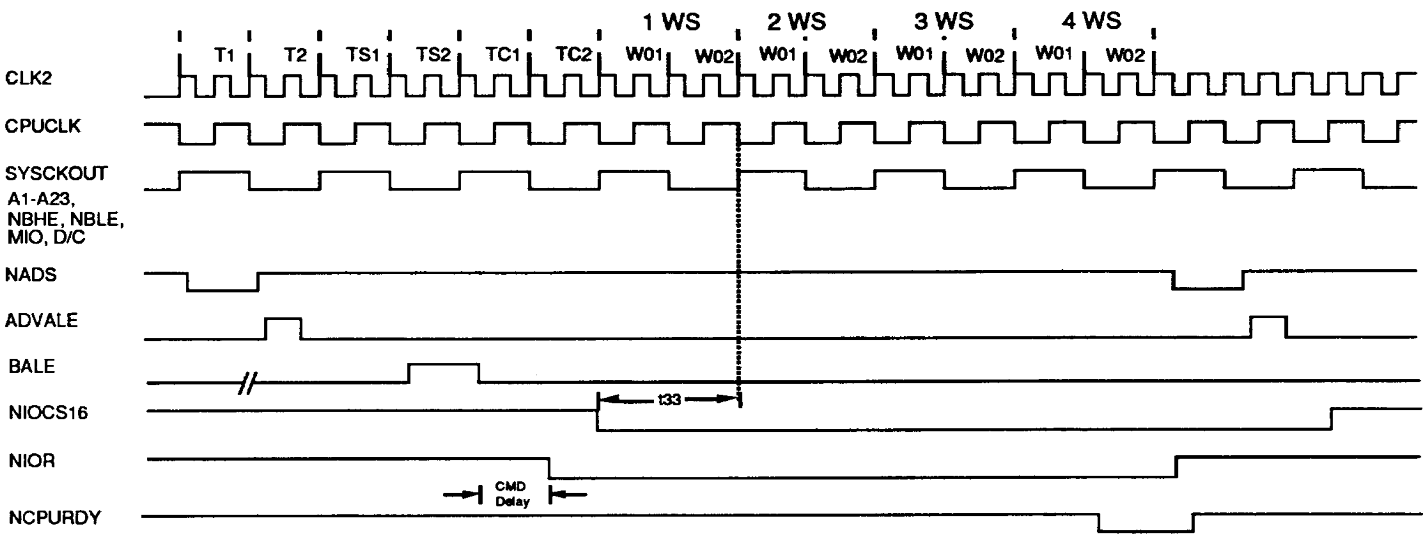


Fig. 12 16-Bit External I/O Cycle with Wait States Non-Pipelined

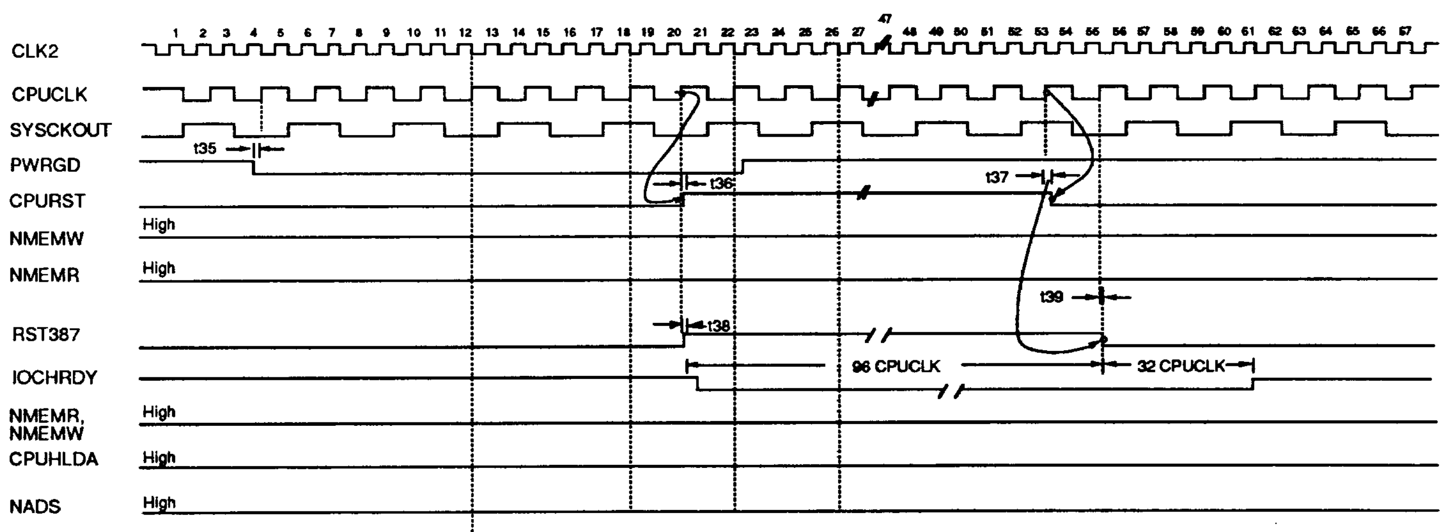


Fig. 13 RESET, CPURST, DMACKOUT, SYSCKOUT Timings and IRQ13 Relationship

AC TIMING DIAGRAMS SL9252

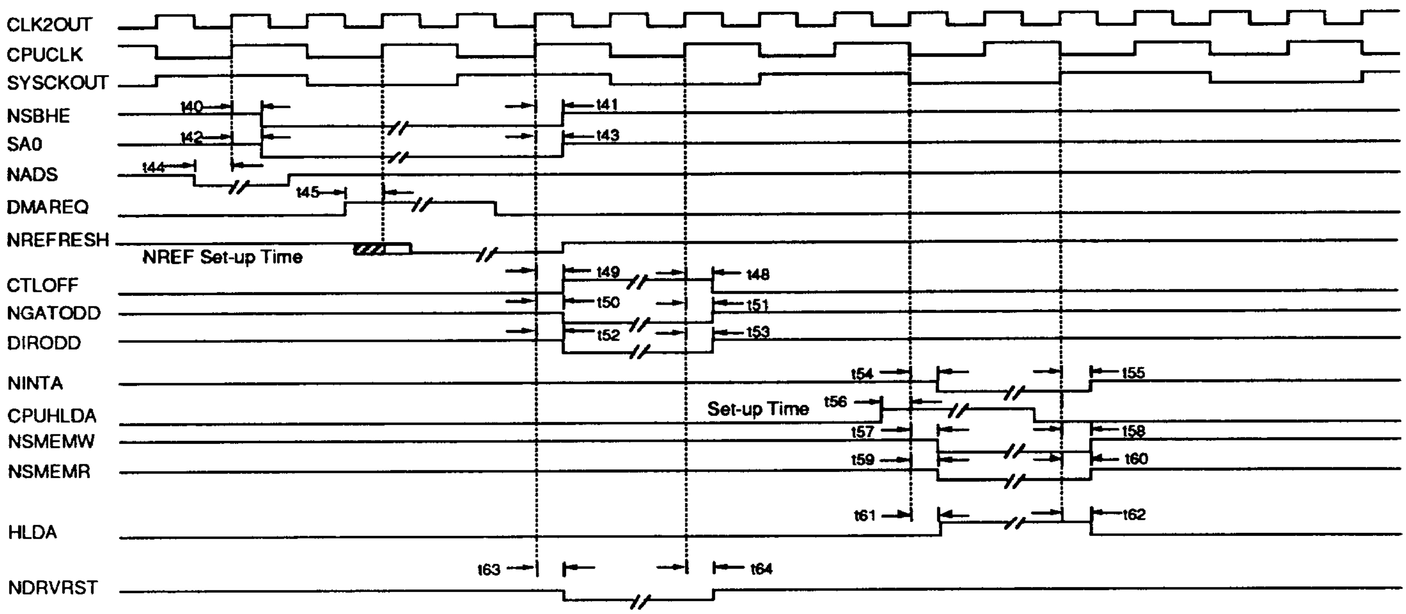


Fig. 14 Set-Up Times and Output Signal Delays from CLK2OUT or CPUCLK

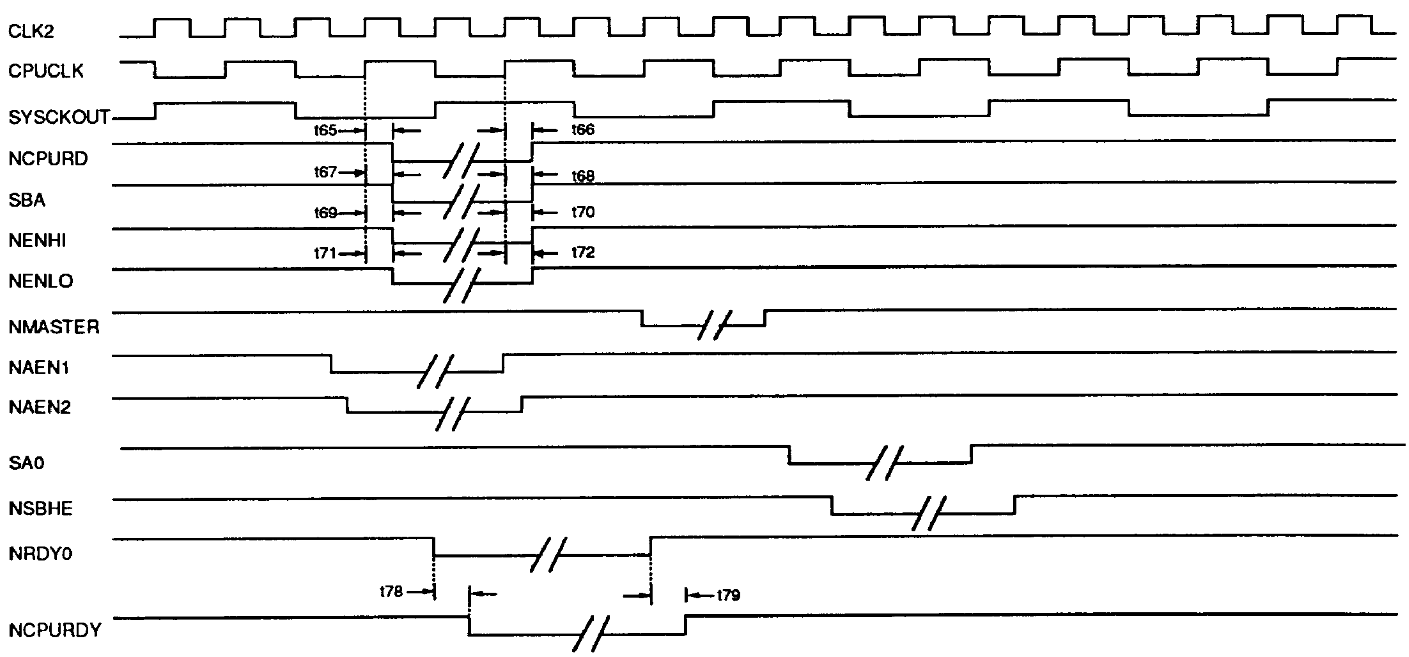


Fig. 15 Output Signal Delays from CPUCLK and NCPURDY Delays

AC TIMING DIAGRAMS SL9352

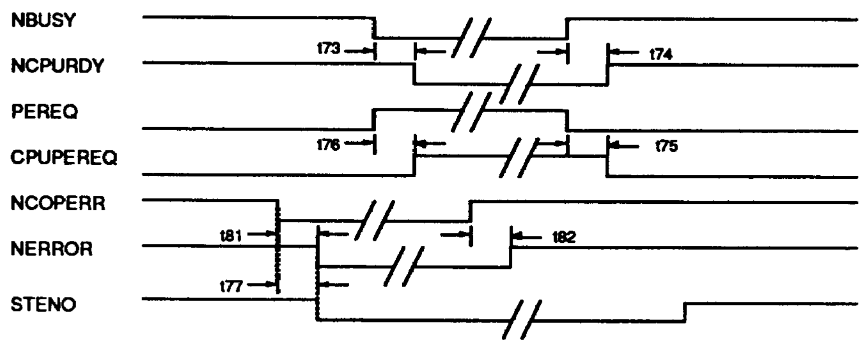
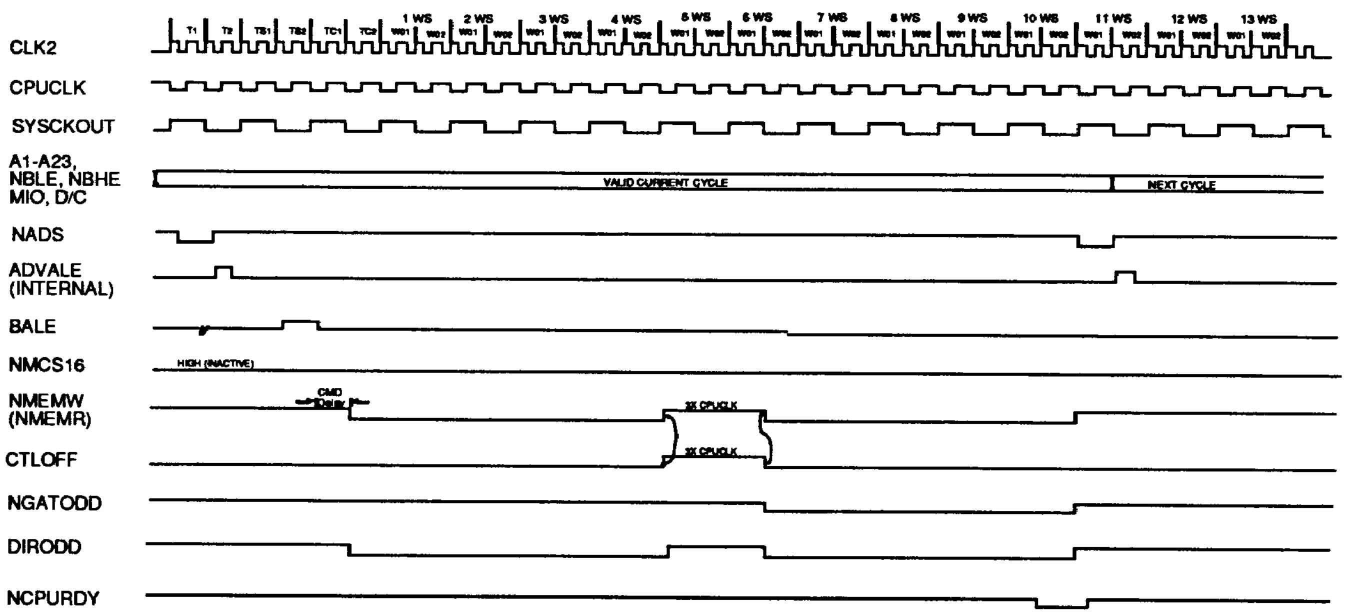


Fig. 16 NPX Cycle Input to Output Signal Delays



NOTES:
1. NPRA0 changes SA0 from logical 0 to logical 1.
2. CTLOFF and NWAIT keep NCPURDY deasserted.
3. CONALE resets the wait state state machine.
4. NGAT1 and DIR1 transfer data from SD[15:8] to SD[7:0]. NENLO=1.

Fig. 17 Data Conversion Cycle

IX. ABSOLUTE MAXIMUM RATINGS SL9252 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage *note 2	VDD	Vss-0.5	6.0	V
Input Voltage *note 2	VI	Vss-0.5	VDD+0.5	V
Output Voltage *note 2	VO	Vss-0.5	VDD+0.5	V
Output Current (IOL = 3.2mA) *note 2	IOS	-40	+40	mA
Output Current (IOL = 8mA) *note 3	IOS	-40	+80	mA
Output Current (IOL = 12mA) *note 3	IOS	-60	+120	mA
Output Current (IOL = 24mA) *note 3	IOS	-90	+180	mA
Storage Temp.	TSTG	-40	+125	°C
Storage Temp.	TBIAS	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. Vss = 0V
3. Not more than one output may be shortened at a time for a maximum duration of one second.

X. RECOMMENDED OPERATING CONDITIONS SL9252

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	VDD	4.75	5.25	V
Operating Temperature	TA	0	70	°C
Input High Voltage for Normal Input	VIH	2.2		V
Input Low Voltage for Normal Input	VIL		0.8	V
Input High Voltage for CMOS Input	VIH	VDDx0.7		V
Input Low Voltage for CMOS Input	VIL		VDDx0.3	V

NOTE: Conditions for outgoing functional test are VIH = 3.0V VIL = 0V

XI. DC CHARACTERISTICS SL9252

(Recommended Operating Conditions Unless Otherwise Noted)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state *note 1
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24 mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	VDD x0.7		V	
Input Low Voltage for CMOS Input	VIL		VDD x0.3	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = VSS

* NOTES:

1. VIH = VDD, VIL = VSS

XII. AC CHARACTERISTICS SL9252

(Recommended Operating Conditions Unless Otherwise Noted)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	CLK2OUT Period	25	-	ns
t2	CLK2OUT High Duration	7	-	ns
t3	CLK2OUT Low Duration	7	-	ns
t4	CLK2OUT High to ADVALE (High)	1.1	5.1	ns
t5	CLK2OUT High to ADVALE (Low)	1.0	4.3	ns
t6	CPUCLK Period	50	-	ns
t7	CPUCLK High Duration	14	-	ns
t8	CPUCLK Low Duration	14	-	ns
t9	CPUCLK Falling to SYSCKOUT (High to Low)	3.0	13.0	ns
t10	CPUCLK Falling to SYSCKOUT (Low to High)	3.7	13.5	ns
t11	CLK2OUT High to NDRAMWE (High to Low)	1.7	8.0	ns
t12	CLK2OUT High to NDRAMWE (Low to High)	1.8	8.8	ns
t13	CPUCLK Falling Edge to BALE (Low to High)	5.3	23.8	ns
t14	CPUCLK Falling Edge to BALE (High to Low)	6.1	33.7	ns
t15	NMEMW Low to NDRAMWE (High to Low)	2.0	8.5	ns
t16	NMEMW High to NDRAMWE (Low to High)	1.7	8.7	ns
t18	ADVALE High to NROMOE (High to Low)	TBD	TBD	ns
t19	ADVALE High to NROMOE (Low to High)	TBD	TBD	ns
t20	CPUCLK Falling Edge to NMEMW (High to Low)	7.1	56.1	ns
t21	CPUCLK Falling Edge to NMEMW (Low to High)	4.7	38.7	ns
t24	SYSCKOUT Falling Edge to NCPURDY (High to Low)	0.6	2.3	ns
t25	CLK2OUT Rising Edge to NCPURDY (Low to High)	3.9	15.6	ns
t27	CLK2OUT High to NRAS0-3 (High to Low)	7.0	34.5	ns
t28	CLK2OUT High to NRAS0-3 (Low to High)	8.0	35.5	ns
t31	CLK2OUT High to NCAS00-31 (High to Low)	4.3	18.0	ns
t32	CLK2OUT High to NCAS00-31 (Low to High)	4.1	17.3	ns
t34	CLK2OUT to Column Address	3.8	16.2	ns
t36	CPUCLK Rising Edge to CPURESET (High)	0.8	3.9	ns
t37	CPUCLK Rising Edge to CPURESET (Low)	1.1	4.5	ns
t38	CPUCLK Rising Edge to COPRESET (High)	1.0	5.5	ns
t39	CPUCLK Rising Edge to COPRESET (Low)	2.1	8.8	ns
t40	CLK2OUT Rising Edge to NSBHE (High to Low)	4.2	17.6	ns
t41	CLK2OUT Rising Edge to NSBHE (Low to High)	4.3	18.1	ns
t42	CLK2OUT Rising Edge to SA0 (High to Low)	2.8	12.0	ns
t43	CLK2OUT Rising Edge to SA0 (Low to High)	6.2	29.5	ns
t48	CPUCLK Falling Edge to CTLOFF (High to Low)	4.1	17.8	ns
t49	CPUCLK Falling Edge to CTLOFF (Low to High)	4.0	18.5	ns
t50	CPUCLK Falling Edge to NGATODD (High to Low)	9.5	-	ns
t51	CPUCLK Falling Edge to NGATODD (Low to High)	4.0	-	ns
t52	CPUCLK Falling Edge to DIRODD (High to Low)	17.0	-	ns
t53	CPUCLK Falling Edge to DIRODD (Low to High)	9.5	-	ns

AC CHARACTERISTICS SL9252 (Cont'd)

(Recommended Operating Conditions Unless Otherwise Noted)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t54	CPUCLK Falling Edge to NINTA (High to Low)	7.5	36.9	ns
t55	CPUCLK Falling Edge to NINTA (Low to High)	7.5	36.9	ns
t57	CPUCLK Falling Edge to NSMEMW (High to Low)	12.9	65.9	ns
t58	CPUCLK Falling Edge to NSMEMW (Low to High)	10.1	45.3	ns
t59	CPUCLK Falling Edge to NSMEMR (High to Low)	14.4	65.6	ns
t60	CPUCLK Falling Edge to NSMEMR (Low to High)	9.9	41.7	ns
t61	CPUCLK Falling Edge to HLDA (High to Low)	4.8	21.1	ns
t62	CPUCLK Falling Edge to HDLA (Low to High)	3.0	14.0	
t63	CPUCLK Rising Edge to NDRVRST (High to Low)	0.7	3.8	ns
t64	CPUCLK Rising Edge to NDRVRST (Low to High)	0.7	3.8	ns
t65	CPUCLK Rising Edge to NCPURD (High to Low)	2.6	12.0	ns
t66	CPUCLK Rising Edge to NCPURD (Low to High)	3.0	13.0	ns
t67	CPUCLK Falling Edge to SBA (High to Low)	8.3	36.0	ns
t68	CPUCLK Falling Edge to SBA (Low to High)	10.3	45.8	ns
t69	CPUCLK Falling Edge to NENHI (High to Low)	6.8	22.3	ns
t70	CPUCLK Falling Edge to NENHI (Low to High)	5.3	22.8	ns
t71	CPUCLK Falling Edge to NENLO (High to Low)	8.5	40.2	ns
t72	CPUCLK Falling Edge to NENLO (Low to High)	6.9	30.6	ns
t73	NCOPBSY to NCPUBUSY Delay (High to Low)	1.4	6.1	ns
t74	NCOPBSY to NCPUBUSY Delay (Low to High)	1.3	5.6	ns
t75	COPEREQ to CPUPEREQ Delay (High to Low)	1.8	7.9	ns
t76	COPEREQ to CPUPEREQ Delay (Low to High)	1.5	6.5	ns
t77	NCOPERR Falling to STENO (High to Low)	2.8	12.9	ns
t78	NCOPRDY Asserted Low NCPURDY (High to Low)	1.3	6.1	ns
t79	NCOPRDY Asserted High NCPURDY (Low to High)	1.2	6.0	ns
t80	CLK2OUT to Row Address	3.8	16.2	ns
t81	NCOPERR to NCPUERR Delay (High to Low)	2.1	9.0	ns
t82	NCOPERR to NCPUERR Delay (Low to High)	1.7	7.2	ns
t17	N0WS Set-up time to CPUCLK Rising Edge	TBD	TBD	ns
t26	NMCS16 Set-up Time to CPUCLK Rising Edge	TBD	TBD	ns
t29	IOCHRDY Set-up Time to SYSCKOUT Rising Edge	TBD	TBD	ns
t30	IOCHRDY Hold Time to SYSCKOUT Rising Edge	TBD	TBD	ns
t33	NIOCS16 Set-up Time to CPUCLK Rising Edge	TBD	TBD	ns
t35	PWRGD Set-up Time to CPUCLK Rising Edge	TBD	TBD	ns
t44	NADS Set-up Time to CLK2OUT Rising Edge	TBD	TBD	ns
t45	DMAREQ Set-up Time to CLK2OUT Rising Edge	TBD	TBD	ns
t56	CPUHLDA Set-up Time to CPUCLK Falling Edge	TBD	TBD	ns

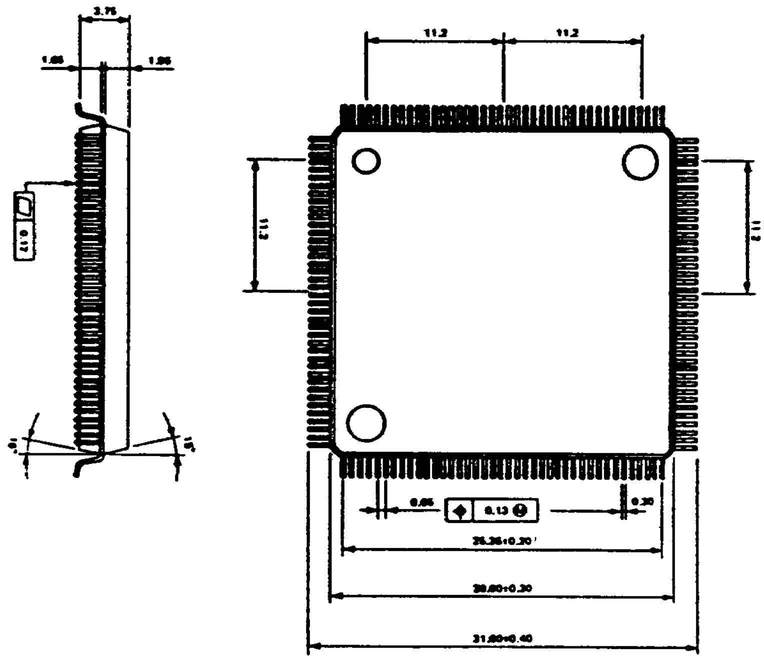
CAPACITANCE SL9252

(TA = 25 ° C, VDD = V1 = 0V, fo = 1MHz)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS
Input Pin Capacitance	C_{IN}	---	16	Pf
Output Pin Capacitance (IOL = 3.2 mA, 8 mA, or 12 mA)	C_{OUT}	---	16	Pf
Output Pin Capacitance (IOL = 24 mA)	C_{OUT}	---	18	Pf
I/O Pin Capacitance (IOL = 3.2 mA, 8 mA, or 12 mA)	$C_{I/O}$	---	16	Pf
I/O Pin Capacitance (IOL = 24 mA)	$C_{I/O}$	---	23	Pf

PACKAGE INFORMATION

160 Pin Flat Pack



ORDERING INFORMATION

Device Type:
SL9352

Package Type:
FP-Plastic Flat Pack

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL9252 XX X

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