The FlexSet™ PC/AT
80386SX Page Interleave Memory Controller
SL9251

PRELIMINARY

FEATURES

- Supports 80386SX based AT Designs.
- Up to 20 MHz Performance.
- Enhanced Fast Page Mode/Page Interleave.
- Supports 8 M bytes of On-Board Memory.
- Shadow RAM Feature
  - 16K granularity
  - 8 remap options
  - System, video, LAN BIOS
- Programmable Memory Options
  - ROM chip select in 16K granularity
  - Wait states for 16 Bit ROM
  - Hit wait states (0-3)
  - Miss wait states (1-4)
  - RAS and CAS precharge
- Programmable Memory Partitioning
  - Disable (on-board) memory to 0K in 128K resolution
  - 512 X 512 split
  - Memory backfill
- Can use 256K x 1, 1 M x 1 and 256K x 4 DRAMs or a mix.
- Staggered RAS Refresh.
- Supports Pipeline and Non-Pipeline Modes.
- Fast Gate A20 and Fast Reset.
- Backward Compatible to SL9250.
- Advanced, Low Power CMOS Technology for Laptops.
- 100 pin Flatpack.

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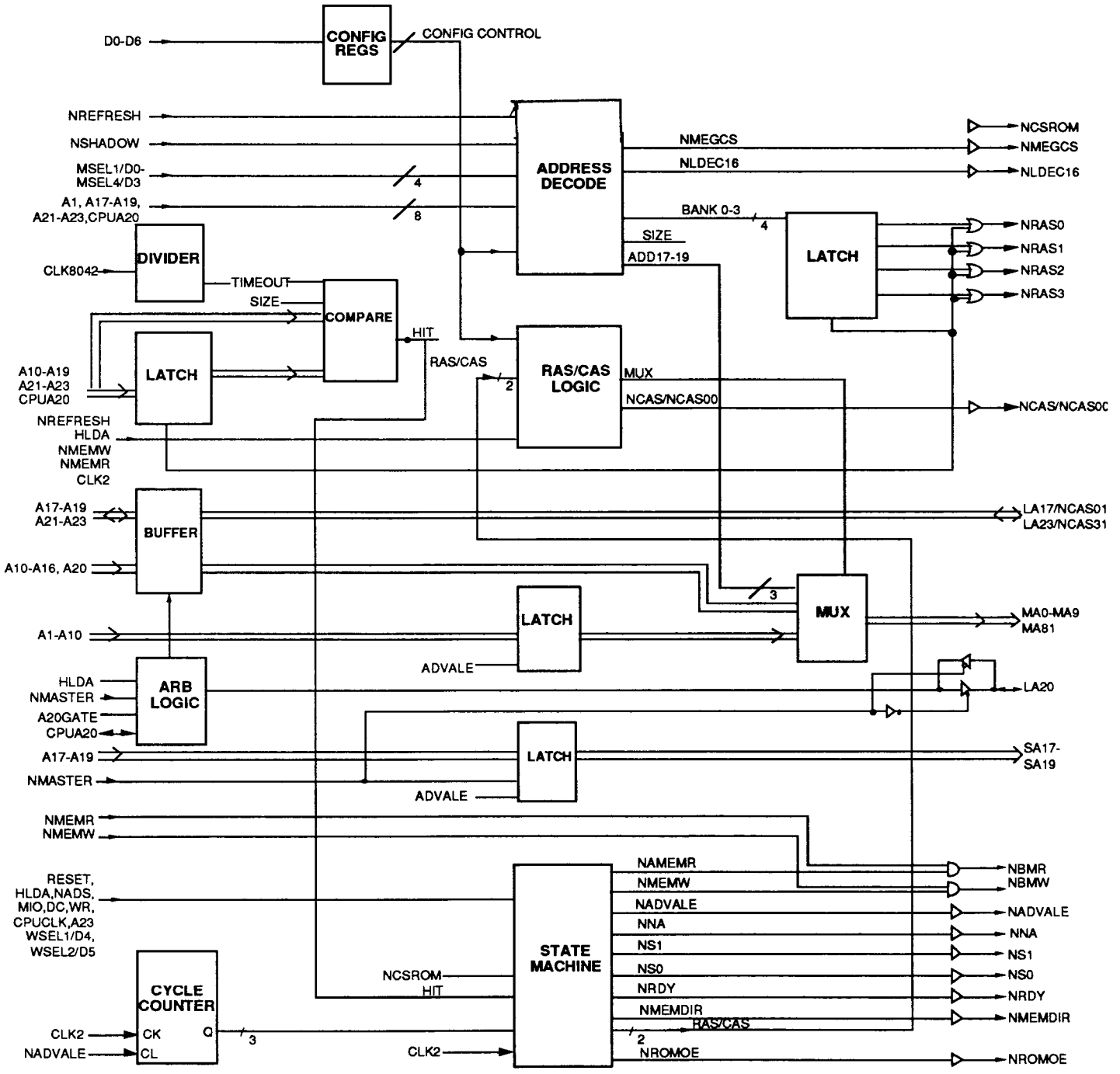
Sunnyvale, CA 94086

BLOCK DIAGRAM SL9251/SL9250 Page Mode



MODE SELECT

The SL9251 operates in three basic modes. The first mode, SL9250 Page Mode, is backward compatible with existing designs utilizing the SL9250 Memory Controller. Refer to Figures 1 and 4. The second mode, SL9251 Page Mode, allows full program flexibility (shadow, wait state select, remapping, RAS/CAS Timing, RAM disabling, etc.) and features a low cost, non interleave memory architecture identical to the SL9250. Refer to Figures 2 and 4. The third mode, SL9251 Page Interleave, allows full program flexibility, 2- or 4- way interleaving, and direct bank CAS output lines, for fast 0 wait state performance. Refer to Figures 3 and 4.

SL9250 Page Mode

In SL9250 Page Mode, the SL9251 is designed to be backward compatible with the SL9250. Hence, an SL9251 may be plugged into an SL9250 "socket". All of the SL9251 pins behave as the SL9250 pins would, with the exceptions listed in Table 1.

The basic system architecture is shown in Figure 1- the 386SX RAM Block Diagram/SL9250 Page Mode. The internal structure is shown in the System Block Diagram SL9251/SL9250 Page Mode. The SL9251 will power up in the SL9250 page mode, and hence will operate in SL9250 architecture, with SL9250 features, unless the mode is changed via a write to the configuration register #2. Memory configuration is set by the four lines MSEL1/D0-MSEL4/D3, as shown in Table 2. Memory miss wait states may be set by the two lines WSEL1/D4 and WSEL2/D5, also shown in Table 4. Memory hits are always 0 wait states.

The option registers should not be addressed in the SL9250 mode, with the exception of configuration register #2 (index13H), which may be written to select SL9250 or SL9251 mode.

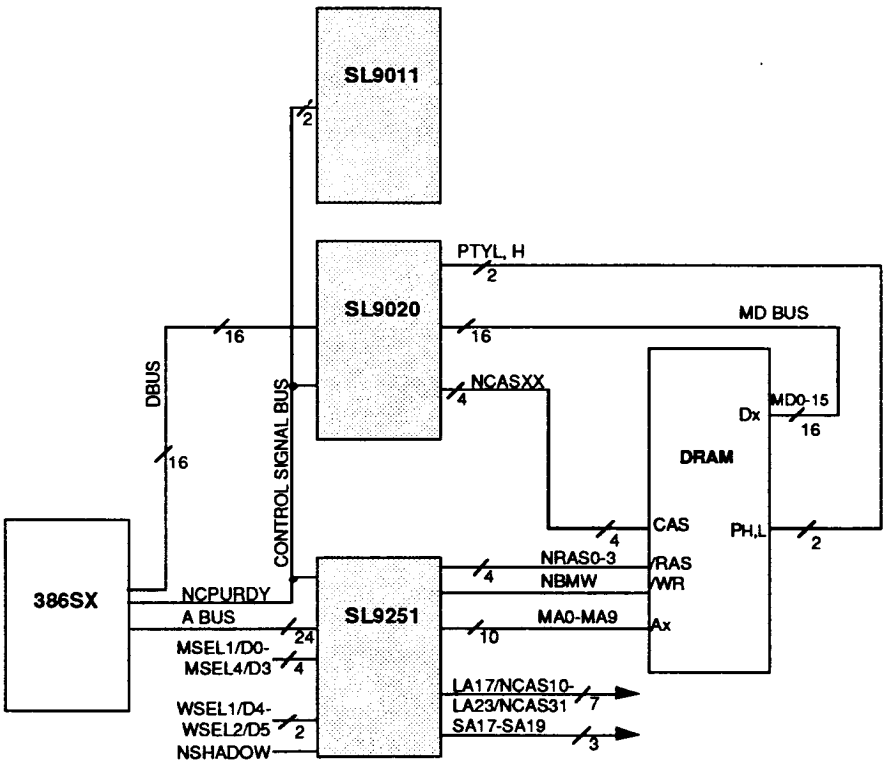


Fig. 1 386SX RAM Block Diagram/SL9250 Page Mode

SL9251 Page Mode

In SL9251 Page Mode, the SL9251 allows full utilization of the 20 internal option register. SL9251 Page Mode is invoked by writing configuration Register #1 D1=0 and D0=0 (address 12h), and writing configuration Register #2 D0=1 (address13h). The RAM block diagram is shown in Figure 2. Note that the structure is the same as in the SL9250 page mode (Fig. 1) with the exception that the option selects (MSEL1/D0-MSEL4/D3, WSEL1/D4 and WSEL2/D5) now go to the 386SX Data Bus instead of select jumpers; NSHADOW is no longer used.

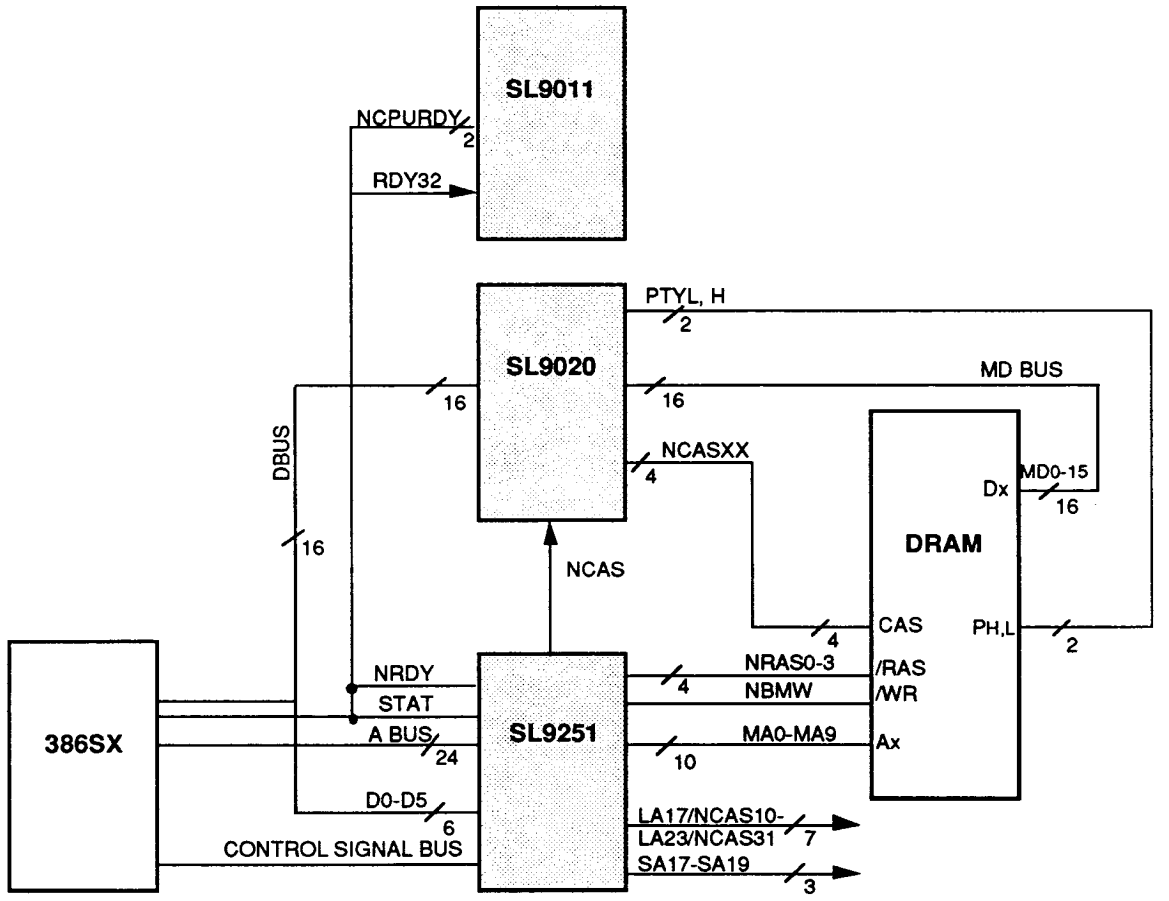


Fig. 2 386SX RAM Block Diagram/SL9251 Page Mode

SL9251 Page Interleave Mode

In SL9251 Page Interleave Mode, the SL9251 allows full utilization of the 20 internal option registers. SL9251 Page Interleave is invoked by writing configuration Register #1 (address 12h) D1=0 and D0=1, and writing configuration Register #2 D0=1 (address13h). The RAM block diagram is shown in Figure 3. Note that the option selects (MSEL1/D0-MSEL4/D3, WSEL1/D4 and WSEL2/D5) now go to the 386SX Data Bus instead of select jumpers. The memory CAS lines are no longer driven from the SL9020, but hook direct from the SL9251 (LA17/NCAS10-LA23/NCAS31, NCAS/NCAS00 and NCAS01).

Since the LAXX/CASXX lines are CAS outputs in the SL9251 page interleave mode, an external buffer is used to provide the A to LA conversion, with the SL9251 signal NENB245 used to select the buffers.

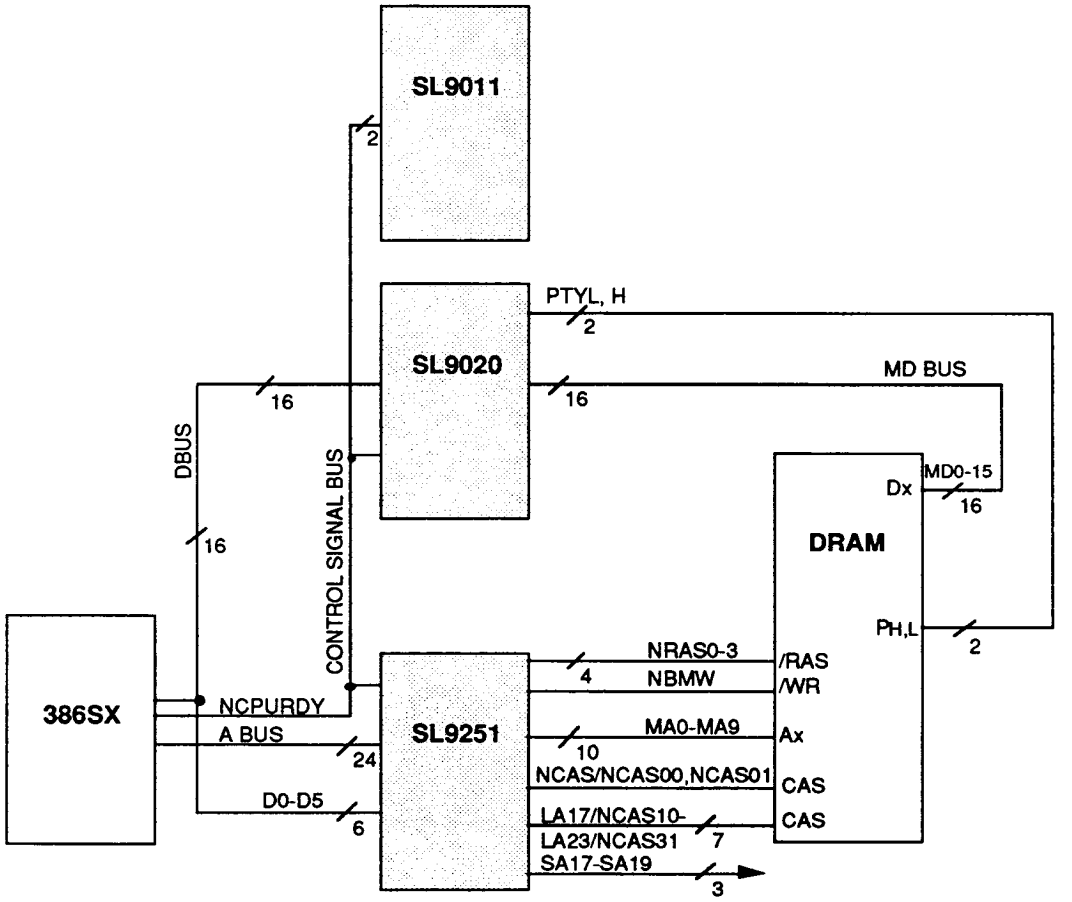


Fig. 3 386SX RAM Block Diagram/SL9251 Page Interleave Mode

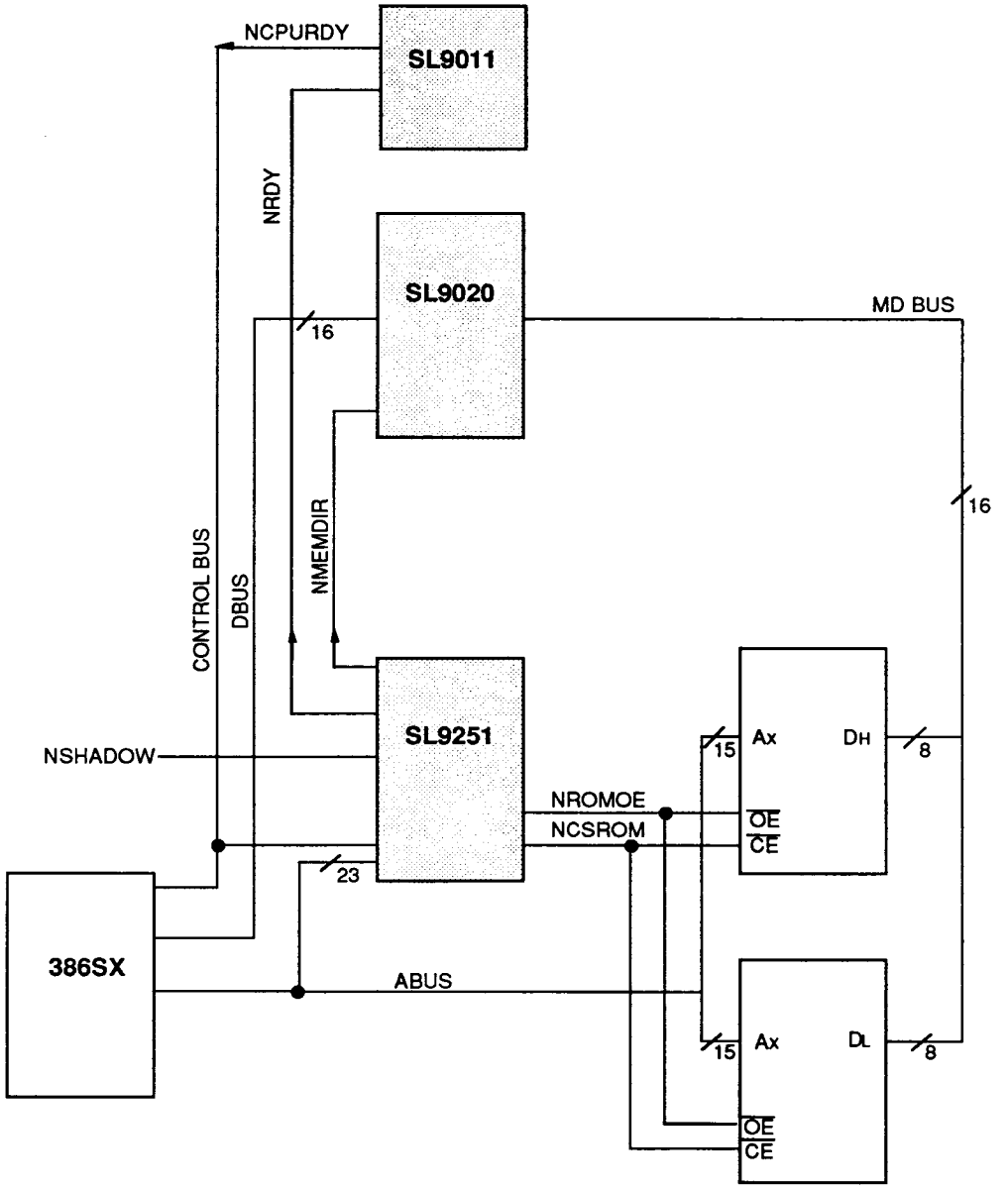


Fig. 4 386SX ROM Block Diagram/SL9250 and SL9251 Modes

SL9251 vs. SL9250 Pin Difference

Signals present on the SL9250, not supported on the SL9251.

PIN NO.	PIN NAME
58	ADD20
77	MA81
9	NLRAM
71	NPAG4K
57	NRAS
73	TEST3
60	TEST4

SL9251 Additions

Signals not present on the SL9250, present on the SL9251.

PIN NO.	PIN NAME
71	A0
77	NENB245
57	NFSTRST

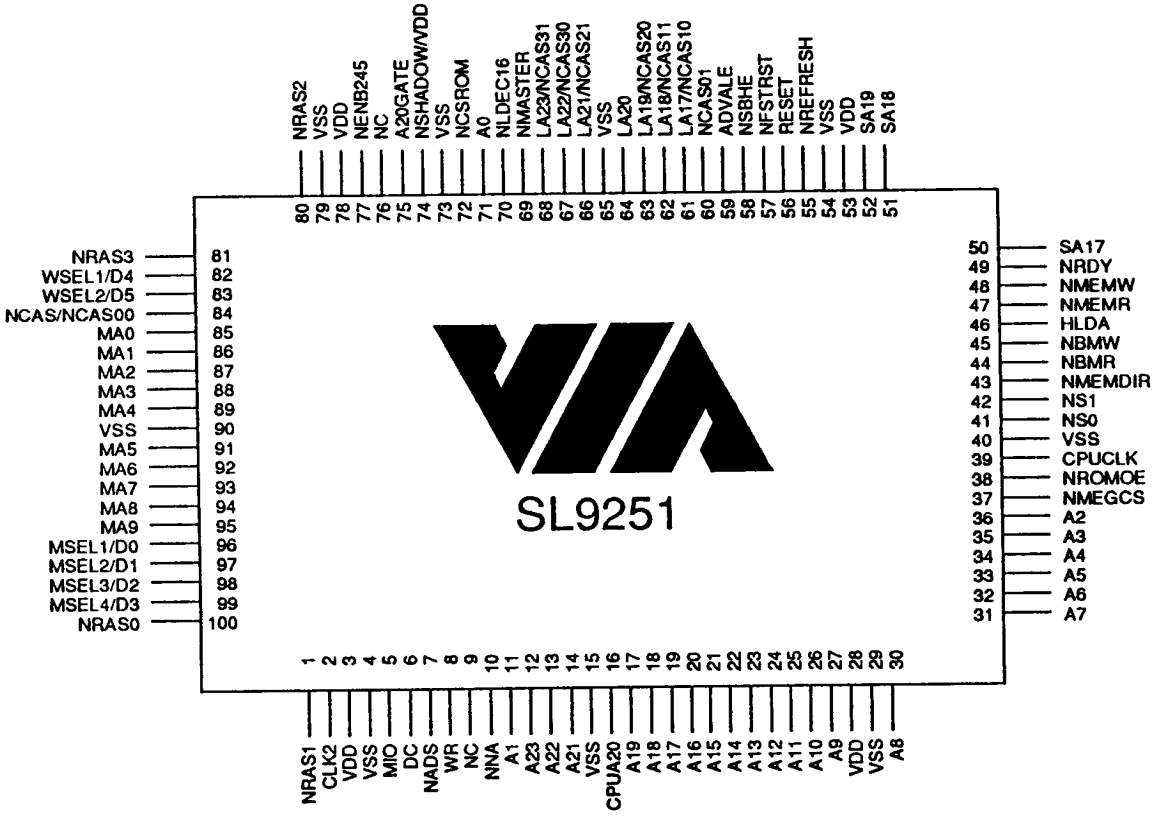
SL9251 Additions/Multi Function

Signals present on the SL9250, present on the SL9251 with multi functions.

PIN NO.	PIN NAME
61	LA17/NCAS10
62	LA18/NCAS11
63	LA19/NCAS20
66	LA21/NCAS21
67	LA22/NCAS30
68	LA23/NCAS31
96	MSEL1/D0
97	MSEL2/D1
98	MSEL3/D2
99	MSEL4/D3
82	WSEL1/D4
83	WSEL2/D5
84	NCAS/NCAS00
74	NSHADOW/VDD
73	GND

Table 1 SL9250 vs. SL9251 Pin Changes

PINOUT



PIN DESCRIPTION SL9251

SYMBOL	PIN	TYPE	DESCRIPTION
A0-A16	71,11,36,35,34, 33,32,31,30,27, 26,25,24,23,22, 21,20	I	CPU Address Bus.
A17-A19 A21-23	19,18,17, 14,13,12	I/O	CPU Address Bus.
A20GATE	75	I	CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH.
ADVALE	59	O	Advanced Address Latch Enable from memory controller. It latches local bus address for the system bus.
CLK2	2	I	Input Clock used to clock internal state machine. It is 2 times the frequency of the CPUCLK.
CLK8042	76	I	7 MHz clock input. It is used to internally generate a RAS time out. (Page mode.)
CPUA20	16	I/O	CPU Address Bus, bit 20.
CPUCLK	39	I	Clock synchronized with 386SX internal clock. It is CLK2 divided by two.
DC	6	I	CPU Status Signal. Differentiates between Data and Control instructions.
HLDA	46	I	CPU Output Signal, asserted to signal that the CPU has relinquished control of the bus to the device requesting MASTER or DMA. It is used to tri-state SLOT addresses during master.
LA20	64	I/O	Local address bus, bit 20. This is CPUA20 gated with A20GATE.
LA17/NCAS10	61	I/O	Local address bus LA17 in SL9250 and SL9251 page modes. In SL9251 page interleave mode, it is CAS for Bank 1, LOW byte.
LA18/NCAS11	62	I/O	Local address bus LA18 in SL9250 and SL9251 page modes. In SL9251 page interleave mode, it is CAS for Bank 1, HIGH byte.

PIN DESCRIPTION SL9251 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
LA19/NCAS20	63	I/O	Local address bus LA19 in SL9250 and SL9251 page modes. In SL9251 page interleave mode, it is CAS for Bank 2, LOW byte.
LA21/NCAS21	66	I/O	Local address bus LA21 in SL9250 and SL9251 page modes. In SL9251 page interleave mode, it is CAS for Bank 2, HIGH byte.
LA22/NCAS30	67	I/O	Local address bus LA22 in SL9250 and SL9251 page modes. In SL9251 page interleave mode, it is CAS for Bank 3, LOW byte.
LA23/NCAS31	68	I/O	Local address bus LA23 in SL9250 and SL9251 page modes. In SL9251 page interleave mode, it is CAS for Bank 3, HIGH byte.
MA0-MA9	85,86,87,88, 89,91,92,93, 94,95	O	RAM Address Bus Output. Directly drives DRAM address inputs.
MIO	5	I	CPU output signal. When HIGH, it indicates a memory cycle, when LOW it indicates an I/O cycle.
MSEL1/D0-MSEL4/D3	96,97,98,99	I	On-board Fast RAM memory size and type select in SL9250 mode, data bus D0-D3 in SL9251 mode. Internally pulled down.
NADS	7	I	CPU output control signal, asserted when address bus outputs are valid.
NSBHE	58	I	Byte HIGH Enable, from SL9011. It is used to determine address/byte boundaries for CAS interleave.
NBMR	44	O	Buffered Memory Read signal. Used to latch the parity in the SL9025 Address Controller chip.
NBMW	45	O	Buffered Memory Write signal. Used to drive DRAM write input.
NC	9,76		No Connect, leave open.
NCSROM	72	O	LOW assert ROM Chip Select. Connects directly to system ROM CS.

PIN DESCRIPTION SL9251 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NENB245	77	O	Low assert buffer enable to route A17-A23 to LA17-23 when in SL9251 mode. It directly drives LS245 Enable Pin.
NFSTRST	57	O	LOW assert Fast Reset. I/O Port 92 Bit 0 output to support PS2 Fast Reset.
NLDEC16	70	O	Decode signal for on-board local HIGH-speed RAM. Indicates a local DRAM transfer is in process.
NMASTER	69	I	Asserted when an external device has control of the AT Bus at slot card output. Used to set address direction from SLOT to system.
NCAS/NCAS00	84	O	Memory column address strobe. Asserted when CPU, DMA or MASTER is accessing the memory in SL9250 or SL9251 page mode. In SL9251 page interleave mode, it is Bank0 LOW byte CAS.
NCAS01	60	O	Memory Column Address Strobe for Bank0, high byte in SL9251 page interleave mode.
NMEGCS	37	O	Select Decode for lower 1M of memory. Used to drive SL9011 NMEGCS input.
NMEMDIR	43	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is used to drive SL9020 NMEMDIR input.
NMEMR	47	I	Read Memory command from SL9011/SLOT.
NMEMW	48	I	Write Memory command from SL9011/SLOT.
NNA	10	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
NRAS0-3	100,1,80,81	O	Row Address Strobes for Banks 0,1,2 & 3 for the on-board memory. Generated during CPU, DMA or MASTER cycle for memory access. Used to directly drive DRAM RAS inputs.
NRDY	49	O	Asserted one clock cycle after NNA is asserted at the end of a local memory cycle. Used to signal SL9011 that data is ready.

PIN DESCRIPTION SL9251 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NREFRESH	55	I	On-board RAM refresh signal.
NROMOE	38	O	Enables ROM output during ROM read cycles. Connects directly to ROMOE pin.
NSHADOW/VDD	74	I	When asserted, enables shadowing in SL9250 mode. In SL9251 mode, it must be pulled HIGH.
NS0,1	41,42	O	80286 compatible status signals for the AT System Controller SL9011.
RESET	56	I	Active HIGH Reset from system controller.
SA17-19	50,51,52	O	System Address Bus.
VDD	3,28,53,78	-	+5V. Power.
VSS	4,15,29,40, 54,65,73,79,90	-	0V. Ground.
WR	8	I	CPU output control signal Write.
WSEL1/D4 WSEL2/D5	82,83	I	Wait-state Select options in SL9250 mode. Data bus D4 and D5 in SL9251 modes. Internally pulled up.

ROM/RAM DECODE / SL9250 PAGE MODE

The device provides all necessary circuitry to decode on board RAM/ROM cycles. User can select one to four banks using 256K, 1MB, or a mix of both using regular or Static Column DRAMs.

The system can be configured for 512K Bytes to 8M Bytes. The bank selection code & sizes are as follows:

D3 MSEL4	D2 MSEL3	D1 MSEL2	D0 MSEL1	RAS0/CAS0	RAS1/CAS1	RAS2/CAS2	RAS3/CAS3	
0	0	0	0	0-512K				
0	0	0	1	0-512K	512-640/1M-1M+384			
0	0	1	0	0-512K	512-640/IM+512-1M+896	1M-1M+512		
0	0	1	1	0-512K	512-640/2M-2M+384	1M-1M+512	1M+512-2M	
0	1	0	0	0-512K				
0	1	0	1	0-512K	512K-640/1M-1M+384			256K DRAMs
0	1	1	0	0-512K	512K-640/3M-3M+384	1M-3M		1M DRAMs
0	1	1	1	0-512K	512K-640/5M-5M+384	1M-3M	3M-5M	
1	1	0	0	0-640/1M-2M/2M-2M+384				
1	1	0	1	0-640/1M-2M/4M-4M+384	2M-4M			
1	1	1	0	0-640/1M-2M/6M-6M+384	2M-4M	4M-6M		
1	1	1	1	0-640/1M-2M/8M-8M+384	2M-4M	4M-6M	6M-8M	

Table 2

Page size is 2KB for 256K DRAMs and 4KB for 1M DRAMs.

When CPU accesses the memory for the first time, the controller runs a one wait state memory cycle and asserts RAS and CAS low at appropriate times (Table 2). CAS is de-asserted at the end of the cycle, but RAS is kept asserted and the current row address is also strobed in an internal register. For all subsequent cycles, the row address is compared to the stored value in the register.

For a match (HIT), RAS is kept asserted. For read cycles, CAS is stroked immediately after ADVALE goes low. For write cycles CAS is strobed 1 CPUCLK cycle after ADVALE goes low.

For a mismatch of the addresses (MISS), the RAS is de-asserted (goes high) for three CLK2 cycles. The RAS is asserted again and the new row address is stored in the register. The controller runs a 1 or 2 wait-state memory cycle depending on the wait-state selection.

CPU Addresses A11-A21, A1 are passed onto MA0-9 as unlatched row addresses whereas A2-A11 are latched on the falling edge of ADVALE and passed onto MA0-9 as column addresses at appropriate time. RAS, MUX, and CAS are separated by one CLK2 period as shown in the timing diagram. This latching of column addresses allows use of static column DRAMs as well.

ROM/ RAM CONTROL

The SL9251 Memory Controller provides all the circuitry needed to generate RAM/ROM controls. RAM controls for Row Address Strobe (NRAS0-3), Column Address Strobe (NCAS), RAM Read Write (NBMW, NBMR), Ready from 16 bit on-board RAM read write (NRDY), next CPU address (NNA), and non on-board memory cycle status (NS0, NS1) are generated at appropriate times as shown in the timing diagram.

MIO	DC	WR	ADDRESS	CYCLE TYPE
1	0	0		MEM CODE READ
1	0	1	2/0	HALT/SHUTDOWN
1	1	0		MEM DATA READ
1	1	1		MEM DATA WRITE
0	0	0		INTA
0	0	1		NOT POSSIBLE
0	1	0		I/O DATA READ
0	1	1		I/O DATA WRITE

Table 3

The chip allows for use of slower DRAMs with selectable wait states. The wait states for a 16 bit, on board, memory miss can be set using the following table.

CPU SPEED	WSEL1	WSEL2	WAIT STATES READ	WAIT STATES WRITE	MEMORY SPEED (ns)
16	0	0	2	2	100
	1	0	2	1	100
	1	1	1	1	80
20	0	0	2	2	80
	1	0	2	1	80
	1	1	1	1	60

Table 4

ROM controls NCSROM & NROMOE are asserted low at appropriate time when address 0E0000h-0FFFFFh (low) or FE0000h-FFFFFFh (high) is decoded during a memory cycle. The timing relationship is shown in the timing diagram. These will be disabled if Shadow RAM option is used. When Shadow RAM option is used by pulling NSHADOW pin low, the ROM code is copied in the corresponding RAM location by BIOS, and the subsequent ROM code reads will be decoded as RAM reads & will be much faster. BIOS can be customized to activate this option at boot. The NSHADOW option affects the 128K region immediately below 1 Meg.

REFRESH SUPPORT

The SL9251 provides support for DRAM refresh. During refresh NRAS0-3 are asserted low, NCAS is held high, the current bus state is ignored, and a refresh address generated by the SL9025 Address Controller is passed from A Bus to MA Bus.

RAM

System RAM is interfaced as shown in Fig. 1. 16 Bit memory data is connected to the MD Bus. Memory data flow is between D Bus and MDbus via the SL9020 Data Controller. Parity data is generated and checked in the SL9020 through parity byte bits PTYL and PTYH. The SL9020's output memory CAS strobes are: NCASA02, NCASA13, NCASB02, NCASB13.

RAM address is passed or latched internally in the SL9251 as necessary from A Bus to memory MA Bus (10 Bit). The MA Bus features 12ma drive capability. The SL9251 provides 24ma direct drive lines for memory RAS (NRAS0-NRAS3) as well as memory Write (NBMW). Eleven signals are output by the SL9251 to facilitate system control during RAM transfers. Their function and destination are covered in Table 5.

SIGNAL	DESTINATION	FUNCTION
ADVALE	SL9025 Address Controller	Used to latch the 386SX address bus A1-A16 to the system address bus SA1-SA16.
	Internal	Used to latch the 386SX address bus A17-A19 to the system address bus SA17-SA19. Transfers and latches 10 Bit CAS address (MA0-MA9) and NLDEC16.
NBMR	SL9025 Address Controller	Trailing edge used to latch parity error.
NBMW	SL9011 System Controller	Drives WE for RAM.
NCAS	SL9020 Data Controller	Used to assert SL9020 CAS output drivers: CASLA, CASLB, CASHA and CASHB.
NMEMDIR	SL9020 Data Controller	Sets MDBUS/DBUS direction. HI = D→MD
NLDEC16	SL9011 System Controller	Indicates a local RAM decode.
NMEGCS	SL9011 System Controller	Indicates a local RAM/ROM decode less than 1Meg address.
NRDY	SL9011 System Controller	Indicates the memory is ready with data.
NNA	386SX	Pipeline request to 386SX.
NS0-NS1	SL9011 System Controller	286 compatible status signal indicating a Read, Write, interrupt acknowledge or idle state.

Table 5. SL9251 Control Signal Function / SL9250 Page Mode

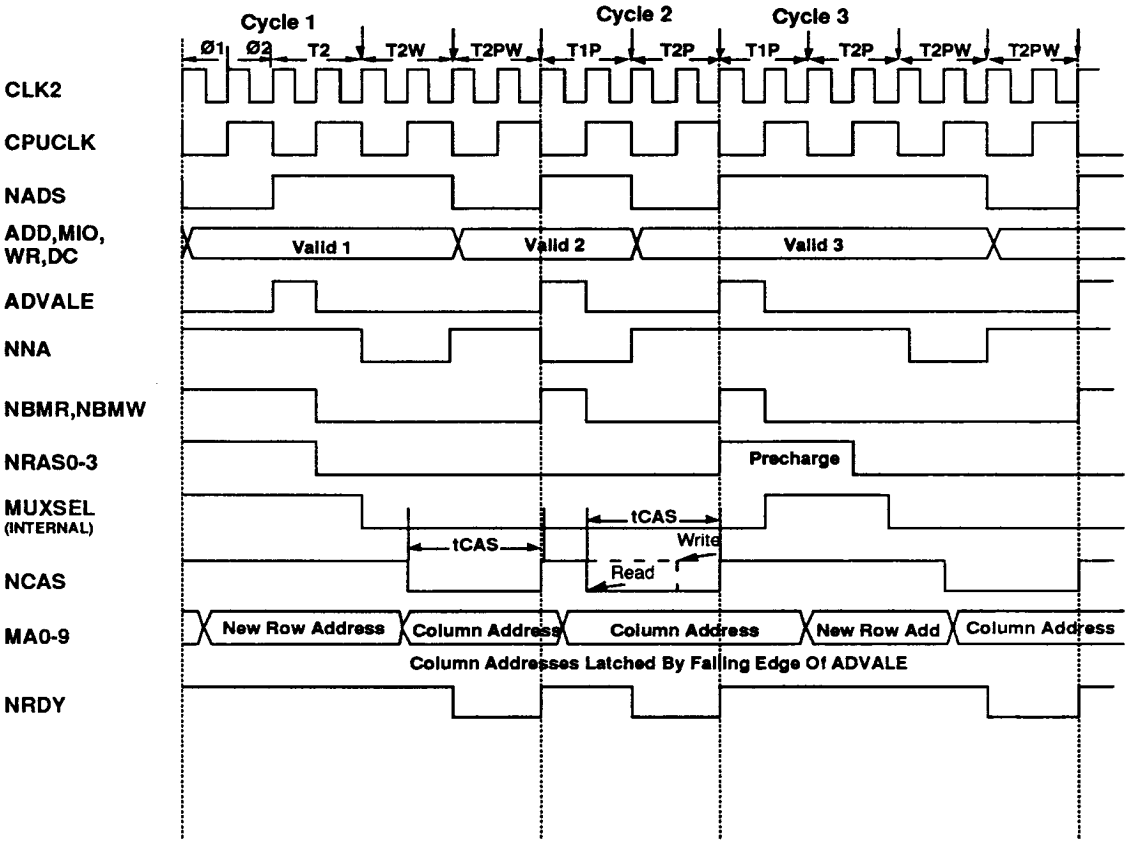


Fig. 5 On-Board Memory Timing Diagram/SL9250 Mode

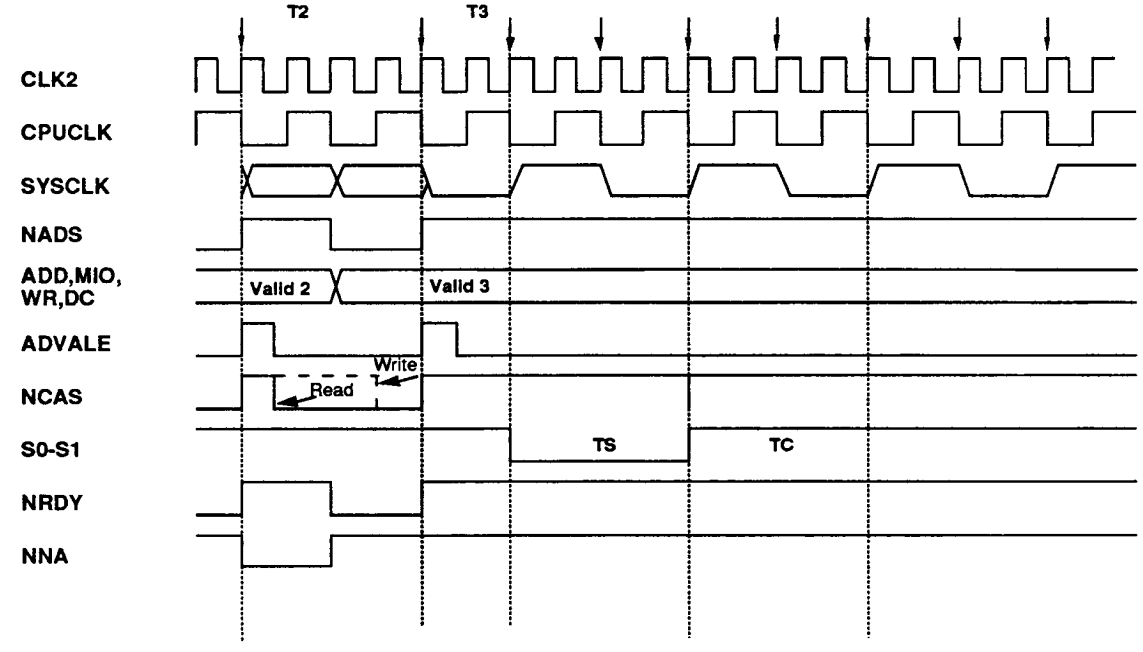


Fig. 6 Off-Board Memory Timing Diagram/SL9250 Mode

RAM (Cont'd)

A local memory cycle (cycle1 in Fig. 5), begins during T1 when the 386SX asserts NADS, MIO, and DC. SL9250 output NLDEC16 asserts, indicating a memory decode within the range specified by memory select jumpers MSEL1-MSEL4, as shown in Table 1. If the present address is within the lower 1 meg range, then MEGCS will also assert at this time. "ROW" addresses A11-A19 and CPUA20 are passed directly through the SL9250 into MA0-MA9. ADVALE is asserted during phase 1 (Phase 1, CPUCLK low) of T2. If the cycle is a Write, the start of T2 phase 2 (Phase 2) brings NBMW valid, thus setting RAM WE. At this time, a RAS line will assert (NRAS0-NRAS3) strobing the MA0-MA9 address into the appropriate bank. ADVALE negates at phase 2, latching A1 through A10 in the SL9250. T2W phase 1 enables latched column address on MA0-MA9, and sets NNA to the 386SX requesting the next cycle to be pipelined. T2W phase 2 asserts NCAS to the SL9020 Data Controller, where the appropriate CAS line CASLA, LB, HA or HB is asserted, thus strobing the RAM column address and enabling RAM data output. NRDY to CPU (via SL9010) asserts at T2PW, signaling CPU to latch RAM data at end of T2PW phase 2. NADS also asserts, indicating a valid pipeline cycle in response to the previous NNA. T2WP phase 2 ends with CPUCLK dropping low, finishing the first cycle: NBMW, NCAS, NRDY and NADS negate, RAM data latches in the 386SX CPU.

The next cycle, (cycle 2 in Fig. 6), T1P, asserts ADVALE, which enables a new column address on MA1-MA9. NNA is asserted, requesting the next cycle to be pipelined. AT T1P phase 2 advale negates, latching column addresses, asserts NBMR or NBMW as appropriate, and NCAS. NCAS assertion gives rise to the assertion of the appropriate RAM CAS line CASLA, LB, HA, or HB. T2P phase 1 negates NNA and asserts NRDY, signaling a page hit. The 386SX asserts NADS indicating a new pipeline cycle. T2P phase 2 end latches RAM data in the 386SX and negates NADS.

Cycle 3 begins in state T1P phase 1 with NADS, NBMW, NRDY, NBUS, NNA NCAS and NRAS negated. ADVALE is asserted. Since NRAS is negated, a page miss is indicated. phase 2 negates ADVALE, asserts NBMW, and sets internal MUXSEL high. The mux is now driving a new row address on MA0-MA9. T2P phase 2 asserts the appropriate NRAS0-NRAS3 strobe, latching DRAM row address. T2P phase 2 end drops internal MUXSEL, presenting as new column address on MA0-MA9. T2PW phase 2 negates NCAS, thus strobing a new column address into DRAM and enabling DRAM output. The second wait state T2PW phase 1 drops NRDY. Data for cycle 3 will then be latched in the CPU at the end of phase 2.

ROM

System ROM is enabled from 0E0000H to 0FFFFFH, or from FE0000H to FFFFFFH. 2 wait states are forced for any ROM access. If shadowing is selected, by asserting NSHADOW high on SL9250, then NROMOE and NCSROM signals are not asserted during the 386SX Read cycle, and a RAM cycle is started instead.

System ROM is added as shown in Fig. 4. 16 Bit ROM data out is connected to the MD Bus. 15 bit ROM address input is connected directly to the 386SX A Bus. ROM enable signals OE and CE are connected to the SL9250 output signals NROMOE and NCSROM. Data path is from MD Bus to 386SX D Bus via the SL9020 Data Controller.

A Read cycle is started when the 386SX asserts MIO, D/C and NADS. The "cycle" is latched internally on the rising edge of CLK2, when CPUCLK is high and a valid ROM address is on A1, A17-A19, A21-A23, and CPUA20. NCSROM is first asserted when a valid ROM address is decoded at T1A. When CPUCLK goes low and CLK2 rises high, (T2A), NBUS16 is asserted for the duration of CPUCLK low, indicating to the 386SX a 16 bit cycle. Next CLK0, CPUCLK goes high and CLK2 rising high (T2B), NROMOE asserts, thus enabling ROM outputs. NMEMDIR asserts at this time, as well, signaling the SL9020 Data Controller to switch the memory data path from MDBus to DBus. After 2 wait states, on CLK2 rising high at T2W2B, NRDY asserts, signaling the SL9010 Controller that data is ready. The SL9010 drops NCPURDY, the CPU latches Bus data, and enters the second 16 Bit cycle by negating BE0, BE1, and NADS at T12 A. The second cycle repeats as the first. After the last ROM access, a valid ROM address will not be decoded and thus NCSROM, NRDMOE, and NMEMDIR will be negated in T1 A.

OPTION REGISTERS

The twenty SL9251 option registers and their functions are listed in Table 6. Following is a description of each register. The option registers are accessed through the index register. Since system RAM, ROM configuration is determined by the option registers, the system BIOS should configure the option registers early in the POST routine. Configuration Registers #1 and #2 should be written first, setting SL9250 vs. SL9251 modes. If a SL9251 mode is selected, the option registers 0 through 11h may be written. If the SL9250 mode is selected (or as defaulted on power up), the option registers should not be written. All option registers are 6 bits wide.

ADDRESS	FUNCTION
0	Shadow CTL 0
1	Shadow CTL 1
2	Shadow CTL 2
3	Shadow CTL 3
4	Shadow CTL 4
5	Shadow CTL 5
6	Shadow CTL 6
7	Shadow CTL 7
8	RAM Wait State Select
9	Remap
A	Local ROM CS 1
B	Local ROM CS 2
C	Local ROM CS 3
D	RAS Timing Register
E	CAS Timing Register 1
F	CAS Timing Register 2
10	Disable to 0K
11	Memory Select
12	Configuration #1
13	Configuration #2
92	Port 92

Table 6 Option Register Functions

OPTION REGISTER, INDEX I/O, 122h

All accesses to the opiton registers are through the index register. The index register is located at I/O address 122h and serves to:

1. point to the desired option register (index), and
2. port data to/from the selected option register.

Thus, only one I/O address is used as a port to the option registers. The index register toggles between index address and data. Upon power up the index register is ready to accept an address. This is accomplished by a write to I/O 122h with the index address as data. The next write (or read) to I/O 122h will write (read) the indexed option registers. This address/data toggling continues with each I/O Port 122 acess.

SHADOW CONTROL REGISTER, INDEX 00-07h, R/W

Each of the eight Shadow registers are divided into three sections, each of which control a 16K block of local RAM (24 blocks/384K total). Two weighted bits per block, SDWB1 and SDWB2, control whether the RAM access is to be locally disabled, 00; Read system/Write local (backfill), 01; Read local/Write system, 10; or Read/Write local, 11.

Index Port	D5	D4	D3	D2	D1	D0
0	A8000	ABFFF	A4000	A7FFF	A0000	A3FFF
1	B4000	B7FFF	B0000	B3FFF	AC000	AFFFF
2	C0000	C3FFF	BC000	BFFFF	B8000	BBFFF
3	CC000	CFFFF	C8000	CBFFF	C4000	C7FFF
4	D8000	DBFFF	D4000	D7FFF	D0000	D3FFF
5	E4000	E7FFF	E0000	E3FFF	DC000	DFFFF
6	F0000	F3FFF*	EC000	EFFFF	E8000	EBFFF
7	FC000	FFFFF*	F8000	FBFFF*	F4000	F7FFF*

SDWB1	SDWB0	
0	0	Shadow RAM disable (RD/WR to system bus)
0	1	RD system bus WR to local RAM (Copy SYS or backfill ROM to RAM)
1	0	RD local RAM WR system bus (Shadow RAM WR protect)
1	1	RD/WR local RAM (Shadow RAM)

** Disable local ROM (if enabled) to activate system access.*

RAM WAIT STATE REGISTER, INDEX 08h, R/W

The wait state register sets the number of RAM wait states for page hits, page miss writes and page miss reads. Two weighted bits are used to set the desired numbers of wait states (0-4) for each operation. Note the power-up default values.

Register 8h

D5	D4	D3	D2	D1	D0
RDMSWTB1	RDMSWTB0	WRMSWTB1	WRMSWTB0	HITWB1	HITWB0

Page Hit Wait States

D1	D0	
0	0	=0
0	1	=1 Default
1	0	=2
1	1	=3

Page Miss Wait States

D3	D2	
0	0	=1
0	1	=2
1	0	=3
1	1	=4 Default

Page Miss Read Wait States

D5	D4	
0	0	=1
0	1	=2
1	0	=3
1	1	=4 Default

RAM REMAP REGISTER, INDEX 09h, R/W

The remap register uses the 3 least significant bits D2-D0 (weighted) to select 8 different remap options. The remap options operate over the 384K segment of RAM located from CPU address A0000-FFFFF (640K - 1M). All options allow accessing the total 384K segment, except disable, which leaves the 384K RAM segment unused and unaccessable. The table lists 2 columns: 1. TOP RAM, and 2. ROM. Top RAM is the amount of 384K RAM that is remapped to the "TOP" of RAM, where TOP refers to maximum amount of RAM installed. Refer to the RAM Map Register. ROM is the amount of 384K RAM that is addressed as "ROM" in the 384K area between 640K and 1M. An example is shown for 2 Meg installed RAM with the 256K remap option, and 2 Meg installed, remap disabled.

Register 09h

D5	D4	D3	D2	D1	D0
0	0	0	RMPCD2	RMPCD1	RMCD0

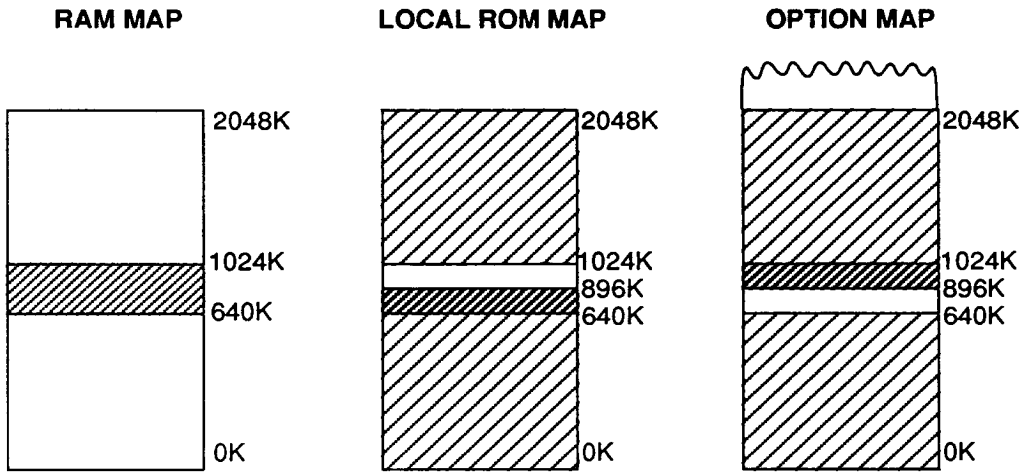
D2	D1	D0	TOP RAM		ROM
0	0	0	0	0	-----
0*	0	1	512K	0	-----
0	1	0	128K	256K	C0000-FFFFF
0	1	1	256K	128K	E0000-FFFFF
1	0	0	288K	96K	E7FFF-FFFFF
1	0	1	320K	64K	F0000-FFFFF
1	1	0	352K	32K	F7FFF-FFFFF
1	1	1	384K	0	-----

* Set Disable Register bit D5=1 to disable RAM access from 512K to 640K.

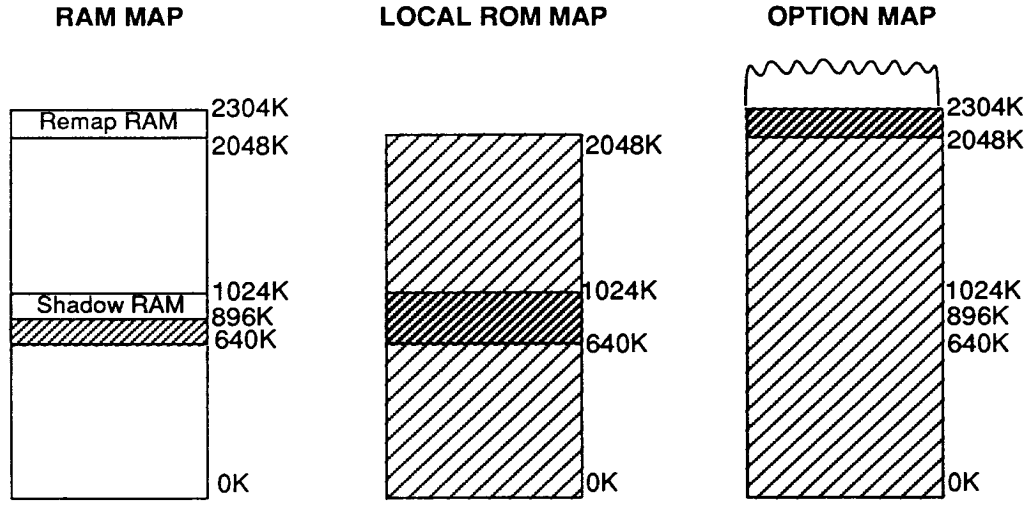
Reserved for future use. Must be set to 0.

SL9251 REMAP OPTION EXAMPLES

Remap Disabled (D=00h)



256K Remap (D=03h)

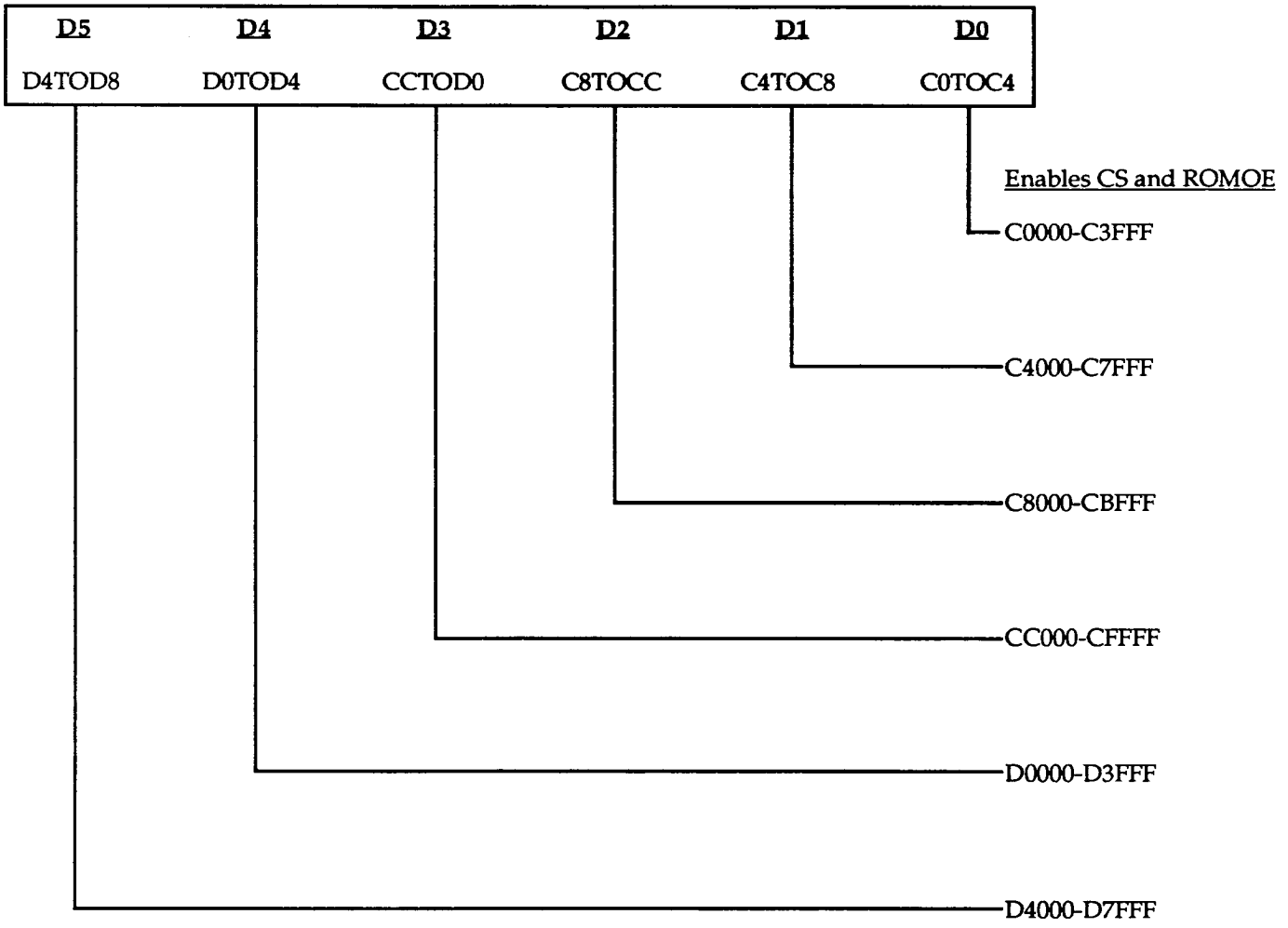


Shaded areas represent unaccessable addresses.

LOCAL ROM CS REGISTER #1, INDEX 0Ah, R/W

The local ROM CS Register #1 is used to set the CPU address range from C0000 to D7FFF over which ROM CS and ROMOE signals are generated (see also LOCAL ROM CS Register #2 and LOCAL ROM CS Register#3). Setting the bit(s) DX=1 will enable the ROM chip select and output enable over the listed 32K segment range(s). Any, none, or all bits may be set. Note that ROM address and RAM address must not be selected over the same CPU address. Default values after reset are 00.

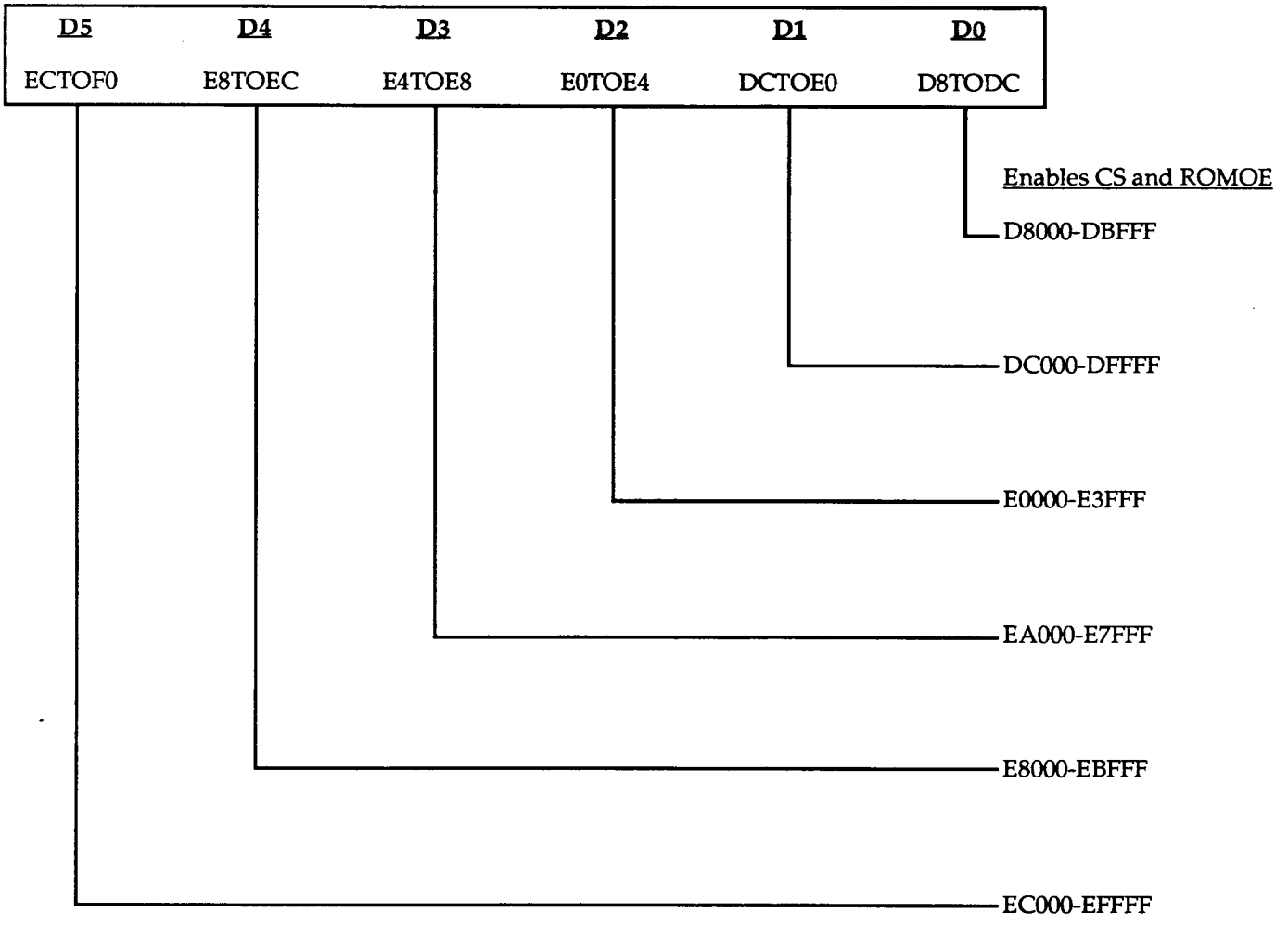
Register 0Ah



LOCAL ROM CS REGISTER #2, INDEX 0Bh, R/W

The local ROM CS Register #2 is used to set the CPU address range from D8000 to EFFFF over which ROM OE and ROM CS signals are generated (see also local ROM CS Register #1 and local ROM CS Register #3). Setting the bit(s) DX=1 will enable the ROM chip select and output enable over the listed 32K segment range(s). Any, none, or all bits may be set. Note that ROM address and RAM address must not be selected over the same CPU address. Default values after reset are 00.

Register 0Bh

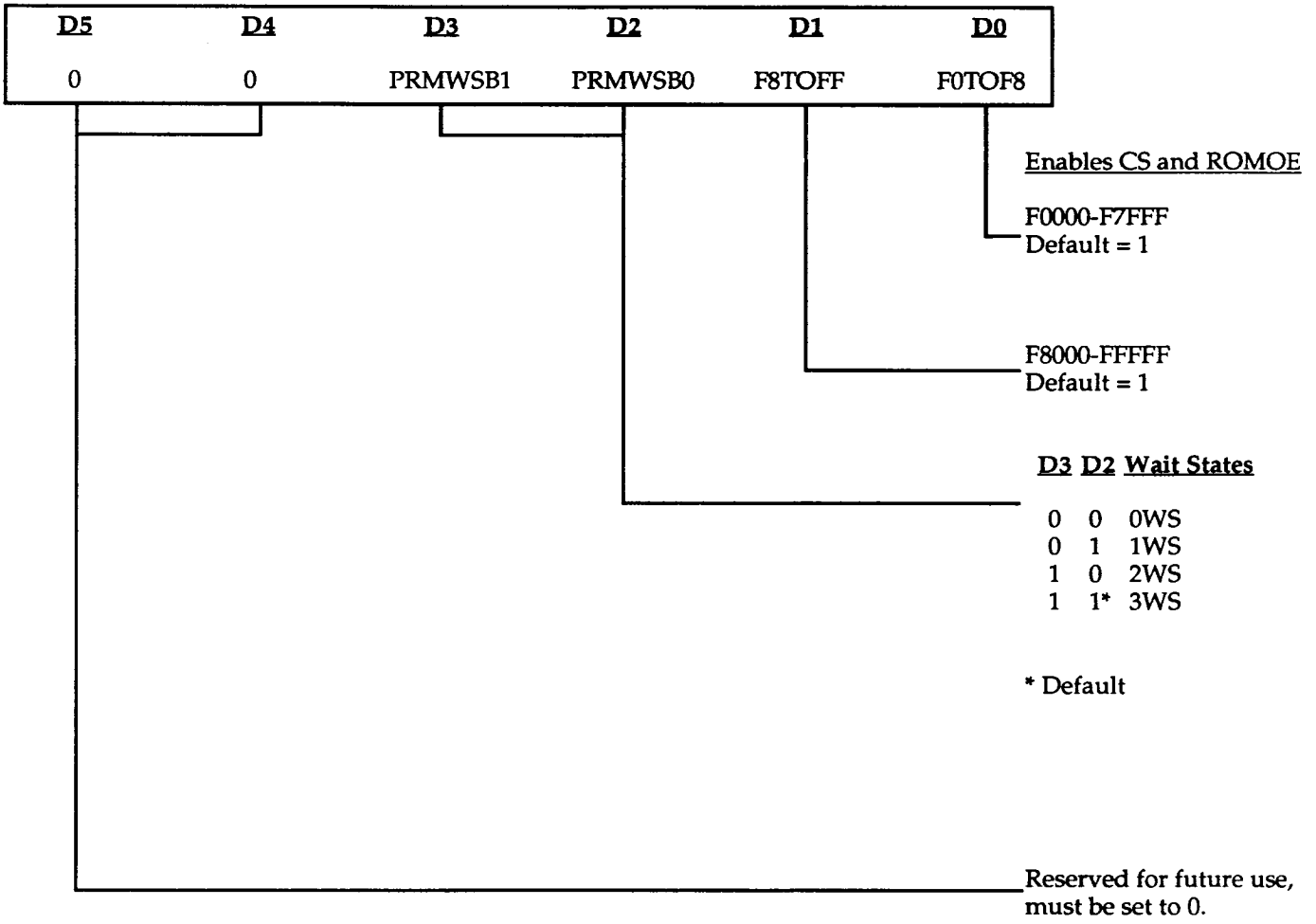


LOCAL ROM CS REGISTER #3, INDEX 0Ch, R/W

The local ROM CS Register #3 bits D0 and D1 are used to set the CPU address range from F0000 to FFFFF over which ROMOE and ROM CS signals are generated. Operation is the same as local ROM CS Register #2, except default values are D1=1 and D0=1.

Bits D2-D4 are weighted and used to select one of eight ROM wait state times. Bit five is 0.

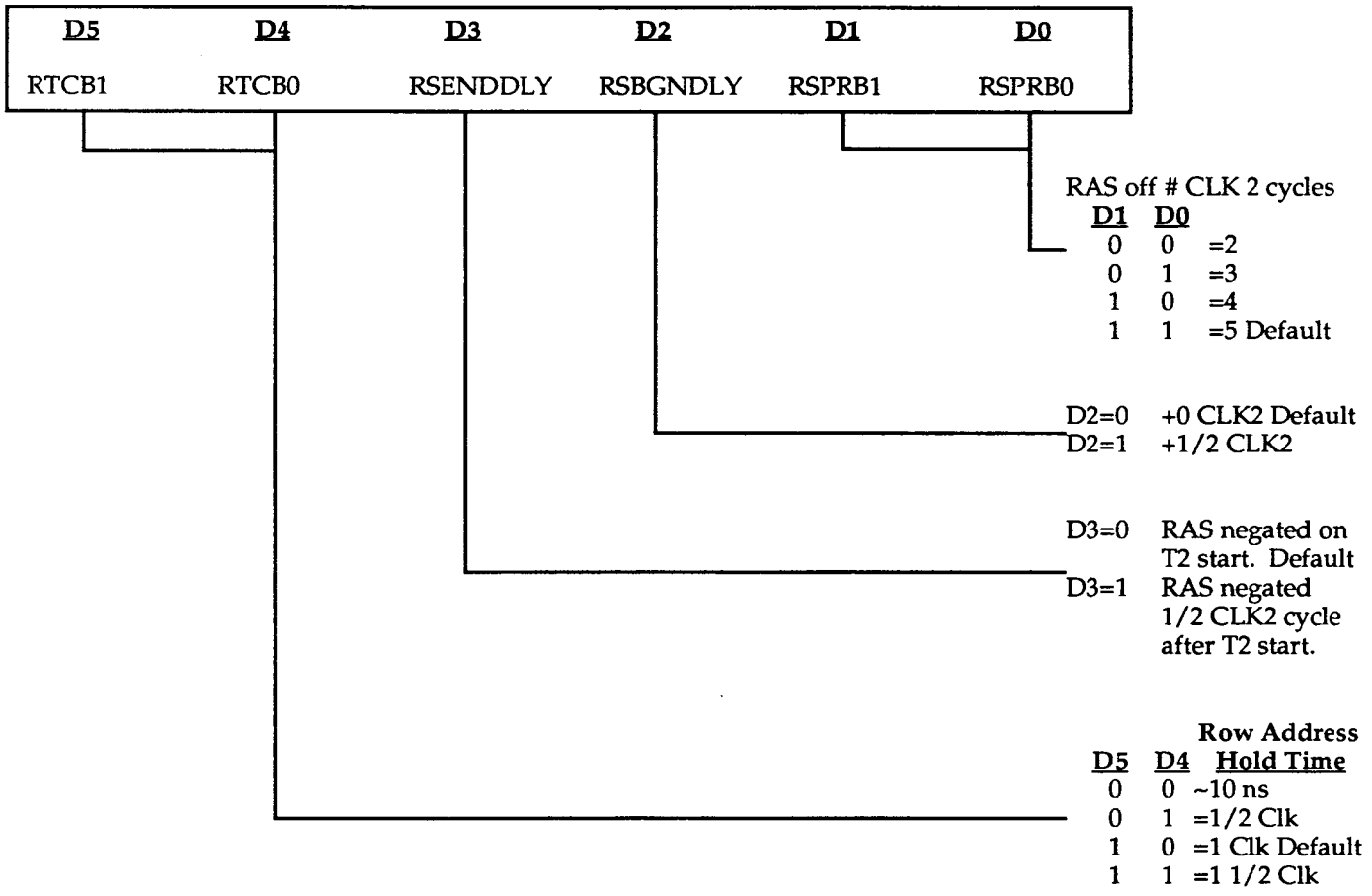
Register 0Ch



RAS TIMING REGISTER, INDEX 0Dh, R/W

The RAS timing register is used to set RAS off timing (precharge), RAS delay, and row address HOLD timing. RAS off timing bits D0 and D1 determine the time, in clock cycles, that RAS is held negated. RAS delay bit D3 allows one half clock cycle delay from NADS negation to RAS negation. Refer to Figures 7 and 8. When set, RAS off time bit D2 adds one half clock cycle to RAS off time. Row address hold time is set be bits D4 and D5. Table lists the relationship between timing register values, clock frequency, and RAM parameters tRD and tRAS.

Register 0Dh



$$tRD = (RSPR + RSBGNDLY)\frac{1000}{f}\ ns$$

Where:
- RSPR = #CLK 2 precharge cycles selected by bitsD0 and D1 in Register 0D.
- RSBGNDLY = #CLK 2 delay cycles selected by bit D2 in Register 0D.
- f = System CLK2 frequency in MHz.
- tRP = RAM RAS Precharge time, ns.

$$tRAS\ (Read) = 2(RDMSWT + 1)\frac{1000}{f} - tRP$$

Where:
- RDMSWT = # wait states selected by bits D5 and D4 in RAM wait state register, 08.

$$tRAS\ (Write) = 2(RWRMSWT + 1)\frac{1000}{f} - tRP$$

Where:
- RWRMSWT = # wait states selected by bits D3 and D2 in RAM wait state register, 08.

$$tCPN\ (Read) = MSRDCS\ \frac{1000}{f}$$

Where:
- MSRDCS = # CLK2 cycles selected by D2, D1 and D0 in Register OE.
- tCPN (Read) = RAM CAS precharge time in ns.

$$tCPN\ (Write) = MSWRCS\ \frac{1000}{f}$$

Where:
- MSWRCS = # CLK2 cycles selected by D5, D4 and D3 in Register OE.
- tCPN (Write) = RAM CAS precharge time in ns.

$$tRCD\ (Read) = tCPN\ (Read) - tRP$$
$$= (-RSPR - RSBGNDLY + MSRDCS)\frac{1000}{f}$$

Where:
- tRCD (Read) = RAM Read RAS to CAS delay in ns.

$$tRCD\ (Write) = tCPN\ (Write) - tRP$$
$$= (MSWRCS - RSBGNDLY - RSPR)\frac{1000}{f}$$

Where:
- tRCD (Write) = RAM Write RAS to CAS delay in ns.

$$tCAS\ (Read) = 2(ROMSWT + 1)\frac{1000}{f} - tCPN\ (Read)$$
$$= (2RDMSWT + 2 - MSRDCS)\frac{1000}{f}$$

Where:
- tCAS (Read) = RAM Read CAS time in ns.

$$tCAS\ (Write) = 2(ROMSWT + 1)\frac{1000}{f}\ ns - tCPN\ (Write)$$
$$= (2WRMSTWT + 2 - MSWRCS)\frac{1000}{f}$$

Where:
- tCAS (Write) = RAM Read CAS time in ns.

Table 7 SL9251 Equations

AC TIMING DIAGRAMS SL9251

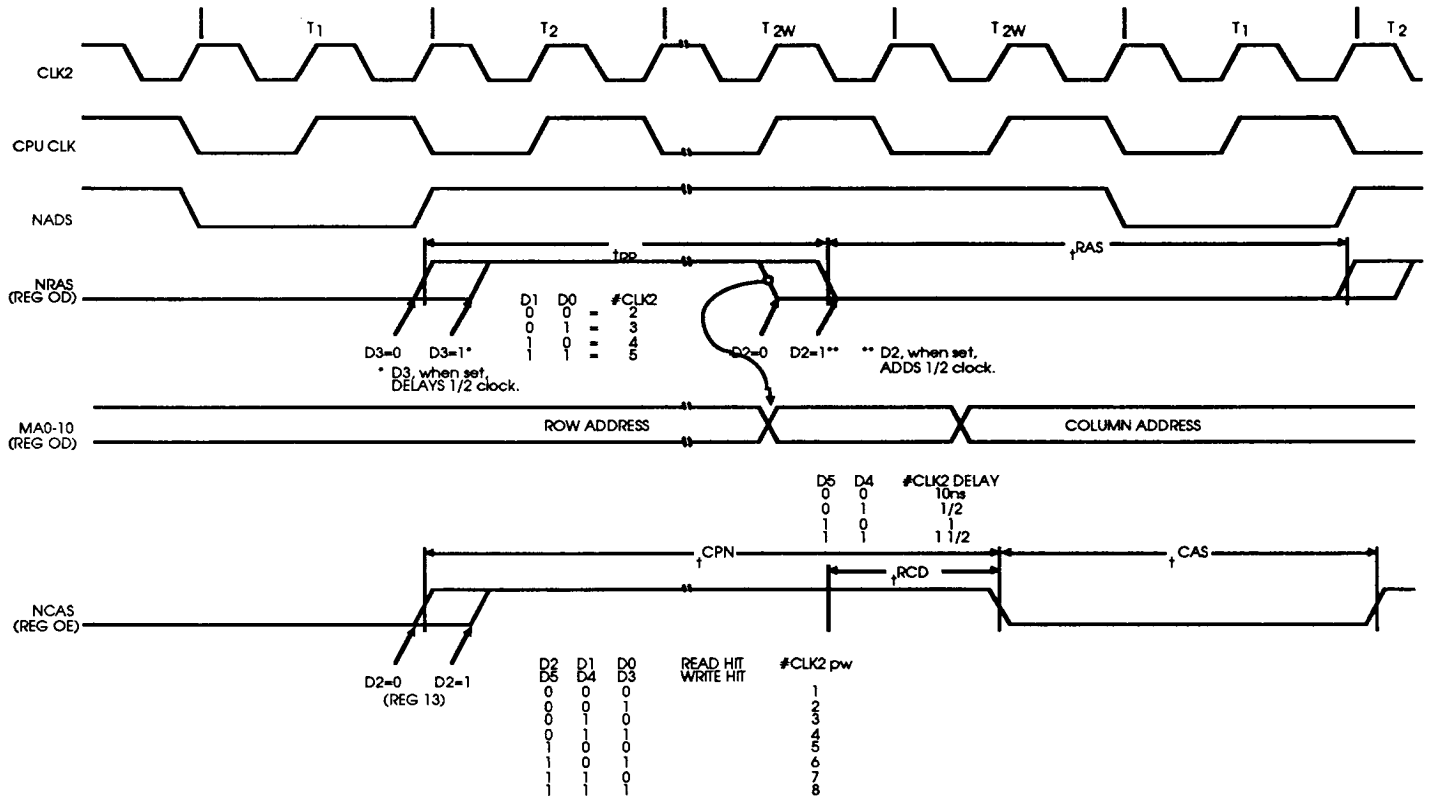
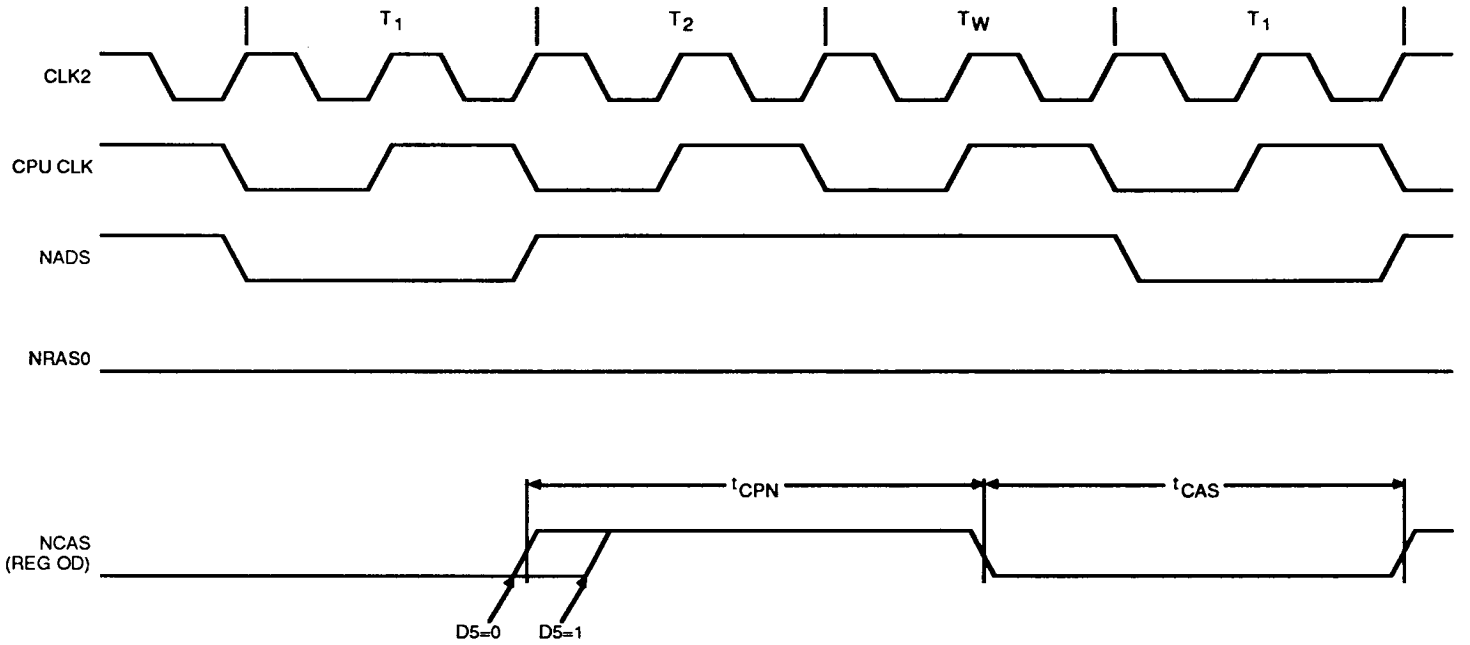


Fig. 7 Page Miss Timings

AC TIMING DIAGRAMS SL9251



D4	D3	#CLK2 Cycles (WRITE Hit)
0	0	1
0	1	2
1	0	3
1	1	4

D2	D1	D0	#CLK2 Cycles (READ Hit)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Fig. 8 Page Hit Timings

CAS TIMING REGISTER #1, INDEX 0Eh, R/W

The CAS timing register defines CAS timing for miss Read/Write cycles. Refer to figure 7. Read misses default to eight CLK2 cycles, and write misses default to seven CLK2 cycles, on power up. Bits D2, D1 and D0 are used to set NCAS False time (tcpn) in CLK2 cycles, for Read misses. Similarly, bits D5, D4 and D3 are used to set NCAS False time (tcpn), in CLK2 cycles, for Write misses. Table 7 lists the relationship between timing register values, clock frequency, and RAM parameters tcpn and tcas.

Register 0Eh

D5	D4	D3	D2	D1	D0
MSWRCSB2	MSWRCSB1	MSWRCSB0	MSRDCSB2	MSRDCSB1	MSRDCSB0

D2	D1	D0	# CLK2 Cycles NCAS False Read Miss
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

D2	D1	D0	# CLK2 Cycles NCAS False Write Miss
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

CAS TIMING REGISTER #2, INDEX 0Fh, R/W

CAS timing register #2 defines CAS timing for hit Read/Write cycles. Refer to figure 8. Bits D2, D1 and D0 are used to define the time (tcpn), in CLK2 cycles, NCAS is negated for Read hit cycles. Similarly, bits D4 and D3 are used to define the time (tcpn), in CLK2 cycles, NCAS is negated for Write hit cycles. Bit D5, when set, delays NCAS negation 1/2 CLK2 cycle. When D5=0, NCAS is negated at the beginning of T2. Both read and write bits default to two cycles on power up, and NCAS is negated at the beginning of T2.

Register 0Fh

D5	D4	D3	D2	D1	D0
CSENDDLY	HTWRDLB1	HTWRDLB0	HTRDCSB2	HTRDCSB1	HTRDCSB0

D2	D1	D0	# CLK2 Cycles NCAS Off Read Hit	
0	0	0	1	
0	0	1	2	Default
0	1	0	3	
0	1	1	4	
1	0	0	5	
1	0	1	6	
1	1	0	7	
1	1	1	8	

D4	D3	# CLK2 Cycles NCAS Off Write Hit	
0	0	1	
0	1	2	Default
1	0	3	
1	1	4	

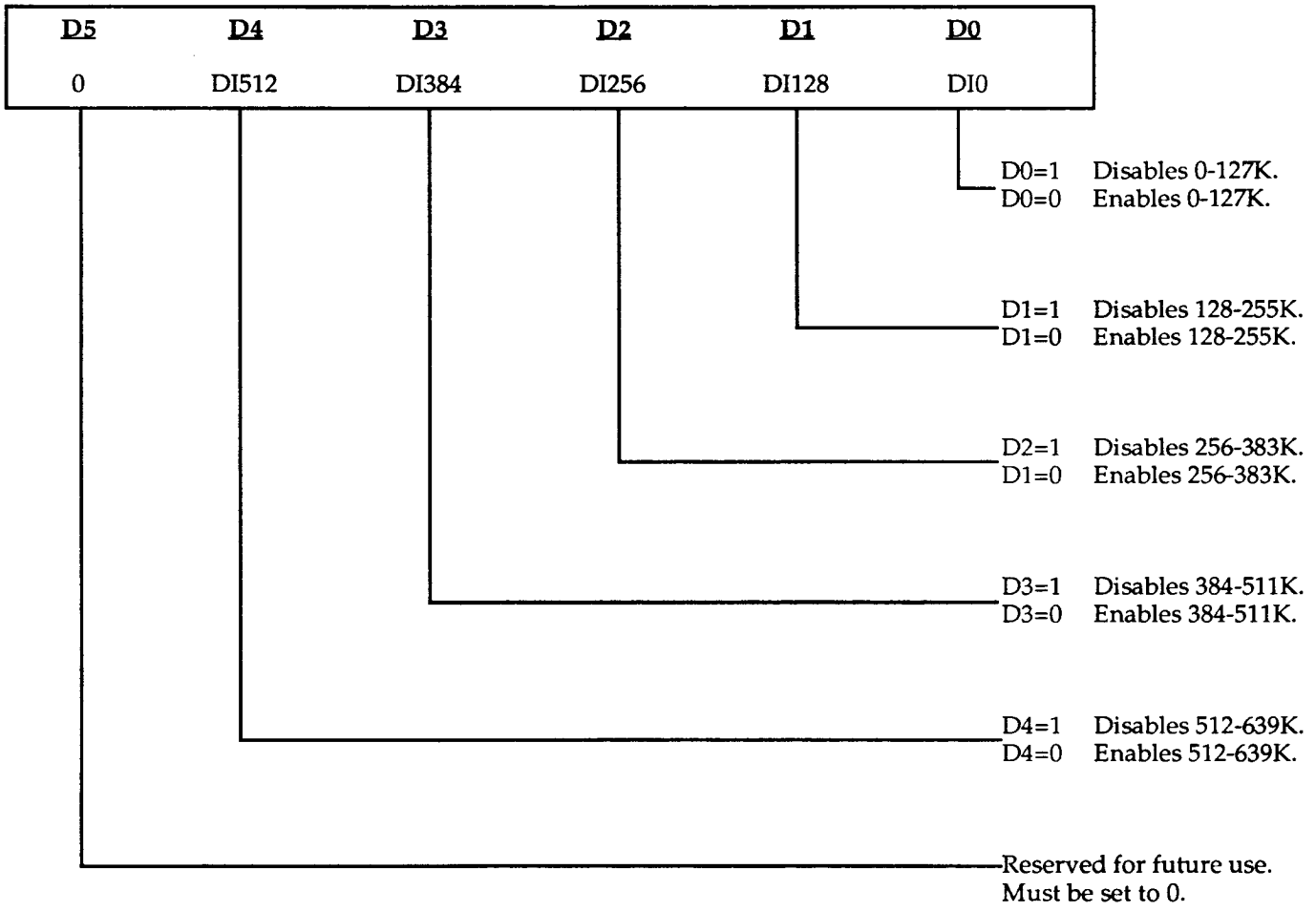
D5=0 CAS negated on T2 beginning. Default.

D5=1 CAS negated 1/2 CLK2 after T2 beginning.

DISABLE MEMORY REGISTER, INDEX 10h, R/W

Bits D4 through D0 are used to selectively disable local memory (RAM and ROM). Each bit, when set, disables its corresponding 128K range. Any, all, or none may be set/cleared. The register defaults, on power up, to 00h, memory enabled.

Register 10h



MEMORY SELECT REGISTER, INDEX 11h, R/W

The memory select register bits D3 through D0 are used to select one of 16 different RAM memory size/configurations. The configuration defaults to 256K on power up.

Register 11

D5	D4	D3	D2	D1	D0
0	0	MSB3	MSB2	MSB1	MSB0

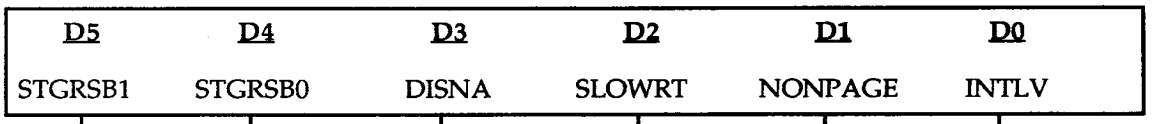
D3	D2	D1	D0	BANK0	BANK1	BANK2	BANK3	Interleave: 2-Way	Interleave: 4-Way
0	0	0	0	256K (Default)					
0	0	0	1	256K	256K			Yes	
0	0	1	0	256K	256K	256K			
0	0	1	1	256K	256K	256K	256K		Yes
0	1	0	0	256K					
0	1	0	1	256K	256K				
0	1	1	0	256K	256K	1M			
0	1	1	1	256K	256K	1M	1M		
1	0	0	0	Reserved					
1	0	0	1	Reserved					
1	0	1	0	Reserved					
1	0	1	1	Reserved					
1	1	0	0	1M					
1	1	0	1	1M	1M			Yes	
1	1	1	0	1M	1M	1M			
1	1	1	1	1M	1M	1M	1M		Yes

D5, D4 — Reserved for future use. Must be set to 0.

CONFIGURATION REGISTER #1, INDEX 12h, R/W

The configuration Register #1 is used to enable/disable interleave, page mode and next address. It may also be used to reduce by 1 the number of Read hit wait states, as well as set up refresh options.

Register 12h



Selects Interleave/Non Interleave Mode

D0=0 Non Interleave Default
D0=1 Interleave

SelectsPage Mode/Non Page Mode

D1=0 Page Mode Default
D1=1 Normal Mode

SelectsRAM Wait States for Write Hits

D2=0 Wait state 1 less than read HIT cyclesDefault
D2=1 Wait state same as specified for read HIT cycles

Enables/Disables Pipeline Mode

D3=0 Enable next address control Default
D3=1 Disable next address control

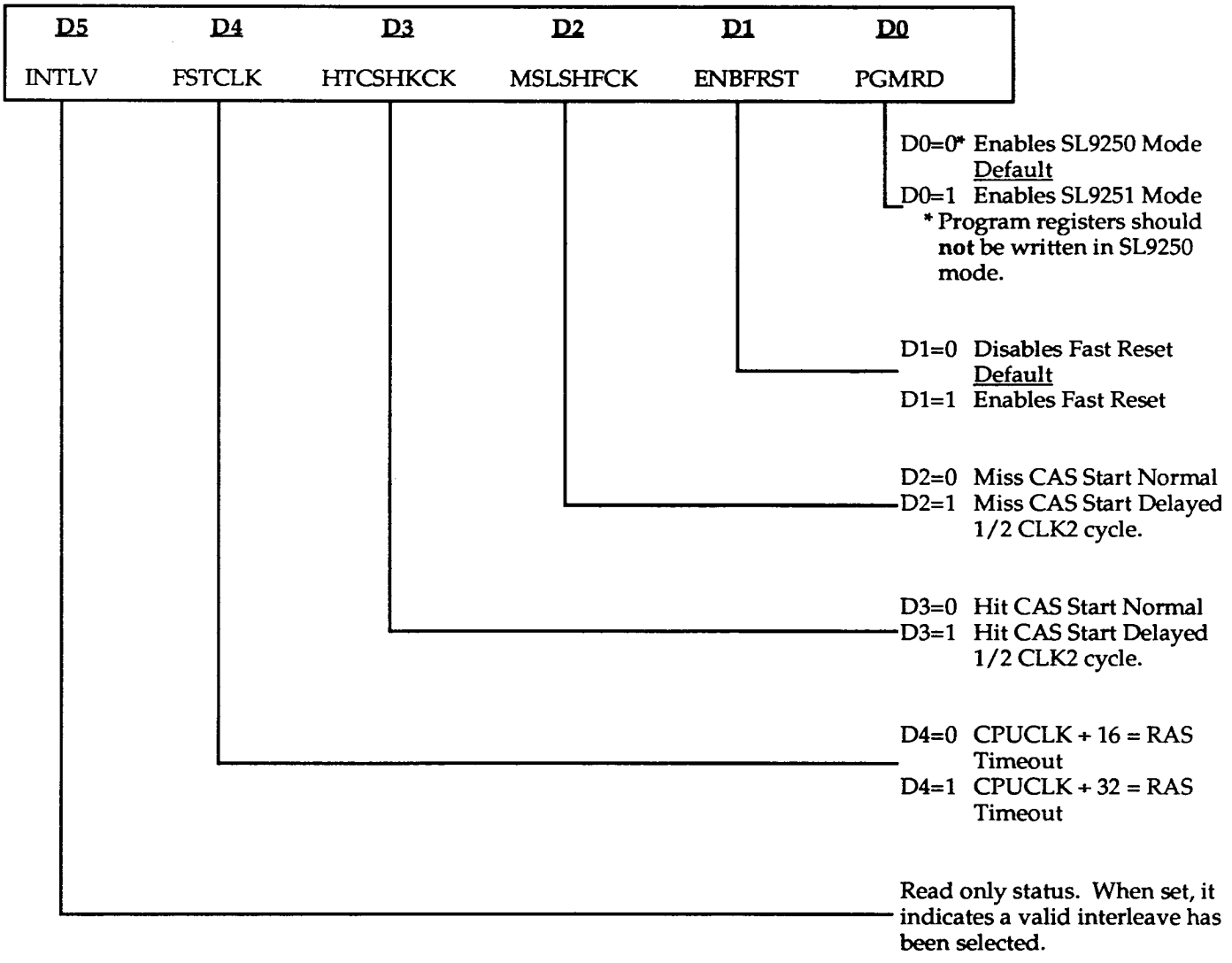
Indicates Number of Clocks To Stagger Refresh RAS's

D5	D4	
0	0	Disable Staggered Refresh
0	1	Reserved
1	0	1 CLK2
1	1	2 CLK2

CONFIGURATION REGISTER #2, INDEX 13h, R/W (Bit 5 - Read only)

The configuration Register #2 is used to select SL9251 mode of operation, enable fast reset, select CAS Hit/Miss delay, and select RAS time out Clock. Refer to Figures 5 and 6 for CAS timings.

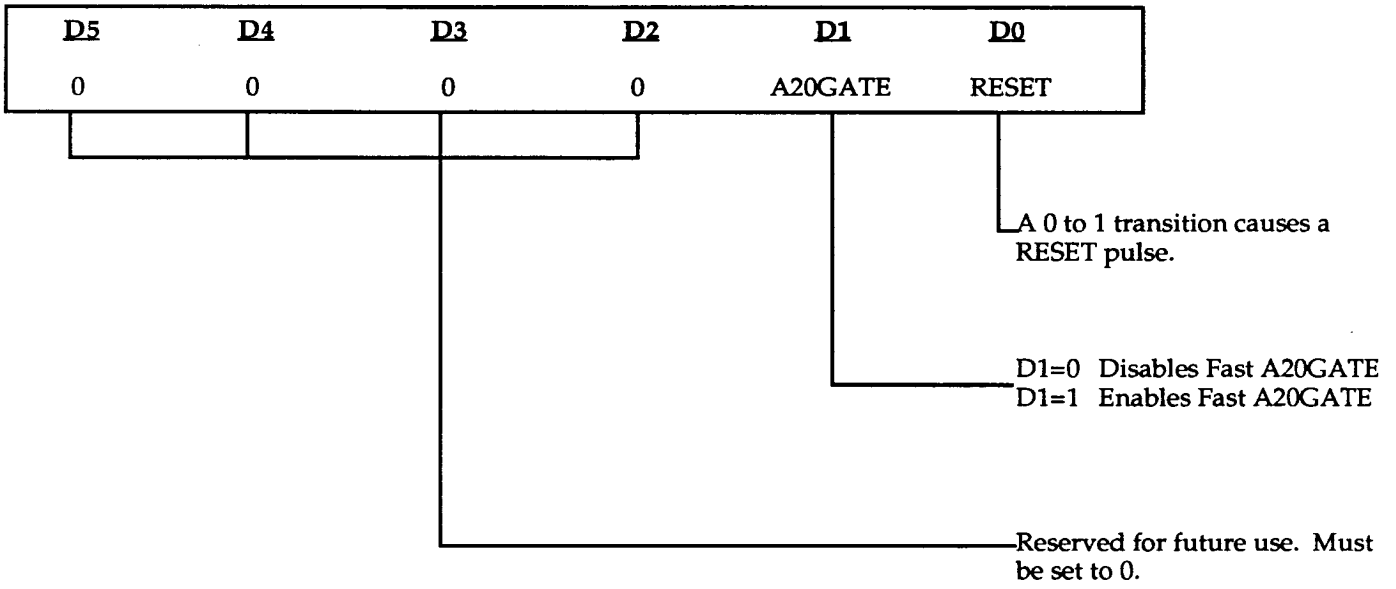
Register 13h



PORT 92 INDEX 92h, R/W

Port 92 is used to generate soft Reset and control A20GATE.

Port 92



AC TIMING DIAGRAMS SL9251

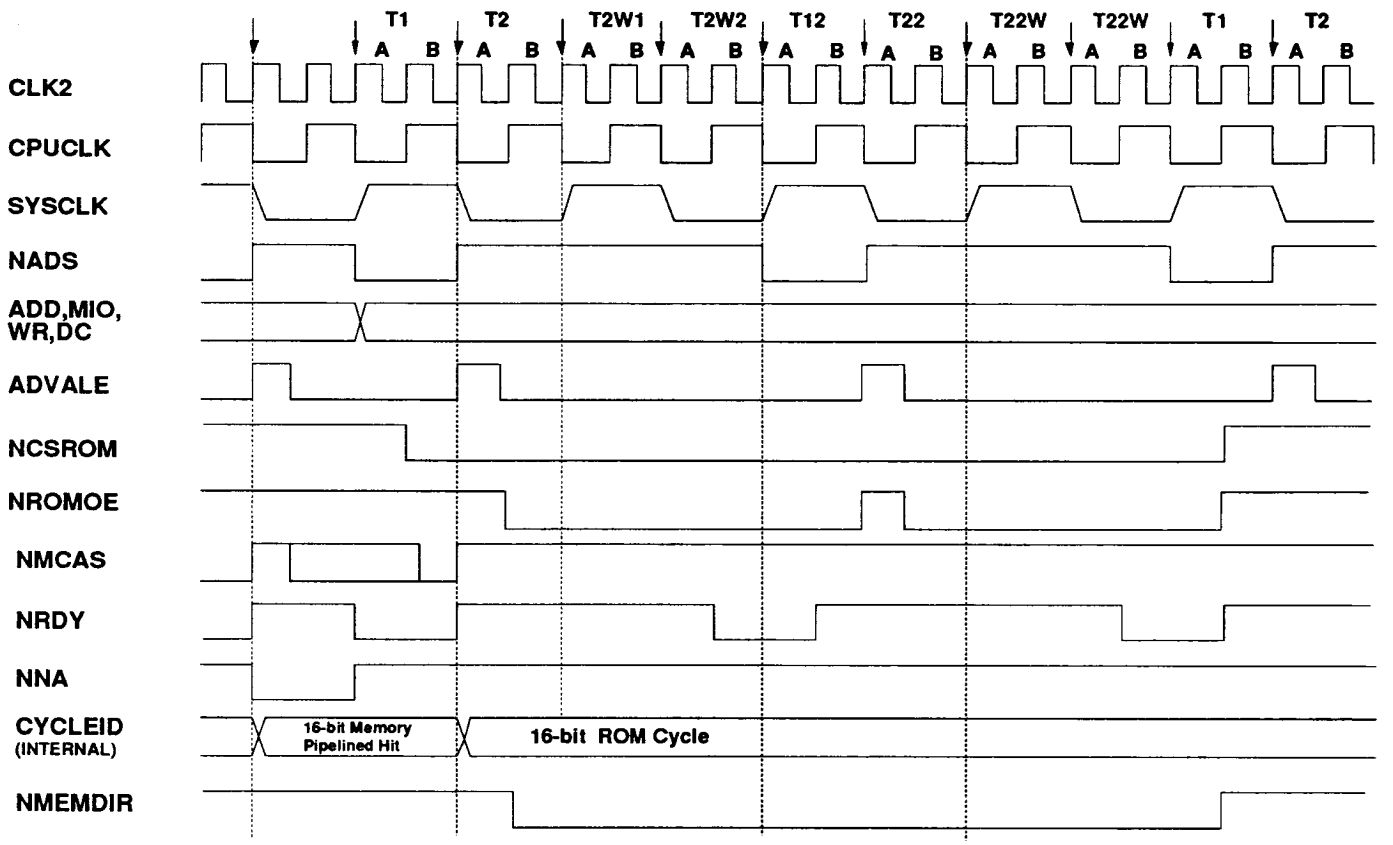


Fig. 9 Timing Diagram for BIOS ROM cycle (16-bit memory)/SL9250 and SL9251 Modes

AC TIMING DIAGRAMS SL9251

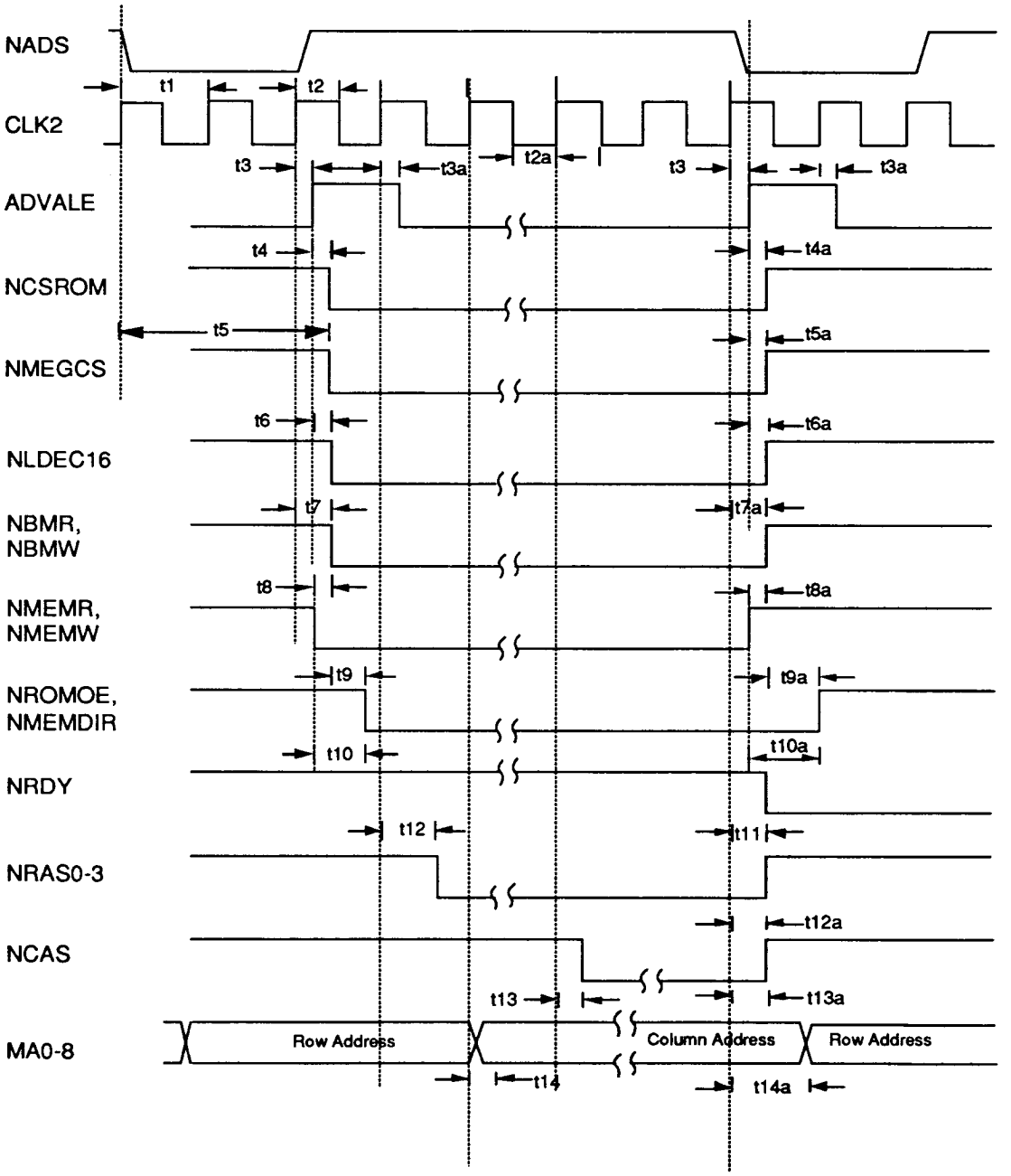


Fig. 10 Timing Spec

ABSOLUT MAXIMUM RATINGS SL9251 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current *note 2	I_{OS}	-40	+40	mA
Output Current *note 3	I_{OS}	-40	+80	mA
Output Current *note 4	I_{OS}	-60	+120	mA
Output Current *note 5	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NNA, NRDY, NROMOE, NS0, NS1, NENB245.
3. A1, A17 - A19, A21-23, CPUA20, NFSTRST.
4. MA0-MA9, LA17/NCAS10 - LA23/NCAS31, NCAS/NCAS00, NCAS01, SA17 - SA19.
5. NBMW, NRAS0 - NRAS3.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9251

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	CONDITIONS
Power Supply Current	IDDS	TBD	TBD	mA	20 MHz
Power Supply Current	IDDS	0	100	µA	Steady state
Output High Voltage *note 1	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output *note 2	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output NBMW, NRAS0-NRAS3	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output *note 3	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output A1, A17-A19, A21-23, CPUA20, NFSTRST	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output *note 4	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output NBMW, NRAS0-NRAS3	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for All Inputs	VIH	2.2		V	
Input Low Voltage for All Inputs	VIL		0.8	V	
Input Leakage Current *note 5	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current, Tri-state *note 6	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = VSS
Input Current, Pull-up *note 7	IILU	-33.5	-20.4	µA	VI = .4V
Input Current, Pull-up *note 7	IIHU	-13.5	-12.4	µA	VI = 2.4V
Input Current, Pull-down MSEL1-MSEL4/D0-D3	IILD	TBD	26	µA	VI = .4V
Input Current, Pull-down MSEL1-MSEL4/D0-D3	IIHD	14	106	µA	VI = 2.4V

NOTES:
1. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1, A1, A17-A19, A21-23, CPUA20
2. LA17/NCAS10-LA23/NCAS30, MA0-MA9, SA17-SA19, NCAS/NCAS00, NCAS01
3. ADVALE, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NMA, NRDY, NROMOE, NS0, NS1, NENB245
4. LA17/NCAS10-LA23/NCAS30, MA0-MA9, SA17-SA19, NCAS/NCAS00, NCAS01
5. A0-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, NREFRESH, RESET, WR
6. A1, A17-A19, A21-A23, CPUA20, LA17-LA23, SA17-SA19
7. WSEL1/D4, WSEL2/D5

AC CHARACTERISTICS SL9251

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNITS
t1	CLK2 Period	25	-	ns
t2	CLK2 High Duration	7	-	ns
t2a	CLK2 Low Duration	7	-	ns
t3	CLK2 to ADVALE (Low to High)	3.3	15.5	ns
t3a	CLK2 to ADVALE (High to Low)	2.9	13.3	ns
t4	ADVALE to NCSROM (Low to High)	10.8	25.4	ns
t4a	ADVALE to NCSROM (High to Low)	10.8	25.4	ns
t5	NADS to NMEGCS (Low to High)	9.9	29.4	ns
t5a	NADS to NMEGCS (High to Low)	9.9	29.4	ns
t6	ADVALE to NLDEC16 (High to Low)	2.3	8.2	ns
t6a	ADVALE to NLDEC16 (Low to High)	2.3	8.2	ns
t7	CLK2 to NBMR, NBMW (High to Low)	1.8	7.9	ns
t7a	CLK2 to NBMR, NBMW (Low to High)	1.2	7.1	ns
t8	NMEMR, NMEMW to NBMR, NBMW (High to Low)	1.1	5.3	ns
t8a	NMEMR,NMEMW to NBMR, NBMW (Low to High)	1.5	6.4	ns
t9	NBMR to NROMOE (High to Low)	0.4	1.4	ns
t9a	NBMR to NROMOE (Low to High)	0.4	1.2	ns
t10	NMEMR to NROMOE (High to Low)	4.0	16.2	ns
t10a	NMEMR to NROMOE (Low to High)	4.0	16.2	ns
t11	CLK2 to NRDY	1.8	7.2	ns
t12	CLK2 to NRAS0-NRAS3 (High to Low)	5.6	26.2	ns
t12a	CLK2 to NRAS0-NRAS3 (Low to High)	6.5	29.2	ns
t13	CLK2 to NCAS (High to Low)	5.4	24.1	ns
t13a	CLK2 to NCAS (Low to High)	4.2	22.8	ns
t14	CLK2 to MA0-MA8 Delay	4.0	16.7	ns

(TA = 25 ° C, VDD = V1 = 5V, fo = 1MHz)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	NOTES
Input Pin Capacitance	C_{IN}	---	16	Pf	note 1
Input Pin Capacitance	C_{IN}	---	TBD	Pf	note 2
Output Pin Capacitance	C_{OUT}	---	16	Pf	note 3
Output Pin Capacitance	C_{OUT}	---	18	Pf	note 4
I/O Pin Capacitance	$C_{I/O}$	---	16	Pf	note 5
I/O Pin Capacitance	$C_{I/O}$	---	23	Pf	note 6

NOTES:
1. A2-A16, A20GATE, CLK2, CLK8042, CPUCLK, DC, HLDA, MIO, NADS, NMASTER, NMEMR, NMEMW, REFRESH, RESET, WR
2. NSHADOW, MSEL1-MSEL4, NPAG4K, TEST 3, TEST 4, WSEL1, WSEL2
3. ADVALE, ADD20, MA0-MA9, MA81, NBMR, NCSROM, NLDEC16, NMEGCS, NMEMDIR, NNA, NRDY, NRAS, NROMOE, NS0, NS1
4. NBMW, NRAS0-NRAS3
5. A1, A17-A19, A21-A23, CPUA20, LA17-LA23, SA17-SA19
6. NBMW, NRAS0-NRAS3

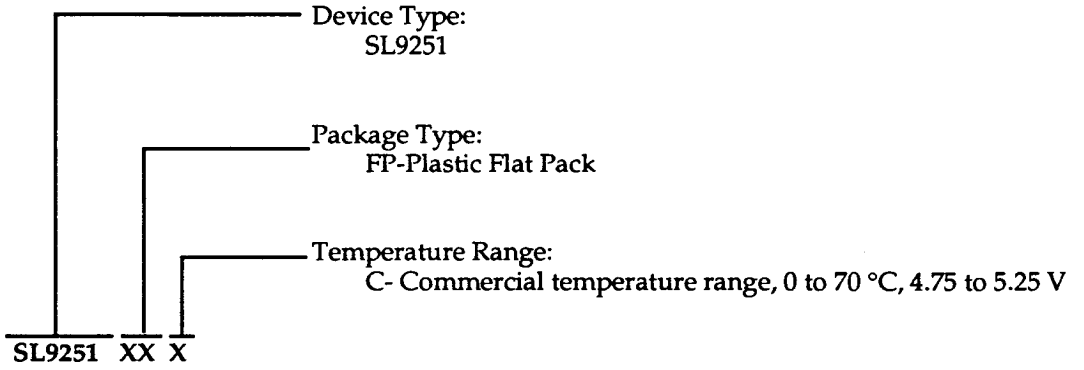
The FlexSet™ PC/AT
80386SX Page Interleave Memory Controller
SL9251

PRELIMINARY

PACKAGE INFORMATION

100 Pin Flat Pack

ORDERING INFORMATION



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April 13, 1990

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