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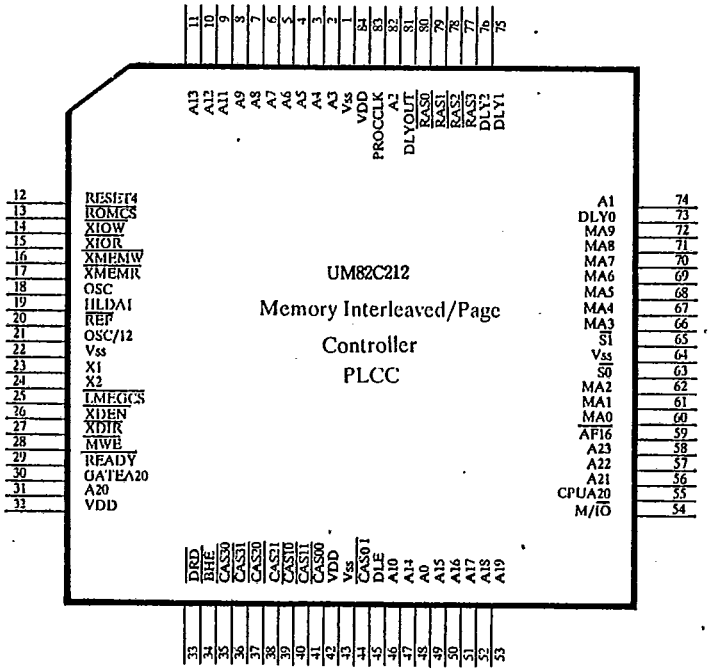
2. UM82C212 MEMORY CONTROLLER

The UM82C212 performs the memory control functions in the UM82C210 system. Several distinquished features are integrated in the UM82C212 that makes the UM82C210 system become one of the most advan- ced 80286 AT compatible systems available. First of all, the UM82C212 provides Page Mode to access the memory with interleaved memory banks. By using this Page-Interleaved scheme, the UM82C212 provides higher performance over conventional DRAM accessing schemes. As a result, the UM82C212 can support a 16 Mhz system with 100 ns DRAM by the use of the Page-Interleaved mode.

The UM82C212 also supports up to 8 Mbytes of on board memory. Also, the UM82C212 will automatically re-map the RAM resident in 640 Kbytes to 1 Mbytes area to the top of the 1 Mbyte address space. In order to access the memory resident beyond the 1 Mbyte address space, the UM82C212 provides address translation logic to support the LIM-EMS 4.0. The shadow RAM feature is also integrated into the UM82C212 for efficient and fast BIOS execution. The UM82C212 also provides OS/2 optimization that allows faster switching between the real mode and protected mode. A staggered DRAM refresh scheme is also included to reduce power supply noise.



2.1 Memory Array Configuration

The memory configuration required by the 80286 PC/AT systems is organized as banks with widths of 18 bits. Sixteen bits of them are used as data words split into high and low order bytes. The other 2 bits are used as parity bits, one for each byte. Since the UM82C212 also provides conventional memory accessing, the minimum memory cofiguration can be a single bank for non-interleaved mode. However, at least two identical memory banks are required for the operation of the Interleaved mode. Table 2.1 shows the commonly used memory configurations.

	DRAM Type				Total Memory	EMS Range
	Bank0	Bank1	Bank2	Bank3		
1	256K	0	0	0	512kb	0
2	1M	0	0	0	2Mb	1Mb to 2Mb
3	256K	256K	0	0	1Mb	1Mb to 1.384Mb
4	1M	1M	0	0	4Mb	1Mb to 4Mb
5	256K	256K	256K	256K	2Mb	1Mb to 2Mb
6	256K	256K	1M	1M	5Mb	1Mb to 5Mb
7	1M	1M	1M	1M	8Mb	1Mb to 8Mb

Table 2.1 Commonly Used Memory Configurations

As mentioned above, the possible memory configurations for Page- Interleaved mode are No. 3, 4, 5, 6, and 7 in Table 2.1.

2.2 Page/Interleaved Operation

Besides conventional memory accessing, there are several different accessing schemes available that make the memory access time much shorter than the access time of the conventional mode. Three most commonly used methods are Interleaved Mode, Page Mode, and Page-Interleaved Mode.

Basically, the Page-Interleaved Mode takes the advantages by combining the operations of Interleaved Mode and Page Mode. It allows the memory to be interleaved at page boundary instead of 2 bytes boundary. Figure 2.1 shows the sequence diagram of the Page-Interleaved operation.

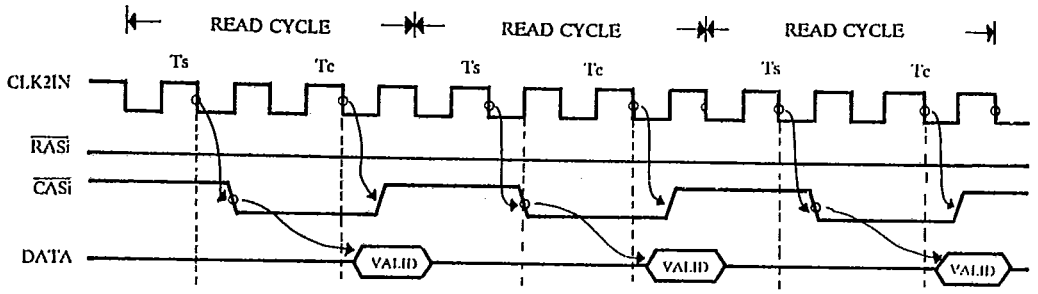


Figure 2.1 Page Mode Operation (Read Cycle)

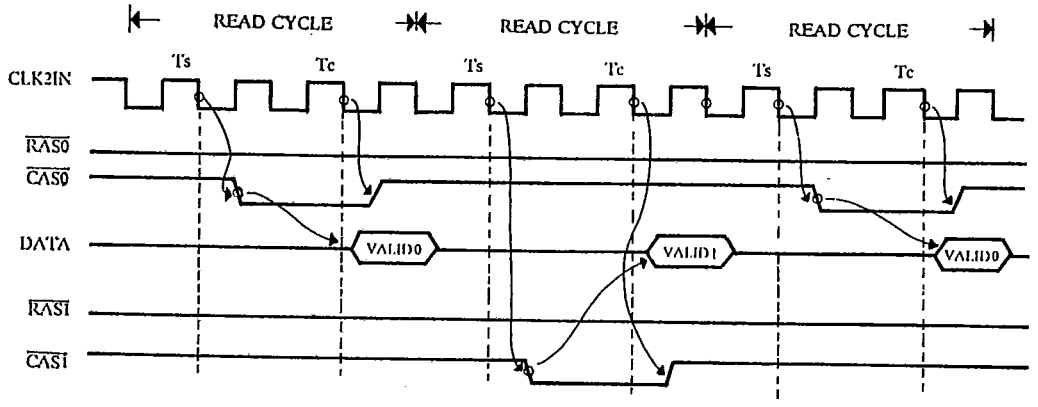


Figure 2.2 Page-Interleaved Mode Operation (Read Cycle)

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2.3 Enhanced Functions

Besides the standard PC/AT functions, several new functions have been included in the UM82C210 chip set. Those enhanced functions are OS/2 operation optimization, memory relocation, shadow RAM, EMS, and etc.

2.3.1 OS/2 Operation Optimization

In order to switch CPU into protected mode for standard PC/AT architectures, the CPU has to issue two commands to the keyboard controller to reset the CPU and to activate GATEA20. The UM82C210 provides another method to handle the mode switching for OS/2 operation optimization. UM82C210 uses two I/O write operations; the CPU will be reset and GATEA20 will be enabled. Since this mrthod involves two I/O writes only, it makes the mode switching much faster.

2.3.2 Memory Relocation

Normally, the memory space from address 640K to 1M is reserved for EPROM use. However, if the system is equipped with 1 Mbyte DRAM, the memory with the addresses higher than 640K has to be relocated in order not to conflict with the EPROM addresses. The UM82C212 provides this kind of mapping that DRAM addresses from 640K to 1M will be translated to new addresses from 1M to 1.384M.

2.3.3 Shadow RAM

PC/AT systems to item execute BIOS codes. For the purpose of efficiency, it is preferable to execute BIOS codes through the DRAM accesses rather than through slower EPROM accesses. The UM82C212 provides the shadow RAM feature that allows the system to copy the BIOS codes from the EPROMs to the DRAMs with the same physical addresses and disable the EPROMs. This feature improves the performance of BIOS call intensive application programs significantly.

2.3.4 Expanded Memory System (EMS)

Due to the limitation of the DOS, the memory space with addresses higher than 1M can not be accessed in the real mode of the 80286 CPU. However, the EMS is a memory mapping scheme that provides a method for the system to access the memory beyond 1 Mbyte address. The EMS is used to map a 64 Kbyte block of memory within the area C0000H-F0000H to anywhere in the 1 Mbyte to 8 Mbyte area. This 64 Kbyte block is divided into four 16 Kbyte pages. Each 16 Kbyte segment can be mapped to anywhere independently through the translation table. The UM82C212 provides all the necessary logic with the translation table for the EMS operation.

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2.4 Configuration Registers

There are twelve 8-bit registers, R21-R2C provided in the UM82C212 for configuration. In order to reduce the number of I/O ports required to access all the registers used in the UM82C210 chip set, the index access scheme is used. To access a particular register, the index address is placed at address port and the data is located at data port.

R21 : (Index address 64H)

Bits	Function
0-4	Reserved.
5,6	Revision number.
7	Chip identifier.

R22 : (Index address 65H)

Bits	Function
0	ROM disabled at F0000H-FFFFFH.
1	ROM disabled at E0000H-EFFFFH.
2	ROM disabled at D0000H-DFFFFH.
3	ROM disabled at C0000H-CFFFFH.
4	Write protection. Shadow RAM at F0000H-FFFFFH.
5	Write protection. Shadow RAM at E0000H-EFFFFH.
6	Write protection. Shadow RAM at D0000H-DFFFFH.
7	Write protection. Shadow RAM at C0000H-CFFFFH.

R23 : (Index address 66H)

Bits	Function
0-6	Reserved.
7	Enable RAM on system board at 80000H-9FFFFH.

R24 : (Index address 67H)

Bits	Function
0	Enable Shadow RAM at B0000H-B3FFFH.
1	Enable Shadow RAM at B4000H-B7FFFH.
2	Enable Shadow RAM at B8000H-BBFFFH.
3	Enable Shadow RAM at BC000H-BFFFFH.
4	Enable Shadow RAM at A0000H-A3FFFH.
5	Enable Shadow RAM at A4000H-A7FFFH.
6	Enable Shadow RAM at A8000H-ABFFFH.
7	Enable Shadow RAM at AC000H-AFFFFH.

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R25 : (Index address 68H)

Bits	Function
0	Enable Shadow RAM at C0000H-C3FFFH.
1	Enable Shadow RAM at C4000H-C7FFFH.
2	Enable Shadow RAM at C8000H-CBFFFH.
3	Enable Shadow RAM at CC000H-CFFFFH.
4	Enable Shadow RAM at D0000H-D3FFFH.
5	Enable Shadow RAM at D4000H-D7FFFH.
6	Enable Shadow RAM at D8000H-DBFFFH.
7	Enable Shadow RAM at DC000H-DFFFFH.

R26 : (Index address 69H)

Bits	Function
0	Enable Shadow RAM at E0000H-E3FFFH.
1	Enable Shadow RAM at E4000H-E7FFFH.
2	Enable Shadow RAM at E8000H-EBFFFH.
3	Enable Shadow RAM at EC000H-EFFFFH.
4	Enable Shadow RAM at F0000H-F3FFFH.
5	Enable Shadow RAM at F4000H-F7FFFH.
6	Enable Shadow RAM at F8000H-FBFFFH.
7	Enable Shadow RAM at FC000H-FFFFFH.

R27 : (Index address 6AH)

Bits	Function
0-4	Reserved.
5	Enable two banks of memory.
6,7	Type of DRAM : 0 0 : Disabled 1 0 : 256K and 64K bit DRAMs used. 0 1 : 256K bit DRAMs used. 1 1 : 1M bit DRAMs used

R28 : (Index address 6BH)

Bits	Function
0,1	ROM access wait state.
2,3	EMS memory access wait states.
4	EMS enable.
5	RAM access wait states.
6	RAM relocation (640K-1M).
7	Page-Interleaved mode enable.

R29 : (Index address 6CH)

Bits	Function
0-3	Reserved.
4	2-way/4-way page interleaved selection.
5	Number of local RAM banks used.
6,7	Local DRAM type : 0 0 : none. 1 0 : Reserved. 0 1 : 256 Kbit. 1 1 : 1 Mbit.

R2A : (Index address 6DH)

Bits	Function
0-3	EMS page register I/O base address. 0 0 0 0 : 208H/209H 1 0 0 0 : 218H/219H 1 0 1 0 : 258H/259H 0 1 1 0 : 268H/269H 0 1 0 1 : 2A8H/2A9H 1 1 0 1 : 2B8H/2B9H 0 1 1 1 : 2E8H/2E9H
4-7	Expanded memory base address. 0 0 0 0 : C0000H,C4000H,C8000H,CC000 1 0 0 0 : C4000H,C8000H,CC000H,D0000 0 1 0 0 : C8000H,CC000H,D0000H,D4000 1 1 0 0 : CC000H,D0000H,D4000H,D8000 0 1 0 0 : D0000H,D4000H,D8000H,DC000 1 0 1 0 : D4000H,D8000H,DC000H,E0000 0 1 1 0 : D8000H,DC000H,E0000H,E4000 1 1 1 0 : DC000H,E0000H,E4000H,E8000 0 0 0 1 : E0000H,E4000H,E8000H,EC000

R2B : (Index address 6EH)

Bits	Function
0,1	EMS block for page 3 : Bit1 Bit0 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte
2,3	EMS block for page 2 : Bit3 Bit2 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte
4,5	EMS block for page 1 : Bit5 Bit4 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte
6,7	EMS block for page 0 : Bit7 Bit6 EMS memory block (A22 A21) 0 0 : 0 - 2 Mbyte 0 1 : 2 - 4 Mbyte 1 0 : 4 - 6 Mbyte 1 1 : 6 - 8 Mbyte

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R2C : (Index address 6FH)

Bits	Function
0	Reserved.
1	CPUA20 enable.
2	RAS time-out enable.
3,4	Reserved.
5-7	Size of EMS memory : 0 0 0 : < 1 Mbyte 1 0 0 : 1 Mbyte 0 1 0 : 2 Mbytes 1 1 0 : 3 Mbytes 0 0 1 : 4 Mbytes 1 0 1 : 5 Mbytes 0 1 1 : 6 Mbytes 1 1 1 : 7 Mbytes