SL82C472 BUS CONTROLLER

- Integrated 32/16/8 bit data bus bridge
- Bus translation among ED(MD), SD and XD
- Data conversion
- Byte Enable translation
- Generates EISA signals for ISA Masters
- Generates ISA Signals for EISA Masters
- Parity generation and detection
- Enhanced EISA NMI Logic
- Enhanced 8259 x 2 interrupt controller
- Enhanced 8254 x 2 timer controller
- Clock generation for the 8254 Timers
- On-board reset generation
- High drive buffer for EISA/ISA bus interface
- CMOS 160-pin PQFP package

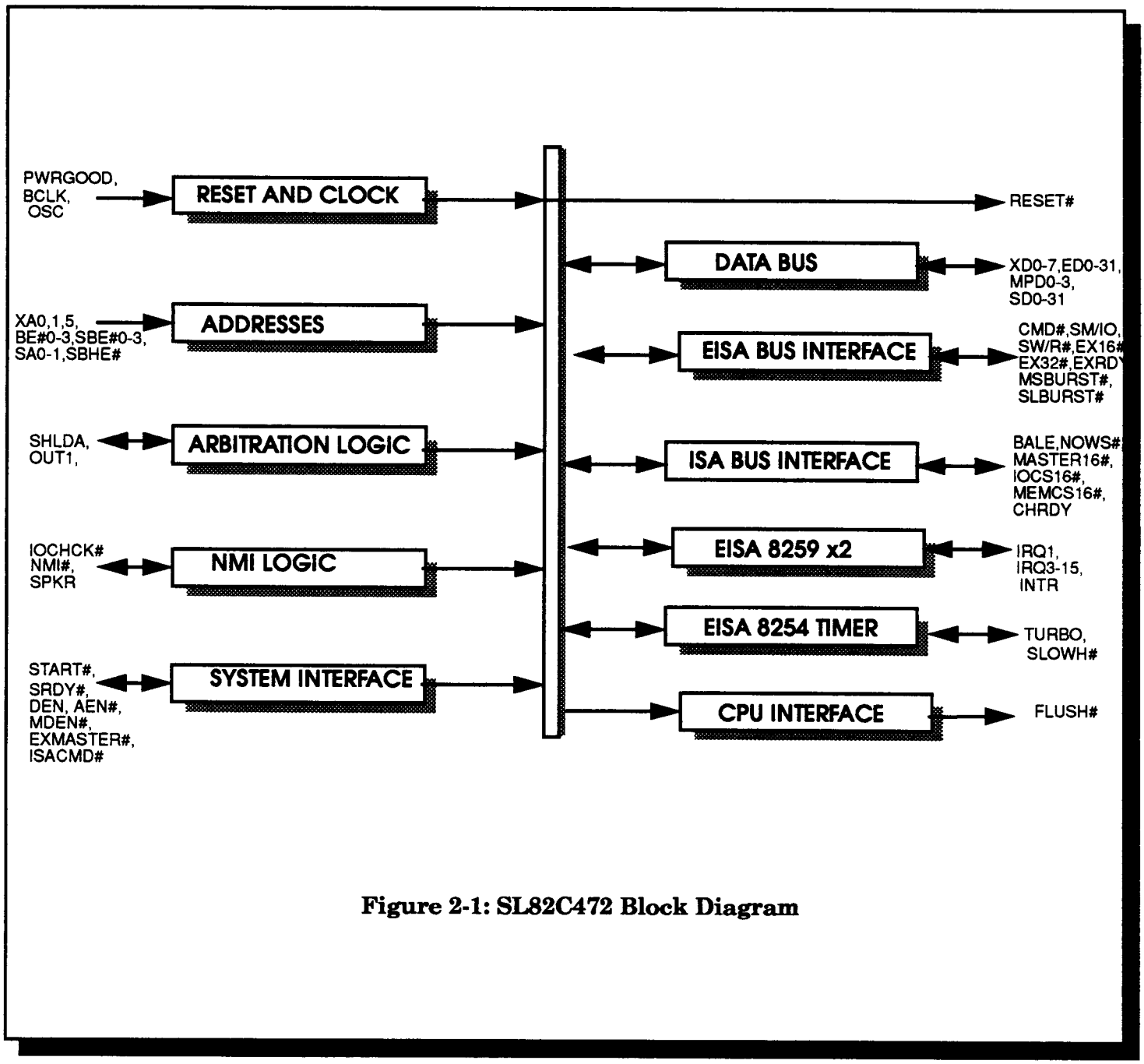


Figure 2-1: SL82C472 Block Diagram

2.1 Functional Description

2.1.1 Clock and Reset Logic

The SL82C472 divides the buffered CLKOUT from the SL82C471 to generate the BCLK for the EISA bus. The programmable divisor can be 2, 2.5, 3, 4, 5, or 6. The BCLK is synchronous with the START# internally. An external 14.31818 MHz clock is fed to the OSC input to generate the OSC/12 for internal timer counters.

The PWRGOOD signal is generated from the power supply to generate RESET# for the whole system. RESET# output resets the chip set and the keyboard controller.

2.1.2 EISA/ISA Bus State Machine

The SL82C472 provides the control signal translation between the CPU, EISA/ISA, and DMA masters and slaves. The SL82C472 translates EISA to ISA, ISA to EISA, and the CPU to EISA or ISA.

The SL82C472 monitors signals: A. SHLDA, B. EXMASTER#, C. MASTER16#, and D. MSBURST# to determine the Bus Master type and size:

A	B	C	D	Size	Master
0	1	1	1	32	CPU
1	0	1	1	32	EISA
1	0	1	0	32	EISA (Burst)
1	0	0	1	16	EISA
1	0	0	0	16	EISA (Burst)
1	1	0	1	16	ISA
1	1	1	1	All	DMA
1	1	1	0	All	DMA (Burst)

The SL82C472 monitors signals: A. EX32#, B. EX16#, C. MEMCS16#, and IOCS16# to determine the bus slave type and size:

A	B	C	D	Size	Slave
0	-	-	-	32	EISA
1	0	-	-	16	EISA
1	1	0	-	16	ISA Memory
1	1	-	0	16	ISA I/O
1	1	-	1	8	ISA Memory
1	1	1	-	8	ISA I/O

2.1.3 Data Bus Control

The SL82C472 controls the direction of the data bus flow between the ED, SD and XD buses according to the cycle translation.

The ED is the 32-bit extended (buffered) CPU data bus, which also supports the 32-bit DRAM data bus. The SD is a 32-bit EISA data bus that can drive the slot directly without external buffers. The XD is an 8 bit bus for on-board peripherals such as the real time clock, the keyboard controller and the BIOS EPROM if the 8-bit option is selected. The SL82C471, SL82C472 and SL82C473 also exchange information through the XD bus. Data assembly and disassembly are performed when the sizes of the source and destination busses do not match. Multi-cycle transfer is detected and performed automatically by the chip set whenever necessary. For multi-cycle CPU read operations, the data read in the earlier cycles are latched for CPU access at the completion of the last cycle.

The data bus is quiet by default to save power consumption and reduce switching noise. The output is enabled only when data is required. Whenever necessary, the output is turned on after the internal data is settled. Early output enabling is only used for speed sensitive paths. The driving requirement of these paths is usually small.

2.1.4 Byte Enable Translations

The SL82C472 translates BE#0-3, SBE#0-3, SA0, SA1 and SBHE# between ISA or EISA and CPU:

In CPU cycles, the BE#0-3 are translated to SBE#0-3 for driving the EISA bus and SBHE#, SA1, and SA0 for driving the ISA Bus. In EISA cycles SBE#0-3 are converted to SA1, SA0 and SBHE# for the ISA Bus. In ISA Master and DMA cycles, SA1,0 and SBHE# are converted to SBE#0-3.

ISA to CPU or EISA Byte Enable Translations:

Input Signals			Output Signals
SBHE#	SA1	SA0	SBE#0-3 or BE#0-3
0	0	0	1100
0	0	1	1101
0	1	0	0011
0	1	1	0111
1	0	0	1110
1	1	0	1011

CPU or EISA to ISA Byte Enable Translations:

Input Signals	Output Signals		
SBE#0-3 or BE#0-3	SBHE#	SA1	SA0
1110	1	0	0
1101	0	0	1
1100	0	0	0
1011	1	1	0
1001	0	0	1
1000	0	0	0
0111	0	1	1
0011	0	1	0
0001	0	0	1
0000	0	0	0

2.1.5 EISA Master Back-off

When there is a mismatch in the EISA master transfer, the EISA master must back-off the bus to allow the SL82C472 to perform the data bus translation. The SL82C471 will drive the EX16# and EX32# active at the end of data transfer to return the cycle control to the bus master.

2.1.6 Parity Generation and Detection

The SL82C472 provides the logic required to generate parity bits for each byte of data during the DRAM write cycles. It also detects and generates parity error during the DRAM read cycles.

The memory data is internally latched by the rising edge of the MDEN# signal during the local DRAM read cycles. This action allows early termination of CAS signals for the most flexible DRAM control. Tracking with the delay due to parity calculation and parity error detection, the DEN or SRDY# signals are used to latch the parity error signal during local DRAM read cycles.

2.1.7 EISA Interrupt Controller

Two enhanced 8259 interrupt controllers which conform to the EISA standard are included in the SL82C472. Each controller handles eight interrupt channels, and each interrupt can be set as edge sensitive or level sensitive. The interrupt controller can be commanded to operate in various modes. The default modes are: 80x86 mode, Edge-sensitive, Normal End-of-Interrupt, Non buffered mode, Special Fully Nested Mode disabled, Fixed priority and Cascade mode.

In the default mode, the two interrupt controllers are internally cascaded to handle 15 interrupt channels. Furthermore, IRQ0 is internally connected to the OUT0 of the 8254 counter/timer 1 and is not available as an external input. The IRQ8 is an active low signal, which is connected to the RTC interrupt. All external IRQ lines are internally pulled up to eliminate noise on the request pins that are not connected.

The following I/O map lists the 8 bits I/O port address map for the interrupt registers:

Interrupts	I/O address	Register
IRQ<7:0>	0020h	Control Register I
IRQ<7:0>	0021h	Mask Register I
IRQ<7:0>	04D0h	Edge/Level Register I
IRQ<15:8>	00A0h	Control Register II
IRQ<15:8>	00A1h	Mask Register II
IRQ<15:8>	04D1h	Edge/Level Register II

2.1.8 NMI Logic

The SL82C472 implements the NMI ports defined by EISA specification. The following I/O map lists the 8-bit port addresses used for NMI registers (Port 461 and 462 and BUS Time-out function are implemented in the SL82C473):

NMI registers	I/O address
NMI Status register (R/W)	0061h
NMI Enable register(W)	0070h
Extended NMI register(R/W)	0461h
Software NMI register(W)	0462h

Port 61 logic contains REFRESH# input checking, NMI status and control, speaker (8254 counter 2) output checking and muting. Port 461 provides additional NMI status and control. The source of an interrupt includes the following conditions:

- ❑ Parity from the system memory
- ❑ ISA/EISA system board asserts IOCHK#
- ❑ Fail -Safe Timer Time-out
- ❑ BUS Time-out
- ❑ Software Generated NMI

The write only Port 462 is the software NMI generation port. A write to this port generates an NMI. Generation of NMI can be globally enabled and disabled by clearing and setting the register bit 7 of IO port 70H.

2.1.9 EISA 8254 Timer/Counter Controller

Two 8254 equivalent counter/timer are included in the SL82C472 to comply to the EISA specification. Timer 1 contains three counters. Timer 2 contains two counters. The clocks for the five timer counters are generated from the 14.31818 MHz clock or the BCLK. The following I/O map shows the addresses for the five interval timer counters (The Fail-Safe Timer counter is implemented in the SL82C473):

Interval Timer registers	I/O address
Timer 1, System Timer (counter 0)	040h
Timer 1, Refresh Request (counter 1)	041h
Timer 1, Speaker Tone (counter 2)	042h
Timer 1, Control word	043h
Timer2, Fail-Safe Timer (counter 0)	048h
Timer 2, Reserved	049h
Timer 2, CPU speed Control (Counter 2)	04Ah
Timer 2, Control Word	04Bh

The output of Timer 1, counter 0, is connected to the IRQ0 input of the interrupt controllers. The clock for this counter is 1.193 MHz. The gate input of counter 0 is always enabled. It provides a system timer interrupt for system timing functions, such as: time-of-day, diskette time-out, etc.

The output of Timer 1, counter 1, is connected to the output pin OUT1 to the arbitration unit inside the SL82C473 to request a DRAM refresh. The clock for this counter is 1.193 MHz. The gate input of this counter is always enabled.

The output of Timer 1, counter 2, generates the tone for the speaker. The clock for this counter is 1.193 MHz. The input gate of this counter can be negated or asserted by programming bit 0 of Port 61.

The output of Timer 2, counter 0, generates the fail-safe NMI interrupt to prevent the system from locking up. Fail-safe NMI can be disabled or enabled by programming bit 2 of Port 461. This counter bears a 298.3 KHz clock and is always enabled.

The output of Timer 2, counter 2, is tied to the SLOWH# output pin of the SL82C472 and then is connected to the SLOW# input pin of the SL82C473 to generate a HOLD request to slow down the CPU speed for compatible mode operation. The clock source for this counter is BCLK. This counter is defaulted to an active low one-shot mode and is triggered by the refresh request signal from Timer 1, counter 2. After the initial count value is loaded, the counter output activates SLOWH# for a period equal to the product of BCLK and the initial count value each time Timer 1, counter 2, asserts Refresh Request.

2.2 SL82C472 Signal Description

Signal Name	Pin Number	TYPE	Signal Description
CLOCK			
CLKOUT	33	I	CPU CLOCK: input from the CLKOUT of the SL82C471.
BCLK	21	O	EISA BUS CLOCK: to drive the EISA bus and the SL82C471 and SL82C473. This pin has 24mA drive capability.
OSC	59	I	OSC CLOCK: input from an external oscillator (or crystal) of frequency 14.318 MHz to drive the internal timer channels.
RESET			
PWRGOOD	35	I	SYSTEM POWER GOOD: input generated from the power supply.
RESET#	34	O	ON BOARD RESET: to reset the chip set and the keyboard controller.
CPU INTERFACE			
FLUSH#	19	O	CACHE FLUSH: output to the 486 CPU to invalidate its entire internal cache. This signal is asserted for only one CPU cycle.
SYSTEM INTERFACE			
START#	23	B	START CYCLE: provides timing control at the start of a system cycle. START# is input from the SL82C471 during CPU and refresh cycles and from the SL82C473 during ISA master cycles and from the EISA bus during EISA master cycles. START# is output when a data bus translation is performed. When the size of the master and the slave is a mismatch, this pin switches from input to output at the end of the first START#. It switches back to the input mode at the end of the last CMD#. This pin has 24mA drive capability.
SRDY#	24	B	SYSTEM READY: output to or input from the SL82C471 to indicate that the current EISA/ISA cycle is complete. This signal is activated for one BCLK period.
MDEN#	25	I	MEMORY DATA ENABLE: input from the SL82C471 to indicate that the cache or on-board DRAM is accessed.
DEN	102	I	DATA OUTPUT ENABLE: input from the SL82C471 to control the output driver to the CPU data bus during CPU read cycles. The output driver is turned off during on-board DRAM read cycles and the trailing edge of DEN signifies the latching of parity.

AEN#	114	I	ADDRESS ENABLE: input from the SL82C473 to indicate a DMA cycle is in progress.
EXMASTER#	8	I	EISA MASTER: input from the SL82C473 to indicate if the current bus master is an EISA master. This signal along with MASTER16# and AEN# is used to distinguish between 32-bit EISA, 16-bit EISA, 16-bit ISA and DMA cycles.
ISACMD#	18	B	ISA COMMAND: output to the SL82C473 during CPU and EISA master cycles to initiate ISA commands. ISACMD is input from the SL82C473 during ISA master cycles to initiate CMD#.

EISA BUS INTERFACE

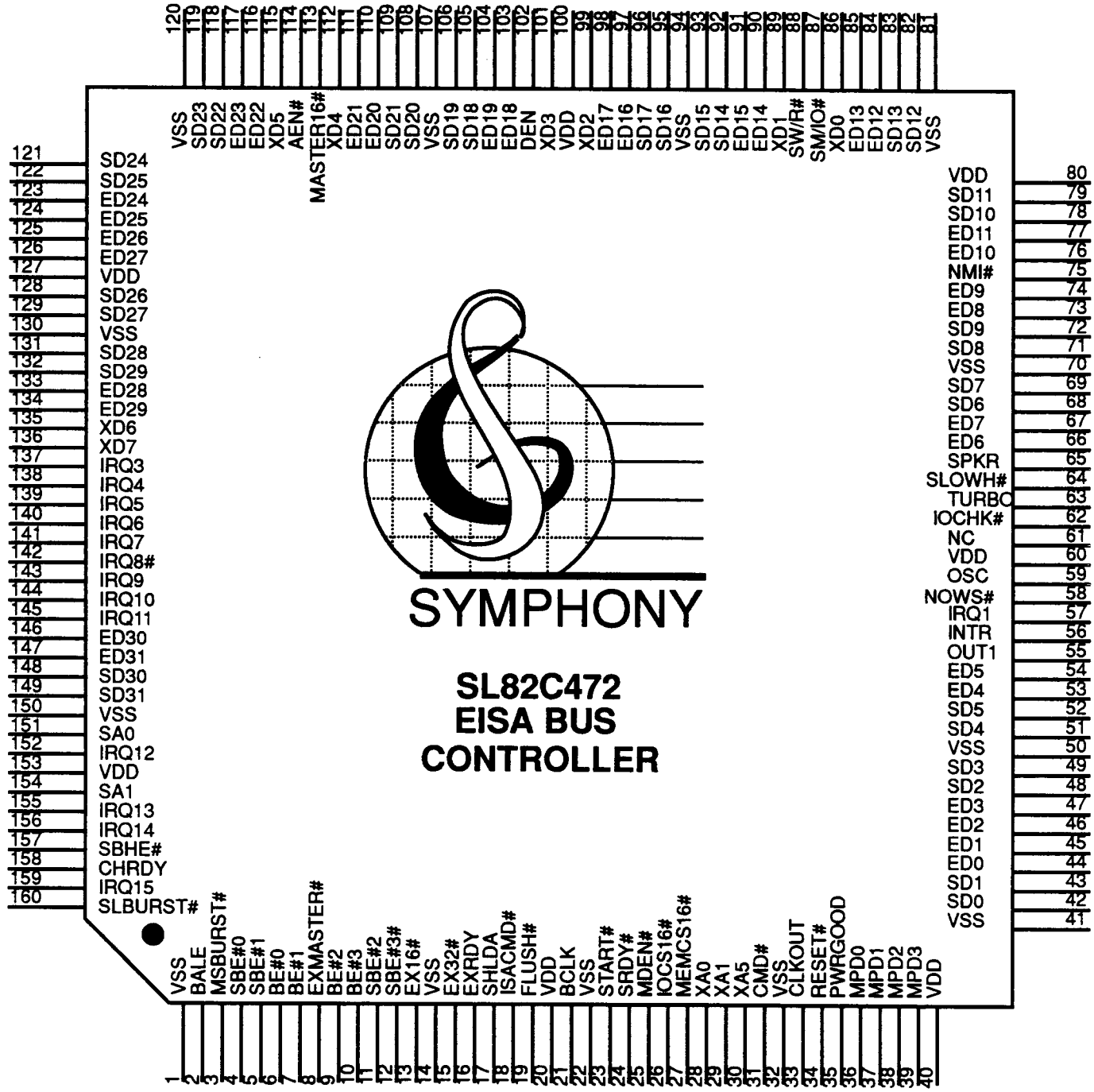
CMD#	31	O	COMMAND: output to the EISA bus and the chip set to initiate an EISA bus cycle. This pin has 24mA drive capability.
SM/IO#	87	I	SYSTEM MEMORY/IO: input from the SL82C471 during CPU/Refresh cycles, from the SL82C473 during DMA and ISA master cycles and from the EISA bus during EISA master cycles. High indicates a memory cycle and low indicates an IO cycle.
SW/R#	88	I	SYSTEM WRITE/READ: input from the SL82C471 during CPU/Refresh cycles, from the SL82C473 during DMA and ISA master cycles and from the EISA bus during EISA master cycles. High indicates a write cycle and low indicates a read cycle.
MSBURST#	3	B	MASTER BURST: input from the EISA bus during EISA master cycles and output to the SL82C471 during DMA cycles to indicate the burst transfer capability of the master device. This pin has 18mA drive capability.
SLBURST#	160	B	SLAVE BURST: output to the EISA bus when cache or on-board DRAM is accessed during EISA master cycles. This pin has 18mA drive capability. This pin along with MSBURST# determines if burst mode will be used for the data transfer.
EX32#	15	B	EISA 32-BIT DEVICE: activated when either a 32-bit EISA slave (input mode) or cache/on-board DRAM is accessed (output mode). This information is used by both the SL82C472 and the EISA master to determine if a data size conversion is required. This pin has 18mA drive capability.
EX16#	13	B	EISA 16-BIT DEVICE: input from a 16-bit EISA slave. As an output, EX16# along with EX32# indicates the completion of the current cycle in which the master and the slave are mismatched. This pin has 18mA drive capability.

EXRDY	16	B	EISA READY: input from an EISA slave to activate SRDY# to complete the CPU cycle. As an output, EXRDY# is generated at the completion of a cycle when the system board is a slave. This pin has 18mA drive capability.
ISA BUS INTERFACE			
BALE	2	O	BUS ADDRESS LATCH ENABLE: output to the EISA bus to indicate a valid address is present on the LA lines. ISA devices should latch the address lines on the falling edge of BALE. This pin has 18mA drive capability.
MASTER16#	113	I	16-BIT MASTER: input from the bus to indicate a 16-bit ISA or EISA master is active.
IOCS16#	26	I	16-BIT IO: input from the EISA bus to indicate a 16-bit ISA IO device is accessed.
MEMCS16#	27	B	16-BIT MEMORY: input from the EISA bus to indicate a 16-bit ISA memory device is accessed. During ISA master cycles, this signal is driven active if EX16# is active or if cache or on-board DRAM is accessed. This pin has 12mA drive capability.
CHRDY	158	B	CHANNEL READY: input from the EISA bus to indicate a not ready condition (when low) and to force insertion of wait states. If an EISA slave is accessed by an ISA master, CHRDY is driven low by the SL82C472 until EXRDY becomes active. This pin has 12mA drive capability.
NOWS#	58	I	NO WAIT STATE: input from the bus to terminate the EISA bus cycle earlier than the predefined completion time.
ADDRESSES			
BE#0-3	6,7,9,10	I	HOST BYTE ENABLE: input from the CPU to select active bytes within a doubleword. BE#0-3 is translated into SBE#0-3, SA0-1 and SBHE# to drive the EISA bus.
SBE#0-3	4,5,11,12	B	EISA BYTE ENABLE: to select active bytes within a doubleword. These signals act as output during CPU (converted from BE#0-3), DMA cycles (converted from XD bus code) and ISA master cycles (converted from SA0-1, SBHE#). These signals act as input during EISA master cycles to convert to SA0-1 and SBHE# to the bus and convert the XD bus code to the chip set. During mismatched EISA master cycles, SBE#0-3 switches from input to output one BCLK after START# becomes inactive and switches back to input with the negation of the last CMD#. Each of these pins has 12mA drive capability.
SA0-1, SBHE#	151,154, 157	B	SYSTEM ADDRESS BIT 1 and 0: input from the EISA bus during ISA master cycles. In turn, these signals are converted

			to SBE#0-3 to drive the EISA bus and converted to the XD bus code for the chip set. As output, these signals convert BE#0-3 in CPU cycles, XD bus code in DMA cycles and SBE#0-3 in EISA master cycles to drive the EISA bus. Each of these pins has 18mA drive capability.
XA0,1,5	28,29,30	B	PERIPHERAL ADDRESS BUS: to exchange status information with the SL82C473. XA5 is an input only pin.
DATA BUS			
XD0-7	86,89,99,101 112,115,135, 136	B	PERIPHERAL DATA BUS: XD0-7 carry on-board IO data and status information.
ED0-31	44-47,53,54, 66,67,73,74, 76,77,84,85, 90,91,97,98, 103,104,110,111, 116,117,123-126, 133,134,146,147	B	EXTENDED CPU DATA BUS.
MPD0-3	36-39	B	MEMORY PARITY DATA BUS.
SD0-31	42,43,48,49, 51,52,68,69, 71,72,78,79, 82,83,92,93,95, 96,105,106,108, 109,118,119,121, 122,128,129,131, 132,148,149	B	SYSTEM DATA BUS.
ARBITRATION			
SHLDA	17	I	SYSTEM HOLD ACKNOWLEDGE: input from the SL82C471 to grant the bus to refresh, DMA or master devices.
OUT1	55	O	TIMER CHANNEL 1 OUTPUT: to request a DRAM refresh to the arbitration unit inside the SL82C473.
INTERRUPT INTERFACE			
IRQ3-7,9-15	137-141, 143-145,152, 155,156,159	I	INTERRUPT REQUEST: input from the EISA bus to interrupt the CPU for service. In compatible mode, the interrupt is recognized when the IRQx line makes a low-to-high transition and remains high before the first interrupt acknowledgment. If programmed to level-sensitive mode, the interrupt is recognized when the IRQx line is asserted low.

IRQ1	57	I	INTERRUPT REQUEST 1: input from the keyboard controller.
IRQ8	142	I	INTERRUPT REQUEST 8: input from the 146818A real time clock. This signal is always level-sensitive and active low.
INTR	56	O	INTERRUPT REQUEST: output to the CPU to request service for the pending interrupt.
PORTB LOGIC			
NMI#	75	B	NON-MASKABLE INTERRUPT: open-drain output to be combined with pin NMI# from the SL82C473 and inverted to feed the NMI pin of the CPU.
IOCHCK#	62	I	I/O CHECK BUS ERROR: from the EISA bus to indicate that an error in the bus has occurred.
SPKR	65	O	SPEAKER DATA OUTPUT.
MISC			
TURBO	63	I/O	TURBO SELECTION: connects to the external turbo switch to select the CPU speed between turbo and compatible modes.
SLOWH#	64	O	SLOW DOWN CPU: output to the SL82C471 to slow down the CPU execution. This signal is derived from the output of the slowdown timer counter (channel 2 of timer 2), internal register and the TURBO pin.
POWER AND GROUND			
VDD	20,40,60,80, 100,127,153	I	POWER SUPPLY of 4.5-5.5V.
VSS	1,14,22,32, 41,50,70,81, 94,107,120, 130,150	I	Ground.

2.2.1 SL472 Pin Diagram



2.3 82C472 Electrical and Timing Characteristics

2.3.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient Operating Temperature	0	70	Degree C
Storage Temperature	-65	125	Degree C
Supply Voltage (Vdd)	-0.5	7.0	V
Input Voltage	-0.5	Vdd+0.5	V
Output Voltage	-0.5	Vdd+0.5	V

2.3.2 DC Characteristics (Ta=0-70 degree C, Vdd=5V+/-5%)

Parameter	Min.	Typ.*	Max.	Unit
Input low level (TTL)	-0.5	---	0.8	V
Input high level (TTL)	2.2	---	5.5	V
Output low voltage				
4mA buffer, IOL=4mA	---	0.15	0.4	V
8mA buffer, IOL=8mA	---	0.18	0.4	V
12mA buffer, IOL=12mA	---	0.18	0.4	V
16mA buffer, IOL=16mA	---	0.17	0.4	V
Output high voltage				
4mA buffer, IOL=4mA	3.0	4.54	---	V
8mA buffer, IOL=8mA	3.0	4.44	---	V
12mA buffer, IOL=12mA	3.0	4.46	---	V
16mA buffer, IOL=16mA	3.0	4.46	---	V
Input low current	-10	-0.01	---	uA
with 50K pullup resistor	-250	-80	-20	uA
Input high current	---	0.01	10	uA
Tristate output off current low	-10	-0.01	---	uA
Tristate output off current high	---	0.01	10	uA
Input capacitance**	---	10	---	pF
Output capacitance**	---	10	---	pF
I/O capacitance**	---	10	---	pF

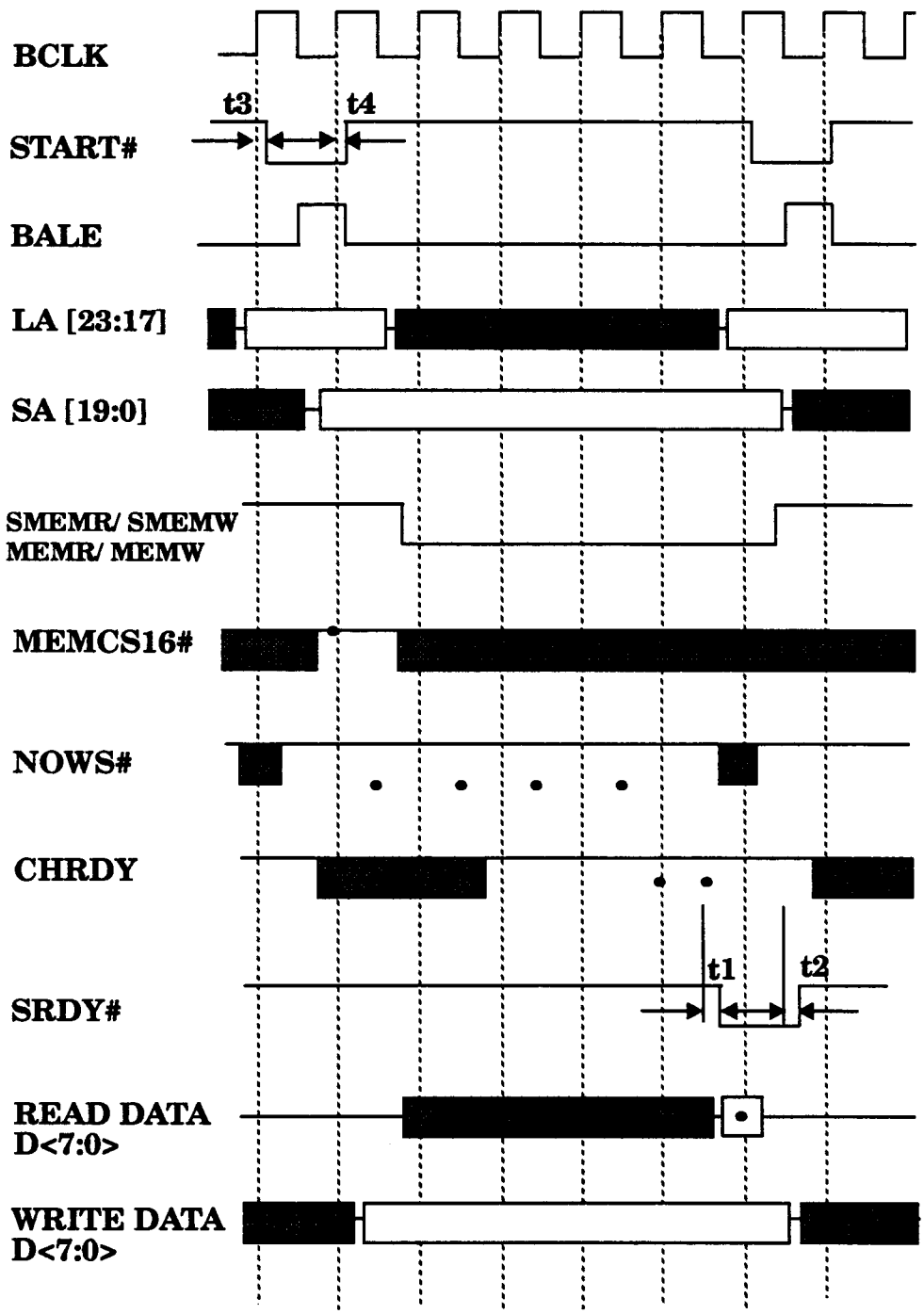
* Typical is under the condition of Vdd=5.0+/-5% and Ta=25 degree C.
** Capacitance includes the capacitance of I/O cell plus package pin.

2.3.3 AC Characteristics (Ta=0-70 degree C, Vdd=5V+/-5%; Unit=ns)

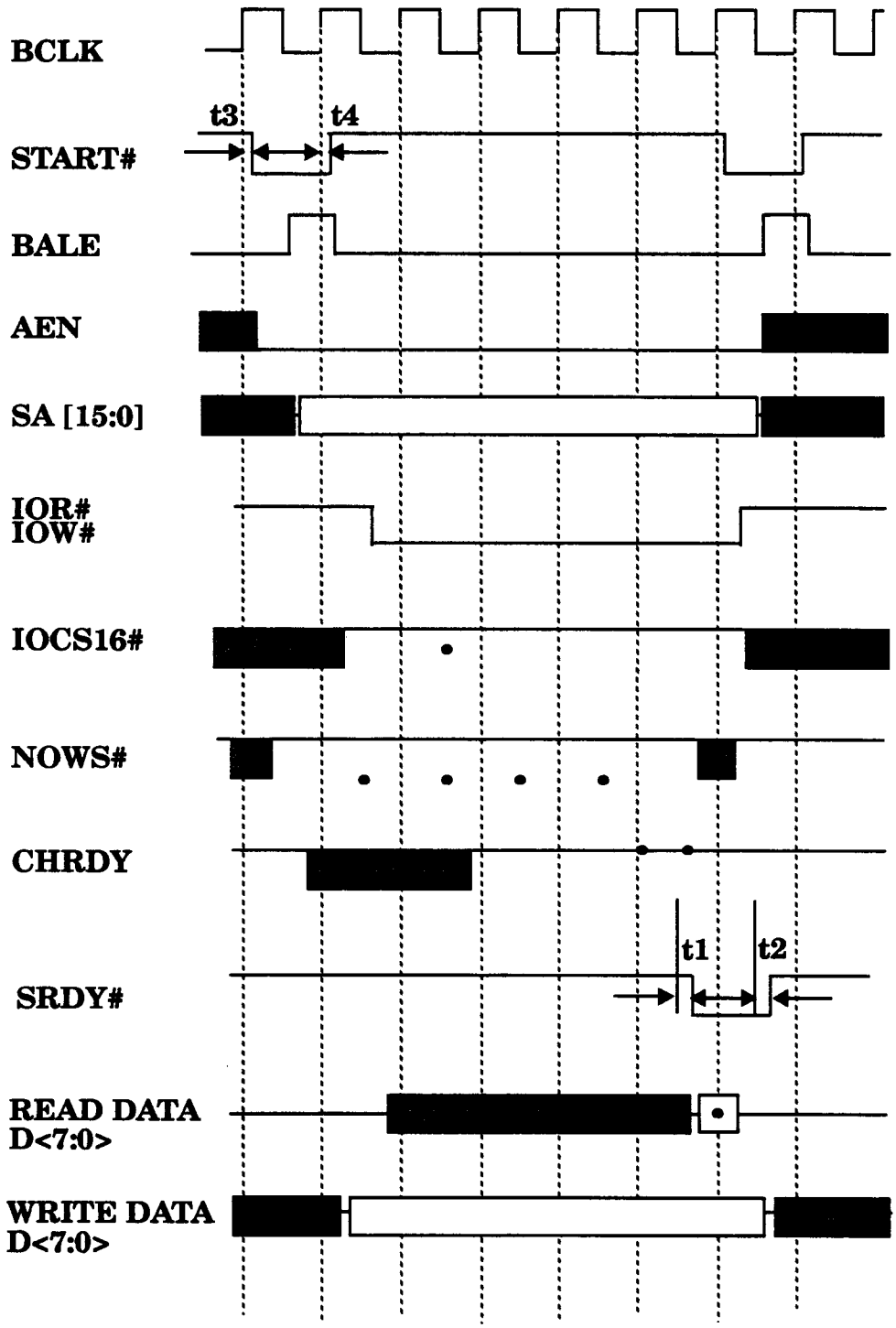
Description	Symbol	Min.	Typ.	Max.
Clock				
SRDY# active low to BCLKN rising	t1			36.7
SRDY# negated high to BCLKN rising	t2			28.2
START# active low to BCLK rising	t3			20
START# negated high to BCLK rising	t4			18

Else: Follow the EISA Specifications.

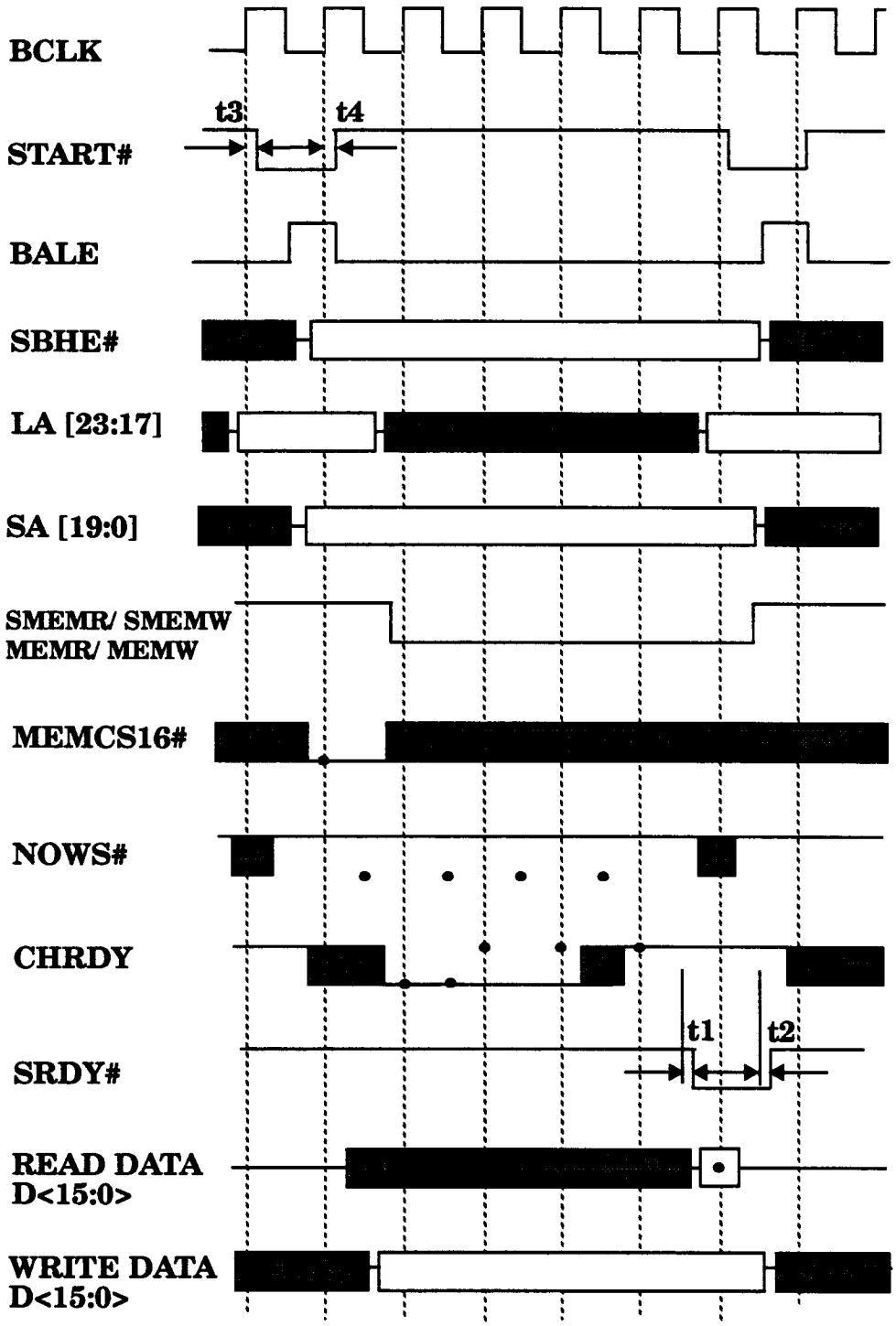
Memory Access to 8-Bit ISA Slave - Standard Cycle (6 BLCK)



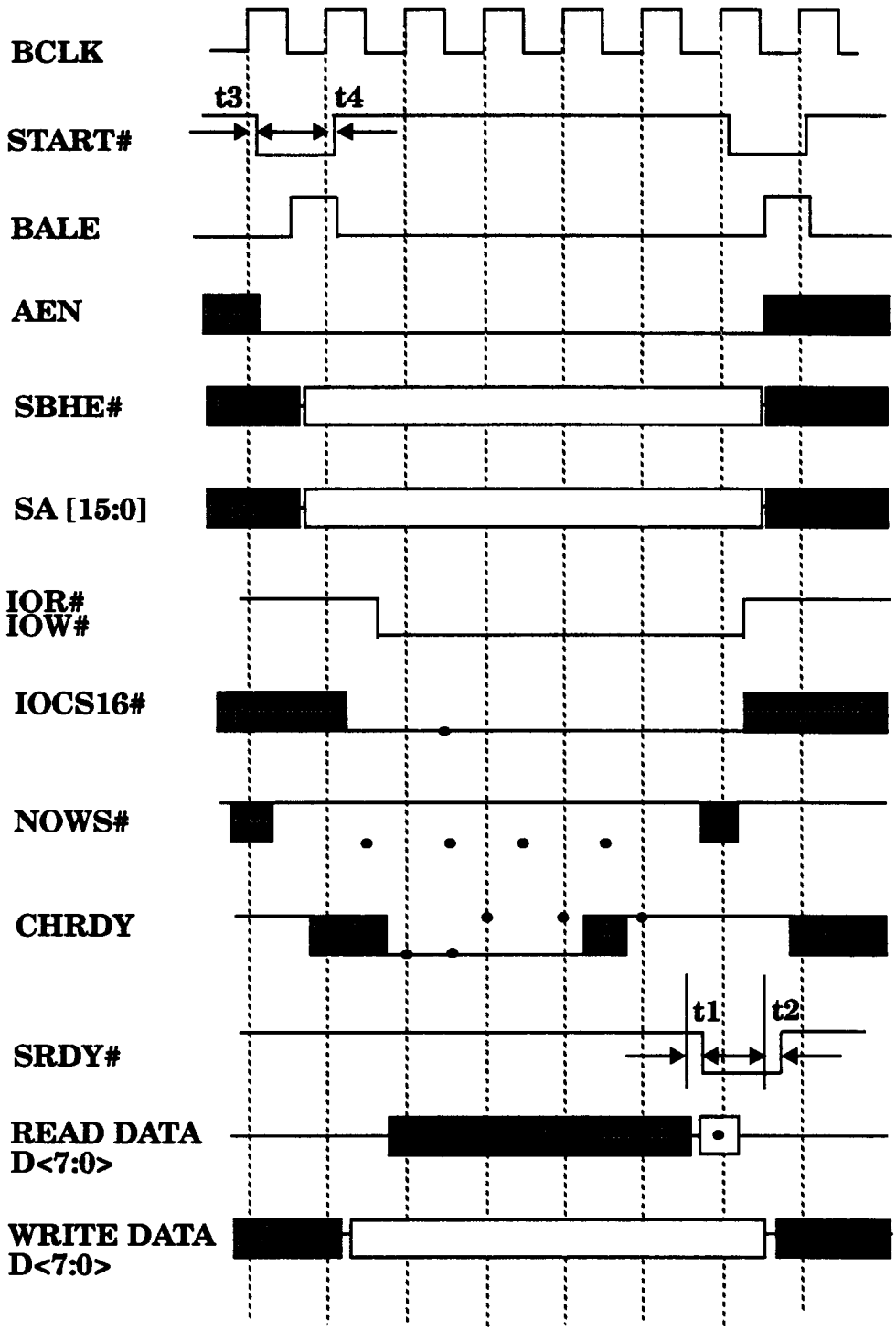
I/O Access to 8-Bit ISA Slave - Standard Cycle (6 BCLK)



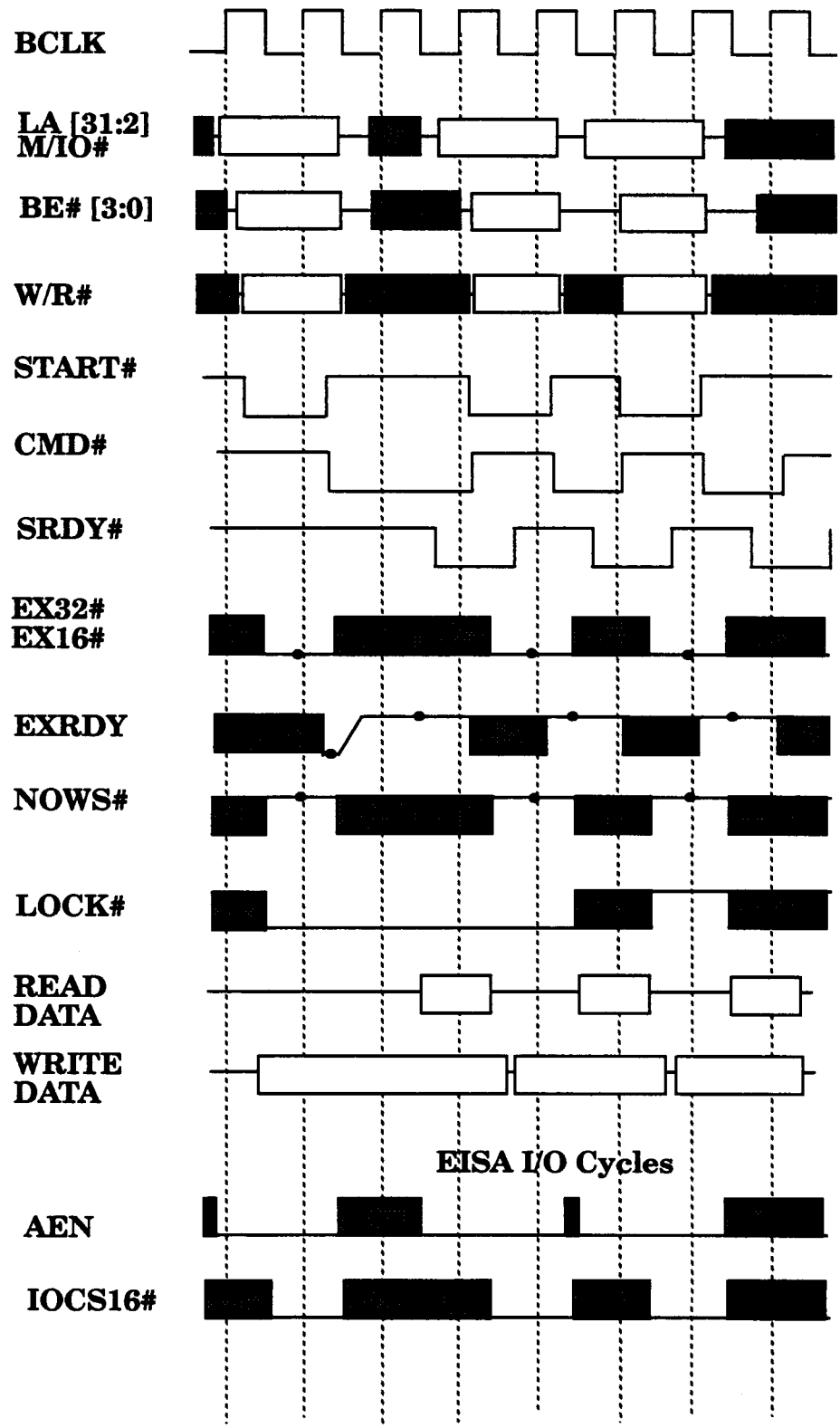
Memory Access to 16-Bit ISA Slave (6 BCLK)



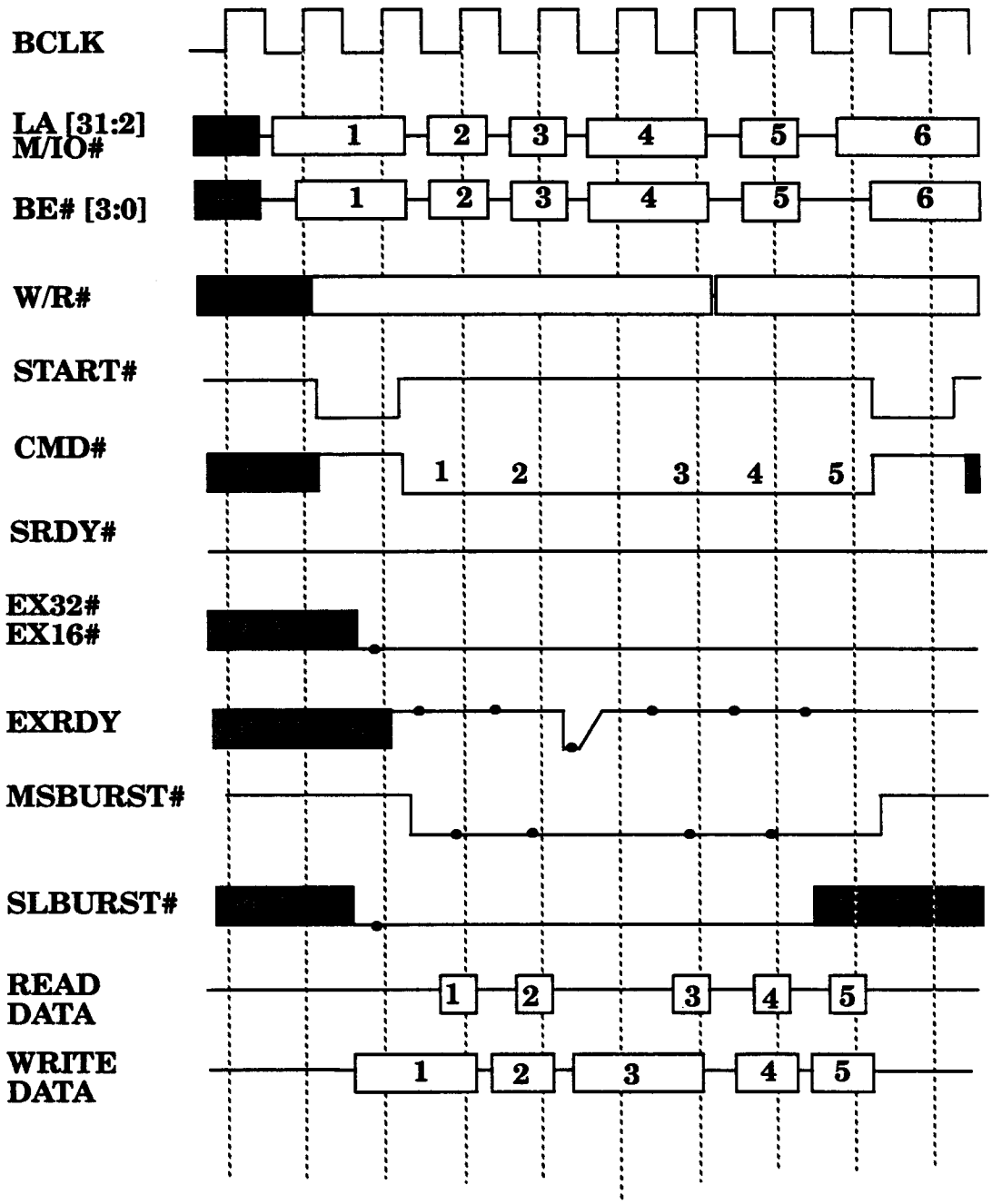
I/O Access to 16-Bit ISA Slave - Standard Cycle (6 BCLK)



Access to EISA Slave - 3 BCLK and Standard (2 BCLK) Cycles



Access to EISA Slave - Burst Cycles (With and Without Wait States)



1) EISA Standard Access Start
2) EISA Burst Access
3) EISA Burst Access with One Wait State
4/5) EISA Burst Access
6) EISA Standard Access