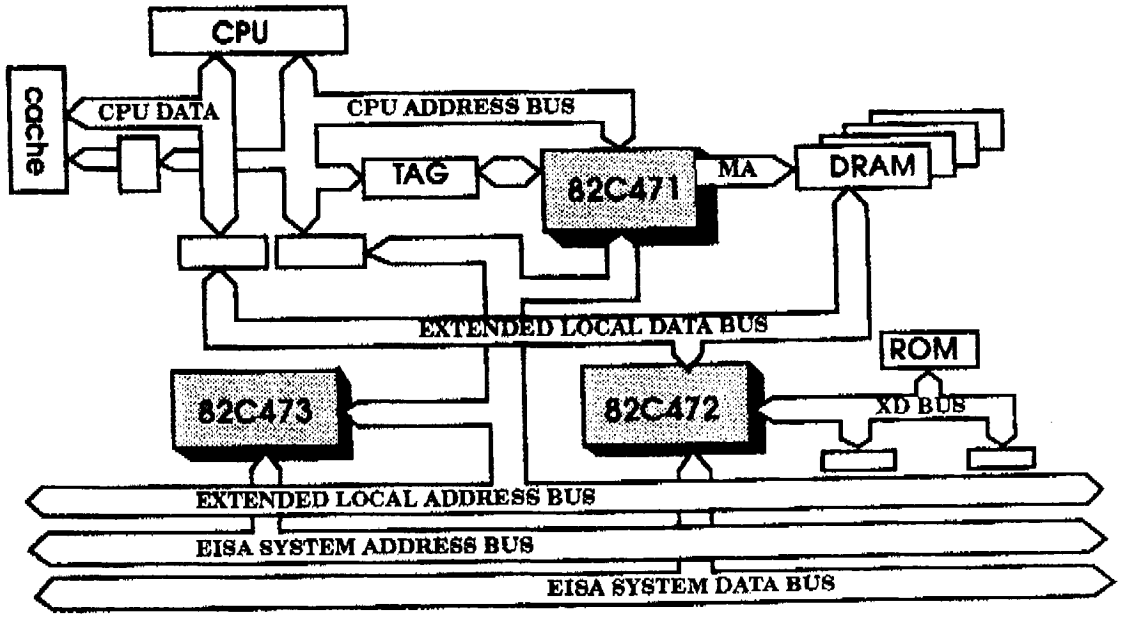
SL82C470 486/386 EISA CHIPSET

SL82C471 Cache/DRAM Controller
SL82C472 EISA Bus Controller
SL82C473 DMA Controller

- 100% EISA compatible
- 20/25/33/50 MHz 80486 DX/SX CPU operation
- 25/33/40 Mhz 80386DX CPU operation
- Integrated write back cache controller with built-in tag comparator
- Concurrent CPU-cache and DMA/master operations with bus snooping
- Only ten TTL components are required
- Complete EISA system can be built on a baby AT sized motherboard
- Flexible cache size from 64KB to 1MB
- Page mode DRAM operation supporting 1 to 4 banks up to 256MB
- Video/system BIOS shadowing and caching
- Supports both conventional and concurrent configurations
- Inclusive secondary cache for snoop filtering
- Synchronous EISA bus clock
- Transparent Gate A20 and CPU reset
- CPU local bus device support
- Supports 80387, 80487SX and Weitek 3167/4167 co-processors
- Decoupled refresh without holding CPU
- Staggered DRAM refresh to minimize power supply noise
- Rich set of register options to allow customization
- Three 160-pin PQFP packages in low power and high speed 0.8um CMOS Technology



SL82C470 system block diagram

The SL82C470 chip set provides a very high performance, highly integrated and cost-effective implementation for personal computer systems based on the standard EISA bus. It supports both 386DX and 486DX/SX CPUs over the entire performance range, from 20Mhz to 50Mhz. The chip set can operate in either 'conventional' or 'concurrent' configuration. Under the conventional configuration, the cache subsystem is dedicated to bus snooping when a DMA or master device becomes active. Under the concurrent configuration, the CPU-cache operation continues while bus snooping is performed for the DMA or master device to explore maximum concurrency between the CPU and the EISA bus. Only ten TTLs are required for a complete motherboard design under the conventional configuration in addition to the chip set and memory devices. Five additional TTLs are required for the concurrent configuration. A complete EISA system of either configuration can be easily implemented on a baby AT sized motherboard.

The SL82C470 chip set consists of three 160-pin PQFP devices: the SL82C471 integrated cache/ DRAM controller, the SL82C472 EISA bus controller and the SL82C473 DMA controller.

SL82C471 Cache/DRAM Controller

The SL82C471 Cache/DRAM controller controls the cache and DRAM accesses from the CPU, EISA/ISA masters and DMA devices. The chip adopts a write-back cache scheme to minimize the interference between the CPU-cache and DMA/ master during their concurrent operations. The cache size ranges from 64KB to 1MB with advanced features such as 2-1-1-1 burst line fill, snoop-filtering, local bus support and programmable non-cacheable and write-protected regions. The page mode DRAM controller supports 1 to 4 banks of DRAMs up to 256MB. A mixture of 256KB, 1MB, 4MB and 16MB DRAMs is supported. The video and system BIOS can be shadowed or cached independently. The cache-DRAM subsystem allows zero wait state burst mode DMA transfers to take full advantage of the high bandwidth of the EISA bus.

The DRAM data bus can either be connected directly to the CPU local bus or be buffered externally. The control signals for the external buffers are generated by the SL82C471.

SL82C472 EISA Bus Controller

The SL82C472 EISA bus controller translates bus control signals between the CPU, EISA/ISA and DMA masters and slaves. The chip also includes buffers and byte/word swap logic between the CPU (or DRAM) and the EISA bus. The bus conversion and data alignment are performed automatically.

The SL82C472 includes two 8259 interrupt controllers and four 8254 timer channels modified for 100% EISA compatibility. The chip also includes parity generation and check logic and NMI and time-out logic.

SL82C473 EISA DMA Controller

The SL82C473 DMA controller implements seven EISA DMA channels, the system arbiter and the co-processor interface logic. The DMA controller supports compatible, type A, type B and type C (burst) mode operations with the buffer chaining capability. The multi-level rotating priority arbitration with fail-safe time-out is implemented for the system arbiter. Six sets of slot-specific master handshake signals (MACK and MREQ) are provided directly without any external components.

The address latches and buffers for the EISA bus are also included in the SL82C473.

2620 Augustine Dr., Suite #250, Santa Clara, Ca. 95054. Tel:(408)986-1701 Fax:(408)986-1771