SL82C465 CACHE CONTROLLER

- Integrated direct mapped cache controller
- Supports 486/386DX/386SX CPU
- Supports both 1X and 2X CPU clock
- Supports 486DX/SX/DX2/SLC up to 50 MHz
- Supports 386DX/SX/SXLV up to 40 MHz
- 16KB to 4MB cache size
- Line size from 1 to 4 doublewords
- VL-Bus Master Device support
- 2-1-1-1 burst mode cache fill
- Data streaming in external and internal cache
- SRAM banks interleaving capability
- Built-in tag comparator
- Posted write buffer control
- Cache invalidation support
- Non-cacheable region support
- 387SX/387/3167/4167 interface
- Arbitration between reset and HOLD
- CMOS 100-pin RQFP package

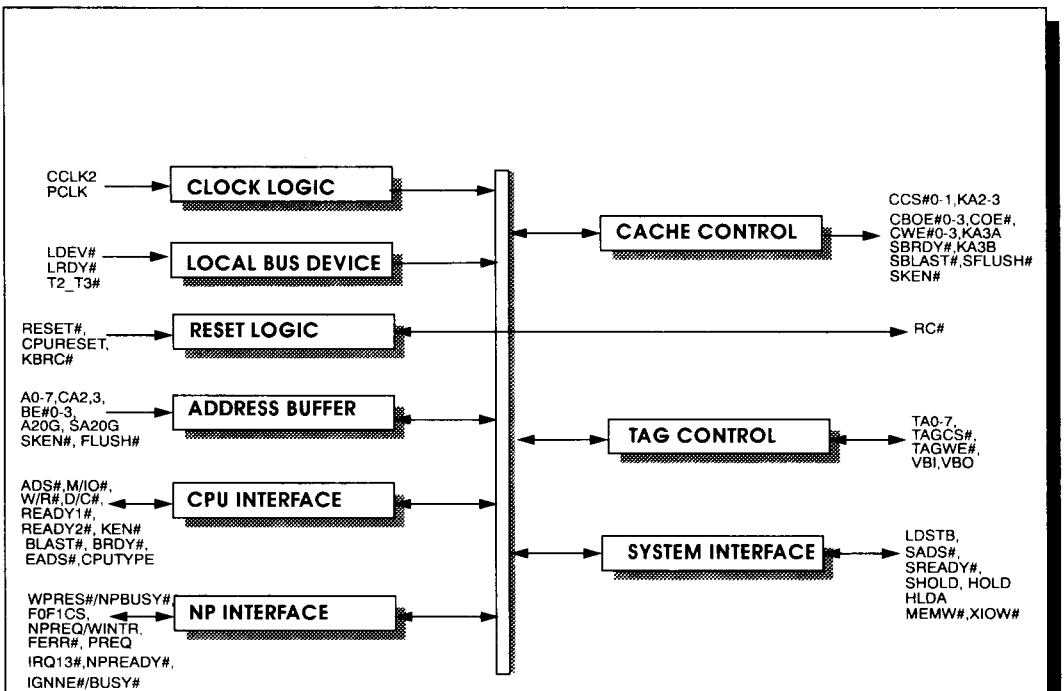


Figure 1-1: 82C465 Block Diagram

1 Functional Description

1.1 Clock mode

The SL82C465 cache controller supports both 1X and 2X clock modes. The 1X clock mode means that the CCLK2 signal is used as the CPU clock; the 2X clock mode means that the PCLK signal (half the frequency and the phase indicator of CCLK2) is used as the CPU clock. The SL82C465 and other CPU local bus devices run at the same clock frequency as the CPU, while the rest of the system runs at the frequency of PCLK. In other words, the operating frequency of the system logic is either the same (2X clock mode) or half the speed of the CPU (1X clock mode). For the 1X clock mode, the timing of the signals between the CPU/Cache and the system logic interface is converted by the SL82C465 automatically to satisfy the requirement of individual clocks. Table 1-1 lists the operating frequencies of the CPU local bus and the system logic with the oscillator used.

Mode	CPU	System	Osc.
1X	50	25	50Mhz
1X	40	20	40Mhz
2X	40	40	80Mhz
2X	33	33	66Mhz
2X	25	25	50Mhz

Table 1-1: CPU and System Clock

The 2X clock mode is recommended for a CPU frequency no faster than 33Mhz because the system logic is available at the targeted speed and the performance is slightly better than if 1X clock mode were used. For a CPU frequency faster than 33Mhz, the 1X clock mode is preferred for 486 systems because it becomes increasingly more difficult to build a reliable system with an oscillator faster than 66Mhz.

1.2 Cache Organization

The SL82C465 supports a direct-mapped cache system with data size ranging from 16KB to 4MB and line size ranging from 1 to 4 doublewords (words for a 386SX system). Without any external logic, the SL82C465 supports 1 to 4 banks of cache SRAMs independent of the line size.

There is almost no limitation to the size of the cache directory. Table 1-2 lists some common cache organizations with cache size ranging from 32K to 4MB for 386/486 systems and 16K to 256K for 386SX systems. Refer to section 1.14 for detail design examples.

386/486	l-size	tag	index
32K	1	A22:15	A14:2
32K	4	A22:15	A14:4
64K	1	A23:16	A15:2
64K	4	A23:16	A15:4
128K	1	A24:17	A16:2
128K	4	A24:17	A16:4
256K	4	A25:18	A17:4
512K	4	A25:19	A18:4
1M	4	A25:20	A19:4
2M	4	A25:21	A20:4
4M	4	A25:22	A21:4
386SX	**l-size**	**tag**	**index**
16K	1	A21:14	A13:1
32K	1	A22:16	A14:1
64K	2	A23:16	A15:2
128K	2	A23:17	A16:2
256K	4	A23:19	A18:4

Table 1-2: Cache Organization

An 8-bit tag RAM and a 1-bit valid RAM that match the size of the cache directory are required for the cache implementation as is indicated in Figure 1-1. Both SRAMs can be implemented with or without the OE (output enable) pin. SRAMs with the OE pin consume less power while those without are usually less expensive.

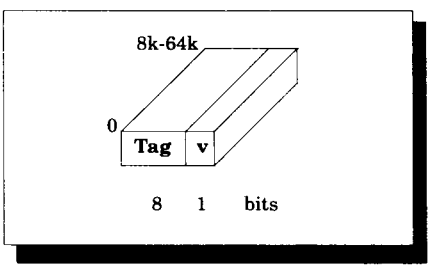


Figure 1-1: Cache Directory Organization

The 1-bit valid RAM can be combined into the tag RAM to save the component costs. The number of tag bits is reduced to 7 in such configurations. This option is selected by conditioning the RC# pin (#52) during power on reset. See section 1.13 for details.

1.3 486 Burst Mode Cache Fill

In a 486 system, burst mode cache fill is supported independently for the two level caches: the BRDY# and BLAST# signals are used in the interface between the CPU internal cache and the SL82C465-controlled external (secondary) cache. The SBRDY# and SBLAST# signals are used in the interface between the secondary cache and the system logic.

In a cache hit the burst length (the number of burst cycles performed) is determined by the line size of the secondary cache and the number of cycles before the CPU asserts the BLAST#. If the read results in a cache miss, then the SADS# and SBLAST# are asserted to notify the system to transfer data using the burst mode. The burst length is determined by the line size of the secondary cache and the number of cycles performed before the system asserts SREADY# (instead of SBRDY#).

1.4 Burst transfer in 386DX/SX systems

The SL82C465 supports 486-style burst mode transfer in 386DX/SX systems through the SBRDY# and SBLAST# pins. This allows the SL82C465 to support a larger cache size with a bigger line size for 386DX/SX cache systems without increasing the size of the tag RAM. However, the penalty is also greater in the case of cache miss cycles because of the longer cache fill process. This penalty can be reduced by the burst mode transfer mechanism.

When SBRDY# is received, the KA3 and KA2 are counted according to the 486-burst order but with such adjustment that the last data filled into cache is the data requested by the CPU. For instance, if the CPU requests the 3rd doubleword from a cache with line size 4, then the burst order is 4->0->C->8, which is 486-burst order with the last doubleword being the one that is requested.

The assertion of SBRDY# indicates the external system is capable of performing burst mode data transfer. Then no further SADS# will be asserted. If SREADY# is received instead of SBRDY#, the SL82C465 switches back to normal non-burst transfer automatically by activating SADS#. In this case, the 'CPU' address seen by the system logic (pin KA2-3) will be updated for each cycle.

1.5 Cache Operation

When the CPU starts a cycle, the index field of the CPU address selects a line from the cache directory. The tag stored in this line is compared with the tag field of the CPU address to determine a hit. If a hit is detected and the line is valid, the cache control signals CWE#3:0,CBOE#3:0/COE# are asserted for the proper cache data transfer.

A special data streaming technique is used to enable the 486 internal cache to be filled at the same time while the secondary cache is filled. After the first doubleword is transferred, the CPU can continue its operation while the rest of the line is filled. This technique results in a significant improvement on the system performance.

Write-through algorithm is used in write cycles to ensure that the data present in the cache is identical to the data in the main memory. Also, one level of posted-write buffer is supported to minimize the write-through penalty.

1.5.1 Read Hit Operation

When a read hit occurs, the SL82C465 starts transferring data to the CPU. If the line size of the secondary cache is 1 doubleword, then non-burst transfer is used with READY# returned to the CPU. Otherwise, the burst mode is used for the transfer until either the burst cycle count equals the line size or the CPU asserts the BLAST# signal. The maximum burst length is 4 doublewords.

In the case of 1 doubleword transfer, the READY# signal will be returned to the CPU by the end of T2 cycle to provide a zero wait state operation. To relax the data SRAM access time, COE# is always asserted when a CPU memory read cycle is detected. This signal remains asserted in the T2 cycle to drive cache data onto the CPU data bus if a read-hit is detected; otherwise the signal returns to high at the start of T2 cycle. COE# is mainly used in configurations with one bank of SRAMs. For configurations with two banks of SRAMs, CBOE#0-1are used to activate and deactivate each bank.

In a 486 system, there are two options available for the number of CPU cycles spent on each burst transfer: 2-1-1-1 and 3-2-2-2. The 2-1-1-1 option means two CPU cycles for the first transfer and one CPU cycle for the following three transfers. These numbers are the best possible timing with the 80486 CPU. However, high speed SRAM or external TTL data buffers are required. The timing for a 3-2-2-2 transfer is much more relaxed with a slight degradation on the system performance. This option is selected by conditioning pin EADS#

during power on reset. Refer to section 1.13 for details.

The 2-1-1-1 timing is easier to achieve with two or four banks of SRAMs. To save the board real estate and cost, cache address interleaving is implemented to allow two banks of SRAMs executing 2-1-1-1 burst transfer. Note that the least significant bit of the SRAM address needs to be toggled during the burst transfer period. Since the address to data access time is longer than the OE to data access time, the address needs to be settled one cycle before the OE activates. By interleaving the doublewords into the two banks, one bank is activated while the address of the other bank is changed. This arrangement makes 2-1-1-1 transfer timing possible. Pin KA3A and KA3B (multi-function pin CCS#2-3) are the interleaved address pins that connect to the least significant bit of each bank of the SRAMs.

3-2-2-2 transfer relaxes the timing requirement in three ways:

1. The tag RAM speed is relaxed because three cycles are available to determine the cache hit instead of two.
2. The OE to data access time for the data RAM is relaxed because another half clock cycle is available.

3. The OE to data tri-state time is relaxed because the activation of one OE lags half a clock cycle from the deactivation of the previous OE.

During cache read hits, the previous data latched in the posted-write buffer can be concurrently popped out without slowing down the CPU execution.

1.5.2 Read Miss Operation

If the CPU address mis-matches the tag or the matched tag is invalid, a cache miss is indicated. If a cache read miss occurs, wait states are added to hold the CPU until the data retained in the write buffer is cleared and the requested data is ready on the CPU data bus.

When the write buffer is empty, the signal SADS# is asserted to initiate the system logic for DRAM or AT bus cycle.

In a 386DX/SX system, if the read request is cacheable through input pin SKEN#, cache line fill operation is initiated as follow:

A number of DRAM read cycle performs;
CWE#3:0 are all activated for each cycle;
CCS#3:0 and KA3:2 are updated for each double word filled;
The requested data is presented in the last cycle;
The valid bit is set for the filled line;
The tag is updated.

The number of read cycles performed is equal to the line size of the cache. If the read request is not cacheable, then only one read cycle for the requested data is performed regardless of the line size and neither the tag nor the valid bit is updated.

In a 486 system, when a read miss happens, if the line size of the secondary cache is 1 doubleword, then non-burst transfer is used with SBLAST# asserted at the very first cycle. Otherwise, the burst mode is used for the transfer until either the burst cycle count equals the line size, the system replies with SREADY# (instead of SBRY#) or the CPU terminates the burst transfer with BLAST# asserted. The maximum burst length is 4 doublewords.

Unless the burst transfer is terminated by the CPU, a new cycle will start by issuing another SADS# to continue the cache fill process. The process repeats until it is terminated by the CPU.

The CPU internal cache is filled at the same time while the secondary cache is filled, thus the first doubleword transferred is the one requested by the CPU. The CPU then continues its operation while the rest of the line is filled.

1.5.3 Write Hit Operation

During the write hit, both cache memory and system memory need to be updated. For cache, CWE#0-3 of the active bytes are asserted to write data into the cache memory, and READY# is returned to the CPU for the next command. For the system memory, the data is held temporarily in the write buffer, and the system logic takes over to complete the data write operation.

Write cycle can be either zero wait state or one wait state. The timing requirement for the tag RAM is more relaxed for the one-wait-state option while the performance is slightly better for the zero-wait-state option. For the zero-wait-state option, a pull-down resister is required on pin KEN#/WWS(#49) for proper configuration.

If the write buffer is loaded with previous data, the

CPU is held until previous write operation is complete and the current data can be latched into the write buffer.

1.5.4 Write Miss Operation

If a cache miss occurs in a write cycle, no cache write operation is performed. The 82C465 bypasses the cache and writes to DRAM directly.

1.5.5 DMA/Master Operation

During the DMA or external master cycles, the CPU is held and the cache control logic does not perform any function except the line invalidation. All the memory operations are directly interfaced to the DRAM control logic.

If a hit occurs in the memory write operation during DMA and master cycles, the corresponding valid bit is reset; otherwise no action is taken.

1.6 Cache Initialization

A valid bit is associated with each line in the cache to indicate whether the data in the cache are valid. The valid bit is set for each cache fill and reset by the bus snooping or cache flush. All cache memory entries must be initialized by a memory access with the flush signal asserted. The flush signal can be asserted by programming a register in the SL82C460 chip set. The cache controller is disabled after power-on reset and is enabled after the flush input has been toggled for three times.

1.7 Non-Cacheable Regions

All I/O address space is not cacheable. Whether a memory cycle is cacheable depends on input pin SKEN# which is sampled at the start of T2 cycle. The SKEN# can be directly driven by pin KEN# of the SL82C460 chip set which supports two non-cacheable regions with sizes ranging from 16K to 4MB in addition to the standard non-cacheable region A0000h to BFFFFh. As the third non-cacheable region, the memory address space above 8MB, 16MB or 32MB can also be turned into non-cacheable regions.

1.8 Posted-Write Buffer Control

One level of posted-write buffer is supported by the SL82C465 to minimize the write penalty incurred by the slower DRAM and AT bus devices. The CPU data is temporarily stored in the buffer so that the CPU bus can be released for the following cache read-hit operations. The buffer is released for the next write command upon completion of the system write operation.

The write buffer built inside the SL82C460 chip set is directly controlled by the LDSTB pin of SL82C465. When this pin goes high, the CPU data becomes transparent. The data is latched into the buffer at the falling edge of LDSTB.

The posted write capability is disabled upon power-on reset. This capability is turned on after the flush signal has been toggled for five times.

1.9 READY Generation

There are two possible connections of 'ready' signal between SL82C465 and the CPU: READY1# and READY2#. These two signals are identical for read-hit cycles and the difference is for cycles that are passed to the system logic or other CPU local devices such as the Weitek WT4167. Pin READY1# returns ready to the CPU in the same cycle that these devices activate ready, while pin READY2# waits for another CPU cycle. The performance is slightly better with READY1# connection. However, for clock frequency higher than 33Mhz, READY2# connection should be used to meet the required setup time by the CPU.

1.10 NP Interface

Haydn chip set supports all of the commercially available Numeric Co-processors. In a cache system, the NP interface pins are located in the SL82C465. In a non-cache system, NP interface are located in the SL82C461.

The ready output generated by the 387/387SX/WT3167/WT4167 is combined with that from the system logic and cache read hit operation for the CPU READY#.

387SX/387/3167/4167 cycles are detected through CPU command status and address pin CA31 and CA29. The SL82C465 detects the presence of NP automatically during power-on reset. NP cycles without the presence of NP are handled by the SL82C465.

The SL82C465 supports the floating point errors in conjunction with the 486 CPU. The trailing edge of FERR# triggers an internal flip flop to generate the IRQ signal which is ORed with the WINTR signal from

the WT4167 to form the interrupt level 13 (IRQ13#). After FERR# is asserted, the interrupt service routine handles the error and then clears the interrupt by executing an IO write to port F0h. The IGNNE# goes low in response to allow non-controlling instructions to be executed prior to the time the FERR# signal is reset by the CPU. This logic is implemented for AT compatibility.

NPREQ, NPBUSY# and NPERR# are inputs from the 387/387SX to be converted as PREQ and BUSY# to the 386 CPU, respectively. IRQ13# is asserted when NPERR# is asserted for an NP error.

F0F1CS is input from the SL82C461 chip to indicate an IO write cycle to address F0h-F7h for clearing the ERROR status of the NP interface.

1.11 Arbitration

The CPU hold request is arbitrated in the SL82C465 with the RC# signal from the keyboard controller (KBRC#). This arbitration guarantees the CPU cannot be reset when it is in a HOLD status. The HOLD signal is also arbitrated with the state machine that controls the posted-write operation. The CPU does not receive the hold request until the write buffer is cleared.

1.12 GateA20 Logic

There are two sources of GateA20 in a typical PC/AT system: the keyboard controller and the fast GateA20 register. The effective GateA20 is the logic OR of these two signals.

The GateA20 input from the keyboard controller is connected to pin A20G and is converted to open source output in pin SA20G. This signal is then combined with the SA20G open source output of the SL82C461 to obtain the final GateA20 for the 80486 CPU and the Haydn chip set.

CA20 is usually the most critical bit of the CPU address because one additional AND gate is required for the GateA20 logic. This address bit is always allocated as one of the tag bits rather than index bits in the SL82C465 cache controller. Note that the timing requirement for a tag bit is far more relaxed than that for an index bit so that the system performance is not penalized by the presence of the GateA20 logic.

There are eight bits of tag that are supported by the SL82C465: pin A0 to A7. The connection of these bits to the CPU address bus depends on the cache configuration (Table 1-2). For a cache size no larger than 1MB, CA20 which is always a tag bit should be connected to pin A4. The other seven bits can be connected arbitrarily with the other seven address bits. For a cache size larger than 1MB, CA is not a tag bit and pin A4 should be tied to VSS. Only seven bits of tag remain which is not a concern for such a large cache size.

1.13 Cache Configurations

The SL82C465 supports a flexible cache configuration determined by the condition of a few pre-designated pins during power-on reset. A pull-up '1" or pull-down '0' resistor on these pins (each pin is internally pulled up by a 50K resistor) set the SL82C465 configurations as follows:

Clock mode: (IRQ13#-60)
- (0) - 1X clock mode
- (1) - 2X clock mode

Line size: (TAGOE#-37, VBO-31)
- (0,0) or (1,1) - 1 doubleword
- (0,1) - 2 doublewords
- (1,0) - 4 doublewords

SRAM banks: (SBLAST#-76)
- (0) - 1 bank or 4 banks
- (1) - 1 bank or 2 banks (VL-Bus master mode)

Burst fill rate: (EADS#-48)
- (0) - 3-2-2-2 burst timing
- (1) - 2-1-1-1 burst timing

Write wait state: (KEN#-49)
- (0) - 0 wait state
- (1) - 1 wait state

Combined valid/tag SRAM: (RC#-52)
- (0) - not combined
- (1) - combined

1.14 Design Examples

Following are recommended cache configurations based on the most popular SRAMs in the market today. For cost considerations, the cache valid bit is combined into the Tag SRAM. Figure 1-2 is the block diagram for these examples.

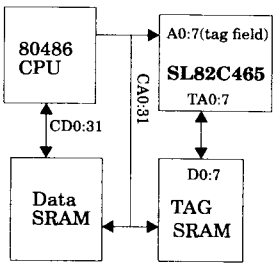


Figure 1.2: Cache Subsystem

1.14.1 Recommended cache configurations for 486 Family

Cache Size	64K	128K	256K	512K	1M
Cache Bank	2	1	2	1	2
Data SRAM	8Kx8x8	32Kx8x4	32Kx8x8	128Kx8x4	128Kx 8x8
Tag SRAM	8Kx8x1	8Kx8x1	32Kx8x1	32Kx8x1	128Kx8x1
Line Size	128 bit	128 bit	128 bit	128 bit	128 bit
Cacheable range	8 Mbyte	16 Mbyte	32 Mbyte	64 Mbyte	64 Mbyte
Tag comparator Address connection in SL82C465					
A4	CA20	CA20	CA20	CA20	CA20
A7	VCC	VCC	VCC	VCC	VCC
A[0,1,2,3,5,6]	CA[16-22]	CA[17-23]	CA[18-24]	CA[19-25]	CA[20-25]
Tag SRAM connection					
Address (Index)	CA[4-15]	CA[4-16]	CA[4-17]	CA[4-18]	CA[4-19]
Data (Tag)	CA[16-22]	CA[17-23]	CA[18-24]	CA[19-25]	CA[20-25]
CE#	GND	GND	GND	GND	GND
OE#	TAGOE#	TAGOE#	TAGOE#	TAGOE#	TAGOE#
WE#	TAGWE#	TAGWE#	TAGWE#	TAGWE#	TAGWE#
DATA SRAM Connection					
Address	KA3A/KA3B	CA[2-16]	KA3A/KA3B	CA[2-18]	KA3A/KA3B
	CA[4-15]		CA[4-17]		CA[4-19]
CE#	CCS#0/	GND	CCS#0/	GND	CCS#0/
	CCS#1		CCS#1		CCS#1
OE#	CBOE#0/	COE#	CBOE#0/	COE#	CBOE#0/
	CBOE#1		CBOE#1		CBOE#1
WE#	CWE#0-3	CWE#0-3	CWE#0-3	CWE#0-3	CWE#0-3

1.14.2 Recommended cache configurations for 386 Family

Cache Size	32K	64K	128K	256K
Cache Bank	1	2	1	2
Data SRAM	8Kx 8x4	8Kx8x8	32Kx8x4	32Kx8x8
Tag SRAM	8Kx8x1	8Kx8x1	32Kx8x1	32Kx8x1
Line Size	32 bit	64 bit	32 bit	64 bit
Cacheable range	4 Mbyte	8 Mbyte	16 Mbyte	32 Mbyte
Tag comparator Address connection in SL82C465				
A4	CA20	CA20	CA20	CA20
A7	VCC	VCC	VCC	VCC
A[0,1,2,3,5,6]	CA[15-21]	CA[16-22]	CA[17-23]	CA[18-24]
Tag SRAM connection				
Address (Index)	CA[2-14]	CA[3-15]	CA[2-16]	CA[3-17]
Data (Tag)	CA[15-21]	CA[16-22]	CA[17-23]	CA[18-24]
CE#	GND	GND	GND	GND
OE#	TAGOE#	TAGOE#	TAGOE#	TAGOE#
WE#	TAGWE#	TAGWE#	TAGWE#	TAGWE#
DATA SRAM Connection				
Address	CA[2-14]	CA[3-15]	CA[2-16]	CA[3-17]
CE#	GND	CCS#0/ CCS#1	GND	CCS#0/ CCS#1
OE#	COE#	CBOE#0/ CBOE#1	COE#	CBOE#0/ CBOE#1
WE#	CWE#0-3	CWE#0-3	CWE#0-3	CWE#0-3
SL82C461 Address Line Connection				
A2	CA2	KA2	CA2	KA2

1.14.3 Recommended cache configurations for 386 SX Family

Cache Size	16K	32K	64K	128K
Cache Bank	1	2	1	2
Data SRAM	8Kx 8x2	8Kx8x4	32Kx8x2	32Kx8x4
Tag SRAM	8Kx8x1	8Kx8x1	32Kx8x1	32Kx8x1
Line Size	16 bit	32 bit	16 bit	32 bit
Cacheable range	2 Mbyte	4 Mbyte	8 Mbyte	16 Mbyte

Tag comparator Address connection in SL82C465				
A4	CA20	CA20	CA20	CA20
A7	VCC	VCC	VCC	VCC
A[0,1,2,3,5,6]	CA[15-21]	CA[16-22]	CA[17-23]	CA[18-24]
Tag SRAM connection				
Address (Index)	CA[1-13]	CA[2-14]	CA[1-15]	CA[2-16]
Data (Tag)	CA[14-20]	CA[15-21]	CA[16-22]	CA[17-23]
CE#	GND	GND	GND	GND
OE#	TAGOE#	TAGOE#	TAGOE#	TAGOE#
WE#	TAGWE#	TAGWE#	TAGWE#	TAGWE#
DATA SRAM Connection				
Address	CA[1-13]	CA[2-14]	CA[1-15]	CA[2-16]
CE#	GND	CCS#0/ CCS#1	GND	CCS#0/ CCS#1
OE#	COE#	CBOE#0/ CBOE#1	COE#	CBOE#0/ CBOE#1
WE#	CWE#0-1	CWE#0-1	CWE#0-1	CWE#0-1
SL82C461 Address Line connection				
A1	CA1	KA2	CA1	KA2
A2	CA2	KA3	CA2	KA3

1.15 VL-Bus master device support

The SL82C465 rev.1.2 has built-in support for VESA compatible Local Bus devices. The SL82C465 samples the existence of LDEV# from a local bus device either at the end of the first T2 or the second T2 depending on the pull-up/down resistor status of pin T2_T3# during the power-on reset period. The LDEV# signal is also connected to the SL82C461 to indicate that the current cycle is a local bus cycle, and relinquish the control to the local bus devices. The SL82C465 has two ways to return the LRDY# signal from a local bus device to the CPU. LRDY# is internally ANDed with the SL82C465 ready sources and returns the ready signal through READY1# or READY2#. When LRDY# is activated, the READY#1 is activated low immediately while READY#2 is activated after being synchronized with the CPU clock. READY#1 is recommended for local bus systems running under 33MHz. For local bus systems running higher than 33MHz, READY#2 is recommended. The local bus device should alway: monitor READY# input signal and keep the data vali until the CPU reads the data back.

In some new revisions of the SL82C465 pin 44 and 55 have been mutiplexed to support the VL-Bus master function. When pin 76(SBLAST#) is pulled high, pin 44 and 55 become the LREQ# and LGNT# signals. When pin 76(SBLAST#) is pulled low, pin 44 and 55 are the CBOE2 and CBOE3 signals. LREQ# and LGNT# work conjunctionly. The VL-Bus master asserts LREQ# to the SL82C465, then the SL82C465 responds by asserting LGNT# to allow the VL-Bus master to gain the control of the VL-Bus.

2 SL82C465 Signal Description

Signal Name	Pin Number	Type	Signal Description
CLOCK /RESET			
CCLK2	14	I	Clock input from the SL82C461. It is the same clock input to the CPU in the 1X clock mode.
PCLK	79	I	Phase clock from the SL82C461. A logic high indicates phase 1 and low indicates phase 2. It is the same clock input to the CPU in the 2X clock mode.
CPURESET	80	I	CPU reset.
RESET#	35	I	Active low system reset.
KBRC#	51	I	Keyboard RC# to request the CPU reset. This input is arbitrated with HLDA to generate RC# to the system logic.
RC#	52	O	RC# to the SL82C461 for the CPU reset after arbitration with HLDA.
CPU INTERFACE			
ADS#	74	I	Address strobe. The falling edge indicates the start of a CPU cycle.
M/IO#	73	I	Memory/IO status from the CPU. High indicates a memory cycle and low indicates an IO cycle.
W/R#	71	I	Write/read status from the CPU. High indicates a write cycle and low indicates a read cycle.
D/C#	72	I	Data/code status from the CPU. High indicates data transfer and low indicates control operation.
READY1#	84	O	Ready output #1. The falling edge indicates the completion of the current CPU cycle. For system and WT4167 cycles, READY1# is activated in the same CPU cycle when SREADY# or NPREADY# is activated. This output is a push-pull drive.
READY2#	85	O	Ready output #2. For system and WT4167 cycles, READY1# is activated in the next CPU cycle when SREADY# or NPREADY# is activated. This output is a push-pull drive.
KEN#	49	O	In a 486 system this is the cache enable pin to the CPU. This pin also sets the write operation to zero wait state if a 4.7K pull-down resistor is connected, otherwise, the write operation has one wait state inserted.

BLAST#	45	I	Last burst cycle indicator from the 486 CPU. This pin should be tied to VDD in the 386DX/SX applications.
BRDY#	77	O	Burst ready output to the 486 CPU. This pin is a no connect pin in the 386DX/SX applications.
EADS#	48	O	External ADS output to the 486 CPU to force an internal cache invalidation cycle. This pin is a no connect pin in the 386DX/SX applications.
CPUTYPE	13	B	This pin indicates the CPU type installed in a system. In a 486 system, this pin is tied to VSS, In a 386DX/SX system, this pin is tied to VDD.
LOCAL BUS DEVICE			
LDEV#	26	I	This pin is connected to LDEV# of a Local Bus device. SL82C465 samples the LDEV# at the end of the first T2 or the second T2 depending upon the high/low status of Pin 46 during power-up.
LRDY#	30	I	This pin is connected to LRDY# of a local device which signals Haydn the termination of a Local Bus cycle. The LRDY# is ANDed with the 465 internal ready logics and then activates either READY1# or READY2# output pin of SL82C465 to send a ready signal to the CPU. READY1# is activated low immediately after detecting LRDY# active, while READY2# is activated low after being synchronized with the CPU clock.
T2_T3#	46	I	This pin is internally pulled high. SL82C465 samples this pin's Pull high or low status at power on reset period. A 'high' sets SL82C465 to sample the LDEV# signal at the end of first T2. A 'low' sets SL82C465 to sample the LDEV# at the end of second T2. When this pin is set at low every data write from the CPU will always be 1-wait-state.
LREQ#/CBOE3	44	I/O	Multifunction pin. When SBLAST# (pin 76) is pulled-up, this pin is the LREQ# signal from the VL-Bus master to gain the control of the VL-Bus. When SBLAST# (pin76) is pulled- down, this pin is the CBOE3 for the fourth cache bank.
LGNT#/CBOE2	50	O	Multifunction pin. When SBLAST#When SBLAST# (pin 76) is pulled-up, this pin is the LGNT# signal. When the VL-Bus master asserts LREQ#, the SL82C465 responds by asserting LGNT# to allow the VL-Bus master to have the control of the VL-Bus. When SBLAST# (pin76) is pulled- down, this pin is the CBOE2 for the third cache bank.

ADDRESS BUS

A0-7	7,6,98,97,96 95,94,93	I	Address inputs from the CPU for comparison with TA0-7. A4 always connects to pin CA20 of CPU. The connection of other bits depend on the cache configuration.
CA29,31	25,10	I	CPU address inputs for WT4167 decoding.
CA2,3	20,19	I	CPU address inputs for caches with larger line size.
KA2,3	18,17	O	Address converted from CA2,3 to drive the SL82C461.
BE0-3#	70,69,68,67	I	Byte enable input from the CPU.
A20G	43	I	Gate A20 input from the keyboard controller.
SA20G	42	B	Open source conversion of the A20G input from the keyboard controller. This allows wired-or connection with the fast Gate A20 output from the SL82C461.

TAG RAM CONTROL

TA0-7	9,8,100,99 89,88,87,86	B	Tag address bus connected to the data bus of the TAG RAM.
TAGOE#	37	O	Tag RAM output enable.
TAGWE#	24	O	Tag/valid RAM write enable.
VBI	5	I	Input from valid bit RAM to indicate valid status. This pin should tie high for combined tag/valid implementations.
VBO	31	O	Output to valid bit RAM. This pin is not used for combined tag/valid implementations.

CACHE CONTROL

SFLUSH#	36	I	Flush input from pin FLUSH# of the SL82C461 to force a cache miss.
SKEN#	1	I	Cacheable input pin from KEN# of SL82C461.
COE#	39	O	Cache RAM output enable. This pin is used when only one bank of cache is installed.
CBOE0-1#	38,63	O	Cache RAM output enable for cache bank 0, 1.
CCS0-1#	27,16	O	Cache RAM chip select for bank 0 and bank1.
KA3A	4	O	Used as KA3A to connect to the least significant address bit of bank 0 cache SRAM if 2 SRAM bank option is selected.

KA3B	92	O	Used as KA3B to connect to the least significant address bit of bank 1 cache SRAM if 2 SRAM bank option is selected.
CWE0-3#	23,21,11,2	O	Cache data write byte enable.
SBRDY#	81	I	Burst ready input from pin BRDY# of the SL82C461.
SBLAST#	76	O	Last burst cycle indicator to pin BLAST# of the SL82C461. The pull-up or pull-down status during power up decides the definition of pin 44(LREQ#/CBOE3) and pin 44(LGNT#/CBOE2).
NP INTERFACE			
F0F1CS	59	I	Input from the SL82C461 indicating an IO write to address F0h-F7h.
FERR#	58	I	**486 mode:** Input from the 486 CPU to indicate the occurrence of a NP error. **387 mode:** input from the ERROR# of 80387 to indicate that the current instruction has generated a non-mask error. In response, IRQ13# is generated and BUSY# and PREQ is forced active until a write to port F0h/F1h and/or NPRESET by the interrupt handler. **3167 mode:** not used.
IGNNE#/ BUSY#	61	O	**486 mode**: output to the 486 CPU to force the NP to ignore the NP error. **387 mode:** output to pin BUSY# of the CPU to indicate that the NP is not ready to accept a new instruction. On occurrence of NP errors, the signal is latched and held active until an occurrence of a write to port F0h or F1h or NPRESET. **3167 mode:** not used.
NPREQ/ WINTR	57	I	**387 mode:** input from pin PREQ of 80387 to indicate that the NP is requesting an operand transfer to or from memory by the CPU. **4167/3167 mode:** input from pin INTR of WT4167/3167 for interrupt request.
PREQ	62	O	**387 mode:** output to pin PEREQ of the CPU. This signal is returned to active on the occurrence of NP errors after NPBUSY# has gone inactive. A write to port F0h returns control of PREQ to directly follow NPREQ. **3167 mode:** not used.
WPRES#/ NPBUSY#	56	I	**4167/3167 mode:** input from pin PRES# of WT4167/3167 to detect its existence during power-on reset. **387/387SX mode:** input from pin BUSY# of 387/387SX co-processor to indicate that the NP is executing an instruction and is not ready to accept new one.

NPREADY#	83	I	Input from WT4167/WT3167/387/387SX ready output.
IRQ13#	60	O	Interrupt request 13 when there is an NP error.

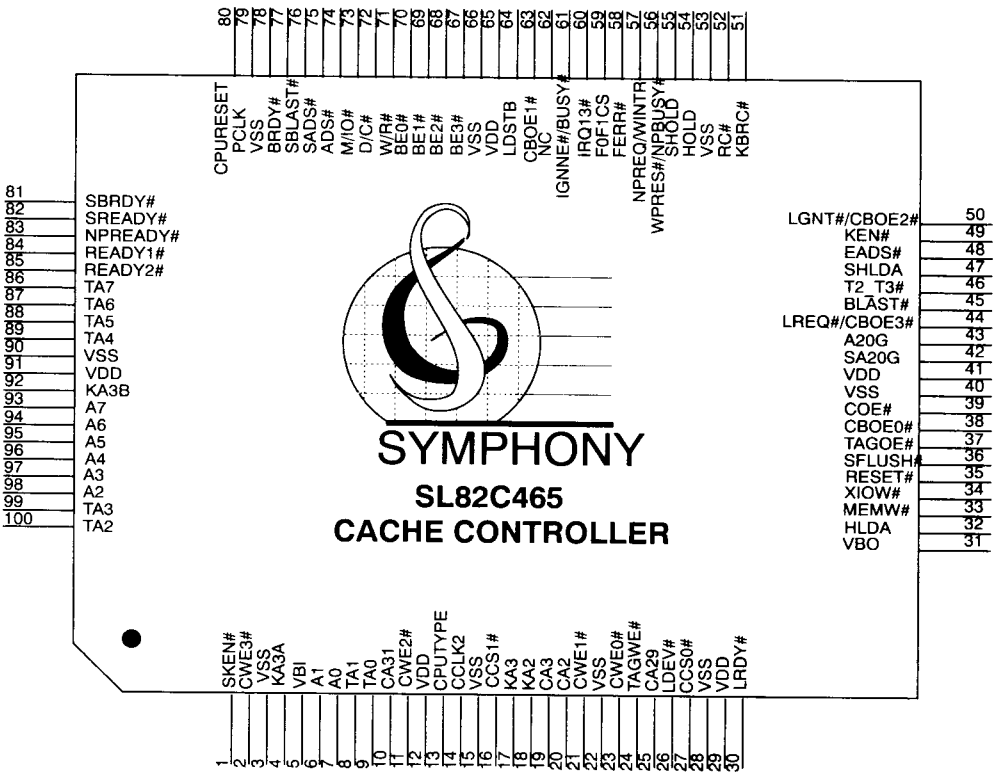
SYSTEM INTERFACE

LDSTB	64	O	Write buffer load strobe output to the SL82C362. When high, the CPU data is transparent. The data is latched into the buffer at the falling edge of LDSTB.
SADS#	75	O	System ADS# to the SL82C461.
SREADY#	82	I	System ready input from the SL82C461.
SHOLD	55	I	Hold request from the SL82C362.
HOLD	54	O	Hold request to the CPU
HLDA	32	I	Hold acknowledgment from the CPU in response to a hold request.
SHLDA	47	O	Hold acknowledgment to the system logic.
MEMW#	33	I	Memory write command for cache snooping.
XIOW#	34	I	IO write during power-on period for reading the jumper setting.

POWER AND GROUND

VDD	12,29,41,65,91
VSS	3,15,22,28,40,53,66,78,90

SL82C465 Pin Diagram



3 82C465 Electrical and Timing Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient Operating Temperature	0	70	Degree C
Storage Temperature	-65	125	Degree C
Supply Voltage (Vdd)	-0.5	7.0	V
Input Voltage	-0.5	Vdd+0.5	V
Output Voltage	-0.5	Vdd+0.5	V

3.2 DC Characteristics (Ta=0-70 degree C, Vdd=5V+/-5%)

Parameter	Min.	Typ.*	Max.	Unit
Input low level (TTL)	-0.5	---	0.8	V
Input high level (TTL)	2.2	---	5.5	V
Output low voltage				
4mA buffer, IOL=4mA	---	0.15	0.4	V
8mA buffer, IOL=8mA	---	0.18	0.4	V
12mA buffer, IOL=12mA	---	0.18	0.4	V
16mA buffer, IOL=16mA	---	0.17	0.4	V
Output high voltage				
4mA buffer, IOL=4mA	3.0	4.54	---	V
8mA buffer, IOL=8mA	3.0	4.44	---	V
12mA buffer, IOL=12mA	3.0	4.46	---	V
16mA buffer, IOL=16mA	3.0	4.46	---	V
Input low current	-10	-0.01	---	uA
with 50K pullup resistor	-250	-80	-20	uA
Input high current	---	0.01	10	uA
Tristate output off current low	-10	-0.01	---	uA
Tristate output off current high	---	0.01	10	uA
Input capacitance**	---	10	---	pF
Output capacitance**	---	10	---	pF
I/O capacitance**	---	10	---	pF

* Typical is under the condition of Vdd=5.0+/-5% and Ta=25 degree C.
** Capacitance includes the capacitance of I/O cell plus package pin.

3.3 AC Characteristics (Ta=0-70 degree C, Vdd=5V+/-5%; Unit=ns)

Description	Symbol	Min.	Typ.	Max.
CACHE READ HIT CYCLE				
READY1# fall from CCLK rise	t100	4		12
READY1# rise from CCLK rise	t101	7		20
READY2# fall from CCLK rise	t102	4		12
READY2# rise from CCLK rise	t103	7		18
COE# fall from ADS# fall	t104	3		10
COE# rise from CCLK rise	t105	4		15
SKEN# setup to TA valid	t107	0		
SKEN# hold from CCLK rise	t108	0		
SFLUSH# setup to TA valid	t109	0		
SFLUSH# hold from CCLK rise	t110	0		
VBI setup to TA valid	t111	0		
VBI hold from CCLK rise	t112	0		
CBOE#0-3 fall from CCLK rise	t113	3		12
CBOE#0-3 rise from CCLK rise	t114	3		12
KA3A(B) valid from ADS# fall	t118	4		12
KA3A(B) valid from CCLK rise	t119	4		12
BRDY# fall from TA valid	t120	4		11
BRDY# rise from CCLK rise	t121	7		20
CACHE READ MISS CYCLE				
SADS# fall from CCLK rise	t200	3		14
SADS# fall from TA valid	t201	4		12
SADS# rise from CCLK rise	t202	3		13
CWE#0-3 fall from CCLK rise	t203	3		10
CWE#0-3 rise from CCLK rise	t204	2		9
READY1# fall from SREADY#	t205	2		8
SREADY# setup to CCLK rise	t207	4		
SREADY# hold from CCLK rise	t208	0		
VBO rise from CCLK rise	t209	4		17
VBO fall from CCLK rise	t210	4		17
TA valid from TAGWE# fall	t212	3		12
TA float from TAGWE# rise	t213	3		13
TAGOE# rise from CCLK rise	t214	5		17
TAGOE# fall from CCLK rise	t215	5		19
TAGWE# fall from CCLK rise	t216	4		15
TAGWE# rise from CCLK rise	t217	4		15
CCS#0-3 rise from CCLK rise	t218	4		15

CCS#0-3 fall from CCLK rise	t219	4	15
SBRDY# setup to CCLK rise	t220	7	
SBRDY# hold from CCLK rise	t221	0	
KA2/3 valid from ADS# fall	t225	3	9
KA2/3 valid from CCLK rise	t226	3	9
CCS#0-3 valid from CCLK rise	t227	2	8
READY1# fall from SBRDY# fall	t230	2	8
BRDY# fall from SBRDY# fall	t240	2	8
BRDY# rise from CCLK rise	t241	7	15
BRDY# fall from CCLK rise	t242	4	15
KEN# fall from CCLK rise	t245	4	15
KEN# rise from CCLK rise	t246	7	15
KEN# delayed from SKEN#	t247		10

WRITE CYCLE

READY1# fall from CCLK rise	t301	4	13
LDSTB rise from CCLK rise	t302	3	11
LDSTB fall from CCLK rise	t303	3	12
SADS# fall from ADS# fall	t304	2	8
SADS# fall from SREADY# fall	t305	2	8

DMA/MASTER CYCLE

MEMW# setup to CCLK rise	t401	5	20
TAGOE# rise from CCLK rise	t402	4	17
TAGOE# fall from CCLK rise	t403	4	17
TAGWE# fall from CCLK rise	t404	4	15
TAGWE# rise from CCLK rise	t405	4	15
TA valid from TAGWE# fall	t406	3	12
TA float from TAGWE# rise	t407	3	13
CWE#0-3 fall from CCLK rise	t408	3	10
CWE#0-3 rise from CCLK rise	t409	2	9
EADS# fall from CCLK rise	t410	5	20
EADS# rise from CCLK rise	t411	7	20
SHOLD setup to PCLK rise	t412	7	
SHOLD hold to PCLK rise	t413	0	
HOLD rise from PCLK rise	t414	5	15
HOLD fall from PCLK rise	t415	4	12

COPROCESSOR CYCLE

IRQ13# rise from FERR# fall	t501	7	18
IRQ13# fall from F0F1CS# fall	t502	4	15
IGNNE# fall from F1F0CS# fall	t503	4	15
IGNNE# rise from FERR# rise	t504	7	18

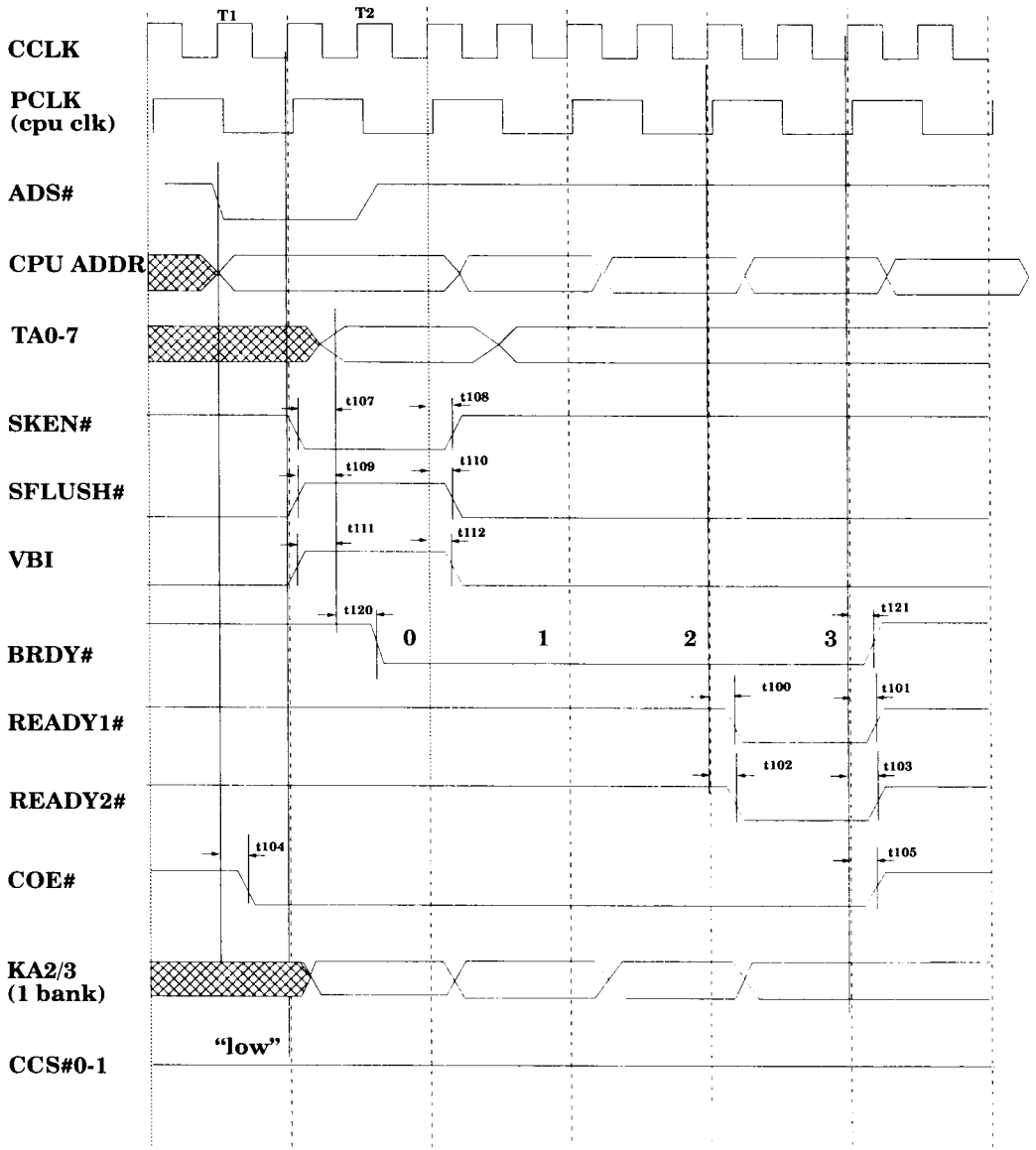
NPREADY# setup to CCLK rise	t505	4	
NPREADY# hold to CCLK rise	t506	0	
READY1# delayed from NPREADY#	t507	4	10

LOCAL BUS CYCLE

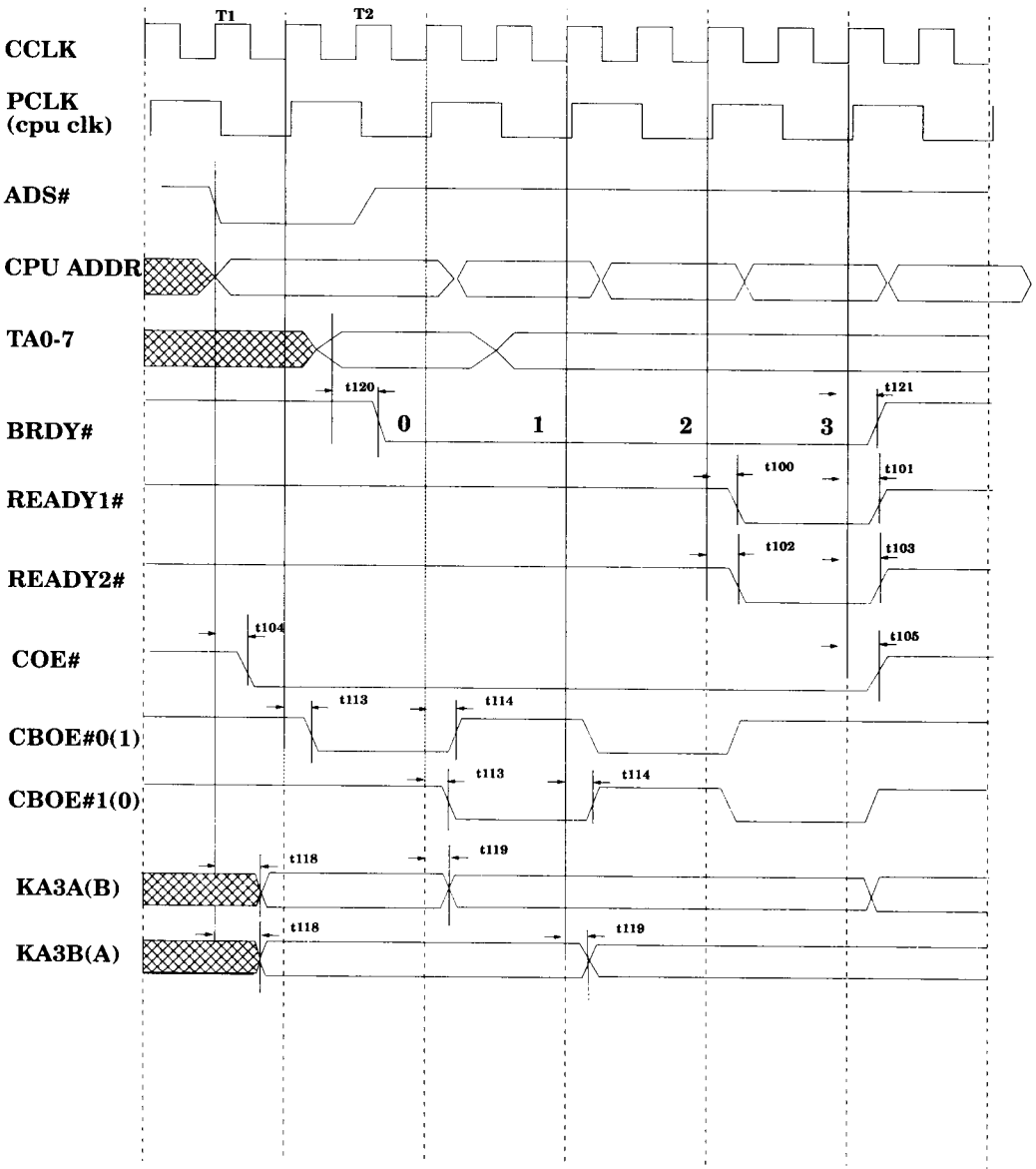
LDEV# delayed from CA, CMD	t601		25
LDEV# setup time to LCLK	t602	5	
LDEV# hold time from CCLK	t603	3	
LRDY# setup time from LCLK	t604	5	
LRDY# hold time from LCLK	t605	3	
CD[31-0] driven from end of T1	t606	5+1LCLK	
CD[31-0] released from LCLK	t607		12
READY1# dealyed from LRDY#	t608		10
CPU READY# setup time	t609	refer CPU spec.	
CPU READY# hold time	t610	refer CPU spec.	

The following loadings are assumed for the above timing specifications.
READY1#, READY2#, BRDY#, SADS#, LDSTB: 40pf
Other signals: 50pf

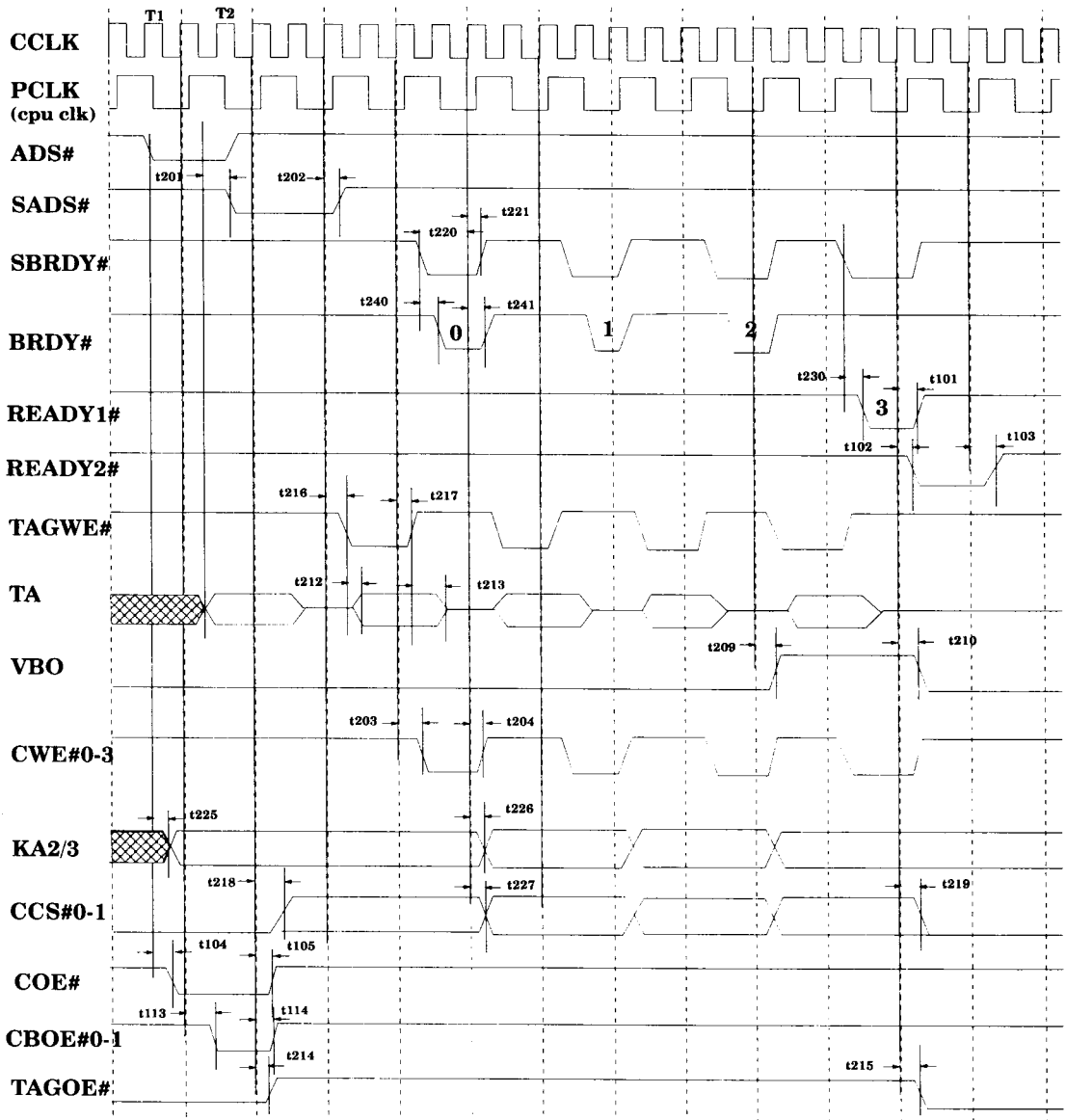
486 mode, Cache Read Hit 2-1-1-1 (2X clock, 1 bank)



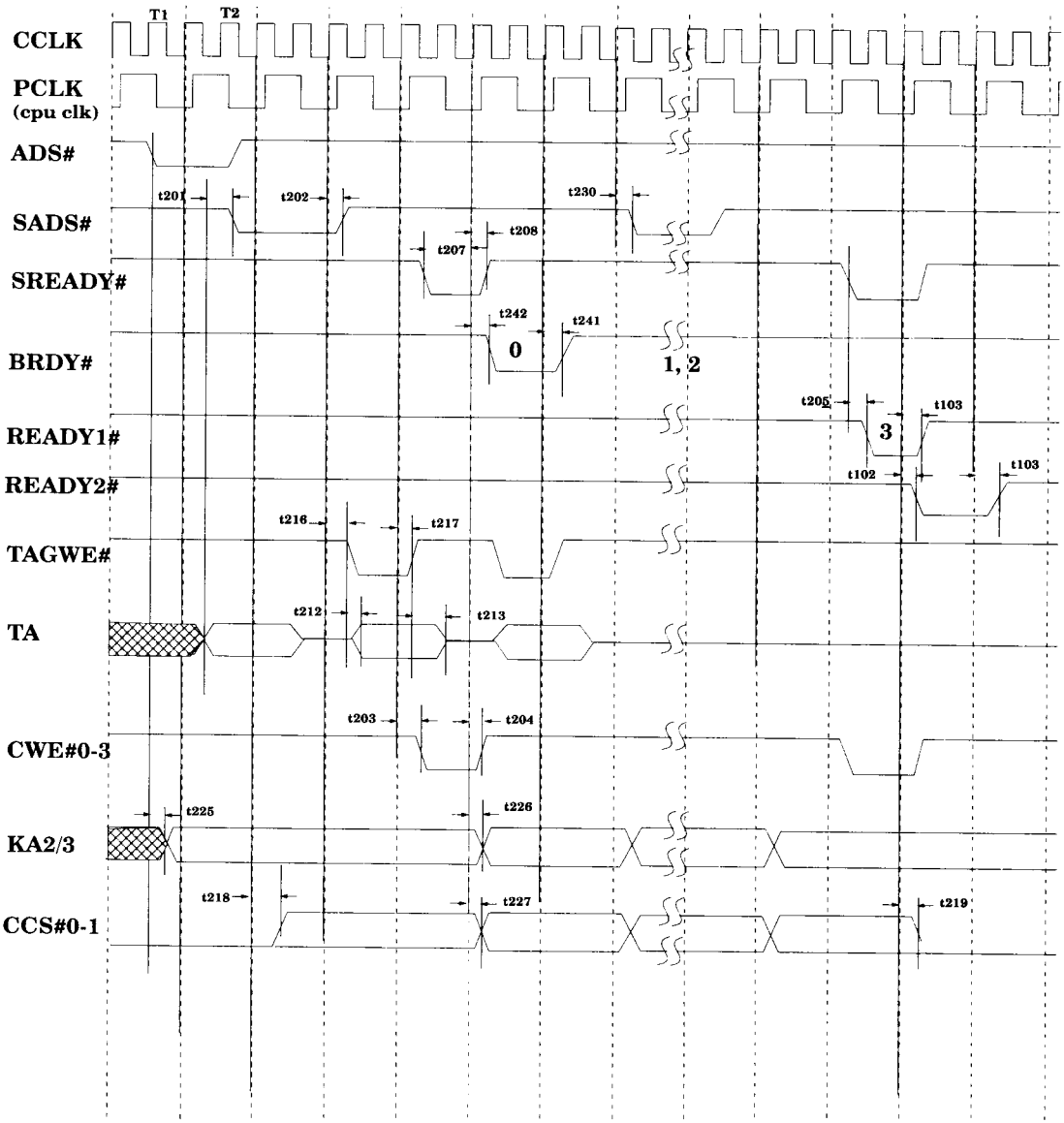
486 mode, Cache Read Hit 2-1-1-1 (2X clock, 2 bank)



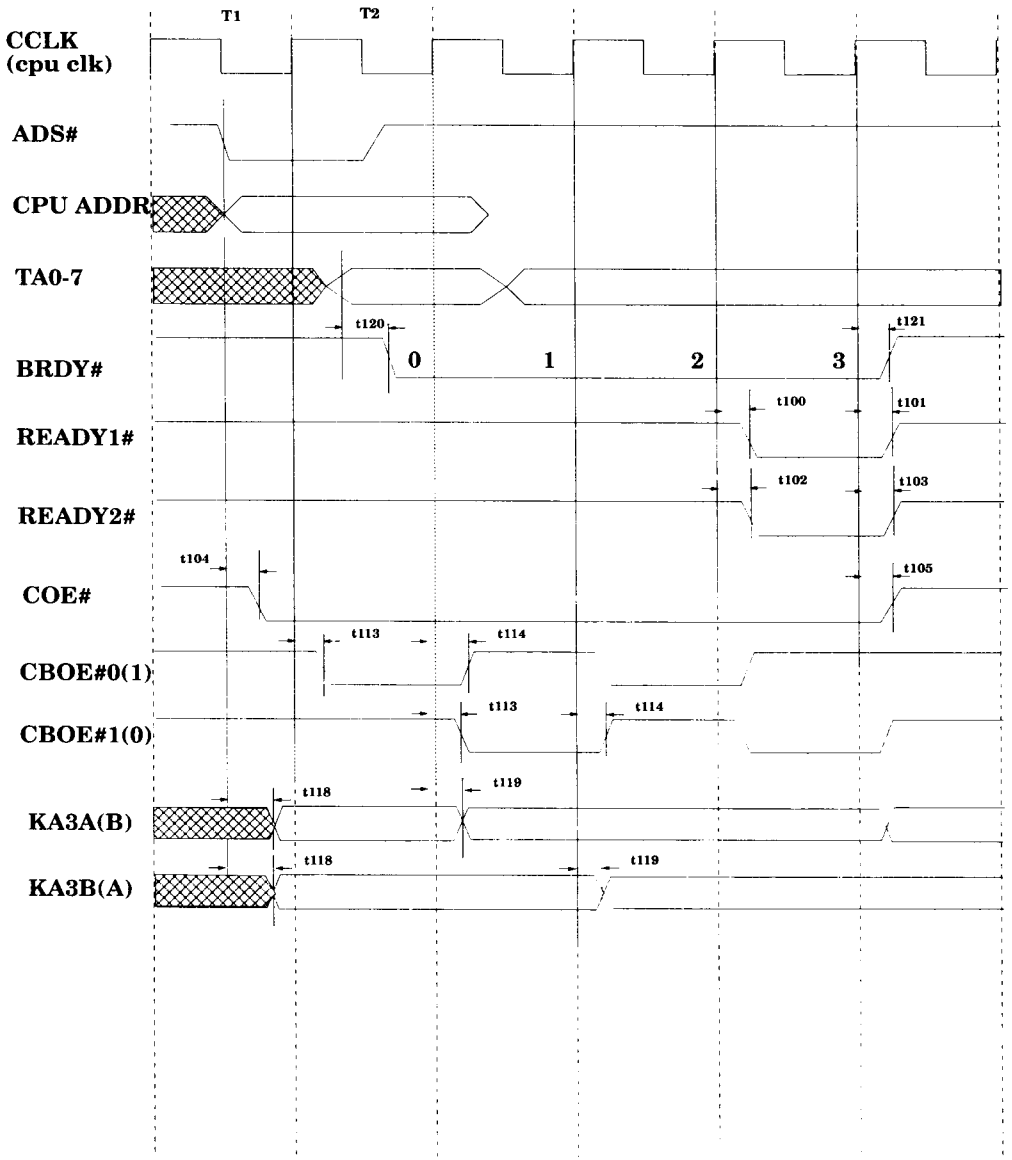
486 mode, Cache Read Miss, burst fill (2X clock)



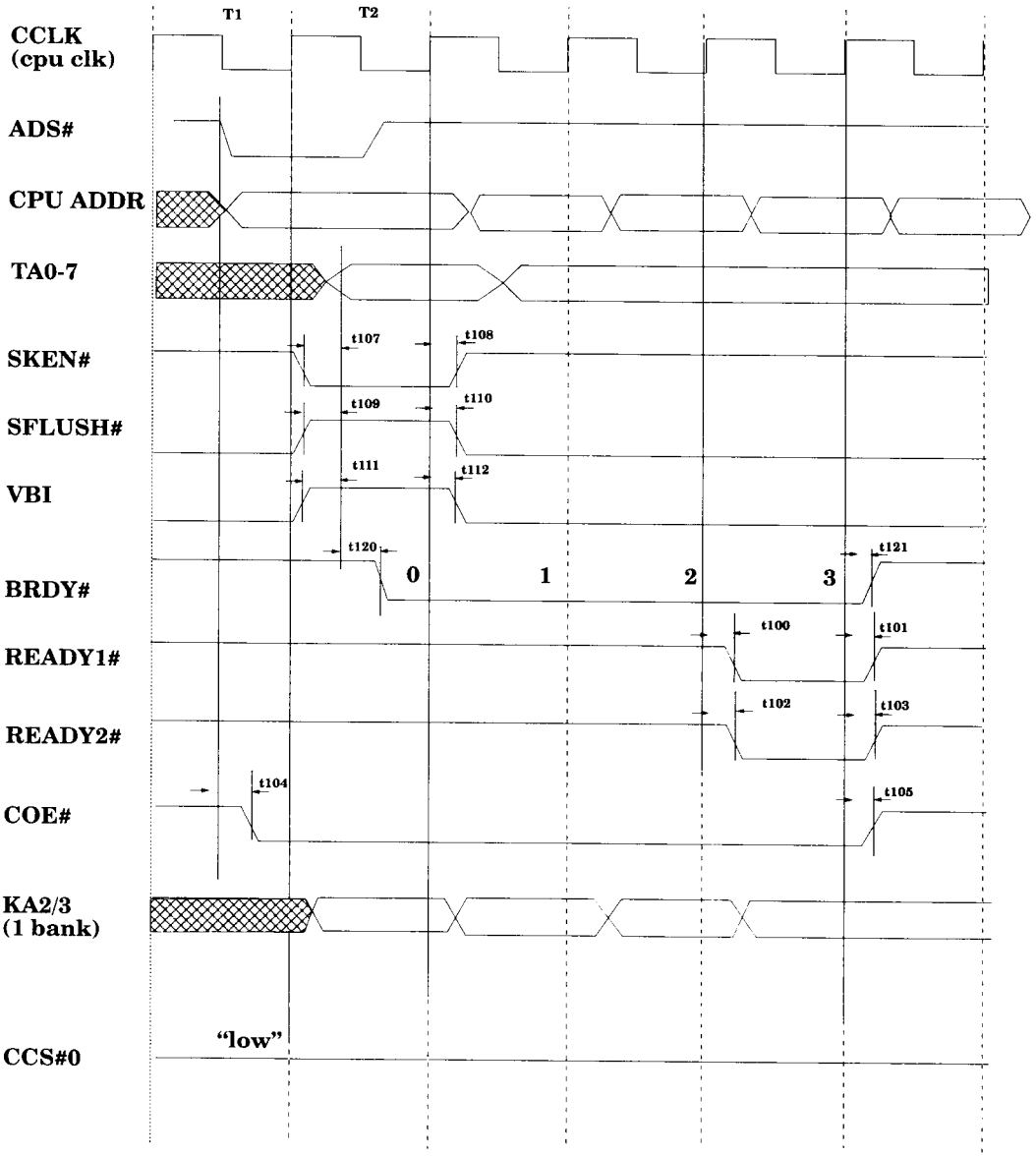
486 mode, Cache Read Miss, non-burst fill (2X clock)



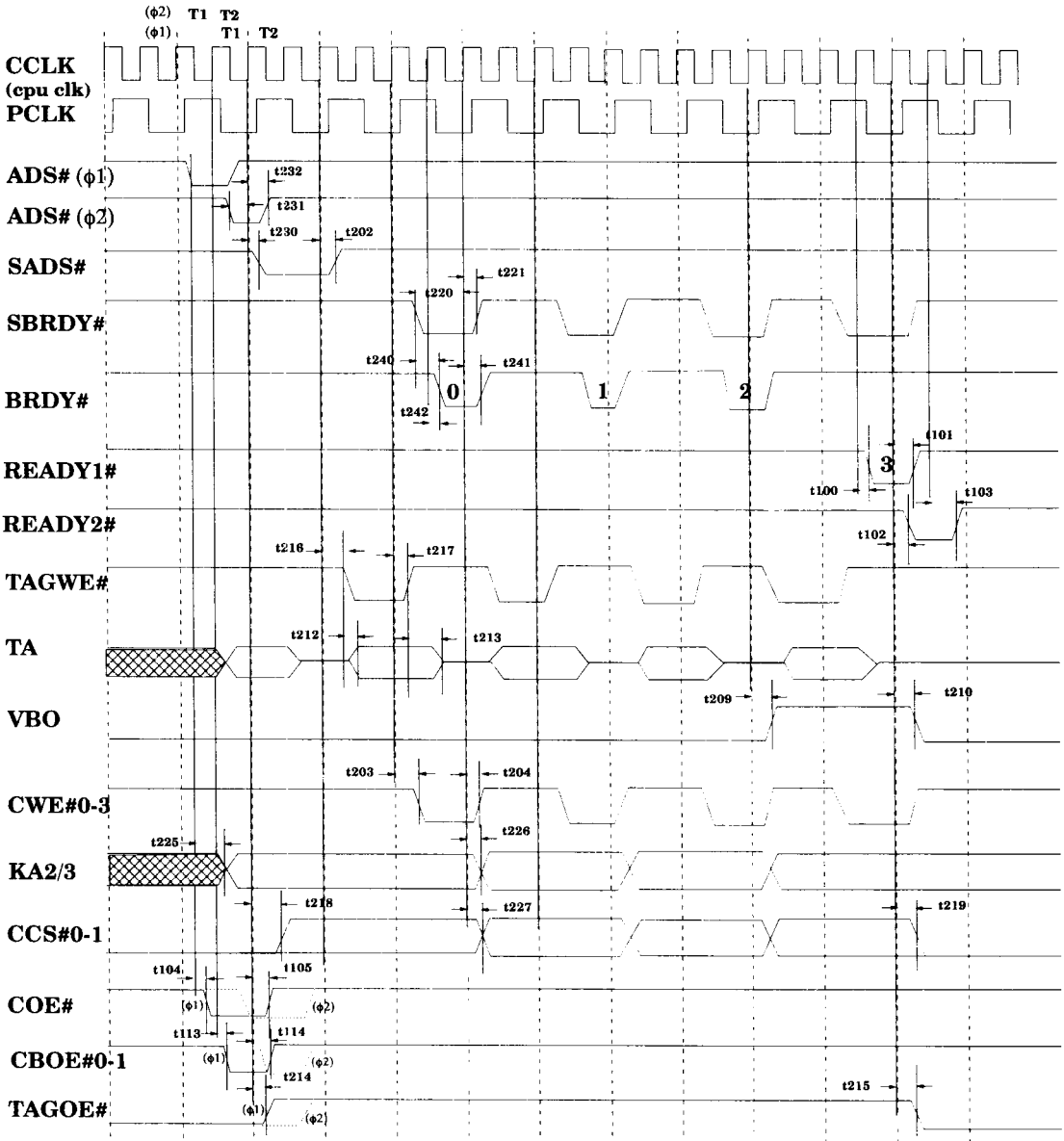
486 mode, Cache Read Hit 2-1-1-1 (1X clock, 2 bank)



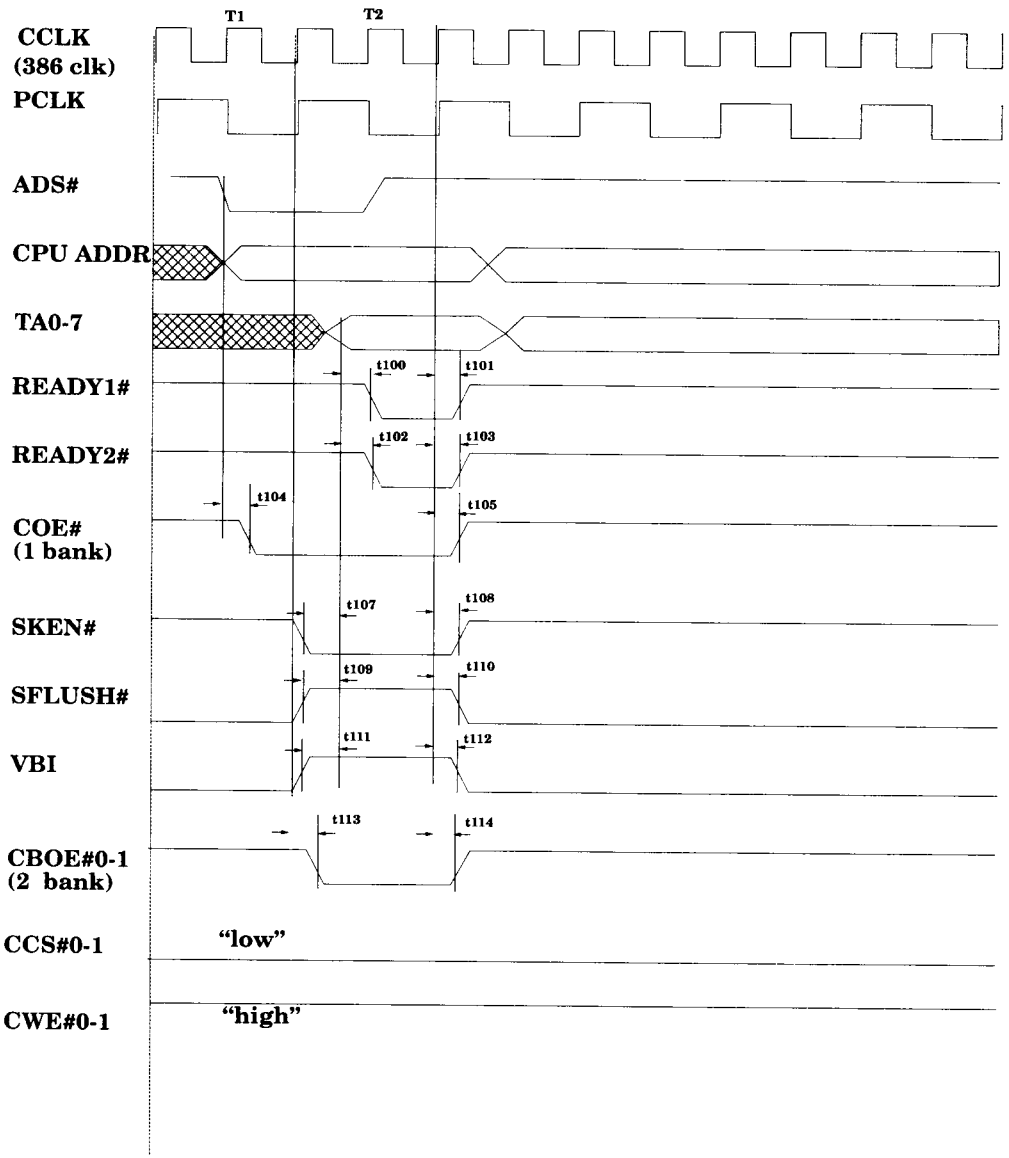
486 mode, Cache Read Hit 2-1-1-1 (1X clock, 1 bank)



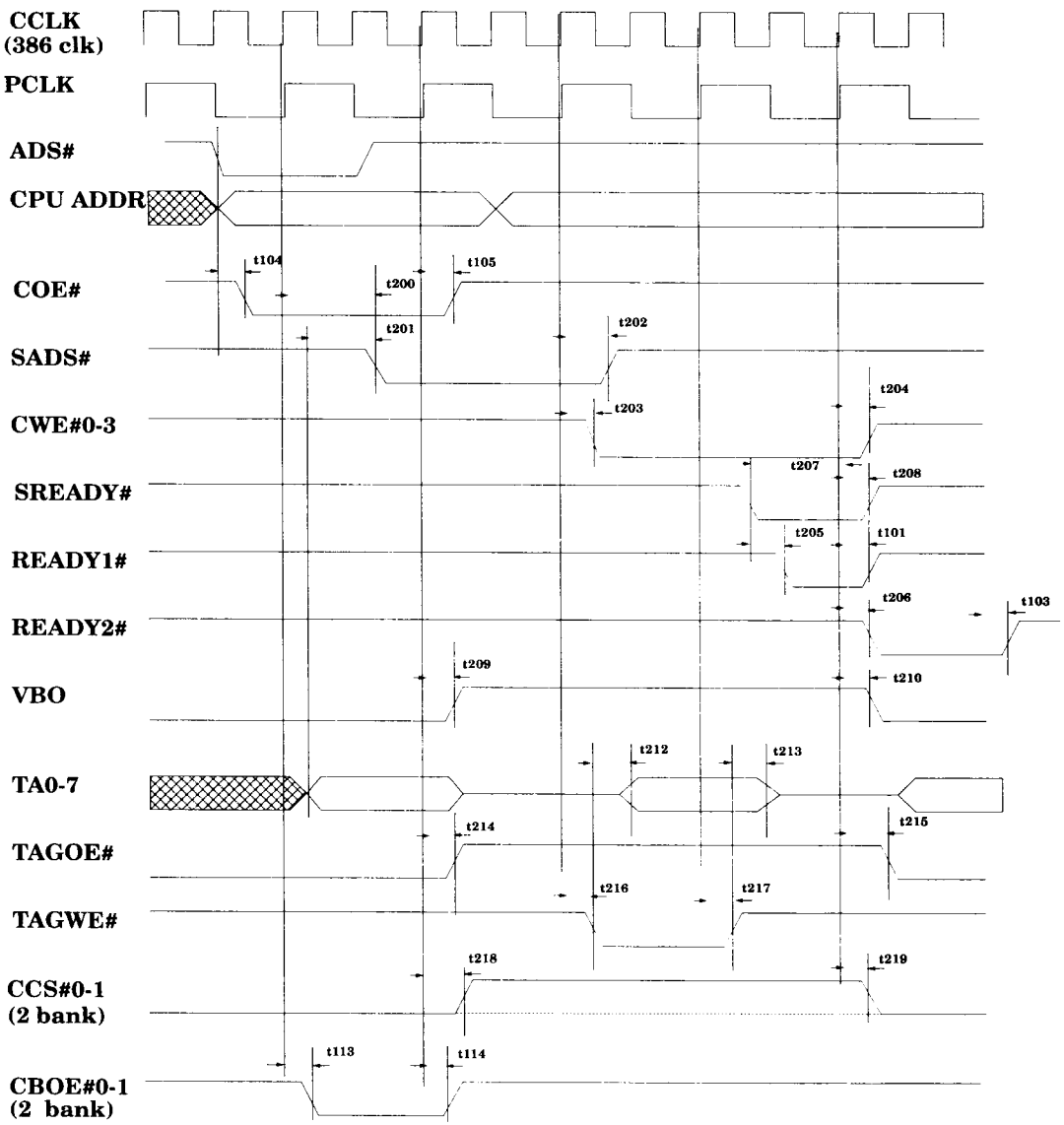
486 mode, Cache Read Miss, burst fill (1X clock)



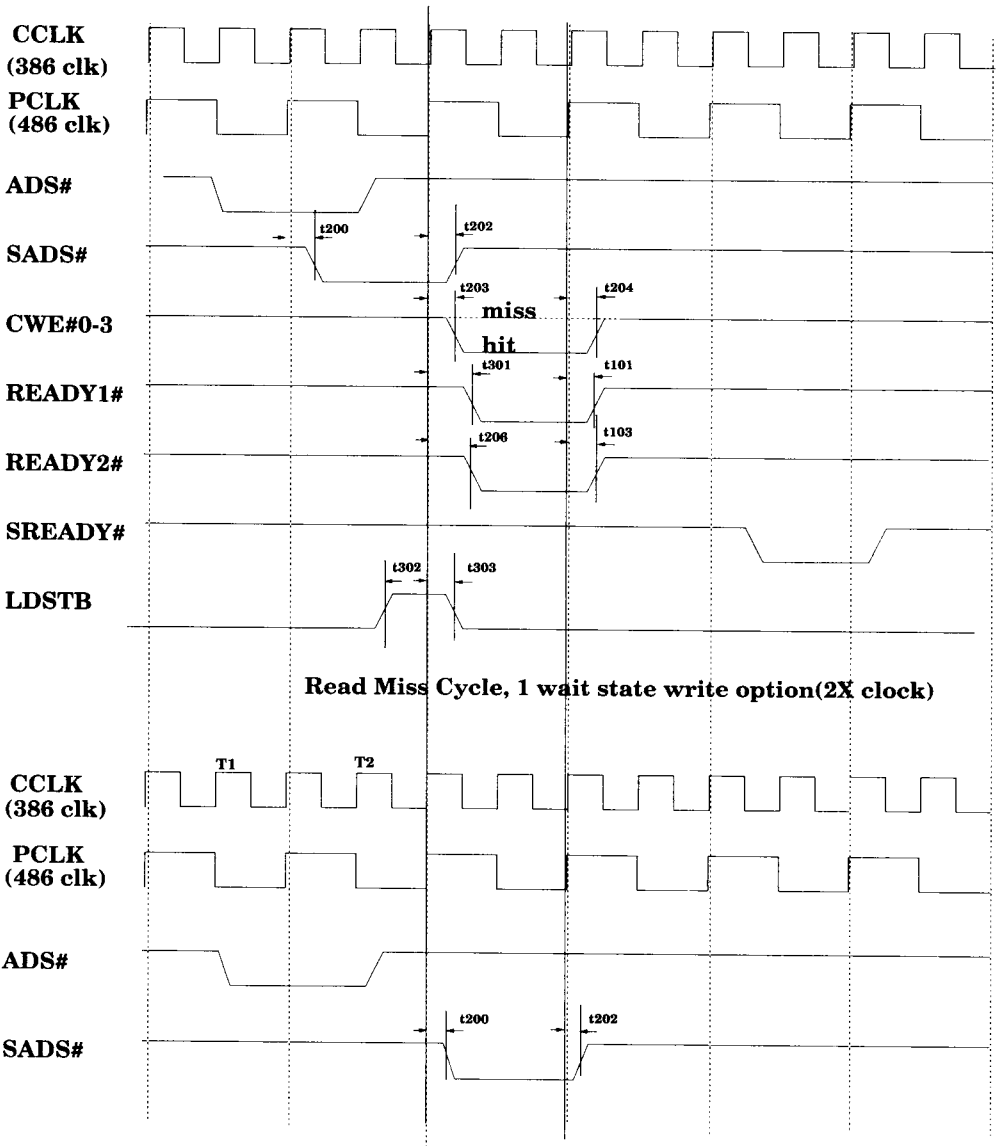
386 mode, Cache Read Hit, Non-Burst Fill



386 mode, Cache Read Miss - Line Size = 1 Dword

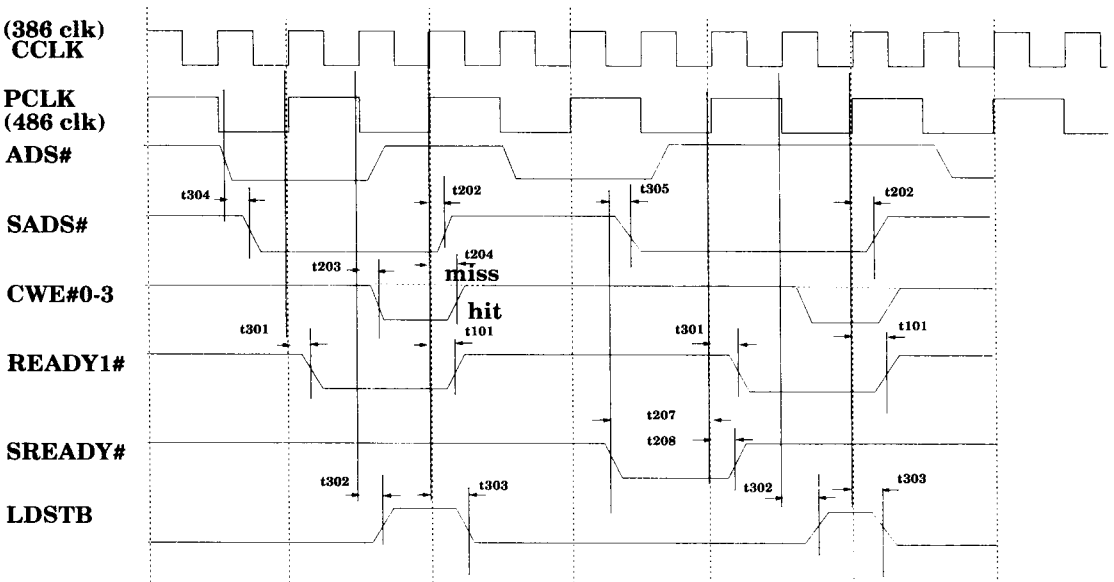


Write Cycle, 1 wait state(2X clock)

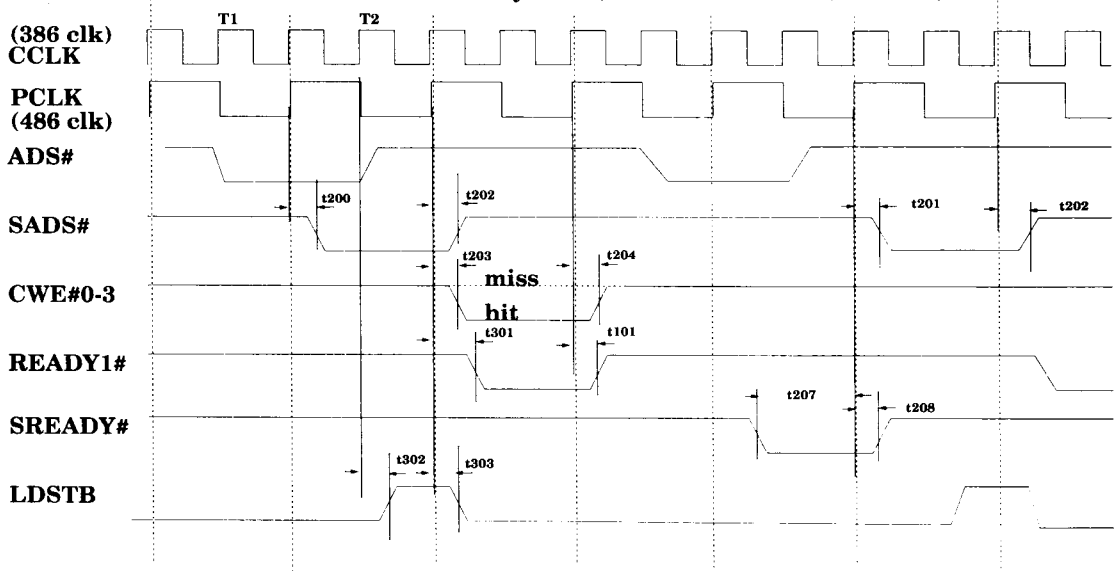


Read Miss Cycle, 1 wait state write option(2X clock)

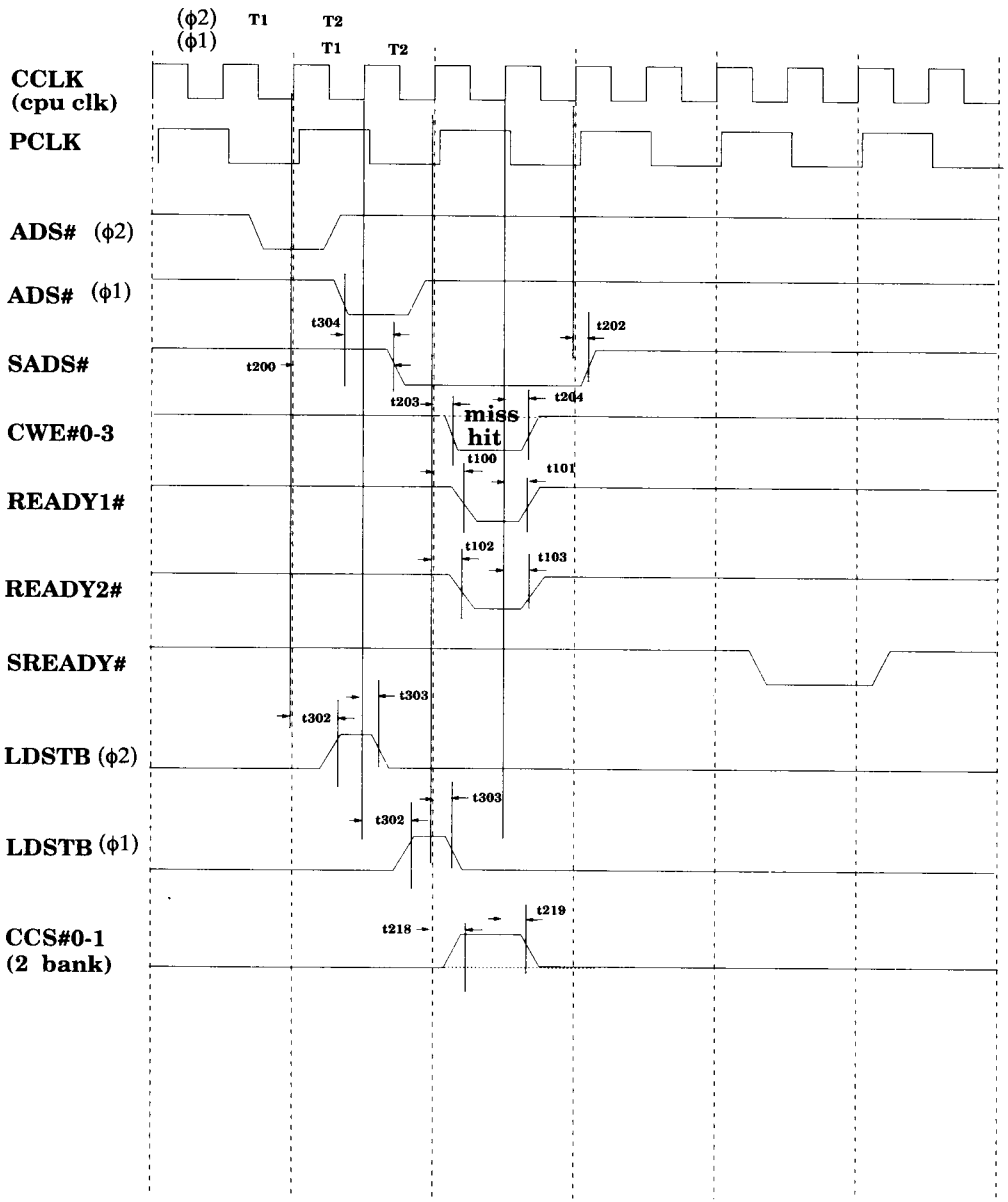
Buffered write followed by write, 0 wait state write(2X clock)



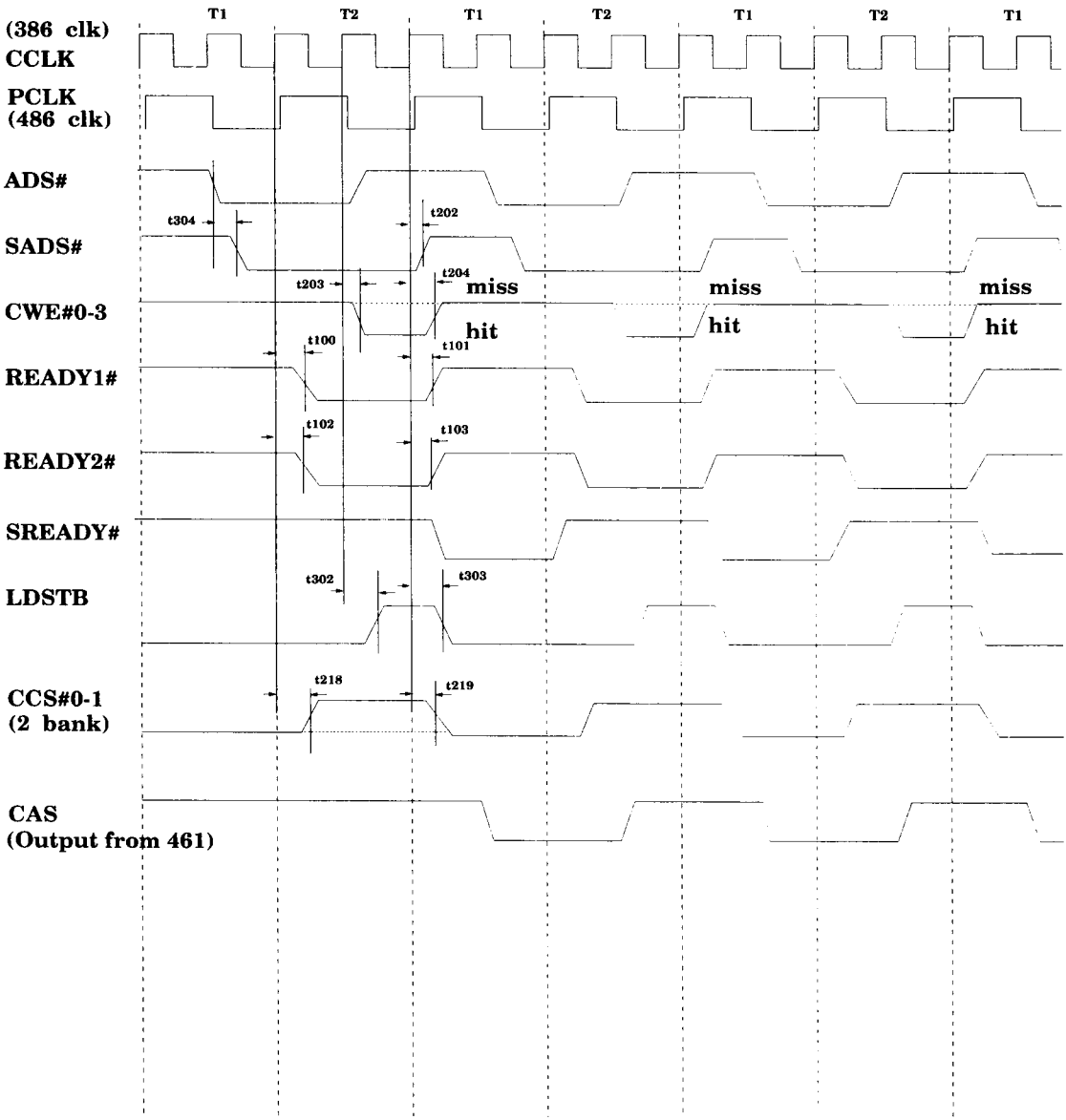
Buffered write followed by write, 1 wait state write(2X clock)



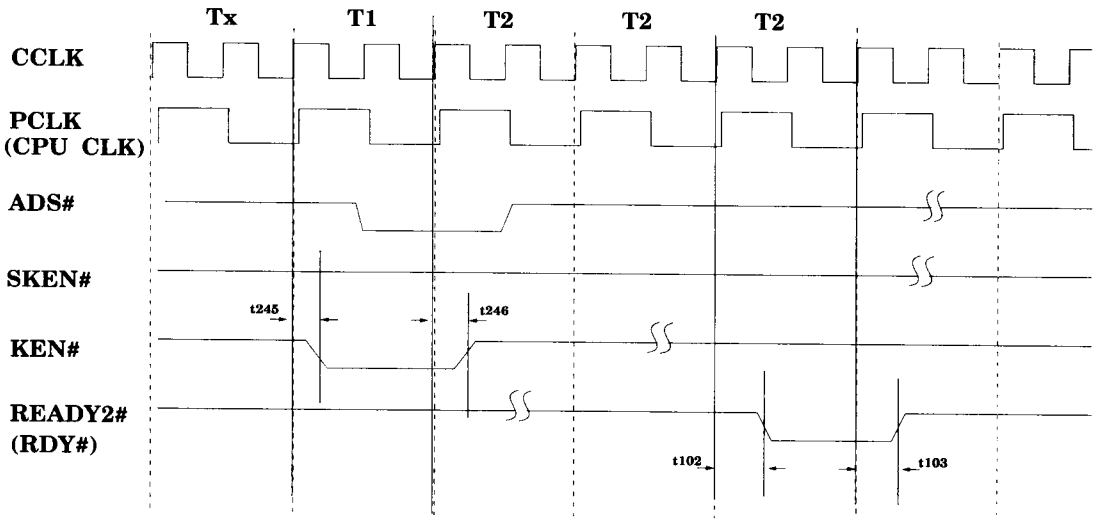
Write Cycle, 1 wait state (1X clock)



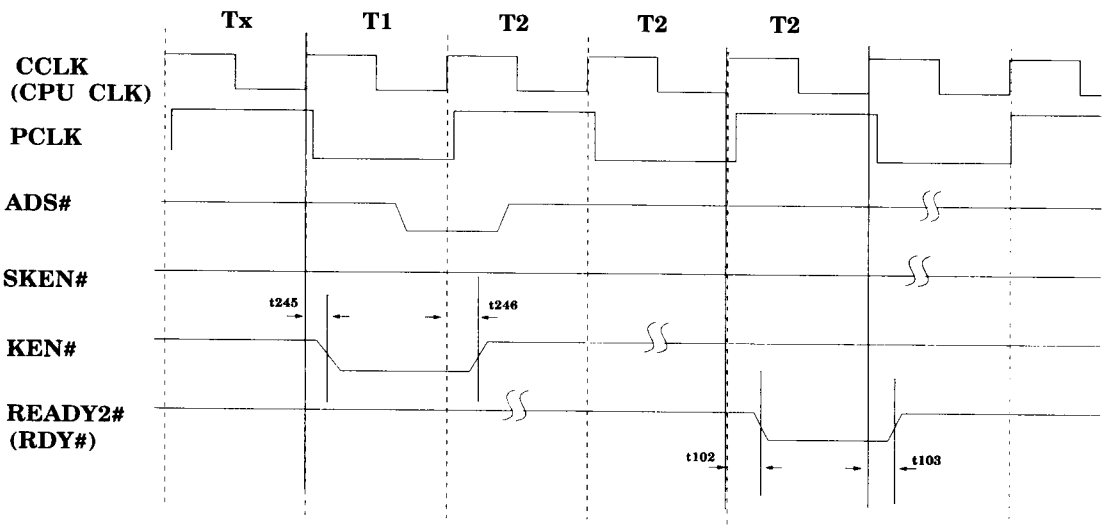
Write Cycle, Pipelined, 0 wait state (2X clock)



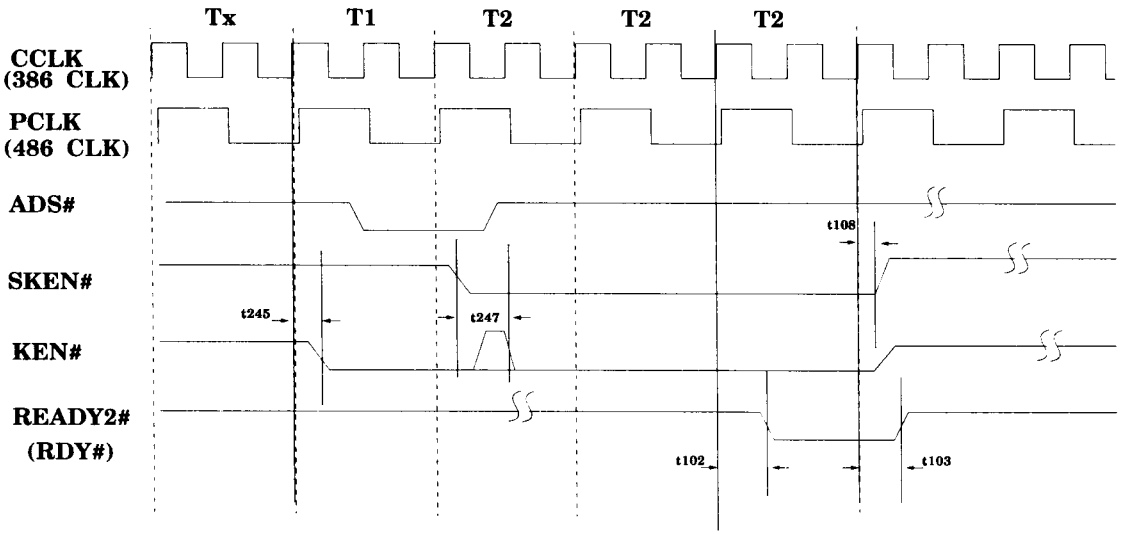
Non-Cacheable Read KEN#(2X Cycle)



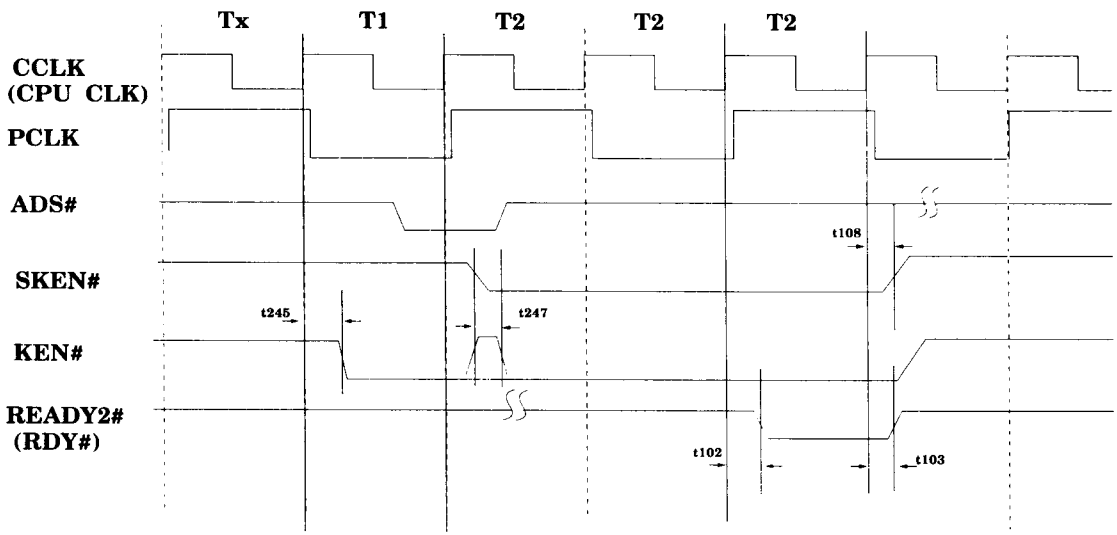
Non-Cacheable Read KEN#(1X Cycle)



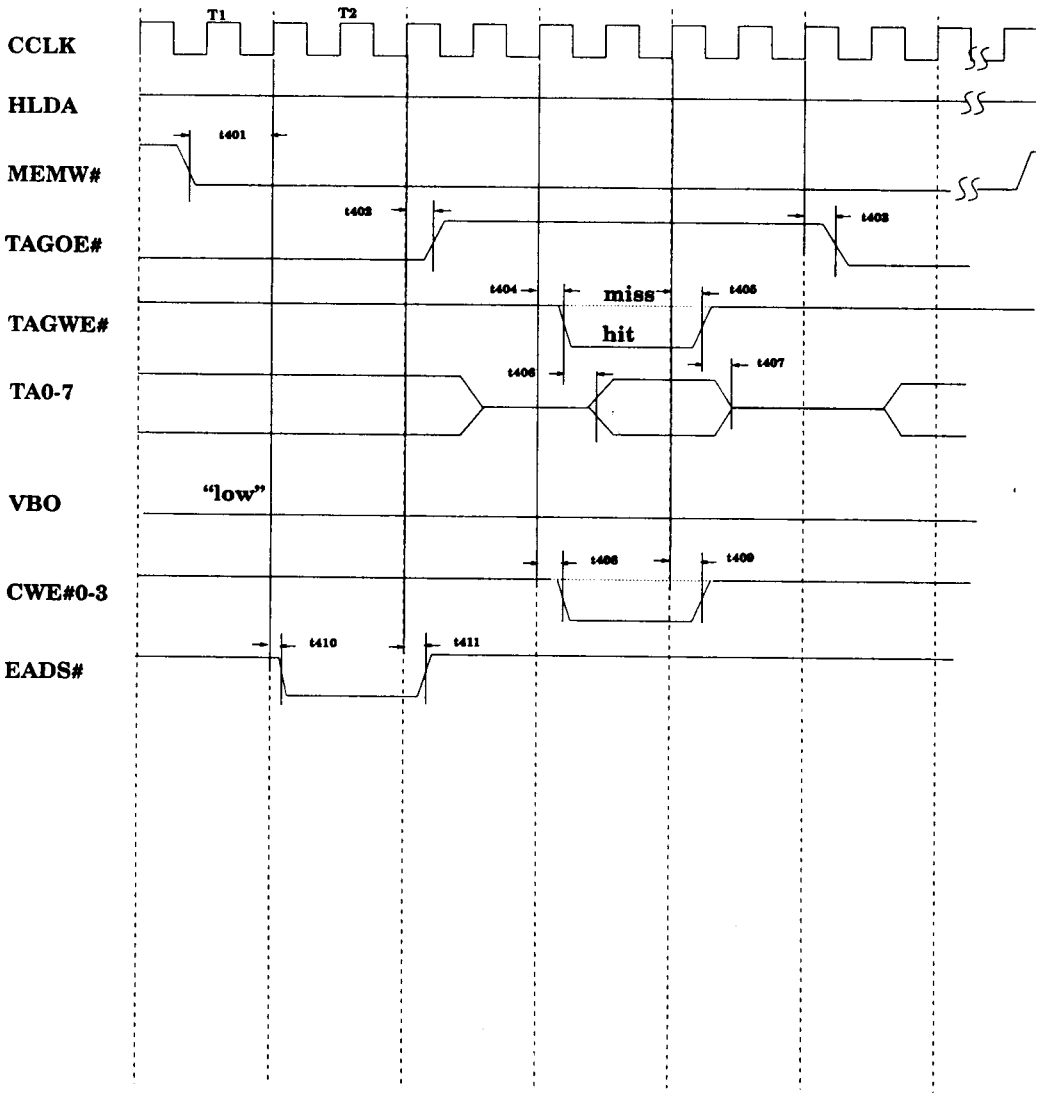
Cacheable Read KEN#(2X Cycle)



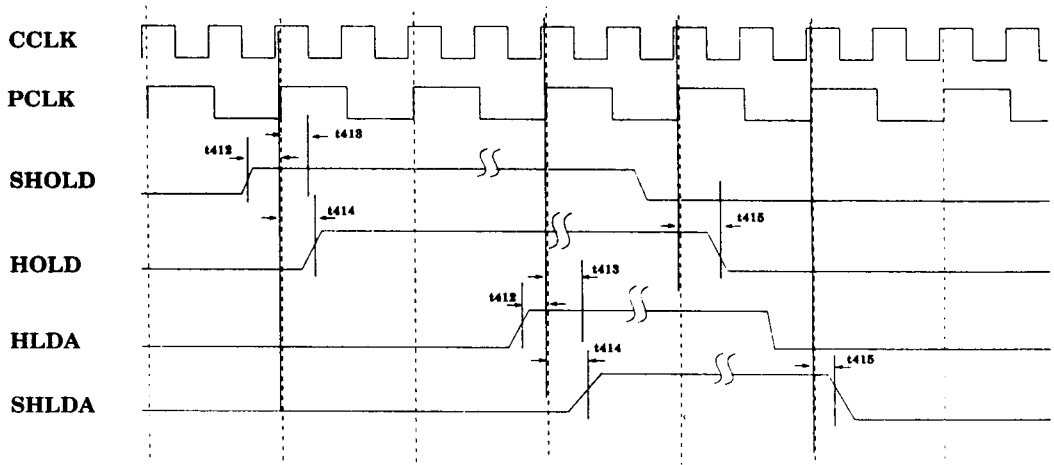
Cacheable Read KEN#(1X Cycle)



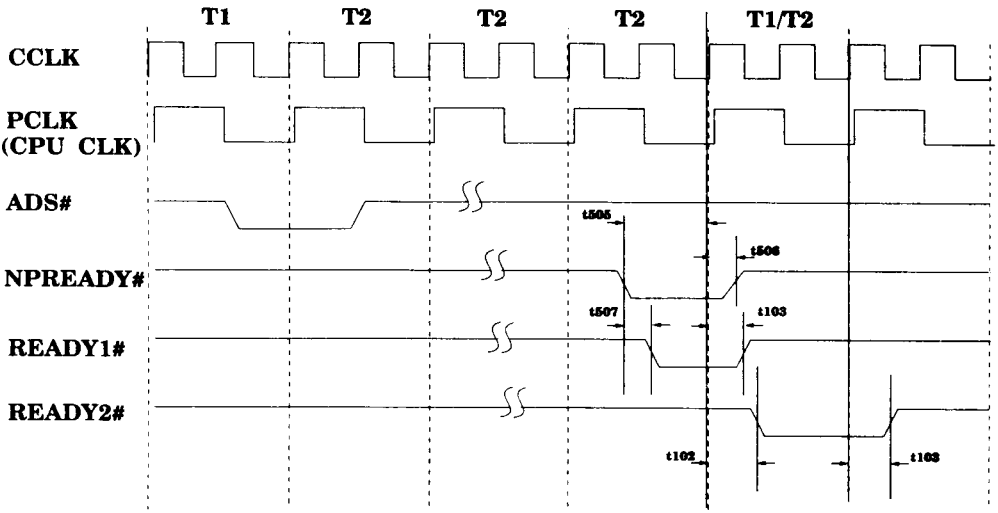
DMA/Master Memory Write



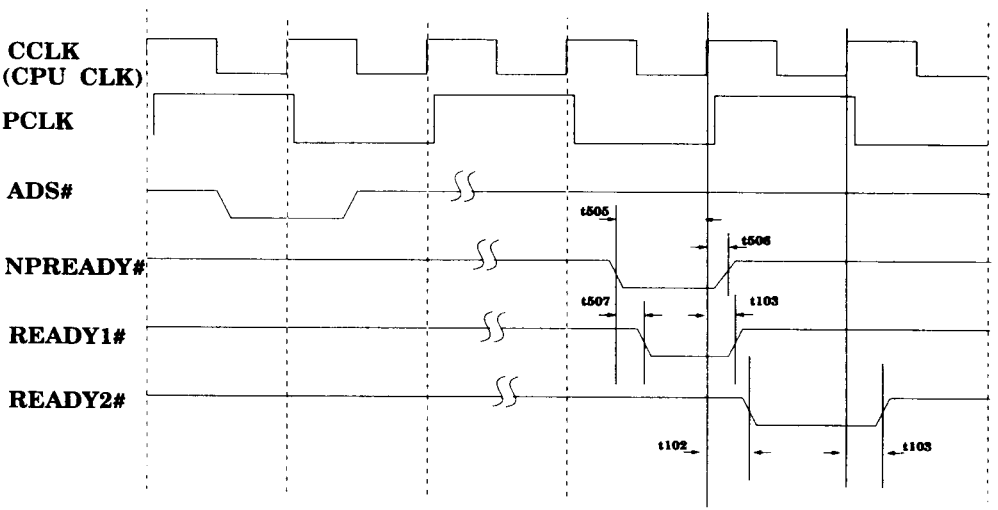
HOLD /HLDA CYCLE



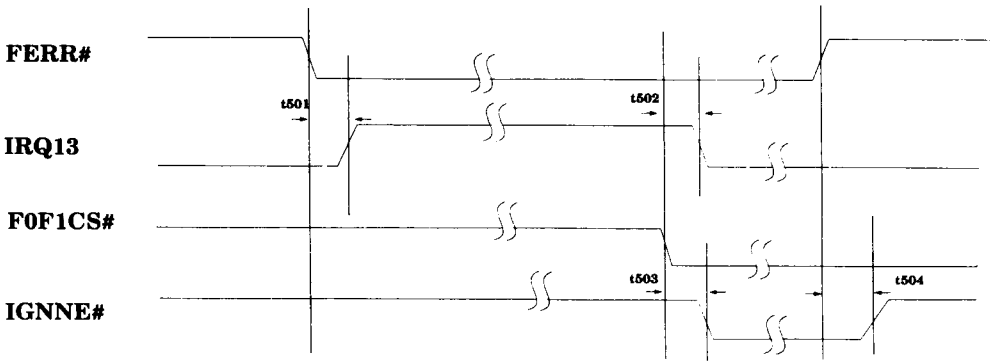
Coprocessor 2X Cycle



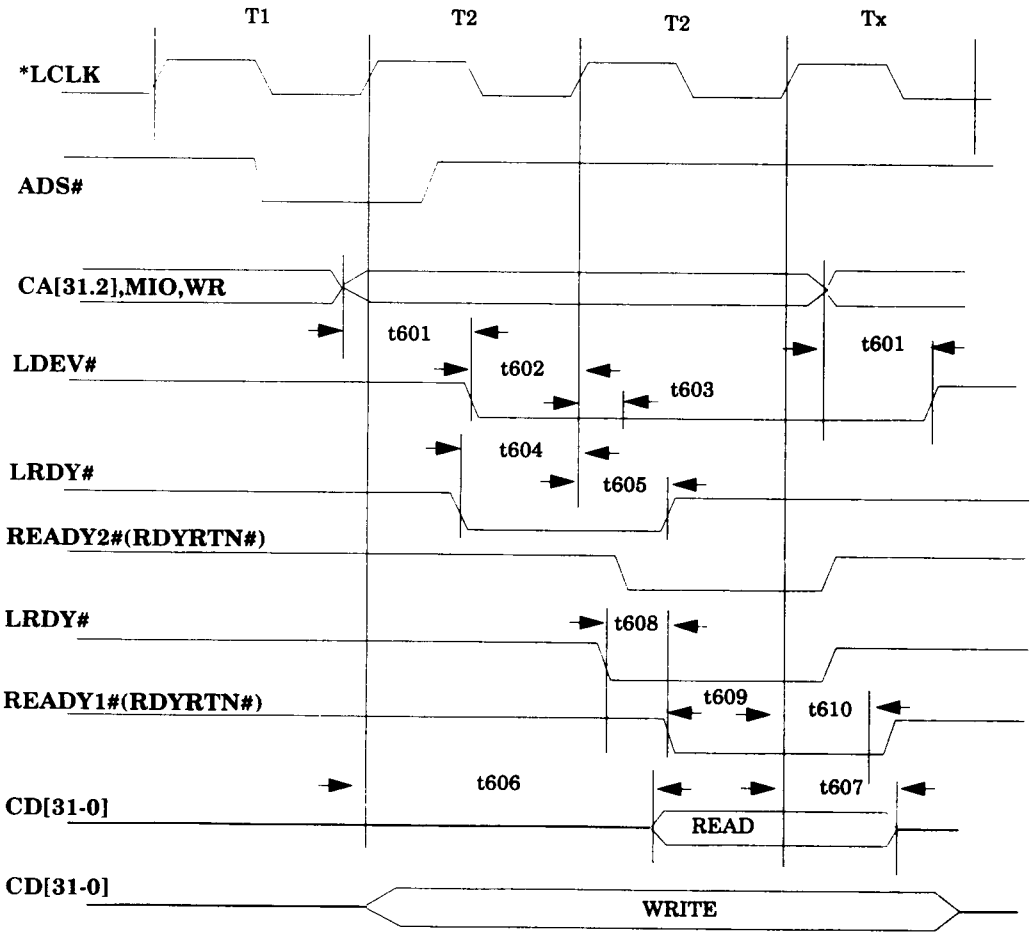
Coprocessor 1X Cycle



COPROCESSOR ERROR CYCLE

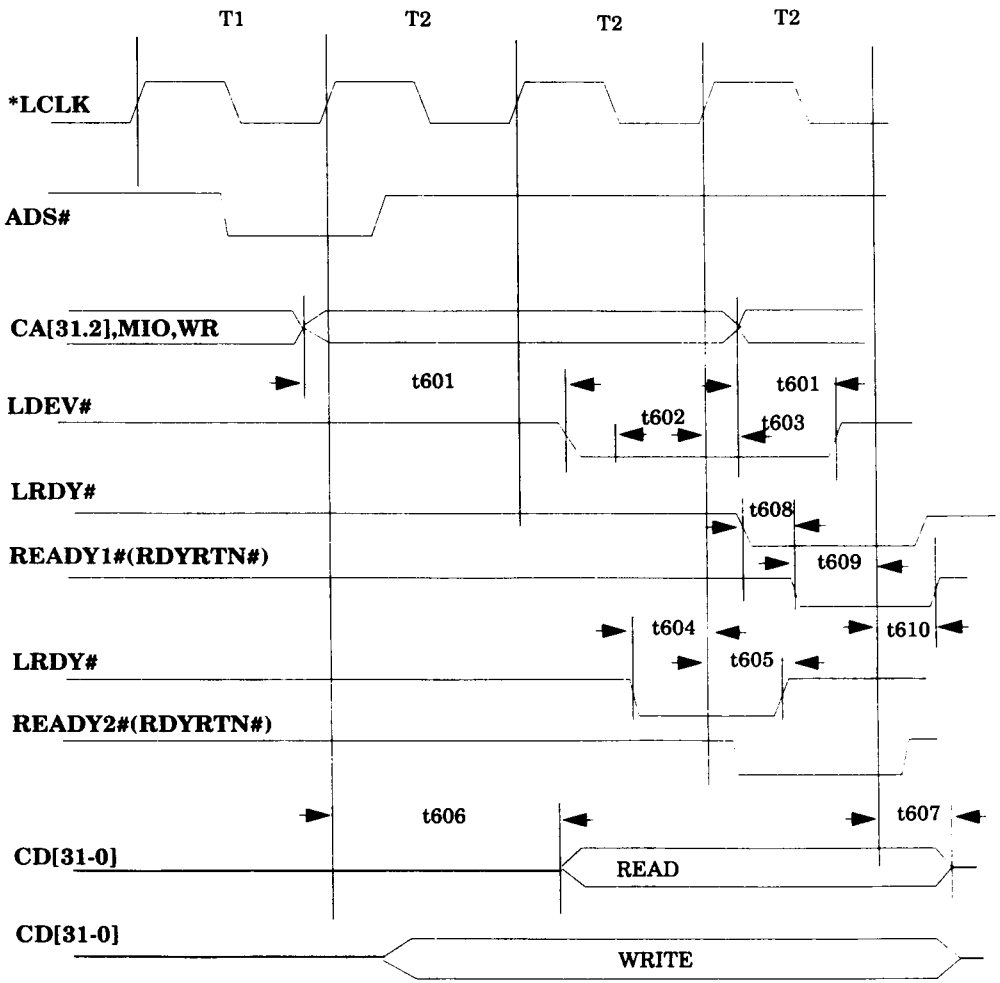


LOCAL BUS CYCLE (T2 mode)



* LCLK = CCLK at 1X clock
LCLK = PCLK at 2X clock

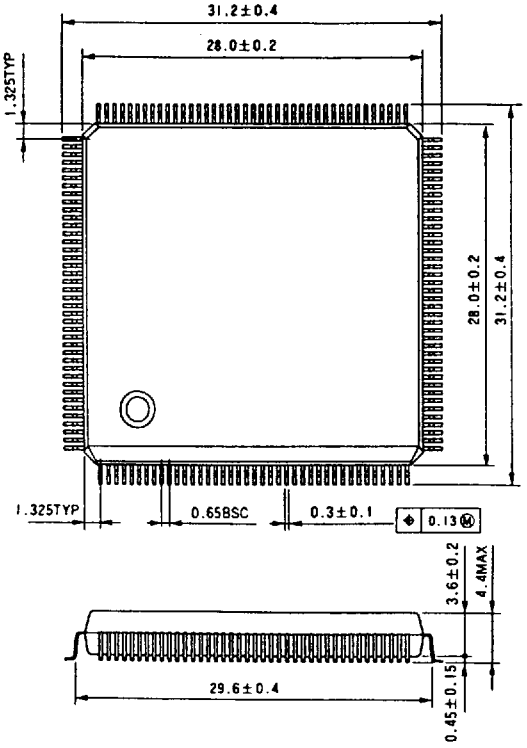
LOCAL BUS CYCLE (T3# mode)



* LCLK = CCLK at 1X clock
LCLK = PCLK at 2X clock

Production Package Specification

Package: 160-Pin PQFP
Unit: mm
Chip: SL82C461
SL82C362



Production Package Specification

Package: 100-Pin Plastic Rectangular Flat Package
Unit: mm
Chip: SL82C465