SL82C365 386 CACHE CONTROLLER

- Integrated cache controller
- 25/33/40MHz 80386DX/80386SX support
- Non-pipeline operation
- 16KB to 1MB cache size
- Line size from 1 to 4 doublewords
- 1 to 4 banks of SRAM
- Burst mode cache fill
- Built-in tag comparator
- Posted write buffer control
- Cache invalidation support
- Non-cacheable region support
- 80387/WT3167 interface
- Arbitration between reset and HOLD
- Interface with SL82C360/360SX chipset
- CMOS 100-pin RQFP package

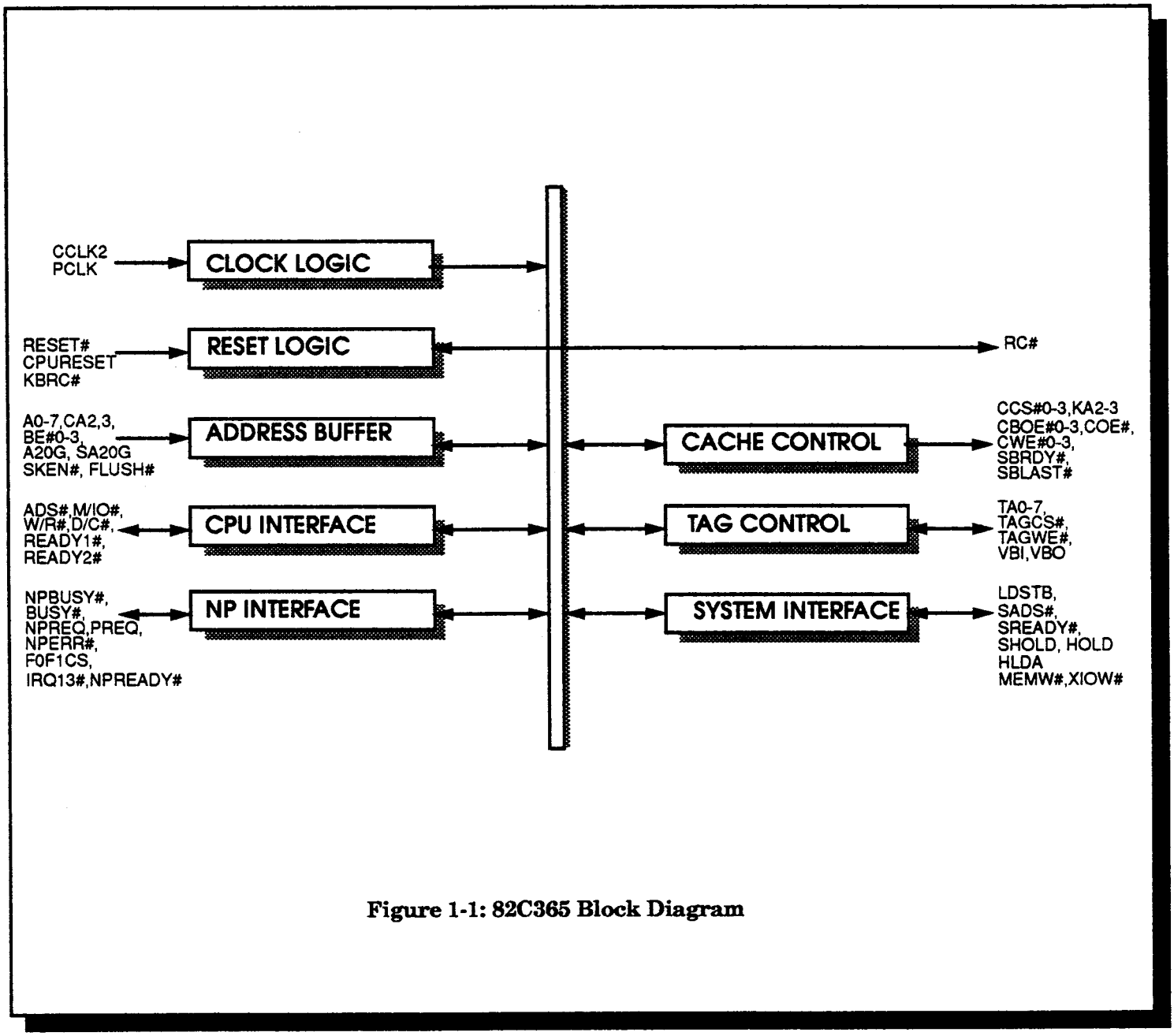


Figure 1-1: 82C365 Block Diagram

1 Functional Description

1.1 Cache Organization

The SL82C365 supports direct-mapped cache system with data size ranged from 16KB to 1MB and line size ranged from 1 to 4 doublewords[1]. Without any external logic, SL82C365 supports 1 to 4 banks of cache SRAMs independent of the line size. An 8-bit tag comparator is integrated into the chip which not only saves on the system cost but also improves the overall performance. 25ns tag SRAM and 35ns data SRAM are adequate for zero wait state non-pipelined 33Mhz operation. Assuming 8Kx8, 16Kx4, 32Kx8 and 64Kx4 SRAMs are used for tag SRAM, the selectable organization is indicated in Table 1-1. More options are available for data RAM configurations because of the flexibility in selecting the number of banks. Refer to section 1.13 for detailed design examples.

386DX	l-size	tag	index
32K	1	A22:15	A14:2
64K	1	A23:16	A15:2
128K	1	A24:17	A16:2
128K	2	A24:17	A16:3
256K	1	A25:18	A17:2
256K	2	A25:18	A17:3
256K	4	A25:18	A17:4
512K	2	A26:19	A18:3
512K	4	A26:19	A18:4
1M	4	A27:20	A19:4
386SX	**l-size**	**tag**	**index**
16K	1	A21:14	A13:1
32K	1	A22:16	A14:1
64K	1	A23:16	A15:1
64K	2	A23:16	A15:2
128K	2	A23:17	A16:2
128K	4	A23:17	A17:3
256K	4	A23:19	A18:4

Table 1-1: Cache Organization

The speed requirement for the tag and data SRAM at different clock frequencies and different cache line sizes is indicated in Table 1-2.The reason why faster data cache RAM is required for line size larger than one is that not all address lines to the data SRAMs are derived directly from the CPU. Depending on the line size being 2 or 4, the least significant one or two bits of the address are counted and driven by the SL82C365. About 10ns is required by this logic as opposed to 5ns of the TTL address buffers.

Mhz	l-size	tag	data
25	1	35ns	45ns
25	2,4	35ns	35ns
33	1	25ns	35ns
33	2,4	25ns	25ns
40	1	20ns	25ns
40	2,4	20ns	20ns

Table 1-2: SRAM Speed Requirement

1.2 Cache Directory

There is almost no limitation to the size of the cache directory. Practically speaking, 8K, 16K, 32K and 64K are the sizes that make the most sense. As a result, there are 13, 14, 15 and 16 bits of index, respectively, as is indicated in Table 1-1.

An 8-bit tag RAM and a 1-bit valid RAM that match the size of the cache directory is required for the cache implementation as is indicated in Figure 1-1. Both SRAMs can be implemented with or without output enable options. SRAMs with output enable consume less power while those without output enable are usually less expensive.

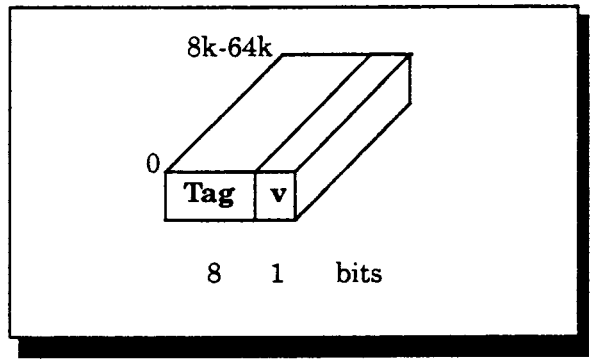


Figure 1-1: Cache Directory Organization

The 1-bit valid RAM can be combined into the tag RAM to save component cost. The number of tag bits reduces to 7 in such configurations.ber of tag bits reduces to 7 in such configurations. The option is selected by conditioning the RC# pin (#52) during power on reset. See section 1.12 for details.

1. 'doubleword' is meant to be 'word' for the 80386 SX systems throughout the context of this specification

1.3 Cache Operation

When the CPU starts a cycle, the index field of the CPU address is used to select a line from the cache directory. The tag stored in this line is compared with the tag field of the CPU address to determine a hit. If a hit is detected and the line is valid, the cache control signals CWE#3:0 or CBOE#3:0 (or COE#) are asserted for the proper cache data transfer.

Write-through algorithm is used to ensure that the data present in the cache are identical to the data in the main memory. Furthermore, one level of posted-write buffer is supported to minimize the write-through penalty.

1.5.1 Read Hit Operation

When a read hit occurs, the SL82C365 activates the READY# signal to the CPU by the end of T2 cycle to provide a zero wait state operation.

To relax the data SRAM access time, COE# is always asserted when a CPU memory read cycle is detected. This signal remains asserted in the T2 cycle to drive cache data onto the CPU data bus if a read-hit is detected; otherwise the signal returns to high at the start of T2 cycle.

COE# is mainly used in configurations with one bank of SRAMs. For configurations with two or four banks of SRAMs, CBOE#0-3 are used to activate and deactivate each bank.

During cache read hits, the previous data latched in the posted-write buffer can be concurrently popped out without slowing down the CPU execution.

1.5.2 Read Miss Operation

If the CPU address mis-matches the tag or the matched tag is invalid, a cache miss is indicated. If a cache read miss occurs, wait states are added to hold the CPU until the data retained in the write buffer are cleared and the requested data are ready on the CPU data bus.

When the write buffer is empty, the signal SADS# is asserted to initiate the system logic for DRAM or AT bus cycle.

If the read request is cacheable through input pin SKEN#, cache line fill operation is initiated as follow:

A number of DRAM read cycle performs;
CWE#3:0 are all activated for each cycle;
CCS#3:0 and KA3:2 are updated for each double word filled;
The requested data are presented in the last cycle;
The valid bit is set for the filled line;
The tag is updated.

The number of read cycles performed is equal to the line size of the cache. If the read request is not cacheable, then only one read cycle for the requested data is performed independent of the line size and neither the tag nor the valid bit is updated.

1.5.3 Write Hit Operation

During the write hit, both cache memory and system memory need to be updated. For cache, CWE#0-3 of the active bytes are asserted to write data into the cache memory, and READY# is returned to the CPU for the next command. For the system memory, the data is held temporarily in the write buffer, and the system logic takes over to complete the data write operation.

Write cycle can be either zero wait state or one wait state. The timing requirement for the tag RAM is more relaxed for the one-wait-state option while the performance is slightly better for the zero-wait-state option. For the zero-wait-state option, a pulldown resister is required on pin WWS (#49) for proper configuration. Refer to section 1.12 for details.

If the write buffer is loaded with previous data, however, the CPU is held until previous write operation is complete and the current data can be latched into the write buffer.

1.5.4 Write Miss Operation

If a cache miss occurs in a write cycle, no cache write operation is performed. The rest of the actions remain the same as the write hit operation.

1.5.5 DMA/Master Operation

During the DMA or external master cycles, the CPU is held and the cache control logic does not perform any function except the line invalidation. All the memory operations are directly interfaced to the DRAM control logic.

In the SL82C360 chip set, the LA and SA addresses are driven out to the CA bus during DMA and master cycles. No multiplexer is required to select the address to connect to the tag RAM and SL82C365 for tag

comparison. The same address flow applies to both CPU cycles and DMA/master cycles.

If a hit occurs in the memory write operation during DMA and master cycles, the corresponding valid bit is reset; otherwise no action is taken.

1.4 Burst Mode Operation

Larger line size can support larger cache size without increasing the size of the tag RAM. However, the penalty is also greater for the cache miss cycles because of the longer cache fill process. This penalty can be reduced by the burst mode transfer mechanism.

486-style burst mode transfer is supported by SL82C365 through the SBRDY# and SBLAST# pins. When SBRDY# is received, the KA3 and KA2 are counted according to the 486-burst order but with such adjustment that the last data filled into cache is the data requested by the CPU. For instance, if the CPU requests the 3rd doubleword from a cache with line size 4, then the burst order is 4->0->C->8, which is 486-burst order with the last doubleword being the one that is requested.

The assertion of SBRDY# indicates the external system is capable of performing burst mode data transfer. Then no further SADS# will be asserted. If SREADY# is received instead of SBRDY#, SL82C365 switches back to normal non-burst transfer automatically by activating SADS#. In this case, the 'CPU' address seen by the system logic (pin KA2-3) will be updated for each cycle.

The SL82C360 chip set supports 486-style burst transfer and can be directly interfaced with SL82C365 for a very efficient cache system of large line size.

1.5 Cache Initialization

A valid bit is associated with each line in the cache to indicate whether the data in the cache are valid. The valid bit is set for each cache fill and reset by the bus snooping or cache flush. All cache memory entries must be initialized by a memory access with the flush signal asserted. The flush signal can be asserted by programming a register in the SL82C360 chip set. The cache controller is disabled after power-on reset and is enabled after the flush input has been toggled for three times.

1.6 Non-Cacheable Regions

All I/O address space is not cacheable. Whether a memory cycle is cacheable depends on input pin SKEN# which is sampled at the start of T2 cycle. The SKEN# can be directly driven by pin SKEN# of the SL82C360 chip set which supports two non-cacheable regions with sizes ranging from 16K to 4MB in addition to the standard non-cacheable region A0000h to BFFFFh.

1.7 Posted-Write Buffer Control

One level of posted-write buffer is supported by the SL82C365 to minimize the write penalty incurred by the slower DRAM and AT bus devices. The CPU data is temporarily stored in the buffer so that the CPU bus can be released for the following cache read-hit operations. The buffer is released for the next write command upon completion of the system write operation.

The write buffer built inside the SL82C360 chip set is directly controlled by the LDSTB pin of SL82C365. When this pin goes high, the CPU data becomes transparent. The data is latched into the buffer at the falling edge of LDSTB.

The posted write capability is disabled upon power-on reset. This capability is turned on after the flush signal has been toggled for five times.

1.8 READY Generation

There are two possible connections of 'ready' signal between SL82C365 and the CPU in a cached system: READY1# and READY2#. These two signals are identical for read-hit cycles, both being zero wait state access. The difference is for cycles that are passed to the system logic or other local devices such as the NP. Pin READY1# returns ready to the CPU in the same cycle that these devices activate ready, while pin READY2# waits for another CPU cycle. The performance is slightly better with READY1# connection. However, for clock frequency higher than 33Mhz, READY2# connection should be used to guarantee the required setup time by the CPU.

1.9 NP Interface

Both Intel 80387 and Weitek WT3167 are supported by SL82C365. The ready output generated by the two devices is combined with that from the system logic and cache read hit operation for the CPU READY#.

80387 or WT3167 cycles are detected through CPU

command status and address pin A31 and A29. SL82C365 detects the presence of 80387 or WT3167 automatically during power-on reset. Both 80387 cycles without the presence of 80387 and the WT3167 cycles without the presence of WT3167 are handled by the SL82365.

NPREQ, NPBUSY# and NPERR# are inputs from the 80387 to be converted as PREQ and BUSY# to the 386 CPU, respectively. IRQ13# is asserted when NPERR# is asserted for an NP error.

F0F1CS is input from the SL82C360 chip set to indicate an IO write cycle to address F0h-F7h for clearing the ERROR status of the NP interface.

1.10 Arbitration

CPU hold request is arbitrated in SL82C365 with the RC# signal from the keyboard controller (KBRC#). This arbitration guarantees the CPU cannot be reset when it is in a HOLD status.

The HOLD signal is also arbitrated with the state machine that controls the posted-write operation. The CPU does not receive the hold request until the write buffer is cleared.

1.11 GateA20 Logic

There are two sources of GateA20 in a typical PC/AT system: the keyboard controller and the fast GateA20 register. The effective GateA20 is the logic OR of these two signals.

There are two ways to implement this logic for SL82C365. If the OR'ed signal is available in the system, then this signal can be directly input to the chip through pin A20G. The other alternative is to combine the two GateA20 signals through a wired-or connection. This alternative is adopted by the SL82C365 and the SL82C360 chip set combination. The GateA20 input from the keyboard controller is connected to pin A20G of SL82C365 and is converted an open-source driver type in pin SA20G to be combined with the fast GateA20 register setting in the SL82C360 chip set. The combined result can be used in both the SL82C360 chip set and the SL82C365 cache controller.

CA20 is usually the most critical bit of the CPU address because one additional AND gate is required for the GateA20 logic. This address bit is always allocated as one of the tag bits rather than index bits in the SL82C365 cache controller. Note that the timing requirement for a tag bit is far more relaxed than that for an index bit so that the system performance is not penalized by the presence of the GateA20 logic.

There are eight bits of tag that are supported by the SL82C365: pins A0-A7. The connection of these bits to the CPU address bus depends on the cache configuration. Refer to Table 1-1 for possible connections. Note that CA20 is always one of the tag bits. Because of the pre-wired logic of GateA20, CA20 always connects to pin A4. The other seven bits can be connected arbitrarily with the other seven address bits.

1.12 Jumper Setting

Although SL82C365 supports both 386DX and 386SX CPU and a great deal of cache configurations, the functionality of the chip remains almost the same. The customization is mainly determined by the CPU/SRAM devices and their connections rather than by configuring the SL82C365. Therefore, there is no need for configuration registers. There are a few options, however, supported by the SL82C365 and they are determined by the condition of a few pre-designated pins during power-on reset. The condition of these pins is determined by whether a pulldown resistor (with recommended value 4.7K) is connected to the pin. The available options and the name and pin number of the designated pin/pins are indicated as follows. The '0' option is selected when a pulldown resistor is connected to the corresponding pin. The pullup resister is not necessary for the '1' option because each of these pins is internally pulled up by a 50K resistor.

Line size: (TAGOE#-37, VBO-31)
- (0,0) or (1,1) - 1 doubleword
- (0,1) - 2 doublewords
- (1,0) - 4 doublewords

SRAM banks: (SBLAST#-76)
- (0) - 1 bank or 4 banks
- (1) - 1 bank or 2 banks

Write wait state: (WWS-49)
- (0) - 0 wait state
- (1) - 1 wait state

Combined valid/tag SRAM: (RC#-52)
- (0) - not combined
- (1) - combined

1.13 Design Examples

Refer to Figure 1-2 for the following design examples.

Example 1: 64K Cache with line size 1 doubleword

(386DX)
TAG RAM: two 16Kx4 SRAMs (total size 16Kx8)
Address to TAG RAM: CA15-2
Tag Field:CA23-16 (separated valid RAM)
VB,CA22-16 (combined valid RAM)
Data RAM:
option 1: 1 bank of 16Kx4 x8
data RAM address: CA15-2
data RAM OE: COE#
data RAM CS: VSS
option 2: 2 banks of 8Kx8 x4
data RAM address: CA15-3
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1

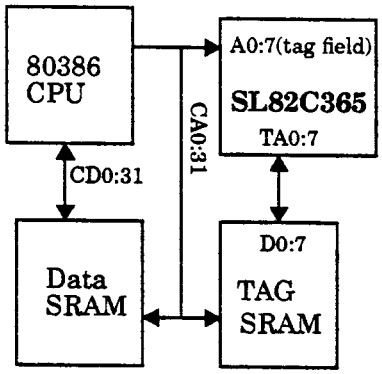


Figure 1.2: Cache subsystem

Example 2: 128K Cache with line size
1 doubleword (386DX)
TAG RAM: one 32Kx8 SRAM
Address to TAG RAM: CA16-2
Tag Field: CA24-17 (separated valid RAM)
VB,CA23-17 (combined valid RAM)
Data RAM:
option 1: 1 bank of 32Kx8 x4
data RAM address: CA16-2
data RAM OE: COE#
data RAM CS: VSS
option 2: 2 banks of 16Kx4 x8
data RAM address: CA16-3
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1

Example 3: 256K Cache with line size
1 doubleword (386DX)
TAG RAM: two 64Kx4 SRAMs (total size 64Kx8)
Address to TAG RAM: CA17-2
Tag Field: CA25-18 (separated valid RAM)
VB,CA24-18 (combined valid RAM)
Data RAM:
option 1: 1 bank of 64Kx4 x8
data RAM address: CA17-2
data RAM OE: COE#
data RAM CS: VSS
option 2: 2 banks of 32Kx8 x4
data RAM address: CA17-3
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1

Example 4: 256K Cache with line size
2 doublewords (386DX)
TAG RAM: one 32Kx8 SRAM
Address to TAG RAM: CA17-3
Tag Field: CA25-18 (separated valid RAM)
VB,CA24-18 (combined valid RAM)
Data RAM:
option 1: 1 bank of 64Kx4 x8
data RAM address: CA17-3, KA2
data RAM OE: COE#
data RAM CS: VSS
option 2: 2 banks of 32Kx8 x4
data RAM address: CA17-3
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1

Example 5: 512K Cache with line size
2 doublewords (386DX)
TAG RAM: two 64Kx4 SRAMs (total size 64Kx8)
Address to TAG RAM: CA18-3
Tag Field: CA26-19 (separated valid RAM)
VB,CA25-19 (combined valid RAM)
Data RAM:
option 1: 2 banks of 64Kx4 x8
data RAM address: CA18-3
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1
option 2: 4 banks of 32Kx8 x4
data RAM address: CA18-4
data RAM OE: CBOE#0, CBOE#1
CBOE#2, CBOE#3
data RAM CS: CCS#0, CCS#1
CCS#2, CCS#3

Example 6: 1M Cache with line size
4 doublewords (386DX)
TAG RAM: two 64Kx4 SRAMs (total size 64Kx8)
Address to TAG RAM: CA19-4
Tag Field: CA27-20 (separated valid RAM)
VB,CA26-20 (combined valid RAM)
Data RAM:
option 1: 4 banks of 64Kx4 x8
data RAM address: CA19-4

data RAM OE: CBOE#0, CBOE#1
CBOE#2, CBOE#3
data RAM CS: CCS#0, CCS#1
CCS#2, CCS#3
option 2: 1 bank of 256Kx4 x8
data RAM address: CA19-4,KA3-2
data RAM OE: COE#
data RAM CS: VSS

Example 7: 16K Cache with line size 1 word (386SX)

TAG RAM: one 8Kx8 SRAM
Address to TAG RAM: CA13-1
Tag Field: CA21-14 (separated valid RAM)
VB,CA20-14 (combined valid RAM)
Data RAM: 1 bank of 8Kx8 x2
data RAM address: CA13-1
data RAM OE: COE#
data RAM CS: VSS

Example 8: 32K Cache with line size 1 word (386SX)

TAG RAM: two 16Kx4 SRAMs (total size 16Kx8)
Address to TAG RAM: CA14-1
Tag Field:CA22-15 (separated valid RAM)
VB,CA21-15 (combined valid RAM)
Data RAM:
option 1: 1 bank of 16Kx4 x4
data RAM address: CA14-1
data RAM OE: COE#
data RAM CS: VSS
option 2: 2 banks of 8Kx8 x2
data RAM address: CA14-2
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1

Example 9: 32K Cache with line size 2 words (386SX)

TAG RAM: one 8Kx8 SRAM
Address to TAG RAM: CA13-1
Tag Field: CA21-14 (separated valid RAM)
VB,CA20-14 (combined valid RAM)
Data RAM:
option 1: 1 bank of 16Kx4 x4
data RAM address: CA14-2,KA2
data RAM OE: COE#
data RAM CS: VSS
option 2: 2 banks of 8Kx8 x2
data RAM address: CA14-2
data RAM OE: CBOE#0, CBOE#1
data RAM CS: CCS#0, CCS#1

2 SL82C365 Signal Description

Signal Name	Pin Number	Type	Signal Description
CLOCK /RESET			
CCLK2	14	I	Clock input from SL82C361. It is the same clock input to CPU.
PCLK	79	I	Phase clock from SL82C361. A logic high indicates phase 1.
CPURESET	80	I	CPU reset.
RESET#	35	I	Active low system reset.
KBRC#	51	I	Keyboard RC# to request CPU reset. This input is arbitrated with HLDA to generate RC# to the system logic.
RC#	52	O	RC# to SL82C361 for CPU reset after arbitration with HLDA.
CPU INTERFACE			
ADS#	74	I	Address strobe. The falling edge indicates the start of a CPU cycle.
M/IO#	73	I	Memory/IO status from CPU. High indicates a memory cycle and low indicates an IO cycle.
W/R#	71	I	Write/read status from CPU. High indicates a write cycle and low indicates a read cycle.
D/C#	72	I	Data/code status from CPU. High indicates data transfer and low indicates control operation.
READY1#	84	O	Ready output #1. The falling edge indicates the completion of the current CPU cycle. Zero wait state access is always for a cache read hit. For system and NP cycles, READY1# is activated in the same CPU cycle when SREADY# and NPREADY# is activated. This output is of push-pull drive.
READY2#	85	O	Ready output #2. Zero wait state access is always for a cache read hit. For system and NP cycles, READY1# is activated in the next CPU cycle when SREADY# and NPREADY# is activated. This output is of push-pull drive.
ADDRESS BUS			
A0-7	7,6,98,97,96 95,94,93	I	Address inputs from CPU for comparison with TA0-7. A4 always connects to pin CA20 of CPU. The connection of other bits depend on the cache configuration.
CA29,31	25,10	I	CPU address inputs for 80387 or WT3167 decoding.

CA2,3	20,19	I	CPU address inputs for caches with larger line size.
KA2,3	18,17	O	Address converted from CA2,3 to drive SL82C361.
BE#0-3	70,69,68,67	I	Byte enable input from CPU.
A20G	43	I	Gate A20 input from the keyboard controller.
SA20G	42	B	Open source conversion of the A20G input from the keyboard controller. This allows wired-or connection with the fast Gate A20 output from the SL82C361.

TAG RAM CONTROL

TA0-7	9,8,100,99 89,88,87,86	B	Tag address bus connected to the data bus of TAG RAM.
TAGOE#	37	O	Tag RAM output enable.
TAGWE#	24	O	Tag/valid RAM write enable.
VBI	5	I	Input from valid bit RAM to indicate valid status. This pin should tie high for combined tag/valid implementations.
VBO	31	O	Output to valid bit RAM. This pin is not used for combined tag/valid implementations.

CACHE CONTROL

SFLUSH#	36	I	Flush input from SL82C361 to force cache miss.
SKEN#	1	I	Cacheable input pin from SL82C361.
COE#	39	O	Cache RAM output enable.
CBOE#0-3	38,63,50,44	O	Cache RAM output enable for each bank.
CCS#0-1	27,16	O	Cache RAM chip select for bank 0 and bank1.
CCS#2/KA3A	4	O	Multi-function pin: used as CCS#2 for bank 2 chip select if 4 SRAM bank option is selected. Used as KA3A to connect to the least significant address bit of bank 0 cache SRAM if 2 SRAM bank option is selected.
CCS#3/KA3B	92	O	Multi-function pin: used as CCS#3 for bank 3 chip select if 4 SRAM bank option is selected. Used as KA3B to connect to the least significant address bit of bank 1 cache SRAM if 2 SRAM bank option is selected.
CWE#0-3	23,21,11,2	O	Cache data write byte enable.

SBRDY#	81	I	Burst ready input from SL82C361.
SBLAST#	76	O	Last burst cycle indicator to SL82C361.
WWS	49	B	Write wait state jumper. Left unconnected for one wait state and pulled down by 4.7K resister for zero wait state write operation.

NUMERICAL PROCESSOR INTERFACE

Several pins in this category are multi-function pins and their definition depends on whether 80387 or WT3167 is used as the co-processor. The type of co-processor is detected automatically by the SL82C365 during power-on reset.

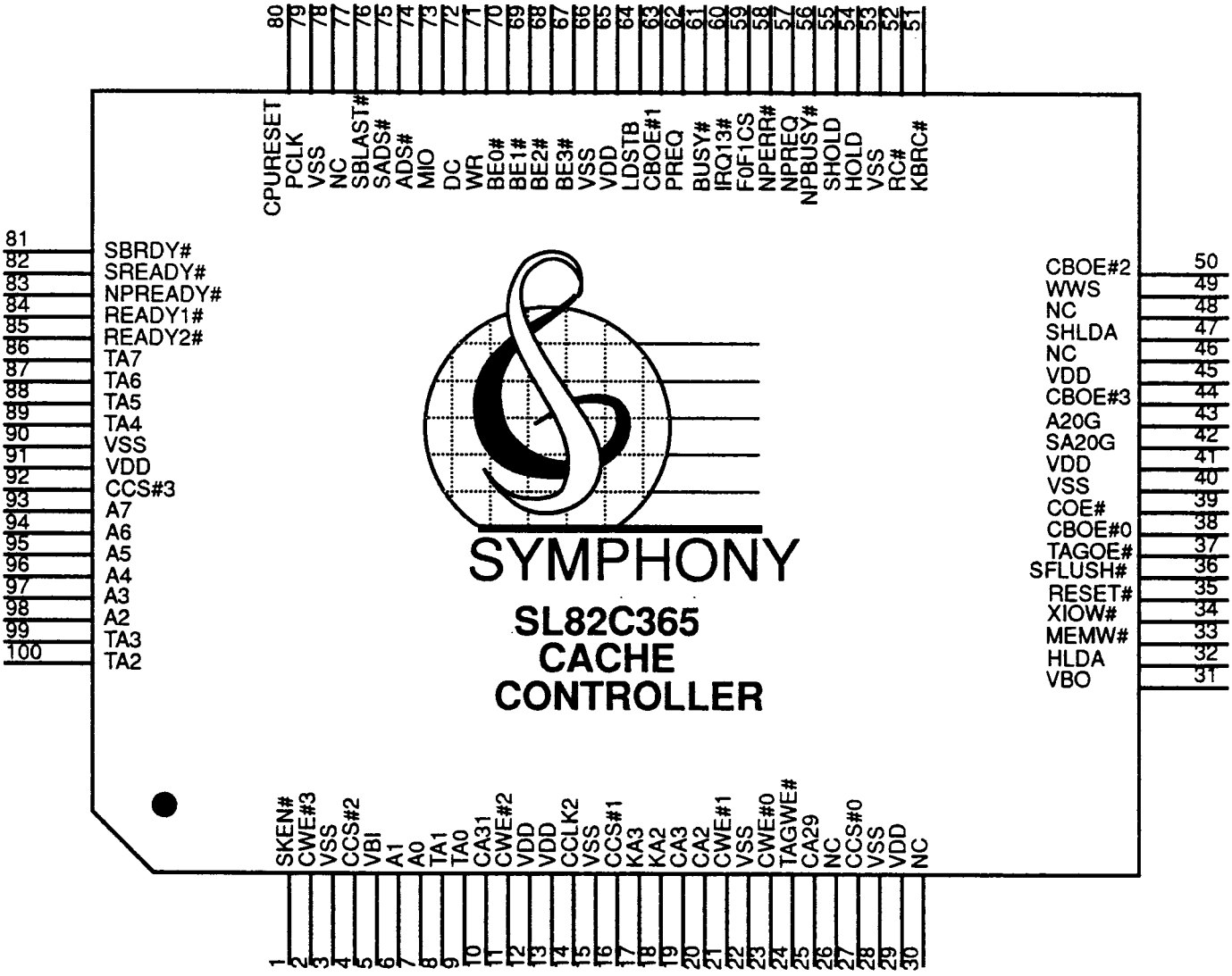
NPBUSY#/ WPRES#	56	I	**387 mode:** input from pin BUSY# of 80387 co-processor to indicate that the NP is executing an instruction and is not ready to accept new one. **3167 mode:** input from pin PRES# of WT3167 to detect its existence during power-on reset.
BUSY#	61	O	**387 mode:** output to pin BUSY# of CPU to indicate that the NP is not ready to accept a new instruction. On occurrence of NP errors, the signal is latched and held active until an occurrence of a write to port F0h or F1h or NPRESET. **3167 mode:** not used.
NPREQ/ WINTR	57	I	**387 mode:** input from pin PREQ of 80387 to indicate that the NP is requesting an operand transfer to or from memory by the CPU. **3167 mode:** input from pin INTR of WT3167 for interrupt request.
PREQ	62	O	**387 mode:** output to pin PEREQ of the CPU. This signal is returned to active on the occurrence of NP errors after NPBUSY# has gone inactive. A write to port F0h returns control of PREQ to directly follow NPREQ. **3167 mode:** not used.
NPERR#	58	I	**387 mode:** input from the ERROR# of 80387 to indicate that the current instruction has generated a non-mask error. In response, IRQ13# is generated and BUSY# and PREQ is forced active until a write to port F0h/F1h and/or NPRESET by the interrupt handler. **3167 mode:** not used.
NPREADY#	83	I	Input from 80387 or WT3167 ready output.
IRQ13#	60	O	Interrupt request 13 when there is an NP error.
F0F1CS	59	I	Input from SL82C361 indicating an IO write to address F0h-F7h.

SYSTEM INTERFACE

LDSTB	64	O	Write buffer load strobe output to SL82C362. When high, the CPU data is transparent. The data is latched into the buffer at at the falling edge of LDSTB.
SADS#	75	O	System ADS# to SL82C361.
SREADY#	82	I	System ready input from SL82C361.
SHOLD	55	I	Hold request from SL82C362.
HOLD	54	O	Hold request to CPU
HLDA	32	I	Hold acknowledgment from CPU in response to a hold request.
SHLDA	47	O	Hold acknowledgment to the system logic.
MEMW#	33	I	Memory write command for cache snooping.
XIOW#	34	I	IO write during power-on period for reading jumper setting.

POWER AND GROUND

VDD	12,13,29,41,45,65,91
VSS	3,15,22,28,40,53,66,78,90


80 CPURESET
79 PCLK
78 VSS
77 NC
76 SBLAST#
75 SADS#
74 ADS#
73 MIO
72 DC
71 WR
70 BE0#
69 BE1#
68 BE2#
67 BE3#
66 VSS
65 VDD
64 LDSTB
63 CBOE#1
62 PREQ
61 BUSY#
60 IRQ13#
59 F0F1CS
58 NPERR#
57 NPREQ
56 NPBUSY#
55 SHOLD
54 HOLD
53 VSS
52 RC#
51 KBRC#
81 SBRDY#
82 SREADY#
83 NPREADY#
84 READY1#
85 READY2#
86 TA7
87 TA6
88 TA5
89 TA4
90 VSS
91 VDD
92 CCS#3
93 A7
94 A6
95 A5
96 A4
97 A3
98 A2
99 TA3
100 TA2
SYMPHONY
SL82C365
CACHE
CONTROLLER
50 CBOE#2
49 WWS
48 NC
47 SHLDA
46 NC
45 VDD
44 CBOE#3
43 A20G
42 SA20G
41 VDD
40 VSS
39 COE#
38 CBOE#0
37 TAGOE#
36 SFLUSH#
35 RESET#
34 XIOW#
33 MEMW#
32 HLDA
31 VBO
1 SKEN#
2 CWE#3
3 VSS
4 CCS#2
5 VBI
6 A1
7 A0
8 TA1
9 TA0
10 CA31
11 CWE#2
12 VDD
13 VDD
14 CCLK2
15 VSS
16 CCS#1
17 KA3
18 KA2
19 CA3
20 CA2
21 CWE#1
22 VSS
23 CWE#0
24 TAGWE#
25 CA29
26 NC
27 CCS#0
28 VSS
29 VDD
30 NC

3 82C365 Electrical and Timing Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient Operating Temperature	0	70	Degree C
Storage Temperature	-65	125	Degree C
Supply Voltage (Vcc)	-0.5	7.0	V
Input Voltage	-0.5	Vcc+0.5	V
Output Voltage	-0.5	Vcc+0.5	V

3.2 DC Characteristics (Ta=0-70 degree C, Vdd=5V+/-5%)

Parameter	Min.	Typ.*	Max.	Unit
Input low level (TTL)	-0.5	---	0.8	V
Input high level (TTL)	2.2	---	5.5	V
Output low voltage				
4mA buffer, IOL=4mA	---	0.15	0.4	V
8mA buffer, IOL=8mA	---	0.18	0.4	V
12mA buffer, IOL=12mA	---	0.18	0.4	V
16mA buffer, IOL=16mA	---	0.17	0.4	V
Output high voltage				
4mA buffer, IOL=4mA	3.0	4.54	---	V
8mA buffer, IOL=8mA	3.0	4.44	---	V
12mA buffer, IOL=12mA	3.0	4.46	---	V
16mA buffer, IOL=16mA	3.0	4.46	---	V
Input low current	-10	-0.01	---	uA
with 50K pullup resistor	-250	-80	-20	uA
Input high current	---	0.01	10	uA
Tristate output off current low	-10	-0.01	---	uA
Tristate output off current high	---	0.01	10	uA
Input capacitance**	---	10	---	pF
Output capacitance**	---	10	---	pF
I/O capacitance**	---	10	---	pF

* Typical is under the condition of Vcc=5.0+/-5% and Ta=25 degree C.
** Capacitance includes the capacitance of I/O cell plus package pin.

3.3 AC Characteristics (Ta=0-70 degree C, Vdd=5V+/-5%; Unit=ns)

Description	Symbol	Min.	Typ.	Max.
CACHE READ HIT CYCLE				
READY1# fall from TA valid	t100	4		12
READY1# rise from CCLK rise	t101	5		20
READY2# fall from TA valid	t102	4		12
READY2# rise from CCLK rise	t103	5		18
COE# fall from ADS# fall	t104	3		10
COE# rise from CCLK rise	t105	4		15
SKEN# setup to TA valid	t107	0		
SKEN# hold from CCLK rise	t108	0		
SFLUSH# setup to TA valid	t109	0		
SFLUSH# hold from CCLK rise	t110	0		
VBI setup to TA valid	t111	0		
VBI hold from CCLK rise	t112	0		
CBOE#0-3 fall from CCLK rise	t113	3		12
CBOE#0-3 rise from CCLK rise	t114	3		12
CACHE READ MISS CYCLE				
SADS# fall from CCLK rise	t200	4		14
SADS# fall from TA valid	t201	4		12
SADS# rise from CCLK rise	t202	3		13
CWE#0-3 fall from CCLK rise	t203	3		10
CWE#0-3 rise from CCLK rise	t204	2		9
READY1# fall from SREADY#	t205	2		7
READY2# fall from CCLK rise	t206	3		12
SREADY# setup to CCLK rise	t207	4		
SREADY# hold from CCLK rise	t208	0		
VBO rise from CCLK rise	t209	4		17
VBO fall from CCLK rise	t210	4		17
TA valid from TAGWE# fall	t212	3		12
TA float from TAGWE# rise	t213	3		13
TAGOE# rise from CCLK rise	t214	5		17
TAGOE# fall from CCLK rise	t215	5		19
TAGWE# fall from CCLK rise	t216	4		15
TAGWE# rise from CCLK rise	t217	4		15
CCS#0-3 rise from CCLK rise	t218	4		15
CCS#0-3 fall from CCLK rise	t219	4		15
SBRDY# setup to CCLK rise	t220	7		
SBRDY# hold from CCLK rise	t221	0		

READY1# fall from SBRDY# fall	t222	3	8
SBLAST# rise from CCLK rise	t223	3	10
SBLAST# fall from CCLK rise	t224	5	16
KA2/3 valid from ADS# fall	t225	3	9
KA2/3 valid from CCLK rise	t226	3	9
CCS#0-3 valid from CCLK rise	t227	2	8

WRITE CYCLE

READY1# fall from CCLK rise	t301	4	13
LDSTB rise from CCLK rise	t302	3	11
LDSTB fall from CCLK rise	t303	3	12
SADS# fall from ADS# fall	t304	2	8
SADS# fall from SREADY# fall	t305	2	8

DMA/MASTER CYCLE

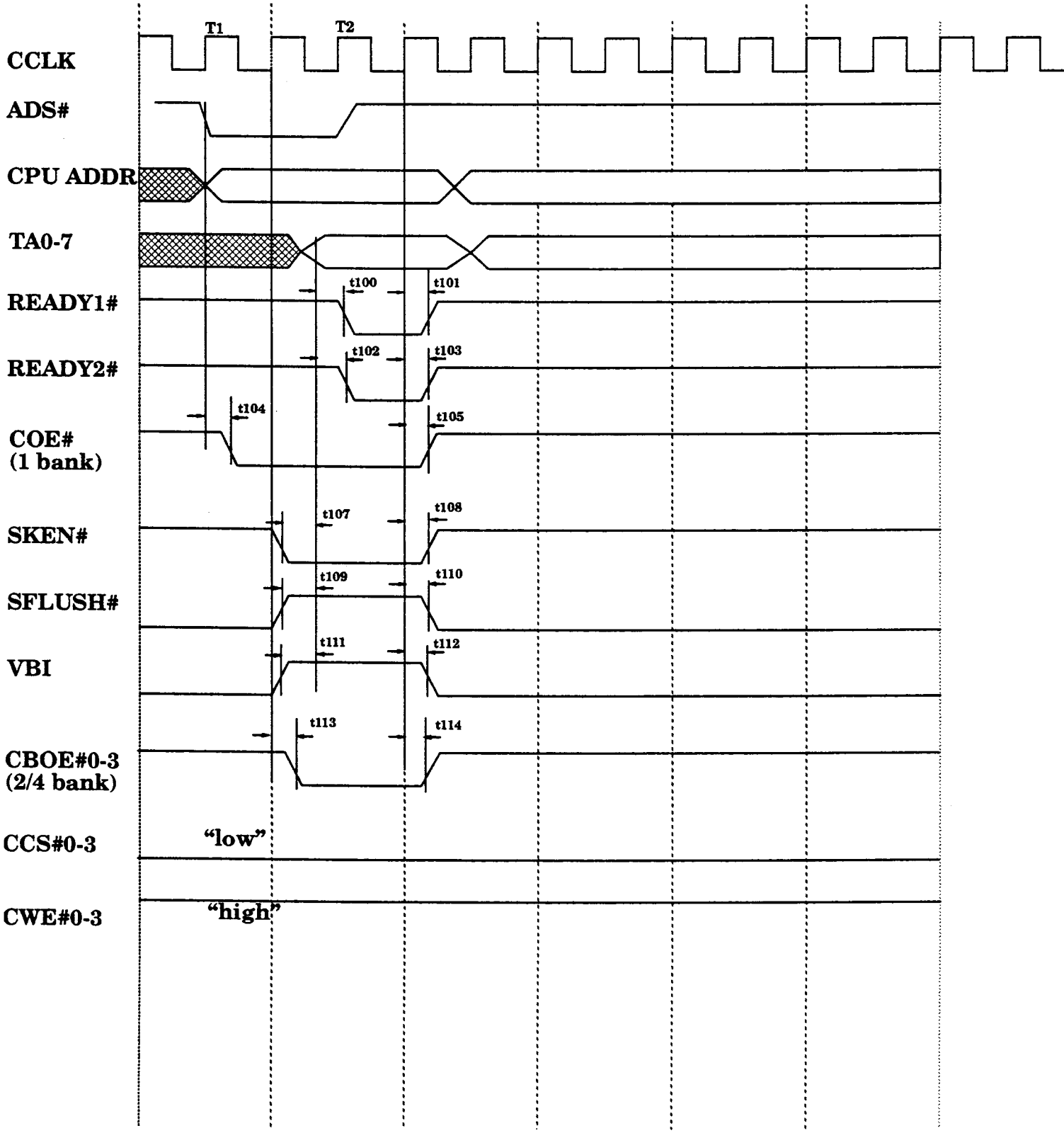
MEMW# setup to CCLK rise	t401	5	20
TAGOE# rise from CCLK rise	t402	4	17
TAGOE# fall from CCLK rise	t403	4	17
TAGWE# fall from CCLK rise	t404	4	15
TAGWE# rise from CCLK rise	t405	4	15
TA valid from TAGWE# fall	t406	3	12
TA float from TAGWE# rise	t407	3	13
CWE#0-3 fall from CCLK rise	t408	3	10
CWE#0-3 rise from CCLK rise	t409	2	9

NP CYCLE

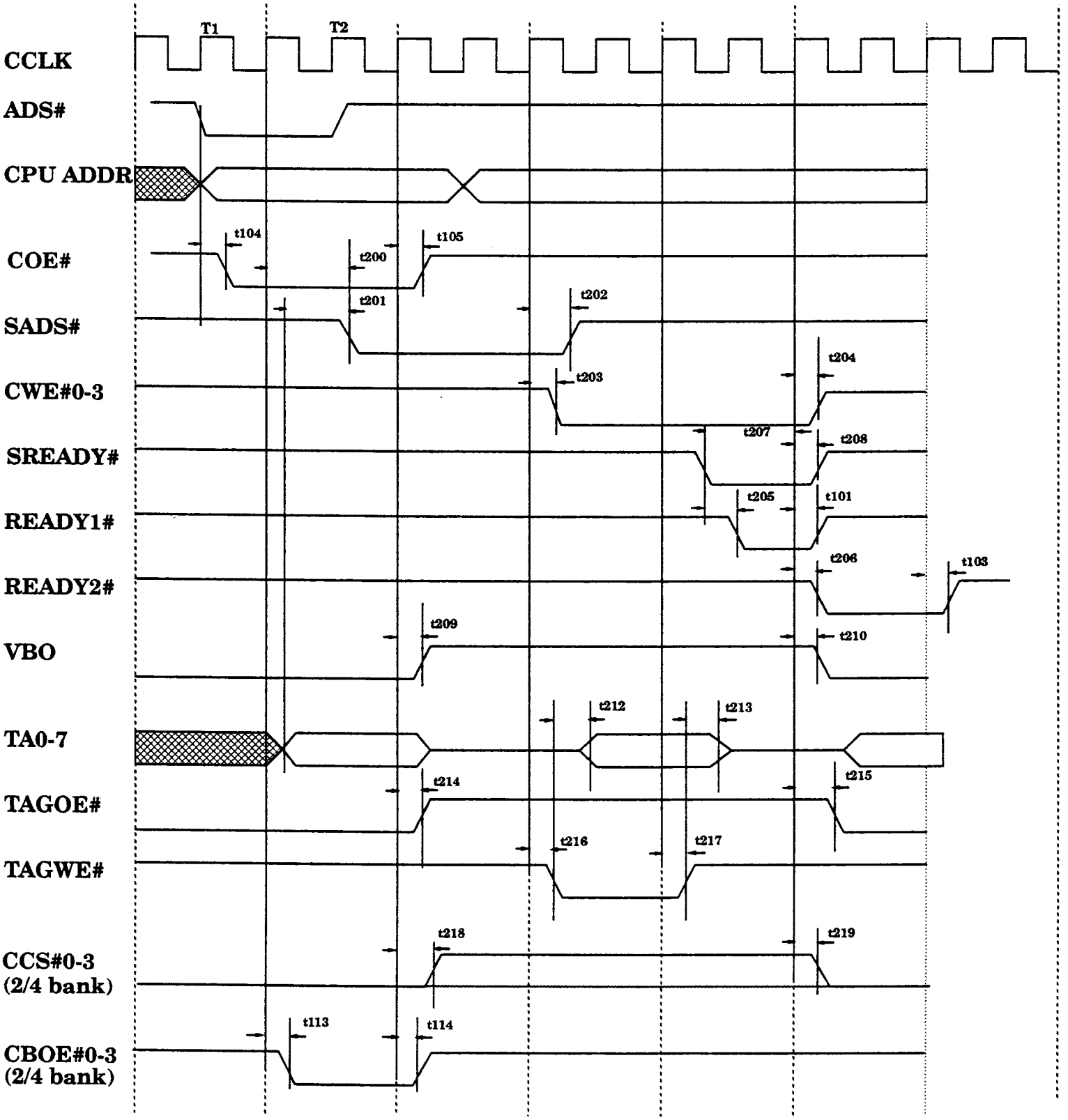
READY1# fall from NPREADY#	t501	3	8
READY1# fall from CCLK (No NP)	t502	5	17
NPREADY# setup to CCLK rise	t503	7	
NPREADY# hold from CCLK rise	t504	0	

The following loadings are assumed for the above timing specifications.
READY1#, READY2#, SADS#, LDSTB: 40pf
Other signals: 50pf

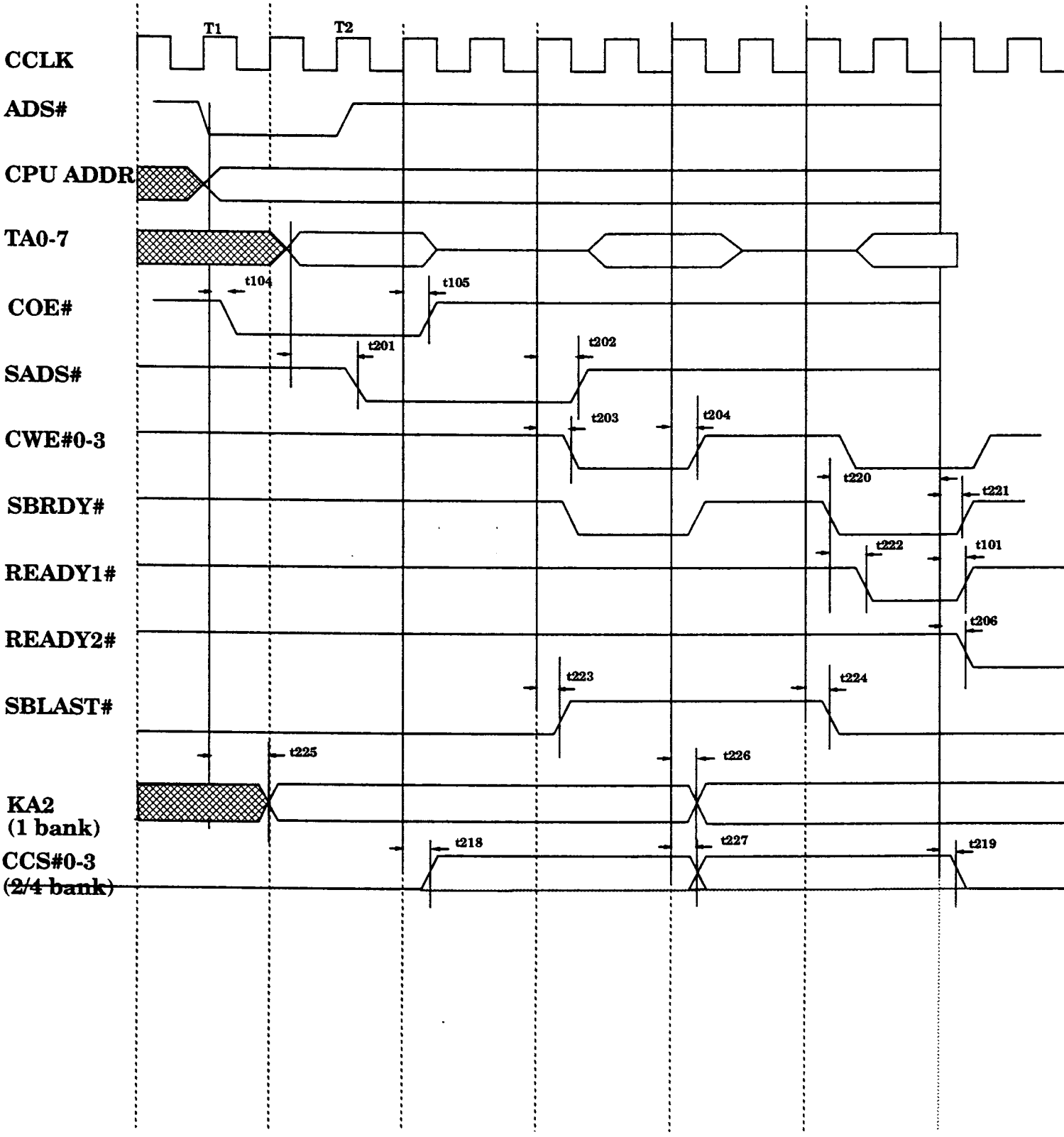
Cache Read Hit



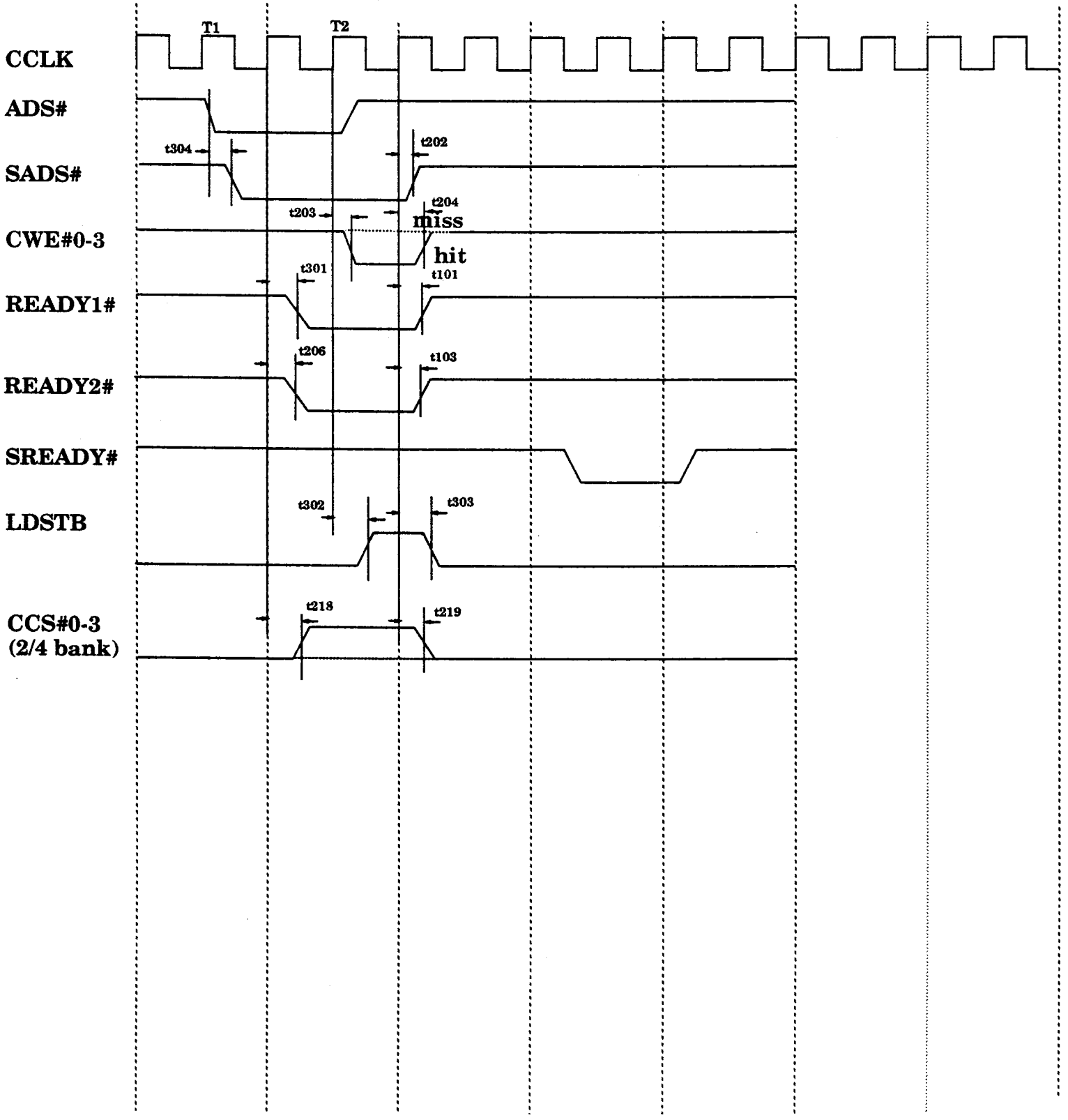
Cache Read Miss - Line Size = 1 Dword



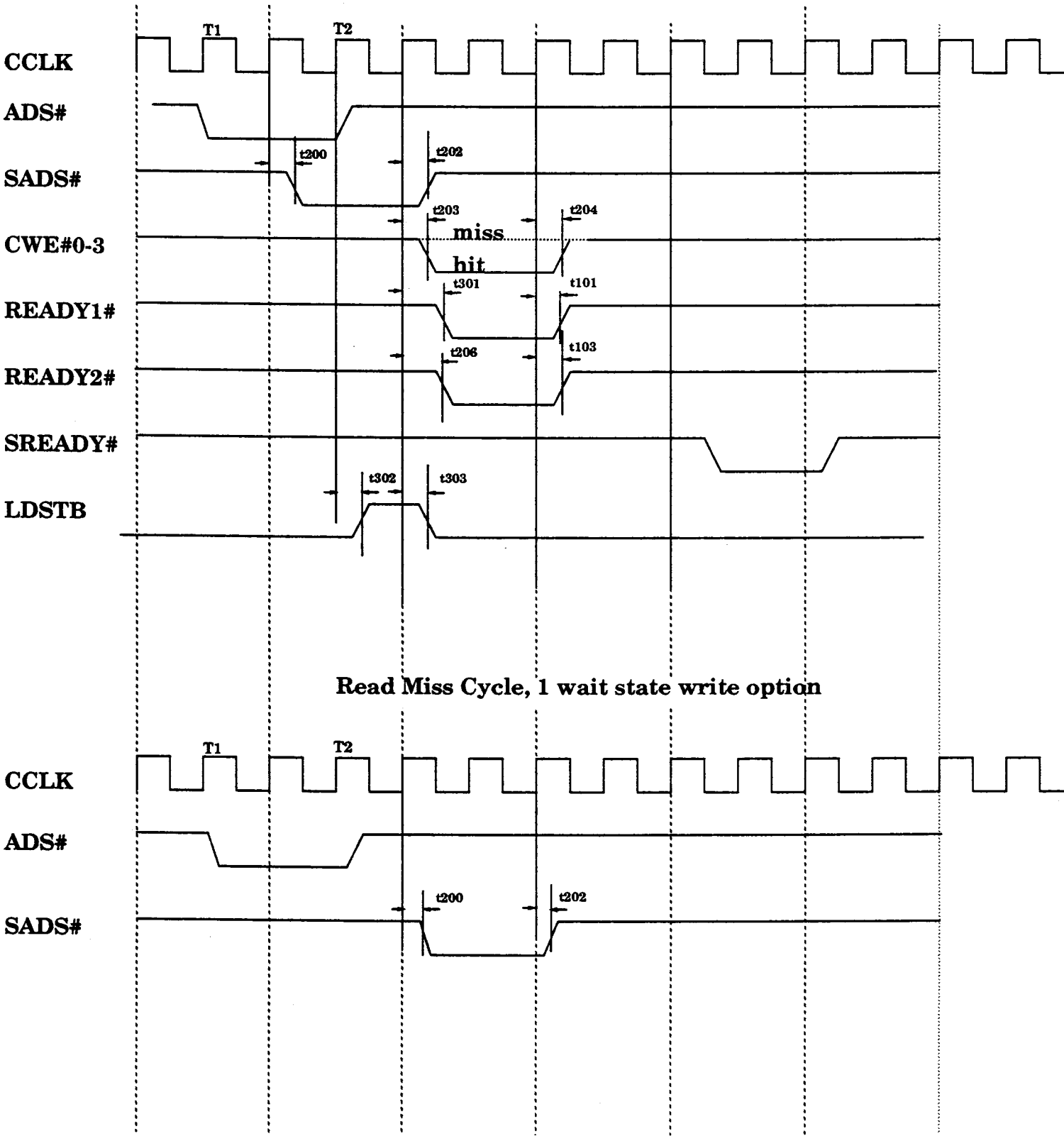
Cache Read Miss - 2 Doublewords, burst



Write Cycle, 0 wait state

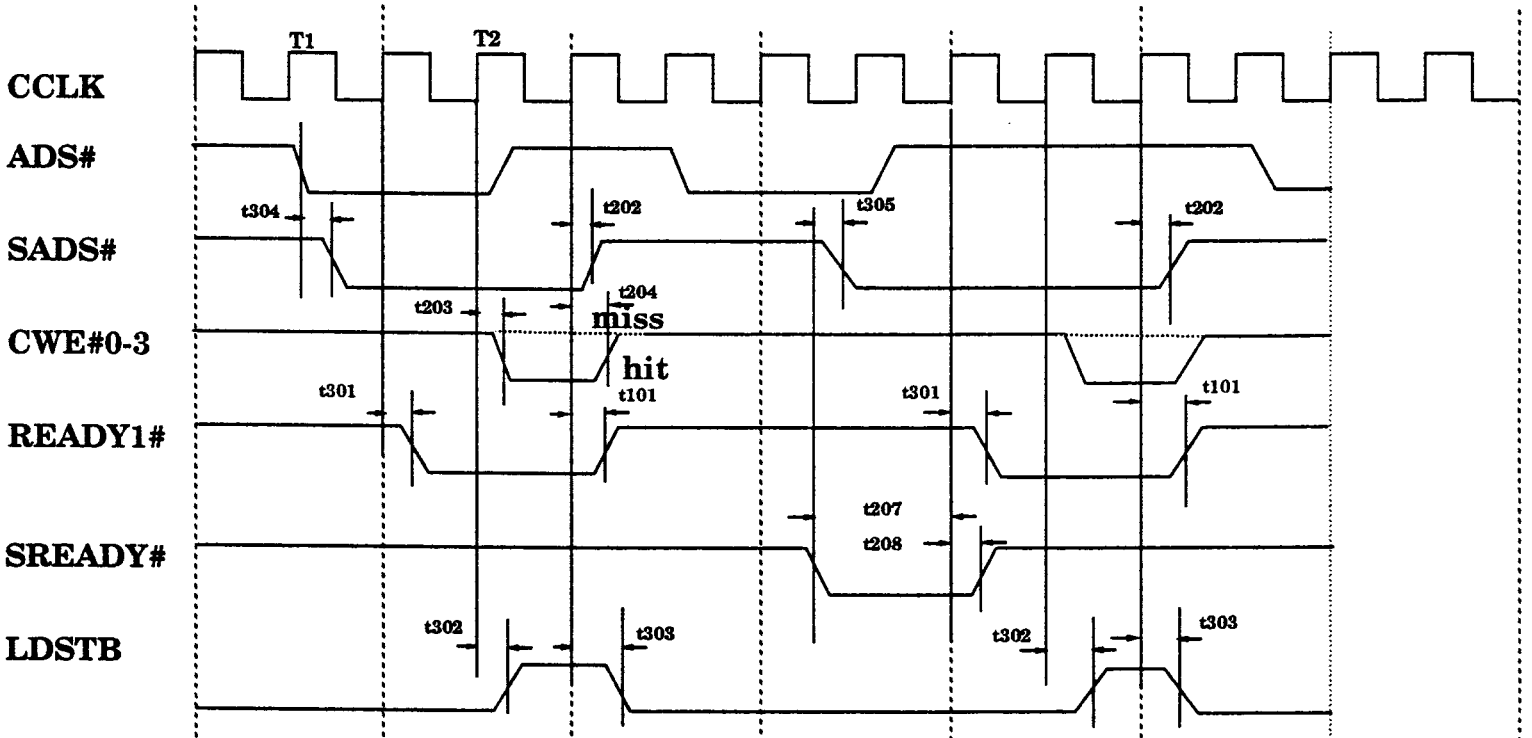


Write Cycle, 1 wait state

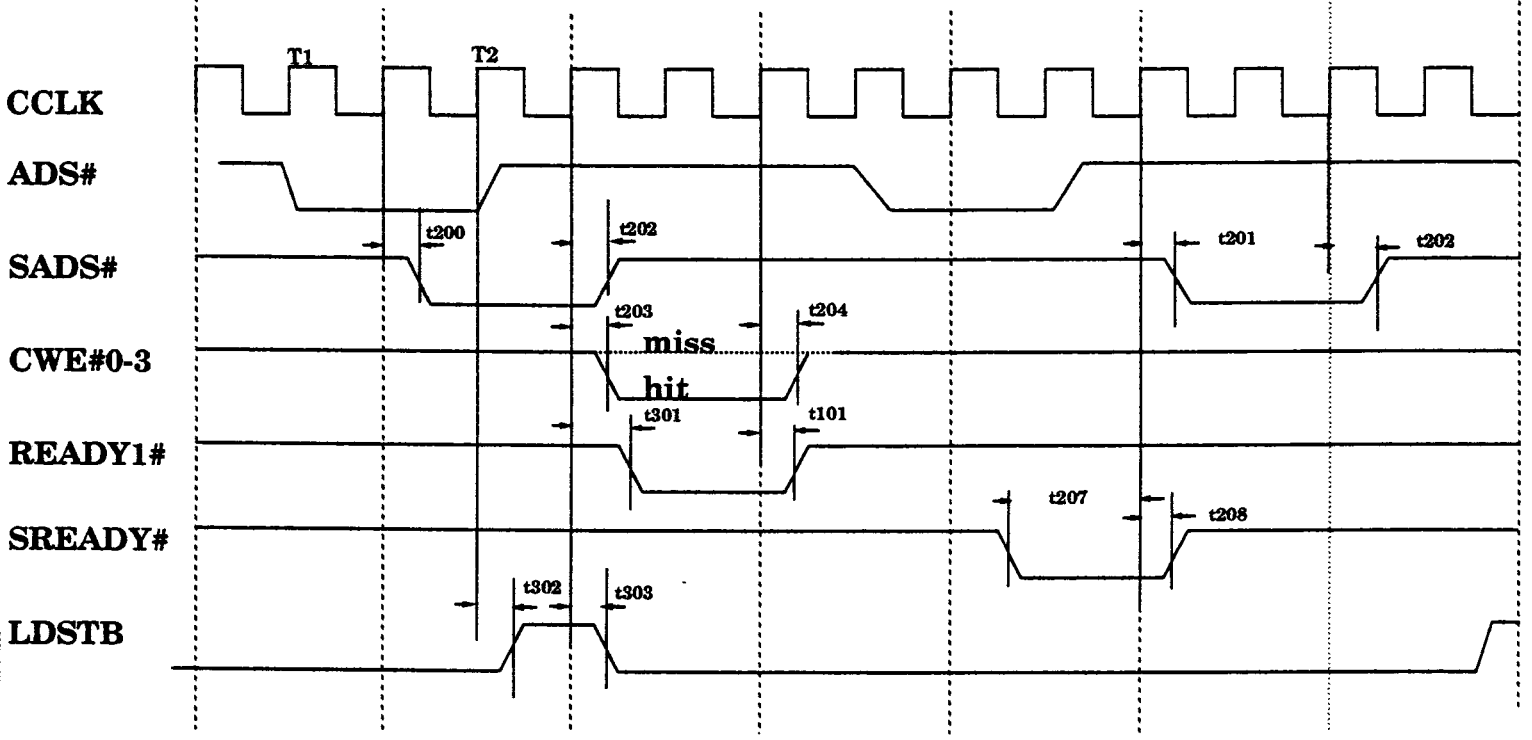


Read Miss Cycle, 1 wait state write option

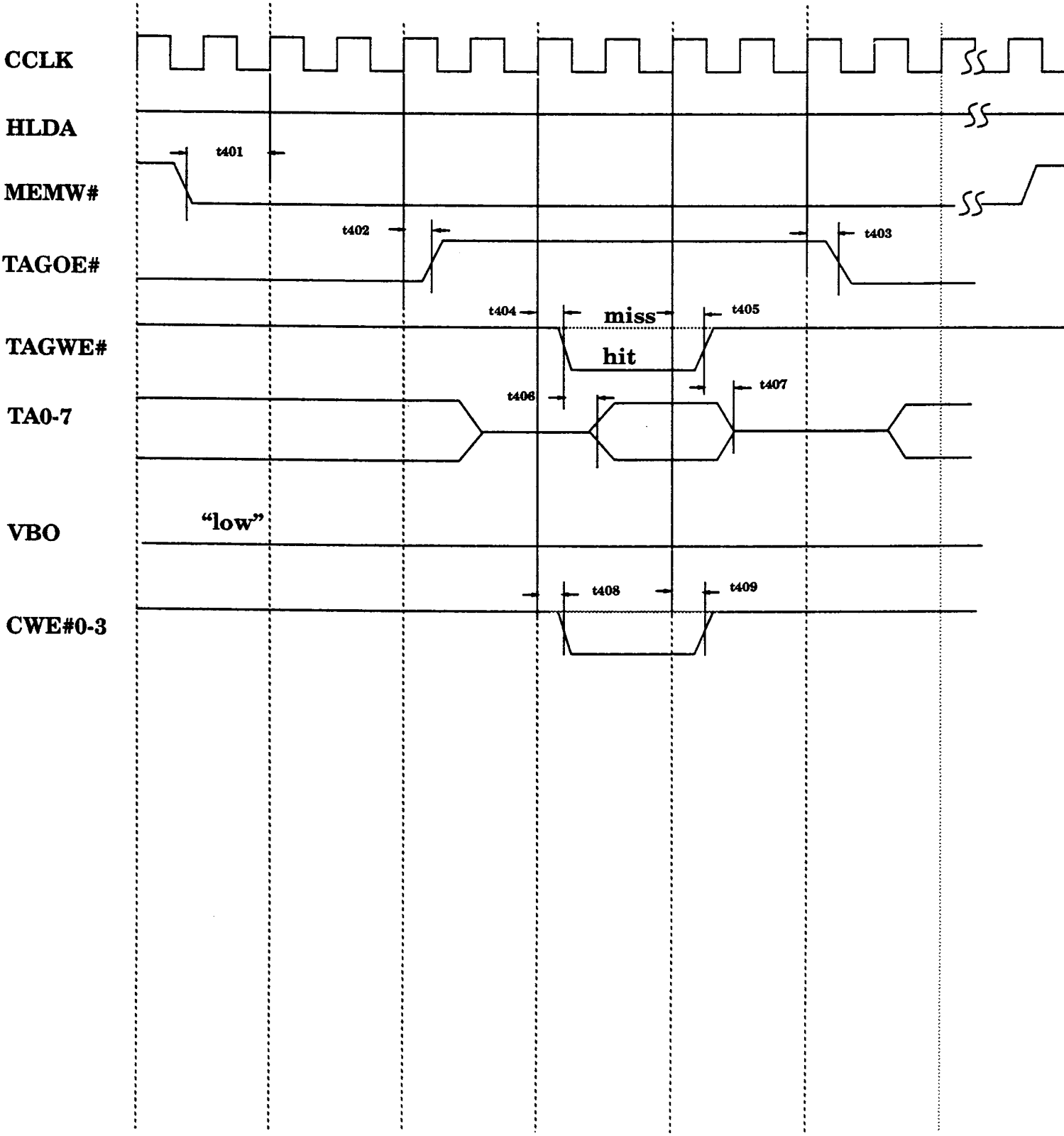
Buffered write followed by write, 0 wait state write



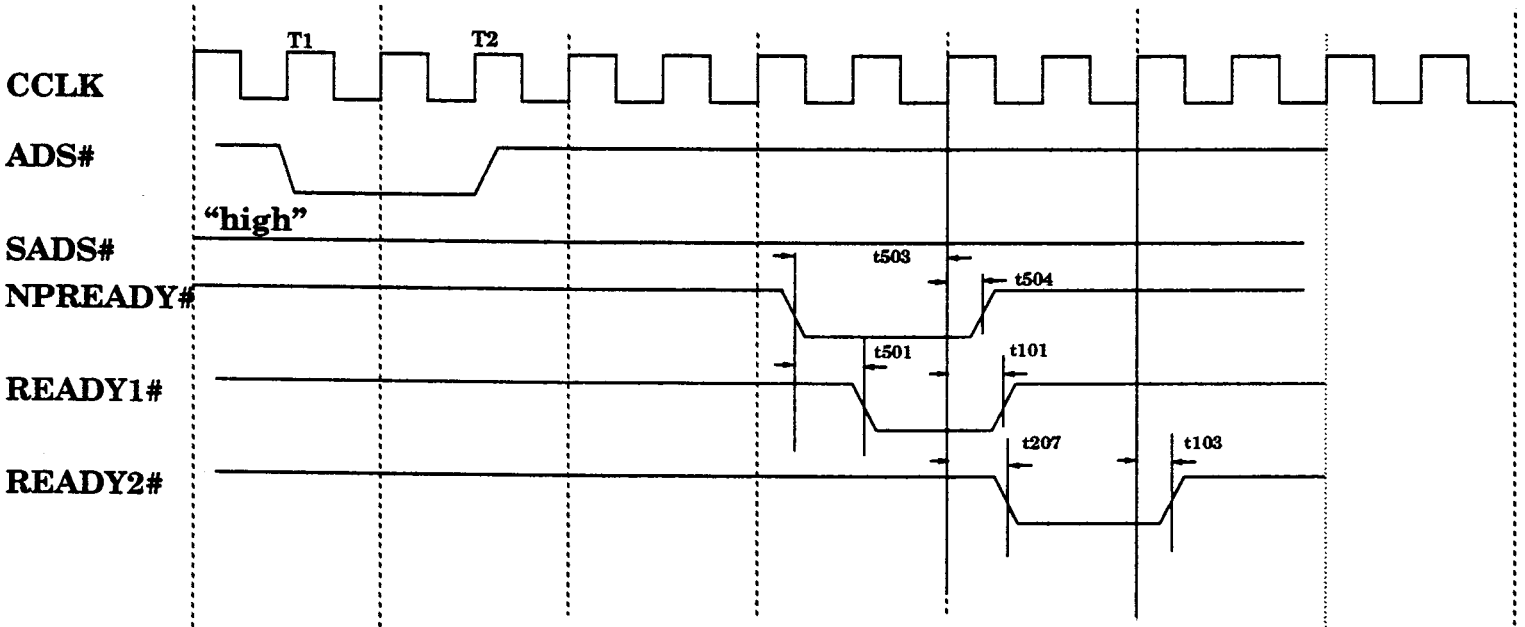
Buffered write followed by write, 1 wait state write



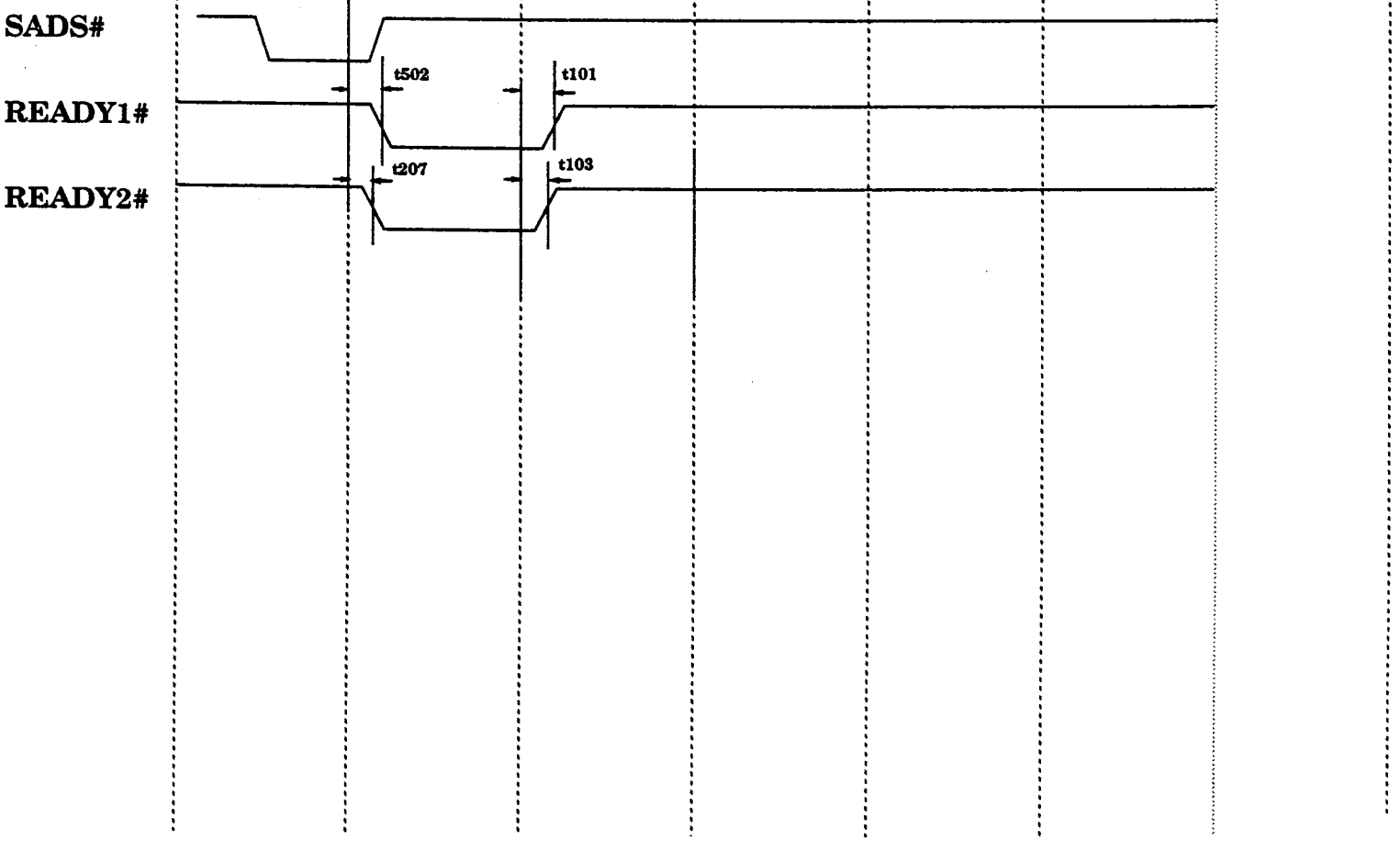
DMA/Master Memory Write



NP/Weitek cycle - NP/Weitek present

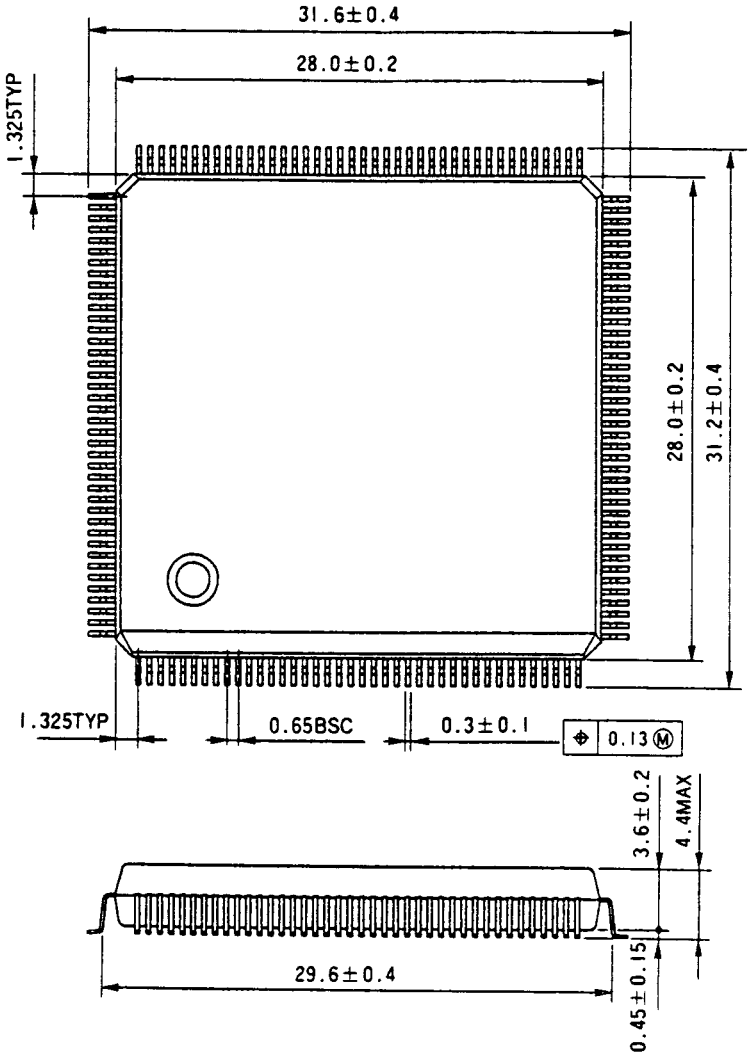


NP/Weitek cycle - NP/Weitek not present



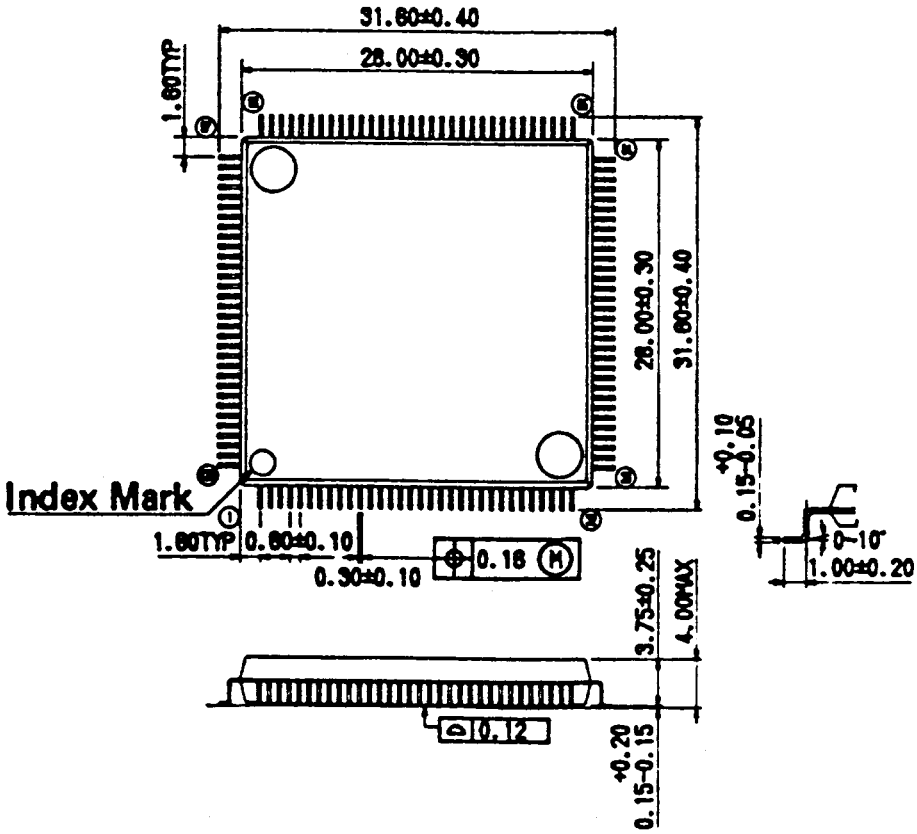
160-Pin Plastic Flat Package
for SL82C461
SL82C361
SL82C362

Unit: mm



128-Pin Plastic Flat Package for SL82C362SX

Unit: mm



100-Pin Plastic Rectangular Flat Package for SL82C465 SL82C365

Unit: mm