ST62BC001-B
SYS: System Controller

FEATURES:

- Dual clock oscillators
- Divided by 3 and 6 clock for PCLK and DMACLK
- Early RAS signal for DRAM
- Early WE signal for DRAM
- Early OE signal for BIOS ROM
- 2 wait state operation for 16-bit I/O
- 2 clock command delay function
- 6 wait state operation for 8-bit I/O
- 1.5 µm BiCMOS technology
- 68 pin PLCC PACKAGE

DESCRIPTION:

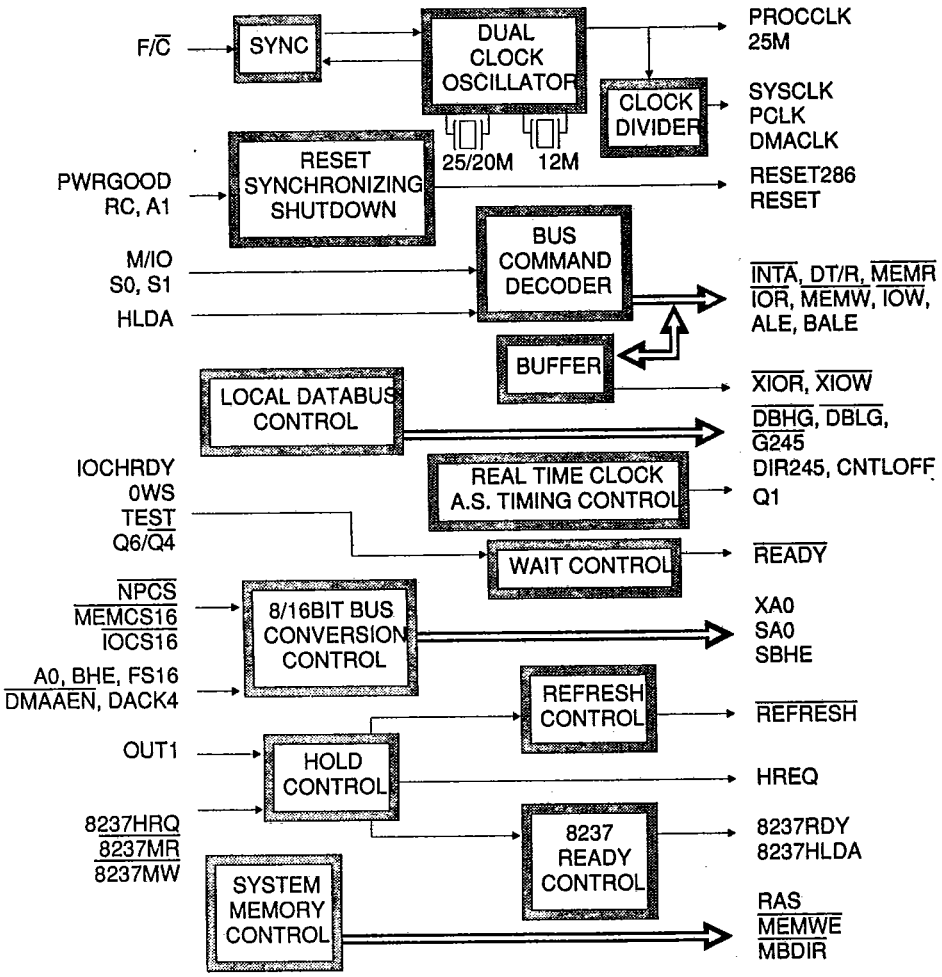
The ST62BC001–B generates control signals and clocks for 80286 CPU. It functions as a system controller and sends control signals to other parts of the system.

The ST62BC001–B provides a reset synchronization circuit for smooth operation. It decodes status signal and generates READY signal for 80286 CPU. The chip's various operation of 8, 16 bits memory and I/O cycles are controlled by the wait state control circuit. Refresh signal is asserted during refresh cycle.

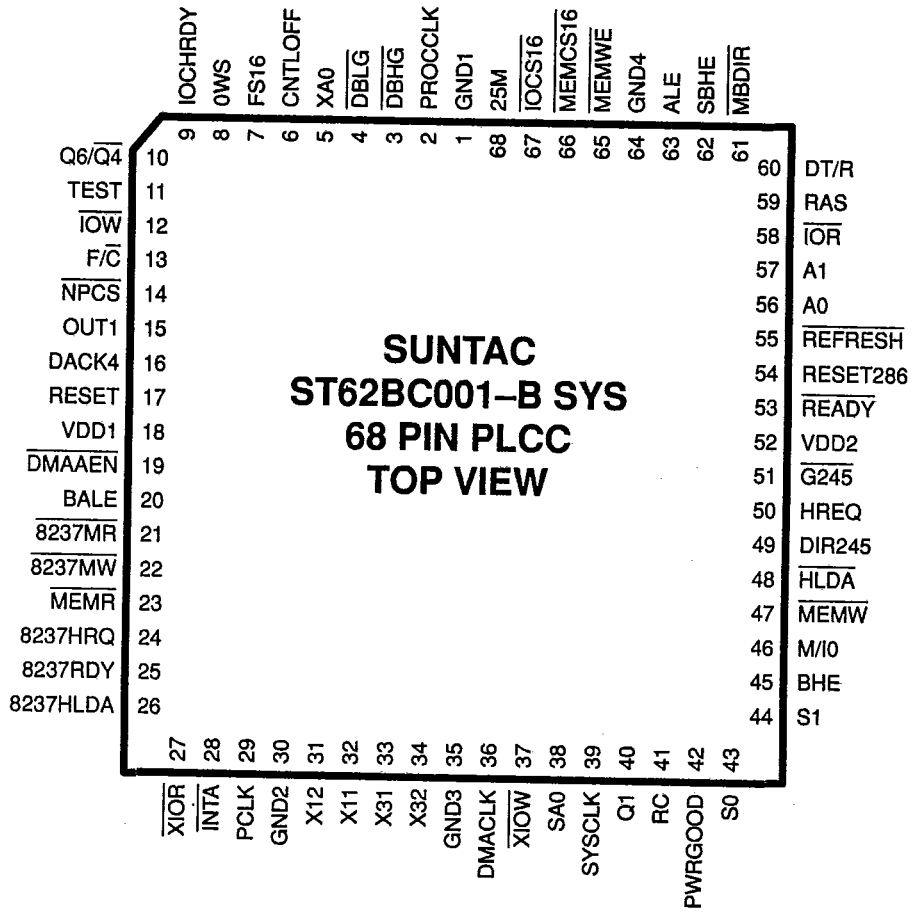
The ST62BC001–B provides memory control circuitry to allow for reliable operation at high speed (12.5MHz)and fast accessing of the memory system. It secures sufficient memory access time by implementing early RAS, early WE and early OE timing control. A memory system timing diagram is included in this section of the manual.

For reliable low speed peripheral I/O operation under high speed CPU clock, the ST62BC001–B provides functions of PCLK and DMACLK divisions by 3 and 6, 8-bit I/O 6 wait state circuit, 16-bit I/O 2 wait state circuit, and 2-cycle command delay for a recovery time of more than 200nsec for $\overline{IOR}$ and $\overline{IOW}$ signals.

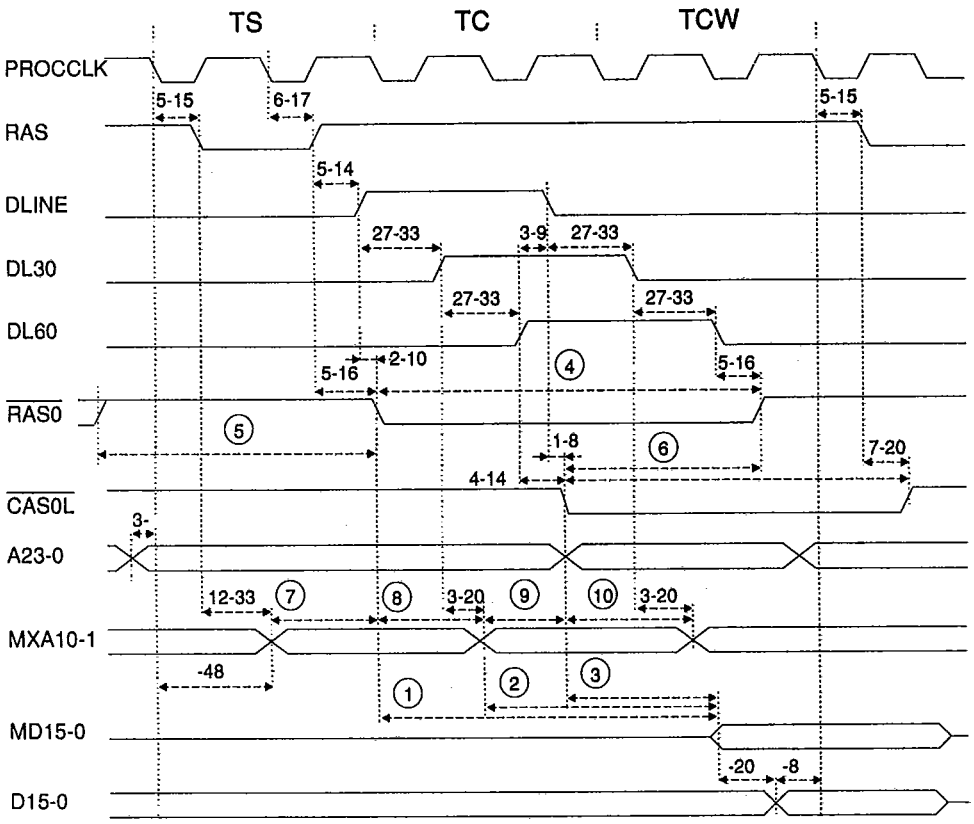
ST62BC001-B FUNCTIONAL BLOCK DIAGRAM



ST62BC001-B PIN DIAGRAM



MEMORY SYSTEM TIMING DIAGRAM



ST62BC001-B
Pin Description

Symbol	Pin No.	Type	Functions
$\overline{\text{MEMW}}$	47	I/O	I/O Terminal indicating that the data for memory device is being outputted to data bus.
$\overline{\text{MEMR}}$	23	I/O	I/O terminal instructing memory device to output data to data bus.
$\overline{\text{IOW}}$	12	I/O	I/O terminal indicating that the data for I/O device is being outputted to data bus.
$\overline{\text{IOR}}$	58	I/O	I/O terminal instructing I/O device to output data to data bus.
S0	43	I	Connects to 80286 status signal "S0".
S1	44	I	Connects to 80286 status signal "S1".
$\overline{\text{NPCS}}$	14	I	Connects to chip select signal of 80287.
M/IO	46	I	Connects to 80286 status signal "M/IO".
$\overline{\text{READY}}$	53	O	Output terminal indicating the end of bus cycle currently executed. This output is open collector output and requires 470 ohms external resistor.
HLDA	48	I	Connects to 80286 hold acknowledge signal "HLDA".
RESET	17	O	Active high output signal indicating system reset.
X31	33	I	Connects to low clock XTAL (12MHz).
X32	34	O	Connects to low clock XTAL (12MHz).
X11	32	I	Connects high clock rate XTAL (25/20MHz).
X12	31	O	Output terminal, connects to high clock XTAL (25/20MHz).
SYSCLK	39	O	Output signal of system clock, with a frequency of "PROCCLK" frequency divided by 2.
PROCCLK	2	O	Clock pulse for 80286. This terminal requires an external pull-up resistor of 220 ohm.

Symbol	Pin No.	Type	Functions
A0	56	I	Input terminal connects to 80286 address bus, "A0".
A1	57	I	Input terminal connects to 80286 address bus, "A1".
RESET286	54	O	Reset signal output for 80286.
BHE	45	I	Input terminal, connects to "BHE" signal which indicates 80286 high data bus, D8-D15 to be valid.
IOCHRDY	9	I	Input terminal, connects to "IO READY" signal; indicating the end of either access cycle to memory on I/O slot or I/O devices.
$\overline{8237MR}$	21	I	Input terminal, connects to "$\overline{MEMR}$" signal of 8237.
8237RDY	25	I	Input terminal, connects to "READY" signal of 8237.
$\overline{DMAAEN}$	19	I	Input signal indicating address signal of 8237 output to be valid during DMA cycle.
XA0	5	I/O	I/O terminal connects to internal I/O address bus, "XA0".
DMACLK	36	O	Clock signal for DMA controller 8237. The clock frequency is system clock frequency divided by 2.
PCLK	29	O	Clock signal for IC 8742. The clock frequency is PROCCLK frequency divided by 2.
$\overline{XIOR}$	27	I/O	I/O signal instructing internal I/O device to output data to data bus.
$\overline{XIOW}$	37	I/O	I/O signal indicating data for internal I/O device being outputted to data bus.
DACK4	16	I	Active high input signal to acknowledge DMA request for DMA controller (No.2) CH0 has been received
BALE	20	O	Active high output signal indicating data on address bus is valid.

Symbol	Pin No.	Type	Functions
SA0	38	I/O	I/O terminal, connects to system address bus, "SA0".
SBHE	62	I/O	Active low I/O signal , indicating SD8-SD15 of system data bus is valid.
8237HLDA	26	O	Output terminal, connects to 8237 hold acknowledge HLDA.
RC	41	I	Input terminal, to software reset CPU80286 by keyboard controller 8742.
PWRGOOD	42	I	Input terminal, connects to "POWERGOOD" signal which goes high after 100ms delay after system power is stabilized.
0WS	8	I	Active low input signal of active low to cancel wait state inserted into the bus cycle.
TEST	11	I	This terminal must keep low level.
Q6/$\overline{Q4}$	10	I	Input terminal selecting either 4 or 6 wait state for memory and 8-bit I/O operation.
$\overline{IOCS16}$	67	I	Active low input signal of active low signal, "$\overline{IOCS16}$", indicating 16-bit I/O operation.
$\overline{MEMCS16}$	66	I	Active low input terminal of active low signal, "$\overline{MEMCS16}$", indicating the memory operation on I/O slot is 16-bit.
$\overline{REFRESH}$	55	I/O	I/O terminal, connects to "$\overline{REFRESH}$" signal indicating refresh cycle.
8237HRQ	24	I	Input terminal, connects to hold request signal from 8237, "HREQ".
OUT1	15	I	Input terminal, connects to refresh request signal from counter 8254, "OUT1".
F/$\overline{C}$	13	I	When at "H" level, high rate XTAL is selected.
V_{DD}	18,52	...	+5V.
GND	1,35 64,30	...	To be connected to system ground.
$\overline{8737MW}$	22	I	Input terminal, connects to "$\overline{MEMW}$" signal of 8237.

Symbol	Pin No.	Type	Functions
$\overline{DBLG}$, $\overline{DBHG}$ CONTLOFF $\overline{G245}$, DIR245, DT/R	4, 3, 6 51, 49 60	O	Output control signal for system data bus "D0-D15, SD0-SD15, MD0-MD15.
FS16	7	I	Input terminal, connects to "FS16" signal indicating system memory Read/Write cycle.
$\overline{INTA}$	28	O	Output terminal, connects to "$\overline{INTA}$" signal indicating interrupt acknowledge cycle.
Q1	40	O	Output terminal, connects to "Q1" signal of ST62C005-B.
HREQ	50	O	Output signal indicating hold request to 80286.
RAS	59	O	Output signal indicating the start of a bus cycle, this is an active high signal.
$\overline{MBDIR}$	61	O	Output signal instructing system memory device to output data to data bus.
ALE	63	O	Address latch enable signal.
$\overline{MEMWE}$	65	O	Output terminal, connects to "$\overline{WE}$" of DRAM.
25M	68	O	25M is TTL level output of "PROCCLK"