SIS 85C330

Data Buffer

Rev 1.1

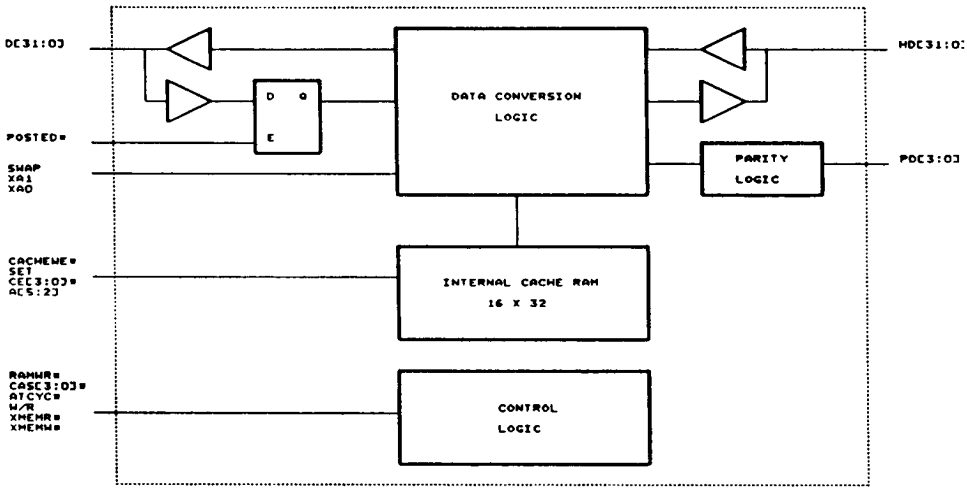
Preliminary

FEATURES

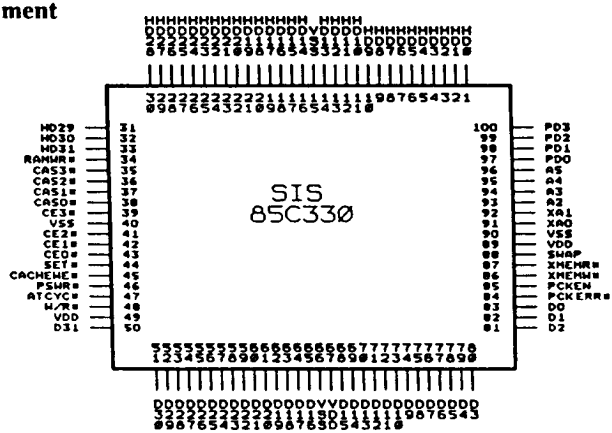
- Provides 32 Bits Data Buffer between CPU and 386 AT System
- Provides 128 Bytes Internal Cache Memory
- Bus Conversion and Swap Logic for 32 Bits, 16 Bits and 8 Bits Transfers in CPU and DMA Cycles
- Parity Generation and Detection Logic
- Data Latch in Posted Write Cycle
- 100-Pin Plastic QFP

The SIS 85C330 is designed to provide the bi-directional data buffers between the CPU and the peripherals. It performs all the necessary data conversion and byte swap logic during DMA and CPU cycles. The 85C330 also provides the parity generation and detection logic for the local memory read/write. Additionally, 128-byte internal cache SRAM is integrated in SIS 85C330 to enhance the system performance when external cache memory is not used.

Functional Block Diagram



Pin Assignment



Pin Description

Pin No.	Type	Symbol	Description
50-65 68-83	I/O	D<31:16> D<15:0>	LOCAL DATA BUS: The 32 Bit data bus is connected to CPU and is only activated in CPU read cycle (except external cache read) and DMA write cycle.
33-16 14-1	I/O	HD<31:14> HD<13:0>	MEMORY DATA BUS: The 32 Bit data bus is connected to DRAM or ROM directly and is buffered into system data bus.
100-97	I/O	PD<3:0>	DRAM PARITY BIT:These pins generate parity bits in memory write cycle and accept parity bits in memory read cycle.
96-93	I	A<5:2>	ADDRESS: These addresses inputs are used for selecting the internal cache.
34	I	RAMW#	RAM WRITE ENABLE: Active low DRAM write enable input.
35-38	I	CAS3#- CAS0#	CAS ENABLE: These are column address enables. An active low input indicates the corresponding byte is accessed.
39 41-43	I	CE3# CE<2:0>	CACHE ENABLE: Chip enable signals of cache RAM. When activated, they enable respective bytes of internal cache. These inputs should be tied high when external cache is used.
44	I	SET#	CACHE BANK SELECT: This signal determines which bank of cache RAM is selected in a two-way cache mapping.
45	I	CACHEWR#	CACHE WRITE ENABLE: Active low input indicating a write to cache memory.
46	I	PSWR#	POSTED WRITE: This is a synchronized input indicating a post write is on going. It is used to latch data for the posted write cycle.
47	I	ATCYC#	IO BUS CYCLE: This is a synchronized input indicating a cycle that is neither a local memory nor a cache memory.
48	I	W/R#	WRITE/READ: This signal determines whether it is a write or a read cycle during CPU cycle.
87	I	XMEMR#	BUS MASTER MEMORY READ: This input is only accepted during DMA or MASTER cycle.

86	I	XMEMW#	BUS MASTER MEMORY WRITE: This input is only accepted during DMA or MASTER cycle.
88	I	SWAP	SWAP:This signal indicates data should be swapped between different bytes. This signal is always active during DMA 8 bits transfer and is active only when XA0 is high in AT cycle.
92	I	XA1	AT bus address 1.
91	I	XA0	AT bus address 0.
85	I	PCKEN	PARITY CHECK ENABLE: This signal enables the parity check logic when in high state.
84	O	PARERR#	PARITY CHECK OUTPUT: A low output means there is a parity error.
89,67,49	I	VDD	+5V
90,66, 40,15	I	VSS	Ground

Functional Description

The SIS 85C330 has the following function block as illustrated in Fig 3.1:

- Data buffers and latches
- Bus conversion logic
- Parity generation and detection
- Internal cache RAM

Data Buffers and Latches

The SIS 85C330 provides buffering between the local data bus (D0-D31) and the memory data bus (HD0-HD31). Local data bus connects to the CPU, co-processor, and system cache RAM. Memory data bus connect to the system DRAM and the lower two bytes (HD0-HD15) are buffered into the system data bus on the I/O slots.

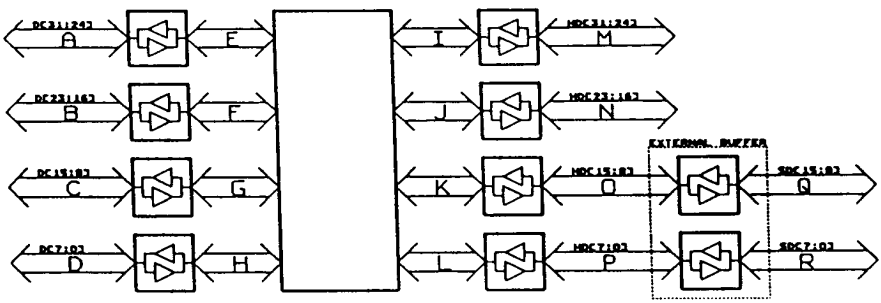
The data from the CPU is latched by PSWR# when the posted cycle is active.

Bus Conversion Logic

The SIS 85C330 provides 16 bit to 8 bit or 8 bit to 16 bit data bus conversion in AT cycle. It also provides the conversion between 32, 16 and 8 bit data bus in DMA cycle. The data conversion is controlled by SWAP, XA1, and XA0 which are generated by the 85C320 or the DMA controller. The conversion logic is listed in the following table.

XA1	XA0	SWAP	Operation	Data Path	PD Gen.	PD Chk
X	0	0	AT Write	C-G-K-O-Q and D-H-L-P-R		
			AT Read	Q-O-K-G-C and R-P-L-H-D		
X	1	1	AT Write	C-G-L-P-R		
			AT Read	R-P-L-G-C		
0	0	1	DMA MEMW#	R-P-L-H-D	PD0	
			DMA MEMR#			PD0
0	1	1	DMA MEMW#	R-P-L-K-O and R-P-L-G-C	PD1	
			DMA MEMR#	Q-K-L-P-R		PD1
1	0	1	DMA MEMW#	R-P-L-J-N and R-P-L-F-B	PD2	
			DMA MEMR#	N-J-L-P-R		PD2
1	1	1	DMA MEMW#	R-P-L-I-M and R-P-L-E-A	PD3	
			DMA MEMR#	M-I-L-P-R		PD3
0	X	0	DMA MEMW#	R-P-L-H-D and Q-O-K-G-C	PD0,PD1	
			DMA MEMR#			PD0,PD1
1	X	0	DMA MEMW#	R-P-L-J-N R-P-L-F-B Q-O-K-I-M and Q-O-K-E-A	PD2,PD3	
			DMA MEMR#	N-J-L-P-R and M-I-K-O-Q		PD2,PD3

Data Path Diagram



Parity Generation and Detection

For the system DRAM write cycles, the 85C330 generates even parity for each of the four bytes. During the system DRAM read cycles, the 85C330 checks for even parity for each HD byte read. If the parity is detected as being odd, the 85C330 will flag a parity error on the PARERR# output. The parity detect logic is enabled by the PCKEN.

Internal Cache RAM

The 85C330 provides 128 bytes SRAM to support the built-in cache function. Without external cache RAM, the CPU can use this SRAM as a small cache and access it in 0 wait state operation. This can greatly enhance the system performance.

Electrical Characteristics

Absolutely Maximum Ratings

Parameter	Min	Max	Unit
Ambient Operating Temperature	0	70	°C
Storage Temperature	-55	125	°C
Input Voltage	-0.5	5.5	V
Output Voltage	-0.5	5.5	V

Note: Stress above these listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics: (T_A = 0°C-70°C, V_{DD} = 5V±5%, V_{SS} = 0V)

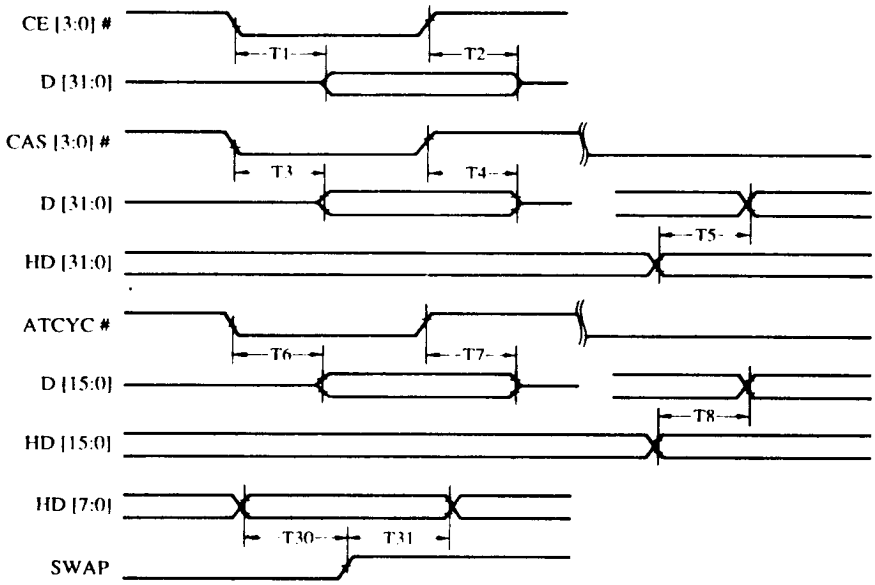
Sym	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA	0.45	V	
V_{OH}	Output High Voltage	I_{OH} = -1mA	2.4	-	V
I_{IL}	Input Leakage	0 < V_{IN} < V_{DD}	-	±10	uA
I_{OZ}	Tri-state Leakage	0.45 < V_{OUT} < V_{DD}		±20	uA

AC Characteristics: (T_A = 0°C-70°C, V_{DD} = 5V±5%, V_{SS} = 0V)

Sym	Description	Min.	Max.	Units
T1	D data valid delay from CE# active	11	25	ns
T2	D data float delay from CE# inactive	4	20	ns
T3	D bus active delay from CAS# active	11	20	ns
T4	D bus float delay from CAS# inactive	5	20	ns
T5	D data valid delay from HD data valid	6	25	ns
T6	D bus active delay from ATCYC# active	11	48	ns
T7	D bus float delay from ATCYC# inactive	6	23	ns
T8	D data valid delay from HD data valid	8	20	ns
T9	D bus active delay from CAS# inactive in DMA	10	43	ns
T10	D bus float delay from CAS# inactive in DMA	5	20	ns
T11	D data valid delay from HD data valid in DMA	8	39	ns
T12	HD bus active delay from RAMW# active	11	25	ns
T13	HD bus float delay from RAMWR# active	6	23	ns
T14	HD data valid delay from D data valid	7	26	ns
T15	HD bus active delay from MEMW# active	10	50	ns
T16	HD bus float delay from MEMW# active	5	21	ns
T17	HD data valid delay from HD data valid	9	40	ns
T18	HD bus active delay from MEMR# active	11	54	ns
T19	HD bus float delay from MEMR# adtive	5	21	ns
T20	HD data valid delay from HD data valid	9	36	ns
T21	HD bus active delay from ATCYC# active	10	43	ns
T22	HD bus float delay from ATCYC# active	5	20	ns
T23	HD data valid delay from D data valid	8	25	ns
T24	PD bus active delay from MEMW#active	10	40	ns
T25	PD bus float delay from MWME# active	4	18	ns
T26	PD data valid delay from HD data valid	18	87	ns
T27	PD bus active delay from RAMWR# active	7	37	ns
T28	PD bus float delay from RAMWR# active	4	16	ns
T29	PD data valid delay from D data valid	10	47	ns
T30	HD data set up time to SWAP rising	0		ns
T31	HD data hold time after SWAP rising	7		ns
T32	D data set up time to POSED# falling	0		ns
T33	D data hold time after POSED# falling	4		ns
T34	D data set up time in cache write	3		ns
T35	D data hold time in cache write	1		ns
T36	PCK# active delay from CAS# inactive		27	ns

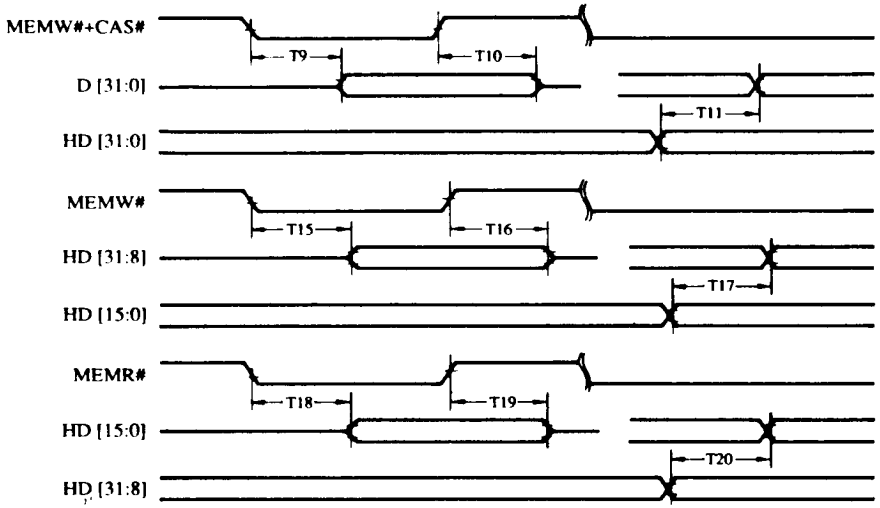
Timing Diagram

Read Cycle:



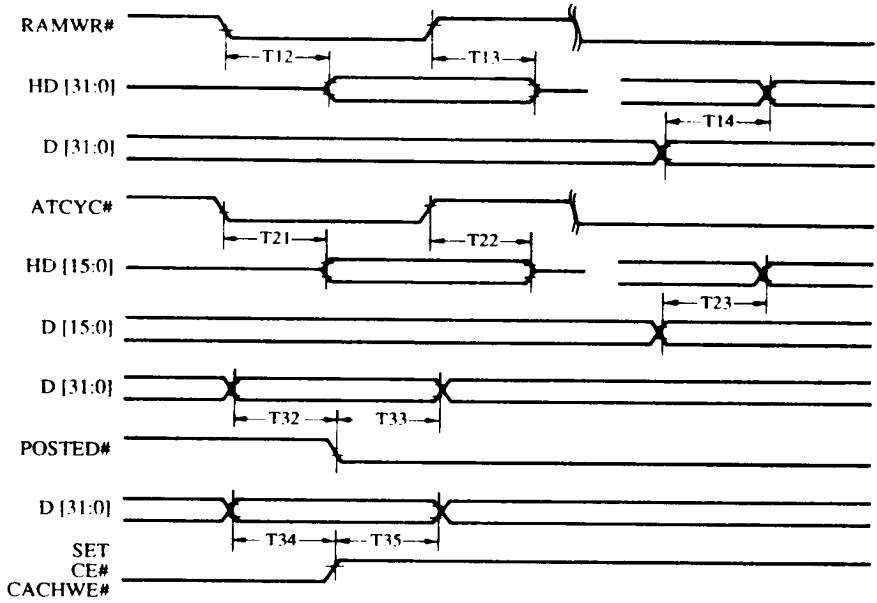
Timing Diagram

DMA Cycle:



Timing Diagram

Write Cycle:



Timing Diagram

Parity Generation: