SIS 85C320

Bus Controller

Rev 1.1

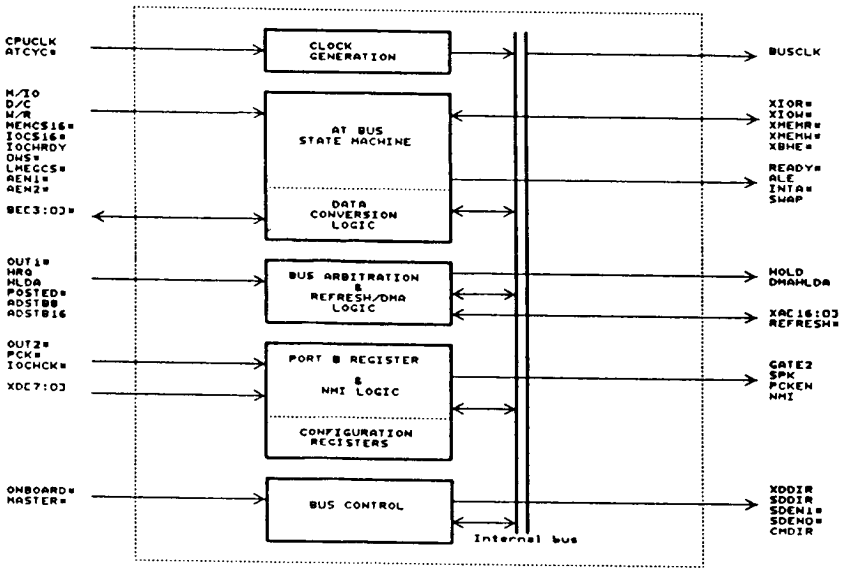
Preliminary

FEATURES

- Clock Generation with Software Speed Selection (1/2, 1/3 or 1/4 System Clock)
- AT Bus State Machine and AT bus control
- Programmable Wait State Generation:
  - 1 or 2 Wait State for 16 Bits Transfer
  - 4 or 5 Wait State for 8 Bits Transfer
- Supports 82C206 or VL82C100
- DMA and Bus Arbitration Logic
- Provides 7.16MHz or 4.77MHz DMA Clock
- Bus Refresh Control Logic
- Data Conversion Control Logic
- Port B Register and NMI Logic
- Two Programmable I/O Pins
- Provides 7.16MHz Keyboard Clock
- 100-Pin Plastic QFP

The SIS 85C320 is a highly integrated AT Bus Controller for 386 based systems. All signals are synchronized with the bus clock so that solid compatibility can be achieved. Besides, the SIS 85C320 has simple interface to other system logic and thus can also be used independently.

Functional Block Diagram



Functional Description

The SIS 85C320 has the following function blocks as illustrated in Figure 2.1:

- Clock generation
- AT bus state machine and data conversion logic
- Refresh, DMA and bus arbitration
- Port B register & NMI Logic
- Configuration register

System Synchronization and Bus Clock Generation

The SIS 85C320 synchronizes itself with the CPU using ATCYC#. Only when ATCYC# is detected active will the 85C320 start a bus cycle. Bus clock will be synchronized with ATCYC# and all subsequent bus control signals are synchronized with the bus clock.

The bus clock is default to be 1/4 of system clock. It can be programmed to be 1/2 or 1/3 of system clock.

AT Compatible Bus

All bus control signals are synchronized with bus clock.

16 bit transfer is default to 1 wait state and can be selected to be 2 wait states. 0WS# input is sampled during 16 bit transfer only.

8 bit transfer is default to be 4 wait states and can be selected to be 5 wait states.

READY# is asserted at the end of command cycle and it will be sampled by 85C310 to terminated the current CPU cycle. For bus I/O write or memory write cycle, READY# is asserted one system clock later than the deactivation of the bus command thus providing one system clock address and data hold time on the bus.

For bus read cycles, READY# is asserted in such a way that the current bus cycle and CPU cycle terminates simultaneously.

Bus Swap

85C320 handles only 16 bit - 8 bit data swap. 32 bit data swap is handled by 80386 as the 85C310 asserts BS16# during all bus cycles.

During CPU cycles, SWAP is active only at the second phase of a conversion cycle when XA0 is 1. However during 8 DMA cycles, SWAP will also be active to control data swap in 85C330.

Refresh, DMA and Bus Arbitration

The SIS 85C320 provides bus arbitration between the CPU, DMA and DRAM refresh logic. It handles HRQ, REFREQ, and ATCYC# and arbitrates them in a preemptive manner. The 85C320 will issue REFRESH# or DMAHLDA in respond to REFREQ or HRQ, otherwise, it enters AT cycle or keeps idle. Because local memory bus and AT system bus are both independent, the 85C320 provides a hidden refresh function to refresh DRAM on AT bus only. Local memory can be refreshed during AT bus cycle and bus memory can be refreshed during non bus cycle. This method will save much time spend on refreshing and increase system performance.

The 85C320 will not relinguish HOLD upon receiving REFREQ. REFREQ will be latched and sampled by BUSCLK and arbitrated it with HRQ and ATCYC#. If there are no AT bus cycle and DMA cycle, the 85C320 will issue REFRESH# addressA0-A9 and XMEMR# whick are needed to execute bus refresh. If there is a bus cycle or DMA cycle, refresh will wait until these cycle is finished.

The start of DMA cycle may be delayed by POSTED#. The generation of DMAHLDA will be postponed if POSTED# is active even when the CPU has already relinguished the bus and HLDA is active.

Port B Register and NMI Logic

The SIS 85C320 provides access to Port B defined for IBM PC/AT as shown.

Bit	Contents
0	GATE2 - Timer 2 Gate
1	SPKEN - Speaker Data
2	PCKEN - Parity Check Enable
3	IOCHCKEN - I/O Channel Check Enable
4	REFRESH - Refresh Detect
5	OUT2 - Timer 2 Out
6	IOCHCK - I/O Channel Check
7	PCK - Parity Check

The NMI logic performs the latching and enabling of I/O and parity error condition and will generate a non-maskable interrupt to the CPU if NMI is enabled. Enabling and disabling of NMI is accomplished by writing to I/O address 070H. NMI is enabled if data bit 7 (XD7) is equal to 0 and disabled if XD7 is equal to 1.

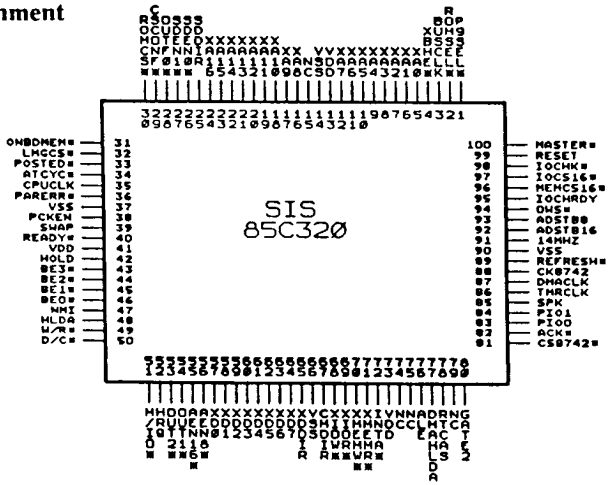
Programmable I/O

To use PIO0 and PIO1, first set Config Register Bit 6 of 85C320 to 0. The following table describes the usage of these two pins.

PIO Register Port 463H (Write only)			
Bit 0	Bit 1	PIO0	PIO1
0	0	DISABLE	DISABLE
0	1	DISABLE	ENABLE
1	0	ENABLE	DISABLE
1	1	ENABLE	ENABLE

PIO Register Port 863H Read/Write			
Bit 0	Bit 1	PIO0	PIO1
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Pin Assignment



Pin Description

Pin No.	I/O	Symbol	Descripton
35	I	CPUCLK	CPU CLOCK: This clock should be synchronized with the CLK2 of 80386.
51	I	M/IO#	MEMORY I/O DEFINITION: A high level input indicates a memory cycle and a low level indicates an I/O cycle.
50	I	D/C#	DATA/CODE DEFINITION: A high level input indicates a data cycle and low level indicates a code cycle. It is used to determine a halt or shutdown cycle.
49	I	W/R#	WRITE/READ DEFINITION: A high level input indicates a write cycle and low level indicates a read cycle. During DMA cycles, this signal should be held high.
43-46	I/O	BE<3:0>#	BYTE ENABLE: These active low signals determine the bytes to be accessed during CPU cycles or DMA cycles. During CPU cycles, they are decoded to generate XA0, XA1 and XBHE. During DMA or Master cycles, the action is reversed.
48	I	HLDA	HOLD ACKNOWLEDGE: This signal indicates that CPU has released the control of bus. 85C320 arbitrates this signal with POSTED and Refresh to generate DMAHLDA to DMA controller. HLDA will be held until POSTED or refresh cycle is finished. HLDA will block refresh cycle if DMA cycle has already started.
42	O	HOLD	HOLD REQUEST: This signal outputs to CPU to request for the control of bus. This signal is active until DMA cycle is fully completed.
40	O	READY#	AT BUS READY : This signal indicates the end of AT bus cycle.
47	O	NMI	NON MASKABLE INTRERRUPT : This is an active high output to CPU and is used to invoke a non-maskable interrupt.

Pin No.	Type	Symbol	Description
34	I	ATCYC#	AT CYCLE: This is an active low input. When active, 85C320 will initiate a memory, I/O or interrupt acknowledge cycle determined by M/IO, D/C and W/R.
33	I	POSTED#	POSTED: This signal indicates a posted cycle. If there is HLDA generated during posted cycle, HLDA will be held and DMAHLDA will not be generated until the end of posted cycle .
38	O	PCKEN	PARITY CHECK ENABLE : This is used to enable parity check logic in 85C330.
36	I	PARERR#	PARITY ERROR: This signal indicates a parity error has occured in DRAM data. NMI will be generated if enabled.
39	O	SWAP	SWAP: This signal indicates when the data should be swapped. It is always active in 8 bit DMA transfer and is active only when XA0 is high during AT cycle.
31	I	ONBDMEM#	LOCAL MEMORY DECODE: This is an address decode input indicating local memory is selected.
32	I	LMGCS#	1 MEG SELECT: This is an address decode input indicating the first 1 megabyte address is selected.
30	I	ROMCS#	ROM DECODE: This is an address decode input indicating BIOS space is selected.
2	I	ROMSEL#	ROM SELECT: This input signal indicates whether the BIOS ROM is placed on the local memory bus or XD bus. A low means local memory bus.
29	O	CSCONF#	CONFIGURATION CHIP SELECT: This signal is output to program the configuration register in 85C310.
5	I/O	XA0	X BUS ADDRESS 0: This pin outputs address 0 for AT bus during AT cycle and refresh cycle, and it is an address input during DMA cycle.
6	I/O	XA1	X BUS ADDRESS 1: This pin behaves in the same manner as XA0, it will be an address input during AT cycle if P9 mode is selected.
7-12	I/O	XA<2:7>	X BUS ADDRESS: These pins output address during refresh cycle and input address in other cases.
16	I/O	XA8	X BUS ADDRESS LINE : This pin outputs address during refresh cycle and 8 bit DMA cycle (AEN8 active), and inputs address in other cycles.
17	I/O	XA9	X BUS ADDRESS LINE : This pin outputs address during refresh cycle and DMA cycle, and it also inputs address in other cycles.
18-23	I/O	XA<10:15>	X BUS ADDRESS LINE : These pins output latched address during DMA transfer, and input address in other cycles.
24	O	XA16	X BUS ADDRESS LINE : This pin outputs the highest bit of the latched address during 16 bit DMA transfer.
57-64	I/O	XD<0:7>	X Bus Data Line D<0:7>.
76	O	ALE	ADDRESS LATCH ENABLE : This is an active high output on AT bus and is synchronized with the AT bus machine clock. It is used to control address latches and hold address during AT cycle.
72	O	INTA#	INTERRUPT ACKNOWLEDGE : This is an active low signal for interrupt controller. It is used to read interrupt vector from interrupt controller to the CPU.

Pin No.	Type	Symbol	Description
69	I/O	XIOR#	X BUS I/O READ : This is an active low signal used to strobe an I/O device to place data on data bus. This is an output signal during AT cycle and is an input in other cases.
68	I/O	XIOW#	X BUS I/O WRITE:This is an active low signal used to strobe data on the data bus into a selected I/O device. This is an output during AT cycle and is an input in other cases.
71	I/O	XMEMR#	X BUS MEMORY READ: This is an active low signal used to direct memory to place data on the data bus. This is an output during AT cycle and is an input in other cases.
70	I/O	XMEMW#	X BUS MEMORY WRITE: This is an active low signal used to write the data on the data bus into the memory selected. This is an output during AT cycle and is an input in other cases.
4	I/O	XBHE#	BYTE HIGH ENABLE:This is an active low signal indicating the high byte has valid data on the 16 bits data bus. This signal always outputs except in Master mode.
3	O	BUSCLK	BUS CLOCK:This is the system clock for AT bus I/O channel. The frequency of AT bus clock is software programmable, it can be programmed to be 1/2, 1/3, or 1/4 system clock. Default is 1/4 system clock, that means 8 MHz for 33 MHz system.
88	O	CK8742	8742 CLOCK : This is the clock for keyboard controller. The frequency of this clock is the half of 14.318 MHz.
91	I	14 MHz	14MHz: This is the input of 14.318 MHz. It is generated by an external oscillator and is used to generate the clock needed by keyboard controller, timer, and DMA controller.
86	O	TMRCLK	TIMER CLOCK : This is the 1.19 MHz clock output for timer.
87	O	DMACLK	DMA CLOCK : This is the clock for DMA controller. The frequency of this clock can be programmed to be 7.159 MHz or 4.773 MHz.
99	I	RESET	RESET : This is the Master Reset input used to initial all logic circuits and registers in this chip.
67	O	CMDIR	COMMAND DIRECTION : This signal determines the direction of the bus command buffer. Commands are normally output to slot, and input only in master mode except refresh cycle.
65	O	XDDIR	X DATA DIRECTION: The signal controls the direction of XD bus. XD bus is normally input from SD bus A high will set the data path from XD bus to SD bus.
25	O	SDDIR	S DATA DIRECTION : This signal controls the direction of SD bus, a high sets the data path from HD bus to SD bus, a low sets the data path from SD bus to HD bus.
26	O	SDEN0#	S DATA ENABLE:This is the enable signal of the low byte buffer of SD bus.
27	O	SDEN1#	S DATA ENABLE : This active low signal is used to enable the high byte buffer of SD bus.

Pin No.	Type	Symbol	Description
83,84	I/O	PIO<0:1>	PROGRAMMABLE I/O : These two pins are additional data I/O, they can be programmed to output data, once a bit for each pin, or they can be inputs if outputs are disabled. Data input can be read directly then.
52	I	HRQ	HOLD REQUEST:The Hold request comes from DMA controller. This signal will be transfered to CPU by HOLD after synchronization
77	O	DMAHLDA	DMA HOLD ACKNOWLEDGE: This signal outputs to DMA controller after arbitrating with refresh and POSTED when HLDA is active.
93	I	ADSTB8	ADDRESS STROBE: This signal latches DMA address A8-A15 from XD0- XD7 during 8 bit DMA transfer.
92	I	ADSTB16	ADDRESS STROBE: This signal latches DMA address A9-A16 from XD0- XD7 during 16 bit DMA transfer.
56	I	AEN8#	ADDRESS ENABLE:This is the address enable signal of 8 bit DMA cycle. It will enable XA8-XA15 and output the address latched from XD0-XD7.
55	I	AEN16#	ADDRESS ENABLE: This is the address enable signal of 16 bit DMA cycle. It will enable XA9-XA16 and output the address latched from XD0-XD7.
54	I	OUT1#	OUT 1:This is the output of the channel 1 of programmable Interval Timer and is used to request for the refresh cycle.
53	I	OUT2#	OUT2: This is the output of the channel 2 of Programmable Interval Timer and is used to generate speaker output . The state of this signal can be read from port B.
80	O	GATE2	GATE2: This is the output of the Bit 0 of port B register and is connected to the GATE2 of the Programmable Interval Timer.
78	O	RTCAS	ADDRESS STROBE OF RTC: This signal is used as the AS input of Real Time Counter.
81	O	CS8742#	KEY BOARD CHIP SELECT : This is the chip select signal decoded for keyboard controller.
28	O	OUTF0#	F0 OUTPUT :This signal outputs low state when system writes to F0 port. This signal is used to clear Coprocessor Busy.
89	I/O	REFRESH#	REFRESH: This is an active low signal. It will initiate refresh cycle and enable address A0-A9 outputs for the AT bus. This signal inputs only in Master mode.
100	I	MASTER#	MASTER: This is an active low signal from AT bus. This signal tells there is another microprocessor which has already taken over the control of the whole system.
95	I	IOCHRDY	I/O CHANNEL READY: This is an active high signal input from AT bus. When low, it indicates not ready condition and system will insert wait states in AT I/O or AT memory cycle. It will allow termination of current AT cycle when high.
94	I	0WS#	0 WAIT STATE: When this signal is active low, system will insert no wait state and terminate current cycle immediately. This signal is accepted in 16 bit transfer only, and ignored during 8 bit transfer.
97	I	IOCS16#	I/O CHANNEL SELECT 16: This is an active low input indicating a 16 bit I/O transfer. It implies an 8 bit I/O transfer if it is high .
96	I	MEMCS16#	MEMORY CHIP SELECT 16: This is an active low input indicating a 16 bit memory transfer. It implies an 8 bit memory transfer if it is high.

Pin No.	Type	Symbol	Description
98	I	IOCHCK#	I/O CHANNEL CHECK: This is an active low input from AT bus indicating there is an I/O error occured on the AT bus. NMI will be generated if enabled.
85	O	SPK	SPEAKER: This is the output for speaker.
82	O	ACK#	ACKNOWLEDGE: This signal is active low only in DMA transfer and refresh cycle, and is used to control the enable or direction of address, command, and data buffer. It is also used to disable peripheral I/O chips.
13,41,73	I	VDD	+5V
14,37, 66,90	I	VSS	Ground
1,15,74 75,79	--	NC	Reserved

Registers Configuration Specifications for 85C320

This chip set have internal registers for system configuration, and they are accessed through I/O port 022H and 023H. Port 022H is used as an indexing register and Port 023H is used as the data register. There are two configuration register in 85C320, these register are accessed by first writing the index 00H or 03H into Port 022H and immeddiately followed by a read or a write to Port 023H. There are two configuration registers in 85C310 that are accessed through 85C320. First writing index 83H into Port 022H and then followed with two continuous reads or writes to Port 023H will assert CSCONF# to access the configuration register in 85C310.

- **Register 00:**

Bit 0, 1

Bus Clock Speed Selection:

Bit 0	Bit 1
0	0 = 1/4 System Clock (default)
1	0 = 1/3 System Clock
0	1 = 1/2 System Clock
1	1 = Reserved

Bit 2

16-Bit AT Cycle Wait States:

0 = 1 Wait State (default)
1 = 2 Wait States

Bit 3

8-Bit AT Cycle Wait States:

0 = 4 Wait States (default)
1 = 5 Wait States

Bit 4

DMA Clock Selection

0 = 7.159 MHz (default)
1 = 4.773 MHz

Bit 5

Reserved

Bit 6

Pin 83, 84 Function Select:

0 = PIO Function Select (default)
1 = RTC R/W# and DS Function Select

Bit 7

Reserved

- **Register 03**

Reserved and should be set to 02H by BIOS

Electrical Characteristics

Absolutely Maximum Ratings:

Parameter	Min	Max	Unit
Ambient Operating Temperature	0	70	°C
Storage Temperature	-55	125	°C
Input Voltage	-0.5	5.5	V
Output Voltage	-0.5	5.5	V

Note: Stress above these listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characterisctics: (T_A = 0°C-70°C, V_{DD} = 5V±5%, VSS = 0V)

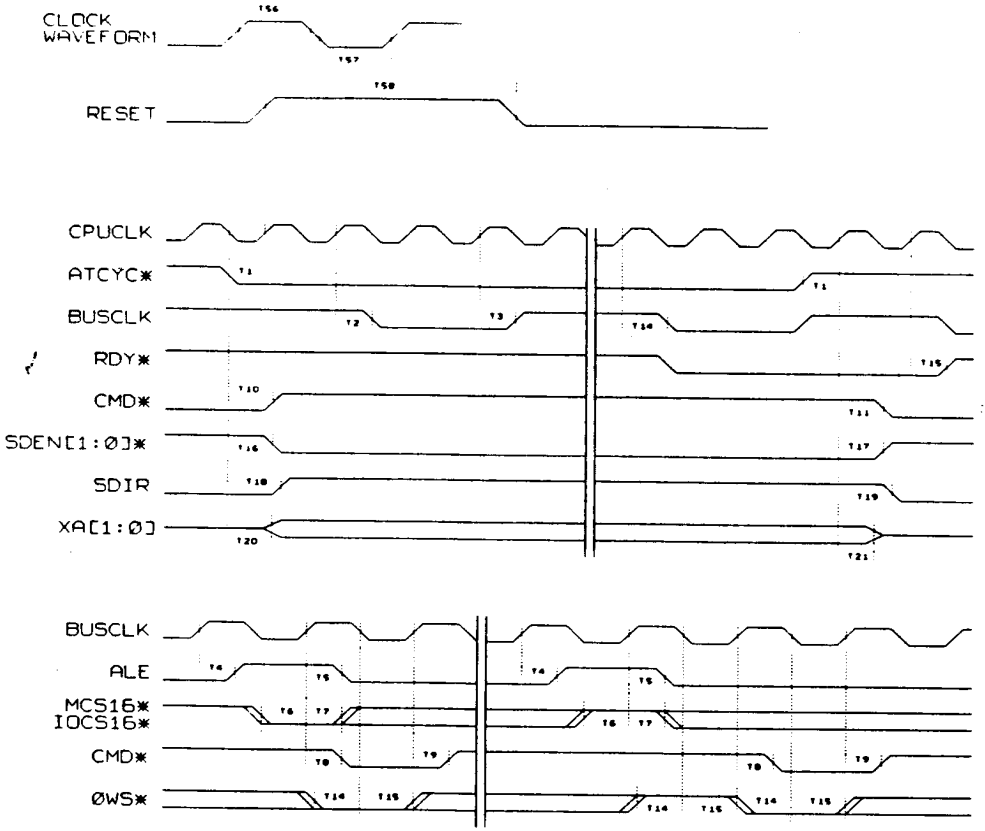
Sym	Parameter	Condition	Min.	Max.	Unit
VV					
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA*	--	0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	2.4	--	V
I_{IL}	Input Leakage	0 < V_{IN} < V_{DD}	--	±10	uA
I_{OZ}	Tri-state leakage	0.45 < V_{OUT} < V_{DD}		±20	uA

AC Characteristics: (T_A = 0°C-70°C, V_{DD} = 5V + 5%, V_{SS} = 0V)

Sym		Min.	Max.	Units
T1	-ATCYC set up time to CPUCLK	3		ns
T2	BUSCLK falling delay from CPUCLK		22	ns
T3	BUSCLK rising delay from CPUCLK		21	ns
T4	ALE active delay from BUSCLK		13	ns
T5	ALE inactive delay from BUSCLK		23	ns
T6	-MCS16, -IOCS16 set up time to ALE	40		ns
T7	-MCS16, -IOCS16 hold time to ALE	0		ns
T8	Command active delay from BUSCLK		17	ns
T9	Command inactive delay from BUSCLK		15	ns
T10	Command bus active delay from -ATCYC		27	ns
T11	Command bus float delay from CPUCLK		25	ns
T12	-READY active delay from CPUCLK		12	ns
T13	-READY inactive delay from CPUCLK		14	ns
T14	-0WS set up time to BUSCLK	39		ns
T15	-0WS hold time from BUSCLK	0		ns
T16	-SDEN active delay from -ATCYC		43	ns
T17	-SDEN inactive delay from -ATCYC		29	ns
T18	SDDIR inactive delay from -ATCYC		31	ns
T19	SDDIR inactive delay from -ATCYC		38	ns
T20	XA0,1 active delay from -ATCYC		25	ns
T21	XA0,1 inactive delay from -ATCYC		20	ns
T22	Data conversion SWAP delay from BUSCLK		30	ns
T23	Data conversion XA0 delay from BUSCLK		30	ns
T24	-OUT1 set up time to BUSCLK	27		ns
T25	-REFRESH active delay from BUSCLK		17	ns
T26	-REFRESH inactive delay from BUSCLK		16	ns

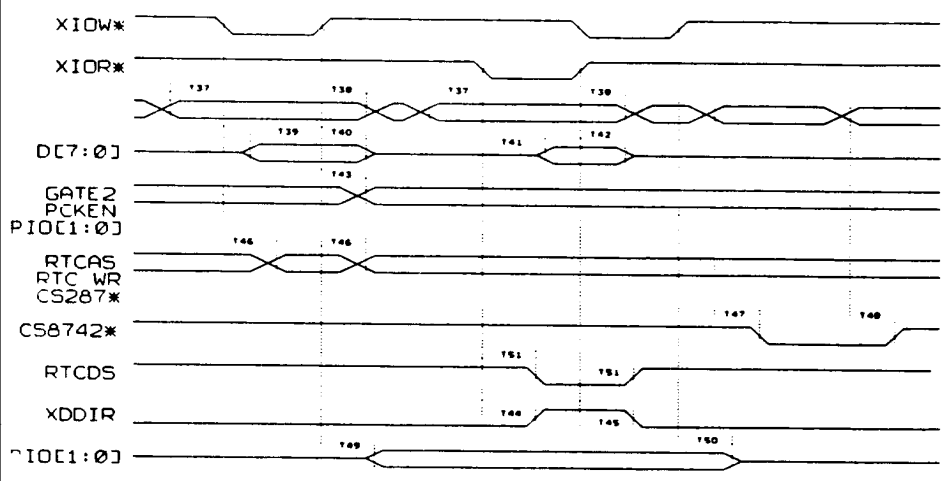
Sym		Min.	Max.	Unit
T27	Command bus active delay from -REFRESH		30	ns
T28	Command bus float delay from -REFRESH		21	ns
T29	Address bus valid delay from -REFRESH		39	ns
T30	Address bus float delay from -REFRESH		20	ns
T31	HRQ set up time to CPUCLK	5		ns
T32	-AEN1,2 set up time to CPUCLK	5		ns
T33	HOLH active delay from CPUCLK	5		ns
T34	HOLD inactive delay from CPUCLK		18	ns
T35	DMHLDA active delay from HLDA		29	ns
T36	DMAHLDA inactive delay from -AEN1,2		42	ns
T37	Address set up time to -IOR, -IOW active	14		ns
T38	Address hold time from -IOR, -IOW inactive	0		ns
T39	XD data set up time to -IOW inactive	10		ns
T40	XD data hold time from -IOW inactive	10		ns
T41	XD data valid delay from -IOR active		50	ns
T42	XD data float delay from -IOR inactive		23	ns
T43	Signal output delay from -IOW inactive		44	ns
T44	XDDIR active delay from -IOR		25	ns
T45	XDDIR inactive delay from -IOR		36	ns
T46	Write signal delay from -IOW		38	ns
T47	-CS8742 active delay from address valid		46	ns
T48	-CS8742 inactive delay from address invalid		30	ns
T49	PIO valid delay from -IOW		41	ns
T50	PIO float delay from -IOW		21	ns
T51	RTCDS delay from -IOR		37	ns
T52	Address valid delay from -AEN1, 2 active		43	ns
T53	Address delay from ADSTB active		41	ns
T54	XD data set up time to ADSTB inactive	5		ns
T55	XD data hold time to ADSTB inactive	5		ns
T56	Clock high time	5		ns
T57	Clock low time	5		ns
T58	Reset pulse width	160		ns

Timing Diagram

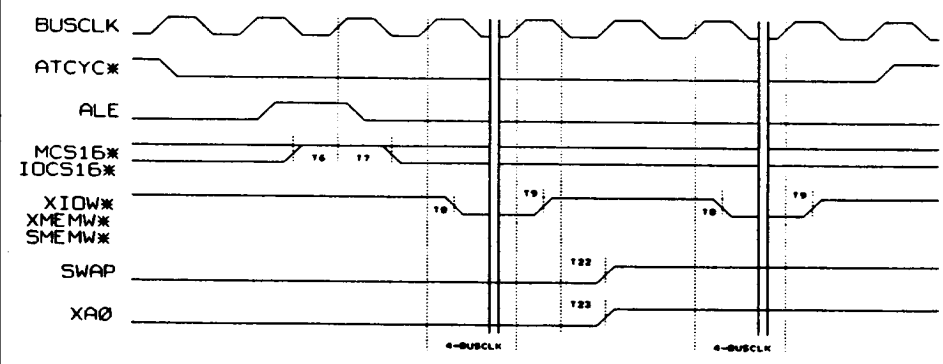


Clock Generation and Bus Command

Timing Diagram

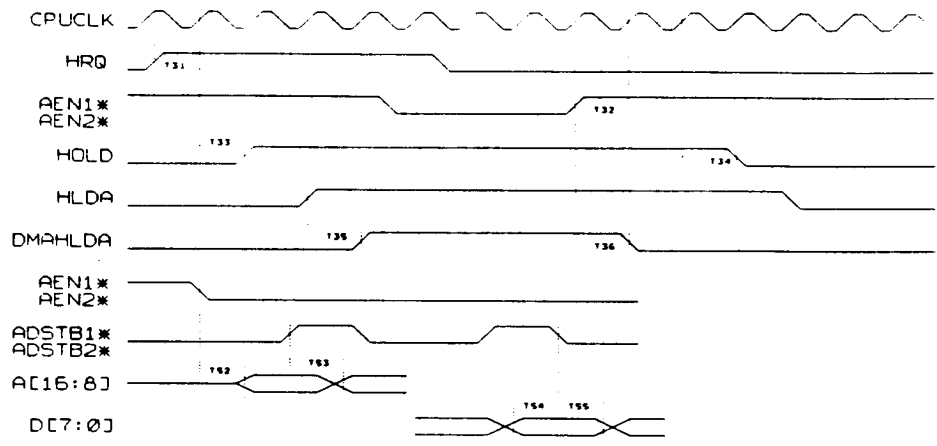


I/O Read/Write Timing

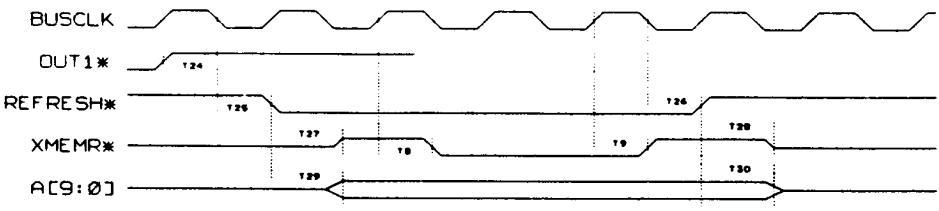


Data Conversion

Timing Diagram



Refresh and DMA Timing



Refresh Timing