SIS 85C310

Cache/Memory Controller

Rev 1.1

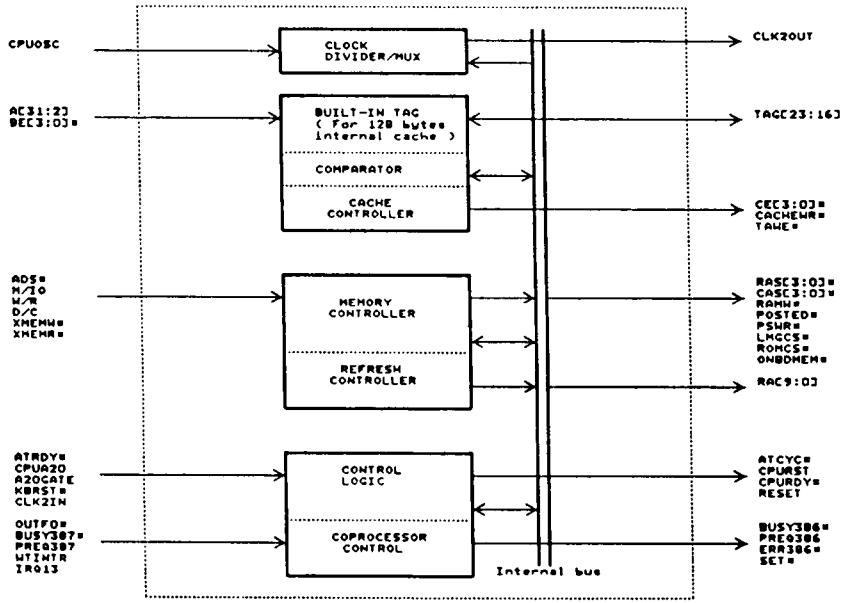
Preliminary

FEATURES

- 25/33MHz Non-Pipeline Operation
- Built-in Direct Mapped Cache Controller for 32K/64K/128K/256K Cache or More
  - 0 Wait State Read Hit
  - Programmable 0/1 Wait State Write Hit
- Built-in 128 Byte 2 Way Cache Tag Memory for Low Cost Systems
- 0 Wait State Posted Write
- Memory Controller for upto 16M of Memory
- Page Mode with Programmable Wait States: 0, 1 or 2
- Shadow BIOS and Video ROM Capability
- Transparent Refresh:
  - Independent Refresh Logic for Local Memory
  - No CPU Hold During Refresh
- Programmable CPU Speed: Divided by 1 or Divided by 2**
- Support both 80387 25/33MHz and WEITEK 25/33**MHz Coprocessor
- 100-Pin Plastic QFP

The SIS 85C310 is a high performance 32-bit memory controller for a 80386-based system. The SIS 85C310 utilizes page mode accessing up to 16M of main memory. Furthermore, it has a built-in cache controller which can handle a 2-way set associative 128 bytes cache architecture or a write through cache architecture with 32 bit line size and a cache size that is only limited by SRAM size and speed. Low cost, high performance and compact board design can be achieved because the SIS 85C310 integrates all cache management and memory control logic on one chip.

Functional Block Diagram



Functional Description

Cache Support

SIS 85C310 supports direct map external cache and 128 bytes internal cache. The line size for both cache schemes is 32-bit wide. The two schemes are mutually exclusive and only one scheme can be chosen upon setup. All cache memory must be initialized by reading memory from valid main memory with read size more than cache size.

On Chip Cache Scheme - The SIS 85C310 has built-in 2 way set associative cache controller for controlling 128 bytes of cache which is for both data and instruction. Cache tags are also built-in. This scheme associates with all 16M memory space.

Off Chip Cache Scheme - The SIS 85C310 has an 8 bit comparator built-in to support external tag RAM for direct map cache scheme. All main memory is cacheable and there is no provision for defining non-cacheable area. There are two sub-scheme:

1. 8M Cacheable Memory Space - Since only an 8-bit comparator is provided, the cache controller associates only up to 8M of memory space when the selected cache memory size is 32K. Tag address A22 to A15 are compared with CPU address A22 to A15. CPU address A23 has to be low to produce a tag comparison. Therefore memory options beyond 8M are not allowed.

2. 16M Cacheable Memory Space - When 64K or above cache option is selected, 16M of main memory are cacheable. For 64K cache, tag address A23 to A16 are compared with the CPU address A23 to A16. For 128K cache or above, since lower order tag address bits are used as cache address bits, during tag comparison, these bits should be directly from CPU instead of tag RAM to produce a match.

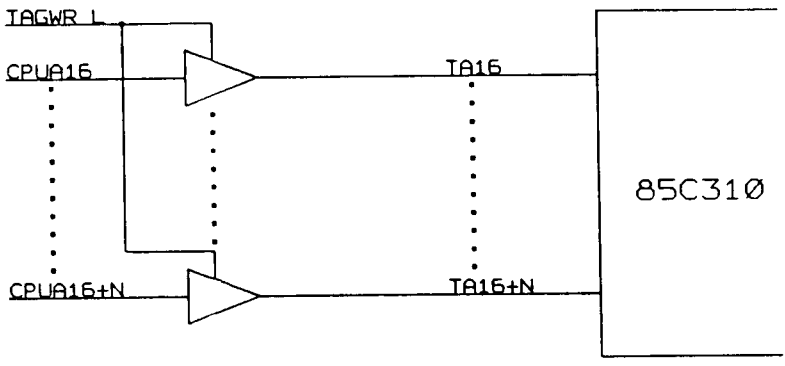
Cache Memory Access at DMA Cycle - If it is a write hit DMA cycle, Cache memory is also updated.

Memory Support

SIS 386 chip set has a built-in page mode memory controller. It can control upto 16M of memory and the built-in refresh controller generates 10 refresh addresses.
The number of wait states during page mode access can be programmed to 0, 1 or 2 wait states. A page read or write miss will take 4 wait states to complete for 0 or 1 wait state options and 5 wait states for 2 wait state option.

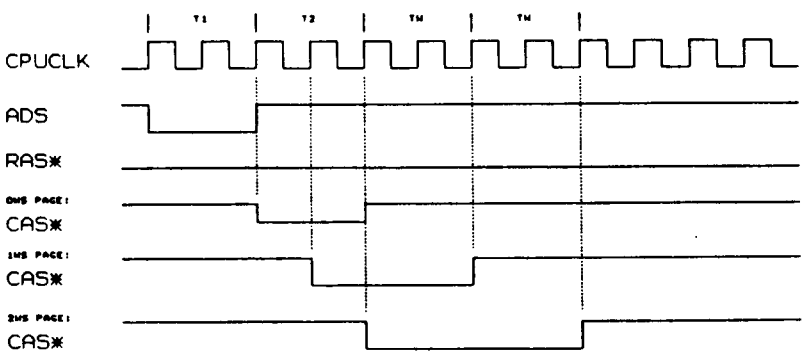
The SIS 85C310 also supports single level posted write for on board main memory. Posted write is 0 wait state if the cache write is programmed to be 0 wait state. If cache write hit is programmed to be 1 wait state, posted write will also be 1 wait state.

Support for 128K or More Cache Memory



CACHE SIZE = 128K X 2^N

Page Mode Access States



Memory Configuration - SiS/386 supports the following memory configurations:

Size	Bank 0	Bank 1	Bank 2	Bank 3
1M	256K			
2M	256K	256K		
5M**	256K	1M		
4M	1M			
8M	1M	1M		
12M	1M	1M	1M	
16M	1M	1M	1M	1M

384K Memory Relocation - The SIS 85C310 supports 384K memory relocation. The relocation is arranged as follow:

Condition	Relocation Memory Size
Shadow RAM Disable	
1M DRAM used	384K
2M DRAM used	384K
4M DRAM used	256K
> 4M DRAM used	0
Shadow RAM Enable	
64K (ROM Space)	256K
128K (ROM Space)	256K
64K + 64K (I/O Bus + ROM)	256K
128K + 128K (I/O Bus + ROM)	0

Coprocessor Support

Both 80387 and WEITEK coprocessors are supported. The presence of the 80387 is detected automatically and no setup is required. WEITEK access is only differentiated by decoding A31 and A29 of the memory space.
When external cache is selected, some of the co-processor handshaking signals need to be implemented with external logic. This is purely a pin-out limitation and these signals are not timing critical. These signals are:

ERROR to 80386
PREQ to 80386
BUSY to 80386
Co-processor Interrupt

When internal cache is selected, the above signals are handled by 85C310**. Users has the option of either using the built-in support or implementing their own.

Co-processor Ready - When an 80387 cycle is detected, 85C310 will detect the ready output from the 80387. Seeing the ready of 80387 will cause 85C310 to signal a ready to CPU. When WEITEK access is detected, the 85C310 ready output to 80386 will be tristated so that the WEITEK co-processor can drive the ready to 80386 directly.

ROM Space Support

The SIS 85C310 supports two ROM space options: 64K and 128K ROM space. The ROM address are assigned as:

1. FF0000-FFFFFF and 0F0000-0FFFFF for 64K ROM
2. FE0000-FFFFFF and 0E0000-0FFFFF for 128K ROM

The SIS 85C310 defaults to 64K ROM space. Any non shadowed ROM access are considered as an AT cycle and ATCYC* will be active.

Shadow RAM Support

The SIS 85C310 supports shadow RAM in one of the following four options:

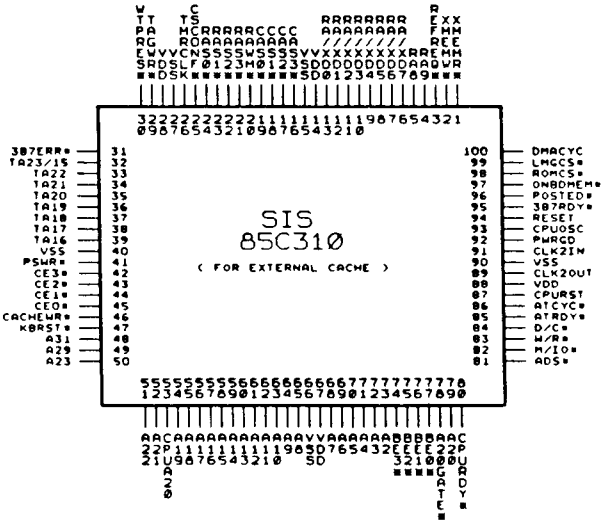
Options	BIOS	BIOS Address	Video	Video Address
1	64K	0F0000-0FFFFF	0	
2	128K	0E0000-0FFFFF	0	
3	64K	0F0000-0FFFFF	64K	0C0000-0CFFFF
4	128K	0E0000-0FFFFF	128K	0C0000-0DFFFF

All shadow memory has to be initialized by enabling write to the specified shadow area. After initialization, the shadowed area becomes read-only area. Reads to these areas are considered main memory access and therefore are cacheable. A write to this area is considered an off board memory cycle (AT cycle) and ATCYC* will be active.

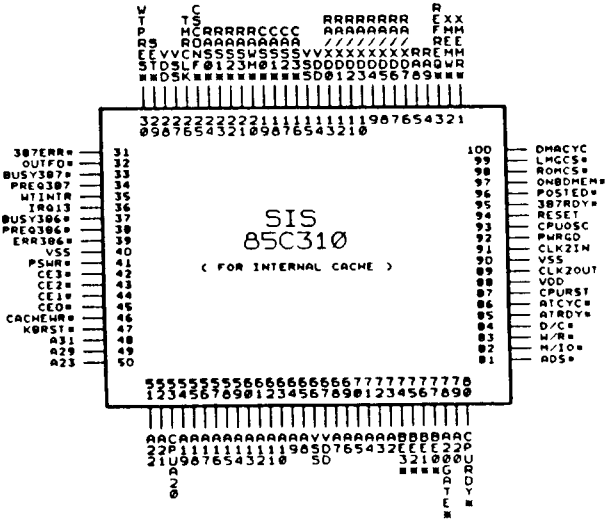
AT Cycle

The SIS 85C310 detects whether an AT cycle is being executed. The AT cycle is defined as off board memory cycles, all I/O cycles and interrupt acknowledge cycle. Besides, no ATCYC# will be active.
Halt and shutdown cycles are not considered as AT cycles and the 85C310 will terminate these cycles with 0 wait state.

Pin Assignment



A. For External Cache



B. For Internal Cache (128Bytes)

Pin Description

Pin No.	Type	Symbol	Description
48-49	I	A31,A29	ADDRESS: These address inputs are used to distinguish between memory cycles and coprecessor cycles. During DMA cycles, these signals are forced to 0 internally.
50-52	I	A23-A21	ADDRESS: These address inputs are used for memory decoding during CPU cycles and DMA cycles.
79	I/O	A20	ADDRESS: During CPU cycles, this is a gated output of CPU address A20. It can be forced to 0 either by GATEA20 low or by a programmable control bit. During DMA, it becomes an input for decoding. The above mentioned control is inactive during DMA cycles.
53	I	CPUA20	ADDRESS: CPU A20 input for decoding during CPU cycles and DMA cycles.
54-65 68-73	I	A19-A2	ADDRESS: These address inputs are used for decoding during CPU cycles and DMA cycles.
74-77	I	BE3#-BE0#	BYTE ENABLE: These active low signals determine the bytes to be accessed during CPU cycles or DMA cycles.
81	I	ADS#	ADRESS STATUS: This active low input indicates a valid CPU cycle definition. During DMA cycles, this input should be held high.
82	I	M/IO#	MEMORY I/O DEFINITION: A high level input indicates a memory cycle and a low level indicates an I/O cycle.
83	I	W/R#	WRITE/READ DEFINITION: A high level input indicates a write cycle and a low level indicates a read cycle. During DMA cycles, this signal should be held high.
84	I	D/C#	DATA/CODE DEFINITION: A high level input indicates a data cycle and low level indicates a code cycle. It is used to determine a halt or shutdown cycle.
95	I	387RDY#	387 READY: This active low input indicates the current 387 cycle is ready. It should be connected to the READY0 output of 80387.
31	I	387ERR#	387 ERROR: This active low input is used to determine if there is an error at the 387 cycle and to determine the presence of 80387 during CPU reset.
30	I	WTPRES#	WEITEK PRESENT: When low, this input indicates the presence of the WEITEK coprocessor.
85	I	ATRDY#	IO BUS READY: This active low input indicates the current bus cycle is ready. It will cause a CPU ready to be generated.
25	I	CSCONF#	CONFIGURATION REGISTER ACCESS: This active low signal controls the access to the internal configuration registers of the 85C310. It is qualified with WR internally to determine whether it is a read or a write access. Data is transferred through RA/XD7-0.
92	I	PWRGD	POWER GOOD: Only until this signal becomes high will the 85C310 accepts valid inputs. This is a Schmitt triggered input.
47	I	KBRST#	CPU RESET CONTROL: A low level at this input will cause the CPU to be reset.
26	I	TMRCLK	TIMER CLOCK: 1.19MHz timer clock used for RAS timeout
100	I	DMACYC	DMA CYCLE: A high level at this input indicates an active DMA cycle.
3	I	REFREQ#	REFRESH REQUEST: A low level input here will cause the 85C310 to generate a refresh cycle to the local DRAM. If DMACYC is active, it will be interpreted as a master refresh cycle that is synchronized with XMEMR input.
1	I	XMEMR#	BUS MASTER MEMORY READ: This input is only accepted during DMA cycle.

Pin Description (continued)

Pin No.	Type	Symbol	Description
2	I	XMEMW#	BUS MASTER MEMORY WRITE: This input is only accepted during DMA cycle.
78	I	A20GATE#	A20 GATE: This is an active low input that forces A20 low during CPU cycle.
4-5	I	RA9-RA8	DRAM ADDRESS: Multiplexed DRAM address outputs.
6-13	I/O	RA/XD7-RA/XD0	MULTIPLEXED DRAM ADDRESS/CONFIGURATION DATA: Multiplexed DRAM address outputs during memory cycles. During access to configuration registers, these are bidirectional data bus.
20	O	RAMW#	RAM WRITE ENABLE: Active low DRAM write enable output.
21-24	O	RAS3#-RAS0#	RAS ENABLE: These are decoded row address enable. An active low output indicates the corresponding bank of memory is accessed. During refresh, all the RAS ENABLE outputs are driven low.
16-19	O	CAS3#-CAS0#	CAS ENABLE: These are column address enables. An active low output indicates the corresponding byte is accessed.
For External Cache Mode			
32	I/O	TA23,TA15	TAG ADDRESS: Bidirectional TAG data. If 32K cache: A15 If 64K or more cache: A23
33-39	I/O	TA22-TA16	TAG ADDRESS: Bidirectional TAG data that correspond to A22-A16
29	O	TAGWR#	TAG WRITE: Active low TAG write enable output.
For Internal Cache Mode			
32	I	OUTF0#	IOW TO F0H: An low input causes the latched IRQ13 to be cleared. It should be a decoded IOW at address F0H if the application is for AT compatibles.
33	I	BUSY387#	387 BUSY: Active low input from 80387 busy signal
34	I	PREQ387	387 REQUEST: Active high input from 80387 request signal.
35	I	WTINTR	WEITEK INTERRUPT: Active high input from WEITEK interrupt output.
36	O	IRQ13	IRQ13: Latched active high interrupt request caused by WTINTR or 80387.
37	O	BUSY386#	386 BUSY: Active low output caused by BUSY387 input. It should be connected to 386 BUSY input.
38	O	PREQ386	386 REQUEST: Active high output caused by PREQ387. It should be connected to 80386 PREQ input.
39	O	ERR386#	386 ERROR: Active low output caused by 387ERR. This signal is only active during CPU reset and is inactive once reset goes away. It should be connected to 80386 ERROR input.
29	O	SET#	CACHE BANK SELECT: This signal determines which bank of cache RAM is selected in a two-way cache mapping.
46	O	CACHEWR#	CACHE WRITE ENABLE: Active low output indicating a write to cache memory.
42-45	O	CE3#-CE0#	CACHE BYTE ENABLE: Active low output indicating the corresponding byte is accessed.
80	O	CPURDY#	CPU READY: Active low output indicating the current CPU cycle can be terminated. This signal is tri-stated during WEITEK cycle to allow WEITEK ready to drive the 80386 directly.
87	O	CPURST	CPU RESET: Active high output to reset both 80386 and 80387.
96	O	POSTED#	POSTED CYCLE: This is a synchronized output indicating a post cycle, either posted write or refresh, is on going.

Pin Description (continued)

Pin No.	Type	Symbol	Description
41	O	PSWR#	POSTED WRITE: This is a synchronized output indicating a post write is on going. It is used to latch data for the posted write cycle.
86	O	ATCYC#	IO BUS CYCLE: This is a synchronized output indicating a cycle that is neither a local memory nor a cache cycle.
97	O	ONBDMEM#	LOCAL MEMORY DECODE: This is an address decode output indicating local memory is selected.
98	O	ROMCS#	ROM DECODE: This is an address decode output indicating BIOS space is selected.
99	O	LMGCS#	1 MEG SELECT: This is an address decode output indicaing the first 1 megabyte address is selected.
94	O	RESET	RESET: Active high output indicating system reset.
93	I	CPUOSC	OSCILATOR INPUT: Oscillator input which will be used as the fundamental clock.
91	I	CLK2IN	CPU CLOCK INPUT: CPU clock input which is used by all internal logic.
89	O	CLK2OUT	CPU CLOCK OUTPUT: CPU clock output which is derived from CPUOSC. This is the clock the CPU should use.
14,28 67,88		VDD	+5V
15,27,40 66,90		VSS	Ground

Registers Configuration Specifications for 85C310

There are two configuration registers and two control modes. All configuration register can be written to and read from.

SIS 85C310 refresh disable control:

Refresh controls on the 85C310 is default to enable. Three consecutive read from port 822H can toggle the refresh control bit inside the 85C310.

Before any access to the configuration registers are made, refresh should be shut off by three consecutive read from port 822H. When done, another three consecutive read will reenable the refresh.

Speed Control:**

CPU clock is default to 1/1 of the input oscillator clock. Four consecutive read to the internal configurations registers, i.e., four consecutive I/O read with active CSCONF* will toggle the 1/2 option control bit inside the 85C310.

This bit determines whether the CPU clock is divide by 1 or divide by 2 output of the input oscillator clock. The clock switching is glitch free.

Feature Control Registers:

The configuration registers are accessed through 85C320. First writing the index 083H into Port 022H and then followed by two continously reads or writes to Port 023H. These reads or writes will issue CSCONF# to access the configuration registers in 85C310. All access to the configuration registers should be contiguous; an access to register 00 has to be followed immediately by an access to register 01.
All control registers are reset to 0 at power up.

Register 00:

Bit 0
shadow C000 segment enable:

0 = disable
1 = enable

Bit 1
Shadow RAM Write Enable:

0 = disable
1 = enable

This control bit should be set to 1 when EPROM data is to be transferred to the shadow RAM area that resides in the BIOS space. After data transferred and Shadow RAM Read enabled, this bit should be set to 0 to prevent BIOS data be modified.

Bit 2
Modified Cache Write:

0 = Cache Write Enable Starts at Middle of T2
1 = Cache Write Enable Starts at Start of T2

Bit 3
ROM Size:

For Version 1.0 Silicon:
0 = 128K ROM Space, 64K shadow RAM space at F000:0
1 = 64K ROM Space, 128K shadow RAM space at E000:0

For Version 2.0 Silicon:
0 = 64K ROM Space, 64K shadow RAM space at F000:0
1 = 128K ROM Space, 128K shadow RAM space at E000:0

When combined with shadow C000 segment control bit, the following shadow options are available.

For Version 1.0 Silicon:

Bit 0	Bit 3	Shadow RAM	ROMCS#(Pin 98)
0	0	64K at 0F0000-0FFFFF	128K at 0E0000-0FFFFF
0	1	128K at 0E0000-0FFFFF	64K at 0F0000-0FFFFF
1	0	64K at 0F0000-0FFFFF 64K at 0C0000-0CFFFF	128K at 0E0000-0FFFFF
1	1	128K at E0000-0FFFFF 128K at 0C0000-0DFFFF	64K at F0000-0FFFFF

For Version 2.0 Silicon:

Bit 0	Bit 3	Shadow RAM	ROMCS#(Pin 98)
0	0	64K at 0F0000-0FFFFF	64K at 0F0000-0FFFFF
0	1	128K at 0E0000-0FFFFF	128K at 0E0000-0FFFFF
1	0	64K at 0F0000-0FFFFF 64K at 0C0000-0CFFFF	64K at 0F0000-0FFFFF
1	1	128K at E0000-0FFFFF 128K at 0C0000-0DFFFF	128K at E0000-0FFFFF

Bit 4

Cache Write Wait States:

0 = 1 Wait State
1 = 0 Wait State

The cache write is default to 1 wait state. This requires the main memory to operate at least 1 wait state. This option is intended for very high speed application while the SRAM can be of a slower type. If programmed, the cache can operate at 0 wait state write.

Bit 5, 6

Cache Size:

Bit 6	Bit 5	Cache Size
0	0	= No Cache Selected
0	1	= 32K Cache
1	0	= 64K or Bigger Cache Size
1	1	= 128 Byte Internal Cache

The SIS 85C310 has built-in comparator which is optimized to support different sizes of cache memory. In addition, it has built-in tag to support upto 128 Bytes of 2-way set associative cache. This is used in conjunction with the SIS 85C330 which has the 128 Bytes cache memory built-in. This option is for low cost system application.

Bit 7

Cache Enable:

0 = Cache Enable
1 = Cache Enable

The cache memory is default to disable.

• **Register 01:**

Bit 0-2

Memory Size:

Bit 2	Bit 1	Bit 0	
0	0	0 =	1M
0	0	1 =	2M
0	1	0 =	5M**
0	1	1 =	Reserved
1	0	0 =	4M
1	0	1 =	8M
1	1	0 =	12M
1	1	1 =	16M

Bit 3

Reserved

Bit 4, 5

DRAM CAS Wait States:

Bit 5	Bit 4	
0	0 =	2 Wait States
0	1 =	1 Wait State
1	0 =	0 Wait State
1	1 =	Illegal

Bit 6

Shadow RAM Read Enable:

0 = Disable
1 = Enable

Bit 7

Page Mode Enable:

0 = Page Mode Disable
1 = Page Mode Enable

Only after BIOS data has been transferred to RAM, this bit should be set to 1 to enabled fast BIOS-reading from shadow RAM.

- Applications Notes

IMPORTANT:

Only CLK2IN is used for all internal state machines. CPUOSC only goes into a clock divider whose output goes directly to CLK2OUT. Therefore CPUOSC and CLK2OUT can be replaced using external logic and clock driver. CLK2IN should be in-phase with CPU clock and should never be skewed ahead of CPU clock.

Electrical Characteristics

Absolutely Maximun Ratings:

Parameter	Min	Max	Unit
Ambient Operating Temperature	0	70	°C
Storage Temperature	-55	125	°C
Input Voltage	-0.5	5.5	V
Output Voltage	-0.5	5.5	V

Note: Stress above these listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

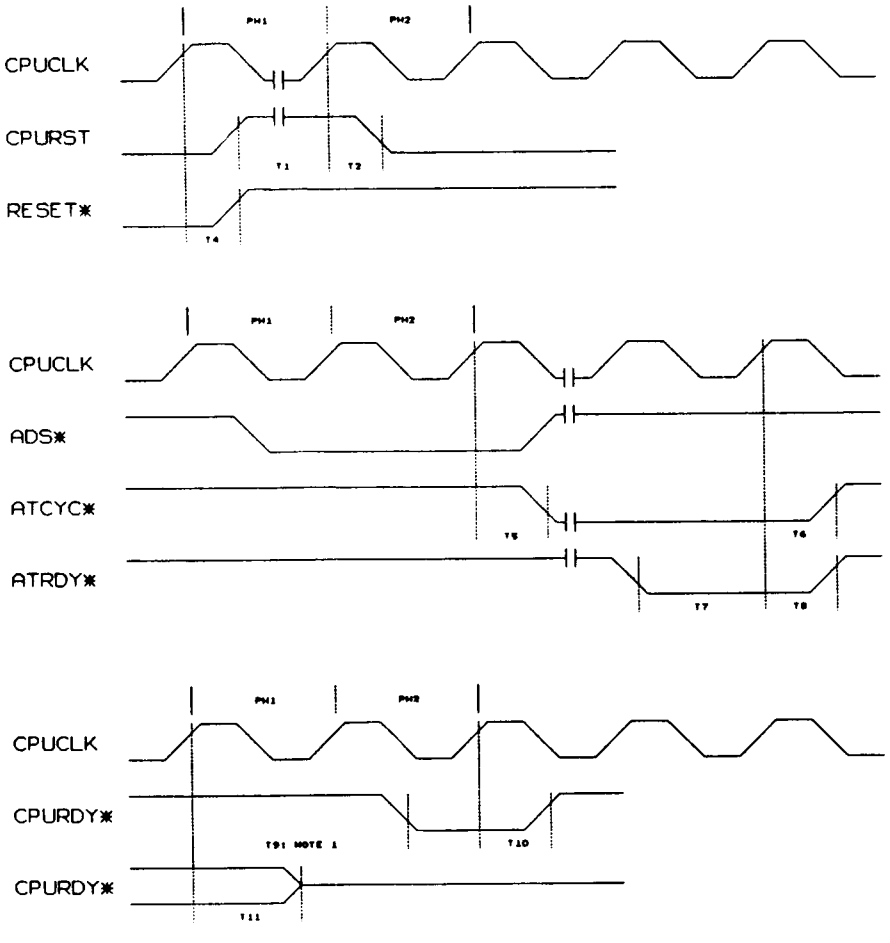
DC Characteristics: (TA = 0°C-70°C, VDD = 5V±5%, VSS = 0V)

Sym	Parameter	Condition	Min	Max	Unit
VIL	Input Low Voltage		-0.5	0.8	V
VIH	Input High Voltage		2.0	VDD + 0.5	V
VOL	Output Low Voltage	IOL = 4mA	--	0.45	V
VOH	OutputHigh Voltage	IOH = -1mA	2.4	--	V
IIL	Input Leakage	0 < VIN < VDD	--	±10	uA
IOZ	Tri-State Leakage	0.45 < VOUT < VDD	--	±20	uA
VILR	RESET Schmitt VIL		--	0.8	V
VILH	RESET Schmitt VIH		3.5	--	V

AC Characteristics: (TA = 0°C-70°C, VDD = 5Væ5%, VSS = 0V)

Sym		Min	Max	Unit
T1	CPURST duration	64		CLK2
T2	CPURST active delay from CPUCLK	4	10	ns
T4	RESET active delay from CPUCLK	6	20	ns
T5	-ATCYC active delay from CPUCLK	4	12	ns
T6	-ATCYC inactive delay	4	13	ns
T7	-ATRDY setup time	17		ns
T8	-ATRDY hold time	0		ns
T9	-CPURDY active delay ** Note 1 on P 1-16		51	ns
T10	-CPURDY inactive delay		30	ns
T11	-CPURDY float delay	7	30	ns
T12	read cycle -CE active delay	4	13	ns
T13	read cycle -CE inactive delay	4	16	ns
T14	write cycle -CE active delay	4	15	ns
T15	write cycle -CE inactive delay	4	17	ns
T16	-CACHEWR active delay	4	13	ns
T17	-CACHEWR inactive delay	4	16	ns
T18	read miss cycle -CACHEWR inactive delay	10	25	ns
T19	-TAGWR active delay	4	12	ns
T20	-TAGWR inactive delay	4	15	ns
T21	tag address set up time	23		ns
T22	memory address set up time	15		ns
T23	address decode valid delay		25	ns
T24	-PSWR active delay	4	17	ns
T25	-PSWR inactive delay	4	19	ns
T26	-POSTED active delay	4	17	ns
T27	-POSTED inactive delay	4	19	ns
T28	-RAS inactive delay	4	17	ns
T29	-RAS active delay	4	19	ns
T30	-RAS precharge time	5		CLK2
T31	column address valid delay	6	17	ns
T32	-CAS active delay	4	20	ns
T33	-CAS inactive delay	4	25	ns
T34	write cycle -CSCONF inactive setup time	15		ns
T35	read cycle -CSCONF inactive setup time	0		ns

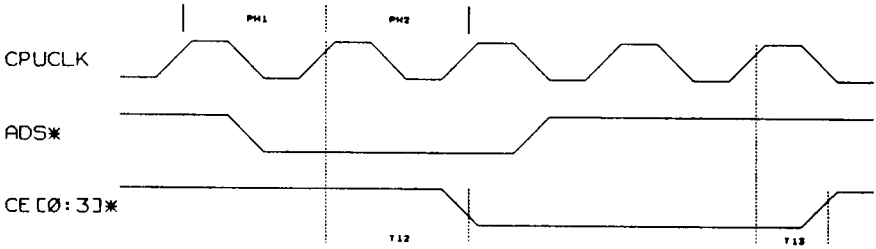
Timing Diagram



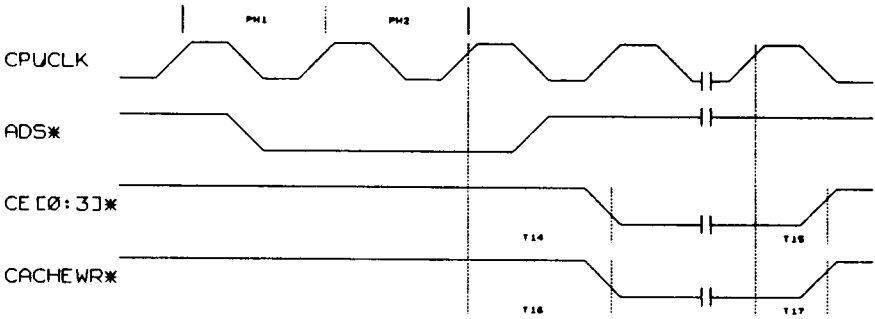
NOTE 1: THIS IS MEASURED AT 33MHZ, USING 20NS TAG SRAM.

Timing Diagram

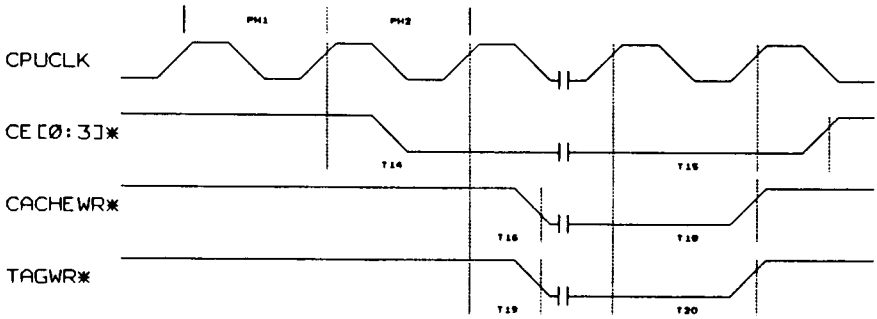
CACHE READ HIT:



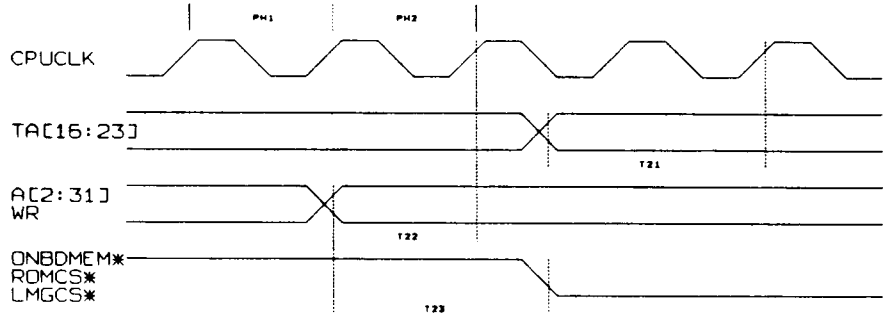
CACHE WRITE HIT:

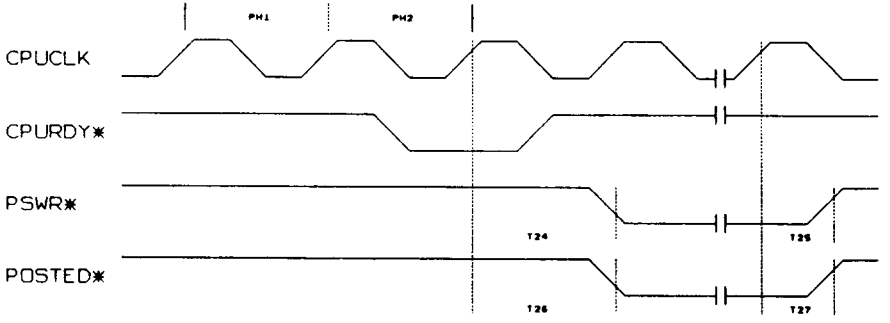


CACHE READ MISS:

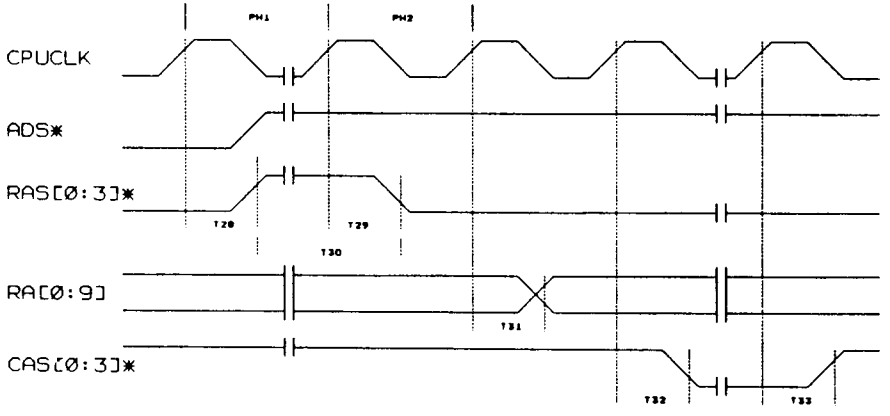


Timing Diagram





PAGE MISS:



Timing Diagram