1. Overview

SiS5596 PCI, Memory & VGA Controller

SiS5513 PCI System I/O

The SiS5596/5513 with built-in VGA controller is a two-chip solution for Pentium PCI/ISA system. A portion of on board DRAM is shared with the built-in VGA controller. In that way, the system cost is substantially reduced.

The SiS5596/5513 two chips solution for shared memory architecture is achieved by allowing both GUI / VGA, and System DRAM controller to control system memory. For the shared memory application, the chipset always acts as the arbiter of memory bus masters. Whenever the GUI wants to access the memory bus, it requests the memory bus from the chipset first. The chipset grants the memory bus to the GUI, only if the memory bus is not needed by the chipset. The chipset also supports the two priority scheme. Other important key features such as direct access frame buffer and memory access latency are also supported. The system block diagram is shown in Figure 1.1.

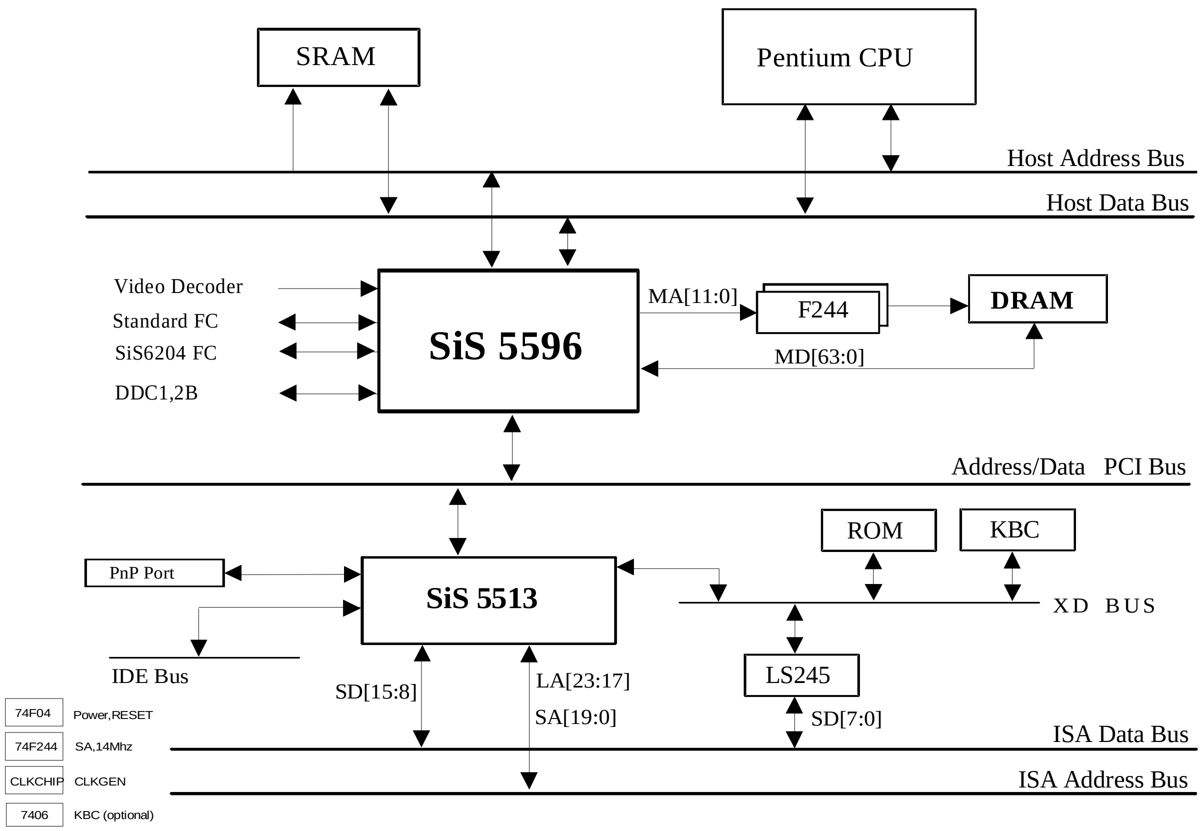


Figure 1.1 System Block Diagram

1.1 General Features

- **Supports Intel Pentium CPU and other compatible CPU at 66/60/50MHz (external clock speed)**
- **Supports VGA Shared Memory Architecture**
  - Direct Memory Accesses
  - Shared Memory Area 0.5M, 1M, 1.5M, 2M, 2.5M, 3M, 3.5M, 4M.
  - Built-in 2-Priority Scheme.
- **Supports the Pipelined Address Mode of Pentium CPU.**
- **Integrated Second Level (L2) Cache Controller**
  - Write Through and Write Back Cache Modes
  - 8 bits or 7 bits Tag with Direct Mapped Cache Organization
  - Supports Pipelined Burst SRAM.
  - Supports 256 KBytes to 1 MBytes Cache Sizes.
  - Cache Read/Write Cycle of 3-1-1-1 Pipelined Burst SRAM at 66 Mhz and 3-1-1-1-1-1-1-1 at back to back read cycle.
- **Integrated DRAM Controller**
  - Supports 4 RAS lines, the memory size is from 4MBytes up to 512Mbytes.
  - Supports 256K/512K/1M/2M/4M/16M x N 70ns FP/EDO DRAM
  - Supports 4K Refresh DRAM
  - Supports 3V or 5V DRAM.
  - Supports Symmetrical and Asymmetrical DRAM.
  - Supports 32 bits/64 bits mixed mode configuration
  - Supports Concurrent Write Back
  - Table-free DRAM Configuration, Auto-detect DRAM size, Bank Density, Single /Double sided DRAM, EDO/ FP DRAM for each bank
  - Supports CAS before RAS "Intelligent Refresh"
  - Supports Relocation of System Management Memory
  - Programmable CAS# Driving Current
  - Fully Configurable for the Characteristic of Shadow RAM (640 KByte to 1 Mbyte)
- **Supports EDO/FP 5/6-2-2-2/-3-3-3 Burst Read Cycles**
- **Two Programmable Non-Cacheable Regions**
- **Option to Disable Local Memory in Non-Cacheable Regions**
- **Shadow RAM in Increments of 16 KBytes**
- **Supports SMM Mode of CPU.**

- **Supports CPU Stop Clock.**
- **Supports Break Switch.**
- **Provides High Performance PCI Arbiter.**
  - Supports 4 PCI Master.
  - Supports Rotating Priority Mechanism.
  - Hidden Arbitration Scheme Minimizes Arbitration Overhead.
  - Supports Concurrency between CPU to Memory and PCI to PCI.
- **Integrated PCI Bridge**
  - Supports Asynchronous PCI Clock.
  - Translates the CPU Cycles into the PCI Bus Cycles
  - Provides CPU-to-PCI Read Assembly and Write Disassembly Mechanism
  - Translates Sequential CPU-to-PCI Memory Write Cycles into PCI Burst Cycles.
  - Zero Wait State Burst Cycles.
  - Supports Advance Snooping for PCI Master Bursting.
  - Maximum PCI Burst Transfer from 256 Bytes to 4 KBytes.
- **388-Pin BGA Package.**
- **0.5µm CMOS Technology.**

1.2 Features for Integrated VGA Controller

1.2.1 PCI Bus Interface

- **PCI 2.1 Compliance**
  - Support subsystem vender ID and subsystem ID, two write-once registers, in PCI configuration space
- **Built-in memory mapped I/O base registers in configuration space**
- **Supports 32-bit PCI local bus standard Revision 2.1**
- **Supports PCI burst write**
- **Supports PCI multimedia design guide Rev. 1.0**

1.2.2 Performance

- **Supports Turbo Queue (Software Command Queue in off-screen memory) architecture to achieve extra-high performance (SiS patent pending)**
- **Built-in an enhanced 64-bit BITBLT graphics engine with the following functions:**
  - 256 raster operation functions

- Rectangle fill
- Color/Font expansion
- Line-drawing with styled pattern
- Built-in 8x8 pattern registers
- Built-in 8x8 mask registers
- 32 doublewords hardware Command Queue

- **Built-in 64x64x2 bit-mapped hardware cursor**
- **Built-in 6 stages CPU write-buffer and 128 bits read-ahead cache to minimize CPU wait-state**
- **Built-in 2 stages engine write-buffer and 320 bits read-buffer to minimize engine wait-state**
- **Built-in 64x32 CRT FIFOs to support super high resolution graphic modes and reduce CPU wait-state**
- **Memory-mapped I/O to reduce I/O trapping overhead under protected mode**
- **Supports linear addressing mode up to 4MByte to speed up graphics performance**
- **Built-in two line-buffers (90x64) with bilinear interpolation logic to improve video quality and video playback frame rate.**
- **Support Direct Draw**

-Built-in transparent Blt logic with source/destination color key.
-Built-in 4-bit blending logic for video overlay.
-Built-in 2-bit blending logic for Blt logic.
-Built-in color key and chroma key for video overlay.
-Support logic to read back current scan line of refresh.
-Support fast page flipping function.

1.2.3 Integration

- **Built-in programmable 24-bit true-color RAMDAC with reference-voltage generator**
- **Built-in dual-clock generator**
- **Built-in monitor-sense circuit**
- **Built-in graphics accelerator and VGA controller**
- **Built-in video accelerator**
- **Built-in Phillips SAA7110/SAA7111, Brooktree Bt815/817/819A, SONY CXA1790q video decoder interface**
- **Built-in PCI multimedia interface**
- **Built-in Standard feature connector logic support**

1.2.4 Resolution, Color & Frame Rate

- **Supports 135 MHz pixel clock**
- **Supports super high resolution graphic modes**
  - 640x480 256/32K/64K/16M colors NI
  - 800x600 16/256/32K/64K/16M colors NI
  - 1024x768 16/256/32K/64K/16M colors NI
  - 1280x1024 16/256 colors NI, 32K/64K colors interlace only
- **Supports virtual screen up to 2048x2048**
- **Supports 80/132 columns text mode in 25, 30, 44 or 60 rows and other modes**
- **Supports 75Hz vertical refresh rate**

1.2.5 Video Functions

- **Supports full motion picture required only 1 Megabyte DRAM and up to 1024x768x256 mode**
- **Uses SiS defined 8-bit feature connector direct connecting to SiS 6204 for video overlay**
- **Supports single frame buffer architecture to save the DRAM cost**
- **Supports graphics/video overlay function by color-key and chroma-key operations**
- **Supports multi-format Video For Windows such as YUV422, RGB565, and RGB555**
- **Supports YUV-to-RGB color space conversion**
- **Supports video scaling in integer increments of 1/64**
- **Support horizontal 2-tap, 8-tap DDA interpolation**
- **Support vertical 2-tap, 8-tap DDA interpolation for better quality of video windows expansion**
- **Built-in 64x16 video capture FIFOs to support video capture**
- **Built-in 64x32 video playback FIFOs to support video playback**
- **Supports Microsoft Video For Windows**
- **Real-Magic MPEG API compatible for interactive title**
- **Supports DCI Drivers and Direct Draw Drivers**
- **Built-in brightness adjustment and contrast enhancement logic to support high quality video playback**
- **Support video overlay for any graphic modes.**
- **Built-in genlock circuit for video capture.**

1.2.6 Power Management

- **Dynamic power management to reduce internal SRAM, DAC and line-buffer power consumption.**
- **Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management**
- **Supports direct I/O command to force graphics controller into standby/suspend/off state**
- **Power down internal SRAM in direct color mode**

1.2.7 Multimedia Application

- **Supports DDC1 and DDC2B specifications**
- **Follows the plug & play specification for display controller**
- **Supports RAMDAC snoop for multimedia applications**

1.2.8 Misc.

- **Support Signature Analysis for automatic test**
- **Support 32/64 bit display memory path**

1.3 Functional Block Diagram

1.3.1 System Block Diagram

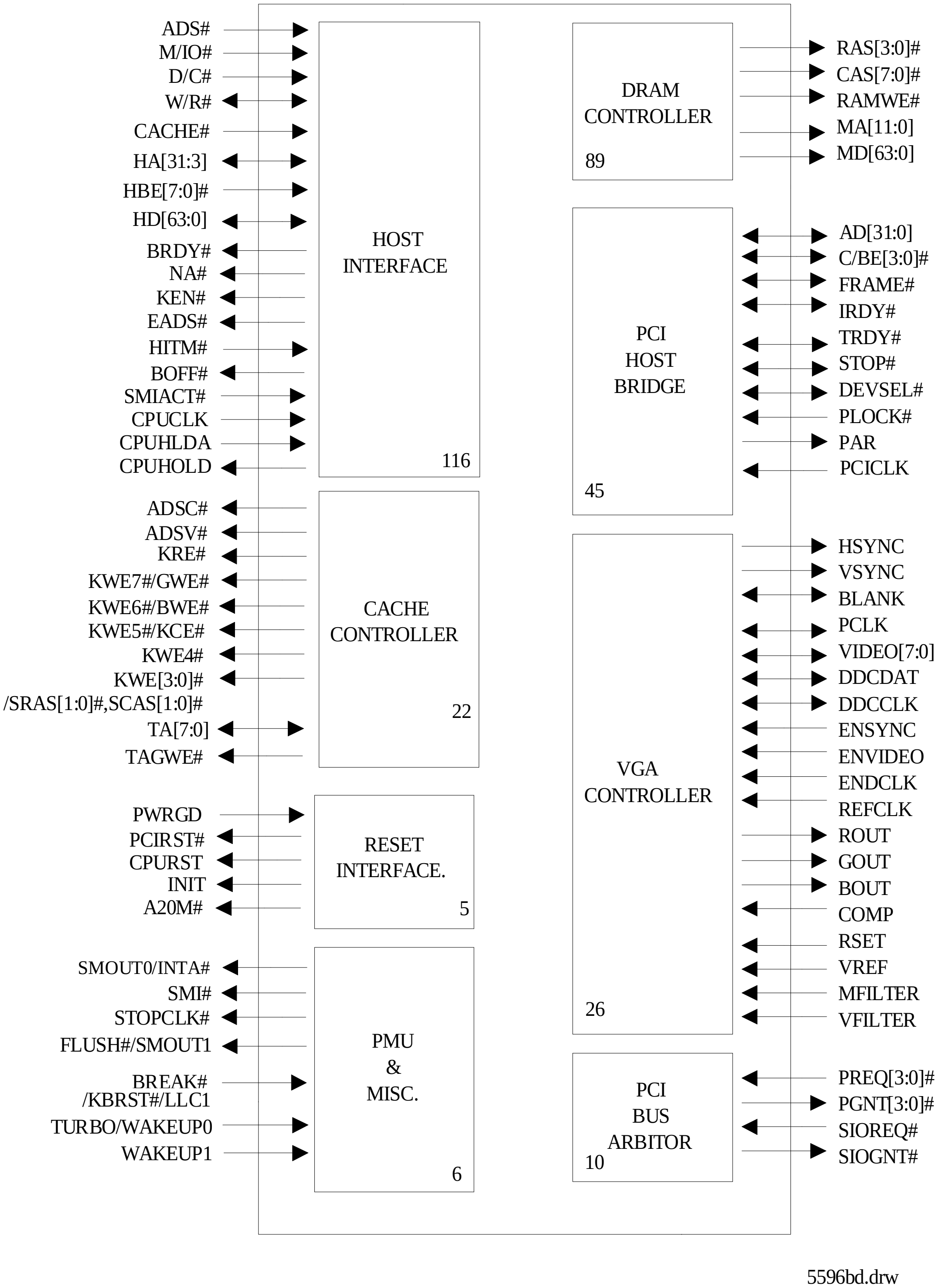


Figure 1.2

1.3.2 Integrated VGA Controller Block Diagram

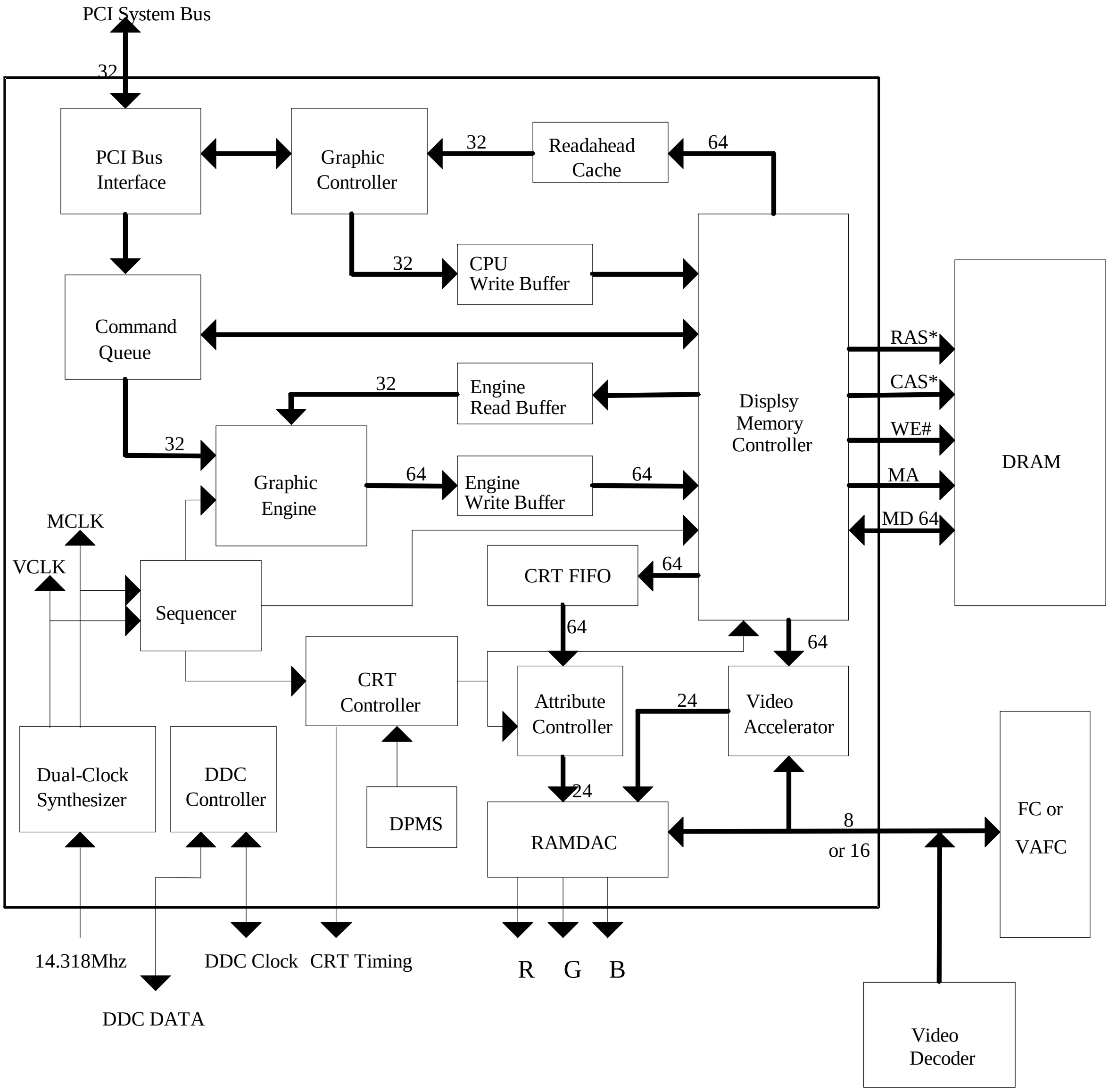


Figure 1.3

1.3.3 Integrated VGA Controller Video Accelerator Block Diagram

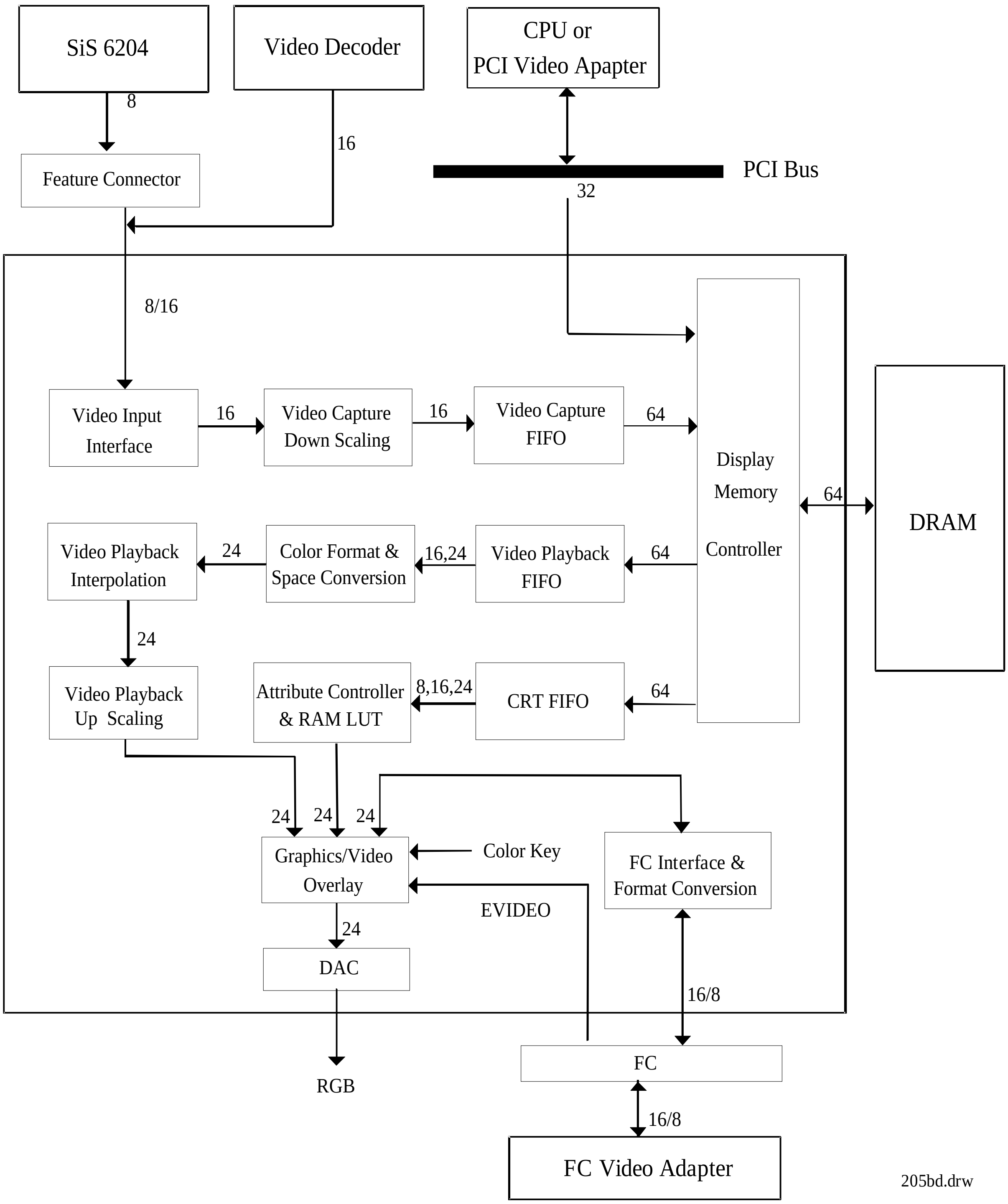


Figure 1.4

2. Functional Description

The SiS5596 integrates the VGA controller, memory controller, PCI bridge, and power management unit into a 388 pin chip that uses the advanced BGA packaging. The memory controller in SiS5596 can support Fast Page and EDO DRAMs and for Level 2 cache it can support Pipelined Burst SRAMs. There are a one line deep posted write buffer in memory controller which can reduce latency between CPU & DRAM.

2.1 CPU Interface

The SiS5596 is designed to support Pentium CPU host interface at 66.667/60/50MHz. The host data bus and the DRAM bus are 64-bit wide.

The SiS5596 supports the pipelined addressing mode of the Pentium CPU by issuing the next address signal, NA#. NA# is only generated in the following cases:

(a) Burst read L2 cache or DRAM, (b) Single read DRAM.

The SiS5596 supports the CPU L1 write back (WB) or write through (WT) cache policies and the 5596 L2 WB or WT cache policies. The L1 cache is snooped by the assertion of EADS# when the CPU is put in the HOLD state.

The SiS5596 issues CPUHOLD to the Pentium CPU in response to the assertion of PCI master requests(REQ[3:0]#, and PHOLD#). Upon receiving the CPUHLDA from the CPU, it does not immediately assert GNT[3:0]# or PHLDA# until both the CPU to PCI posted write buffer and the memory write buffer are empty. During inquire cycles, the CPUHOLD may be negated temporarily to allow the CPU to write back the inquired hit modified line to L2 or DRAM.

2.2 Cache Controller

The built-in L2 Cache Controller uses a direct-mapped scheme, which can be configured as either in the write through or write back mode. Pipelined burst SRAMs are supported.

SiS5596 supports SRAM types auto-detection and auto-sizing. Table 2-1 shows the cache sizes that are supported by the SiS5596 when using synchronous SRAM, with the corresponding TAG RAM sizes, data RAM sizes, and cacheable memory sizes. Tables 2-2 summarize the recommended speed setting when the pipelined Burst SRAMs are used.

Table 2-1 Cache Size with 8-bit tag

Cache Size	Data RAM	Tag RAM	Cacheable Size
256K	32Kx32x2	8Kx8	64M
512K	32Kx32x4	16Kx8	128M
1M	32Kx32x8	32Kx8	256M

The SiS5596 also provides an alternative to save the dirty SRAM chip. This is accomplished by sharing the alter bit with tag address bits in the same 8-bit wide TAG RAM. System uses this implementation supports 7 tag address bits and 1 dirty bit. By doing so, the cacheable local memory sizes are reduced to half of the original sizes as indicated in Table 2-2.

Table 2-2 Cache Size with 7-bit tag and 1 dirty bit

Cache Size	Data RAM	Tag RAM	Cacheable Size
256K	32Kx32x2	8Kx8	32M
512K	32Kx32x4	16Kx8	64M
1M	32Kx32x8	32Kx8	128M

In reality, the L2 Cacheable DRAM Size is determined by:

1) Max. L2 Cacheable Size as described in Table 2-1 and Table 2-2.

2) Non-Cacheable Area defined in register 56h, 57h, 58h and 59h and

3) C, D, E, F Segment Cacheability defined in registers 80h~86h.

4) Non-cacheable SMRAM area

But, the L1 Cacheable size is only determined by 2), 3), 4) and the maximum DRAM size, i.e., 512M bytes. Thus, the cycles with address ranging over the L2 Cacheable Size but within the 512M bytes can also be cacheable to L1. The behavior of KEN# is ruled by the L1 cacheability. Note that only code of C, D, E, F segment is cacheable to L1/L2, and the data portion of C, D, E, F segment is not cacheable to L1/L2.

Table 2-3 Synchronous SRAM Speed Settings

	Data RAM Speed			**Tag RAM Speed**			**Read Performance**	**Write Performance**
	66 MHz	60 MHz	50 MHz	66 MHz	60 MHz	50 MHz		
Pipelined SRAM	15ns	15ns	20ns	12ns	12ns	20ns	3-1-1-1	3-1-1-1
				15ns	15ns	20ns	4-1-1-1	4-1-1-1

NOTE: (1) The SRAM parameters of data RAMs showed in above table are "cycle time".
(2) Use asynchronous SRAM for Tag RAM.

SRAM Address Mapping

Table 2-4 TAG=8-bit

	256K	**512K**	**1M**
TA7	HA23	HA23	HA23
TA6	HA22	HA22	HA22
TA5	HA21	HA21	HA21
TA4	HA20	HA20	HA20
TA3	HA19	HA19	HA27
TA2	HA18	HA26	HA26
TA1	HA25	HA25	HA25
TA0	HA24	HA24	HA24

Table 2-5 TAG=7-bit

	256K	**512K**	**1M**
TA6	HA22	HA22	HA22
TA5	HA21	HA21	HA21
TA4	HA20	HA20	HA20
TA3	HA19	HA19	HA23
TA2	HA18	HA23	HA26
TA1	HA23	HA25	HA25
TA0	HA24	HA24	HA24

NOTE: TA7 acts as ALT.

2.3 DRAM Controller

The 5596 can support up to 512Mbytes of DRAM. Single or Double sided 64/72 bits (with/without parity) FP (Fast Page mode) DRAM or EDO (Extended Data Output) DRAM could be used.

The installed DRAM type can be 256K, 512K, 1M, 2M, 4M or 16M bit deep by n bit wide DRAM, and both symmetrical and asymmetrical type DRAM are supported. It is also permissible to mix the EDO DRAM and FP DRAM bank by bank and corresponding DRAM timing will be switched automatically according to register setting. But if the FP and EDO DRAM are mixed in the same bank, they'll recognized as FP DRAM.

2.3.1 DRAM Configuration

The SiS5596 has four RAS# (RAS[3:0]#) and eight CAS# (CAS[7:0]#) output signals. The DRAM configuration that it can support is described as below.

Suppose there are four DRAM banks, i.e. bank0~3.

1. If there are just two banks used, i.e. bank0 and bank1, the single/double sided DRAM modules can be used with arbitrary order.
2. If there are three banks used, the single sided DRAM module can be used in all banks. But if double sided DRAM module is used, it must be plugged in bank1. In other words, SiS5596 just supports double sided DRAM in bank1 when three banks are used concurrently.
3. If there are four banks used, the single sided DRAM module can still be used in all banks. But it can't support the double sided DRAM module when four banks are used at the same time.
4. Each bank can be half populated bank, but the DRAM module must be plugged in the even SIMM of bank.

Two Banks

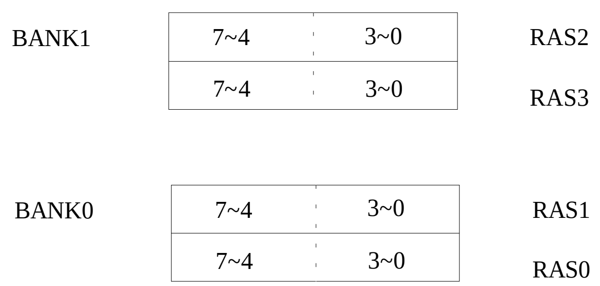


Figure 2.1

Three Banks

BANK2	7~4	3~0	RAS1
BANK1	7~4	3~0	RAS3
	7~4	3~0	RAS2
BANK0	7~4	3~0	RAS0

Figure 2.2

Four Banks

BANK3	7~4	3~0	RAS3
BANK2	7~4	3~0	RAS1
BANK1	7~4	3~0	RAS2
BANK0	7~4	3~0	RAS0

Figure 2.3

The DRAM address MA[11:0] and CAS[7:0]# are connected to each bank.

There are several DBRs (DRAM Bank Register). The DRAM type is recorded in DBR which includes the status of FP/EDO, Half/Full populated and Symmetrical/ Asymmetrical DRAM for each bank. If the DRAM types of even and odd SIMM are different, the type of smaller one is recognized. The accumulated DRAM density is programmed to DBRs which is described below. Note that DBRx-0 has the same value as DBRx-1.

DBR0-0 = DBR0-1 = Amount of DRAM corresponding to RAS0#

DBR1-0 = DBR1-1 = DBR0-0+Amount of DRAM corresponding to RAS2#

DBR2-0 = DBR2-1 = DBR1-0+Amount of DRAM corresponding to RAS1#

DBR3-0 = DBR3-1 = DBR2-0+Amount of DRAM corresponding to RAS3#

By the definition of DBR above, the double sided DRAM in Bank0 will affect the amount of DRAM corresponding to RAS0# and RAS1#. In addition, if the even SIMM of bank0 is plugged with single sided DRAM and the odd SIMM is plugged with double sided DRAM, then half size of the doubled sided DRAM will appear in the amount of DRAM corresponding to RAS1#, and be recognized as half populated. These rules are also applied to Bank1. Some situations are listed below for reference.

	Bank0	**Bank1**	**Bank2**	**Bank3**
	DBR0-x	DBR1-x	DBR2-x	DBR3-x
Configuration	Sa,Sa	Sb,Sb	-	-
value of DBR	2a	2a+2b	2a+2b	2a+2b
Configuration	De,De	Sa,Sa	-	-
value of DBR	e	e+2a	2a+2e	2a+2e
Configuration	Sa,Sa	De,De	-	-
value of DBR	2a	2a+e	2a+e	2a+2e
Configuration	Sa,D2a	Sb,D2b	-	-
value of DBR	2a	2a+2b	3a+2b	3a+3b
Configuration	De,De	Df,Df	-	-
value of DBR	e	e+f	2e+f	2e+2f
Configuration	Sa,Sa	De,De	Sb,Sb	-
value of DBR	2a	e+2a	2a+e+2b	2a+2b+2e
Configuration	Sa,Sa	Sb,Sb	Sc,Sc	Sd,Sd
value of DBR	2a	2a+2b	2a+2b+2c	2a+2b+2c+2d

where

Sx / Dx indicate single-sided or double-sided DRAM with size equal to X.

2.3.2 DRAM Address Mapping

The following tables show the different address mapping for different DRAM configuration.

Table 2-6 Non-Interleave 64-bit (FP, EDO)

	256K Sym.		**1M Sym.**		**4M Sym.**		**16M Sym.**	
MA	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**
0	4	12	4	22	4	22	4	22
1	11	13	11	13	11	24	11	24
2	3	14	3	14	3	14	3	26
3	5	15	5	15	5	15	5	15
4	6	16	6	16	6	16	6	16
5	7	17	7	17	7	17	7	17
6	8	18	8	18	8	18	8	18
7	9	19	9	19	9	19	9	19
8	10	20	10	20	10	20	10	20
9	NA	NA	12	21	12	21	12	21
10	NA	NA	NA	NA	13	23	13	23
11	NA	NA	NA	NA	NA	NA	14	25

	512K Asym.		**1M Asym.**		**2M Asym.**		**4M Asym.**	
MA	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**
0	4	12	4	12	4	22	4	22
1	11	13	11	13	11	13	11	13
2	3	14	3	14	3	14	3	14
3	5	15	5	15	5	15	5	15
4	6	16	6	16	6	16	6	16
5	7	17	7	17	7	17	7	17
6	8	18	8	18	8	18	8	18
7	9	19	9	19	9	19	9	19
8	10	20	10	20	10	20	10	20
9	NA	21	NA	21	12	21	12	21
10	NA	NA	NA	22	NA	23	NA	23
11	NA	NA	NA	NA	NA	NA	NA	24

	12x8 Asym.		**12x9 Asym.**	
MA	CAS	RAS	CAS	RAS
0	4	22	4	22
1	10	13	11	13
2	3	14	3	14
3	5	15	5	15
4	6	16	6	16
5	7	17	7	17
6	8	18	8	18
7	9	19	9	19
8	NA	20	10	20
9	NA	21	NA	21
10	NA	12	NA	23
11	NA	11	NA	12

Table 2-7 Non-Interleave 32-bit

	256K Sym.		**1M Sym.**		**4M Sym**		**16M Sym**	
MA	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**
0	4	12	4	12	4	22	4	22
1	2	13	2	13	2	13	2	24
2	3	14	3	14	3	14	3	14
3	5	15	5	15	5	15	5	15
4	6	16	6	16	6	16	6	16
5	7	17	7	17	7	17	7	17
6	8	18	8	18	8	18	8	18
7	9	19	9	19	9	19	9	19
8	10	11	10	20	10	20	10	20
9	NA	NA	11	21	11	21	11	21
10	NA	NA	NA	NA	12	23	12	23
11	NA	NA	NA	NA	NA	NA	13	25

	512K Asym.		**1M Asym.**		**2M Asym.**		**4M Asym.**	
MA	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**	**CAS**	**RAS**
0	4	12	4	12	4	22	4	22
1	2	13	2	13	2	13	2	13
2	3	14	3	14	3	14	3	14
3	5	15	5	15	5	15	5	15
4	6	16	6	16	6	16	6	16
5	7	17	7	17	7	17	7	17
6	8	18	8	18	8	18	8	18
7	9	19	9	19	9	19	9	19
8	10	20	10	20	10	20	10	20
9	NA	11	NA	21	11	21	11	21
10	NA	NA	NA	11	NA	12	NA	23
11	NA	NA	NA	NA	NA	NA	NA	NA

	12x8 Asym		**12x9 Asym.**	
MA	**CAS**	**RAS**	**CAS**	**RAS**
0	4	12	4	22
1	2	13	2	13
2	3	14	3	14
3	5	15	5	15
4	6	16	6	16
5	7	17	7	17
6	8	18	8	18
7	9	19	9	19
8	NA	20	10	20
9	NA	21	NA	21
10	NA	10	NA	12
11	NA	11	NA	11

2.3.3 DRAM Performance

All the DRAM cycles are synchronous with the CPU clock. The following table shows the different possible speed settings that depend on different DRAM type, RAS# setting, CAS# setting, and so forth.

Table 2-8 DRAM Performance

Cycle Type	DRAM type	66/60 MHz	50MHz
Read Page hit	EDO	5-2-2-2	5-2-2-2
	FP	5-3-3-3	5-2-2-2
Read Row start	EDO/FP	7-3-3-3	7-3-3-3
Read Page miss	EDO/FP	11-3-3-3	11-3-3-3
Post Write	EDO/FP	3-1-1-1	3-1-1-1
Write Retire (Buffer to DRAM)	EDO	2/3	2/3
	FP	3/4	3/4

There is a one level built-in CPU to Memory post-write buffer with 4 Quad Word deep (CTMFF). All the write access to DRAM will be buffered. For the CPU read miss / Line fill cycle, the write-back data from the second level cache will be buffered first, and the SiS5596 will start to read data from DRAM at the same time. The buffered data are written to DRAM right after the read cycle. With this concurrent write back policy, many wait states are eliminated. However, any other cycle targeting DRAM will be pending until the CTMFF is empty.

For the read access, there will be either single or burst read cycle to access the DRAM which depends on the cacheability of the cycle. If the current DRAM configuration is half-populated bank, then the SiS5596 will assert 8 consecutive cycles to access DRAM for the burst cycle. For the single cycle that only accesses DRAM within a Dword, the SiS5596 will only issue one cycle to access DRAM. For the single cycle that accesses one Qword or cross Dword boundary, the SiS5596 will issue two consecutive cycles to access DRAM.

2.3.4 Refresh cycle

The refresh cycle will occur every 15.6 us. It is timed by a counter of 14Mhz input. The CAS[7:0]# will be asserted at the same time. The RAS[3:0]# are asserted sequentially. In order to reduce the impact of performance, the "Intelligent Refresh" will only refresh those populated banks.

2.3.5 Characteristics of Shadow RAM

The SiS5596 defines the characteristics of any 16K memory block between 640 KBytes to 1 MByte address range through register 80h to 86h. Through these registers, the memory blocks

can be programmed not only to be directly accessible by the CPU or PCI Bus Master (combined with another enable bit for PCI Master accessible), but also their cacheability attributes. There are three bits: Read Enable, Write Enable, and Cache Enable, in each registers to define the corresponding memory blocks as normal read/write DRAM function, these bits also specify the cacheability of these blocks to the first/second level cache.

Table 2-9 shows the attributes of these enable bits, Table 2-10 is the attribute bits assignments and the attribute definitions, and Table 2-11 represents the registers and their corresponding memory segments.

Table 2-9 Attributes of Enable Bits

Read Enable	When this bit is set to 1, the CPU read cycles that access to the corresponding memory block are regarded as normal DRAM read cycles. Otherwise, the read cycles are directed to the PCI bus.
Write Enable	When this bit is set to 1, the CPU write cycles that access to the corresponding memory block are regarded as normal DRAM write cycles. Otherwise, the write cycles are directed to the PCI bus.
Cache Enable	When this bit is set to 1, the corresponding memory block is programmed to be L1/L2 cacheable. Note that the cacheable function is for code portion only, and the cacheability works only if Read Enable bit is also enabled.

Table 2-10: Attribute Bit Assignments and Attribute Definitions

Read Enable	**Cache Enable**	**Write Enable**	**Attribute**	**Definition**
0	0	0	Disable	Cycles are transferred to PCI bus.
0	0	1	Write Only	Write cycles are conducted to DRAM in normal manners, and read cycles are passed to PCI bus for termination.
0	1	0	Disable	Cycles are transferred to PCI bus.
0	1	1	Write Only	Write cycles are conducted to DRAM in normal manners, and read cycles are passed to PCI bus for termination.
1	0	0	Read Only	Read cycles are conducted to DRAM in normal manners, and write cycles are passed to PCI bus for termination.
1	0	1	Read/Write	Normal DRAM Read/Write cycles.
1	1	0	Read/Cacheable	Normal DRAM read cycles and code portion is cacheable to L1/L2.
1	1	1	Read/Write/ Cacheable	Normal DRAM Read/Write cycles and code portion is cacheable to L1/L2.

NOTE: When PCI master access enable bit is set, the PCI master Read/Write cycles are served as the same as the descriptions in Table 2-9. And the relation of registers and corresponding memory blocks is described in Table 2-10.

Table 2-11 Registers and Corresponding Memory Blocks

Reg	Bits	Attribute				Memory Block
80h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0c0000-0c3fffh
	3:0	Read Enable	Cache Enable	Write Enable	Reserved	0c4000-0c7fffh
81h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0c8000-0cbfffh
	3:0	Read Enable	Cache Enable	Write Enable	Reserved	0cc000-0cffffh
82h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0d0000-0d3fffh
	3:0	Read Enable	Cache Enable	Write Enable	Reserved	0d4000-0d7fffh
83h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0d8000-0dbfffh
	3:0	Read Enable	Cache Enable	Write Enable	Reserved	0dc000-0dffffh
84h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0e0000-0e3fffh
	3:0	Read Enable	Cache Enable	Write Enable	Reserved	0e4000-0e7fffh
85h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0e8000-0ebfffh
	3:0	Read Enable	Cache Enable	Write Enable	Reserved	0ec000-0effffh
86h	7:4	Read Enable	Cache Enable	Write Enable	Reserved	0f0000-0fffffh

2.3.6 SMRAM Area Re-mapping

The SMRAM area is 64K or 32K. This area can be re-mapped to A or B segments. Table 2-12 shows the types of remapping corresponding registers setting.

Table 2-12

Reg	Bit 7	Bit 6	Logical Address	Physical Address	Size
65h	0	0	E0000~E7FFFh	E0000~E7FFFh	32K
	0	1	E0000~E7FFFh	B0000~B7FFFh	32K
	1	0	E0000~E7FFFh	A0000~A7FFFh	32K
	1	1	A0000~AFFFFh	A0000~AFFFFh	64K

2.3.7 Others

It is supported to assert the RAMW# at the end of each memory read cycle when EDO DRAM is accessed. When the power saving mode is enabled, the RAMW# pulse will be 1.5 CPU clock at least to reduce the power consumption.

The DRAM always-page-miss modes, code always-page-miss and data always-page-miss, are also supported. Once it is programmed, the DRAM cycle will be a page-start cycle.

The CAS current can be programmed as 8 mA or 4 mA by register 5Dh bit 3 and 4.

2.4 PCI Arbiter

The SiS5596 contains a high performance hidden arbitration scheme that allows efficient bus sharing among five PCI Masters and the CPU. Note that one PCI master is reserved for the PSIO chip.

The SiS5596 employs the priority rotation scheme that is done at two different layers. The first layer is shared between PSIO and four PCI Masters as a group. The second layer consists of four PCI masters with equal priority. Arbitration is done at both layers. The winner of arbitration among the four PCI masters arbitrates the PCI bus against PSIO. Fair rotation scheme applies only at layer level. The arbitration scheme assures that ISA master or DMA channels (represented by PSIO) can access the bus with short bus latency required by the traditional ISA masters or DMA devices. This implementation together with PCI Programmable Bursting Address Counter guarantees ISA device will not be starved during PCI master long bursting cycle. For example, when the maximum bursting length is 512 bytes, the maximum arbitration latency for PSIO, and PCI master is about 12us, and 40us respectively. The following two figures detail the rotation arbitration structure and its corresponding timing diagram.

Rotation Arbitration Scheme:

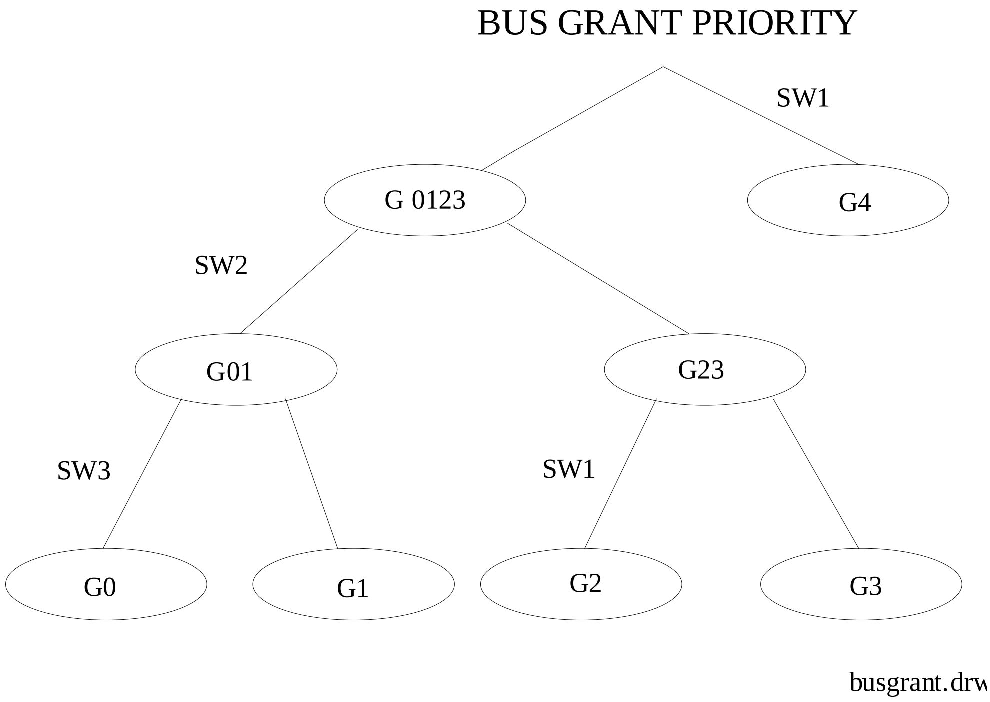


Figure 2.4

Notation:

SW1:is the switch for path from node G4 or G0123 to BUS GRANT PRIORITY

SW2:is the switch for path from node G01 or G23 to node G0123

SW3:is the switch for path from node G0 or G1 to node G01

SW4:is the switch for path from node G2 or G3 to node G23

G01,G23,G0123:are intermediate nodes

G4:is the bus request from PSIO

G0, G1, G2, G3:are the bus requests from PCI device 0, device 1, device 2, device 3 respectively.

Initial Path Parking:

SW1: BUS GRANT PRIORITY-G4

SW2: G0123-G01

SW3: G01-G0

SW4: G23-G2

Rule of Rotating Priority for Bus Arbitration:

- BUS GRANT PRIORITY will choose a path whenever it encounters an optional path.
- PCI bus will be granted as Daisy Chain
- Path switches will be toggled from BUS GRANT PRIORITY to any request node(G4,G0,G1,G2,G3) if any of them have been utilized

Example:

Initial Priority:G4,G01,G0,G2

1.PSIO(G4) Request Bus
PHLDA# is asserted
SW1 is toggled to G0123 (since it has been utilized)
Priority change to G0,G1,G2,G3,G4

2.PSIO,REQ3,REQ2,REQ1,REQ0 are requesting bus
GNT0# is asserted
SW1, SW2 and SW3 are toggled to G4, G23 and G1 respectively (since they have been utilized)
Priority change to G4,G2,G3,G1,G0

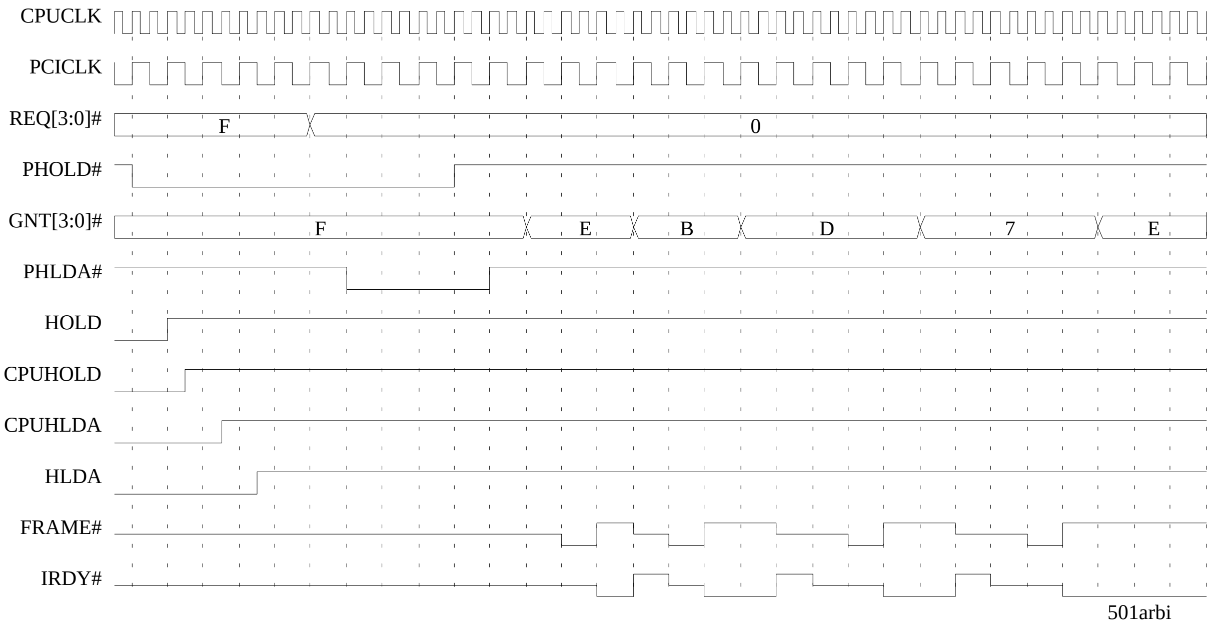
3.REQ3,REQ2,REQ1,REQ0 are active
GNT2# is asserted
SW2 and SW4 are toggled to G01 and G3 respectively(since they have been utilized)
Priority change to G4,G1,G0,G3,G2

4.REQ3,REQ2,REQ1,REQ0 are active
GNT1# is asserted
SW2 and SW3 are toggled to G23 and G0 respectively(since they have been utilized)
Priority change to G4,G3,G2,G0,G1

5.REQ3,REQ2,REQ1,REQ0 are active
GNT3# is asserted
SW2 and SW4 are toggled to G01 and G2 respectively(since they have been utilized)
Priority change to G4,G0,G1,G2,G3

6. During 3-5, if there is a request coming from PSIO, the Arbiter will grant bus to PSIO.

PCI Arbiter - Rotation Arbitration scheme



Note : HOLD and HLDA are internal signals.

Figure 2.5

A PCI master can burst so long as the PCI target can source/sink the data, and no other agent requests the bus. However, PCI specifies two mechanisms that cap a master's tenure in the presence of other requests, so that predictable bus acquisition latency can be achieved. One is the Master Latency Timer(LT) that is not implemented into the SiS5596, the other is the Target Initiated Termination. In the SiS5596, a programmable Bursting Address Counter(PBAC) is implemented to disconnect the PCI master during the long bursting cycle. In this way, high throughput is maintained, and the bus latency is still kept reasonably small. Note that the bursting length is naturally applied to PCI master to local memory accessing. When PCI master access non-local memory target, both the master and target should have the responsibility of maintaining reasonable latency.

The PCI arbiter asserts only one GNT# at any time. The SiS5596 has also implemented a time-out counter to prevent faulty device hugging the bus. If the PCI bus is granted to a PCI device and the bus is currently idle, 16 PCI clocks is the limitation that device should assert FRAME# during the period of time. If time-out occurs, the arbiter will mask request line, therefore deasserts GNT#. When this happens, all PCI devices start arbitration again. Note that PSIO is free to this constraint.

The SiS5596 will release the host bus to CPU when PCI master is not targeting to main memory. The arbiter will keep the GNT# to that PCI master until the PCI bus is idle even when other PCI master has asserted REQ# to SiS5596.

2.5 PCI Bridge

2.5.1 PCI Master Controller

The PCI Master Controller forwards the CPU cycles not targeting the local memory to the PCI bus. In the case of a 64-bit CPU request or a misaligned 32-bit CPU request, the SiS5596 assumes the read assembly and write disassembly control. A 4 level posted write buffer (CTPFF) is implemented to improve the CPU to PCI memory write performance. Except for on-board memory write cycles, any cycles forwarded to the PCI bus will be suspended until the CTPFF is empty. For PCI bus memory write cycles, the CPU data are pushed into the CTPFF if it is not full. The push rate for a DW is 3 CPUCLKs. The pushed data are, at later time, written to the PCI bus. If the consecutive written data are in DW incremental sequence, they will be transferred to the PCI bus in a burst manner.

The SiS5596 provides a mechanism for converting standard I/O cycles on the CPU bus to Configuration cycles on the PCI bus. Configuration Mechanism#1 in PCI Specification 2.0 page 61 is used to do the cycle conversion.

The SiS5596 always intercepts the first interrupt acknowledge cycle from CPU bus, and forwards the second interrupt acknowledge cycle onto the PCI bus.

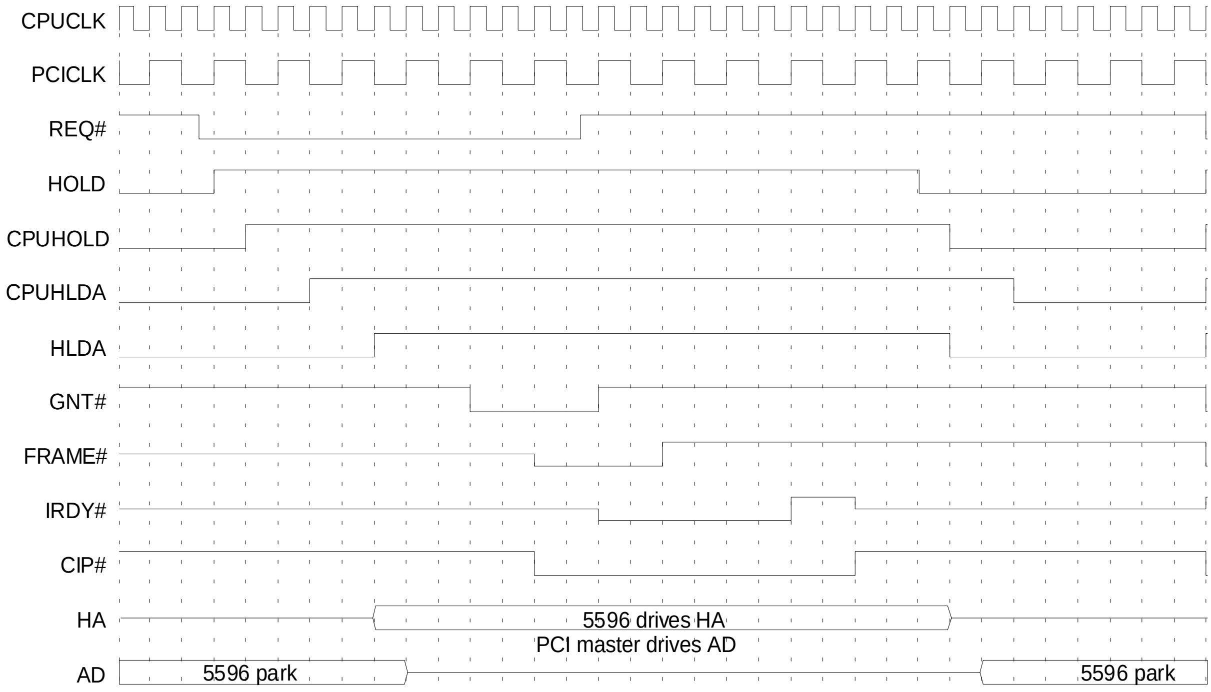
The general timing required for CPU read from/write to PCI bus is shown in the following table.

Table 2-13

CPU forwards to PCI cycle	CPUCLK=50/60/66MHz
CPU read	12~14
CPU write (nonposted)	14~16
CPU posted write	3

2.5.2 PCI Slave Controller

The SiS5596 operates as a slave on the PCI bus whenever a PCI master requests an access to the SiS5596 resource such as Cache, DRAM and the SiS5596 internal registers. Note that the internal registers can only be accessed by the SiS5596 itself when in CPU cycle. In the SiS5596 PCI/ISA system, the CPU is placed in HOLD state before granting the PCI bus to a PCI master. The following figure shows the behavior of CPUHOLD/CPUHLDA in response to PCI masters requests. Only linear ordered PCI cycles are supported by the SiS5596 PCI slave interface.



Note: HOLD, HLDA# and CIP# (current in progress) are internal signal

Figure 2.6

A PCI master to the local memory access is not conducted until the snoop cycle has completed. The snoop cycle is used to inquire the first level cache to maintain coherency between first level and second level caches and main memory. Snoop cycles are performed by driving the PCI master address onto the CPU bus and asserting EADS#. Depending on the status of HITM# two clocks after the assertion of EADS#, SiS5596 conducts the PCI master cycles as Table 2-14 outlines.

Table 2-14

PCI Master Read Cycle		
L1	L2	Data Transfer
Miss (or Unmodified)	Miss	Data transfer from DRAM to PCI
Miss (or Unmodified)	Hit (Dirty or !Dirty)(*1)	Data transfer from L2 to PCI
HitM	Miss	Data is first written back from L1 to DRAM. Then, PCI master gets data from DRAM.(*3)
HitM	Hit (Dirty or !Dirty)(*1)	Data is first written back from L1 to L2. Then, PCI master gets data from L2. The line is marked dirty in the L2.(*3)

PCI Master write Cycle		
L1	L2	Data Transfer
Miss (or Unmodified)	Miss	Data transfer from PCI to DRAM
Miss (or Unmodified)	Hit (Dirty or !Dirty)(*2)	Data transfer from PCI to DRAM and L2. The Dirty bit is not changed.
HitM	Miss	Data is first written back from L1 to DRAM. Then, PCI master writes data to DRAM.(*3)
HitM	Hit (Dirty or !Dirty)(*2)	Data is first written back from L1 to L2. Then, PCI master writes data to L2 and DRAM. The Line is marked dirty in the L2. (*3)

NOTE:

(*1) For burst or pipeline SRAM, the rule is changed as it is described below. If L2 is in WT mode, data transfer is always from DRAM to PCI side. If L2 is in WB mode, data transfer is from DRAM to PCI side if the line is not dirty. If the line is dirty, data transfer is from L2 to PCI side, and PCI transfer is disconnected after the completion of reading this line.

(*2) The rule is changed when burst or pipeline SRAM is used. No matter that the line may be dirty or not, data transfer conducts from PCI to L2 side, and PCI transfer is disconnected after the completion of writing this line.

(*3) This case is only applied to the initial line(line 0). The PCI transfer will be disconnected after the completion of line n if line n+1 is a Modified one in L1, where n>=0. The snooping write back cycle will be deferred until line n is completely transferred.

In the SiS5596, the INV signal of the CPU should be connected to W/R# that is driven by the SiS5596 in the PCI master cycle. In this way, the SiS5596 can invalidate the line that is currently inquired via the assertion of EADS# in the PCI master write cycles.

The SiS5596 slave interface supports PCI burst transfers, the bursting length can be 256 bytes, 512 bytes, 1K bytes, 2K bytes, or 4K bytes. A burst transfer will be disconnected (retry) if the transfer goes across the bursting length. In this way, at most 128 cache lines can be uninterruptedly transferred if they are in I, S, or E state in the L1 cache. Another reason for the constraint is that page miss may occur only once during the entire bursting transaction since the maximum bursting length is always within the page size in any of the used DRAM .

There is a 4QW deep FIFO to prefetch data when PCI master reads from the local memory. To achieve the utmost data transfer speed, the SiS5596 implements an advanced prefetch algorithm and snoop ahead function. It causes the PCI burst transfer performed in the pace of X-1-1-1.... SiS5596 always prefetches one or two QW from L2/DRAM in advance to the asserting of TRDY#. This can be programmed by writing bit 2 of configuration register 5Bh. The snoop ahead mechanism ensures the acquiring of the hit modify status of the next prefetching line(line n+1) before the prefetching of line n is completed. If n+1 is not a Modified line in L1, prefetching of n+1 can be conducted right after the completion of prefetching line n. In such a case, SiS5596 keeps piping data into the FIFO in L2/DRAM side, and it also keeps piping data out of the FIFO in the PCI side in 0 wait state. If n+1 is a Modified line in L1, 5512 will issue STOP# to disconnect the burst transfer after line n being consumed. This function also performs on PCI master write cycle. The PCI master writes are buffered in the 4 QW deep PCI to memory posted write buffer(PTHFF). The SiS5596 always posted an aligned QW PCI write data into the write buffer and then retires it into the DRAM array or the L2 cache. The PCI write performance is X-1-1-1.

The PCI bus data transfer rate can be calculated from the following formula.

DATA TRANSFER RATE = NB/{ X + (W + 1) * [(NB / 4) -1] } * (1 / f)

where

NB: Total number of bytes Transferred or Bursting Length which is defined in bit 6-4 of configuration register 5Bh.

X: number of PCI clocks for the first data transfer or leadoff cycle time.

W: number of wait state for PCI burst transfer

F: frequency of PCI clock

Since SiS5596 PCI bridge is designed as asynchronous to CPU clock, the PCI clock is always running at 33MHz to gain the fast transfer rate.

The leadoff cycle is in general determined by: 1) the relative clock phase between CPUCLK and PCICLK, and 2) L1 cache policy. Specifically, in the PCI master read cycle, the leadoff cycle is determined by the logic of bit 2 of register 5Bh. Moreover, whether the initial line hits L2 or whether it is a page hit or miss cycle also affects the leadoff cycle time. It is estimated that the leadoff cycle is 4 to 5 PCICLKs and 6 to 10 PCICLKs for PCI master write and read cycle, respectively. If the initial line hits a modified line in L1, ten more PCICLKs is required for the leadoff cycle. The following table illustrates the PCI Master performance in different Bursting length when the leadoff cycle is 5 and 7 for write and read, respectively.

Table 2-15

Data Transfer Rate		
PCI master cycle	7-1-1-1...read	5-1-1-1...write
Bursting length		
512 bytes	127MB/s	129MB/s
1K bytes	130MB/s	131MB/s
2K bytes	131MB/s	132MB/s
4K bytes	132MB/s	133MB/s

An important factor in the sustaining of 0 wait PCI transferring is the prefetching and retiring rate that the system controller can perform. The following table outlines the rates that SiS5596 can keep. The rate is numbered in terms of CPUCLK per Qw. For 32-bit DRAM organization, it takes twice the parameters cited below.

Table 2-16

	EDO	**FP**	**PBSRAM**
Prefetching Rate	2/3	2/3	2
Retiring Rate	2/3	3	2

Concurrent refresh will still be performed when CPU is put into Hold state. If the DRAM is idle, refresh can be conducted at any time. If refresh request occurs at the same time that a PCI master wants to access DRAM, an arbitration scheme is employed to resolve the conflict. The refresh request may thus get service while the PCI master accessing is suspended until refresh cycle is completed. Although refresh may win the DRAM bus, at most one refresh cycle may be conducted for each individual PCI transaction, i.e. for each FRAME# initiating. On the other hand, refresh may be also deferred until the DRAM is idle. In SiS5596 system, the refresh may be postponed for no more than 33 us in the worst case when a PCI master is reading the whole 128 lines through one burst transaction.

2.6 Green PC Function

The following paragraphs are the PMU (Power Management Unit) features description:

2.6.1 Power States

The PMU provides different power management states, which are described in the following sections.

(i) Monitor Standby State

The Monitor will be blanked and the external devices are turned off through SMOUT when the Monitor standby timer expires.

Monitor Standby monitors the following events:

IRQ 1-15

HOLD

NMI

Each IRQ has two sets of mask bits, one for wake up mask, and the other for standby mask. The HOLD includes the PCI local masters and the ISA master request. Each event is maskable. If no event happens during the monitored period and the timer expires, an SMI is generated and the monitor enters the standby state.

Once the Monitor is in the standby state, any event from IRQ1-15, NMI or HOLD will cause an SMI which brings the Monitor back to the normal state.

The time slot of the Monitor standby timer is programmable to 6.6sec, 0.84sec, 13.3ms, 1.6ms.

(ii) System Standby State

If the system standby timer expires, an SMI is generated for the system to enter the system standby state. The following events happen:

STPCLK# is asserted to stop the CPU clock

The hard disk drives spindle motors can be turned off

The serial, parallel ports or the programmable I/O port can be turned off

Once the STPCLK# is asserted, any events from IRQ1-15, NMI, HOLD, INIT will cause the STPCLK# be de-asserted. If any of the Hard disk motors, serial, parallel or programmable I/O ports were turned off, they will be back to the normal state only when they are accessed.

System Standby monitored events (each event is maskable)

Programmable I/O ports (one is a 10-bit I/O port, another is a16-bit I/O port)

IRQ 1-15 (each has 2 sets of mask bits as for Monitor Standby State)

HOLD

NMI

Hard Disk ports (1F0-1F7h, 3F6-3F7h, 170-17Fh, 320-32Fh)

Serial ports (2F8-2FFh, 3F8-3FFh, 2E8-2EFh, 3E8-3EFh)

Parallel ports (278-27Fh, 378-37Fh, 3BC-3BEh)

A0000-AFFFFh or B0000-BFFFFh Address trap (Video RAM)

C0000-C7FFFh Address trap (Video BIOS)

3Bx-3Dxh (Video I/O port)

The time slot of the System standby timer is programmable to 9 sec, 1.1 sec, 70ms, and 8.85ms.

(iii) Throttling state

In throttling state, STPCLK# is asserted and de-asserted periodically. This function is maskable. The throttling timer (Registers 61h and 62h) is programmable and the time slot is 35us.

2.6.2 Break Switch SMI

Whenever the break switch is pressed, it caused an SMI to enter or leave power saving state. The signal from the break switch is a level trigger signal which lasts for more than 3 CPU clocks.

2.6.3 Software SMI

If the software SMI enable bit is set and a '1' is written to bit 1 of Register 60h, an SMI# is generated and the software SMI service routine is invoked. The bit 1 of Register 60h should be cleared at the end of the SMI handler.

2.7 Internal Data Buffer

The Internal Data Buffer provides a bi-directional data buffering among the 64-bit Host Data Bus, the 64/32-bit Memory Data Bus, and the 32-bit PCI Address/Data bus. The Internal Data Buffer incorporates three FIFOs and one read buffer among the bridges of the CPU, PCI, and memory buses. This buffering scheme smoothes the differences in access latencies and bandwidths among three buses, therefore improves the overall system performance. During bus operation between the Host, PCI, and Memory, the Internal Data Buffer performs functions such as latching data, forwarding data to destination bus, data assemble and disassemble.

The main features of integrated data buffer are listed below:

-1 level CPU-to-Memory Posted Write Buffer (CTMFF) with 4 QW Deep

-4 level CPU-to-PCI Posted Write Buffer(CTPFF) with 4 DW Deep

-1 level CPU-to-PCI IDE Read Prefetch Buffer(PTHFF) with 1 DW Deep

-1 level PCI-to-Memory Posted Write Buffer(PTHFF) with 4 QW Deep

-1 level PCI-to-Memory Read Prefetch Buffer(CTPFF) with 4 QW Deep

In CPU read DRAM cycle, a one QW read buffer (CTMRB) is used to latch the DRAM data onto host bus.

2.8 Integrated VGA Controller

Integrated VGA Controller is a high performance 3-in-1 PCI true-color graphics accelerator with video accelerate functions. Integrated VGA Controller video accelerator could work in four different modes: standard FC (Feature Connector) mode, SiS FC (SiS Proprietary Defined Feature Connector) mode, direct video interface mode, and PCI multimedia mode.

Furthermore Integrated VGA Controller could work with SW MPEG Player Programs through DCI driver or Direct Draw driver to provide high performance SW MPEG playback to meet future PC trends.

In SiS FC mode, after receiving the video data from SiS 6204, Integrated VGA Controller would perform scaling and store these scaled video data to the display memory. Furthermore Integrated VGA Controller would perform color-space conversion, interpolation, and scaling on the stored video data before overlaying with graphics data for final display.

In direct video mode, Integrated VGA Controller could work with the Philips SAA7110 / SAA7111, Sony CXA1790Q, Brooktree Bt815/817/819A (8-bit SPI mode 1, 2), to provide the PC-Video solution and provide the very flexible overlaying ability mentioned above.

In PCI multimedia mode, Integrated VGA Controller supports PCI multimedia design guide Rev. 1.0 spec to meet future potential trend.

2.8.1 Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking, alternate font selection, and underlining are performed by the Attribute Controller.

2.8.2 CRT Controller

The CRT Controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the Attribute Controller.

2.8.3 CRT FIFO

The 64x32 CRT FIFO allows the Display Memory Controller to access the display memory for screen refresh at maximum memory speed rather than at the screen refresh rate. It provides 3 programmable thresholds - CRT/CPU Threshold Low, CRT/CPU Threshold High, and CRT/Engine Threshold High. With adequate programming these three thresholds, the CPU wait-time would be reduced to improve the graphics performance.

2.8.4 DDC Controller

The DDC Controller provides two different channels to communicate with the monitor which supports DDC level 1 or DDC level 2B. One is DDC CLK channel which is bidirectional and provides the clock for DDC. The other is DDC DATA channel which is bidirectional and could query some information from monitor.

With the advantage of DDC, VGA BIOS could realize the capability of the connected monitor and take adequate action (such as to program the parameters for higher frame rate, ..., etc.) to make end users feel more comfortable.

2.8.5 Display Memory Controller

The Display Memory Controller generates timing for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE*.

2.8.6 DPMS

It provides some registers to control the CRT timing to be compatible with the VESA DPMS specification.

2.8.7 Dual-Clock Synthesizer

The Dual-Clock Synthesizer generates MCLK and VCLK with single external reference clock. With this character, we could set the MCLK at the maximum speed which the display memory could work normally, thus it takes the advantage of the real peak memory bandwidth and improves the graphics performance.

2.8.8 Graphics Controller

It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

2.8.9 Graphics Engine

It is an enhanced 64-bit BitBlt Graphics Engine.

For enhanced 256-color graphics mode, the engine supports the following functions:

* 256 Raster Operation Functions
* Rectangle Fill
* Color/Font Expansion
* Enhanced Color expansion
* Enhanced Font expansion
* Line Drawing
* Built-in 8x8 Pattern Registers
* Built-in 8x8 Mask Registers
* Direct Draw

For 32K or 64K high-color graphics mode, the engine supports the following functions:

* 256 Raster Operation Functions
* Rectangle Fill
* Color/Font Expansion
* Enhanced Color expansion
* Enhanced Font expansion
* Line Drawing
* Built-in 8x8 Mask Registers
* Direct Draw

For 16M-color graphics mode, due to different graphics process methods, the engine supports the following functions:

* Source/Destination BitBlt
* Pattern/Destination BitBlt

* Color/Font Expansion
* Enhanced Font expansion

Descriptions of the graphics engine functions are summarized as follows:

Bit Block Transfer (BitBlt)

BitBlt moves a block of data from one location (source) to another location (destination). It is a ternary operation. The operands could be the source data, the destination data, and the brush pattern. There are three different kinds of BitBlt: from the host memory to the display memory, from the display memory to the host memory, and from one location of the display memory to another location of the display memory.

In the first two cases, the operation simply uses the "move string instruction" (REP MOVS) to move the source data to the destination to accomplish the BitBlt operation. It is called "CPU-driven BitBlt".

In the case of moving from the display memory to the display memory, integrated VGA Controller could gain the advantage of its advanced engine design to solve the problems of memory overlapping during the block transfers. The only effort is to program the adequate parameters.

BitBlt with Mask

When the BitBlt operation deals with the hatched brush pattern, the programmer just needs to set the monochrome mask into Mask Registers and program an adequate BG Rop and Background Color, then the engine would handle the complicated process.

Color/Font Expansion

The color/font expansion is used to expand a monochrome data (one bit per pixel) into a second color format which is n-bit per pixel during a moving operation.

The foreground color and background color is addressed respectively from I/O address 8290h to 8292h and from I/O address 8294h to 8296h. The font patterns are stored in the pattern registers (I/O address 82ACh to 82EBh) or in the off-screen memory which is called Enhanced Color/Font Expansion. These pattern registers store the monochrome bitmap. The BitBlt engine can expand 512 pixels at a time. Thus the font-drawing and monochrome bitmap expansion can be easily accomplished.

Enhanced Color Expansion

If the size of a monochrome bitmap is larger than 512 pixels, there is not enough space in pattern registers to store this bitmap. In this case, the bitmap should be stored in the off-screen display memory instead of the pattern registers. The operation is called Enhanced Color Expansion or Enhanced Font Expansion depended on the data format.

The format written into the off-screen memory of the Enhanced Color Expansion operation is m x n.

When the Command 1 Register D[5] (Enhanced Color Expansion Enable Bit, I/O address 82ABh) is set to 1, the Enhanced Color Expansion mode is enable. The SRC Start Linear

Address (I/O address 8280h to 8282h) is used to specify the starting address of the off-screen memory. Integrated Graphics Controller stores the monochrome bitmap into the assigned off-screen memory. Therefore the BitBlt engine could expand more pixels using the Enhanced Color Expansion.

Enhanced Font Expansion

The Enhanced Font Expansion is very similar to the Enhanced Color Expansion. The major difference is the format stored in the off-screen memory. The format written into the off-screen memory of the Enhanced Font Expansion operation is 8 x n.

When the Command 1 Register D[4] (Enhanced Font Expansion Enable Bit, I/O address 82ABh) is set to 1, the Enhanced Font Expansion mode is enable. The SRC Start Linear Address (I/O address 8280h to 8282h) is used to specify the start address of the off-screen memory. Integrated Graphics Controller stores the monochrome bitmap into off-screen memory byte by byte successively. Therefore the BitBlt engine would expand these pixels using the Enhanced Font Expansion.

Line Drawing

The Bresenham's Line Algorithm is a well popular algorithm in graphics, which is used to draw a line. The drawing line could be either a solid line or a dashed line. To draw a solid line, we must use one solid foreground color. To draw a dashed line, we'll use two colors specified by the foreground and background color registers. There are several registers involved to control the starting location, pixel count, error term, and line style, etc.

Rectangle Fill

A rectangle area fill is a function to fill a specified rectangle area by using either a solid color (rectangle fill) or a pattern (pattern fill).

Rectangle Fill is simply to fill the destination rectangle with a solid color. The solid color is specified into the foreground color register.

Pattern Fill repeats a source pattern into a destination rectangle. Therefore the pattern registers (I/O address 82ACh to 82EBh) must be specified. The pattern often consists of a background and foreground color because the color expansion would be used in conjunction with the pattern fill.

Raster Operations (Raster Ops or ROPs)

Raster Ops would perform some logical or arithmetic operations on the graphics data. There are 256 raster ops defined by Microsoft. Each raster op code is a Boolean operation with three operands: the source, the selected pattern, and the destination.

Direct Draw

The Windows 95 Game SDK enables the creation of world class computer games. Direct Draw is a component of that SDK that allows direct manipulation of video display memory. In order to enhance the performance of games, Integrated VGA Controller provides some Direct Draw functions.

Since the former engine functions can just support part of Direct Draw capabilities, three new functions are added into the graphics accelerator in order to meet the other Direcr Draw functions. They are color key range comparison, alpha blending, and Direct Draw raster operation.

The register format for Direct Draw is different from those of the engine's functions listed above.

To enable Direct Draw, the Direct Draw enable bits must be set to “11”. Once Direct Draw is enabled, all of the engine operations are under the “Read-Modify-Write” mode. That is, the destination data have to be read from memory for processing before being written back.

After receiving the destination data, the source and destination data are sent to the color key range comparators to determine whether they are between the high and low color key values. If they are in the color key range, the Direct Draw raster operation (D_Rop) will determine whther the data after alpha blending or the original destination will be written back to memory.

There are two control bits for alpha blending. They are the S_Alpha bit and D_alpha Bit. The table below shows the relationship between these two control bits and the data after alpha blending.

S_Alpha	**D_Alpha**	**Data after Alpha Blending**
0	0	Source
0	1	Destination
1	0	Source
1	1	(Source+Destination)/2

2.8.10 RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC.

The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital color value to three analog voltages for red, green, and blue.

2.8.11 Read-ahead Cache

It is a 128-bit cache. With this cache, the times of the operation of display memory read would be reduced, thus increase the performance.

2.8.12 Write FIFO

The Write FIFO contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. With this queue, the Integrated VGA Controller will release CPU as soon as it records the address and data, and then write into display memory when the display memory is available. Thus CPU performance is increased.

2.8.13 Bus Interface

The Integrated VGA Controller dedicatedly supports 32-bit PCI Local Bus Standard Revision 2.1. Furthermore Integrated VGA Controller supports PCI burst write to take advantage of PCI bus advanced feature to further improve performance. But PCI burst read is not supported since it has very little impact on performance in graphics application.

2.8.14 DRAM Support

Integrated VGA Controller supports 0.5 MB, 1 MB, 1.5 MB, 2 MB, 2.5 MB, 3 MB, 3.5 MB,and 4 MB FP DRAM and EDO DRAM configuration.

2.8.15 Video Memory Data Bus Architecture

The Integrated VGA Controller uses the 64-bit DRAM data bus with peak video memory bandwidth of 220 MByte/sec for FP DRAM with 55Mhz MCLK.

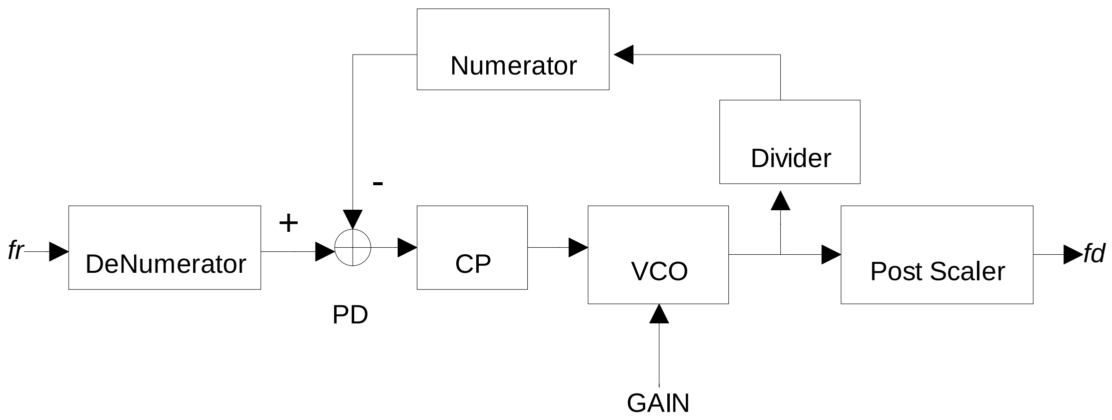
In 2MByte DRAM configuration, Integrated VGA Controller can support 1024x768x32K color, 1024x768x64K color, and 800x600x16M color resolutions with no degradation in the graphics performance.

In 4MByte DRAM configuration, Integrated VGA Controller can support 1024x768x16M color, 1280x1024x32K color, and 1280x1024x64K color resolutions. These resolutions are not easily implemented by the regular Graphics Controller architecture.

2.8.16 Internal Dual-Clock Synthesizer

Integrated VGA Controller has built-in a dual-clock synthesizer to generate the MCLK and VCLK. This clock synthesizer could generate several variable frequencies, thus it could provide the flexibility for selecting the working frequency.

The following block diagram is for clock synthesizer.



where PD is phase detection,

CP is charge pump,

VCO is voltage controlled oscillator,

fr is reference frequency, and

fd is desired frequency.

The operation of clock synthesizer is described as follow:

When the synthesizer outputs the steady frequency, it means that

fr/DeNumerator = *fd**Post Scaler /(Divider*Numerator).

i.e.

fd=*fr**(Numerator/DeNumerator)*(Divider/Post Scaler).

With this formula, we could select adequate values for Numerator, DeNumerator, Divider, and Post Scaler to obtain the desired frequency.

The planned Video Clocks (VCLK) are as follow: (units: MHz)

25.175	28.322	40.000	50.000	77.000
36.000	44.889	135.000	120.000	80.000
31.500	110.000	65.000	75.000	94.500

These frequencies are compatible with ICS2494-275 or -280.

Other video clocks would be added to the scheme after verified OK.

The planned Memory Clocks (MCLK) are from 50 MHz to 80 MHz with resolution 2 MHz.

Higher memory clocks would be added after verified OK.

2.8.17 Power Management

To satisfy the power saving for Green PC, Integrated VGA Controller supports the control protocol of DPMS (Display Power Management Signaling) proposed by VESA Monitor Committee. This protocol can reduce the VGA Monitors' power consumption.

Integrated VGA Controller has built-in two timers for stand-by and suspend modes that can be programmed from 2 minutes to 30 minutes (2 min./increase) with the extended registers.

Integrated VGA Controller also supports forcing the video subsystem into stand-by, suspend, or off modes with the extended registers.

Power saving is done by blocking HSYNC and/or VSYNC signals to the VGA monitor. The sources of activation are from the monitoring of keyboard, hardware cursor, and/or video memory read/write. The overview of the signal blocking requirements are as follows:

POWER MANAGEMENT STATE	**HORIZONTAL SYNC**	**VERTICAL SYNC**	**VIDEO DISPLAY**
ON	Pulses	Pulses	Yes

Stand-By	No Pulses	Pulses	No
Suspend	Pulses	No Pulses	No
OFF	No Pulses	No Pulses	No

2.8.18 Resolutions Supported

Resolution	0.5 MB	1 MB	1.5 MB	2 MB	2.5 MB	3MB	3.5 MB	4 MB
640x480x8	*	*	*	*	*	*	*	*
640x480x16		*	*	*	*	*	*	*
640x480x24		*	*	*	*	*	*	*
800x600x4	*	*	*	*	*	*	*	*
800x600x8	*	*	*	*	*	*	*	*
800x600x16		*	*	*	*	*	*	*
800x600x24			*	*	*	*	*	*
1024x768x4	*	*	*	*	*	*	*	*
1024x768x8		*	*	*	*	*	*	*
1024x768x16			*	*	*	*	*	*
1024x768x24					*	*	*	*
1280x1024x4		*	*	*	*	*	*	*
1280x1024x8			*	*	*	*	*	*
1280x1024x16						*	*	*

Except these real resolution modes, Integrated VGA Controller is also built-in virtual screen mode which could support up to 2048x2048 resolution.

2.8.19 Turbo Queue

In Integrated VGA Controller, the graphics engine performs the acceleration functions via the acceleration commands stored in the command queue. The command queue is a FIFO (First In First Out) and ring structure. i.e. If an acceleration command is filled in the last stage of the command queue, then the following acceleration command would be filled in the first stage of the command queue.

Once this command queue is congested, the CPU's request will be pending until the command queue has free space to accept more acceleration commands. This would downgrade the graphics system performance severely. Thus the length of command queue will dominate the performance of the graphics engine.

To lengthen the command queue as long as required, Integrated VGA Controller provides two different kinds of command queue. The first one is built in Integrated VGA Controller, which is called Hardware Command Queue. The other one is built in the off-screen display memory, which is called Turbo Queue.

The Hardware Command Queue is a 32 doublewords queue built in front of the graphics engine. Since the average length of an engine command is 8 doublewords, it could be regarded as 5 stages command queue, the first one is in the active state and the last four are in the wait states.

The Turbo Queue is an extraordinary structure developed and patent pending by SiS Corp.

The system configuration of the two command queues and the graphics engine is shown in the following diagram.

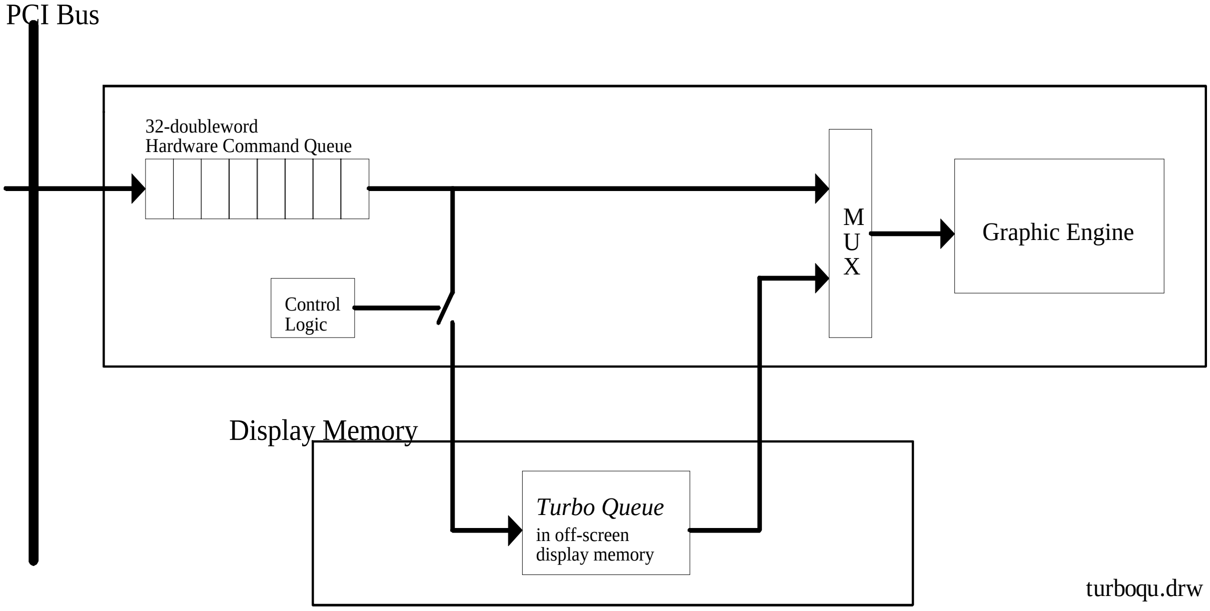


Figure 2.7 Turbo Queue Architecture

The Turbo Queue is also a FIFO and ring structure as stated before. The size of the Turbo Queue in Integrated VGA Controller is 32K bytes. Thus the stages of graphics engine could be regarded as infinity. It could get rid of the disadvantages of the CPU waiting problems due to the limited length of command queue and It could get extra high graphics performance.

To program the extended register SR2C (Turbo Queue Base Address Register) could allocate the Turbo Queue into the off-screen region of the display memory automatically. Once the commands in the Hardware Command Queue were moved into the Turbo Queue, the free space in the Hardware Command Queue could be vacated to store the next acceleration command and the condition of CPU waiting could be avoided. If both the command queues are not empty, the graphics engine would perform the commands in Turbo Queue first until Turbo Queue is empty.

2.8.20 Video Accelerator

Video Password/Identification Register

A video registers protection is implemented in the index 80h of CRT index register 3D4. To disable the protection, the software must first match the protection key value of 86h. If not match, read/write to any of the video associated registers are denied.

Video Capture and PlayBack

Integrated VGA Controller video accelerator can work in four different modes: standard FC (feature connector) mode, SiS FC (SiS Proprietary Defined Feature Connector) mode, direct video mode, and PCI multimedia mode.

In standard FC mode, Integrated VGA Controller supports standard FC operation.

In SiS FC mode, Integrated VGA Controller would co-operate with SiS 6204 MPEG and/or video adapter. After receiving the video data from SiS 6204, Integrated VGA Controller would perform scaling and store these video data to display memory. Furthermore Integrated VGA Controller would perform color-space conversion, interpolation, and scaling on the stored video data before overlaying with graphics data for final display.

The SiS proprietary defined feature connector are described in the next table:

Symbol	FC Pin No.	Description
VIDEO[7:0]	1-8	Video Data The 8-bit video data format can be RGB 555, RGB 565, YUYV 422, YVYU 422, UYVY 422, VYUY 422 and Brooktree ByteStream™ format.
VDDE	10	Video Data Valid Active high signalWhen VDDE is high, the video data will be captured by Integrated VGA Controller.
PCLK	9	Video pixel clock The video data output is based on PCLK. The frequency should be under 30MHz.
VDVSYNC	18	Video Data Vertical Sync Signal This signal is active when frame is change. The positive edge will be detected.
VDFIELD	19	Video Data Field Signal This signal indicates the current frame is odd or even frame.
EVIDEO	17	Enable Video Data Intput Active low When this pin is low and the video controller is programmed to video capture mode, the video data can be transformed from Feature Connector or direct input by using the same signal definition.

In direct video mode, Integrated VGA Controller could work with the Philips SAA7110 / SAA7111, Sony CXA1790Q, and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) to provide the PC-Video solution and provide the very flexible overlaying ability mentioned above.

In PCI multimedia mode, Integrated VGA Controller supports PCI multimedia design specification to meet future potential trend.

In addition to the SiS proprietary video solution, Integrated VGA Controller also supports the industry standard FC spec to provide a standard video link to the third-parties' video adapters.

Furthermore in PCI multimedia mode, Integrated VGA Controller supports PCI multimedia design guide Rev. 1.0 spec to meet future potential trend.

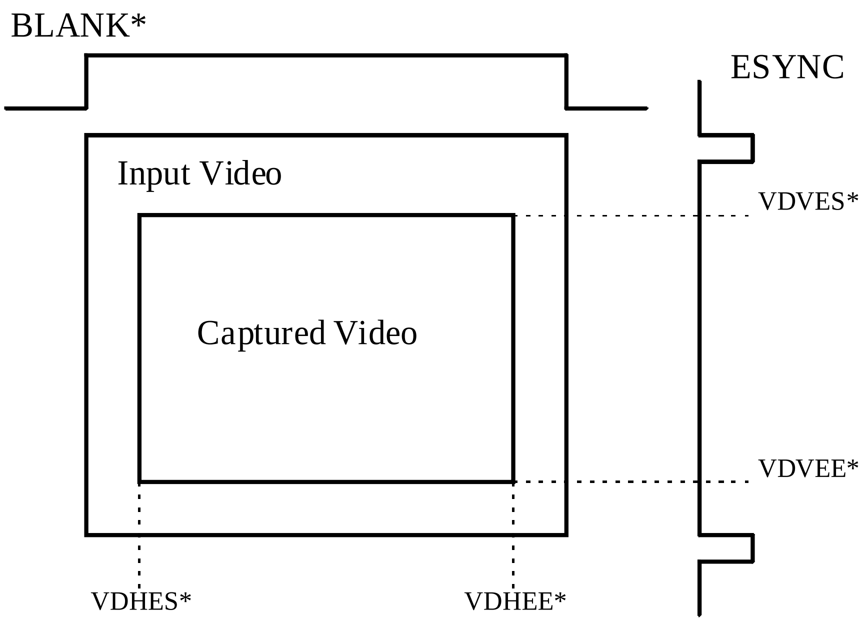
Feature Connector Interface

In standard feature connector mode, Integrated VGA Controller would transfer the graphics data to the connected video adapter for overlay and can accept the video data from the connected video adapter.

However in SiS feature connector mode, SiS redefined the pin definition of the feature connector allowing SiS 6204 to pass the video data to Integrated VGA Controller. The passed video data format is RGB565 and the maximum data rate is 30 MByte/sec. The RGB565 data are 16-bit. SiS 6204 would transfer the 16-bit data by two successive bytes cycle. Integrated VGA Controller would recover the data back to RGB565 format.

The data input/output direction of Integrated VGA Controller is controlled by the ESYNC, EVDCLK, EVIDEO pins and is automatically controlled by BIOS.

Video Capture Window



Integrated VGA Controller provides video capture windowing to select a part of input video to be captured into video frame buffer. This capture window is defined by four parameter: video data horizontal start (VDHES), video data horizontal end (VDHEE), video data vertical start (VDVES), and video data vertical end (VDVEE).

There are the video data horizontal counter and the video data vertical counter inside Integrated VGA Controller. The video data horizontal counter is reset at the positive edge of signal BLANK* and counted up by PCLK or LLC1. The video data vertical counter is reset at the positive edge of ESYNC and counted up by positive of BLANK*. When the value of the video data horizontal counter is equal to or greater than VDHES and the video data vertical counter is equal to or greater than VDVES, the video data capture starts or continues. After the value of the video data horizontal counter is equal to or greater than VDHEE or the video data vertical counter is equal to or greater than VDVEE, the video capture ends.

Video Captured Down Scaling

Integrated VGA Controller provides independent X-Y down scaling of the captured video image in integer increments of 1/64. Images may be scaled down to n/64 (n = 1 ~ 64) of the original image size to support video icons for graphics user interfaces, or to reduce the memory bandwidth. The scaling factor is controlled by HDSF and VDSF, which ranging from 0 to 63, and the scaling factors are (64-HDSF)/64 in horizontal and (64-VHSF)/64 in vertical.

Video Capture FIFO

The scaled-down video data would be fed into the video capture FIFO before being stored to display memory. The 64x16 video capture FIFOs serve as buffers between the video capture mechanisms and the display memory, are provided to fit the bandwidth limitation of the display memory during video image capture operation.

Multi-format Video Frame Buffer

The video frame buffer of Integrated VGA Controller is shared with graphics frame buffer and is a multi-format frame buffer. It could accept 16-bpp YUV422, RGB555, and RGB565 color format.

The decompression CODEC, hardware or software, could fill the valid decompressed video frame data into the off-screen video frame buffer through the PCI local bus.

The other PCI motion video card or CPU can transfer the video data through PCI local bus directly into video frame buffer.

Thus Integrated VGA Controller can overlay the video on the screen.

Video Playback Line Buffers

When CRT refresh the screen, the video data must be overlaid with graphics data. Therefore the video data would first be read out from off-screen video frame buffer into the video playback line buffers for further handling.

The video playback line buffers serve as buffers between display memory and the playback mechanisms, are provided to fit the limitation of the display memory during video playback operation.

Color Space Conversion & Color Format Conversion

If the data read from the video frame buffer is in YUV422, the real time YUV-to-RGB converter will be turn on. The video data would be converted to RGB888 format for successive processing. The YUV422 are converted following the CCIR601-2 standard.

If the data read from the video frame buffer is in RGB format, the YUV-to-RGB converter would be bypassed. All the RGB565 and RGB555 format are supported and then would be converted to RGB888 format.

Horizontal Interpolation DDA

The DDA (Digital Differential Accumulator) using the following mathematical calculation with 2-tap, N-phase and scaling up factor UFACT (from J points scaling up to J * UFACT points):

$$\text{Destination}[i] = (1 - \text{Weight}) * \text{Source}[j] + \text{Weight} * \text{Source}[j+1]$$

j = TRUNC(i / UFACT)

Weight" = TRUNC(i / UFACT) - j

However since the Weight" is not an integer, the multiplication is hard to implement and therefore the following Weight is used for calculation.

Weight = TRUNC(Weight" * N) / N

The Integrated VGA Controller built-in an X-interpolation DDA mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

Vertical Interpolation DDA

The Integrated VGA Controller built-in a Y-interpolation DDA mechanism and two line buffers mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

Video Playback Horizontal Zooming

The playback video data can be horizontal zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in about m/16 factor (m = 1 ~ 16). The zooming factor (HPFACT) is controlled by 4-bit integer part and 6-bit fraction part. The horizontal video size will be zoomed to 1/HPFACT. If HPFACT<1, it will performing horizontal up scaling. If HPFACT>1, it will performing horizontal down scaling.

Video Playback Vertical Zooming

The playback video data can be vertical zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in arbitrary factor. The zooming factor (VPFACT) is controlled by 6-bit fraction part. The video size will be zoomed to 1/VPFACT. Since the VPFACT is always less than 1, therefore you can only perform vertical up scaling by this factor. The vertical down scaling can be done by multiplying the Video Frame Buffer Offset with an integer I. Then the vertical video size will be zoomed to 1/(I*VPFACT).

Video Data Blending

The pixels of graphics data can be blended by graphics data alpha value, then add with the blended video data to generate blended data. The accuracy of the blending is 4 bits, the 4 MSBs of Graphic data alpha value register.

The pixels of video data can be blended by video data alpha value, then add with the blended graphics data to generate blended data. The accuracy of the blending is 4 bits, the 4 MSBs of Video data alpha value register.

Color Keying

A control signal is generated by comparing the 24 bits graphics data to the 24 bits color key low value and 24 bits clolor key high value. The bit number is dependent on color depth used. If the graphics data value is between the two color key values (all of three RGB parts), the color key is detected. This comparison mechanism can be disable by setting the video window size to zero, i.e. X-start=0, X-end=0, Y-start=0, and Y-end=0.

Chroma Keying

A control signal is generated by comparing the 24 bits video data to the 24 bits chroma key low value and 24-bit chroma key high value. The chroma key can be YUV or RGB format. If the video data value is between two chroma key values (all of three RGB or YUV parts), the chroma key is detected.

Graphics & Video Overlay

The overlay of the graphics data and the video data is performed by color keying and chroma keying method. The overlay operation is set by Key Overlay Operation Mode Register. The operation is defined below:

Operation Mode	Operation
0000	always select graphics data
0001	select blended data when color key and chroma key,otherwise select graphics data
0010	select blended data when color key and not chroma key,otherwise select graphics data
0011	select blended data when color key,otherwise select graphics data
0100	select blended data when not color key and chroma key,otherwise select graphics data
0101	select blended data when chroma key,otherwise select graphics data
0110	select blended data when color key xor chroma key,otherwise select graphics data
0111	select blended data when color key or chroma key,otherwise select graphics data
1000	select blended data when not color key and not chroma key,otherwise select graphics data
1001	select blended data when color key xnor chroma key,otherwise select graphics data
1010	select blended data when not chroma key,otherwise select graphics data
1011	select blended data when color key or not chroma key,otherwise select graphics data
1100	select blended data when not chroma key,otherwise select graphics data

1101	select blended data when not color key or chroma key,otherwise select graphics data
1110	select blended data when not color key or not chroma key,otherwise select graphics data
1111	always select blended data

Video Window Control Registers

The video window area is defined by six registers that specify a rectangular region by X-start, X-end, Y-start, and Y-end (X: Horizontal, Y: Vertical).

The location of the video window is referenced to the VGA sync signals.

The size of the video window is defined in VGA pixels and lines.

Video Panning

The displayed video image could be panned around the captured video image by setting the video display starting address. i.e. You may selectively display any part of the captured video image. The video display starting address is equal to the video frame buffer starting address adds the panning offset.

Overlay Memory Data

The display memory is configured to two areas: one is the graphics area (which is the actual screen display area) storing graphics pixel data, and the other is the video area (which is also called off-screen area) storing the video pixel data.

In the graphics area, the corresponding video window area is reserved with the color key value. During the CRT scan period, a comparison of graphics data with color key data is performed. Once a match meet, the CRT output path would be switched from graphics path to video path to display the video data.

When the shared-memory architecture is used, the video frame buffer could be anywhere of the system memory, independent with the location of the graphics frame buffer. This provides more flexiblility for video control application program. The video frame buffer should be set to non-cacheable and non-swappable.

2.8.21 Video Playback Contrast Enhancement and Brightness Control

To achieve higher video quality, the SiS 6205 built-in the Contrast Enhancement and Brightness Control mechanism.

For Contrast Enhancement, first, the brightness mean value is calculated by some pixels and some frames. The number of sampled pixels and frames is programmable by registers. Contrast Enhancement mechanism then increases the difference between the video data and mean value. The increasing rate is programmed by gain. The value of gain is from 1.0 to 1.4375.

The Brightness of video data can also be controlled. The Brightness is a 2's complement value from -128 to +127. This value is then added with the video data to increase or decrease the brightness of video.

2.8.22 Signature Analysis

The signature analysis is provided to automatically test the graphics data which is the input of the DAC. This technique is based on the concept of cyclic redundancy checking (CRC) and is realized in hardware using linear feedback shift registers (LFSRs). It is composed of a 16-bit signature generator register which is called multiple-input signature register (MISR, shown in the following figure) and is used to ensure a unique signature of different patterns.

For a given test image, the signature analysis could get a right unique signature number. If an error occurs in the controller or the data manipulation, it would result in a different wrong signature number as compared to the pre-calculated signature value. Thus a test technician could sort the good or bad chips more quickly and accurately and requires no visual inspection of the screen for errors in the mass product environment. This could save significant testing time. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different when blink-off and blink-on for those frames. Assume all error patterns are equally likely, then the probability of failing to detect an error by the MISR is approximately 0.000015.

To match the inputs of MISR, the 24-bit graphics data (i.e. the input of the DAC of the RAMDAC) would be first converted into 16-bit data. The corresponding transfer function of the MISR of the following figure is

$$p(x) = 1 + c_1 \cdot x + c_2 \cdot x^2 + c_3 \cdot x^3 + \ldots + c_{16} \cdot x^{16}$$

where can be either 0 or 1. Integrated VGA Controller sets the parameters of the signature register as

$$p(x) = 1 + x + x^7 + x^{10} + x^{16}$$

Once the software enables the signature analysis function, Integrated VGA Controller could test itself intelligently and automatically. This function could also be disabled by the extended control register for power saving purposes.

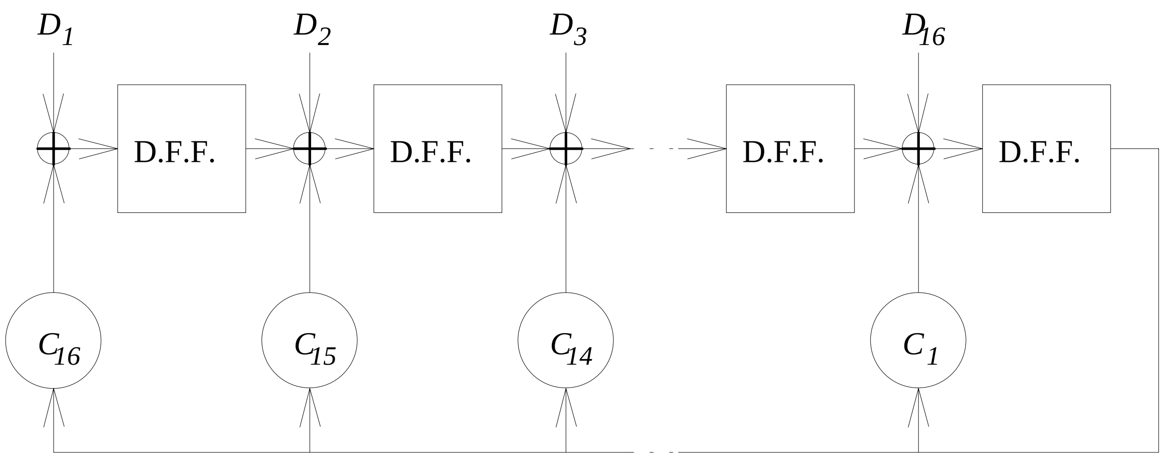


Figure 2.8 Multi-Input Signature Register (MISR)

2.8.23 Compatibility

The Integrated VGA Controller is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes.

2.8.24 Software Support

To fully utilize and support the Integrated VGA Controller hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers developed by SiS. The following applications are currently supported:

* 3D Studio Ver. 3.0 & 4.0
* AutoCAD/386 Release 11, 12, 13
* Auto Shade/386 Ver. 2.0
* GEM 3.0/Ventura 2.0
* Lotus 1-2-3/Symphony Ver. 3.x
* MicroSoft Windows 3.1
* MicroSoft Windows 95
* MicroSoft Windows NT Ver. 3.1 & 3.5
* OrCad (SDT/VST/PCB) Rel 4
* OS/2 Presentation Manager 2.1 & 3.0
* P-CAD Ver. 6.06
* VersaCAD/386 Ver. 2.1
* Word Perfect 5.x & 6.0

Video operation are supported by software application drivers developed by SiS. The following applications are currently supported:

* Microsoft Video For Windows
* DCI driver
* Direct Draw driver

2.9 Mode Table

2.9.1 Standard VGA Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
0	A/N	320x200	16	40x25	B800	8x8	8
0*	A/N	320x350	16	40x25	B800	8x14	8
0+	A/N	360x400	16	40x25	B800	9x16	8
1	A/N	320x200	16	40x25	B800	8x8	8
1*	A/N	320x350	16	40x25	B800	8x14	8
1+	A/N	360x400	16	40x25	B800	9x16	8
2	A/N	640x200	16	80x25	B800	8x8	8
2*	A/N	640x350	16	80x25	B800	8x14	8
2+	A/N	720x400	16	80x25	B800	9x16	8
3	A/N	640x200	16	80x25	B800	8x8	8
3*	A/N	640x350	16	80x25	B800	8x14	8
3+	A/N	720x400	16	80x25	B800	9x16	8
4	APA	320x200	4	40x25	B800	8x8	1
5	APA	320x200	4	40x25	B800	8x8	1
6	APA	640x200	2	80x25	B800	8x8	1
7	A/N	720x350	4	80x25	B000	9x14	8
7+	A/N	720x400	4	80x25	B000	9x16	8
0D	APA	320x200	16	40x25	A000	8x8	8
0E	APA	640x200	16	80x25	A000	8x8	4
0F	APA	640x350	2	80x25	B000	8x14	2
10	APA	640x350	16	80x25	A000	8x14	2
11	APA	640x480	2	80x30	A000	8x16	1
12	APA	640x480	16	80x30	A000	8x16	1
13	APA	320x200	256	40x25	A000	8x8	1

NOTE: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
0	320x200	16	70	31.5 K	25.1 M
0*	320x350	16	70	31.5 K	25.1 M
0+	360x400	16	70	31.5 K	28.3 M
1	320x200	16	70	31.5 K	25.1 M
1*	320x350	16	70	31.5 K	25.1 M
1+	360x400	16	70	31.5 K	28.3 M
2	640x200	16	70	31.5 K	25.1 M
2*	640x350	16	70	31.5 K	25.1 M
2+	720x400	16	70	31.5 K	28.3 M
3	640x200	16	70	31.5 K	25.1 M
3*	640x350	16	70	31.5 K	25.1 M
3+	720x400	16	70	31.5 K	28.3 M
4	320x200	4	70	31.5 K	25.1 M
5	320x200	4	70	31.5 K	25.1 M
6	640x200	2	70	31.5 K	25.1 M
7*	720x350	4	70	31.5 K	28.3 M
7+	720x400	4	70	31.5 K	28.3 M
0D	320x200	16	70	31.5 K	25.1 M
0E	640x200	16	70	31.5 K	25.1 M
0F	640x350	2	70	31.5 K	25.1 M
10	640x350	16	70	31.5 K	25.1 M
11	640x480	2	60	31.5 K	25.1 M
12	640x480	16	60	31.5 K	25.1 M
13	320x200	256	70	31.5 K	25.1 M

NOTE: i - interlaced mode
n - noninterlaced mode

2.9.2 Enhanced Video Modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
22	A/N	1056x352	16	132x44	B800	8x8	2
23	A/N	1056x350	16	132x25	B800	8x14	4
24	A/N	1056x364	16	132x28	B800	8x13	4
25	APA	640x480	16	80x60	A000	8x8	1
26	A/N	720x480	16	80x60	B800	9x8	3
29	APA	800x600	16	100x37	A000	8x16	1
2A	A/N	800x600	16	100x40	B800	8x15	4
2D	APA	640x350	256	80x25	A000	8x14	1
2E	APA	640x480	256	80x30	A000	8x16	1
2F	APA	640x400	256	80x25	A000	8x16	1
30	APA	800x600	256	100x37	A000	8x16	1
37	APA	1024x768	16	128x48	A000	8x16	1
38	APA	1024x768	256	128x48	A000	8x16	1
39	APA	1280x1024	16	160x64	A000	8x16	1
3A	APA	1280x1024	256	160x64	A000	8x16	1
40	APA	320x200	32K	40x25	A000	8x8	1
41	APA	320x200	64K	40x25	A000	8x8	1
42	APA	320x200	16.8M	40x25	A000	8x8	1
43	APA	640x480	32K	80x30	A000	8x16	1
44	APA	640x480	64K	80x30	A000	8x16	1
45	APA	640x480	16.8M	80x30	A000	8x16	1
46	APA	800x600	32K	100x37	A000	8x16	1
47	APA	800x600	64K	100x37	A000	8x16	1
48	APA	800x600	16.8M	100x37	A000	8x16	1
49	APA	1024x768	32K	128x48	A000	8x16	1
4A	APA	1024x768	64K	128x48	A000	8x16	1
4B	APA	1024x768	16.8M	128x48	A000	8x16	1
4C	APA	1280x1024	32K	160x64	A000	8x16	1
4D	APA	1280x1024	64K	160x64	A000	8x16	1

NOTE: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
22	1056x352	16	70	30.5 K	40.0 M
23	1056x350	16	70	30.5 K	40.0 M
24	1056x364	16	70	30.5 K	40.0 M
25	640x480	16	60	31.5 K	25.1 M
26	720x480	16	60	31.5 K	25.1 M
29	800x600	16	56	35.1 K	30.0 M
29*	800x600	16	60	37.9 K	40.0 M
29+	800x600	16	72	48.0 K	50.0 M
29#	800x600	16	75	46.8 K	50.0 M
29##	800x600	16	85	53.7 K	56.3 M
2A	800x600	16	56	35.1 K	36.0 M
2D	640x350	256	70	31.5 K	25.1 M
2E	640x480	256	60	31.5 K	25.1 M
2E*	640x480	256	72	37.9 K	31.5 M
2E+	640x480	256	75	37.5 K	31.5 M
2E++	640x480	256	85	43.4 K	36.0 M
2F	640x400	256	70	31.5 K	25.1 M
30	800x600	256	56	35.1 K	36.0 M
30*	800x600	256	60	37.9 K	40.0 M
30+	800x600	256	72	48.0 K	50.0 M
30#	800x600	256	75	46.8 K	50.0 M
30##	800x600	256	85	53.7 K	56.3 M
37i	1024x768	16	87	35.5 K	44.9 M
37n	1024x768	16	60	48.4 K	65.0 M
37n+	1024x768	16	70	56.5 K	75.0 M
37n#	1024x768	16	75	60.2 K	80.0 M
37n##	1024x768	16	85	68.7 K	94.5 M
38i	1024x768	256	87	35.5 K	44.9 M
38n	1024x768	256	60	48.4 K	65.0 M
38n+	1024x768	256	70	56.5 K	75.0 M
38n#	1024x768	256	75	60.2 K	80.0 M

38n##	1024x768	256	85	68.7 K	94.5 M
39i	1280x1024	16	87	48.8 K	80.0 M
39n	1280x1024	16	60	65.0 K	110.0 M
39n+	1280x1024	16	75	80.0 K	135.0 M
3Ai	1280x1024	256	87	48.8 K	80.0 M
3An	1280x1024	256	60	65.0 K	110.0 M
3An+	1280x1024	256	75	80.0 K	135.0 M
40	320x200	32K	70	31.5 K	25.1 M
41	320x200	64K	70	31.5 K	25.1 M
42	320x200	16.8M	70	31.5 K	25.1 M
43	640x480	32K	60	31.5 K	25.1 M
43*	640x480	32K	72	37.9 K	31.5 M
43+	640x480	32K	75	37.5 K	31.5 M
43++	640x480	32K	85	43.4 K	36.0 M
44	640x480	64K	60	31.5 K	25.1 M
44*	640x480	64K	72	37.9 K	31.5 M
44+	640x480	64K	75	37.5 K	31.5 M
44++	640x480	64K	85	43.4 K	36.0 M
45	640x480	16.8M	60	31.5 K	25.1 M
45*	640x480	16.8M	72	37.9 K	31.5 M
45+	640x480	16.8M	75	37.5 K	31.5 M
45++	640x480	16.8M	85	43.4 K	36.0 M
46	800x600	32K	56	35.1 K	36.0 M
46*	800x600	32K	60	37.9 K	40.0 M
46+	800x600	32K	72	48.0 K	50.0 M
46#	800x600	32K	75	46.8 K	50.0 M
46##	800x600	32K	85	53.7 K	56.3 M
47	800x600	64K	56	35.1 K	36.0 M
47*	800x600	64K	60	37.9 K	40.0 M
47+	800x600	64K	72	48.0 K	50.0 M
47#	800x600	64K	75	46.8 K	50.0 M
47##	800x600	64K	85	53.7 K	56.3 M
48	800x600	16.8M	56	35.1 K	36.0 M

48*	800x600	16.8M	60	37.9 K	40.0 M
48+	800x600	16.8M	72	48.0 K	50.0 M
48#	800x600	16.8M	75	46.8 K	50.0 M
48##	800x600	16.8M	85	53.7 K	56.3 M
49i	1024x768	32K	87	35.5 K	44.9 M
49n	1024x768	32K	60	48.4 K	65.0 M
49n+	1024x768	32K	70	56.5 K	75.0 M
49n#	1024x768	32K	75	60.2 K	80.0 M
49n##	1024x768	32K	85	68.7 K	94.5 M
4Ai	1024x768	64K	87	35.5 K	44.9 M
4An	1024x768	64K	60	48.4 K	65.0 M
4An+	1024x768	64K	70	56.5 K	75.0 M
4An#	1024x768	64K	75	60.2 K	80.0 M
4An##	1024x768	64K	85	68.7 K	94.5 M
4Bi	1024x768	16.8M	87	35.5 K	44.9 M
4Bn	1024x768	16.8M	60	48.4 K	65.0 M
4Bn+	1024x768	16.8M	70	56.5 K	75.0 M
4Bn#	1024x768	16.8M	75	60.2 K	80.0 M
4Bn##	1024x768	16.8M	85	68.7 K	94.5 M
4Ci	1280x1024	32K	89	48.8 K	80.0 M
4Di	1280x1024	64K	89	48.8 K	80.0 M

NOTE: i - interlaced mode

n - noninterlaced mode

* For the limitation of memory bandwidth in 1MB DRAM configuration, the following video modes is not supported in 1MB configuration: modes 45*, 45+, 46+, 46#, 47+, and 47#.

2.10 Application Description

The SiS5596 can be configured to support the Philips SA7110 to provide the PC-Video solution and provide the very flexible overlaying ability. The application circuit as shown below: (Please see the pin definition in this data sheet for more details.)

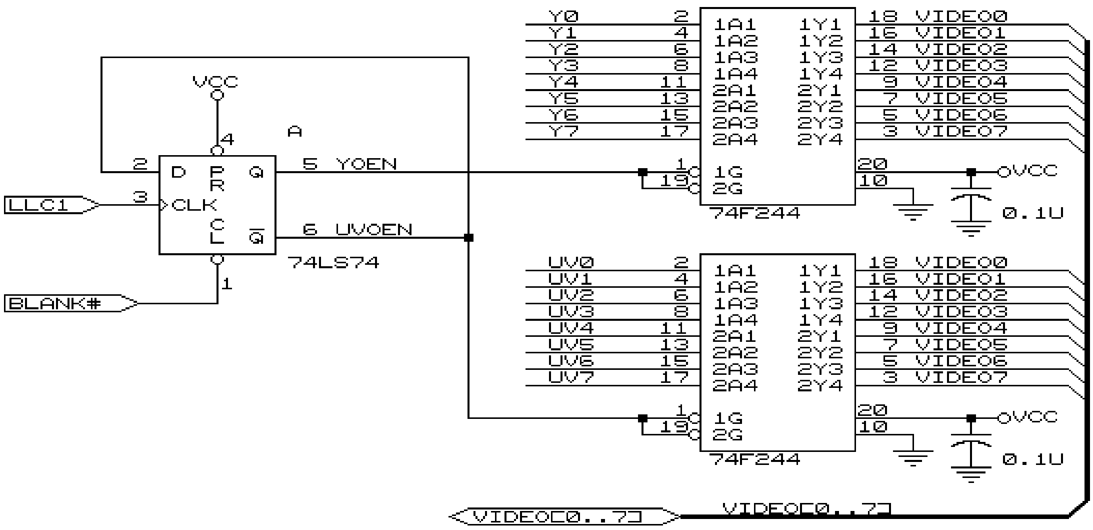


Figure 2.9

2.11 Timing Diagram

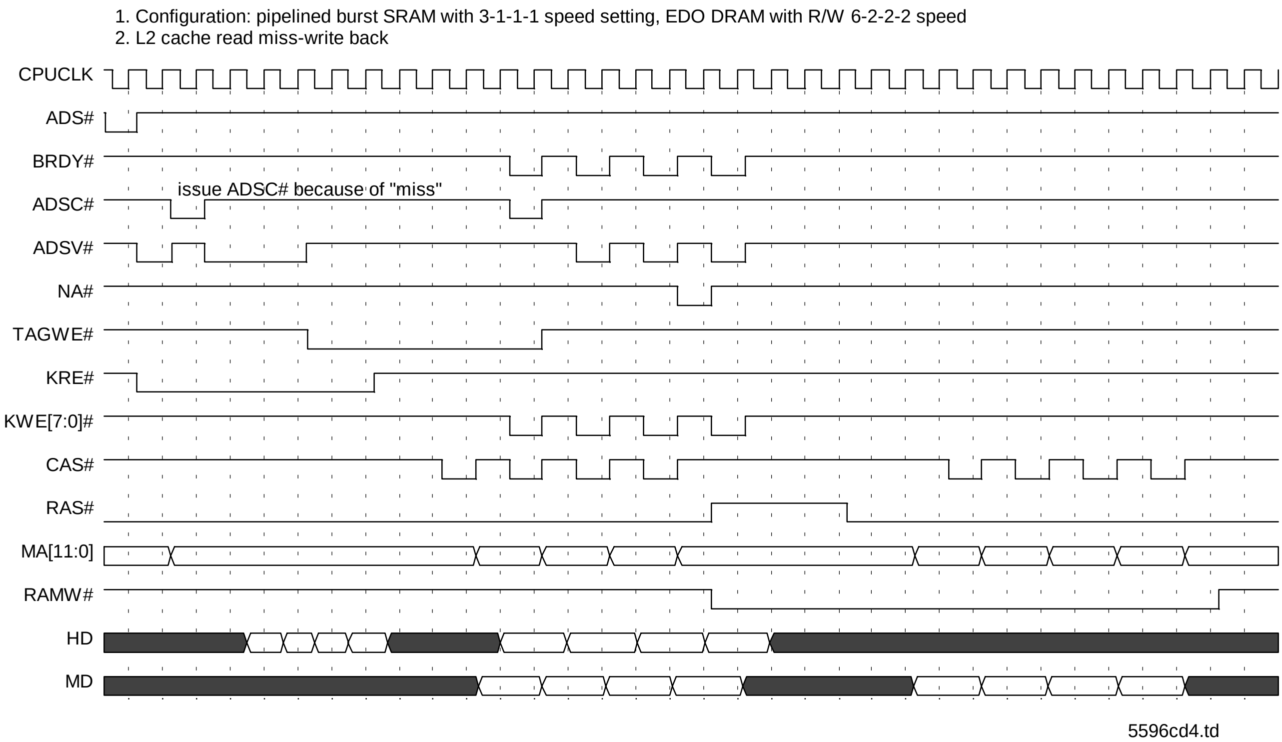


Figure 2.10

1. Configuration: pipelined burst SRAM with speed setting 3-1-1-1, FP DRAM with speed setting R/W 6-3-3-3
2. The first cycle is L2 cache read miss-write back cycle
3. The second cycle is L2 cache read hit cycle

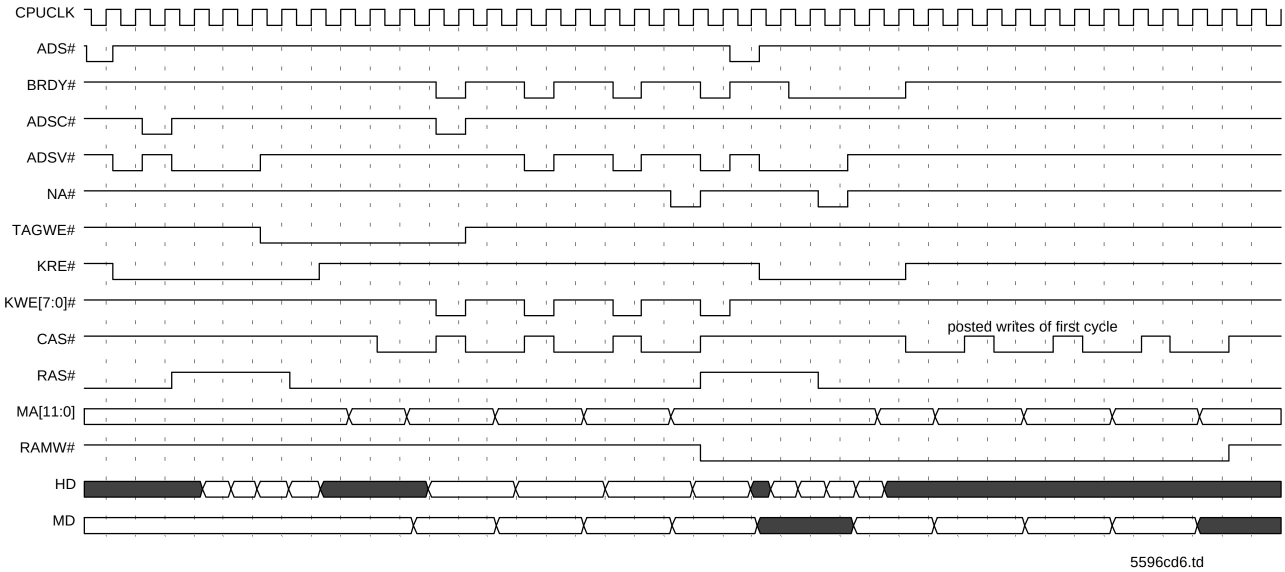


Figure 2.11

1. Configuration: pipelined burst SRAM with speed setting 3-1-1-1, EDO DRAM with speed setting 6-2-2-2
2. The first cycle is L2 cache read miss-write back cycle
3. The second cycle is L2 cache read hit cycle
4. The third cycle is L2 cache write hit cycle

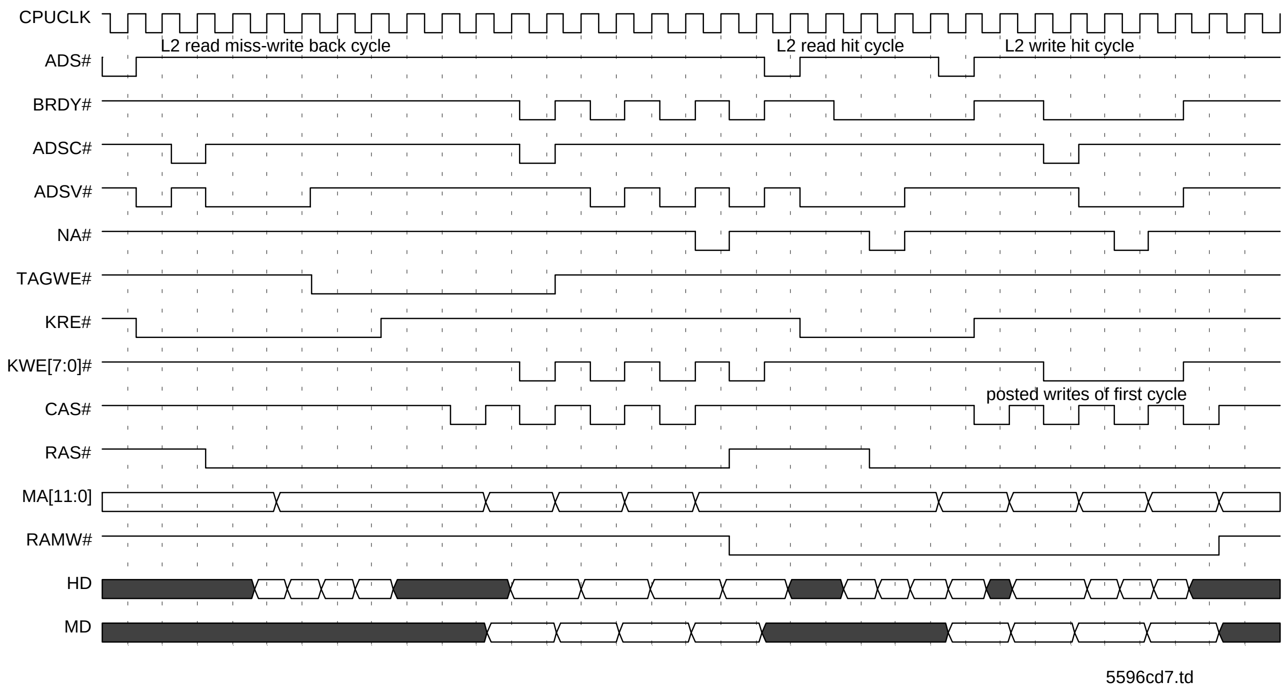


Figure 2.12

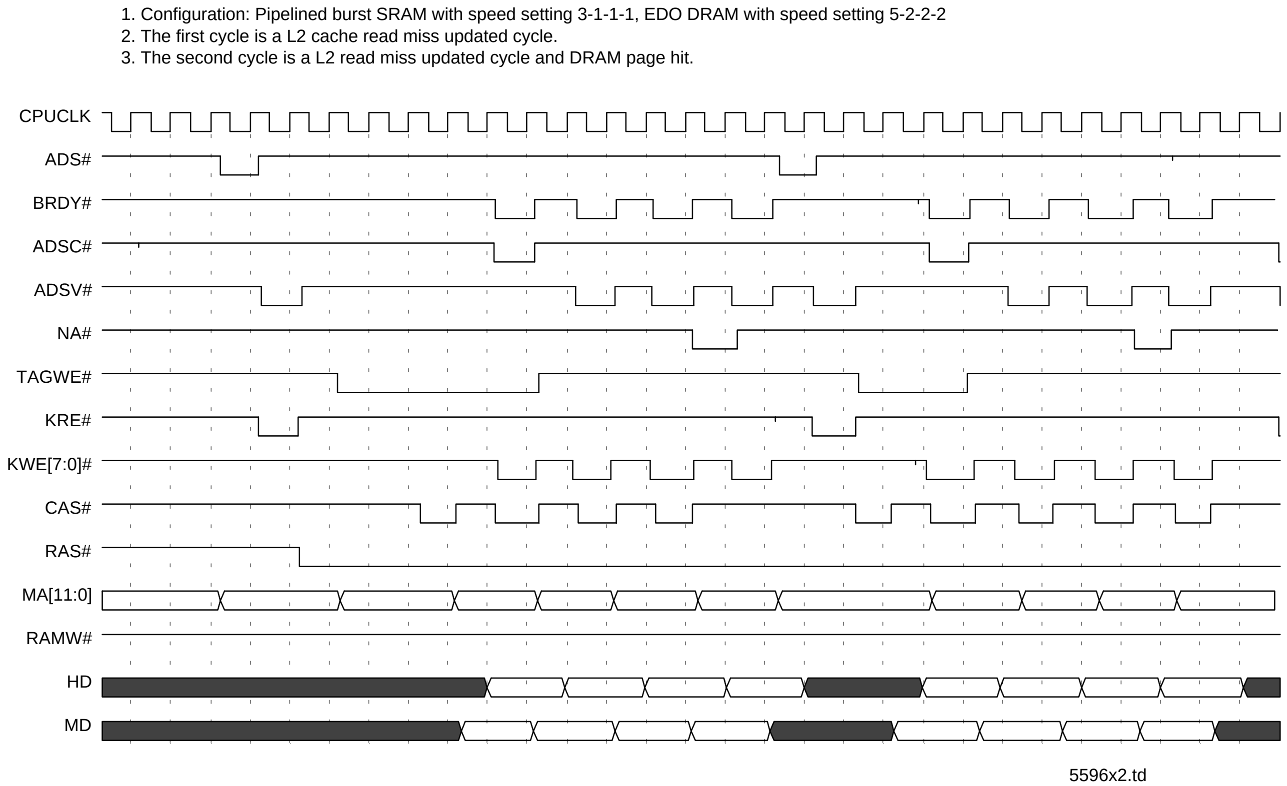


Figure 2.13

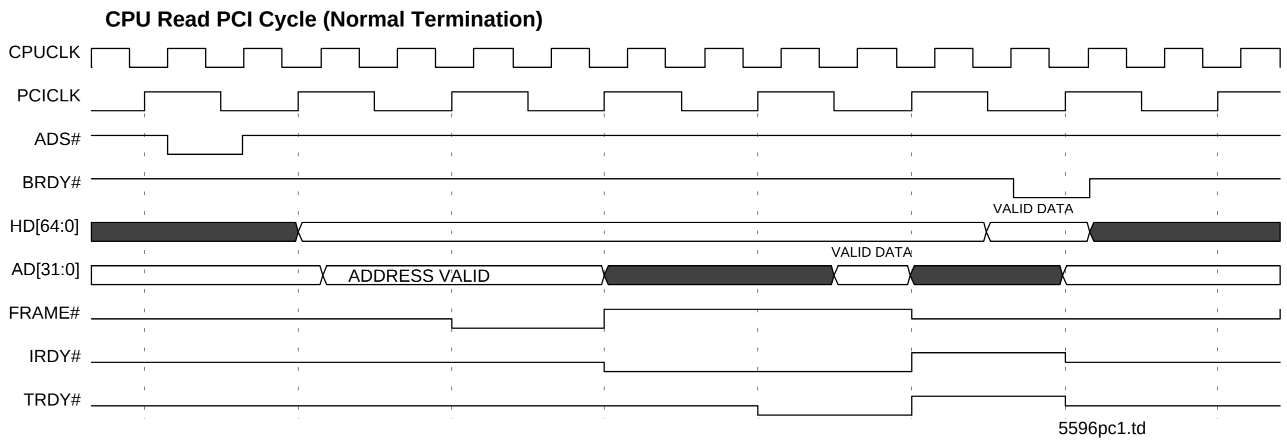


Figure 2.14

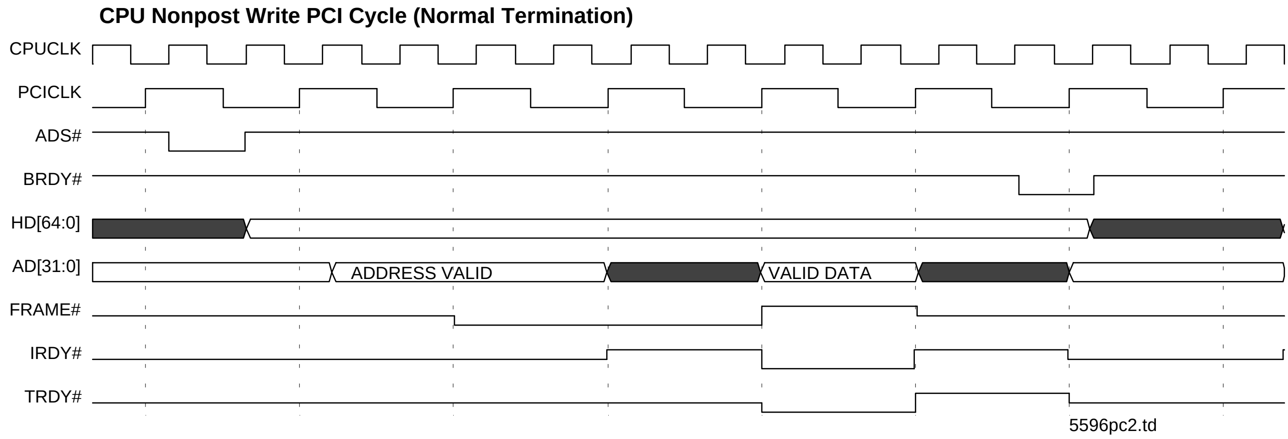


Figure 2.15

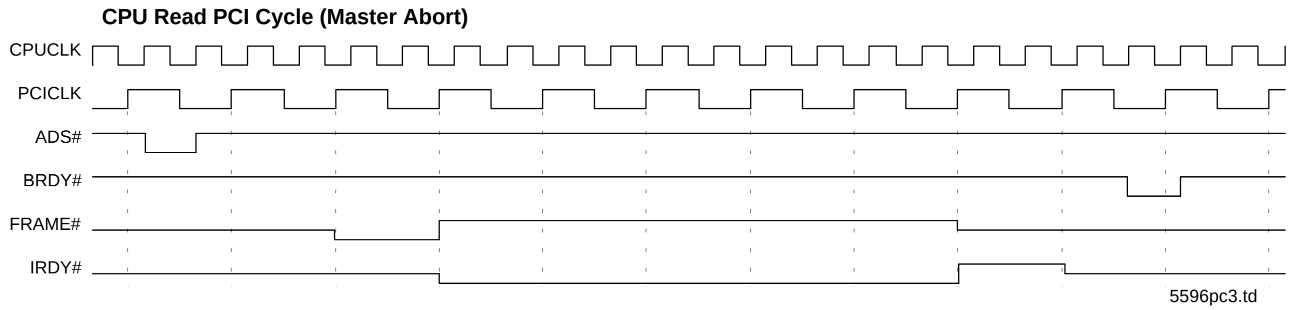


Figure 2.16

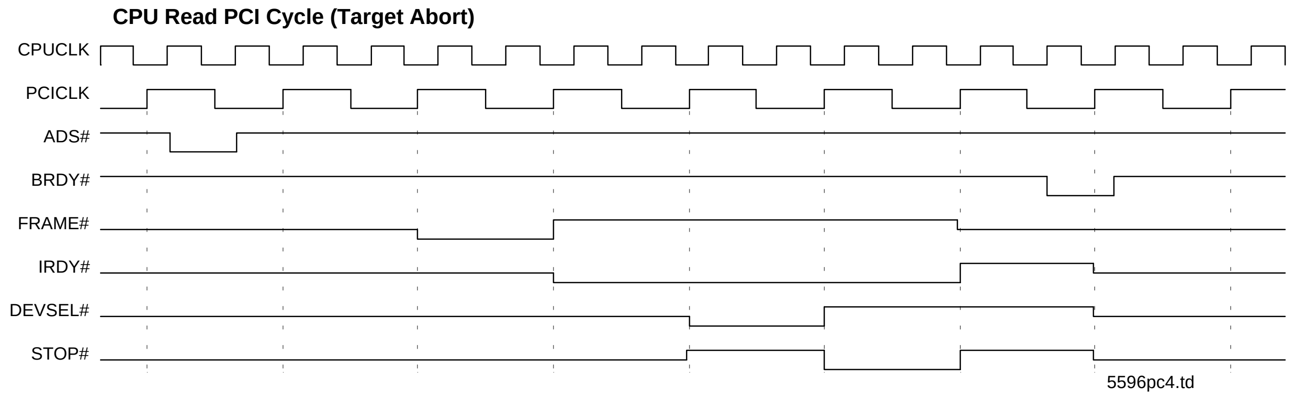


Figure 2.17

CPU Read Boff# Cycle

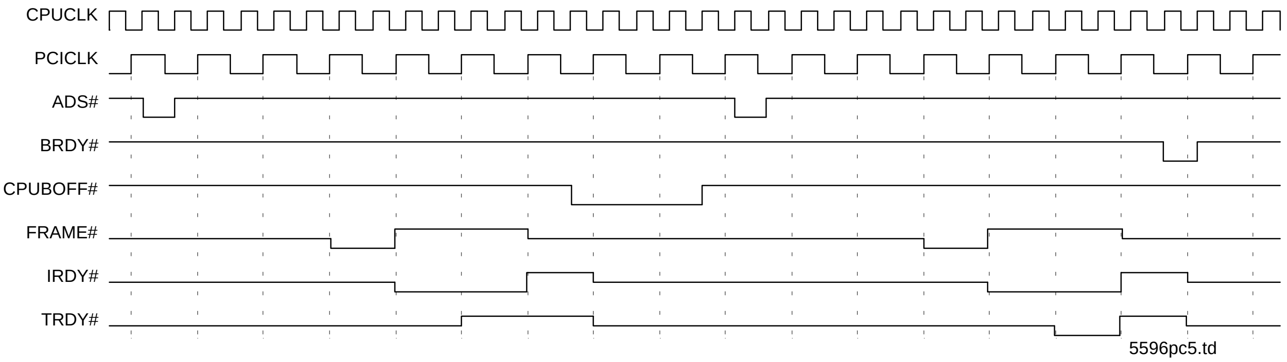


Figure 2.18

CPU Read IDE Cycle

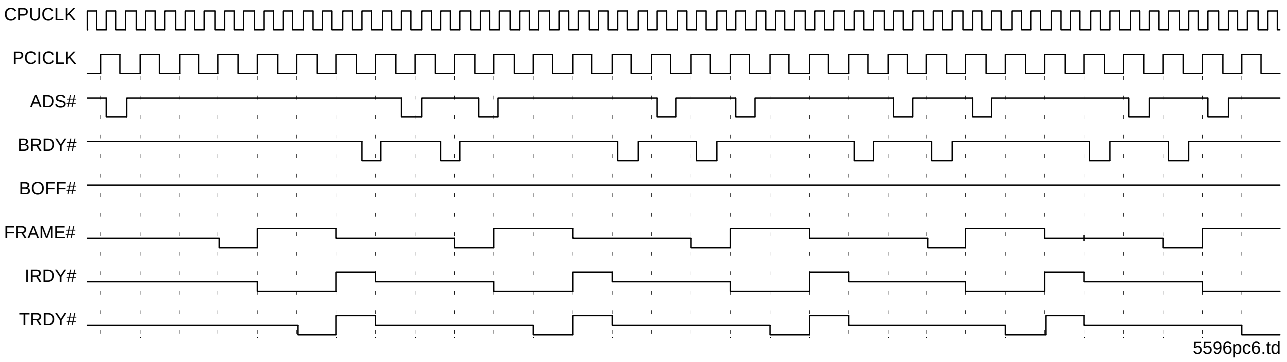


Figure 2.19

PCI Master Read Cycle

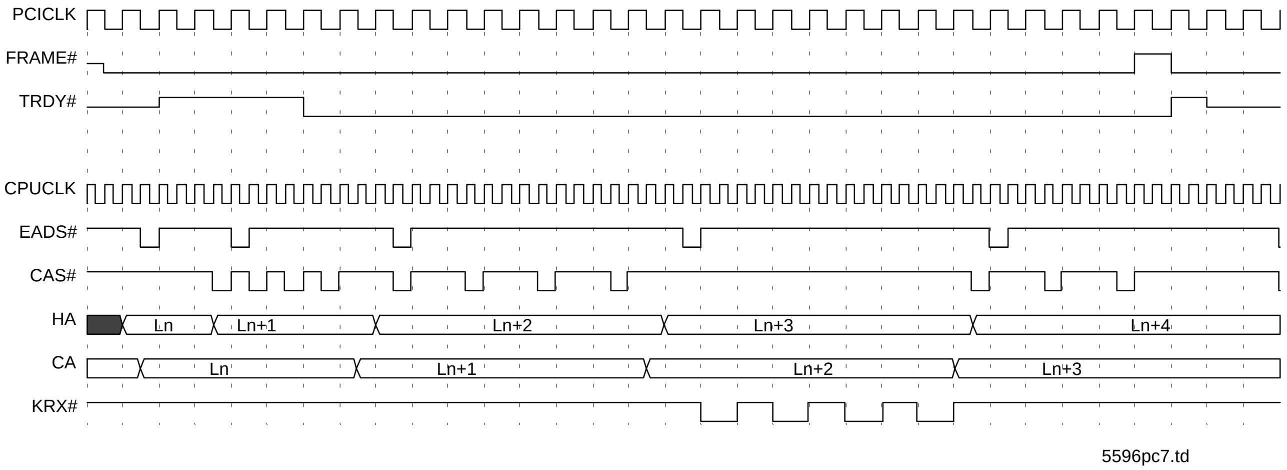


Figure 2.20

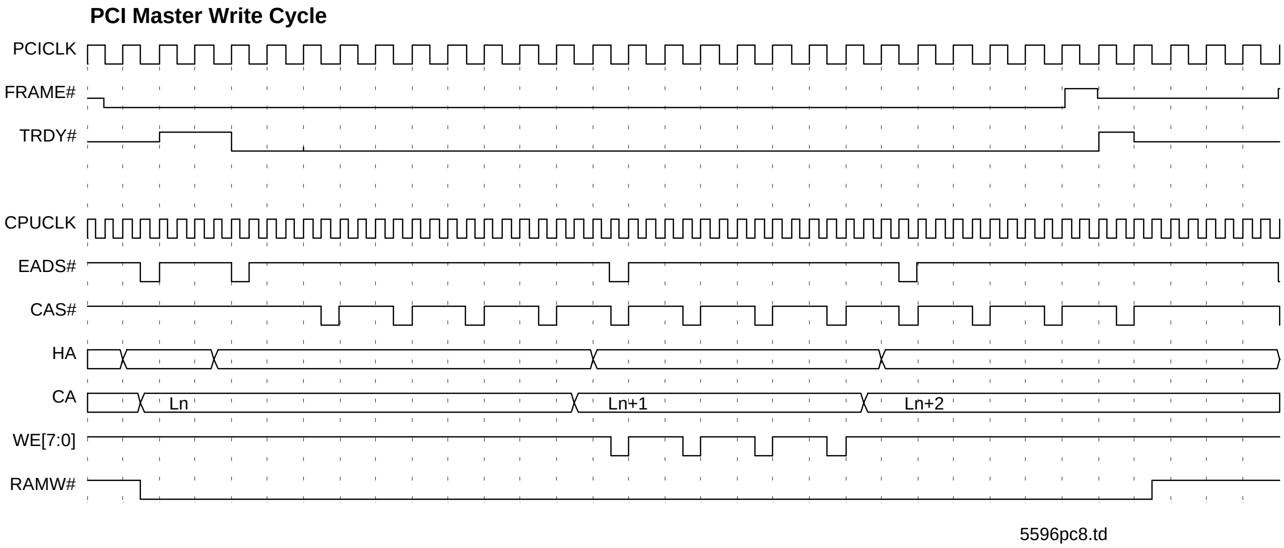

PCI Master Write Cycle
PCICLK
FRAME#
TRDY#
CPUCLK
EADS#
CAS#
HA
CA
Ln
Ln+1
Ln+2
WE[7:0]
RAMW#
5596pc8.td

Figure 2.21

3. Register Description

There are three types of registers in the SiS5596, I/O mapped registers and PCI configuration space registers.

3.1 I/O Mapped Registers

The 5596 uses PCI configuration space access mechanism #1. This mechanism defines two registers, CONFIG_ADDRESS(CF8h) register and CONFIG_DATA(CFCh) register. Both CONFIG_ADDRESS and CONFIG_DATA are read/write registers, and the length is Dword. The mechanism is to write a value into CONFIG_ADDRESS first, then read or write to CONFIG_DATA. The write to CONFIG_ADDRESS specifies the PCI bus, device on that bus, and the configuration register in that device being accessed. The read or write to CONFIG_DATA will cause the host bridge to translate the CONFIG_ADDRESS value to the requested configuration cycle.

The definition of CONFIG_ADDRESS register is described below:

Register 0CF8h CONFIG_ADDRESS Register

31	30 24	23 16	15 11	10 8	7 2	1	0
	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0

Enable bit ('1' = enabled, '0' = disabled)

Bit 31 **is an enable flag for determining if the accesses to CONFIG_DATA should be translated to configuration cycles on the PCI bus.**

Bits 30:24 Reserved, read only, and must return 0's when read.

Bits 23:16 Choose a specific PCI bus in the system.

Bits 15:11 Choose a specific device on the bus.

Bits 10:8 Choose a specific function in a device.

Bits 7:2 Choose a Dword in the device's configuration space.

Bits 1:0 Read only and must return 0's when read.

A full Dword I/O write to address 0CF8h, the host bridge will load the data into CONFIG_ADDRESS register. Also, a full Dword I/O read to 0CF8h, the host bridge gets the data from CONFIG_ADDRESS register. Any non-Dword writes or reads to 0CF8h are treated as normal PCI I/O cycles. When the host bridge of 5596 sees an I/O access that falls inside the Dword beginning at CONFIG_DATA address, it checks the enable bit of the CONFIG_ADDRESS register. If bit 31 of CONFIG_ADDRESS register is 1, the I/O cycle is translated into a configuration cycle.

There are two types of configuration cycle determined by bus number. If the Bus Number is zero, the configuration cycle will be Type 0. If the Bus Number is non-zero, the configuration cycle will be Type 1.

For type 0 configuration cycle, AD[1:0] is driven to "00" during the address phase of the cycle. The host bridge decodes the device number of CONFIG_ADDRESS to assert only one "1" on the AD[31:11] and copies bits[10:2] of CONFIG_ADDRESS to AD[10:2] directly. For instance, when accessing the configuration registers of SiS5596, because SiS5596 is considered device 0 on bus 0, AD11 will be high, and bits[10:2] of CONFIG_ADDRESS are copied to AD[10:2] directly. Never use AD11 as the IDSEL line for any other PCI target device since it is reserved for SiS5596. The 5596 responds to configuration by asserting DEVSEL#.

For type 1 configuration cycle, AD[1:0] is driven to "01" and bits[31:2] of CONFIG_ADDRESS are copied to AD[31:2] directly during the address phase of the cycle.

The byte-enables for the data phase of both types 0 and type 1 configuration cycles are copied from the HBE[7:4]# directly.

The following programming sequences is an example of writing register 51h in SiS5596 and of reading register 5Ch, 5Dh, 5Eh and 5Fh in SiS5596.

write 51h:

```
MOV     EAX, 80000050h
OUT     0CF8h, EAX
MOV     AL, DATA
OUT     0CFDh, AL
```

read 5Ch, 5Dh, 5Eh and 5Fh:

```
MOV     EAX, 8000005Ch
OUT     0CF8h, EAX
IN      0CFCh
```

Register 0CF9h   Turbo and Reset Control Register .

Bits 7:5 Reserved

Bit 4 INIT Enable

When this bit is set to 1 ,the SiS5596 drives INIT during software reset. When this bit is cleared to 0, the SiS5596 drives CPURST during software reset, and INIT is inactive.

Bit 3 BIST

When this bit is set to 1 and bit 4 as well as bit 1 are enabled, a subsequent initiation of the CPU hard reset through bit 2 of this register enables the Built In Self Test(BIST) mode of the CPU. The SiS5596 also drives the INIT during the hard reset.

Bit 2 Reset CPU.

There are two types of resets to the CPU: a hard reset using the CPURST signal and a soft reset using the INIT signal. If bit 1 of this register is set to 1 and bit 2 transitions from 0 to 1, the SiS5596 initiates a hard reset. A hard reset through this register thus requires two write operations to this register: the first write operation writes a 1 to bit 1 and a 0 to bit 2. The second write operation writes a 1 to bit 1 and a 1 to bit 2. When bit 1 of this register is 0 and bit 2 transitions from 0 to 1, the SiS5596 initiates a soft reset. The sequence to initiate a soft reset through this register is identical to that of a hard reset except a 0 is written to bit 1 in the first write operation.

Bit 1 **Enable System Hard Reset.**

When this bit is set to 1 and bit 2 transitions from 0 to 1, the SiS5596 initiates a hard reset to the CPU . When this bit is 0 and bit 2 transitions from 0 to 1, the SiS5596 initiates a soft reset to the CPU.

Bit 0 **Reserved**

3.2 PCI Configuration Space Mapped Registers

Register 00h Vendor ID - low byte

Bits 7:0 **39h**

Register 01h Vendor ID - high byte

Bits 7:0 **10h**

Register 02h Device ID - low byte

Bits 7:0 **96**

Register 03h Device ID - high byte

Bits 7:0 **55h**

Register 04h Command - low byte

Bits 7:0 **07h**

Register 05h Command - high byte

Bits 7:0 **00h**

Register 06h Status - Low Byte

Bits 7:0 **00h**

Register 07h Status - High Byte (default = 02h)

Bit 7 **Detected Parity Error.**

This bit is always 0 since the SiS5596 does not support parity checking on the PCI bus.

Bit 6 **Reserved**

Bit 5 **Received Master Abort.**

This bit is set by the SiS5596 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.

Bit 4 **Received Target Abort.**

This bit is set by the SiS5596 whenever it terminates a transaction with target abort. This bit is cleared by writing a 1 to it.

Bit 3 **Signaled Target Abort.**

This bit is always 0 since the SiS5596 will not terminate a transaction with target abort.

Bits 2:1 **DEVSEL# Timing DEVT.**

The two bits define the timing to assert DEVSEL#. The SiS5596 asserts the DEVSEL# signal within three clocks after the assertion of FRAME#. The default value is DEVT=10. In fact, the SiS5596 always asserts DEVSEL# in medium timing except in CPU writes to I/O port 64h or 60h.

Bit 0 **Reserved**

Register 08h Revision Identification.

Bits 7:0 **00h**

Register 09h~0Bh Class ID

Bits 23:0 **060000h**

Register 0Eh Header Type

Bits 7:0 **00 (Read Only)**

Register 2Ch ~ 2Fh Subsystem ID & Subsystem Vendor ID

Bits 31:0 **00000000h**

3.3 SiS5596 Specific Registers

Register 50h (default = 00h)

Bit 7 **L2 Cache Exist or not**

0: There is no L2 cache

1: L2 cache exists

When this bit is set to 0, no cache cycle occurs. This bit is programmed by BIOS before it processes the cache auto-sizing function, and is disabled after the function has been finished.

Bit 6 **L2 Cache Enable**

0: Disable

1: Enable

When this bit is disabled, all the cache cycles will be cache miss cycles. We can not read data from cache, but the data in cache can still be updated whenever update cycles occur. This makes the data in the L2 cache is always coherent with the data in DRAM. Then, whenever we enable L2 cache, we can get the correct data from cache immediately. This bit is programmed by BIOS when L2 is auto-detected and initialized.

Bits 5:4 **SRAM Type**

00 : Reserved

01 : Reserved
10 : Pipeline Burst SRAM
11 : Reserved

Bit 3 **L2 Cache WT/WB Policy**
0 : Write Through Mode
1 : Write Back Mode

Bits 2:1 **L2 Cache Size**
00: Reserved
01: 256 K Byte
10: 512 K Byte
11: 1M Byte

Bit 0 **CPU L1 Cache Write Back Mode Enable**
0: Disable
1: Enable

Register 51h (default = 00h)

Bits 7:5 **Reserved**

Bit 4 **Synchronous SRAM Leadoff Timing**
0: 3 CPUCLK
1: 4 CPUCLK

Bit 3 **Cache burst Addressing Support**
0: Toggle mode
1: Linear mode

Bit 2 **Cache Tag size Selection**
0: 7 bits(7+1)
1: 8 bits(always dirty)

Bit 1 **Cache Sizing Enable**
0: Normal Operation
1: Always Cache hit regardless the input Tag address
By setting this bit, BIOS can implement L2 cache auto-detection and sizing operation.

Bit 0 **Reserved**

Register 52h (default = 20h)

Bit 7 **Reserved**

Bit 6 **Reserved**
This bit should be programmed to 1.

Bit 5 **FP DRAM CAS Precharge Time**
0: 2 CPUCLK
1: 1 CPUCLK

Bits 4:3 **EDO Cycle CAS Pulse Width, when non-interleave**

	Read	Write	
00	2	2	CPUCLK
01	1	1	CPUCLK
10	1	2	CPUCLK
11	Reserved		

Bit 2 **EDO CAS Precharge Time**
0: 1 CPUCLK
1: 2 CPUCLK

Bit 1 **MDLE Timing when EDO DRAM Is Read (Internal Signal of Data Buffer)**
0: 1 CPUCLK delay from CAS pulse
1: 1.5 CPUCLK delay from CAS pulse

Bit 0 **BRDY# Timing when EDO DRAM Is Read**
0: 1 CPUCLK delay from CAS pulse
1: 2 CPUCLK delay from CAS pulse

Register 53h (default = 00h)

Bits 7:6 **DRAM RAS to CAS Delay Timing**
00: 4 CPUCLK
01: 3 CPUCLK
10: 2 CPUCLK
11: Reserved

Bits 5:4 **DRAM RAS Precharge Timing for FP DRAM**
00: 5 CPUCLK
01: 4 CPUCLK
10: 3 CPUCLK
11: Reserved

Bits 3:2 **RAS Active When Refresh**
00: 6 CPUCLK
01: 5 CPUCLK
10: 4 CPUCLK
11: Reserved

Bit 1 **RAS Precharge Timing for EDO DRAM**
0: 3 CPUCLK
1: 4 CPUCLK

Bit 0 **CAS Output Delay from push HD into CTMFF in DRAM Posted-Write Cycle**
0: 1 CPUCLK
1: 2 CPUCLK

Register 54h (default = 00h)

Bits 7:6 Reserved

Bit 5 This bit must be programmed to 0

Bit 4 RAMW# Power Saving Mode When EDO Bank Is Being Accessed
0: Normal mode
1: Power saving mode

Bit 3 NA# Disable
0: Enable
1: Disable

Bit 2 EDO Test Mode
0: Normal Mode
1: Test Mode
When set, 5596 will delay the assertion of BRDY# by 15us after the negation of CAS#. The EDO test procedure is summarized below:
1. Enable this bit.
2. Write data to DRAM and then read it.
3. If the read data is the same as the write data, EDO type DRAM is used.

Bit 1 This bit must be programmed to 0.

Bit 0 Reserved
This bit should be programmed to 1.

Register 55h (default = 00h)

Bit 7 Slow Refresh Enable (1:4)
0: Disable
1: Enable

Bit 6 Deturbo Enable
0: Disable
1: Enable

Bit 5 KBRST#/BREAK#/LLC1 Selection Bit
0: KBRST#/BREAK# (refer to Register 60h Bit 2)
1: LLC1

Bit 4 This bit should always be programmed to 1.

Bit 3 Selection of Current Rating of RAS[3:0]#
0: 8 mA
1: 12 mA

Bit 2 This bit should always be programmed as 1 to support more than 128M Bytes.

Bits 1:0 Reserved

Register 56h (default = 00h)

Bit 7 **Allocation of Non-Cacheable Area I**
0: Local DRAM
1: PCI Bus. The local DRAM is disabled.

Bit 6 **Non-Cacheable Area I Enable**
0: Disable
1: Enable

Bits 5:3 **Size of Non-Cacheable Area I (within 512 MBytes)**

000	64KB	100	1MB
001	128KB	101	2MB
010	256KB	110	4MB
011	512KB	111	8MB

Bits 2:0 **A26~A24 of Non-Cacheable Area I (within 512 MBytes)**

Register 57h (default = 00h)

Bits 7:0 **A23~A16 of Non-Cacheable Area I (within 512 MBytes)**

Register 58h (default = 00h)

Bit 7 **Allocation of Non-Cacheable Area II**
0: Local DRAM
1: PCI Bus. The local DRAM is disabled.

Bit 6 **Non-Cacheable Area II Enable**
0: Disable
1: Enable

Bits 5:3 **Size of Non-Cacheable Area II**

000	64KB	100	1MB
001	128KB	101	2MB
010	256KB	110	4MB
011	512KB	111	8MB

Bits 2:0 **A26~A24 of Non-Cacheable Area II (within 512 MBytes)**

Register 59h (default = 00h)

Bits 7:0 **A23~A16 of Non-Cacheable Area II (within 512 MBytes)**

Register 5Ah (default = 00h)

Bit 7 **Fast Gate A20 Emulation Enable**
0 : Disable
1 : Enable

The sequence to generate A20M# is: write D1h to I/O port 64h followed by I/O write to port 60h with data 00h. When this bit is enabled, the SiS 5596 responds the cycle by asserting DEVSEL# in slowest timing. Otherwise, the cycle is subtractively decoded by SiS 5513, and then is passed to 8042 on the ISA bus.

Bit 6 **Fast Reset Emulation Enable**

0 : Disable

1 : Enable

The Fast reset command is I/O write to port 64h with data 1111XXX0b.

After the command is issued, the assertion of INIT or CPURST is delayed by 2us or 6us which can be programmed in bit 5, and is held for 25 CPUCLK.

Bit 5 **Fast Reset Latency Control**

0 : 2us

1 : 6us

Bit 4 **Reserved**

Bit 3 **CPU-to-PCI Post Write Rate Control**

0: 4 CPUCLK

1: 3 CPUCLK (recommended)

Bit 2 **Latency from the Disarming of "Full" to the Assertion of BRDY# for the Pending CPU to PCI Write Cycle**

0: 1 CPUCLK (recommended)

1: 2 CPUCLK

Bit 1 **CPU-to-PCI Burst Memory Write Enable**

0: Disable

1: Enable

Bit 0 **CPU-to-PCI Post Memory Write Enable**

0: Disable

1: Enable

Register 5Bh (default = 00h)

Bit 7 **Enable/Disable DRAM refresh cycle in PCI master cycles**

0: Disable

1: Enable

Bits 6:4 **Maximum burstable address range in PCI master accessing main memory.**

When 32-bit DRAM organization is employed with 256K or 512K type DRAM, maximum burstable range reduces to 2KB only because the physical page size is 2KB in this situation. Thus, never program these bits to 100b in 32 bit DRAM organization.

000: 256B

001: 512B

010: 1KB

011: 2KB

100: 4KB

others: reserved

Bit 3 **Reserved**

Bit 2 **TRDY# assertion timing in PCI master read cycle**
0: Assert TRDY# after prefetching two Qws
1: Assert TRDY# after prefetching one Qw

Bit 1 **Enable/Disable advanced snoop in PCI master write cycle**
0:Disable
1:Enable

Bit 0 **Enable/Disable advanced snoop in PCI master read cycle**
0:Disable
1:Enable

Register 5Ch Default=00h

Bit 7 **Enable/Disable CPU to L2/DRAM and PCI peer-to-peer concurrency mode**
0: Disable
1: Enable

Bit 6 **This bit should always be programmed to Logic 0.**

Bit 5 **Reserved**

Bit 4 **This bit should be set to 1 to meet PCI Spe. Ver 2.1.**

Bit 3 **Push MD to Internal Data Buffer timing control in PCI master reading EDO DRAM.**
0: 1 CPUCLK delay from the assertion of CAS#(recommended in 50MHz)
1: 2 CPUCLK delay from the assertion of CAS#(recommended in 60/66MHz)

Bit 2 **Pshmd of HCR[3:0] timing control in PCI master reading FP DRAM**
0: 1 CPUCLK delay from the assertion of CAS#(recommended in 50MHz)
1: 2 CPUCLK delay from the assertion of CAS#(recommended in 60/66MHz)

Bit 1 **Retiring rate from Internal Data Buffer to EDO in PCI master write cycle**
0: 3 CPUCLK(Recommended)
1: 2 CPUCLK

Bit 0 **Prefetching rate from EDO DRAM in PCI master read cycle**
0: 3 CPUCLK
1: 2 CPUCLK (Recommended)

Register 5Dh (default = 00h)

Bit 7:5 **Reserved**

Bit 4 **Selection of CAS[7:0]# Buffer Strength**
This bit is recommended to be programmed to 1, when 3.3 V DRAM is employed, so that 5596 can provide higher buffer strength.

Bit 3 **Selection of Current Rating of CAS[7:0]#**
0: 4 mA
1: 8 mA

Bit 2 **Selection of MA[11:0]# Buffer Strength**
0: 5V (for 5V DRAM)

1: 3.3V (for 3.3V DRAM)

Bit 1 **Reserved**

Bit 0 **Selection of RAS[3:0]# Buffer Strength**

This bit is recommended to be programmed to 1, when 3.3 V DRAM is employed, so that 5596 can provide higher buffer strength.

Register 5Eh (default = 00h)

This register mainly defines the enable bits for the events monitored by System Standby timer. If any monitored event occurs during the programmed time, the System standby timer will be reloaded and starts to count down again.

Bit 7 **Programmable 10 bit I/O Port Enable**

When set, any I/O access to the address will cause the timer be reloaded. The address is defined in Registers 66h and 67h.

Bit 6 **Programmable 16 bit I/O Port Enable**

When set, any I/O access to the address will cause the timer be reloaded. The address is defined in Registers 6Dh and 6Eh.

Bit 5 **Hard Disk Port Enable**

When set, any I/O access to the Hard Disk ports (1F0-1F7h or 3F6h) will cause the timer be reloaded.

Bit 4 **Serial Port Enable**

When set, any I/O access to the Serial Ports (2F8-2FFh, 3F8-3FFh, 2E8-2EFh or 3E8-3EFh) will cause the timer be reloaded.

Bit 3 **Parallel Port Enable**

When set, any I/O access to the Parallel ports (278-27Fh, 378-37Fh or 3BC-3BEh) will cause the timer be reloaded.

Bit 2 **Hold Enable**

When set, any event from the ISA master or the PCI Local Master will cause the timer be reloaded.

Bit 1 **IRQ1~15, NMI**

When set, any event from the IRQ1-15 or NMI will cause the timer be reloaded.

Bit 0 **Reserved**

Register 5Fh (default = 00h)

Bits 7:6 **Define the events monitored by the Monitor standby timer**

Bits 5:0 **Define the events to break the Monitor and System standby state.**

Bit 7 **IRQ 1-15, NMI**

When set, any event from the IRQ1-15 or NMI will cause the Monitor standby timer be reloaded.

Bit 6 **HOLD**

When set, any event from the ISA master or the PCI local master will cause the Monitor standby timer be reloaded.

Bit 5 **IRQ 1-15, NMI**

When enabled, any event from the IRQ1-15 or NMI will bring the Monitor back to the Normal state from the Standby state.

Bit 4 **HOLD**

When enabled, any event from the ISA master or the PCI local master will bring the Monitor back to the Normal state from the Standby state.

Bit 3 **IRQ 1-15, NMI**

When enabled, any event from the IRQ1-15 or NMI will de-assert the STPCLK#.

Bit 2 **HOLD**

When enabled, any event from the ISA master or the PCI local master will de-assert the STPCLK#.

Bit 1 **INIT**

When enabled, an event from the INIT will de-assert the STPCLK#.

Bit 0 **Reserved (must be '0')**

Register 60h (default = 00h)

Bit 7 **Reserved. It should be written with 0.**

Bit 6 **Reserved. It should be written with 0.**

Bit 5 **STPCLK# Enable**

When set, writing a '1' to bit 3 of Register 60h will cause the STPCLK# to become active. This bit can be cleared.

Bit 4 **Throttling Enable**

When set, writing a '1' to bit 3 of Register 60h will cause the STPCLK# throttling state to become active. The throttling function can be disabled by clearing this bit.

Bit 3 **STPCLK# Control**

When this bit is set, the STPCLK# will be asserted or the Throttling function will be enabled depending on bits 5 and 4. If both bits 5 and 4 are enabled, the system will do the throttling function.

Bit 2 **Break SW., Keyboard reset selection**

0: KBRST #

1: BREAK#

The Break SW. disable function can be done by programming register 68 bit 1 to "0".

Bit 1 **APM SMI**

When Register 68h bit 0 is enabled, and a '1' is written to this bit, an SMI is generated. It is used by the software controlled SMI function like APM. This bit should be cleared at the end of the SMI handler.

Bit 0 **Reserved.**

Register 61 STPCLK# Assertion Timer (default = FFh)

Bits 7:0 **This register defines the period of the STPCLK# assertion time.**

Bits[7:0] define the period of the STPCLK# assertion time when the STPCLK# enable bit is set. The timer will not start to count until the Stop Grant Special Cycle is received. The timer slot is 35 us.

Register 62 STPCLK# De-assertion Timer (default = FFh)

Bits 7:0 This register defines the period of the STPCLK# de-assertion time.

Bits[7:0] define the period of the STPCLK# de-assertion time when the STPCLK# enable bit is set. The timer starts to count when the STPCLK# assertion timer expires. The timer slot is 35us.

When these two registers are read, the current values are returned.

Register 63h System Standby Timer (default = FFh)

Bits 7:0 The register defines the duration of the System Standby Timer.

When the System Standby Timer expires, the system enters System Standby State. If any non-masked event occurs before the timer expires, the timer is reloaded with programmed number and the timer starts counting down again.

Register 64h (default = 00h)

Bit 7 M1 SMAC access

It must be set whenever the M1 CCR1 bit 2 is set and cleared if CCR1 bit 3 is cleared.

Bit 6 M1 MMAC access

If set, access to address within SMM space is conducted to main memory instead of SMM area. It must be set whenever the M1 CCR1 bit 3 is set and cleared if CCR1 bit 3 is cleared.

In the M1's specification, the SMIACT will be de-asserted when MMAC is set and re-asserted after it is cleared. This allows the SMI service routine to access normal memory area instead of SMM memory area.

Bit 5 M1 CPU

It should be set if the current CPU is M1.

Bit 4 Toggle Mode Enable

0: Break SW. without toggle mode

1: Break SW. with toggle mode

Bit 3 Flush Function Block Mode

It is suggested to block the FLUSH (Deturbo Mode) when the STPCLK is asserted.

0: Un-block

1: Block

Bit 2 SMOUT0 Control

When this bit is set to "1", the SMOUT is asserted low. Otherwise, it should be tri-state. In order to keep high, it has to be pulled up by a 10K ohm resistor.

Bit 1 WAKEUP0, TURBO Selection

0: WAKEUP0

1: TURBO

Bit 0 SMOUT0, INTA# Selection

0: INTA#

1: SMOUT0

Register 65h (default = 00h)

Bits 7:6 SMRAM Area Selection

	Logic Address	**Physical address**
00	E0000h ~ E7FFFh	E0000h ~ E7FFFh
01	E0000h ~ E7FFFh	B0000h ~ B7FFFh
10	E0000h ~ E7FFFh	A0000h ~ A7FFFh
11	A0000h ~ AFFFFh	A0000h ~ AFFFFh

Bit 5 Reserved

Bit 4 SMRAM Access Control

1: When set, the SMRAM area can be used. This bit can be set whenever it is necessary to access the SMRAM area. It is cleared after the access is finished.

0: The SMRAM area can only be accessed during the SMI handler.

Bits 3:0 Reserved

Register 66h (default = 00h)

Bit 7 Reserved

Bits 6:5 Define the time slot of the Monitor Standby timer

00 : 6.6 seconds
01 : 0.84 seconds
10 : 13.3 milli-seconds
11 : 1.6 milli-seconds

Bits 4:2 Programmable 10-bit I/O port address mask bits

000 : No mask
001 : A0 masked
010 : A1-A0 masked
011 : A2-A0 masked
100 : A3-A0 masked
101 : A4-A0 masked
110 : A5-A0 masked
111 : A6-A0 masked

Bits 1:0 Programmable 10-bit I/O port address bits A1, A0.

Bits 1:0 correspond to the address bits A1 and A0.

Register 67h (default = FFh)

Bits 7:0

Bits 7:0 define the programmable 10-bit I/O port address bits A[9:2].

Register 68h (default = 00h)

This register defines the enable status of the devices in SMM. The bits 6:2 are set when the devices are in standby state and cleared when the respective devices are in normal state.

Bit 7 System Standby SMI enable

When no non-masked event occurs during the programmed duration of the system standby timer, the timer expires. If this bit is enabled, the SMI# is generated and the system enters the System Standby state.

Bit 6 Programmable 10-bit I/O port wake up SMI enable

When set, any I/O access to this port will be monitored to generate the SMI# to wake up this I/O port from the standby state to the Normal state. This bit is enabled only when the I/O port is in the Standby state.

Bit 5 Programmable 16-bit I/O port wake up SMI enable

When set, any I/O access to this port will be monitored to generate the SMI# to wake up this I/O port from the standby state to the Normal state. This bit is enabled only when the I/O port is in the Standby state.

Bit 4 Serial ports wake up SMI enable

When set, any I/O access to the serial ports will be monitored to generate the SMI# to wake up the serial ports from the standby state to the Normal state. This bit is enabled only when the serial ports are in the Standby state.

Bit 3 Parallel ports wake up SMI enable

When set, any I/O access to the parallel ports will be monitored to generate the SMI# to wake up the parallel ports from the standby state to the Normal state. This bit is enabled only when the parallel ports are in the Standby state.

Bit 2 Hard Disk port SMI enable

When set, any I/O access to the hard disk port will be monitored to generate the SMI# to wake up the hard disk from the standby state to the Normal state. This bit is enabled only when the hard disk port is in the Standby state.

Bit 1 Break Switch SMI enable

When set, the break switch can be pressed to generate the SMI# for the system to enter the Standby state.

Bit 0 Software SMI enable

When set, an I/O write to register 60h bit 1 will generate an SMI.

Register 69h (default = 00h)

This register defines the SMI request status. If the respective SMI enable bit is set, each specific event will cause the respective bit to be set. The asserted bit should be cleared at the end of the SMI handler.

Bit 7 System Standby SMI request

This bit is set when the system standby timer expires.

Bit 6 Programmable 10-bit I/O port wake up request

This bit is set when there is an I/O access to the port.

Bit 5 Programmable 16-bit I/O port wake up request

This bit is set when there is an I/O access to the port.

Bit 4 Serial ports wake up request

This bit is set when the serial ports are accessed.

Bit 3 Parallel ports wake up request

This bit is set when the parallel ports are accessed.

Bit 2 **Hard Disk port wake up request**
This bit is set when the hard disk port is accessed.

Bit 1 **Break Switch SMI request**
This bit is set when the break switch is pressed.

Bit 0 **Software SMI request**
This bit is set when an I/O write to the bit 1 of register 60h.

Register 6Ah (default = 00h)

Bit 7 **Monitor Standby SMI enable**
0 : Disable
1 : Enable
When there is no access from the IRQ1-15, HOLD and NMI during the programmed time of the Monitor Standby Timer, the timer expires. If this bit is set, an SMI is generated to bring the Monitor to the standby state.

Bit 6 **Monitor Standby SMI request**
This bit is set when the Monitor Standby Timer expires. This bit should be cleared at the end of the SMI handler.

Bit 5 **Monitor wake up SMI enable**
When set, any event from the IRQ1-15, HOLD or NMI will be monitored to generate the SMI# to wake up the monitor from the standby state to the normal state.

Bit 4 **Monitor wake up request**
This bit is set when there is an event from the IRQ1-15, HOLD or NMI, and the Monitor is in the standby state.

Bit 3 **Throttling wake up SMI request**
This bit is set when there is any unmasked event from the NMI, INIT, IRQ1-15, or HOLD when the system is in the throttling state.

Bit 2 **Throttling wake up SMI enable**
When set, any unmasked event from the NMI, INIT, IRQ1-15, or HOLD will cause an SMI to be generated to bring the system back to the Normal state from the throttling state.

Bit 1 **System wake up SMI enable**
When set, any unmasked event from the NMI, INIT, IRQ1-15, or HOLD will cause an SMI to be generated to bring the system back to the Normal state from the standby state.

Bit 0 **System wake up SMI request**
This bit is set when there is any unmasked event from the NMI, INIT, IRQ1-15, or HOLD when the system is in the standby state.

Register 6Bh Monitor Standby timer - Low byte (default = FFh)

Bits 7:0 **Bits 7:0 define the low byte of the Monitor standby timer.**

It is a count-down timer and the time slot is programmable for 6.6s, 0.84s, 13.3 ms or 1.6ms. The value programmed to this register is loaded when the timer is enabled and the timer starts counting down. The timer is reloaded when an event from the IRQ1-15, HOLD or NMI occurs before the timer expires. When this register is read, the current value is returned.

Register 6Ch Monitor Standby timer - High byte (default = FFh)

Bits 7:0 **Bits 7:0 define the high byte of the Monitor standby timer.**

Register 6Dh Programmable 16-bit I/O port - Low byte (default = FFh)

Bits 7:0 **Bits 7:0 define the low byte of the Programmable 16-bit I/O port.**

Register 6Eh Programmable 16-bit I/O port - High byte (default = FFh)

Bits 7:0 **Bits 7:0 define the high byte of the Programmable 16-bit I/O port.**

Register 6Fh (default = 00h)

This register except bits 6, 7 mainly defines the events monitored by the System Standby timer. If any unmasked event occurs before the timer expires, the System Standby Timer will be reloaded and the timer starts to count down again.

Bit 7 **Enable Wakeup1 as SMI# Input from SIO (5513C)**

0: Disable

1: Enable

Bit 6 **Wakeup1 as SMI# Input Status (5513C)**

This bit is setted when there is a SMI# from SIO.

Bit 5 **A0000h - AFFFFh or B0000 - BFFFFh Address trap**

When set, any memory access to the address range will cause the timer to be reloaded.

Bit 4 **C0000h - C7FFFh Address trap**

When set, any memory access to the address range will cause the timer to be reloaded.

Bit 3 **3B0-3BFh, 3C0-3CFh, 3D0-3DFh Address trap**

When set, any I/O access to the I/O addresses will cause the timer to be reloaded.

Bit 2 **Secondary Drive port**

When set, any I/O access to the secondary drive port (170-17Fh, 320-32Fh, 3F7h) will reload the system standby timer.

Bits 1:0 **System Standby Timer Slot**

11 : 8.85 milli seconds

10 : 70 milli seconds

01 : 1.1 seconds

00 : 9 seconds

Register 70h DRAM Bank Register 0-0(*) (default = 04h)

NOTE: *means DRAM Bank Register x-y, where x=0, 1, 2, or 3 stand for bank x.

Bits 7:0 **DRAM Boundary Address HA[28:21]**

00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Register 71h DRAM Bank Register 0-0 (default = 00h)

Bits 7:2 Define the characteristics of Bank 0

Bit 7 Half populated Bank for the first BANK 0
0: Full Populated Bank (64 Bits Data)
1: Half Populated Bank (32 Bits Data)

Bit 6 FP DRAM / EDO DRAM setting
0: FP DRAM
1: EDO DRAM

Bit 5 Reserved

Bits 4:2 DRAM type setting
000: 1M x N Symmetric DRAM
001: 512K x N 4 Asymmetric DRAM
010: 4M x N Symmetric DRAM
011: 2M x N Asymmetric DRAM (11x10)
100: 4M x N Asymmetric DRAM (12x10)
101: 256K x N Symmetric DRAM
110: 16M x N Symmetric DRAM
111: 1MxN Asymmetric DRAM

Bits 1:0 DRAM Boundary Address HA[30:29]

Register 72h DRAM Bank Register 0-1 (default = 04h)

Bits 7:0 DRAM Boundary Address HA[28:21]
00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Register 73h DRAM Bank register 0-1 (default = 80h)

Bit 7 **This bit is set when RAS0 is populated.**

Bit 6:5 **Reserved**

Bits 4:3 **DRAM type setting of BANK 0**
10: 1MxN asymmetric DRAM (12 X 8)
11: 2MxN asymmetric DRAM (12 X 9)
00, 01 reserved

Bit 2 **Reserved**

Bits 1:0 **DRAM Boundary Address HA[30:29]**

Register 74h DRAM Bank Register 1-0 (default = 04h)

Bits 7:0 **DRAM Boundary Address HA[28:21]**
00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Register 75h DRAM Bank Register 1-0 (default = 00h)

Bit 7 **Half populated Bank for BANK 1**
0: Disable
1: Enable

Bit 6 **FP DRAM / EDO DRAM setting**
0: FP DRAM
1: EDO DRAM

Bit 5 **Reserved**

Bits 4:2 **DRAM type setting**
000: 1M x N Symmetric DRAM
001: 512K x N Asymmetric DRAM
010: 4M x N Symmetric DRAM
011: 2M x N Asymmetric DRAM (11x10)
100: 4M x N Asymmetric DRAM (12x10)
101: 256K x N Symmetric DRAM
110: 16M x N Symmetric DRAM
111: 1MxN Asymmetric DRAM

Bits 1:0 **DRAM Boundary Address HA[30:29]**

Register 76h DRAM Bank Register 1-1 (default = 04h)

Bits 7:0 **DRAM Boundary Address HA[28:21]**
00h: 0MByte

01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Register 77h DRAM bank Register 1-1 (default = 80h)

Bit 7 **This bit is set when RAS2 is populated.**

Bits 6:5 **Reserved**

Bit 4:3 **DRAM type setting**
10: Asymmetric 12 X 8
11: Asymmetric 12 X 9
00, 01: reserved

Bit 2 **Reserved**

Bits 1:0 **DRAM Boundary Address HA[30:29]**

Register 78h DRAM Bank Register 2-0 (default = 04h)

Bits 7:6 **DRAM Boundary Address HA[28:21]**
00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Bits 5:3 **DRAM type setting**
010: Asymmetric 12 X 8
011: Asymmetric 12 X 9
000: 001, 100, 101, 110, 111 reserved

Bit 2 **Reserved**

Bits 1:0 **DRAM Boundary Address HA[28:21]**
00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte

40h: 128MByte
80h: 256MByte

Register 79h DRAM Bank Register 2-0 (default = 00h)

Bit 7 **Half populated Bank for BANK 2**
0: Disable
1: Enable

Bit 6 **FP DRAM / EDO DRAM setting**
0: FP DRAM
1: EDO DRAM

Bit 5 **Reserved**

Bits 4:2 **DRAM type setting**
000: 1M x N Symmetric DRAM
001: 512K x N Asymmetric DRAM
010: 4M x N Symmetric DRAM
011: 2M x N Asymmetric DRAM (11x10)
100: 4M x N Asymmetric DRAM (12x10)
101: 256K x N Symmetric DRAM
110: 16M x N Symmetric DRAM
111: 1MxN Asymmetric DRAM

Bits 1:0 **DRAM Boundary Address HA[30:29]**

Register 7Ah DRAM Bank Register 2-1 (default = 04h)

Bits 7:0 **DRAM Boundary Address HA[28:21]**
00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Register 7Bh DRAM Bank Register 2-1 (default = 80h)

Bit 7 **This bit is set when RAS1 is populated.**

Bit 6:5 **Reserved**

Bits 4:3 **DRAM type setting**
10: Asymmetric 12 X 8
11: Asymmetric 12 X 9
00, 01: reserved

Bit 2 **Reserved**
0: Non-exist

1: Exist

Bits 1:0 DRAM Boundary Address HA[30:29]

Register 7Ch DRAM Bank Register 3-0 (default = 04h)

Bits 7:0 DRAM Boundary Address HA[28:21]

00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte
40h: 128MByte
80h: 256MByte

Register 7Dh DRAM Bank Register 3-0 (default = 00h)

Bit 7 Half populated Bank for BANK 3

0: Disable
1: Enable

Bit 6 FP DRAM / EDO DRAM setting

0: FP DRAM
1: EDO DRAM

Bit 5 Reserved

Bits 4:2 DRAM type setting

000: 1M x N Symmetric DRAM
001: 512K x N Asymmetric DRAM
010: 4M x N Symmetric DRAM
011: 2M x N Asymmetric DRAM (11x10)
100: 4M x N Asymmetric DRAM (12x10)
101: 256K x N Symmetric DRAM
110: 16M x N Symmetric DRAM
111: 1MxN Asymmetric DRAM

Bits 1:0 DRAM Boundary Address HA[30:29]

Register 7Eh DRAM Bank Register 3-1 (default = 04h)

Bits 7:0 DRAM Boundary Address HA[28:21]

00h: 0MByte
01h: 2MByte
02h: 4MByte
04h: 8MByte
08h: 16MByte
10h: 32MByte
20h: 64MByte

40h: 128MByte
80h: 256MByte

Register 7Fh DRAM Bank Register 3-1 (default = 80h)

Bit 7 **This bit is set when RAS3 is populated.**

Bits 6:5 **Reserved**

Bits 4:3 **DRAM type setting**
10: Asymmetric 12 X 8
11: Asymmetric 12 X 9
00, 01: reserved

Bit 2 **Reserved**

Bits 1:0 **DRAM Boundary Address HA[30:29]**

(Register 80h to register 86h define the attribute of the Shadow RAM from 640 KByte to 1 MByte. All of the registers 80h to 85h are defined as below, and each register defines the corresponding memory segment's attribute which are listed in the following table.)

Registers 80h (default = 00h)

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **This bit should always be programmed as 1 to support more than 512M Bytes.**

Bit 3 **Read enable**

Bit 2 **L1/L2 cacheable**

Bit 1 **Write enable**

Bit 0 **This bit should always be programmed as 1 to support more than 512M Bytes.**

Register	**Defined Range**	**Register**	**Defined Range**
register 80h bits 7:5	0C0000h-0C3FFFh	register 83h bits 7:5	0D8000h-0DBFFFh
register 80h bits 3:1	0C4000h-0C7FFFh	register 83h bits 3:1	0DC000h-0DFFFFh
register 81h bits 7:5	0C8000h-0CBFFFh	register 84h bits 7:5	0E0000h-0E3FFFh
register 81h bits 3:1	0CC000h-0CFFFFh	register 84h bits 3:1	0E4000h-0E7FFFh
register 82h bits 7:5	0D0000h-0D3FFFh	register 85h bits 7:5	0E8000h-0EBFFFh
register 82h bits 3:1	0D4000h-0D7FFFh	register 85h bits 3:1	0EC000h-0EFFFFh

Registers 81h (default = 00h)

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **Reserved**

Bit 3 **Read enable**

Bit 2 **L1/L2 cacheable**

Bit 1 **Write enable**

Bit 0 **Reserved**

Registers 82h (default = 00h)

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **Reserved**

Bit 3 **Read enable**

Bit 2 **L1/L2 cacheable**

Bit 1 **Write enable**

Bit 0 **This bit should be programmed to 1.**

Registers 83h (default = 00h)

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **Reserved**

Bit 3 **Read enable**

Bit 2 **L1/L2 cacheable**

Bit 1 **Write enable**

Bit 0 **Pipeline Burst SRAM with back to back 3-1-1-1-1-1....**
0: Disable, but 3-1-1-1-2-1-1-1...
1: Enable

Register 84h

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **Reserved**

Bit 3 **Read enable**

Bit 2 **L1/L2 cacheable**

Bit 1 **Write enable**

Bit 0 **Internal 2-wire/3-wire priority support**
0: 2-wire
1: 3-wire

Registers 85h (default = 00h)

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **Reserved**

Bit 3 **Read enable**

Bit 2 **L1/L2 cacheable**

Bit 1 **Write enable**

Bit 0 **Reserved**

Register 86h (default = 00h)

Bits 7:4 define the attributes of BIOS area 0F0000-0FFFFFh

Bit 7 **Read enable**

Bit 6 **L1/L2 cacheable**

Bit 5 **Write enable**

Bit 4 **Reserved**

Bit 3 **Shadow RAM enable for PCI master access**
0: Disable
1: Enable

Bits 2:1 **Reserved**

Bit 0 **This bit should be currently programmed to 0. When set, the hidden refresh cycle would be conducted to some extent in the sense of availing the duration of L2 accessing to perform refresh cycles more heuristically.**

Register 88h (R/W): DBR7~0's DRAM Boundary Register Address (DBA) HA[20]

Bit 7 **DRAM Bank Register 3-1**

Bit 6 **DRAM Bank Register 3-0**

Bit 5 **DRAM Bank Register 2-1**

Bit 4 **DRAM Bank Register 2-0**

Bit 3 **DRAM Bank Register 1-1**

Bit 2 **DRAM Bank Register 1-0**

Bit 1 **DRAM Bank Register 0-1**

Bit 0 **DRAM Bank Register 0-0**
NOTE: This register must be used together with Register 70h, 72h, 74h, 76h, 78h, 7Ah, 7Ch, 7Eh.

Register 89h (R/W): CPU Interface Register

Bit 7 **This bit should be set to 1 to meet PCI Spec. Ver 2.1.**

Bits 6:4 **Reserved**

Bits 3:1 **Shared memory size**
000: 1M
001: 0.5M
010: 1.5M

011: 2M
100: 2.5M
101: 3M
110: 3.5M
111: 4M

Bit 0 **Shared memory mode**
0: Disable
1: Enable

Register 8E BANK's bottom address HA[27:21] of VGA used share memory

Bit 7 **Reserved**

Bits 6:0 **HA[27:21]**

Register 93 (R/W): Internal Data Buffer Delay Adjustment Register

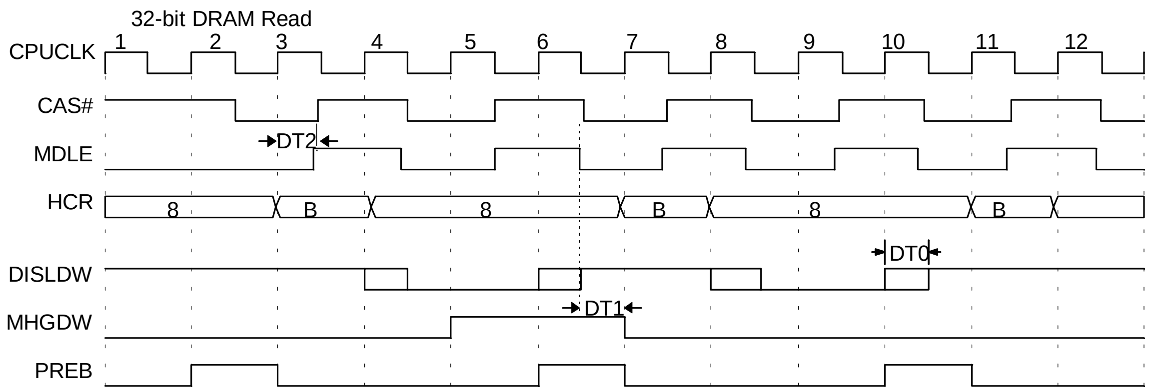
Bits 7:4 As in **Figure 3.1**, MHGDW (memory high double word switch, asserted high) is a controlled signal to switch high/low double word of 32-bit DRAM bank. Those bits are "don't care at 64-bit Bank". It controls DRAM's low double word switch to high double word at write DRAM in 32-bit DRAM bank. Because it can't control asserted CAS# delay which changes by loading capacitances, it use those bits to adjust the better position to switch low/high double word. Default value is 0111 about 7 ns. (DT0)

0000 : No delay	1000 : delay 8 ns
0001 : delay 1 ns	1001 : delay 9 ns
0010 : delay 2 ns	1010 : delay 10 ns
0011 : delay 3 ns	1011 : delay 11 ns
0100 : delay 4 ns	1100 : delay 12 ns
0101 : delay 5 ns	1101 : delay 13 ns
0110 : delay 6 ns	1110 : delay 14 ns
0111 : delay 7 ns	1111 : delay 15 ns

Bits 3:0 In 32-bit accessing, the 64 bit latch is further divided into two 32 bit ones. The timing control of the two latch is controlled by the MDLE and the HCR[3:0] as Figure 3.1 shows. Whenever internal data buffer samples the code B on HCR[3:0], the internal signal Disable Low Double Word(DISLDW) is asserted on that CPUCLK rising edge and is lasted until the CPUCLK rising edge that the immediately next MDLE is sampled to be active. Logically, the enable of the low DW is controlled by MDLE * DISLDW while that of the high DW is MDLE * DISLDW. Due to the possible racing on MDLE and DISLDW, an extra programmable delay is inserted between the MDLE and DISLDW. The

programmable delay can be as the following shows. It is recommend to program 0111 about 7 ns. (DT1)

0000 : No delay	1000 : delay 8 ns
0001 : delay 1 ns	1001 : delay 9 ns
0010 : delay 2 ns	1010 : delay 10 ns
0011 : delay 3 ns	1011 : delay 11 ns
0100 : delay 4 ns	1100 : delay 12 ns
0101 : delay 5 ns	1101 : delay 13 ns
0110 : delay 6 ns	1110 : delay 14 ns
0111 : delay 7 ns	1111 : delay 15 ns



Note: DISLDW, MDLE, HCR, MHGDW, PREB are internal signals.

Figure 3.1

Register 0A0h (R/W): DRAM Boundary Register (DBR) Resolution Selection

Bits 7:0 **DRAM Boundary Address A19**
This register defines the resolution of DBRs down to 512K byte.

Bit 7 **DRAM Bank Register 3-1**

Bit 6 **DRAM Bank Register 3-0**

Bit 5 **DRAM Bank Register 2-1**

Bit 4 **DRAM Bank Register 2-0**

Bit 3 **DRAM Bank Register 1-1**

Bit 2 **DRAM Bank Register 1-0**

Bit 1 **DRAM Bank Register 0-1**

Bit 0 **DRAM Bank Register 0-0**

Register 0A1h (R/W): GUI Interface Register

Bits 7:6 **Reserved.**

Bit 5 **Reserved**

Bits 4:2 **The bank corresponding to the share memory.**

000: Bank 0-0
001: Bank 0-1
010: Bank 1-0
011: Bank 1-1
100: Bank 2-0
101: Bank 2-1
110: Bank 3-0
111: Bank 3-1

Bit 1 **Data Always-page-miss enable**
0: Disable
1: Enable

Bit 0 **Code Always-page-miss enable**
0: Disable
1: Enable

Register 0A2h (R/W): Direct Access Register

This register defines the address range that allows the CPU to directly access shared memory without going through the PCI bus.

Bits 7:3 **These bits define the direct access address of A23-A19.**

Bit 2 **Direct access area read enable.**

Bit 1 **Direct access area write enable.**

Bit 0 **Direct access area PCI master access Disable. (Default enable)**

Register 0A3h (R/W): Direct Access Register

Bits 7:0 **Define shared memory hole area A31~A24**
NOTE: Shared memory hole concept
When CPU accesses off-board DRAM, it will be forwarded to PCI side then write to or read from shared memory area data through VGA chip. If we define a shared memory hole area , any logical area, we can access the shared memory area by remapping the logical area to physical area of the shared memory through system chip. We can save some time wasted on PCI bus.

Register A4h (R/W): Default 00h

Bit 7:0 **Reserved**

Register A5h (R/W): Default is 00h

Bits 7:1 **Reserved**

Bit 0 **DRAM Leadoff Timing.**
This bit controls the leadoff cycle time to 5/6 CPUCLKs in serving FP/EDO.

0: 6 CPUCLKs for FP(EDO)
1: 5 CPUCLKs for FP(EDO)

Register A6h (R/W): Default is 00h

Bits 7:4 **Reserved**

Bits 3:0 **MDLE Timing Adjustment.**

These bits are used to set the delay time from the rising edge of the 3rd CPUCLK to internal MDLE (Memory data latch signal of internal data buffer) as describing in Figure 3.1.(DT2)

0000 : No delay	1000 : delay 8ns
0001 : delay 1ns	1001 : delay 9ns
0010 : delay 2ns	1010 : delay 10ns
0011 : delay 3ns	1011 : delay 11ns
0100 : delay 4ns	1100 : delay 12ns
0101 : delay 5ns	1101 : delay 13ns
0110 : delay 6ns	1110 : delay 14ns
0111 : delay 7ns	1111 : delay 15ns

Register A7h (R/W): Default is 00h

Bit 7 **Currently this bit should be programmed with 0.**

When set, the 5596 timing is adjusted to serve those bus master agents that do not follow the PCI specification to have 12 ns max. propagation delay time of AD in the address phase.

Bit 6 **Reserved**

Bit 5 **SMOUT1 control (refer to Register 64h bit 2 SMOUT0 Control)**

Bit 6 **FLUSH/SMOUT1 Selection**

0: FLUSH (default)
1: SMOUT1

Bits 3:2 **A28~A27 of Non-Cacheable Area II (within 512 MBytes)**

Bits 1:0 **A28~A27 of Non-Cacheable Area I (within 512 MBytes)**

3.4 VGA General Registers

Miscellaneous Output Register

Register Type: Read/Write
Read Port: 3CC
Write Port: 3C2
Default: 00h

D7 **Vertical Sync Polarity**

0: Select 'positive vertical sync'
1: Select 'negative vertical sync'

D6 **Horizontal Sync Polarity**
0: Select 'positive horizontal sync'
1: Select 'negative horizontal sync'

Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 **Odd/Even Page**
0: Select low page of memory
1: Select high page of memory

D4 **Reserved**

D[3:2] **Clock Select**

Table for Video Clock Selection

D3	D2	FS[3:0]
0	0	0000 (25.175 MHz)
0	1	0001 (28.322 MHz)
1	0	Don't Care
1	1	For external clock, refer to Extended Registers SR7, Index_07h D[3:0].For internal clock generator, it's don't care.

D1 **Display RAM Enable**
0: Disable processor access to video RAM
1: Enable processor access to video RAM

D0 **I/O Address Select**
0: Sets addresses for monochrome emulation
1: Sets addresses for color graphics emulation

Feature Control Register

Register Type: Read/Write
Read Port: 3CA

Write Port: 3BA/3DA

Default: 00h

D[7:4] Reserved (0)

D3 Vertical Sync Select

0: Normal Vertical Sync output to monitor

1: [Vertical Sync OR Vertical Display Enable] output to monitor

D[2:0] Reserved (0)

Input Status Register 0

Register Type: Read only

Read Port: 3C2

Default: 00h

D7 Vertical Retrace Interrupt Pending

0: Cleared

1: Pending

D[6:5] Reserved

D4 Switch Sense

D[3:0] Reserved

Input Status Register 1

Register Type: Read only

Read Port: 3BA/3DA

Default: 00h

D[7:6] Reserved

D[5:4] Diagnostic

Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1	
D5	D4	D5	D4
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 **Vertical Retrace**
0: Inactive
1: Active

D[2:1] **Reserved**

D0 **Display Enable Not**
0: Display period
1: Retrace period

VGA Enable Register

Register Type: Read/Write

Read/Write Port:3C3 or 46E8

Default: 00h

D0 **VGA Enable (for 3C3 only)**
0: Disable
1: Enable

D3 **VGA Enable (for 46E8 only)**
0: Disable
1: Enable

Segment Selection Register 0

Register Type: Read/Write

Read/Write Port:3CD

Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then

D[7:6] **Reserved**

D[5:0] **Segment Selection Write Bit[5:0]**

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then

D[7:6] **Reserved**

D[5:3] **Segment Selection Write Bit[2:0]**

D[2:0] Segment Selection Read Bit[2:0]

Segment Selection Register 1

Register Type: Read/Write

Read/Write Port:3CB

Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then

D[7:6] Reserved

D[5:0] Segment Selection Read Bit[5:0]

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then

D[7:0] Reserved

3.5 CRT Controller Registers

CRT Controller Index Register

Register Type: Read/Write

Read/Write Port:3B4/3D4

Default: 00h

D[7:5] Reserved

D[4:0] CRT Controller Index

- 00h ~ 18h for standard VGA
- 19h ~ 26h for SiS extended registers

Index (3B4/3D4)	**CRT Controller Registers (3B5/3D5)**
0h	Horizontal Total
1h	Horizontal Display Enable End
2h	Horizontal Blank Start
3h	Horizontal Blank End
4h	Horizontal Retrace Start
5h	Horizontal Retrace End
6h	Vertical Total
7h	Overflow Register
8h	Preset Row Scan
9h	Max Scan Line/Text Character Height
Ah	Text Cursor Start
Bh	Text Cursor End
Ch	Screen Start Address High
Dh	Screen Start Address Low

Eh	Text Cursor Location High
Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
19h	Extended Signature Read-Back Register 0
1Ah	Extended Signature Read-Back Register 1
22h	Graphics Data Latch Readback Register
24h	Attribute Controller Toggle Readback Register
26h	Attribute Controller Index Readback Register

CR0: Horizontal Total

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 00h

Default: 00h

D[7:0] Horizontal Total Bit[7:0]

CR1: Horizontal Display Enable End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 01h

Default: 00h

D[7:0] Horizontal Display Enable End Bit[7:0]

CR2: Horizontal Blank Start

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 02h

Default: 00h

D[7:0] Horizontal Blank Start Bits[7:0]

CR3: Horizontal Blank End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 03h

Default: 00h

D7 **Reserved**

D[6:5] **Display Skew Control Bit[1:0]**
00: No skew
01: Skew 1 character
10: Skew 2 characters
11: Skew 3 characters

D[4:0] **Horizontal Blank End Bit[4:0]**

CR4: Horizontal Retrace Start

Register Type: Read/Write

Read/Write Port: 3B5/3D5, Index 04h

Default: 00h

D[7:0] **Horizontal Retrace Start Bits[7:0]**

CR5: Horizontal Retrace End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 05h

Default: 00h

D7 **Horizontal Blank End Bit[5]**

D[6:5] **Horizontal Retrace Delay Bit[1:0]**
00: Skew 0 character clock
01: Skew 1 character clock
10: Skew 2 character clocks
11: Skew 3 character clocks

D[4:0] **Horizontal Retrace End Bit[4:0]**

CR6: Vertical Total

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 06h

Default: 00h

D[7:0] **Vertical Total Bit[7:0]**

CR7: Overflow Register

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 07h

Default: 00h

D7 **Vertical Retrace Start Bit[9]**

D6 **Vertical Display Enable End Bit[9]**

D5 **Vertical Total Bit[9]**

D4 **Line Compare Bit[8]**

D3 **Vertical Blank Start Bit[8]**

D2 **Vertical Retrace Start Bit[8]**

D1 **Vertical Display Enable End Bit[8]**

D0 **Vertical Total Bit[8]**

CR8: Preset Row Scan

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 08h

Default: 00h

D7 **Reserved**

D[6:5] **Byte Panning Control Bit[1:0]**

D[4:0] **Preset Row Scan Bit[4:0]**

CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 09h

Default: 00h

D7 **Double Scan**

0: Disable

1: Enable 400 lines display

D6 **Line Compare Bit[9]**

D5 **Vertical Blank Start Bit[9]**

D[4:0] **Character Cell Height Bit[4:0]**

CRA: Text Cursor Start

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 0Ah

Default: 00h

D[7:6] **Reserved**

D5 **Text Cursor Off**

0: Text Cursor On
1: Text Cursor Off

D[4:0] **Text Cursor Start Bit[4:0]**

CRB: Text Cursor End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 0Bh

Default: 00h

D7 **Reserved**

D[6:5] **Text Cursor Skew**
00: No skew
01: Skew one character clock
10: Skew two character clocks
11: Skew three character clocks

D[4:0] **Text Cursor End Bit[4:0]**

CRC: Screen Start Address High

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 0Ch

Default: 00h

D[7:0] **Screen Start Address Bit[15:8]**

CRD: Screen Start Address Low

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 0Dh

Default: 00h

D[7:0] **Screen Start Address Bits[7:0]**

CRE: Text Cursor Location High

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 0Eh

Default: 00h

D[7:0] **Text Cursor Location Bits[15:8]**

CRF: Text Cursor Location Low

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 0Fh

Default: 00h

D[7:0] **Text Cursor Location Bits[7:0]**

CR10: Vertical Retrace Start

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 10h

Default: 00h

D[7:0] Vertical Retrace Start Bits[7:0]

CR11: Vertical Retrace End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 11h

Default: 00h

D7 Write Protect for CR0 to CR7

0: Disable Write Protect

1: Enable Write Protect

D6 Alternate Refresh Rate

0: Selects three refresh cycles per scanline

1: Selects five refresh cycles per scanline

D5 Vertical Interrupt Enable

0: Enable

1: Disable

D4 Vertical Interrupt Clear

0: Clear

1: Not Clear

D[3:0] Vertical Retrace End Bit[3:0]

CR12: Vertical Display Enable End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 12h

Default: 00h

D[7:0] Vertical Display Enable End Bit[7:0]

CR13: Screen Offset

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 13h

Default: 00h

D[7:0] Screen Offset Bits[7:0]

CR14: Underline Location Register

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 14h

Default: 00h

D7 **Reserved**

D6 **Doubleword Mode Enable**

0: Disable
1: Enable

D5 **Count by 4**

0: Disable
1: Enable

D[4:0] **Underline Location Bit[4:0]**

CR15: Vertical Blank Start

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 15h

Default: 00h

D[7:0] **Vertical Blank Start Bits[7:0]**

CR16: Vertical Blank End

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 16h

Default: 00h

D[7:0] **Vertical Blank End Bits[7:0]**

CR17: Mode Control Register

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 17h

Default: 00h

D7 **Hardware Reset**

0: Disable horizontal and vertical retrace outputs
1: Enable horizontal and vertical retrace outputs

D6 **Word/Byte Address Mode**

0: Set the memory address mode to word
1: Set the memory address mode to byte

D5 **Address Wrap**

0: Disable the full 256K of memory
1: Enable the full 256K of memory

D4 **Reserved**

D3 **Count by Two**

0: Byte refresh
1: Word refresh

D2 **Horizontal Retrace Select**

0: Normal
1: Double Scan

D1 **RA1 replace MA14**
0: Enable
1: Disable

D0 **RA0 replace MA13**
0: Enable
1: Disable

CR18: Line Compare Register

Register Type: Read/Write

Read/Write Port:3B5/3D5, Index 18h

Default: 00h

D[7:0] **Line Compare Bit[7:0]**

CR19: Extended Signature Read-Back Register 0

Register Type: Read Only

Read/Write Port:3B5/3D5, Index 19h

Default: 00h

D[7:0] **Signature read-back bit[7:0]**

CR1A: Extended Signature Read-Back Register 1

Register Type: Read Only

Read/Write Port:3B5/3D5, Index 1Ah

Default: 00h

D[7:0] **Signature read-back bit[15:8]**

CR22: Graphics Data Latch Readback Register

Register Type: Read Only

Read/Write Port:3B5/3D5, Index 22h

D[7:0] **Graphics Data Latch bit[7:0]**

CR24: Attribute Controller Toggle Readback Register

Register Type: Read Only

Read/Write Port:3B5/3D5, Index 24h

D7 **Attribute Controller Toggle**

D[6:0] **Reserved**

CR26: Attribute Controller Index Readback Register

Register Type: Read Only

Read/Write Port:3B5/3D5, Index 26h

D[7:6] **Reserved**

D5 **Video Enable**

D[4:0] **Attribute Controller Index bit[8:4]**

3.6 Sequencer Registers

Sequencer Index Register

Register Type: Read/Write

Read/Write Port:3C4

Default: 00h

D[7:6] **Reserved**

D[5:0] **Sequencer Index Bit[5:0]**

Table of Sequencer Registers

Index (3C4)	**Sequencer Register (3C5)**
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

SR0: Reset Register

Register Type: Read/Write

Read/Write Port:3C5, Index 00h

Default: 00h

D[7:2] **Reserved**

D1 **Synchronous reset**
0: Reset
1: Normal

D0 **Asynchronous reset**
0: Reset
1: Normal

SR1: Clock Mode Register

Register Type: Read/Write

Read/Write Port:3C5, Index 01h

Default: 00h

D[7:6] Reserved

D5 Screen Off

0: Display On

1: Display Off

D4 Shifter Load 32 enable

0: Disable

1: Data shifter loaded every 4th Character Clock

D3 Dot Clock Divide by 2 enable

0: Disable

1: Video Clock is divided by 2 to generate Dot Clock

D2 Shifter Load 16 (while D4=0)

0: Disable

1: Data shifter loaded every 2nd Character Clock

D1 Reserved

D0 8/9 Dot Clock

0: Dot Clock is divided by 9 to generate Character Clock

1: Dot Clock is divided by 8 to generate Character Clock

SR2: Color Plane Write Enable Register

Register Type: Read/Write

Read/Write Port:3C5, Index 02h

Default: 00h

D[7:4] Reserved

D3 Plane 3 write enable

0: Disable

1: Enable

D2 Plane 2 write enable

0: Disable

1: Enable

D1 Plane 1 write enable

0: Disable

1: Enable

D0 Plane 0 write enable

0: Disable

1: Enable

SR3: Character Generator Select Register

Register Type: Read/Write

Read/Write Port:3C5, Index 03h

Default: 00h

D[7:6] **Reserved**

D5 **Character generator table B select Bit[2]**

D4 **Character generator table A select Bit[2]**

D[3:2] **Character generator table B select Bit[1:0]**

D[1:0] **Character generator table A select Bit[1:0]**

Table of Selecting Active Character Generator

D5	D3	D2	Used when text attribute bit 3 is 1
D4	D1	D0	Used when text attribute bit 3 is 0
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

SR4: Memory Mode Register

Register Type: Read/Write

Read/Write Port:3C5, Index 04h

Default: 00h

D[7:4] **Reserved**

D3 **Chain-4 Mode enable**
0: Disable
1: Enable

D2 **Odd/Even Mode enable**
0: Enable
1: Disable

D1 **Extended Memory**
0: Select 64K
1: Select 256K

D0 **Reserved**

3.7 Graphics Controller Registers

Graphics Controller Index Register

Register Type: Read/Write

Read/Write Port:3CE

Default: 00h

D[7:4] Reserved

D[3:0] Graphics Controller Index Bit[3:0]

Index (3CE)	**Graphics Controller Register (3CF)**
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

GR0: Set/Reset Register

Register Type: Read/Write

Read/Write Port:3CF, Index 00h

Default: 00h

D[7:4] Reserved

D3 Set/Reset Map for plane 3

D2 Set/Reset Map for plane 2

D1 Set/Reset Map for plane 1

D0 Set/Reset Map for plane 0

GR1: Set/Reset Enable Register

Register Type: Read/Write

Read/Write Port:3CF, Index 01h

Default: 00h

D[7:4] Reserved

D3 Enable Set/Reset for plane 3

0: Disable
1: Enable

D2 **Enable Set/Reset for plane 2**
0: Disable
1: Enable

D1 **Enable Set/Reset for plane 1**
0: Disable
1: Enable

D0 **Enable Set/Reset for plane 0**
0: Disable
1: Enable

GR2: Color Compare Register

Register Type: Read/Write

Read/Write Port:3CF, Index 02h

Default: 00h

D[7:4] **Reserved**

D3 **Color Compare Map for plane 3**

D2 **Color Compare Map for plane 2**

D1 **Color Compare Map for plane 1**

D0 **Color Compare Map for plane 0**

GR3: Data Rotate/Function Select Register

Register Type: Read/Write

Read/Write Port:3CF, Index 03h

Default: 00h

D[7:5] **Reserved**

D[4:3] **Function Select**

Table of Function Select

D4	D3	Function
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] **Rotate Count**

Table of Rotate Count

D2	D1	D0	Right Rotation
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

GR4: Read Plane Select Register

Register Type: Read/Write

Read/Write Port:3CF, Index 04h

Default: 00h

D[7:2] **Reserved**

D[1:0] **Read Plane Select bit 1, 0**

00: Plane 0
01: Plane 1
10: Plane 2
11: Plane 3

GR5: Mode Register

Register Type: Read/Write

Read/Write Port:3CF, Index 05h

Default: 00h

D7 **Reserved**

D6 **256-color Mode**

0: Disable
1: Enable

D5 **Shift Register Mode**

0: Configure shift register to be EGA compatible
1: Configure shift register to be CGA compatible

D4 **Odd/Even Addressing Mode enable**

0: Disable
1: Enable

D3 **Read Mode**

0: Map Select Read
1: Color Compare Read

D2 **Reserved**

D[1:0] **Write mode**

Table for Write Mode

D1	D0	Mode Selected
0	0	Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).
0	1	Write Mode 1: Use content of latches as write data.
1	0	Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply)

GR6: Miscellaneous Register

Register Type: Read/Write

Read/Write Port:3CF, Index 06h

Default: 00h

D[7:4] **Reserved**

D[3:2] **Memory Address Select**

Table of Memory Address Select

D3	D2	Address range
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 **Chain Odd And Even Maps**
0: Disable
1: Enable

D0 **Graphics Mode Enable**
0: Select alphanumeric mode
1: Select graphics mode

GR7: Color Don't Care Register

Register Type: Read/Write

Read/Write Port:3CF, Index 07h

Default: 00h

D[7:4] **Reserved**

D3 **Plane 3 Don't Care**
0: Disable color comparison
1: Enable color comparison

D2 **Plane 2 Don't Care**
0: Disable color comparison
1: Enable color comparison

D1 **Plane 1 Don't Care**
0: Disable color comparison
1: Enable color comparison

D0 **Plane 0 Don't Care**
0: Disable color comparison
1: Enable color comparison

GR8: Bit Mask Register

Register Type: Read/Write

Read/Write Port:3CF, Index 08h

Default: 00h

D[7:0] **Bit Mask Enable Bit[7:0]**

3.8 Attribute Controller and Video DAC Registers

Attribute Controller Index Register

Register Type: Read/Write

Read Port: 3C0

Write Port: 3C0

Default: 00h

D[7:6] **Reserved**

D5 **Palette Address Source**
0: From CPU
1: From CRT

D[4:0] **Attribute Controller Index Bit[4:0] (00h-14h)**

Index (3C0)	**Attribute Controller Register (3C0)**
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Pixel Panning Register
14h	Color Select Register (VGA)

AR0~ARF: Palette Registers

Register Type: Read/Write
Read Port: 3C1, Index 00h ~ 0Fh
Write Port: 3C0, Index 00h ~ 0Fh
Default: 00h

D[7:6] Reserved

D[5:0] Palette Entries

AR10: Mode Control Register

Register Type: Read/Write
Read Port: 3C1, Index 10h

Write Port: 3C0, Index 10h

Default: 00h

D7 P4, P5 Source Select

0: AR0-F Bits[5:4] are used as the source for the Lookup Table Address Bits[5:4]

1: AR14 Bits[1:0] are used as the source for the Lookup Table Address Bits[5:4]

D6 Pixel Double Clock Select

0: The pixels are clocked at every clock cycle

1: The pixels are clocked at every other clock cycle

D5 PEL Panning Compatibility with Line Compare

0: Disable

1: Enable

D4 Reserved

D3 Background Intensity or Blink enable (while the Character Attribute D7=1)

0: Background Intensity attribute enable

1: Background Blink attribute enable

D2 Line Graphics enable

0: The ninth bit of nine-bit-wide character cell will be the same as the background.

1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.

D1 Display Type

0: The contents of the Attribute byte are treated as color attribute.

1: The contents of the Attribute byte are treated as MDA-compatible attribute.

D0 Graphics/Text Mode

0: The Attribute Controller will function in text mode.

1: The Attribute Controller will function in graphics mode.

AR11: Screen Border Color

Register Type: Read/Write

Read Port: 3C1, Index 11h

Write Port: 3C0, Index 11h

Default: 00h

D[7:6] Reserved

D[5:0] Palette Entry

AR12: Color Plane Enable Register

Register Type: Read/Write

Read Port: 3C1, Index 12h

Write Port: 3C0, Index 12h

Default: 00h

D[7:6] Reserved

D[5:4] Display Status MUX Bit[1:0]

These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table for Video Read-back Through Diagnostic Bit (I)

Color Plane Enable Register		Input Status Register 1	
D5	D4	D5	D4
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table for Video Read-back Through Diagnostic Bit (II)

Color Plane Enable Register		Input Status Register 1	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

AR13: Pixel Panning Register

Register Type: Read/Write

Read Port: 3C1, Index 13h

Write Port: 3C0, Index 13h

Default: 00h

D[7:4] Reserved

D[3:0] Pixel Pan Bit[3:0]

This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

D3	**D2**	**D1**	**D0**	**Monochrome Text**	**VGA Mode 13**	**All others**
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2

0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

AR14: Color Select Register

Register Type: Read/Write

Read Port: 3C1, Index 14h

Write Port: 3C0, Index 14h

Default: 00h

D[7:4] Reserved

D[3:2] Color Bit[7:6]

These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6]

D[1:0] Color Bit[5:4]

If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

3.9 Color Registers

DAC Status Register

Register Type: Read Only

Read Port: 3C7

Default: 00h

D[7:2] Reserved

D[1:0] DAC State Bit[1:0]

00: Write Operation in progress
11: Read Operation in progress

DAC Index Register (Read Mode)

Register Type: Write Only

Write Port: 3C7

Default: 00h

D[7:0] DAC Index Bit[7:0]

DAC Index Register (Write Mode)

Register Type: Read/Write

Read/Write Port:3C8

Default: 00h

D[7:0] DAC Index Bit[7:0]

DAC Data Register

Register Type: Read/Write

Read/Write Port:3C9

Default: 00h

D[7:6] Reserved

D[5:0] DAC Data [5:0]

Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.

Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.

PEL Mask Register

Register Type: Read/Write

Read/Write Port:3C6

Default: 00h

D[7:0] Pixel Mask Bit[7:0]

This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

3.10 Integrated VGA Controller Extended Registers

Extended Index Register

Register Type: Read/Write

Read/Write Port:3C4

Default: 00h

D[7:6] Reserved

D[5:0] Extended Register Index Bit[5:0] (05h ~ 37h)

Index (3C4)	**Extended Enhanced Register (3C5)**
05h	Extended Password/Identification Register
06h	Extended Graphics Mode Control Register
07h	Extended Misc. Control Register 0
08h	Extended CRT/CPU Threshold Control Register 0
09h	Extended CRT/CPU Threshold Control Register 1
0Ah	Extended CRT Overflow Register
0Bh	Extended Misc. Control Register 1
0Ch	Extended Misc. Control Register 2
0Dh	Extended Configuration Status 0
0Eh	Extended Configuration Status 1
0Fh	Extended Scratch Register 0
10h	Extended Scratch Register 1
11h	Extended DDC and Power Control Register
14h	Extended Hardware Cursor Color 0 Red Register
15h	Extended Hardware Cursor Color 0 Green Register
16h	Extended Hardware Cursor Color 0 Blue Register
17h	Extended Hardware Cursor Color 1 Red Register
18h	Extended Hardware Cursor Color 1 Green Register
19h	Extended Hardware Cursor Color 1 Blue Register
1Ah	Extended Hardware Cursor Horizontal Start Register 0
1Bh	Extended Hardware Cursor Horizontal Start Register 1
1Ch	Extended Hardware Cursor Horizontal Preset Register
1Dh	Extended Hardware Cursor Vertical Start Register 0
1Eh	Extended Hardware Cursor Vertical Start Register 1
1Fh	Extended Hardware Cursor Vertical Preset Register
20h	Extended Linear Addressing Base Address Register 0

21h	Extended Linear Addressing Base Address Register 1
22h	Extended Standby/Suspend Timer Register
23h	Extended Misc. Control Register 3
24h	Extended Graphics Frame Buffer Location Address Register
25h	Extended Scratch Register 2
26h	Extended Graphics Engine Regiser 0
27h	Extended Graphics Engine Register 1
28h	Extended Internal Memory Clock Register 0
29h	Extended Internal Memory Clock Register 1
2Ah	Extended Internal Video Clock Register 0
2Bh	Extended Internal Video Clock Register 1
2Ch	Extended Turbo Queue Base Address
2Dh	Extended Memory Start Control Register
2Eh	Extended Shared Memory Control Register
2Fh	Extended DRAM Frame Buffer Size Register
30h	Fast Page Flip Starting Address Low Register
31h	Fast Page Flip Starting Address Middle Register
32h	Fast Page Flip Starting Address High Register
33h	Extended Reserved Register
34h	Extended Reserved Register
35h	Extended Misc. Control Register 4
36h	Extended Scratch Register 3
37h	Extended Scratch Register 4

SR5: Extended Password/Identification Register

Register Type: Read/Write

Read/Write Port:3C5, Index 05h

Default: 00h

D[7:0] Password/Identification Bit[7:0]

If 86h is written into this register, then A1h will be read from this register , and unlock all the extension registers.

If the value other than 86h is written into this register, then 21h will be read from this register, and lock all the extension registers.

SR6: Extended Graphics Mode Control Register

Register Type: Read/Write

Read/Write Port:3C5, Index 06h

Default: 00h

D7 **Graphics mode linear addressing enable**
0: Disable
1: Enable

D6 **Graphics mode hardware cursor display enable**
0: Disable
1: Enable

D5 **Graphics mode interlaced enable**
0: Disable
1: Enable

D4 **True Color graphics mode enable**
0: Disable
1: Enable

D3 **64K Color graphics mode enable**
0: Disable
1: Enable

D2 **32K Color graphics mode enable**
0: Disable
1: Enable

D1 **Enhanced graphics mode enable**
0: Disable
1: Enable

D0 **Enhanced text mode enable**
0: Disable
1: Enable

SR7: Extended Misc. Control Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 07h

Default: 00h

D7 **Intelligent CRT prefetch**
0: Disable
1: Enable

D6 **Enable feature connector (VIDEO 0-7, PCLK) output**
0: Enable
1: Disable

D5 **Internal RAMDAC operation**
0: Low Speed mode (low power consumption)
1: High Speed mode

D4 **Extended video clock frequency divided by 2**

0: Disable
1: Enable

D[3:0] Reserved

SR8: Extended CRT/CPU Threshold Control Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 08h

Default: 00h

D[7:4] CRT/CPU Arbitration Threshold Low Bit[3:0]

D[3:0] CRT/Engine Threshold High Bit[3:0]

SR9: Extended CRT/CPU Threshold Control Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 09h

Default: 00h

D[7:4] ASCII/Attribute Threshold Bit[3:0]

D[3:0] CRT/CPU Threshold High Bit[3:0]

SRA: Extended CRT Overflow Register

Register Type: Read/Write

Read/Write Port:3C5, Index 0Ah

Default: 00h

D[7:4] Extended Screen Offset Bit[11:8]

D3 Extended Vertical Retrace Start Bit[10]

D2 Extended Vertical Blank Start Bit[10]

D1 Extended Vertical Display Enable End Bit[10]

D0 Extended Vertical Total Bit[10]

SRB: Extended Misc. Control Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 0Bh

Default: 00h

D7 True-Color Graphics mode RGB Sequence Selection

0: Red, Green, and Blue in byte order
1: Blue, Green, and Red in byte order

D[6:5] Memory-mapped I/O Space Selection Bit[1:0]

00: Disable
01: Select Axxxxh as Memory-mapped I/O Space
10: Select Bxxxxh as Memory-mapped I/O Space

11: Select PCI config register 14H as Memory-mapped I/O space

D4 **True-Color frame rate modulation enable**
0: Disable
1: Enable

D3 **Dual segment register mode enable**
0: Disable
1: Enable

D2 **I/O gating enable while write buffer is not empty**
0: Disable
1: Enable

D1 **16-color packed pixel enable**
0: Disable
1: Enable

D0 **CPU-driven BITBLT operation enable**
0: Disable
1: Enable

SRC: Extended Misc. Control Register 2

Register Type: Read/Write

Read/Write Port:3C5, Index 0Ch

Default: 00h

D7 **Graphics mode 32 bit memory access enable**
0: Disable
1: Enable

D6 **Text mode 16 bit memory access enable**
0: Disable
1: Enable

D5 **Read-ahead cache operation enable**
0: Disable
1: Enable

D4 **Reserved**

D3 **Test mode enable**
0: Disable
1: Enable

D[2:1] **Memory Configuration Bit[1:0]**
00: 1MByte/1 bank
01: 2MByte/2 banks
10: 4MByte/2 banks or 4 banks
11: 1MByte/2 banks

D0 **Synchronous reset timing generator enable**
0: Disable

1: Enable

SRD: Extended Configuration Status 0

Register Type: Read Only

Read Port: 3C5, Index 0Dh

Default: 00h

D7 **Enable 64K ROM decoding**
0: Disable
1: Enable when MD23 is pulled up with resistor.

D6 **Clock Generator Selection**
0: Select external clock generator (used for SiS internal test only)
1: Select internal clock generator when MD22 is pulled up with resistor

D5 **EDO DRAM Type Selection**
0: Select Fast Page DRAM type
1: Select EDO DRAM type when MD21 is pulled up with resistor.

D4 **PCI Function Device Behavior**
0: Single Function Device
1: Multi-Function Device when MD20 is pulled up with resistor.

D3 **256Kx16 DRAM Type Selection**
0: 1-WE/2-CAS 256Kx16 DRAM type
1: 2-WE/1-CAS 256Kx16 DRAM type when MD19 is pulled up with resistor.

D2 **BIOS ROM decoding logic**
0: Enable
1: Disable when MD18 is pulled up with resistor.

D1 **Video subsystem enable/disable at power-on is**
0: Controlled by System BIOS
1: Forced to disable when MD17 is pulled up with resistor.

D0 **Select I/O address 3C3h or 46E8h as video subsystem port**
0: Select 3C3h
1: Select 46E8h when MD16 is pulled up with reSiStor.

SRE: Extended Configuration Status 1

Register Type: Read Only

Read Port: 3C5, Index 0Eh

Default: 00h

D[7:6] **Reserved**

D5 **GPIO pin polarity**
0: Positive
1: Negative when MD29 is pulled up with resistor.

D4 **Reserved**

D3 **INTA# Selection**
0: Disable
1: Enable when MD27 is pulled up with resistor

D[2:0] **PCI Function Number Bit[2:0] which are configured by whetherMD[26:24] are pulled up with resistors (bit=1) or not (bit=0)**
[000:111]=PCI Function Device Number[0:7] (default=0)

SRF: Extended Scratch Register 0

Register Type: Read/Write
Read/Write Port:3C5, Index 0Fh
Default: 00h

D[7:0] **Reserved for video BIOS**

SR10: Extended Scratch Register 1

Register Type: Read/Write
Read/Write Port:3C5, Index 10h
Default: 00h

D[7:0] **Reserved for video BIOS**

SR11: Extended DDC and Power Control Register

Register Type: Read/Write
Read/Write Port:3C5, Index 11h
Default: 00h

D7 **Force VGA into suspend mode**
0: Disable
1: Enable

D6 **Force VGA into standby mode**
0: Disable
1: Enable

D5 **Enable video memory access as activation source**
0: Disable
1: Enable

D4 **Enable keyboard and hardware cursor as system activation source**
0: Disable
1: Enable

D[3:2] **Reserved**

D1 **DDC DATA Programming**
While writing this bit,
0: Output '0' logic into DDC Data Signal.
1: Output '1' logic into DDC Data Signal.

While reading this bit,
0: Get '0' logic from DDC Data Signal .
1: Get '1' logic from DDC Data Signal .

D0 **DDC CLK Programming**
While writing this bit,
0: Output '0' logic into DDC Clock Signal.
1: Output '1' logic into DDC Clock Signal.
While reading this bit,
0: Get '0' logic from DDC Clock Signal .
1: Get '1' logic from DDC Clock Signal .

SR14: Extended Hardware Cursor Color 0 Red Register

Register Type: Read/Write

Read/Write Port:3C5, Index 14h

Default: 00h

D[7:6] **Reserved**

D[5:0] **Hardware Cursor Color 0 Red Bit[5:0]**

SR15: Extended Hardware Cursor Color 0 Green Register

Register Type: Read/Write

Read/Write Port:3C5, Index 15h

Default: 00h

D[7:6] **Reserved**

D[5:0] **Hardware Cursor Color 0 Green Bit[5:0]**

SR16: Extended Hardware Cursor Color 0 Blue Register

Register Type: Read/Write

Read/Write Port:3C5, Index 16h

Default: 00h

D[7:6] **Reserved**

D[5:0] **Hardware Cursor Color 0 Blue Bit[5:0]**

SR17: Extended Hardware Cursor Color 1 Red Register

Register Type: Read/Write

Read/Write Port:3C5, Index 17h

Default: 00h

D[7:6] **Reserved**

D[5:0] **Hardware Cursor Color 1 Red Bit[5:0]**

SR18: Extended Hardware Cursor Color 1 Green Register

Register Type: Read/Write

Read/Write Port:3C5, Index 18h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 1 Green Bit[5:0]

SR19: Extended Hardware Cursor Color 1 Blue Register

Register Type: Read/Write

Read/Write Port:3C5, Index 19h

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Color 1 Blue Bit[5:0]

SR1A: Extended Hardware Cursor Horizontal Start Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 1Ah

Default: 00h

D[7:0] Hardware Cursor Horizontal Start Bit[7:0]

SR1B: Extended Hardware Cursor Horizontal Start Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 1Bh

Default: 00h

D[7:3] Reserved

D[2:0] Hardware Cursor Horizontal Start Bit[10:8]

SR1C: Extended Hardware Cursor Horizontal Preset Register

Register Type: Read/Write

Read/Write Port:3C5, Index 1Ch

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Horizontal Preset Bit[5:0]

SR1D: Extended Hardware Cursor Vertical Start Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 1Dh

Default: 00h

D[7:0] Hardware Cursor Vertical Start Bit[7:0]

SR1E: Extended Hardware Cursor Vertical Start Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 1Eh

Default: 00h

D[7:4] Hardware Cursor Pattern Select Bit[3:0]

D3 Reserved

D[2:0] Hardware Cursor Vertical Start Bit[10:8]

SR1F: Extended Hardware Cursor Vertical Preset Register

Register Type: Read/Write

Read/Write Port:3C5, Index 1Fh

Default: 00h

D[7:6] Reserved

D[5:0] Hardware Cursor Vertical Preset Bit[5:0]

SR20: Extended Linear Addressing Base Address Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 20h

Default: 00h

D[7:0] Linear Addressing Base Address Bit[26:19]

SR21: Extended Linear Addressing Base Address Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 21h

Default: 00h

D7 Reserved

D[6:5] Linear Addressing Space Aperture Bit[1:0]

00: 512 KByte
01: 1 MByte
10: 2 Mbyte
11: 4MByte

D[4:0] Linear Addressing Base Address Bit[31:27]

SR22: Extended Standby/Suspend Timer Register

Register Type: Read/Write

Read/Write Port:3C5, Index 22h

Default: 00h

D[7:4] Suspend Timer Bit[3:0]

The resolution for Suspend Timer is 2 minutes.

D[3:0] **Standby Timer Bit[3:0]**
The resolution for Standby Timer is 2 minutes.

SR23: Extended Misc. Control Register 3

Register Type: Read/Write

Read/Write Port:3C5, Index 23h

Default: 00h

D7 **General purpose output pin (GPIO)**
When GPIO polarity is positive,
0: GPIO pin output low
1: GPIO pin output high
When GPIO polarity is negative,
0: GPIO pin output high
1: GPIO pin output low

D6 **CRC Generator Enable**
0: Disable
1 Enable

D5 **EDO DRAM Enable Bit**
0: Disable
1: Enable

D4 **Bypass SRAM**
0: Disable
1: Enable

D3 **Video compatible Hardware Cursor visibility enable**
0: Disable
1: Enable

D2 **Reserved**

D[1:0] **DRAM Control Signal Delay Compensation Bit[1:0]**
00: Delay 4 ns
01: Delay 5 ns
10: Delay 6 ns
11: Delay 7 ns

SR24: Extended Graphics Frame Buffer Location Address Register

Register Type: Read/Write

Read/Write Port:3C5, Index 24h

Default: 00h

D[7:0] **Grapphics Frame Buffer Location address Bit[7:0]**
When 32-bit mode, this register is in unit of 256 KB
When 64-bit mode, this register is in unit of 512 KB

SR25: Extended Scratch Register 2

Register Type: Read/Write

Read/Write Port:3C5, Index 25h

Default: 00h

D[7:0] Reserved for VGA BIOS

SR26: Extended Graphics Engine Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 26h

Default: 00h

D7 Enable ASCII Page-Hit Detection
0: Disable
1: Enable

D6 Power-down Internal RAMDAC
0: Disable
1: Enable

D5 PCI Burst-Write Mode enable
0: Disable
1: Enable

D4 Continuous Memory Data Access Enable Bit
0: Disable
1: Enable

D3 Internal VGAREQ* and VGAGNT* synchronize to HCLK
0: Asynchronous
1: Synchronous

D2 Slow DRAM RAS pre-charge time
0: Disable (3 MCLK/DRAM cycle)
1: Enable (4 MCLK/DRAM cycle)

D1 Slow DRAM Timing enable
0: Disable (7 MCLK/DRAM cycle)
1: Enable (8 MCLK/DRAM cycle)

D0 Reserved

SR27: Extended Graphics Engine Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 27h

Default: 00h

D7 Turbo Queue Engine enable
0: Disable
1: Enable

D6 **Graphics Engine Register Programming enable**
0: Disable
1: Enable

D[5:4] **Logical Screen Width and Byte-Per-Pixel Select Bit[1:0]**
00: 1024, 256 colors or 512, 32k/64k colors
01: 2048, 256 colors or 1024, 32k/64k colors
10: 4096, 256 colors or 2048, 32k/64k colors
11: invalid

D[3:0] **Extended Screen Start Address Bit[19:16]**

SR28: Extended Internal Memory Clock Register 0

Register Type: Read/Write

Read/Write Port:3C5, Index 28h

Default: 00h

D[7] **MCLK Divider**
0: Do not divide
1: Divide by 2

D[6:0] **MCLK Numerator Bit[6:0]**
[0000000:1111111] = [1:128]

NOTE: For the operation of internal memory clock generation, please refer to "Sec. 2.6 Internal Dual-Clock Synthesizer".

SR29: Extended Internal Memory Clock Register 1

Register Type: Read/Write

Read/Write Port:3C5, Index 29h

Default: 00h

D7 **MCLK VCO Gain**
0: Gain for low frequency operation
1: Gain for high frequency operation

D[6:5] **MCLK Post-Scale Bit[1:0]**
00: Do not scale
01: Scale by 2
10: Scale by 3
11: Scale by 4

D[4:0] **MCLK DeNumerator Bit[4:0]**
[00000:11111] = [1:32]

NOTE: For the operation of internal memory clock generation, please refer to "2.8.16 Internal Dual-Clock Synthesizer" on page 38.

SR2A: Extended Internal Video Clock Register 0

Register Type: Read/Write

Read/Write Port:3C5h,Index 2Ah

Default: 00h

D[7] VCLK Divider

0: Do not divide

1: Divide by 2

D[6:0] VCLK Numerator Bit[6:0]

[0000000:1111111] = [1:128]

NOTE: For the operation of internal video clock generation, please refer to "2.8.16 Internal Dual-Clock Synthesizer" on page 38.

SR2B: Extended Internal Video Clock Register 1

Register Type: Read/Write

Read/Write Port:3C5h, Index 2Bh

Default: 00h

D7 VCLK VCO Gain

0: Gain for low frequency operation

1: Gain for high frequency operation

D[6:5] VCLK Post-Scale Bit[1:0]

00: Do not scale

01: Scale by 2

10: Scale by 3

11: Scale by 4

D[4:0] VCLK DeNumerator Bit[4:0]

[00000:11111] = [1:32]

NOTE: For the operation of internal video clock generation, please refer to "2.8.16 Internal Dual-Clock Synthesizer" on page 38.

SR2C: Extended Turbo Queue Base Address

Register Type: Read/Write

Read/Write Port:3C5h, Index 2Ch

Default: 00h

D7 Reserved

D[6:0] Turbo Queue Base Address Bits[6:0]

SR2D: Extended Memory Start Control Register

Register Type: Read/Write

Read/Write Port:3C5, Index 2Dh

Default: 00h

D7 Column Address Scramble Enable

0: Disable

1: Enable

D6 **Shared-memory 3-wire, 2-request Mode**
0: Disable
1: Enable

D5 **Special Asynmetric DRAM Type**
0: Disable
1: Enable

D4 **Shared-memory 2-wire, 2-request Mode**
0: Disable
1: Enable

D[3:0] **Page Size Select**
0000: 2 KB at 32-bit mode, 4 KB at 64-bit mode
0001: 4 KB at 32-bit mode, 8 KB at 64-bit mode
0010: 8 KB at 32-bit mode, 16 KB at 64-bit mode
0011: 16 KB at 32-bit mode, 32 KB at 64-bit mode
0100: 1 KB at 32-bit mode, 2 KB at 64-bit mode
Others: Reserved

SR2E: Extended Shared Memory Control Register

Register Type: Read/Write

Read/Write Port:3C5h, Index 2Eh

Default: 00h

D[7:4] **Memory Address Scrambling Table Selection Bit[3:0]**

D[3:2] **Row Address Selection Bit[1:0]**
00: Row address [11:0] = memory address [20:9]
01: Row address [11:0] = memory address [21:10]
10: Row address [11:0] = memory address [22:11]
11: Row address [11:0] = memory address [23:12]

D[1:0] **RAS Selection Bit[1:0]**
00: RAS0 active
01: RAS1 active
10: RAS2 active
11: RAS3 active

SR2F: Extended DRAM Frame Buffer Size Register

Register Type: Read/Write

Read/Write Port:3C5, Index 2Fh

Default: 00h

D7 **Reserved**

D6 **Read-Modified-Write Timing Selection**
0: 5 MCLK

1: 6 MCLK

D5 **Enable Fast Change Mode Timing**
0: Disable
1: Enable

D4 **Enable Fast Page Flip**
0: Disable
1: Enable

D3 **Enable Extended DRAM Frame Buffer Sizing**
0: Disable
1: Enable

D[2:0] **Extended DRAM Frame Buffer Size Bit[2:0]**
000: 256 KB for 32-bit DRAM data bus, 512 KB for 64-bit DRAM data bus
001: 512 KB for 32-bit DRAM data bus, 1 MB for 64-bit DRAM data bus
010: 768 KB for 32-bit DRAM data bus, 1.5 MB for 64-bit DRAM data bus
011: 1 MB for 32-bit DRAM data bus, 2 MB for 64-bit DRAM data bus
100: 1.25 MB for 32-bit DRAM data bus, 2.5 MB for 64-bit DRAM data bus
101: 1.5 MB for 32-bit DRAM data bus, 3 MB for 64-bit DRAM data bus
110: 1.75 MB for 32-bit DRAM data bus, 3.5 MB for 64-bit DRAM data bus
111: 2 MB for 32-bit DRAM data bus, 4 MB for 64-bit DRAM data bus

SR30: Fast Page Flip Starting Address Low Register

Register Type: Read/Write

Read/Write Port:3C5, Index 30h

Default: 00h

D[7:0] **Fast Page Flip Starting Address bits[7:0]**

SR31: Fast Page Flip Starting Address Middle Register

Register Type: Read/Write

Read/Write Port:3C5, Index 31h

Default: 00h

D[7:0] **Fast Page Flip Starting Address bits[15:8]**

SR32: Fast Page Flip Starting Address High Register

Register Type: Read/Write

Read/Write Port:3C5, Index 32h

Default: 00h

D[7:4] **Reserved**

D[3:0] **Fast Page Flip Starting Address bits[19:16]**

SR33: Extended Reserved Register

Register Type: Read/Write

Read/Write Port:3C5, Index 33h

Default: 00h

D[7:0] Reserved

SR34: Extended Reserved Register

Register Type: Read/Write

Read/Write Port:3C5, Index 34h

Default: 00h

D[7:0] Reserved

SR35: Extended Misc. Controller Register 4

Register Type: Read/Write

Read/Write Port:3C5, Index 35h

Default: 00h

D[7:4] Reserved

D[3:2] CAS Delay timing compensation bits[1:0]

00: 0 ns
01: 2 ns
10: 4 ns
11: 6 ns

D1 Enable PCI Bus Write Cycle Retry

0: Disable
1: Enable

D0 Enable PCI Bus Read Cycle Retry

0: Disable
1: Enable

SR36: Extended Scratch Register 3

Register Type: Read/Write

Read/Write Port:3C5, Index 36h

Default: 00h

D[7:0] Reserved for VGA BIOS

SR37: Extended Scratch Register 4

Register Type: Read/Write

Read/Write Port:3C5, Index 37h

Default: 00h

D[7:0] Reserved for VGA BIOS

3.11 Graphics Engine Related Registers

Integrated VGA Controller integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in Integrated VGA Controller include BitBlt, BitBlt with mask, Color/Font Expansion, Enhanced Color/Font Expansion, Line Drawing, and Direct Draw.

Since the register formats for the line drawing and Direct Draw are different from those of the other general engine functions, we would like to describe these three register formats seperately in the following paragraphs:

Register Format for General Engine Functions

The following table shows the register format for the general Graphics Engine functions.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Reserved	SRC Start Linear Address [21:0]			8280h
Reserved	DST Start Linear Address [21:0]			8284h
DST Pitch		SRC Pitch		8288h
Rectangular Height		Rectangular Width		828Ch
FG Rop	FG (Foreground) Color			8290h
BG Rop	BG (Background) Color			8294h
Mask3	Mask2	Mask1	Mask0	8298h
Mask7	Mask6	Mask5	Mask4	829Ch
Top Clipping		Left Clipping		82A0h
Bottom Clipping		Right Clipping		82A4h
Command 1	Command 0	Command Queue Status		82A8h
Pattern 3	Pattern 2	Pattern 1	Pattern 0	82ACh
Pattern 7	Pattern 6	Pattern 5	Pattern 4	82B0h
Pattern 11	Pattern 10	Pattern 9	Pattern 8	82B4h
Pattern 15	Pattern 14	Pattern 13	Pattern 12	82B8h
Pattern 19	Pattern 18	Pattern 17	Pattern 16	82BCh
Pattern 23	Pattern 22	Pattern 21	Pattern 20	82C0h
Pattern 27	Pattern 26	Pattern 25	Pattern 24	82C4h
Pattern 31	Pattern 30	Pattern 29	Pattern 28	82C8h
Pattern 35	Pattern 34	Pattern 33	Pattern 32	82CCh
Pattern 39	Pattern 38	Pattern 37	Pattern 36	82D0h

Pattern 43	Pattern 42	Pattern 41	Pattern 40	82D4h
Pattern 47	Pattern 46	Pattern 45	Pattern 44	82D8h
Pattern 51	Pattern 50	Pattern 49	Pattern 48	82DCh
Pattern 55	Pattern 54	Pattern 53	Pattern 52	82E0h
Pattern 59	Pattern 58	Pattern 57	Pattern 56	82E4h
Pattern 63	Pattern 62	Pattern 61	Pattern 60	82E8h

Source Start Linear Address

Register Type: Read/Write

Read/Write Port:8280h~8283h

Default: 00h

D[31:22] Reserved

D[21:0] Source Start Linear Address Bit[21:0]

Destination Start Linear Address

Register Type: Read/Write

Read/Write Port:8284h~8287h

Default: 00h

D[31:22] Reserved

D[21:0] Destination Start Linear Address Bit[21:0]

Source Pitch

Register Type: Read/Write

Read/Write Port:8288h~8289h

Default: 00h

D[15:12] Reserved

D[11:0] Source Pitch Bit[11:0]

Destination Pitch

Register Type: Read/Write

Read/Write Port:828Ah~828Bh

Default: 00h

D[15:12] Reserved

D[11:0] Destination Pitch Bit[11:0]

Rectangular Width

Register Type: Read/Write

Read/Write Port:828Ch~828Dh

Default: 00h

D[15:12] Reserved

D[11:0] Destination Rectangular Width Bit[11:0]

Rectangular Height

Register Type: Read/Write

Read/Write Port:828Eh~828Fh

Default: 00h

D[15:12] Reserved

D[11:0] Destination Rectangular Height Bit[11:0]

Foreground Color

Register Type: Read/Write

Read/Write Port:8290h~8292h

Default: 00h

D[23:0] Foreground Color Bit[23:0]

FG Rop

Register Type: Read/Write

Read/Write Port:8293h

Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

Background Color

Register Type: Read/Write

Read/Write Port:8294h~8296h

Default: 00h

D[23:0] Background Color Bit[23:0]

BG Rop

Register Type: Read/Write

Read/Write Port:8297h

Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

Mono Mask Register

Register Type: Read/Write

Read/Write Port:8298h~829Fh

Default: 00h

D[63:0] Mono Mask Bit[63:0]

Left Clipping

Register Type: Read/Write

Read/Write Port:82A0h~82A1h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write

Read/Write Port:82A2h~82A3h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write

Read/Write Port:82A4h~82A5h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write

Read/Write Port:82A6h~82A7h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read

Read/Write Port:82A8h~82A9h

Default: 00h

If Hardware Command Queue is enable, then

D[15:5] reserved

D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] **Head/Tail Index Bit[15:0]**

The Head Index is written into this register, and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write

Read/Write Port:82AAh

Default: 00h

D7 **Rectangular clipping mode**

0: Clipping internal region

1: Clipping external region

D6 **Rectangular Clipping Control**

0: Disable rectangular clipping logic

1: Enable rectangular clipping logic

D5 **Y direction control**

0: Y counter decrease

1: Y counter increase

D4 **X direction control**

0: X counter decrease

1: X counter increase

D[3:2] **Pattern select bit 1-0**

00: From background color registers

01: From foreground color registers

10: From pattern registers

11: Reserved

D[1:0] **Source select bit 1-0**

00: From background color registers

01: From foreground color registers

10: From video memory

11: From CPU-driven BitBlt source data

Command Register 1

Register Type: Read/Write

Read/Write Port:82ABh

Default: 00h

D7 **Hardware Command Queue status**

0: Hardware Command queue is not empty

1: Hardware Command queue is empty

D6 **Graphics engine status**

0: Graphics engine is idle and Hardware command queue is empty

1: Graphics engine is busy or Hardware command queue is not empty

D5 **Enhanced Color/Font Expansion**
0: Disable enhanced color expansion
1: Enable enhanced color expansion

D4 **Software Command Queue Status**
0: Software Command queue empty
1: Software Command queue not empty

D3 **Line drawing last pixel control**
0: Last pixel will be drawn
1: Last pixel will not be drawn

D2 **Line drawing major axial selection**
0: Y-axial is major
1: X-axial is major

D[1:0] **Command type select Bit[1:0]**
00: BitBlt
01: BitBlt with mask
10: Color/Font expansion
11: Line drawing

NOTE: Word_Writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

Pattern Register n

Register Type: Read/Write

Read/Write Port:82ACh-82EBh

Default: 00h

D[7:0] **For 256 color mode with BitBlt engine, these registers store the 8x8 color bitmap.**
For Color-Expansion, these registers store the monochrome bitmap, thus it can expand 512 pixels at a time.

Register Format for Line Drawing

The register format for Line-Drawing is shown in following table.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	IO Address
Reserved		X Start		8280h
Reserved		Y Start		8284h
Reserved		Reserved		8288h
Reserved		Major Axial Pixel Count		828Ch
FG Rop	FG (Foreground) Color			8290h

BG Rop	BG (Background) Color		8294h
K2 Term	K1 Term		8298h
Line Style	Error Term		829Ch
Top Clipping	Left Clipping		82A0h
Bottom Clipping	Right Clipping		82A4h
Command/Status	Reserved	Status 0	82A8h

X Start

Register Type: Read/Write

Read/Write Port:8280h~8281h

Default: 00h

D[15:12] Reserved

D[11:0] X Start Bit[11:0]

Y Start

Register Type: Read/Write

Read/Write Port:8284h~8285h

Default: 00h

D[15:12] Reserved

D[11:0] Y Start Bit[11:0]

Major Axial Pixel Count

Register Type: Read/Write

Read/Write Port:828Ch~828Dh

Default: 00h

D[15:12] Reserved

D[11:0] Major Axial Pixel Count Bit[11:0]

Foreground Color

Register Type: Read/Write

Read/Write Port:8290h~8292h

Default: 00h

D[23:0] Foreground Color Bit[23:0]

FG Rop

Register Type: Read/Write

Read/Write Port:8293h

Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

Background Color

Register Type: Read/Write

Read/Write Port:8294h~8296h

Default: 00h

D[23:0] Background Color Bit[23:0]

BG Rop

Register Type: Read/Write

Read/Write Port:8297h

Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

K1 Term

Register Type: Read/Write

Read/Write Port:8298h~8299h

Default: 00h

D[15:14] Reserved

D[13:0] K1 Term Bit[13:0]

K2 Term

Register Type: Read/Write

Read/Write Port:829Ah~829Bh

Default: 00h

D15:14] Reserved

D[13:0] K2 Term Bit[13:0]

Error Term

Register Type: Read/Write

Read/Write Port:829Ch~829Dh

Default: 00h

D[15:14] Reserved

D[13:0] Error Term Bit[13:0]

Line Style

Register Type: Read/Write

Read/Write Port:829Eh~829Fh

Default: 00h

D[15:0] Style Pattern Bit[15:0]

Left Clipping

Register Type: Read/Write

Read/Write Port:82A0h~82A1h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write

Read/Write Port:82A2h~82A3h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write

Read/Write Port:82A4h~82A5h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write

Read/Write Port:82A6h~82A7h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read/Write

Read/Write Port:82A8h~82A9h

Default: 00h

If Hardware Command Queue is enable, then

D[15:5] reserved

D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] **Head/Tail Index Bit[15:0]**
The Head Index is written into this register, and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write

Read/Write Port:82AAh

Default: 00h

D7 **Rectangular Clipping Mode**
0: Clipping internal region
1: Clipping external region

D6 **Rectangular Clipping Control**
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic

D5 **Y direction control**
0: Y counter decrease
1: Y counter increase

D4 **X direction control**
0: X counter decrease
1: X counter increase

D[3:2] **Pattern select bit 1-0**
00: From background color registers
01: From foreground color registers
10: From pattern registers
11: Reserved

D[1:0] **Source select bit 1-0**
00: From background color registers
01: From foreground color registers
10: From video memory
11: From CPU-driven BitBlt source data

Command Register 1

Register Type: Read/Write

Read/Write Port:82ABh

Default: 00h

D7 **Hardware Command Queue status**
0: Hardware Command queue is not empty
1: Hardware Command queue is empty

D6 **Graphics engine status**
0: Graphics engine is idle and Hardware command queue is empty
1: Graphics engine is busy or Hardware command queue is not empty

D5 **Enhanced Color/Font Expansion**
0: Disable enhanced color expansion
1: Enable enhanced color expansion

D4 **Software Command Queue Status**
0: Software Command queue empty
1: Software Command queue not empty

D3 **Line drawing last pixel control**
0: Last pixel will be drawn
1: Last pixel will not be drawn

D2 **Line drawing major axial selection**
0: Y-axial is major
1: X-axial is major

D[1:0] **Command type select bit 1-0**
00: Bitblt
01: BitBlt with mask
10: Color/Font expansion
11: Line drawing

NOTE: Word_writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

The Register Format for Direct Draw

The register format for Direct Draw is shown in following table.

D[31:24]	D[23:16]	D[15:08]	D[07:00]	IO Address
Reserved	Source Start Linear Address			8280h
Reserved	Destination Start Linear Address			8284h
Destination Pitch		Source Pitch		8288h
Rectangular Height		Rectangular Width		828Ch
S_Alpha Bit	High Value of Source Color Key			8290h
D_Alpha Bit	High value of Destination Color Key			8294h
D_Rop	Low Value of Source Color Key			8298h
Reserved	Low Value of Destination Color Key			829Ch
Top Clipping		Left Clipping		82A0h
Bottom Clipping		Right Clipping		82A4h
Command/Status		Command Queue Status		82A8h

Source Start Linear Address

Register Type: Read/Write

Read/Write Port:8280h~8283h

Default: 00h

D[31:22] Reserved

D[21:0] Source Start Linear Address Bit[21:0]

Destination Start Linear Address

Register Type: Read/Write

Read/Write Port:8284h~8287h

Default: 00h

D[31:22] Reserved

D[21:0] Destination Start Linear Address Bit[21:0]

Source Pitch

Register Type: Read/Write

Read/Write Port:8288h~8289h

Default: 00h

D[15:12] Reserved

D[11:0] Source Pitch Bit[11:0]

Destination Pitch

Register Type: Read/Write

Read/Write Port:828Ah~828Bh

Default: 00h

D[15:12] Reserved

D[11:0] Destination Pitch Bit[11:0]

Rectangular Width

Register Type: Read/Write

Read/Write Port:828Ch~828Dh

Default: 00h

D[15:12] Reserved

D[11:0] Destination Rectangular Width Bit[11:0]

Rectangular Height

Register Type: Read/Write

Read/Write Port:828Eh~828Fh

Default: 00h

D[15:12] Reserved

D[11:0] Destination Rectangular Height Bit[11:0]

High value of Source Color Key

Register Type: Read/Write

Read/Write Port:8290h~8292h

Default: 00h

D[23:0] High Value of Source Color Key Bit[23:0]

Alpha Blending Control Bit for Source Color (S_Alpha Bit)

Register Type: Read/Write

Read/Write Port:8293h

Default: 00h

D[7:1] Reserved

D0 Control Bit for Source Color Alpha Blending

High Value of Destination Color Key (D_Alpha Bit)

Register Type: Read/Write

Read/Write Port:8294h~8296h

Default: 00h

D[23:0] High Value of Destination Color Key Bit[23:0]

Alpha Blending Control Bit for Destination Color (D_Alpha Bit)

Register Type: Read/Write

Read/Write Port:8297h

Default: 00h

D[7:1] Reserved

D0 Control Bit for Destination Color Alpha Blending

Low Value of Source Color Key

Register Type: Read/Write

Read/Write Port:8298h~829Ah

Default: 00h

D[23:0] Low Value of Source Color Key Bit[23:0]

Direct Draw Rop (D_Rop)

Register Type: Read/Write

Read/Write Port:829Bh

Default: 00h

D[7:4] Reserved

D[3:0] Direct Draw Raster Operation Bit[3:0]

Low Value of Destination Color Key

Register Type: Read/Write

Read/Write Port:829Ch~829Fh

Default: 00h

D[23:0] Low Value of Destination Color Key Bit[23:0]

Left Clipping

Register Type: Read/Write

Read/Write Port:82A0h~82A1h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write

Read/Write Port:82A2h~82A3h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write

Read/Write Port:82A4h~82A5h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write

Read/Write Port:82A6h~82A7h

Default: 00h

D[15:12] Reserved

D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read/Write

Read/Write Port:82A8h~82A9h

Default: 00h

If Hardware Command Queue is enable, then

D[15:5] **reserved**

D[4:0] **Available Command Queue Length Bit[4:0]**

If Turbo Queue is enable, then

D[15:0] **Head/Tail Index Bit[15:0]**

The Head Index is written into this register, and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write

Read/Write Port:82AAh

Default: 00h

D7 **Rectangular Clipping Mode**

0: Clipping internal region

1: Clipping external region

D6 **Rectangular Clipping Control**

0: Disable rectangular clipping logic

1: Enable rectangular clipping logic

D5 **Y direction control**

0: Y counter decrease

1: Y counter increase

D4 **X direction control**

0: X counter decrease

1: X counter increase

D[3:2] **Direct Draw Enable**

00: Reserved

01: Reserved

10: Reserved

11: Enable Direct Draw

The two bits (D[3:2]) must be set to “11” then the Direct Draw function can be enabled.

D[1:0] **Source select bit 1-0**

00: From background color registers

01: From foreground color registers

10: From video memory

11: From CPU-driven BitBlt Source Data

Command Register 1

Register Type: Read/Write

Read/Write Port:82ABh

Default: 00h

D7 **Hardware Command Queue status**
0: Hardware Command queue is not empty
1: Hardware Command queue is empty

D6 **Graphics engine status**
0: Graphics engine is idle and Hardware command queue is empty
1: Graphics engine is busy or Hardware command queue is not empty

D5 **Enhanced Color/Font Expansion**
0: Disable enhanced color expansion
1: Enable enhanced color expansion

D4 **Software Command Queue Status**
0: Software Command queue empty
1: Software Command queue not empty

D3 **Line drawing last pixel control**
0: Last pixel will be drawn
1: Last pixel will not be drawn

D2 **Line drawing major axial selection**
0: Y-axial is major
1: X-axial is major

D[1:0] **Command type select bit 1-0**
00: Bitblt
01: BitBlt with mask
10: Color/Font expansion
11: Line drawing

NOTE: Word_writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

3.12 Video Accelerator Registers

Index(3D4)	**Video Acclerator Register (3D5)**
80h	Password/Identification Register
81h	Video Window Horizontal Display Start Low Register
82h	Video Window Horizontal Display End Low Register
83h	Video Window Horizontal Display Overflow Register
84h	Video Window Vertical Display Start Low Register
85h	Video Window Vertical Display End Low Register
86h	Video Window Vertical Display Overflow Register
87h	Video Capture Frame Buffer Starting Address Low Register
88h	Video Capture Frame Buffer Starting Address Middle Register
89h	Video Frame Buffer Overflow Register

8Ah	Video Display Frame Buffer Starting Address Low Register
8Bh	Video Display Frame Buffer Starting Address Middle Register
8Ch	Video Frame Buffer Offset Low Register
8Dh	Video Display Frame Buffer End Address Low Register
8Eh	Video Frame Buffer Offset Address High Register
8Fh	Video Capture Threshold Value Register
90h	Video Capture Horizontal Down Scaling Factor Register
91h	Video Capture Vertical Down Scaling Register
92h	Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register
93h	Vertical Up Scaling Factor Register
94h	Horizontal Scaling Factor Integer Register
95h	Video Overlay Color Key Blue Low Value Register
96h	Video Overlay Color Key Green Low Value Register
97h	Video Overlay Color Key Red Low Value Register
98h	Video Control Misc. Register 0
99h	Video Control Misc. Register 1
9Ah	Video Chroma Key B/Y Low Value Register
9Bh	Video Chroma Key G/U Low Value Register
9Ch	Video Chroma Key R/V Low Value Register
9Dh	Video Control Misc. Register 3
9Eh	Video Playback Threshold Low Value Register
9Fh	Video Playback Threshold High Value Register
A0h	Line Buffer Size Register
A1h	Video Overlay Color Key Blue High Value Register
A2h	Video Overlay Color Key Green High Value Register
A3h	Video Overlay Color Key Red High Value Register
A4h	Video Chroma Key B/Y High Value Register
A5h	Video Chroma Key G/U High Value Register
A6h	Video Chroma Key R/V High Value Register
A7h	Gaphics Data Alpha Value Register
A8h	Video Data Alpha Value Register
A9h	Key Overlay Operation Mode Register
AAh	Video Capture Horizontal Start Register

ABh	Video Capture Horizontal End Register
ACh	Video Capture Vertical Start Register
ADh	Video Capture Vertical End Register
AEh	Video Capture Horizontal Overflow Register
AFh	Video Capture Vertical Overflow Register
B0h	System Memory Video Frame Buffer Setting Register 1
B1h	System Memory Video Frame Buffer Setting Register 2
B2h	System Memory Video Frame Buffer Setting Register 3 and Video Control Register
B3h	Contrast Enhancement Mean Value Sampling Rate Factor Register
B4h	Brightness Register
B5h	Contrast Enhancement Control Register
B6h	Video Control Misc. Register 4

Password/Identification Register

Register Type: Read/Write

Read/Write Port:3D5, Index 80h

Default: 00h

D[7:0] Password/identification Bit[7:0]

Description:

If 86h is written to this register, A1h will be read from this register and all the video extension registers would be unlocked to allow desired change.

If any value other than 86h is written to this register, 21h will be read from this register and all the video extension registers would be locked to prevent unauthorized change.

Video Window Horizontal Display Start Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 81h

Default: 00h

D[7:0] Video window horizontal display start Bit[7:0]

Description:

The Video Window Horizontal Display Start Bit[10:0] form the left boundary of the video window. The Bit[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h, Sec. 5.9.4). The boundary is in unit of pixel.

Video Window Horizontal Display End Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 82h

Default: 00h

D[7:0] Video window horizontal display end Bit[7:0]

Description:

The Video Window Horizontal Display End Bit[10:0] form the right boundary of the video window. The Bit[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h, Sec. 5.9.4). The boundary is in unit of pixel.

Video Window Horizontal Display Overflow Register

Register Type: Read/Write

Read/Write Port:3D5, Index 83h

Default: 00h

D[2:0] Video window horizontal display start Bit[10:8]

D3 Reserved

D[6:4] Video window horizontal display end Bit[10:8]

D7 Reserved

Video Window Vertical Display Start Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 84h

Default: 00h

D[7:0] Video window vertical display start Bit[7:0]

Description:

The Video Window Vertical Display Start Bit[10:0] form the top boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h, Sec. 5.9.7). The boundary is in unit of pixel.

Video Window Vertical Display End Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 85h

Default: 00h

D[7:0] Video window vertical display end Bit[7:0]

Description:

The Video Window Vertical Display End Bit[10:0] form the bottom boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h, Sec. 5.9.7). The boundary is in unit of pixel.

Video Window Vertical Display Overflow Register

Register Type: Read/Write

Read/Write Port:3D5, Index 86h

Default: 00h

D[2:0] Video window horizontal display start Bit[10:8]

D3 Reserved

D[6:4] Video window horizontal display end Bit[10:8]

D7 Reserved

Video Capture Frame Buffer Starting Address Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 87h

Default: 00h

D[7:0] Video capture frame buffer starting address Bit[7:0]

Description:

The Video Capture Frame Buffer Starting Address Bit[19:0] form the video frame buffer starting address in unit of doubleword. The Bit[15:8] are located in the Video Capture Frame Buffer Starting Address Middle Register (Index 88h, Sec. 5.9.9). The Bit[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h, Sec. 5.9.10).

Video Capture Frame Buffer Starting Address Middle Register

Register Type: Read/Write

Read/Write Port:3D5, Index 88h

Default: 00h

D[7:0] Video capture frame buffer starting address Bit[15:8]

Video Frame Buffer Overflow Register

Register Type: Read/Write

Read/Write Port:3D5, Index 89h

Default: 00h

D[3:0] Video capture frame buffer starting address Bit[19:16]

D[7:4] Video display frame buffer starting address Bit[19:16]

Video Display Frame Buffer Starting Address Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 8Ah

Default: 00h

D[7:0] Video display frame buffer starting address Bit[7:0]

Description:

The Video Display Frame Buffer Starting Address Bit[19:0] form the video display starting address in unit of doubleword. The Bit[15:8] are located in the Video Display Frame Buffer Starting Address Middle Register (Index 8Bh, Sec. 5.9.12). The Bit[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h).

This address could be different from the video capture frame buffer starting address to perform the video display panning function.

Video Display Frame Buffer Starting Address Middle Register

Register Type: Read/Write

Read/Write Port:3D5, Index 8Bh

Default: 00h

D[7:0] Video display frame buffer starting address Bit[15:8]

Video Frame Buffer Offset Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 8Ch

Default: 00h

D[7:0] Video frame buffer offset Bit[7:0]

Description:

The Video Frame Buffer Offset Bit[11:0] form the offset of the video frame buffer. The Bit[11:8] are located in the Video Frame Buffer Offset High Register (Index 8Eh, Sec. 5.9.15).

The offset defines the size of the scan line of the video data captured in the video frame buffer in unit of double word. It should slightly larger than the actual size of captured video image to avoid the data over stored to next scan line buffer.

Video Display Frame Buffer End Address Low Register

Register Type: Read/Write

Read/Write Port:3D5, Index 8Dh

Default: 00h

D[7:0] Video display frame buffer end address Bit[7:0]

Description:

The Video Capture Frame Buffer End Address Bit[7:0] form the end address of the video frame buffer. The address is in unit of 16k bytes. This address defines the end address of the capture frame buffer. It can prevent the captured data to distory the other data outside the capture frame buffer when the video data input is unstable.

Video Frame Buffer Offset Address High Register

Register Type: Read/Write

Read/Write Port:3D5, Index 8Eh

Default: 00h

D[3:0] Video frame buffer offset Bit[11:8]

D[7:4] Reserved

Video Capture Threshold Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 8Fh

Default: 00h

D[2:0] Video capture threshold low Bit[2:0]

D3 Reserved

D[6:4] Video capture threshold high Bit[2:0]

D7 Reserved

Description:

This register contains the video capture FIFO threshold low and the video capture FIFO threshold high.

The threshold low defines the FIFO lower boundary which indicates the FIFO is full enough and the data in the FIFO can be written into the DRAM. But if the priority of the threshold low is lower than others, it can wait until it is able to write the data of FIFO into the DRAM.

The threshold high defines the FIFO upper boundary which indicates the FIFO is about to be overflow and the data of the FIFO mush be written into the DRAM as soon as possible.

These two thresholds should be modified to catch the maximum performance by compromising with the CRT threshold, video display threshold, and DRAM refresh rate, etc.

Video Capture Horizontal Down Scaling Factor Register

Register Type: Read/Write

Read/Write Port:3D5, Index 90h

Default: 00h

D[5:0] Video capture horizontal down scaling factor Bit[5:0]

D[7:6] Reserved

Description:

This register contains the video capture horizontal down scaling factor (HDSF). The horizontal size of the captured video frame will be scaled to (64-HDSF)/64. Since the scaled-down video frame maybe will not fit into the video display window, the margins outside the video display window will be cut off. This factor is not only used to fit the window size but also is used to reduce the bandwidth required for the video capture and video display.

Video Capture Vertical Down Scaling Register

Register Type: Read/Write

Read/Write Port:3D5, Index 91h

Default: 00h

D[5:0] Vertical down scaling factor Bit[5:0]

D[7:6] Reserved

Description:

This register contains the video capture vertical down scaling factor (VDSF). The vertical size of the captured video frame will be scaled to (64-VDSF)/64. Since the scaled-down video frame maybe will not fit into the video display window, the margins outside the video display window will be cut off. This factor is not only used to fit the window size but also is used to reduce the bandwidth required for the video capture and video display.

Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register

Register Type: Read/Write

Read/Write Port:3D5, Index 92h

Default: 00h

D[5:0] Horizontal up scaling factor Bit[5:0]

D[7:6] Horizontal up-scaling interpolation accuracy factor

00:replication
01:2-phase
10:4-phase
11:8-phase

Description:

This field contains the video playback horizontal up scaling factor fraction (HSFF). It is combined with the horizontal scaling factor integer (HSFI) register (Index 94h, Sec. 5.9.21) to form horizontal scaling. The horizontal size will be scaled to 1/(HSFI+(HSFF/64)). The HSFI should be zero for up-scaling. The HSFI should not be zero for down-scaling.

The Up-scaling interpolation accuracy factor can modify the up-scaling interpolation DDA accuracy phases.

Vertical Up Scaling Factor Register

Register Type: Read/Write

Read/Write Port:3D5, Index 93h

Default: 00h

D[5:0] Vertical up scaling factor Bit[5:0]

D[7:6] Video frame buffer data format selection Bit[1:0]

for YUV format,
00: UYVY 4:2:2
01: VYUY 4:2:2
10: YUYV 4:2:2
11: YVYU 4:2:2

for RGB format,
00: RGB 5:5:5
01: RGB 5:6:5

Description:

This field contains the video playback vertical up scaling factor (VUSF). The vertical size will be scaled to 64/VUSF. If VUSF=0, the vertical size will not be scaled.

Horizontal Scaling Factor Integer Register

Register Type: Read/Write

Read/Write Port:3D5, Index 94h

D[3:0] Horizontal Scaling Factor Integer Bit[3:0]

D[7:4] Reserved

Video Overlay Color Key Blue Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 95h

Default: 00h

D[7:0] Blue Key Bit[7:0]

Description:

This register contains the blue video overlay color key low value.

In 8-bit color mode, it is used as the color key low value.

In 16-bit color mode, it is used as the low byte of color key low value.

In 24-bit color mode, it is used as the blue byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the garphics data may be reaplaced by video data in the way defined by key operation mode.

Video Overlay Color Green Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 96h

Default: 00h

D[7:0] Green Key Bit[7:0]

Description:

This register contains the green video overlay color key low value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is used as the high byte of color key low value.

In 24-bit color mode, it is used as the green byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the garphics data may be reaplaced by video data in the way defined by key operation mode.

Video Overlay Color Red Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 97h

Default: 00h

D[7:0] Red Key Bit[7:0]

Description:

This register contains the red video overlay color key low value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is invalid.

In 24-bit color mode, it is used as the red byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the garphics data may be reaplaced by video data in the way defined by key operation mode.

Video Control Misc. Register 0

Register Type: Read/Write

Read/Write Port:3D5, Index 98h

Default: 00h

D0 Enable video capture

0: Disable video capture
1: Enable video capture

This bit could enable the video capture. If the video data is input through feature connector (FC), this bit should be set. The video pause function can be performed by disable this bit but enable the video playback bit.

D1 Enable video playback

0: Disable video playback
1: Enable video playback

This bit could enable the video playback. When the data of the video frame buffer are fetched by the system, the bandwidth of DRAM maybe not enough. The video playback can be disabled to gain the bandwidth but the video will not be played back.

D2 Reserved

D3 Reserved

D4 Video only display mode

0: Disable video only display mode
1: Enable video only display mode

The graphics display can be disable by setting this bit. This can reduce the DRAM bandwidth especially on the full screen video playback mode.

D5 **Video capture interlace control**
0: Disable video capture interlace control
1: Enable video capture interlace control

The video data input through feature connector could be interlaced. If the input video data are interlaced this bit should be set.

D6 **Video format selection**
0: Select RGB format
1: Select YUV format

This bit is used with the video frame buffer data format selection field of register CR92 to select the correct video data format.

D7 **Field Polarity Selection**
0: Select Odd/*Even
1: Select *Odd/Even
This bit can select the polarity of Field signal.

Video Control Misc. Register 1

Register Type: Read/Write

Read/Write Port:3D5, Index 99h

Default: 00h

D0 **Enable YUV data capture**
0: Capture RGB format video data
1: Capture YUV format video data
The video capture can be RGB and YUV format.

D1 **Enable dithering**
0: Disable dithering
1: Enable dithering
The captured video data can be dithered for better video quality.

D2 **Capture format select**
0: Format RGB 565
1: Format RGB 555
The capture video data may be RGB 555 or RGB565 format.

D[5:3] **Horizontal filter select**
000: 1
001: (1/8(1+3z-1+3z-2+z-3))
010: (1/4(1+2z-1+z-2))
011: (1/2(1+z-1))
others: Reserved

D6 **Enable vertical sync. interrupt**
0: Disable

1: Enable

The video input vertical sync. signal could cause interrupt when this bit is enabled.

D7 **Clear vertical sync. interrupt**

0: Disable

1: Enable

After the vertical sync. caused an interrupt, this bit should be set for clear the interrupt request.

Video Chroma Key B/Y Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 9Ah

Default: 00h

D[7:0] **Video Chroma B/Y Key Low Bit[7:0]**

Description:

This register contains the blue or Y video overlay chroma key low value.

In RGB chroma key mode, it is used as the blue byte of the chroma key low value.

In YUV chroma key mode, it is used as the Y of the chroma key low value.

If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be reaplaced graphics data in the way defined by key operation mode.

Video Chroma Key G/U Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 9Bh

Default: 00h

D[7:0] **Video Chroma G/U Key Low Bit[7:0]**

Description:

This register contains the green or U video overlay chroma key low value.

In RGB chroma key mode, it is used as the green byte of the chroma key low value.

In YUV chroma key mode, it is used as the U of the chroma key low value.

If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be reaplaced graphics data in the way defined by key operation mode.

Video Chroma Key R/V Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 9Ch

Default: 00h

D[7:0] **Video Chroma R/V Key Low Value Bit[7:0]**

Description:

This register contains the red or V video overlay chroma key low value.

In RGB chroma key mode, it is used as the red byte of the chroma key low value.

In YUV chroma key mode, it is used as the V of the chroma key low value.

If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be reaplaced graphics data in the way defined by key operation mode.

Video Control Misc. Register 3

Register Type: Read/Write

Read/Write Port:3D5, Index 9Dh

Default: 00h

D7 **Enable system memory video frame buffer**
0: Disable
1: Enable
The captured frame buffer can be placed on system memory.
But this mode can only be enabled under shared-memory architecture.

D6 **Support for Brooktree Bt819A video decoder SPI mode 1**
0: Disable
1: Enable

D[5:3] **Reserved**

D2 **Chroma Key Format selection**
0: RGB format
1: YUV format

D1 **UV format select for video playback**
0: CCIR 601 format
1: 2's complement format

D0 **UV format select for video capture**
0: CCIR 601 format
1: 2's complement format

Video Playback Threshold Low Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 9Eh

Default: 00h

D7 **Reserved**

D[6:0] **Video capture threshold low Bit[6:0]**

Description:

This register contains the video line buffer threshold low.

The threshold low defines the video line buffer lower boundary which indicates the line buffer is not enough and the video data should be read from the DRAM.

Video Playback Threshold High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index 9Fh

Default: 00h

D7 Reserved

D[6:0] Video capture threshold high Bit[6:0]

Description:

This register contains the video line buffer threshold high.

The threshold high defines the video line buffer upper boundary which indicates the data in the video line buffer is enough.

These two thresholds (video playback threshold low and threshold high) should be modified to get the maximum performance by compromising with the CRT threshold, video capture threshold, and DRAM refresh rate, etc.

Line Buffer Size Register

Register Type: Read/Write

Read/Write Port:3D5, Index A0h

Default: 00h

D[7:0] Line Buffer Size Bit[7:0]

Description:

This register should be set to the line buffer size used by playback. The size is in unit of quad-word.

Video Overlay Color Key Blue High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A1h

Default: 00h

D[7:0] Blue Key High Value Bit[7:0]

Description:

This register contains the blue video overlay color key high value.

In 8-bit color mode, it is used as the color key high value.

In 16-bit color mode, it is used as the low byte of color key high value.

In 24-bit color mode, it is used as the blue byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be reaplaced by video data in the way defined by key operation mode.

Video Overlay Color Key Green High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A2h

Default: 00h

D[7:0] Green Key High Value Bit[7:0]

Description:

This register contains the green video overlay color key high value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is used as the high byte of color key high value.

In 24-bit color mode, it is used as the green byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be reaplaced by video data in the way defined by key operation mode.

Video Overlay Color Key Red High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A3h

Default: 00h

D[7:0] Red Key High Value Bit[7:0]

Description:

This register contains the red video overlay color key high value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is invalid.

In 24-bit color mode, it is used as the red byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be reaplaced by video data in the way defined by key operation mode.

Video Chroma Key B/Y High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A4h

Default: 00h

D[7:0] Video Chroma B/Y Key High Value Bit[7:0]

Description:

This register contains the blue or Y video overlay chroma key high value.

In RGB chroma key mode, it is used as the blue byte of the chroma key high value.

In YUV chroma key mode, it is used as the Y of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be reaplaced by graphics data in the way defined by key operation mode.

Video Chroma Key G/U High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A5h

Default: 00h

D[7:0] Video Chroma G/U Key High Value Bit[7:0]

Description:

This register contains the green or U video overlay chroma key high value.

In RGB chroma key mode, it is used as the green byte of the chroma key high value.

In YUV chroma key mode, it is used as the U of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be reaplaced by graphics data in the way defined by key operation mode.

Video Chroma Key R/V High Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A6h

Default: 00h

D[7:0] Video Chroma R/V Key High Value Bit[7:0]

Description:

This register contains the red or V video overlay chroma key high value.

In RGB chroma key mode, it is used as the red byte of the chroma key high value.

In YUV chroma key mode, it is used as the V of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be reaplaced grphics data in the way defined by key operation mode.

Gaphics Data Alpha Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A7h

Default: 00h

D[7:0] Gaphics Data Alpha Value Bit[7:0]

Description:

The pixels of graphics data can be blended by graphics data alpha value, then added with the blended video data to generates blended data. The accuracy of the blending is 3 bits, the 3 MSBs of this register.

Video Data Alpha Value Register

Register Type: Read/Write

Read/Write Port:3D5, Index A8h

Default: 00h

D[7:0] Video Data Alpha Value Bit[7:0]

Description:

The pixels of video data can be blended by video data alpha value, then added with the blended graphics data to generates blended data. The accuracy of the blending is 3 bits, the 3 MSBs of this register.

Key Overlay Operation Mode Register

Register Type: Read/Write

Read/Write Port:3D5, Index A9h

Default: 00h

D[7:4] Reserved

D[3:0] Key Overlay Operation Mode Bit[3:0]

Description:

There are two keys for graphics data and video data overlay, which are color key and chroma key. The key overlay operation mode indicates the way the overlay would be performed.

Operation Mode	**Operation**
0000	always select graphics data
0001	select blended data when color key and chroma key,otherwise select graphics data
0010	select blended data when color key and not chroma key,otherwise select graphics data
0011	select blended data when color key,otherwise select graphics data
0100	select blended data when not color key and chroma key,otherwise select graphics data
0101	select blended data when chroma key,otherwise select graphics data
0110	select blended data when color key xor chroma key,otherwise select graphics data
0111	select blended data when color key or chroma key,otherwise select graphics data

1000	select blended data when not color key and not chroma key,otherwise select graphics data
1001	select blended data when color key xnor chroma key,otherwise select graphics data
1010	select blended data when not chroma key,otherwise select graphics data
1011	select blended data when color key or not chroma key,otherwise select graphics data
1100	select blended data when not chroma key,otherwise select graphics data
1101	select blended data when not color key or chroma key,otherwise select graphics data
1110	select blended data when not color key or not chroma key,otherwise select graphics data
1111	always select blended data

Video Capture Horizontal Start Register

Register Type: Read/Write

Read/Write Port:3D5, Index AAh

Default: 00h

D[7:0] Video Capture Horizontal Start Bit[7:0]

Description:

The Video Capture Horizontal Start Bit[10:0] indicate the left boundary of the captured video data. The Bit[10:8] is located in the Video Capture Horizontal Overflow Register (Sec. 5.9.47, Index AEh). The boundary is counted by the input video data clock. When the signal BLANK* is valid, the video data horizontal counter starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

Note: This register should be set to zero at Brooktree BT819A video decoder SPI mode 2.

Video Capture Horizontal End Register

Register Type: Read/Write

Read/Write Port:3D5, Index ABh

Default: 00h

D[7:0] Video Capture Horizontal End Bit[7:0]

Description:

The Video Capture Horizontal End Bit[10:0] indicate the right boundary of the captured video data. The Bit[10:8] is located in the Video Capture Horizontal Overflow Register (Sec. 5.9.47, Index AEh). The boundary is counted by the input video data clock. When the signal BLANK* is valid, the video data horizontal counter starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

Video Capture Vertical Start Register

Register Type: Read/Write

Read/Write Port:3D5, Index ACh

Default: 00h

D[7:0] Video Capture Vertical Start Bit[7:0]

Description:

The Video Capture Vertical Start Bit[9:0] indicate the upper boundary of the captured video data. The Bit[9:8] is located in the Video Capture Vertical Overflow Register (Sec. 5.9.48, Index AFh). The boundary is counted by the input video data clock. In the positive edge of the signal VDVSYNC, the video data vertical counter would be reset and then starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

Video Capture Vertical End Register

Register Type: Read/Write

Read/Write Port:3D5, Index ADh

Default: 00h

D[7:0] Video Capture Vertical End Bit[7:0]

Description:

The Video Capture Vertical End Bit[9:0] indicate the upper boundary of the captured video data. The Bit[9:8] is located in the Video Capture Vertical Overflow Register (Sec. 5.9.48, Index AFh). The boundary is counted by the input video data clock. In the positive edge of the signal VDVSYNC, the video data vertical counter would be reset and then starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

Video Capture Horizontal Overflow Register

Register Type: Read/Write

Read/Write Port:3D5, Index AEh

Default: 00h

D7 Reserved

D[6:4] Video Capture Horizontal End Bit[10:8]

D3 Reserved

D[2:0] Video Capture Horizontal Start Bit[10:8]

Video Capture Vertical Overflow Register

Register Type: Read/Write

Read/Write Port:3D5, Index AFh

Default: 00h

D7 Reserved

D[6:4] Video Data Input Delay Compensation Bit[2:0]

000: no delay
001: 2ns
010: 4ns
011: 6ns
100: inversed
101: 2ns, inversed
110: 4ns, inversed
111: 6ns, inversed

This field is programed for input video data clock and input video data delay compensation.

D[3:2] Video Capture Vertical End Bits[9:8]

D[1:0] Video Capture Vertical Start Bits[9:8]

System Memory Video Frame Buffer Setting Register 1

Register Type: Read/Write

Read/Write Port:3D5, Index B0h

Default: 00h

D[7:4] System Memory Video Frame Buffer Scambling Table Register Bit[3:0]

This field indicates the type of DRAM which the video frame buffer is located.

D[3:2] System Memory Video Frame Buffer Row Selection Register Bit[7:0]

00: Row Address [11:0]=memory address[20:9]

01: Row Address [11:0]=memory address[21:10]
10: Row Address [11:0]=memory address[22:11]
11: Row Address [11:0]=memory address[23:12]

D1 **Reserved**

D0 **Reserved**

System Memory Video Frame Buffer Setting Register 2

Register Type: Read/Write

Read/Write Port:3D5, Index B1h

Default: 00h

D[7:0] **System Memory Video Frame Buffer Segment Register Bit[7:0]**

The System Memory Video Frame Buffer Segment Register indicates the location of video frame buffer in one specified bank of DRAM. The unit is 256k in 32-bit DRAM bus. The unit is 512k in 64-bit DRAM bus.

System Memory Video Frame Buffer Setting Register 3 and Video Control Register

Register Type: Read/Write

Read/Write Port:3D5, Index B2h

Default: 00h

D7 **Enable Video Destination**
0: Disable
1: Enable

D6:5 **Reserved**

D4 **Support for Brooktree BT819A video decoder SPI mode 2**
0: Disable
1: Enable

D3 **Reserved**

D2 **System Memory Video Frame Buffer DRAM Type Selection**
0: Fast Page DRAM
1: EDO DRAM

D[1:0] **System Memory Video Frame Buffer RAS Selection Register Bit[1:0]**
00: Select RAS0
01: Select RAS1
10: Select RAS2
11: Select RAS3

Description:

The value of the System Memory Video Frame Buffer Setting Registers depends on the DRAM type, DRAM bank, and video frame buffer location.

Contrast Enhancement Mean Value Sampling Rate Factor Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B3h

Default: 00h

D[7:0] Contrast Enhancement Mean Value Sampling Rate Factor Bits[7:0]

Description:

The contrast enhancement needs brightness mean of each frame. This mean is calculated by sampling some pixels from one video frame. The sampling rate is "Contrast Enhancement Mean Value Sampling Rate Factor"/1024.

Brightness Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B4h

Default: 00h

D[7:0] Brightness Bit[7:0]

Description:

The Brightness is an 2's complement value from -128 to +127. This value is added with the video data to control the brightness of video.

Contrast Enhancement Control Register

Register Type: Read/Write

Read/Write Port: 3D5, Index B5h

Default: 00h

D[2:0] Contrast Gain Bits[2:0]

000: 1.0
001: 1.0625
010: 1.125
011: 1.1875
100: 1.25
101: 1.3125
110: 1.375
111: 1.4375

D[5:3] Contrast Mean Frame Samples Bits[2:0]

000: 2 frames
001: 4 frames
010: Reserved
011: 8 frames
100: Reserved
101: Reserved
110: Reserved

111: 16 frames

D[7:6] **Contrast Mean Pixel Samples Bits[1:0]**
00: 2048 pixels
01: 4096 pixels
10: 8192 pixels
11: 16384 pixels

Video Control Misc. Register 4

Register Type: Read/Write

Read/Write Port: 3D5, Index B6h

Default: 00h

D0 **CPU writing video data type**
0: RGB format
1: YUV format

D1 **CPU writing video data format**
0: RGB 555
1: RGB 565

D[2:7] **Reserved**

3.13 PCI Configuration Registers

Configuration Register 00h

Register Type: Read

Read Port: 0000h

Default: 02051039h

D[31:16] **Device ID**
SiS 6205 Device ID is 0205h

D[15:0] **Vendor ID**
Integrated Vendor ID is 1039h

Configuration Register 04h

Register Type: Read/Write

Read Port: 0004h

Default: 02000000h

D[26:25] **DEVSEL* timing (= 01, Read Only)**
00: fast
01: medium (fixed at this value)
10: slow

D5 **VGA Palette Snoop**

0:Disable
1:Enable

D1 **Memory Space**
0: Disable
1: Enable

D0 **I/O Space**
0:Disable
1:Enable

Configuration Register 08h

Register Type: Read
Read Port: 0008h
Default: 03000000h

D[31:8] **Class Code (= 030000h)**

D[7:0] **Revision ID (= Exh)**

Configuration Register 10h

Register Type: Read/Write
Read Port: 0010h
Default: 00000000h

D[31:0] **32-bit memory base register for 4MB linear frame buffer**

Configuration Register 14h

Register Type: Read/Write
Read Port: 0014h
Default: 00000000h

D[31:0] **32-bit memory base register for 64KB memory mapped I/O**

Configuration Register 2Ch

Register Type: Read/Write Once Only
Read Port: 002Ch
Default: 00000000h

D[31:16] **Subsystem ID**

D[15:0] **Subsystem Vendor**

Configuration Register 30h

Register Type: Read/Write
Read Port: 0030h
Default: 000C0000h

D[31:11] Expansion ROM Base Address

D0 ROM Enable Bit

0: Disable

1: Enable

Configuration Register 3Ch

Register Type: Read

Read Port: 003Ch

Default: 00000100h

If D3 of SRE is 1, then

D[15:8] Interrupt Pin (= 01h, Read Only)

D[7:0] Interrupt Line (= 00h)

If D3 of SRE is 0, then

D[15:8] Interrupt Pin (= 00h, Read Only)

D[7:0] Interrupt Line (= 00h)

4. Pin Assignment and Description

4.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AD28	AD26	AD27	AD31	MD3	MD7	MD11	MD14	MD18	MD21	MD25	MD29	MD32	MD35	MD39	MD43	MD46	MD50	MD53	MD57	MD61	MA1	MA4	MA8	MA10	CAS0#	A
B	AD25	AD24	AD29	MD0	MD4	MD8	MD12	MD15	MD19	MD22	MD26	MD30	MD33	MD36	MD40	MD44	MD47	MD51	MD54	MD58	MD62	MA2	MA5	MA7	MA9	MA11	B
C	AD23	AD22	AD30	MD1	MD5	MD9	MD13	MD16	MD20	MD23	MD27	MD31	MD34	MD37	MD41	MD45	MD48	MD52	MD55	MD59	MD63	MA3	MA6	CAS2#	CAS1#	RAMWE#	C
D	AD19	AD20	AD21	GND	MD2	MD6	MD10	DVCC	MD17	GND	MD24	MD28	VCC	GND	MD38	MD42	GND	MD49	DVCC	MD56	MD60	MA0	GND	CAS5#	CAS4#	CAS3#	D
E	AD16	AD17	AD18	AD15																			CAS6#	RAS1#	RAS0#	CAS7#	E
F	AD12	AD13	AD14	AD11																			RAS2#	TA0	TAGWE#	RAS3#	F
G	AD8	AD9	AD10	AD7																			TA1	TA4	TA3	TA2	G
H	AD4	AD5	AD6	VCC																			DVCC	TA7	TA6	TA5	H
I	AD1	AD2	AD3	AD0																			KWE0#/SRAS0#	KWE3#/SCAS1#	KWE2#/SRAS1#	KWE1#/SCAS0#	I
J	PREQ3#	PGNT2#	PGNT3#	GND																			GND	KWE6#/BWE#	KWE5#/KCE#	KWE4#	J
K	PCICLK	PGNT0#	PGNT1#	PREQ2#							GND	GND	GND	GND	GND	GND							VCC	ADSV#	ADSC#	KWE7#/GWE#	K
L	PCIRST	PREQ0#	PREQ1#	SIOGNT#							GND	GND	GND	GND	GND	GND							KRE#	HD2	HD1	HD0	L
M	PWRGD	PLOCK#	BREAK#/KBRST#/LLC1	VCC							GND	GND	GND	GND	GND	GND							GND	HD5	HD4	HD3	M
N	C/BE3#	SIOREQ#	WAKEUP1	GND							GND	GND	GND	GND	GND	GND							GND	HD8	HD7	HD6	N
O	C/BE0#	C/BE1#	C/BE2#	FRAME#							GND	GND	GND	GND	GND	GND							HD9	HD12	HD11	HD10	O
P	TRDY#	TURBO/WAKEUP0	IRDY#	DEVSEL#							GND	GND	GND	GND	GND	GND							HD13	HD16	HD15	HD14	P
Q	CPUCLK	PAR	STOP#	GND																			GND	HD19	HD18	HD17	Q
R	HSYNC	VSYNC	SMOUT0/INTA#	BLANK#																			HD20	HD23	HD22	HD21	R
S	REFCLK	VIDEO7	PCLK	VCC																			VCC3	HD26	HD25	HD24	S
T	VIDEO4	VIDEO5	VIDEO6	VIDEO3																			HD27	HD30	HD29	HD28	T
U	VIDEO0	VIDEO1	VIDEO2	ENDCLK																			HD31	HD34	HD33	HD32	U
V	DDCDAT	ENVIDEO	ENSYNC	DDCCLK																			HD35	HD38	HD37	HD36	V
W	BOUT	RSET	AVSS1	GND	KEN#	CACHE#	CPUHOLD	VCC3	HBE5#	GND	SMI#	HA29	VCC	GND	HA19	HA15	GND	HA8	VCC3	HD62	HD58	HD54	GND	HD41	HD40	HD39	W
X	GOUT	COMP	VREF	AVSS3	M/IO#	EADS#	HITM#	SMIACT#	INIT	HBE4#	HBE1#	STOPCLK#	HA28	HA25	HA22	HA18	HA14	HA11	HA7	HA4	HD61	HD57	HD53	HD50	HD42	HD43	X
Y	AVDD1	AVSS2	MFILTER	AVDD3	D/C#	BRDY#	BOFF#	CPURST	HBE7#	HBE3#	HBE0#	HA31	HA27	HA24	HA21	HA17	HA13	HA10	HA6	HA3	HD60	HD56	HD52	HD49	HD44	HD45	Y
Z	ROUT	VFILTER	AVDD2	ADS#	NA#	W/R#	CPUHLDA	FLUSH#/SMOUT1	HBE6#	HBE2#	A20M#	HA30	HA26	HA23	HA20	HA16	HA12	HA9	HA5	HD63	HD59	HD55	HD51	HD47	HD46	HD48	Z
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 4-1 SiS5596 Pin Assignment (Top View)

4.2 Pin Listing (Listed by pin order)

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
A1	AD28	I/O	5V	B07	MD12	I/O	3V/5V
A2	AD26	I/O	5V	B08	MD15	I/O	3V/5V
A3	AD27	I/O	5V	B09	MD19	I/O	3V/5V
A4	AD31	I/O	5V	B10	MD22	I/O	3V/5V
A05	MD03	I/O	3V/5V	B11	MD26	I/O	3V/5V
A06	MD07	I/O	3V/5V	B12	MD30	I/O	3V/5V
A07	MD11	I/O	3V/5V	B13	MD33	I/O	3V/5V
A08	MD14	I/O	3V/5V	B14	MD36	I/O	3V/5V
A09	MD18	I/O	3V/5V	B15	MD40	I/O	3V/5V
A10	MD21	I/O	3V/5V	B16	MD44	I/O	3V/5V
A11	MD25	I/O	3V/5V	B17	MD47	I/O	3V/5V
A12	MD29	I/O	3V/5V	B18	MD51	I/O	3V/5V
A13	MD32	I/O	3V/5V	B19	MD54	I/O	3V/5V
A14	MD35	I/O	3V/5V	B20	MD58	I/O	3V/5V
A15	MD39	I/O	3V/5V	B21	MD62	I/O	3V/5V
A16	MD43	I/O	3V/5V	B22	MA02	O	3V/5V
A17	MD46	I/O	3V/5V	B23	MA05	O	3V/5V
A18	MD50	I/O	3V/5V	B24	MA07	O	3V/5V
A19	MD53	I/O	3V/5V	B25	MA09	O	3V/5V
A20	MD57	I/O	3V/5V	B26	MA11	O	3V/5V
A21	MD61	I/O	3V/5V	C01	AD23	I/O	5V
A22	MA01	O	3V/5V	C02	AD22	I/O	5V
A23	MA04	O	3V/5V	C03	AD30	I/O	5V
A24	MA08	O	3V/5V	C04	MD01	I/O	3V/5V
A25	MA10	O	3V/5V	C05	MD05	I/O	3V/5V
A26	CAS0#	O	3V/5V	C06	MD09	I/O	3V/5V
B01	AD25	I/O	5V	C07	MD13	I/O	3V/5V
B02	AD24	I/O	5V	C08	MD16	I/O	3V/5V
B03	AD29	I/O	5V	C09	MD20	I/O	3V/5V
B04	MD0	I/O	3V/5V	C10	MD23	I/O	3V/5V
B05	MD04	I/O	3V/5V	C11	MD27	I/O	3V/5V
B06	MD08	I/O	3V/5V	C12	MD31	I/O	3V/5V

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
C13	MD34	I/O	3V/5V	D21	MD60	I/O	3V/5V
C14	MD37	I/O	3V/5V	D22	MA0	O	3V/5V
C15	MD41	I/O	3V/5V	D23	GND	-	-
C16	MD45	I/O	3V/5V	D24	CAS5#	O	3V/5V
C17	MD48	I/O	3V/5V	D25	CAS4#	O	3V/5V
C18	MD52	I/O	3V/5V	D26	CAS3#	O	3V/5V
C19	MD55	I/O	3V/5V	E01	AD16	I/O	5V
C20	MD59	I/O	3V/5V	E02	AD17	I/O	5V
C21	MD63	I/O	3V/5V	E03	AD18	I/O	5V
C22	MA03	O	3V/5V	E04	AD15	I/O	5V
C23	MA06	O	3V/5V	E23	CAS6#	O	3V/5V
C24	CAS2#	O	3V/5V	E24	RAS1#	O	3V/5V
C25	CAS1#	O	3V/5V	E25	RAS0#	O	3V/5V
C26	RAMWE#	O	3V/5V	E26	CAS7#	O	3V/5V
D01	AD19	I/O	5V	F01	AD12	I/O	5V
D02	AD20	I/O	5V	F02	AD13	I/O	5V
D03	AD21	I/O	5V	F03	AD14	I/O	5V
D04	GND	-	-	F04	AD11	I/O	5V
D05	MD02	I/O	3V/5V	F23	RAS2#	O	3V/5V
D06	MD06	I/O	3V/5V	F24	TA0	I/O	3V/5V
D07	MD10	I/O	3V/5V	F25	TAGWE#	O	5V
D08	DVCC	-	3V/5V	F26	RAS3#	O	3V/5V
D09	MD17	I/O	3V/5V	G01	AD08	I/O	5V
D10	GND	-	-	G02	AD09	I/O	5V
D11	MD24	I/O	3V/5V	G03	AD10	I/O	5V
D12	MD28	I/O	3V/5V	G04	AD07	I/O	5V
D13	VCC	-	-	G23	TA01	I/O	3V/5V
D14	GND	-	-	G24	TA04	I/O	3V/5V
D15	MD38	I/O	3V/5V	G25	TA03	I/O	3V/5V
D16	MD42	I/O	3V/5V	G26	TA02	I/O	3V/5V
D17	GND	-	-	H01	AD04	I/O	5V
D18	MD49	I/O	3V/5V	H02	AD05	I/O	5V
D19	DVCC	-	3V/5V	H03	AD06	I/O	5V
D20	MD56	I/O	3V/5V	H04	VCC	-	-

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage

H23	DVCC	-	3V/5V	K16	GND	-	-
H24	TA07	I/O	3V/5V	K23	VCC	-	-
H25	TA06	I/O	3V/5V	K24	ADSV#	O	3V
H26	TA05	I/O	3V/5V	K25	ADSC#	O	3V
I01	AD01	I/O	5V	K26	KWE7#/GWE#	O	3V
I02	AD02	I/O	5V	L01	PCIRST	O	5V
I03	AD03	I/O	5V	L02	PREQ0#	I	5V
I04	AD0	I/O	5V	L03	PREQ1#	I	5V
I23	KWE0#/SRAS0#	O	3V	L04	SIOGNT#	O	5V
I24	KWE3#/SCAS1#	O	3V	L11	GND	-	-
I25	KWE2#/SRAS1#	O	3V	L12	GND	-	-
I26	KWE1#/SCAS0#	O	3V	L13	GND	-	-
J01	PREQ3#	I	5V	L14	GND	-	-
J02	PGNT2#	O	5V	L15	GND	-	-
J03	PGNT3#	O	5V	L16	GND	-	-
J04	GND	-	-	L23	KRE#	O	3V
J23	GND	-	-	L24	HD02	I/O	3V
J24	KWE6#/BWE#	O	3V	L25	HD01	I/O	3V
J25	KWE5#/KCE#	O	3V	L26	HD0	I/O	3V
J26	KWE4#	O	3V	M01	PWRGD	I	5V
K01	PCICLK	I	5V	M02	PLOCK#	I	5V
K02	PGNT0#	O	5V	M03	BREAK#/KBRST#/LLC1	I	5V
K03	PGNT1#	O	5V	M04	VCC	-	-
K04	PREQ2#	I	5V	M11	GND	-	-
K11	GND	-	-	M12	GND	-	-
K12	GND	-	-	M13	GND	-	-
K13	GND	-	-	M14	GND	-	-
K14	GND	-	-	M15	GND	-	-
K15	GND	-	-	M16	GND	-	-

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
M23	GND	-	-	P03	IRDY#	I/O	5V

M24	HD05	I/O	3V	P04	DEVSEL#	I/O	5V
M25	HD04	I/O	3V	P11	GND	-	-
M26	HD03	I/O	3V	P12	GND	-	-
N01	C/BE3#	I/O	5V	P13	GND	-	-
N02	SIOREQ#	I	5V	P14	GND	-	-
N03	WAKEUP 1	I	5V	P15	GND	-	-
N04	GND	-	-	P16	GND	-	-
N11	GND	-	-	P23	HD13	I/O	3V
N12	GND	-	-	P24	HD16	I/O	3V
N13	GND	-	-	P25	HD15	I/O	3V
N14	GND	-	-	P26	HD14	I/O	3V
N15	GND	-	-	Q01	CPUCLK	I	5V
N16	GND	-	-	Q02	PAR	O	5V
N23	GND	-	-	Q03	STOP#	I/O	5V
N24	HD08	I/O	3V	Q04	GND	-	-
N25	HD07	I/O	3V	Q23	GND	-	-
N26	HD06	I/O	3V	Q24	HD19	I/O	3V
O01	C/BE0#	I/O	5V	Q25	HD18	I/O	3V
O02	C/BE1#	I/O	5V	Q26	HD17	I/O	3V
O03	C/BE2#	I/O	5V	R01	HSYNC	O	5V
O04	FRAME#	I/O	5V	R02	VSYNC	O	5V
O11	GND	-	-	R03	SMOUT0/INTA#	O	5V
O12	GND	-	-	R04	BLANK#	I/O	5V
O13	GND	-	-	R23	HD20	I/O	3V
O14	GND	-	-	R24	HD23	I/O	3V
O15	GND	-	-	R25	HD22	I/O	3V
O16	GND	-	-	R26	HD21	I/O	3V
O23	HD09	I/O	3V	S01	REFCLK	I	5V
O24	HD12	I/O	3V	S02	VIDEO7	I/O	5V
O25	HD11	I/O	3V	S03	PCLK	I/O	5V
O26	HD10	I/O	3V	S04	VCC	-	-
P01	TRDY#	I/O	5V	S23	VCC3	-	3V
P02	TURBO/WAKEUP0	I/O	5V	S24	HD26	I/O	3V

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
S25	HD25	I/O	3V	W09	HBE5#	I	3V

S26	HD24	I/O	3V	W10	GND	-	-
T01	VIDEO4	I/O	5V	W11	SMI#	O	3V
T02	VIDEO5	I/O	5V	W12	HA29	I/O	3V
T03	VIDEO6	I/O	5V	W13	VCC	-	-
T04	VIDEO3	I/O	5V	W14	GND	-	-
T23	HD27	I/O	3V	W15	HA19	I/O	3V
T24	HD30	I/O	3V	W16	HA15	I/O	3V
T25	HD29	I/O	3V	W17	GND	-	-
T26	HD28	I/O	3V	W18	HA08	I/O	3V
U01	VIDEO0	I/O	5V	W19	VCC3	-	3V
U02	VIDEO1	I/O	5V	W20	HD62	I/O	3V
U03	VIDEO2	I/O	5V	W21	HD58	I/O	3V
U04	ENDCLK	I	5V	W22	HD54	I/O	3V
U23	HD31	I/O	3V	W23	GND	-	-
U24	HD34	I/O	3V	W24	HD41	I/O	3V
U25	HD33	I/O	3V	W25	HD40	I/O	3V
U26	HD32	I/O	3V	W26	HD39	I/O	3V
V01	DDCDAT	I/O	5V	X01	GOUT	A.O	ANALOG
V02	ENVIDEO	I	5V	X02	COMP	A. I	ANALOG
V03	ENSYNC	I	5V	X03	VREF	A. I	ANALOG
V04	DDCCLK	I/O	5V	X04	AVSS3	-	-
V23	HD35	I/O	3V	X05	M/IO#	I	3V
V24	HD38	I/O	3V	X06	EADS#	O	3V
V25	HD37	I/O	3V	X07	HITM#	I	3V
V26	HD36	I/O	3V	X08	SMIACT#	I	3V
W01	BOUT	A.O	ANALOG	X09	INIT	O	5V
W02	RSET	A. I	ANALOG	X10	HBE4#	I	3V
W03	AVSS1	-	-	X11	HBE1#	I	3V
W04	GND	-	-	X12	STOPCLK#	O	3V
W05	KEN#	O	3V	X13	HA28	I/O	3V
W06	CACHE#	I	3V	X14	HA25	I/O	3V
W07	CPUHOLD	O	3V	X15	HA22	I/O	3V
W08	VCC3	-	3V	X16	HA18	I/O	3V

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
X17	HA14	I/O	3V	Y22	HD56	I/O	3V

X18	HA11	I/O	3V	Y23	HD52	I/O	3V
X19	HA07	I/O	3V	Y24	HD49	I/O	3V
X20	HA04	I/O	3V	Y25	HD44	I/O	3V
X21	HD61	I/O	3V	Y26	HD45	I/O	3V
X22	HD57	I/O	3V	Z01	ROUT	A. O	ANALOG
X23	HD53	I/O	3V	Z02	VFILTER	A. I	ANALOG
X24	HD50	I/O	3V	Z03	AVDD2	-	-
X25	HD42	I/O	3V	Z04	ADS#	I	3V
X26	HD43	I/O	3V	Z05	NA#	O	3V
Y01	AVDD1	-	-	Z06	W/R#	I/O	3V
Y02	AVSS2	-	-	Z07	CPUHLDA	I	3V
Y03	MFILTER	A. I	ANALOG	Z08	FLUSH#/ SMOUT1	O	3V
Y04	AVDD3	-	-	Z09	HBE6#	I	3V
Y05	D/C#	I	3V	Z10	HBE2#	I	3V
Y06	BRDY#	O	3V	Z11	A20M#	I/O	3V
Y07	BOFF#	O	3V	Z12	HA30	I/O	3V
Y08	CPURST	O	3V	Z13	HA26	I/O	3V
Y09	HBE7#	I	3V	Z14	HA23	I/O	3V
Y10	HBE3#	I	3V	Z15	HA20	I/O	3V
Y11	HBE0#	I	3V	Z16	HA16	I/O	3V
Y12	HA31	I/O	3V	Z17	HA12	I/O	3V
Y13	HA27	I/O	3V	Z18	HA09	I/O	3V
Y14	HA24	I/O	3V	Z19	HA05	I/O	3V
Y15	HA21	I/O	3V	Z20	HD63	I/O	3V
Y16	HA17	I/O	3V	Z21	HD59	I/O	3V
Y17	HA13	I/O	3V	Z22	HD55	I/O	3V
Y18	HA10	I/O	3V	Z23	HD51	I/O	3V
Y19	HA06	I/O	3V	Z24	HD47	I/O	3V
Y20	HA3	I/O	3V	Z25	HD46	I/O	3V
Y21	HD60	I/O	3V	Z26	HD48	I/O	3V

4.3 Pin Listing (listed by function order)

4.3.1 Host Bus Interface

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
A20M#	Z11	I/O	3V	HA24	Y14	I/O	3V
ADS#	Z04	I	3V	HA25	X14	I/O	3V
BOFF#	Y07	O	3V	HA26	Z13	I/O	3V
BRDY#	Y06	O	3V	HA27	Y13	I/O	3V
CACHE#	W06	I	3V	HA28	X13	I/O	3V
CPUCLK	Q01	I	5V	HA29	W12	I/O	3V
CPUHLDA	Z07	I	3V	HA30	Z12	I/O	3V
CPUHOLD	W07	O	3V	HA31	Y12	I/O	3V
D/C#	Y05	I	3V	HBE0#	Y11	I	3V
EADS#	X06	O	3V	HBE1#	X11	I	3V
HA3	Y20	I/O	3V	HBE2#	Z10	I	3V
HA04	X20	I/O	3V	HBE3#	Y10	I	3V
HA05	Z19	I/O	3V	HBE4#	X10	I	3V
HA06	Y19	I/O	3V	HBE5#	W09	I	3V
HA07	X19	I/O	3V	HBE6#	Z09	I	3V
HA08	W18	I/O	3V	HBE7#	Y09	I	3V
HA09	Z18	I/O	3V	HD0	L26	I/O	3V
HA10	Y18	I/O	3V	HD01	L25	I/O	3V
HA11	X18	I/O	3V	HD02	L24	I/O	3V
HA12	Z17	I/O	3V	HD03	M26	I/O	3V
HA13	Y17	I/O	3V	HD04	M25	I/O	3V
HA14	X17	I/O	3V	HD05	M24	I/O	3V
HA15	W16	I/O	3V	HD06	N26	I/O	3V
HA16	Z16	I/O	3V	HD07	N25	I/O	3V
HA17	Y16	I/O	3V	HD08	N24	I/O	3V
HA18	X16	I/O	3V	HD09	O23	I/O	3V
HA19	W15	I/O	3V	HD10	O26	I/O	3V
HA20	Z15	I/O	3V	HD11	O25	I/O	3V
HA21	Y15	I/O	3V	HD12	O24	I/O	3V
HA22	X15	I/O	3V	HD13	P23	I/O	3V
HA23	Z14	I/O	3V	HD14	P26	I/O	3V

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
HD15	P25	I/O	3V	HD43	X26	I/O	3V
HD16	P24	I/O	3V	HD44	Y25	I/O	3V

HD17	Q26	I/O	3V	HD45	Y26	I/O	3V
HD18	Q25	I/O	3V	HD46	Z25	I/O	3V
HD19	Q24	I/O	3V	HD47	Z24	I/O	3V
HD20	R23	I/O	3V	HD48	Z26	I/O	3V
HD21	R26	I/O	3V	HD49	Y24	I/O	3V
HD22	R25	I/O	3V	HD50	X24	I/O	3V
HD23	R24	I/O	3V	HD51	Z23	I/O	3V
HD24	S26	I/O	3V	HD52	Y23	I/O	3V
HD25	S25	I/O	3V	HD53	X23	I/O	3V
HD26	S24	I/O	3V	HD54	W22	I/O	3V
HD27	T23	I/O	3V	HD55	Z22	I/O	3V
HD28	T26	I/O	3V	HD56	Y22	I/O	3V
HD29	T25	I/O	3V	HD57	X22	I/O	3V
HD30	T24	I/O	3V	HD58	W21	I/O	3V
HD31	U23	I/O	3V	HD59	Z21	I/O	3V
HD32	U26	I/O	3V	HD60	Y21	I/O	3V
HD33	U25	I/O	3V	HD61	X21	I/O	3V
HD34	U24	I/O	3V	HD62	W20	I/O	3V
HD35	V23	I/O	3V	HD63	Z20	I/O	3V
HD36	V26	I/O	3V	HITM#	X07	I	3V
HD37	V25	I/O	3V	KEN#	W05	O	3V
HD38	V24	I/O	3V	M/IO#	X05	I	3V
HD39	W26	I/O	3V	NA#	Z05	O	3V
HD40	W25	I/O	3V	SMIACT#	X08	I	3V
HD41	W24	I/O	3V	W/R#	Z06	I/O	3V
HD42	X25	I/O	3V				

4.3.2 Secondary CACHE Interface

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
ADSC#	K25	O	3V	KWE7# /GWE#	K26	O	3V
ADSV#	K24	O	3V	TA0	F24	I/O	3V/5V
KRE#	L23	O	3V	TA01	G23	I/O	3V/5V
KWE0# /SRAS0#	I23	O	3V	TA02	G26	I/O	3V/5V
KWE1# /SCAS0#	I26	O	3V	TA03	G25	I/O	3V/5V
KWE2# /SRAS1#	I25	O	3V	TA04	G24	I/O	3V/5V
KWE3# /SCAS1#	I24	O	3V	TA05	H26	I/O	3V/5V
KWE4#	J26	O	3V	TA06	H25	I/O	3V/5V
KWE5# /KCE#	J25	O	3V	TA07	H24	I/O	3V/5V
KWE6# /BWE#	J24	O	3V	TAGWE#	F25	O	5V

4.3.3 DRAM Interface

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
CAS0#	A26	O	3V/5V	MD12	B07	I/O	3V/5V
CAS1#	C25	O	3V/5V	MD13	C07	I/O	3V/5V
CAS2#	C24	O	3V/5V	MD14	A08	I/O	3V/5V
CAS3#	D26	O	3V/5V	MD15	B08	I/O	3V/5V
CAS4#	D25	O	3V/5V	MD16	C08	I/O	3V/5V
CAS5#	D24	O	3V/5V	MD17	D09	I/O	3V/5V
CAS6#	E23	O	3V/5V	MD18	A09	I/O	3V/5V
CAS7#	E26	O	3V/5V	MD19	B09	I/O	3V/5V
MA0	D22	O	3V/5V	MD20	C09	I/O	3V/5V
MA01	A22	O	3V/5V	MD21	A10	I/O	3V/5V
MA02	B22	O	3V/5V	MD22	B10	I/O	3V/5V
MA03	C22	O	3V/5V	MD23	C10	I/O	3V/5V
MA04	A23	O	3V/5V	MD24	D11	I/O	3V/5V
MA05	B23	O	3V/5V	MD25	A11	I/O	3V/5V
MA06	C23	O	3V/5V	MD26	B11	I/O	3V/5V
MA07	B24	O	3V/5V	MD27	C11	I/O	3V/5V
MA08	A24	O	3V/5V	MD28	D12	I/O	3V/5V
MA09	B25	O	3V/5V	MD29	A12	I/O	3V/5V
MA10	A25	O	3V/5V	MD30	B12	I/O	3V/5V
MA11	B26	O	3V/5V	MD31	C12	I/O	3V/5V
MD0	B04	I/O	3V/5V	MD32	A13	I/O	3V/5V
MD01	C04	I/O	3V/5V	MD33	B13	I/O	3V/5V
MD02	D05	I/O	3V/5V	MD34	C13	I/O	3V/5V
MD03	A05	I/O	3V/5V	MD35	A14	I/O	3V/5V
MD04	B05	I/O	3V/5V	MD36	B14	I/O	3V/5V
MD05	C05	I/O	3V/5V	MD37	C14	I/O	3V/5V
MD06	D06	I/O	3V/5V	MD38	D15	I/O	3V/5V
MD07	A06	I/O	3V/5V	MD39	A15	I/O	3V/5V
MD08	B06	I/O	3V/5V	MD40	B15	I/O	3V/5V
MD09	C06	I/O	3V/5V	MD41	C15	I/O	3V/5V
MD10	D07	I/O	3V/5V	MD42	D16	I/O	3V/5V
MD11	A07	I/O	3V/5V	MD43	A16	I/O	3V/5V

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
MD44	B16	I/O	3V/5V	MD57	A20	I/O	3V/5V
MD45	C16	I/O	3V/5V	MD58	B20	I/O	3V/5V
MD46	A17	I/O	3V/5V	MD59	C20	I/O	3V/5V
MD47	B17	I/O	3V/5V	MD60	D21	I/O	3V/5V
MD48	C17	I/O	3V/5V	MD61	A21	I/O	3V/5V
MD49	D18	I/O	3V/5V	MD62	B21	I/O	3V/5V
MD50	A18	I/O	3V/5V	MD63	C21	I/O	3V/5V
MD51	B18	I/O	3V/5V	RAMWE#	C26	O	3V/5V
MD52	C18	I/O	3V/5V	RAS0#	E25	O	3V/5V
MD53	A19	I/O	3V/5V	RAS1#	E24	O	3V/5V
MD54	B19	I/O	3V/5V	RAS2#	F23	O	3V/5V
MD55	C19	I/O	3V/5V	RAS3#	F26	O	3V/5V
MD56	D20	I/O	3V/5V				

4.3.4 PCI Bus Interface

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
AD0	I04	I/O	5V	AD17	E02	I/O	5V
AD01	I01	I/O	5V	AD18	E03	I/O	5V
AD02	I02	I/O	5V	AD19	D01	I/O	5V
AD03	I03	I/O	5V	AD20	D02	I/O	5V
AD04	H01	I/O	5V	AD21	D03	I/O	5V
AD05	H02	I/O	5V	AD22	C02	I/O	5V
AD06	H03	I/O	5V	AD23	C01	I/O	5V
AD07	G04	I/O	5V	AD24	B02	I/O	5V
AD08	G01	I/O	5V	AD25	B01	I/O	5V
AD09	G02	I/O	5V	AD26	A02	I/O	5V
AD10	G03	I/O	5V	AD27	A03	I/O	5V
AD11	F04	I/O	5V	AD28	A01	I/O	5V
AD12	F01	I/O	5V	AD29	B03	I/O	5V
AD13	F02	I/O	5V	AD30	C03	I/O	5V
AD14	F03	I/O	5V	AD31	A04	I/O	5V
AD15	E04	I/O	5V	C/BE0#	O01	I/O	5V
AD16	E01	I/O	5V	C/BE1#	O02	I/O	5V

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
C/BE2#	O03	I/O	5V	PCICLK	K01	I	5V
C/BE3#	N01	I/O	5V	PCIRST	L01	O	5V
DEVSEL#	P04	I/O	5V	PLOCK#	M02	I	5V
FRAME#	O04	I/O	5V	STOP#	Q03	I/O	5V
IRDY#	P03	I/O	5V	TRDY#	P01	I/O	5V
PAR	Q02	O	5V				

4.3.5 PCI Arbiter Interface

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
PGNT0#	K02	O	5V	PREQ1#	L03	I	5V
PGNT1#	K03	O	5V	PREQ2#	K04	I	5V
PGNT2#	J02	O	5V	PREQ3#	J01	I	5V
PGNT3#	J03	O	5V	SIOGNT#	L04	O	5V
PREQ0#	L02	I	5V	SIOREQ#	N02	I	5V

4.3.6 VGA Controller Interface

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
BLANK#	R04	I/O	5V	ROUT	Z01	A. O	ANALOG
BOUT	W01	A.O	ANALOG	RSET	W02	A. I	ANALOG
COMP	X02	A. I	ANALOG	VFILTER	Z02	A. I	ANALOG
DDCCLK	V04	I/O	5V	VIDEO0	U01	I/O	5V
DDCDAT	V01	I/O	5V	VIDEO1	U02	I/O	5V
ENDCLK	U04	I	5V	VIDEO2	U03	I/O	5V
ENSYNC	V03	I	5V	VIDEO3	T04	I/O	5V
ENVIDEO	V02	I	5V	VIDEO4	T01	I/O	5V
GOUT	X01	A.O	ANALOG	VIDEO5	T02	I/O	5V
HSYNC	R01	O	5V	VIDEO6	T03	I/O	5V
MFILTER	Y03	A. I	ANALOG	VIDEO7	S02	I/O	5V
PCLK	S03	I/O	5V	VREF	X03	A. I	ANALOG
REFCLK	S01	I	5V	VSYNC	R02	O	5V

4.3.7 PMU & Misc.

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
BREAK#/ KBRST#/L LC1	M03	I	5V	SMI#	W11	O	3V
CPURST	Y08	O	3V	SMOUT0/IN TA#	R03	O	5V
FLUSH#/S MOUT1	Z08	O	3V	STOPCLK#	X12	O	3V
INIT	X09	O	5V	TURBO/WA KEUP0	P02	I/O	5V
PWRGD	M01	I	5V	WAKEUP1	N03	I	5V

4.3.8 Power Pin

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage
AVDD1	Y01	-	-	GND	K16	-	-
AVDD2	Z03	-	-	GND	L11	-	-
AVDD3	Y04	-	-	GND	L12	-	-
AVSS1	W03	-	-	GND	L13	-	-
AVSS2	Y02	-	-	GND	L14	-	-
AVSS3	X04	-	-	GND	L15	-	-
DVCC	D08	-	3V/5V	GND	L16	-	-
DVCC	D19	-	3V/5V	GND	M11	-	-
DVCC	H23	-	3V/5V	GND	M12	-	-
GND	D04	-	-	GND	M13	-	-
GND	D10	-	-	GND	M14	-	-
GND	D14	-	-	GND	M15	-	-
GND	D17	-	-	GND	M16	-	-
GND	D23	-	-	GND	M23	-	-
GND	J04	-	-	GND	N04	-	-
GND	J23	-	-	GND	N11	-	-
GND	K11	-	-	GND	N12	-	-
GND	K12	-	-	GND	N13	-	-
GND	K13	-	-	GND	N14	-	-
GND	K14	-	-	GND	N15	-	-
GND	K15	-	-	GND	N16	-	-

Pin No.	Signal	Type	Voltage	Pin No.	Signal	Type	Voltage

GND	N23	-	-	GND	W04	-	-
GND	O11	-	-	GND	W10	-	-
GND	O12	-	-	GND	W14	-	-
GND	O13	-	-	GND	W17	-	-
GND	O14	-	-	GND	W23	-	-
GND	O15	-	-	VCC	D13	-	-
GND	O16	-	-	VCC	H04	-	-
GND	P11	-	-	VCC	K23	-	-
GND	P12	-	-	VCC	M04	-	-
GND	P13	-	-	VCC	S04	-	-
GND	P14	-	-	VCC	W13	-	-
GND	P15	-	-	VCC3	S23	-	3V
GND	P16	-	-	VCC3	W08	-	3V
GND	Q04	-	-	VCC3	W19	-	3V
GND	Q23	-	-				

4.4 Pin Description

4.4.1 Host Interface

Pin No.	Symbol	Type	Function
Z4	ADS#	I	Address Status is driven by the CPU to indicate the start of a CPU bus cycle.
X5	M/IO#	I	Memory I/O definition is an input to indicate an I/O cycle when low, or a memory cycle when high.
Y5	D/C#	I	Data/Code is used to indicate whether the current cycle is a data or code access.
Z6	W/R#	I/O	Write/Read from the CPU indicates whether the current cycle is a write or read access. It is an output during the PCI master cycles.
W6	CACHE#	I	The Cache pin indicates an L1 internally cacheable read cycle or a burst write-back cycle. If this pin is driven inactive during a read cycle, the CPU will not cache the returned data, regardless of the state of the KEN# pin.

Pin No.	**Symbol**	**Type**	**Function**
Y20, X20, Z19, Y19, X19, W18, Z18, Y18, X18, Z17, Y17, X17, W16, Z16, Y16, X16, W15, Z15, Y15, X15, Z14, Y14, X14, Z13, Y13, X13, W12, Z12, Y12	HA[31:3]	I/O	The CPU Address is driven by the CPU during CPU bus cycles. The SiS5596 forwards it to either the DRAM or the PCI bus depending on the address range. The address bus is driven by the SiS5596 during bus master cycles.
Y11, X11, Z10, Y10, X10, W9, Z9, Y9,	HBE[7:0]#	I	CPU Byte Enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. HBE7# indicates that the most significant byte of the data bus is valid while HBE0# indicates that the least significant byte of the data bus is valid.

Pin No.	Symbol	Type	Function
L24-L26, M24-M26, N24-N26, O23-O26, P23-P26, Q24-Q26, R23-R26, S24-S26, T23-T26, U23-U26, V23-V26, W24-W26, X25, X26, Y25, Y26, Z24-Z26, Y24, X24, Z23, Y23, X23, W23, Z23, Y23, X23, W22, Z22, Y22, X22, W21, Z21, Y21, X21, W20, Z20	HD[63:0]	I/O	Host Data Bus
W7	CPUHOLD	O	CPU Hold Request is used to request the control of the CPU bus. CPUHLDA will be asserted by the CPU after completing the current bus cycle.
Z7	CPUHLDA	I	CPU Hold Acknowledge comes from the CPU in response to a CPUHOLD request. It is active high and remains driving during bus hold period. The assertion of CPUHLDA indicates that the CPU has relinquished the control of the host bus.
Y6	BRDY#	O	Burst Ready indicates that data presented are valid during a burst cycle.
Z5	NA#	O	The SiS5596 can assert NA# when the asynchronous, burst, or pipelined burst SRAMs are used to request Host generating the next address.
W5	KEN#	O	The CPU Cache Enable pin is used when the current cycle is cacheable to the L1 cache of the CPU. It is an active low signal asserted by the SiS5596 during cacheable cycles.

Pin No.	Symbol	Type	Function
X6	EADS#	O	The EADS# is driven to indicate that a valid external address has been driven to the CPU address pins to be used for an inquire cycle.
X7	HITM#	I	Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of the CPU.
Y7	BOFF#	O	The SiS5596 asserts BOFF# to stop the current CPU cycle.
X8	SMIACT#	I	The SMIACT# pin is used as the SMI acknowledgment input from the CPU to indicate that the SMI# is being acknowledged and the processor is operating in System Management Mode(SMM).
Q1	CPUCLK	I	CPU clock input runs at the frequency and skew equal to those of the CPU clock.

4.4.2 Reset Interface

Pin No.	Symbol	Type	Function
M1	PWRGD	I	Power Good is a power on reset and push button reset input.
L1	PCIRST#	O	The PCI Reset forces the PCI devices to a known state.
Y8	CPURST	O	Reset CPU is an active high output to reset the CPU.
X9	INIT	O	The Initialization output forces the CPU to begin execution in a known state. The CPU state after INIT is the same as the state after CPURST except that the internal caches, model specific registers, and floating point registers retain the values they had prior to INIT.
Z11	A20M#	I/O	A20 Mask is the fast A20GATE output to the CPU. It remains high during power up and CPU reset period. It forces A20 to go low when active.

4.4.3 PMU & Misc

Pin No.	Symbol	Type	Function
W11	SMI#	O	System Management Interrupt is used to indicate the occurrence of system management events. It is connected directly to the CPU SMI# input.
X12	STPCLK#	O	Stop Clock indicates a stop clock request to the CPU.

Pin No.	Symbol	Type	Function
Z8	FLUSH#/SMOUT1	O	When this pin is programmed as FLUSH#, it is used to slow down the system in deturbo mode. When this pin is SMOUT, it is used to control external device.
M3	BREAK#/KBRST#/LLC1	I	When the break switch enable bit is set, the KBRST# will be disabled. A signal from the break switch will cause the system enter the standby state. It can be programmed to pixel clock for SA7110.
N3	WAKEUP1	O	When this input is activated, the 5596 will reload the system standby timer. If it is inactive and the system standby timer expires, the system will enter system standby state. During the system standby state, if this input becomes active, the system will wake up from standby state and return back to normal state.
P2	TURBO/WAKEUP0	I	This pin is used to slow down the system by connecting it to ground or act as wakeup input signal.
R3	SMOUT0/INTA#	I/O	This pin can be used as SMOUT to control external device. PCI Interrupt indicates the interrupt signal generated by VGA Controller.

4.4.4 Cache & DRAM Interface

Pin No.	Symbol	Type	Function
K25	ADSC#	O	Cache address strobe for pipelined burst SRAM.
K24	ADSV#	O	Cache address advance for pipelined burst SRAM.
L23	KRE#	O	Cache Read Enable for standard SRAM, or Cache Output Enable for burst and pipelined burst SRAM.
I23	KWE0# /SRAS0#	O	Cache write enable signal multiplexed with RAS signal of SDRAM (Next Version)
I26	KWE1# /SCAS0#	O	Cache write enable signal multiplexed with CAS signal of SDRAM (Next Version)
I25	KWE2# /SRAS1#	O	Cache write enable signal multiplexed with RAS signal of SDRAM (Next Version)
I24	KWE3# /SCAS1#	O	Cache write enable signal multiplexed with CAS signal of SDRAM (Next Version)
J26	KWE4#/	O	Cache write enable signal
J25	KWE5# /KCE#	O	Cache write enable signal multiplexed with cache chip enable signal of pipeline burst SRAM (Next Version)

Pin No.	Symbol	Type	Function
J24	KWE6# /BWE#	O	Cache write enable signal multiplexed with byte write enable signal of pipeline burst SRAM (Next Version)
K26	KWE7# /GWE#	O	Cache write enable signal multiplexed with global write enable signal of pipeline burst SRAM (Next Version)
F24, G23-G26, H24-H26	TA[7:0]	I/O	TAG RAM data bus lines.
F25	TAGWE#	O	TAG RAM write enable output.
E25, E24, F23, F26	RAS[3:0]#	O	Row Address Strobe. Each Row address strobe output signal corresponds to 7:0. DRAM of eight bytes respectively. These signals are used to latch the row addresses on the MA[11:0] bus into the DRAMs.
A26, C25, C24, D24-D26, E23, E26	CAS[7:0]	O	Column Address Strobe. They are the DRAM data output enable signals for bytes 7~0 respectively.
C26	RAMWE#	O	RAM Write is an active low output signal to enable local DRAM writes.
D22, A22, B22, C22, A23, B23, C23, A24, B24, B25, A25, A26	MA[11:0]	O	Memory address [11:0] are the row and column addresses for DRAM.

Pin No.	Symbol	Type	Function
B4, C4, D5, A5, B5, C5, D6, A6, B6, C6, D7, A7, B7, C7, A8, B8, C8, D9, A9, B9, C9, A10, B10, C10, D11, A11, B11, C11, D12, A12, B12, C12, A13, B13, C13, A14, B14, C14, D15, A15, B15, C15, D16, A16, B16, C16, A17, B17, C17, D18, A18, B18, C18, A19, B19, C19, D20, A20, B20, C20, D21, A21, B21, C21,	MD[63:0]	I/O	Memory Data Bus

4.4.5 PCI Host Bridge

Pin No.	Symbol	Type	Function
I1-I4, H1-H3, G1-G4, F1-F4, E1-E4, D1-D3, C2, C1, B2, B1, A1-A3, B3, C3, A4	AD[31:0]	I/O	PCI Address /Data BusIn address phase:1.When the SiS5596 is a PCI bus master, AD[31:0] are output signals.2.When the SiS5596 is a PCI target, AD[31:0] are input signals.In data phase:1.When the SiS5596 is a target of a memory read/write cycle, AD[31:0] are floating.2.When the SiS5596 is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.

Pin No.	Symbol	Type	Function
O1-O3, N1	C/BE[3:0]#	I/O	PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS5596 is a PCI bus master and inputs when it is a PCI slave.
O4	FRAME#	I/O	FRAME# is an output when the SiS5596 is a PCI bus master. The SiS5596 drives FRAME# to indicate the beginning and duration of an access. When the SiS5596 is a PCI slave, FRAME# is an input signal.
P3	IRDY#	I/O	IRDY# is an output when the SiS5596 is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS5596 is a PCI slave, IRDY# is an input.
P1	TRDY#	I/O	TRDY# is an output when the SiS5596 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS5596 is a PCI master, it is an input.
Q3	STOP#	I/O	STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.
P4	DEVSEL#	I/O	The SiS5596 drives DEVSEL# based on the DRAM address range being accessed by a PCI bus master or if the current configuration cycle is to the SiS5596. As an input it indicates if any device has responded to current PCI bus cycle initiated by the SiS5596.
M2	PLOCK#	I	PCI Lock indicates an exclusive bus operation that may require multiple transactions to complete. When PLOCK# is sampled asserted at the beginning of a PCI cycle, the SiS5596 considers itself a locked resource and remains in the locked state until PLOCK# is sampled negated on a new PCI cycle.

Pin No.	Symbol	Type	Function
Q2	PAR	O	Parity is an even parity generated across AD[31:0] and C/BE[3:0]#.
K1	PCICLK	I	The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS5596. It runs at the same frequency and skew of the PCI local bus.

4.4.6 PCI Bus Arbiter

Pin No.	Symbol	Type	Function
L2, L3, K4, J1	PREQ[3:0]#	I	PCI Bus Request is used to indicate to the PCI bus arbiter that an agent requires use of the PCI bus.
K2, K3, J2, J3	PGNT[3:0]#	O	PCI Bus Grant indicates to an agent that access to the PCI bus has been granted.
L4	SIOREQ#	I	SIO Request from the SiS5513 to request the PCI bus.
N2	SIOGNT#	O	SIO Grant. When asserted, SIOGNT# indicates that the PCI arbiter has granted use of the bus to the SiS5513.

4.4.7 Graphic Controller

Pin No.	Symbol	Type	Function
R1	HSYNC	O	Horizontal Sync
R2	VSYNC	O	Vertical Sync
R4	BLANK	I/O	Blank Video signal
S3	PCLK	I/O	Pixel Clock
S2, T3, T2, T1, T4, U3, U2, U1	VIDEO[7:0]	I/O	Video Data Bus
V1	DDCDAT	I/O	Display Data Channel Data Line
V4	DDCCLK	I/O	Display Data Channel Clock Line
V3	ENSYNC	I	Enable Sync Output
V2	ENVIDEO	I	Enable Video Data Output
U4	ENDCLK	I	Enable Video Clock Output
S1	REFCLK	I	Reference Clock 14.318 MHz
Z1	ROUT	A. O	Red Video Signal Output

Pin No.	Symbol	Type	Function
X1	GOUT	A. O	Green Video Signal Output
W1	BOUT	A. O	Blue Video Signal Output
X2	COMP	A. I	Compensation PinBypass this pin with an external 0.1 uF capacitor to AVDD.
W2	RSET	A. I	Reference ResistorAn external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
X3	VREF	A. I	Voltage ReferenceIf an external voltage is used, it must supply this input with a 1.235V reference.
Y3	MFILTER	A. I	Memory Clock Filter
Z2	VFILTER	A. I	Video Clock Filter

NOTE: A. I: Analog Input; A. O: Analog Output

4.4.8 Power and Ground

Pin No.	Symbol	Type	Function
D4, D10, D14, D17, D23, J4, J23, M23 N4, N23, O23, Q4, Q23, Q24, W4, W10, W14, W17, W23,K11-K16,L11-L16, M11-M16, N11-N16, O11-O16, P11-P16	GND	-	Ground
D13, H4, K23, M4, S4, W13	VCC (5V)	-	+5V DC Power
S23, W8, W19	VCC3 (3V)	-	+3V DC Power
D8, D19, H23	DVCC (3V/5V)	-	Power Signals for DRAM Interface. Connected to +5V DC Power for 5V DRAM, while connected to +3V DC power for 3V DRAM.

Pin No.	**Symbol**	**Type**	**Function**
Y1	AVDD1	-	Analog Power
Z3	AVDD2	-	Analog Power for Clock Gen
Y4	AVDD3	-	Analog Power for Clock Gen
W3	AVSS1	-	Analog Grand
Y2	AVSS2	-	Analog Grand for Clock Gen
X4	AVSS3	-	Analog Grand for Clock Gen

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient operation temperature	0	70	0C
Storage temperature	-40	125	0C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V

NOTE:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

5.2 DC Characteristics (I)

Table 5-1 DC Characteristics

Ta= 0 - 70^{0}C, Gnd= 0V, Vcc5= 5V$\pm$5%, Vcc3=3.3V$\pm$5%, Vcc35=3.3/5V$\pm$5%

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Note 1, V_{CC3}=3.3V$\pm$5%
V_{IH1}	Input High Voltage	2.2	V_{CC3}+0.3	V	Note 1
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2
V_{IH2}	Input High Voltage	2.2	V_{CC5}+0.3	V	Note 2
V_{T1-}	Schmitt Trigger Threshold	1.6		V	Note 3
	Voltage Falling Edge				
V_{T1+}	Schmitt Trigger Threshold	3.2	V		Note 3
	Voltage Rising Edge				
V_{H1}	Hysteresis Voltage	0.3	1.2	V	Note 3
V_{OL1}	Output Low Voltage		0.45	V	Note 4
V_{OH1}	Output High Voltage	2.4		V	Note 4
V_{OL2}	Output Low Voltage		0.4	V	Note 5
V_{OH2}	Output High Voltage	2.0	2.4	V	Note 5
V_{OL3}	Output Low Voltage		0.4	V	Note 6
V_{OH3}	Output High Voltage	2.0	V_{CC35}	V	Note 6
I_{OL1}	Output Low Current	8		mA	Note 7

I_{OH1}	Output High Current	-8		mA	Note 7
I_{OL2}	Output Low Current	4, 8		mA	Note 8, 12
I_{OH2}	Output High Current	-4,-8		mA	Note 8, 12
I_{OL3}	Output Low Current	16		mA	Note 9
I_{OH3}	Output High Current	-16		mA	Note 9
I_{OL4}	Output Low Current	8,12		mA	Note 10, 12
I_{OH4}	Output High Current	-8,-12		mA	Note 10, 12
I_{OL5}	Output Low Current	4		mA	Note 11
I_{OH5}	Output high Current	-4		mA	Note 11
I_{IH}	Input Leakage Current		-10	mA	
I_{IL}	Input Leakage Current		+10	mA	
C_{IN}	Input Capacitance		12	pF	Fc=1 Mhz
C_{OUT}	Output Capacitance		12	pF	Fc=1 Mhz
$C_{I/O}$	I/O Capacitance		12	pF	Fc=1 Mhz

NOTE:

1. V_{IL1} and V_{IH1} are applicable to the following signals: HA[31:3], W/R#, HBE[7:0]#, HITM#, D/C#, ADS#, CPUHLDA, SMIACT#, CACHE#, M/IO#, HD[63:0]
2. V_{IL2} and V_{IH2} are applicable to the following signals: AD[31:0], C/BE[3:0]#, REQ[3:0]#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, LOCK#, PCICLK, PHOLD#, WAKEUP1,BREAK#, OSC, CPUCLK
3. V_{T1-}, V_{T1+} and V_{H1} are applicable to PWRGD
4. V_{OL1} and V_{OH1} are applicable to the following signals: AD[31:0], C/BE[3:0]#, GNT[3:0]#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, PHLDA#,SMOUT, PAR, PCIRST
5. V_{OL2} and V_{OH2} are applicable to the following signals: HA[31:3], W/R#,ADSC#, ADSV#, KWE[7:0]#, KRE#, STPCLK#,INIT, SMI#, A20M#, CPURST, EADS#, CPUHLDA, NA#, BRDY#, KEN#, BOFF#
6. V_{OL3} and V_{OH3} are applicable to the following signals: RAS[3:0]#, CAS[7:0]#, TA[7:0], MD[63:0], RAMW#, MA[11:0]
7. I_{OL1} and I_{OH1} are applicable to the following signals: AD[31:0], C/BE[3:0]#, GNT[3:0]#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, PHLDA#,SMOUT, PAR, PCIRST
8. I_{OL2} and I_{OH2} are applicable to the following signals: CAS[7:0]#
9. I_{OL3} and I_{OH3} are applicable to the following signals: ADSC#, ADSV#, KWE[7:0]#

10. I_{OL4} and I_{OH4} are applicable to the following signals: RAS[3:0]#

11. I_{OL5} and I_{OH5} are applicable to the following signals: KRE#, STPCLK#, INIT, SMI#, HA[31:3], W/R#, EADS#, NA#, BRDY#, KEN#, A20M#,BOFF#, CPURST, CPUHLDA.

12. The driving current of CAS[7:0]# and RAS[3:0]# are programmed. Please refer to register description.

5.3 AC Characteristics (I)

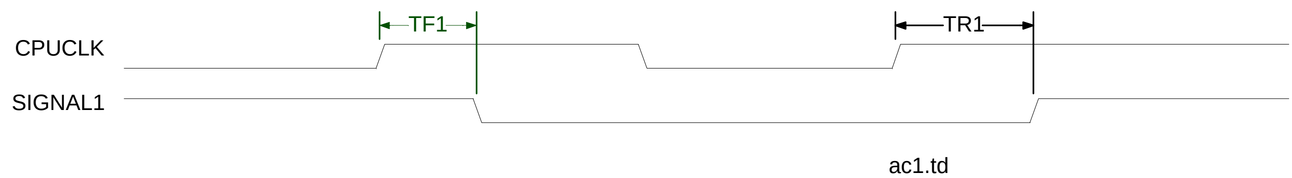
Table 5-2 AC Characteristics

Sym	Parameter	Typ	Max	Unit	CL
T1	BRDY# Active delay from CPUCLK	8	10	ns	35pf
T2	BRDY# Inactive delay from CPUCLK	9	12	ns	35pf
T3	KEN# Active delay from CPUCLK	6	8	ns	35pf
T4	KEN# Inactive delay from CPUCLK	6	8	ns	35pf
T5	NA# Active delay from CPUCLK	7	9	ns	35pf
T6	NA# Inactive delay from CPUCLK	8	10	ns	35pf
T7	EADS# Active delay from CPUCLK	6	8	ns	35pf
T8	EADS# Inactive delay from CPUCLK	6	8	ns	35pf
T9	CPUHOLD Active delay from CPUCLK	7	9	ns	35pf
T10	CPUHOLD Inactive delay from CPUCLK	6	8	ns	35pf
T11	CPURST Inactive delay from CPUCLK	7	9	ns	35pf
T12	CPURST High Pulse Width	33	43	CPUCLK	35pf
T13	KRE# Active delay from CPUCLK	8	11	ns	90pf
T14	KRE# Inactive delay from CPUCLK	10	12	ns	90pf
T15	KWE[7:0]# Active delay from CPUCLK	7	9	ns	35pf
T16	KWE[7:0]# Inactive delay from CPUCLK	6	8	ns	35pf
T17	ADSC# Low Valid delay from CPUCLK	9	11	ns	90pf
T18	ADSC# High Valid delay from CPUCLK	10	12	ns	90pf
T19	ADSV# Low Valid delay from CPUCLK	9	11	ns	90pf
T20	ADSV# High Valid delay from CPUCLK	9	11	ns	90pf
T21	TAGWE# Active delay from CPUCLK	9	11	ns	35pf
T22	TAGWE# Inactive delay from CPUCLK	8	10	ns	35pf
T23	TA[7:0] Output Valid delay from CPUCLK when Hit Cycle	11	15	ns	35pf

T24	TA[7:0] Output Valid delay from CPUCLK in Update Cycle	13	17	ns	35pf
T25	RAS[3:0]# Active delay from CPUCLK	9	12	ns	150pf
T26	RAS[3:0]# Inactive delay from CPUCLK	8	10	ns	150pf
T27	CAS[7:0]# Active delay from CPUCLK	12	15	ns	90pf
T28	CAS[7:0]# Inactive delay from CPUCLK	9	11	ns	90pf
T29	MA[11:0] Low Valid delay from CPUCLK	9	12	ns	35pf
T30	MA[11:0] High Valid delay from CPUCLK	9	12	ns	35pf
T31	MA[11:0] Propagation delay from A[27:3]	8	11	ns	35pf
T32	RAMW# Active delay from CPUCLK	9	11	ns	35pf
T33	RAMW# Inactive delay from CPUCLK	10	13	ns	35pf
T34	A20M# Active delay from CPUCLK	11	14	ns	35pf
T35	A20M# Inactive delay from CPUCLK	12	16	ns	35pf
T36	BOFF# Active delay from CPUCLK	6	8	ns	35pf
T37	BOFF# Inactive delay from CPUCLK	7	8	ns	35pf
T38	INIT Active delay from CPUCLK	6	8	ns	35pf
T39	INIT Inactive delay from CPUCLK	7	8	ns	35pf
T40	PCIRST# Active delay from CPUCLK	9	11	ns	35pf
T41	STPCLK# Active delay from CPUCLK	10	15	ns	35pf
T42	STPCLK# Inactive delay from CPUCLK	10	15	ns	35pf
T43	SMI# Active delay CPUCLK	8	10	ns	35pf
T44	SMI# Inactive delay CPUCLK	8	10	ns	35pf
T45	SMOUT Active delay from CPUCLK	10	15	ns	50pf
T46	SMOUT Inactive delay from CPUCLK	10	15	ns	50pf
T47	HA[31:3] Output valid delay from CPUCLK	15	20	ns	35pf
T48	GNT[3:0]# Active delay from PCICLK	7	9	ns	50pf
T49	GNT[3:0]# Inactive delay from PCICLK	6	8	ns	50pf
T50	PHLDA# Active delay from PCICLK	7	9	ns	50pf
T51	PHOLD# Inactive delay from PCICLK	6	8	ns	50pf
T52	PAR Active delay from PCICLK	9	12	ns	50pf
T53	PAR Inactive delay from PCICLK	9	12	ns	50pf
T54	AD[31:0], C/BE[3:0]# Active delay from PCICLK	9	11	ns	50pf

T55	AD[31:0], C/BE[3:0]# Inactive delay from PCICLK	9	11	ns	50pf
T56	FRAME#, IRDY#, TRDY#, DEVSEL#, STOP# Active delay from PCICLK	9	11	ns	50pf
T57	FRAME#, IRDY#, TRDY#, DEVSEL#, STOP# Inactive delay from PCICLK	9	11	ns	50pf
T58	HD[63:0] data valid delay from MD data valid	8.5	11.5	ns	35pf
T59	HD[63:0] setup time from CPUCLK		2	ns	50pf
T60	HD[63:0] hold time from CPUCLK		2	ns	50
T61	MD[63:0] data valid delay from CPUCLK rising		13	ns	90pf
T62	MD[63:0] setup time from CPUCLK		2	ns	90
T63	MD[63:0] hold time from CPUCLK		2	ns	90
T64	AD[31:0] setup time from CPUCLK		2	ns	50
T65	AD[31:0] hold time from CPUCLK		2	ns	50
T66	HD[63:0] output hold time from PCICLK rising that IRDY# and TRDY# are asserted		13.5	ns	50pf
T67	HD[63:0] data valid delay from PCICLK rising that IRDY# and TRDY# are asserted		15	ns	50pf
T68	MD[63:0] output hold time from PCICLK rising that IRDY# and TRDY# are asserted		12.5	ns	90pf
T69	MD[63:0] data valid delay from PCICLK rising that IRDY# and TRDY# are asserted		13.5	ns	90pf
T70	HD[63:0] output hold time from CPUCLK rising that IRDY# and TRDY# are asserted		11	ns	50pf
T71	HD[63:0] data valid delay from CPUCLK rising that IRDY# and TRDY# are asserted		13	ns	50pf
T72	MD[63:0] output hold time from CPUCLK rising that IRDY# and TRDY# are asserted		9	ns	90pf
T73	MD[63:0] data valid delay from CPUCLK rising that IRDY# and TRDY# are asserted		12.5	ns	90pf

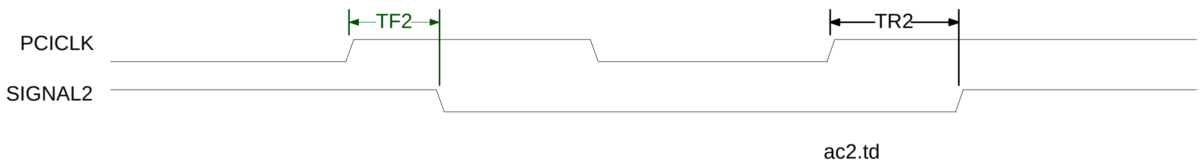
AC timing Diagram



TF1 = T1, T3, T5, T7, T9, T13, T15, T17, T19, T21, T24, T25, T27, T29, T30, T32, T34, T36, T38, T40, T41, T43, T45

TR1=T2, T4,T6,T8,T10, T11, T14, T16, T18, T20, T22, T24, T26, T28, T33, T35, T37, T39, T42, T44, T46

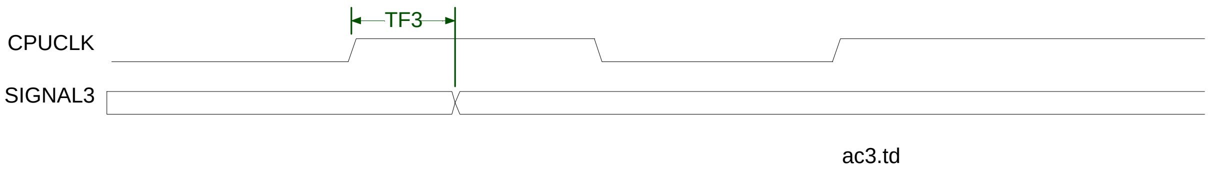
SIGNAL1= BRDY#, KEN#, NA#, EADS#, CPUHOLD, CPURST, KRE#, KWE[7:0]#, ADSC#, ADSV#, TAGWE#, TA[7:0], RAS[3:0]#, CAS[7:0]#, MA[11:0]#, RAMW#, A20M#, SMI#, SMOUT, BOFF#, INIT, HA[31:3], PCIRST#



TF2 = T48, T50, T52, T54, T56

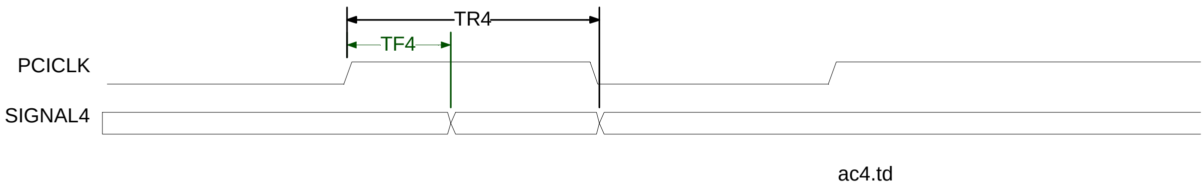
TR2=T49, T51, T53, T55, T57

SIGNAL2= GNT[3:0]#, PHLDA#, PAR#, AD[31:0], C/BE[3:0]#, IRDY#, TRDY#, STOP#, DEVSEL#, FRAME#



TF3 = T23, T24, T47, T61

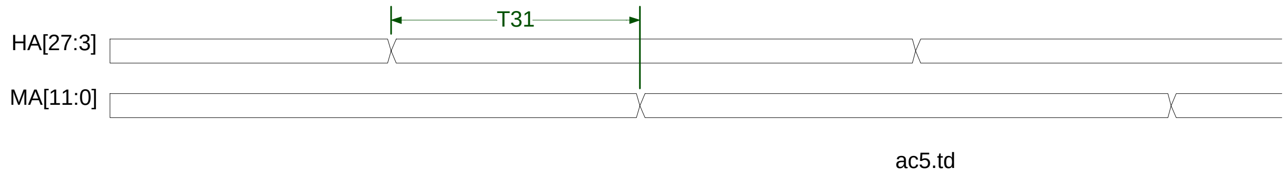
SIGNAL3= TA[7:0], HA[31:3], MD[63:0]

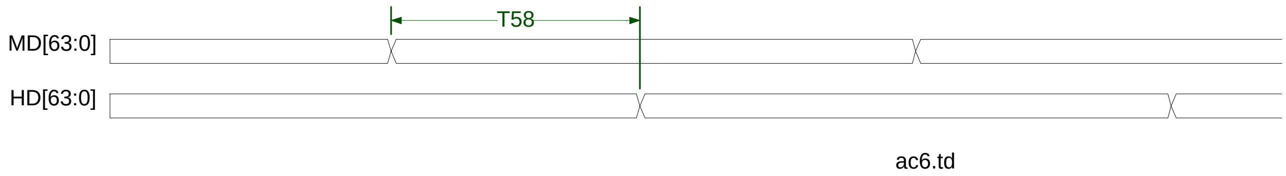


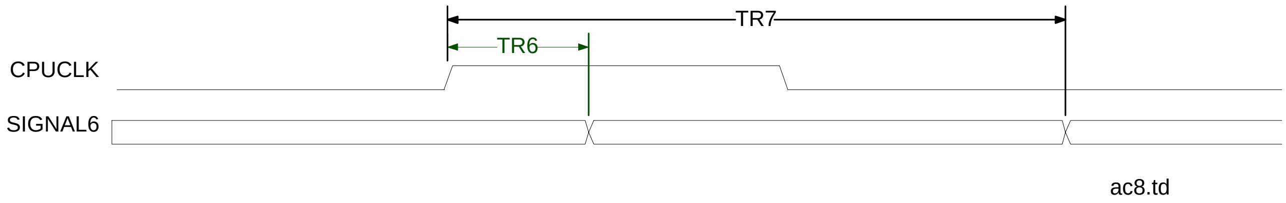
TF4= T54, T66, T68

TR4=T55, T67, T70

SIGNAL4= AD[31:0], CBE[3:0]#, HD[63:0], MD[63:0]







TR6= T70, T72

TR7= T71, T73

SIGNAL6= MD[63:0], HD[63:0]

5.4 DC Characteristics (II)

TA = 0 - 70 0C, VDD = 5 V ± 5 %, GND = 0 V

Symbol	**Parameter**	**Min.**	**Max.**	**Unit**	**Condition**
VIL	Input low voltage	-0.5	0.8	V	
VIH	Input high voltage	2.0	VDD + 0.5	V	
VOL	Output low voltage	-	0.45	V	IOL = 4.0 mA
VOH	Output high voltage	2.4	-	V	IOH = -1.0 mA
IIL	Input leakage current	-	± 10	uA	
IOZ	Tristate leakage current	-	± 20	uA	0.45 < VOUT < VDD

Table 5-3 DC Characteristics for DAC (Analog Output Characteristics)

Description	Min.	Typ.	Max.	Unit
Black Level	-	0	-	V
White Level	-	660	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.625	-	mV
Iref	-	8.40	-	mA

5.5 AC Characteristics (II)

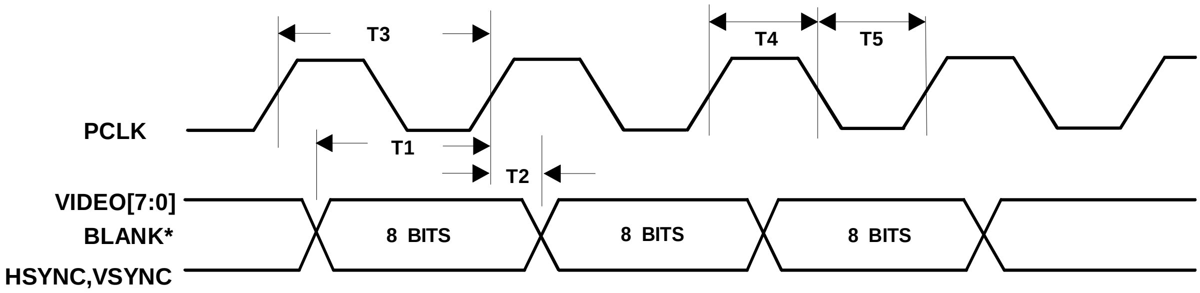


Figure 5.1 Video Timing 4, 8, 24 Bits/Pixel Modes

4,8,16 and 24 BPP Video AC Timing Table

Symbol	Parameter	Min.	Max.	Notes
T_1	VIDEO[7:0], BLANK*, SYNC Setup Time	1.5	-	
T_2	VIDEO[7:0], BLANK*, SYNC Hold Time	1.5	-	
T_3	PCLK Period	7	-	
T_4	PCLK High Time	3	-	
T_5	PCLK Low Time	3	-	

(Units: ns)

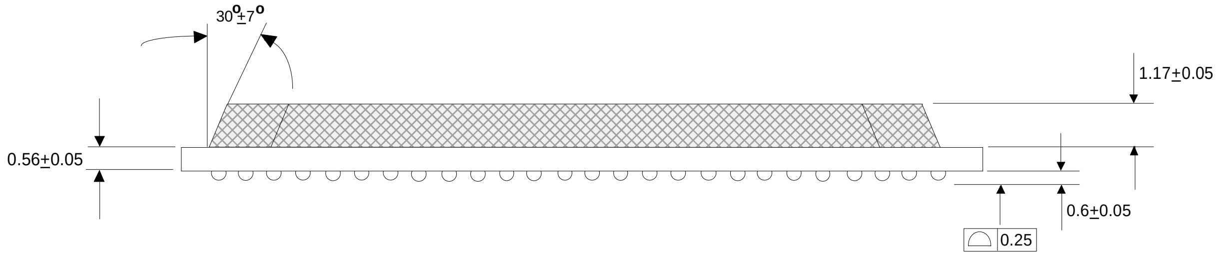
AC Characteristics for DAC (Analog Output Characteristics)

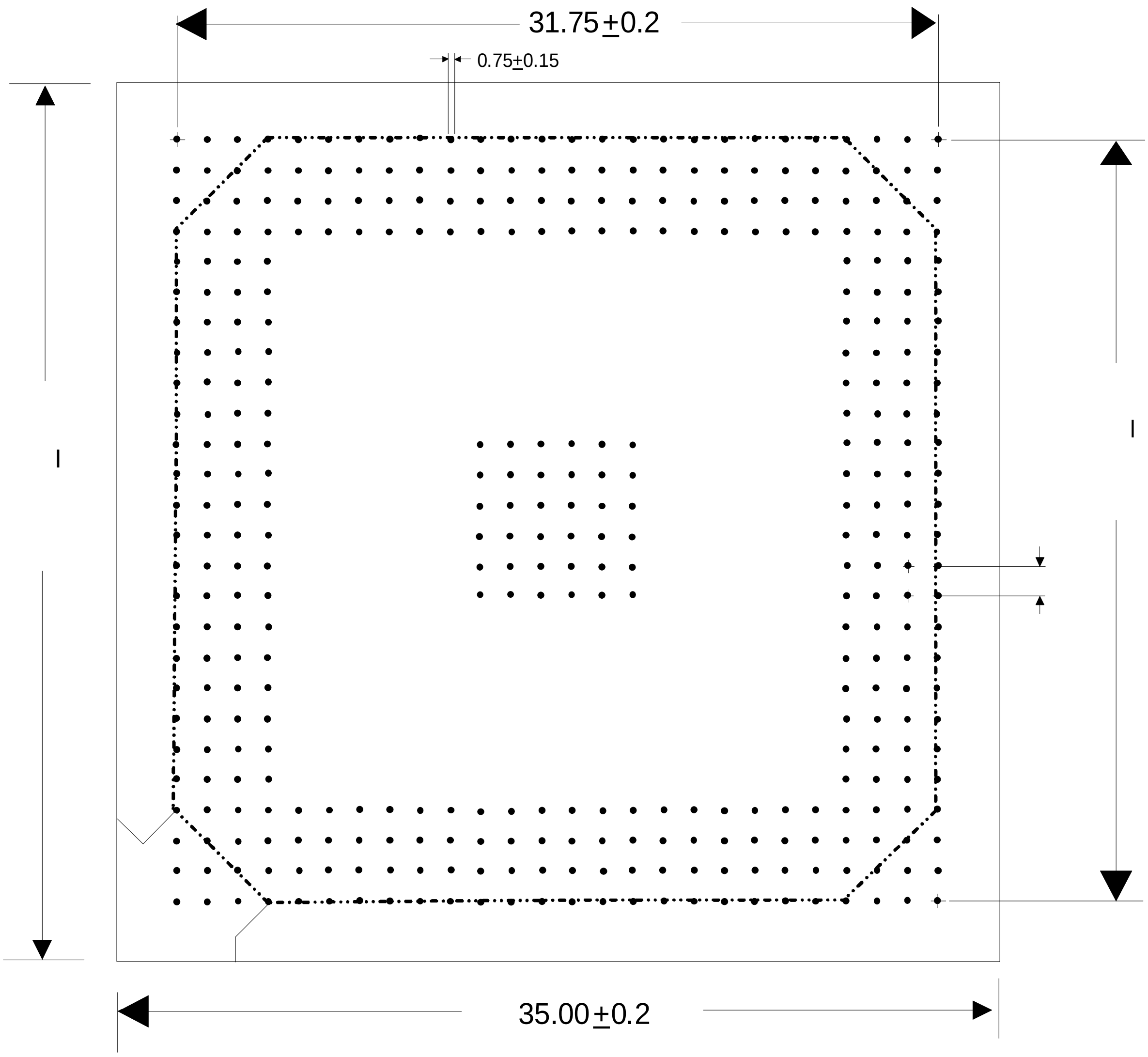
Description	Parameter	Condition	Typ.	Max.	Unit
Settling Time	Tsett	R=37.5 ohmC1=30 pF	-	12.5	ns

6. Mechanical Dimension

6.1 SiS5596 (388 pins)

(Unit: mm)





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