1. SYSTEM OVERVIEW

The OakNote™ Notebook PC subsystem is a set of highly integrated, semi-custom ICs designed from 80286 and 80386SX notebook PCs with clock speeds ranging from 8 Mhz to 20 Mhz. The subsystem consists of:

- OTI041 : System Support and Address Generation Logic
- OTI042 : I/O Control and Data Path Control Logic
- OTI043 : Flat Panel VGA Controller

The OakNote™ subsystem brings to systems designers an optimal solution for implementing a low cost and high performance PC/AT Laptop/Notebook system. To implement a full function PC/AT system, all that is required are: OTI041, OTI042, OTI043, CPU, ROM, RAM, I/O Controller, 8042 & one 7406. This system provides an amazing savings in PC board area. The OakNote™ also features a tightly coupled video subsystem. The Flat Panel VGA Controller (OTI043) achieves the highest possible video performance by utilizing local bus architecture.

With the OakNote™ subsystem, there is no need for extensive BIOS development to implement your power management scheme. The O/S Independent Power Management Scheme and Activities Monitors, inside the subsystem, can bring the Laptop/Notebook system into power savings mode automatically without BIOS intervention.

The OTI041 integrates all the system support logic functions and address generation logic. It is implemented with 1.2 micron HCMOS technology and packaged in a 160 -pin PJQFP. The OTI041 features the following functions:

- Supports 80286 and 80386SX processors.
- Supports local bus video
- Supports local bus programmable memory range
- CPU clock control for power savings in Laptop/Notebook design
- Supports cartridge ROM
- Command state machine generates memory, I/O & Interrupt Acknowledge commands.
- Address and data path control that includes byte swapping for 16 bit to 8 bit memory or I/O devices.
- Memory controller, refresh cycle generator, EMS logic that supports EMS 4.0 specifications.
- Bus arbiter arbitrates the system bus between CPU, DMA, and DRAM refresh requests.
- Two 82C37 DMA controller running up to 8 Mhz.
- DMA support logic provides 7 channels of DMA page map address and burst mode DMA.
- Integrates all address buffers for the AT-bus.
- Supports fast reset to switch from protected mode to real mode for optimized OS/2 operations.

The OTI042 integrates peripheral devices, data and command buffers. It is implemented with a 1.2 micron HCMOS technology and packaged in a 144-pin PJQFP. The OTI042 features the following functions :

- 3 Activities Monitors for power management
- Automatic power-up functions
- Programmable bidirectional control pins
- Programmable I/O chip select pins
- 8254 compatible timer/counter
- Two 8259 compatible interrupt controllers
- Chip select logic for serial/parallel ports, disk controllers, video controller,and keyboard controller.
- Supports both 80287 & 80387SX with 80386 CPU
- Supports 80287 with 80286 CPU
- Memory parity checker & generator
- NMI generation logic
- 146818 compatible real-time clock with 128 bytes of CMOS RAM.
- Integrates all data buffers on the AT-bus.
- 82385SX support
- Optional external data buffer support

The OTI043 integrates all the key system elements for supporting a variety of flat panels on a single chip. It is implemented with a 1.0 micron HCMOS technology and packaged in a 160-pin PJQFP. The OTI043 features the following functions :

- Fully compatible to IBM VGA Hardware
- Supports CRT monitors and flat panel displays
- 800x600 resolution with 64 gray levels for flat panels and 256 colors for CRTs
- Supports 256Kx4 and 64Kx16 DRAMs
- O/S independent power management scheme
- Internal data cache
- Maximum pixel clock frequency up to 50Mhz
- Intelligent color summing and contrast adjusting logic
- Automatic video compensation logic adapts to different panel resolutions
- Integrated palette and separate LCD video timing circuit
- Local bus option with OTI40 Core Logic Subsystem

2.0 INTRODUCTION

The OTI041 is a custom integrated circuit designed for the OakNote™ running with the 80286/80386SX microprocessor. The chip integrates all the functions of CPU interface, data flow control, system and memory address generation. The OTI041, together with OTI042 (peripheral Controller) & OTI043 (Flat Panel VGA Controller), can provide a very cost effective solution to implement a high performance notebook system which is fully compatible with IBM AT architecture.

A summary of the special features provided by the OTI041 is listed as follows:

System Speed:	- supports 8Mhz, 10Mhz,12.5Mhz,16Mhz, and 20Mhz
I/O Channel speed:	- same as or one half of system speed in synchronous mode, fixed at 8Mhz in asynchronous mode
Memory Control:	- page mode and interleave mode for zero wait state cycles
	- supports 60ns to 120ns DRAMs
	- zero wait state ROM cycle with shadow RAM
	- EMS 4.0 hardware with 2 maps of 60 registers each
	- supports 640 Kbytes of system memory, up to 8Mbytes of total on board memory including extended/expanded memory.
	- supports 256K, 1M & 4M type DRAMs
	- slow/staggered/CAS-before-RAS refresh
DMA Control:	- supports fast(8M) & normal(4M) DMA mode with embedded 8237
Laptop Support:	- CPU clock slow/shutdown scheme for CPU power saving
Local bus Support:	- high performance video with OTI043 on the CPU bus
Others:	- Fast reset & gate A20 for the CPU
	- programmable memory range for memory device on local bus

3.0 Pin Description

Pin Name	Pin Type	Description
		*** CPU INTERFACE ***
SA23 - SA0	I/O	CPU ADDRESS BUS : Address bus from CPU. These signals become outputs during DMA or MASTER mode.
BHEn	I/O	BYTE HIGH ENABLE : An active low signal used to enable data on to the most significant half of the data bus (D15 - D8). This signal becomes an output during DMA or MASTER mode.
RESETCPU	O	RESET CPU: An active high output to reset the CPU.
NPRST	O	CO-PROCESSOR RESET: An active high signal to reset the numerical co-processor.
ADSn	I	ADDRESS STROBE : An active low signal coming from 80386SX. This input is also used to detect the presence of 386SX.
S1 - S0	I	BUS CYCLE STATUS : These signals together with M/IO are used to decode different bus cycles. S0 and S1 are connected to W/R- and D/C-,respectively.
M/IO	I	MEMORY OR I/O CYCLE: An input signal from CPU indicating whether the present cycle is memory or I/O access.
CPUCLK	O	CPU CLOCK : ACMOS driven clock signal to the 80286/80386SX CPU. The frequency is programmable through index port 03(hex).
NPCLK	O	CO-PROCESSOR CLOCK: Clock signal for 80287 or 80387SX. This clock can be programmed to stop if co-processor is not used.
SRDYn	O	SYSTEM READY : An active low signal to acknowledge the CPU that the data transfer for either memory or I/O is complete.
		*** DMA INTERFACE ***
DRQ0-3,5-7	I	DMA REQUEST:These are asynchronous active high channel request inputs used by peripheral devices to request DMA service.
DACK0-3,5-7	O	DMA ACKNOWLEDGE: These are active low signals to notify the individual peripheral that it has been granted a DMA cycle.

Pin Name	Pin Type	Description
CPUHRQ	O	HOLD REQUEST : An active high signal connected directly to HOLD of the CPU. This signal is used by the chip to request the bus from the CPU.
CPUHLDA	I	HOLD ACKNOWLEDGE : An active high signal connected directly to HLDA of CPU. This signal is used by the chip to determine if the bus request has been granted by the CPU.
TC	O	TERMINAL COUNT: An active high output pulse signal when the terminal count for any DMA channel is reached.
	***** BUS INTERFACE *****	
PCA(0-19)	I/O	PC BUS ADDRESS : These are the latched version of SA(0-19) and become input during MASTER mode.
LA(17-23)	I/O	UNLATCHED ADDRESS: These are the unlatched version of SA(17-23). The bus become input when MASTER- is active.
PBHEn	I/O	I/O CHANNEL BYTE HIGH ENABLE: An active low signal on the I/O channel. It is a latched version of BHE-. When MASTER- is low, it becomes an input.
WS0n	I	ZERO WAIT STATE : An active low signal indicating the present cycle can be completed without any more wait state.
IOCS16n	I	16-BIT I/O CHIP SELECT : An active low signal indicates to the system that the present data transfer is a 1 wait-state, 16-bit I/O cycle.
MEMCS16n	I	16-BIT MEMORY CHIP SELECT : An active low signal indicates to the system that the present data transfer is a 16-bit memory cycle.
PCALE	O	PC ADDRESS LATCH ENABLE : An active high pulse signal indicatiang the start of any bus cycle and is always high when the CPU bus is held. It is synchronized to BUSCLK.
IOCHRDY	I	I/O CHANNEL READY : An active high ready signal from an I/O channel. It is pulled low by a memory or I/O device to lengthen memory or I/O cycles.
RESET	O	RESET: An active high signal synchronizedto CPUCLK to reset the whole system.

Pin Name	Pin Type	Description
IORDn	I/O	I/O READ COMMAND : An active low command to instruct the I/O device to drive its data onto the data bus. It is input when MASTER- is active.
IOWRn	I/O	I/O WRITE COMMAND : An active low command to instruct the I/O device to read the data present on the data bus. It is input when MASTER- is active.
MEMRDn	I/O	MEMORY READ COMMAND: An active low signal to instruct the memory subsystem to drive its data onto the data bus.It is input when MASTER- is active.
MEMWRn	I/O	MEMORY WRITE COMMAND : An active low signal to instruct the memory subsystem to store the data present on the data bus.It is input when MASTER- is active.
BUSCLK	O	PC-BUS CLOCK : AC MOS driven clock signal for the I/O channel.
	***** SYSTEM INTERFACE *****	
INTAn	I/O	INTERRUPT ACKNOWLEDGE: An active low signal to enable the interrupt controller's interrupt-vector data onto the data bus.
GATEA20	I	GATE A20 : An active high signal from 8042 used to gate address A20.
RST8042n	I	RESET FROM 8042: An active low signal from 8042 to reset the CPU.
CHGCLKn	I	CHANGE SYSTEM SPEED: An active low input signal from OTI042 indicating power-savings modes.
PCENn/WAKEUPn	O	PC DATA BUS ENABLE : An active low control signal to enable the data buffer between CPU and PC data bus. PCENn is active low if : 1. CPU I/O read/write cycle, except coprocessor I/O. 2. CPU memory read/write cycle,except onboard RAM and ROM. 3. Interrupt acknowledge cycle. (INTAn active) This pin carries the WAKEUPn information during powerdown modes.
ENSWAPn	O	ENABLE DATA SWAP: An output to control the output enable of the byte swapping data buffer.

Pin Name	Pin Type	Description
ROMCSn	O	ROM CHIP SELECT : An active low signal used to enable the ROM BIOS to output data on to the data bus.
CROMCSn	O	CARTRIDGE ROM CHIP SELECT: An active low output signal used to access the cartridge ROM.
SEL0	I/O	SELECT FUNCTION 0: One of the two address encoding signals.
SEL1	O	SELECT FUNCTION 1: Together with SEL0 encodes the following address ranges:

SEL1	SEL0	FUNCTION
0	0	Nothing selected
0	1	A15-A10=0(I/O) or on-board video RAM
1	0	on board video ROM
1	1	I/O channel memory but within 1M

PWRGOOD	I	POWER GOOD :An active high signal from the power supply after DC power level is stable.
XD7 - XD0	I/O	XDATA BUS : Bi-directional data lines for accessing this chip.
REFRQT	I	MEMORY REFRESH REQUEST : Memory refresh request signal from 8254 Timer channel 1 which comes from the OTI042.
MREFn	I/O	MEMORY REFRESH : An active low signal indicating that refresh cycle is going on.
ENPARn	O	ENABLE MEMORY PARITY : An active low signal indicating that onboard RAM is being accessed.
RMRDn	I/O	ROM/RAM READ : An active low signal indicating that onboard ROM or RAM is being read.It is an input representing the signal NPBSYn when accessing 80287 operation code for 80386SX CPU.

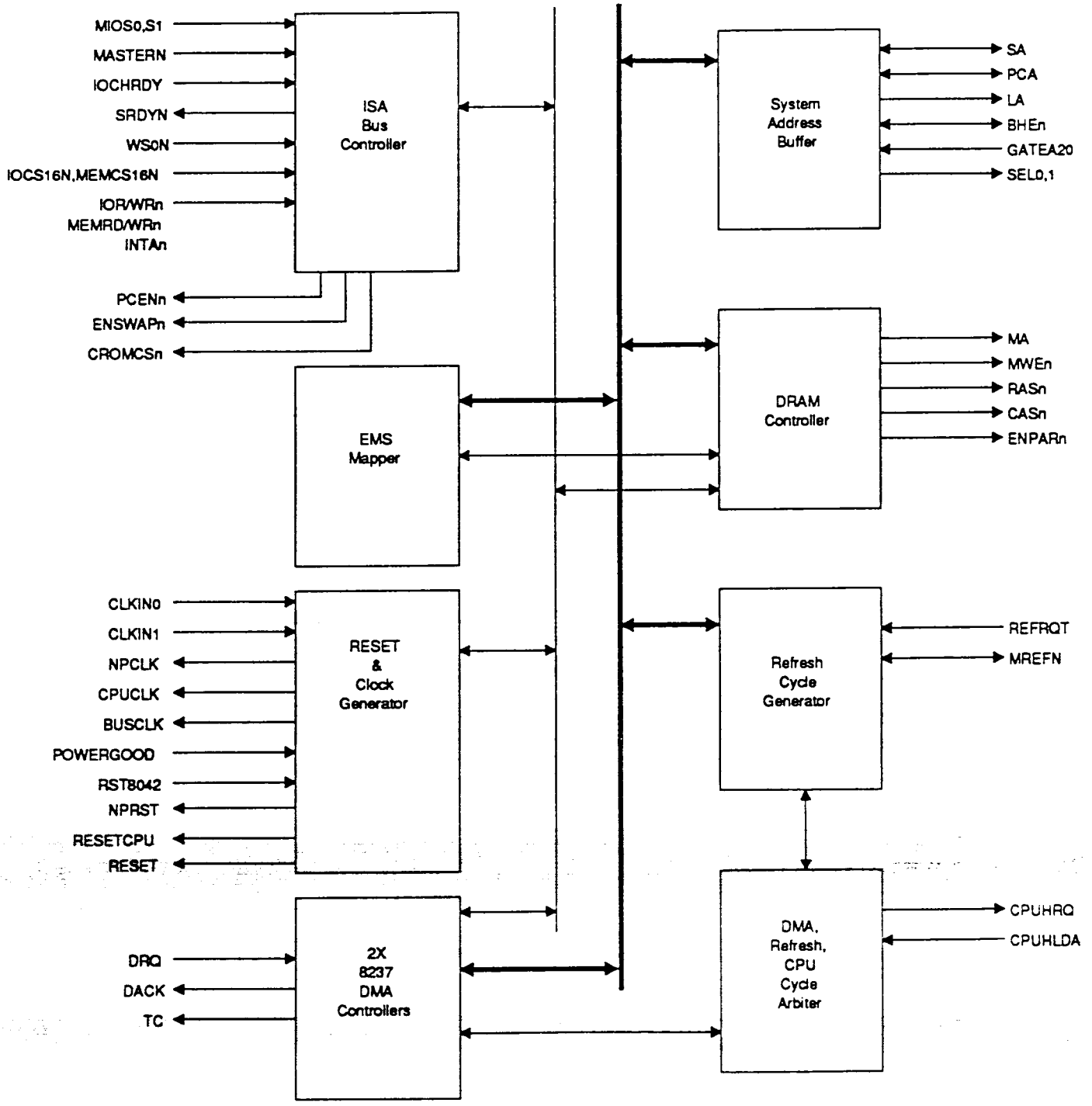
***** MEMORY INTERFACE *****

MA(1-11)	O	MEMORY ADDRESS : It is a time multiplexed memory address bus. (for 256K memory type MA(10,11) are not used, for 1M memory type MA(11) is not used).

Pin Name	Pin Type	Description
RAS0n - RAS3n	O	ROW ADDRESS STROBE: These are active low control signals to the onboard DRAM to strobe the row address .
CASH0-3n - CASL0-3n	O	COLUMN ADDRESS STROBE (High & Low) : These are active low control signals to on board DRAM to strobe the column address: - CASHn for odd byte [D(15-8)]. - CASLn for even byte [D(7-0)].
MWEn	O	MEMORY WRITE ENABLE : An active low signal used to control memory read/write cycle.
	*** MISCELLANEOUS ***	
CLKIN0	I	CLOCK INPUT 0 : A 32 MHz TTL clock input with 50% duty cycle. It is used for: the CPU clock generation with CPU running at 8 or 16MHz, asynchronous bus clock generation, and memory refresh time.
CLKIN1	I	CLOCK INPUT 1 : An optional 20/ 25/40MHz TTL clock input with 50% duty cycle. It is used for CPU clock generation with CPU running at 10, 12.5 & 20 MHz.
VDD		POWER : +5 V supply.
VSS		GROUND

NOTE: OTI041 enters into TEST mode under the following input pin combination : IORD-,IOWR-,INTA-,MEMRD-, and MEMWR- are all low and MASTER- high when PWRGOOD turns from low to high.

4.0 System Block Diagram



5.0 System Memory and I/O Map

The 80286/386SX has a 24-bit address bus to directly access up to 16M bytes of memory . The memory map for AT compatible system is listed as follows:

MEMORY MAP

HEX ADDRESS	DESCRIPTION
00000 - 1FFFF	128KB : BANK 1
20000 - 2FFFF	64KB: BANK 2
30000 - 3FFFF	64KB: BANK 3
40000 - 4FFFF	64KB: BANK 4
50000 - 5FFFF	64KB: BANK 5
60000 - 6FFFF	64KB: BANK 6
70000 - 7FFFF	64KB: BANK 7
80000 - 8FFFF	64KB: BANK 8
90000 - 9FFFF	64KB: BANK 9
A0000 - BFFFF	128KB: Video Buffer
C0000 - DFFFF	128KB: Reserved for BIOS on I/O Channel
E0000 - FFFFF	128KB: System ROM
100000 - XXXXXX	Extended Memory
XXXXXX - YYYYYY	Expanded Memory
E00000 - FFFFFF	128KB: System ROM

The OTI041 supports up to 8M bytes of memory which can be assigned as conventional, extended, shadow RAM, and EMS memory.

I/O MAP

I/O ADDRESS	FUNCTION	OTI041	OTI042
0000 - 000F	DMA Controller 1	R/W	none
0010 - 0018	EMS Registers	R/W	none
001E	OAK Port Addr Ptr	R/W	W
001F	OAK Data Register	R/W	R/W
0020 - 003F	Interrupt Cont.1	none	R/W
0040 - 0043	System Timer	none	R/W
0060-006E	Keyboard Controller	none	none
0061 - 006F	Port B	none	R/W
(odd bytes)			
0070	NMI mask, RTC	none	W
0071 - 007F	Real-time Clock	none	R/W
0080 - 008F	DMA Page Register	R/W	none
0090 - 009F	Reserved	R/W	R/W
00A0 - 00BF	Interrupt Cont.2	none	R/W
00C0 - 00DE	DMA Controller 2	R/W	none
00F0	Clear Copro. Busy	none	W
00F1	Reset Co-proc.	none	W
00F2 - 00F7	Reserved	none	none
00F8 - 00FF	Math Co-processor	none	R/W
0100 - 0107	Prog Option Select	R/W	R/W
02F8 - 02FF	Serial Comm. #2	none	none
01F0 - 01F7	Fixed Disk Cont.	none	none
0320 - 032F	Fixed Disk Cont.	none	none
0278 - 027A	Parallel Port 3	none	none
0378 - 037A	Parallel Port 2	none	none
03BC - 03BE	Parallel Port 1	none	none
03B0 - 03DF	Video System	none	none
03F0 - 03F7	Floppy Disk Cont.	none	none
03F8 - 03FF	Serial Comm. #1	none	none

OTI041 SPECIAL I/O MAP

I/O ADDRESS	ACCESS		FUNCTION NAME
0010	R/W(0-1)	EMSEN:	EMS Enable Register
0011	R/W(0-5)	CEAP:	Current EMS Address Pointer
0012	R/W(0-7)	CMAPL:	Current EMS MAP - Low Byte
0013	R/W(0-1)	CMAPH:	Current EMS MAP - High Byte
0014	R/W(0-7)	EMDMAL:	Enable Alternate MAP for DMA
0015	R/W(0-5)	AEAP:	Alternate EMS Address Pointer
0016	R/W(0-7)	AMAPL:	Alternate EMS MAP - Low Byte
0017	R/W(0-1)	AMAPH:	Alternate EMS MAP - High Byte
0018	R/W(0-7)	EMDMAH:	Enable Alternate MAP for DMA
001E	R/W(0-7)	OAKADR :	OAK PORTS INDEX Register
001F	R/W(0-7)	OAKDAT :	OAK PORTS DATA Register

OTI041 INDEX PORT I/O MAP

INDEX ADDR	ACCESS		FUNCTION NAME
0003	R/W(0-7)	SPCS:	Speed Control Register
0004	R/W(0-7)	VIDEO0	: Video BIOS & I/O Enable
0005	R/W(0-7)	VIDEO1	: Video Memory Enable Register
000E	R/W(0-7)	STAT41	: OTI041 STATUS Register
000F	R(0-7)	CHIPID	: OTI041 ID Register
0010	R/W(1-3)	ENRAS	: RAS Enable Register
0011	R/W(0-7)	RAMT0 :	RAM Timing Control Register 0
0018	W(0-7)	SHDRM0 :	SHADOW RAM CONTROL Register 0
0019	W(0-7)	SHDRM1 :	SHADOW RAM CONTROL Register 1
001A	W(7)	MEMCFG :	MEMORY CONFIGURATION Register
001B	R/W(0-7)	WATCTL :	Wait State Control Register
001C	R/W(0)	EMSPOF:	EMS Mapper Power Enable Register
001D	R/W(0-7)	EXTMEM :	Extended memory boundary (64K)
001E	R/W(0-7)	RAMT1 :	RAM Timing Control Register 1
001F	R/W(0-7)	REV041:	Chip Revision Register

NOTE: To access any OTI index register, write the index to port 'H1E first, then perform READ/WRITE operation to data port 'h1F. After each access to port 'H1F, the index value inside port 'H1E is automatically reset to 'H00.

6.0 OTI041 FUNCTIONAL DESCRIPTION

OTI041 functions can be categorized as follows:

1. Command Cycle Control

2. Address & Data Path

3. Clock Generator and reset control

4. Memory & I/O Decoder & Buffer Control

5. System Ready Generator

6. Power Management

7. Memory Control Unit

8. DMA Control

9. Arbiter & Refresh Control

10. Address Buffers

11. Local Bus Support

6.1 Command Cycle Control

Command Cycle Control contains a state machine that generates commands for various CPU cycles :

- Memory Read/Write Cycle if memory access is outside of on board RAM or ROM.
- I/O Read/Write Cycle.
- Interrupt Acknowledge Cycle.

In addition to these functions, Command Cycle Control also generates the ALE signal internally when it detects the change of CPU Status lines : S0 - S1 & M/IO at TS time for 80286 or ADSn for 80386SX to mark the beginning of the CPU cycle.

The Command Cycle Control is clocked by BUSCLK which can come from two different clock sources depending on the timing mode selected by programming indexed port 'H03 .

In the Synchronous mode, SYSCLK. which is a half or one fourth of CPUCLK , is used as BUSCLK.

In the Asynchronous mode, a fixed 8MHz clock is used as BUSCLK. The state machine would always run independent of the CPU speed, and a very high speed CPU can be used while the system can still maintain AT-compatible bus timing. In this way the command pulse width and command recovery time are independent of the CPU speed. PCALE and commands are all synchronized to this clock which is also the BUSCLK on the PC-BUS.

6.1.1 Memory Read/Write Cycle

If the memory being accessed does not reside in either onboard RAM or ROM area, MEMRDn or MEMWRn signals from OTI041 will become active during TC(T2p or T2I for 80386SX) cycles. The command length is 4.5 BUSCLK's if MEMCS16n is not active and 2 BUSCLK's if MEMCS16n is active.

If IOCHRDY is low before commands end, the command will be extended and will be terminated one BUSCLK minimum after the IOCHRDY is asserted high.

If the current cycle is a 16-bit memory access to 8-bit memory devices, the state machine will generate two consecutive memory commands with the first one accessing the low byte and the second one accessing the high byte . From the end of the first cycle to the beginning of the second one, the command RECOVERY TIME will be 1.5 BUSCLK's. For memory read cycle, low byte of data will be stored in the OTI042 and is output to the CPU bus at the second cycle along with the high byte. If MEMCS16n is low for a 16 bit memory access, no double cycle will be generated. The memory cycle would also be an one wait state command cycle unless IOCHRDY is inactive.

If WS0n is low during any PC memory cycles, the memory cycle would be terminated in the following BUSCLK.

6.1.2 I/O Read/Write Cycle

During CPU I/O cycle, IORDn or IOWRn command will be asserted at phase 2 of TC(T2p or T2I for 80386SX). Command length is fixed at 4.5 BUSCLK's and recovery time at 1.5 BUSCLK's.

If IOCHRDY is low before commands end, the command will be extended and will be terminated 1 BUSCLK minimum after the IOCHRDY is asserted high.

Similar to memory commands, if the current cycle is a 16-bit I/O access to 8 bit I/O devices, the state machine will generate 2 consecutive cycles with a command recovery time of 1.5 BUSCLK's. However, if IOCS16n is low, no double cycle will be generated, and the current cycle would be an one wait state command cycle unless IOCHRDY is inactive.

6.1.3 Interrupt Acknowledge Cycle

CPU will generate two consecutive interrupt acknowledge (INTAn) cycles to an interrupt controller in response to the interrupt request (INTR) signal. During the first cycle, the interrupt controller will resolve the priority if there are more than one interrupt pending. In the second cycle, the interrupt controller will output onto the 8 bit data bus (D0 - D7) the interrupt vector address pointing to the interrupt routine table. INTAn is asserted at phase 2 of TC(T2p or T2I for 80386SX). The IOCHRDY can also extend the duration of the cycle which will be terminated 1 clock minimum after the IOCHRDY is asserted high. The minimum period (if IOCHRDY is always high) of INTAn is one and a half BUSCLK's. HOLD request to the CPU is blocked between the two INTAn cycles .

6.1.4 ROM BIOS Read Cycle

A separate state machine generates the RMRDn command if it is a memory access between 0E0000 and 0FFFFF memory space. RMRDn is asserted at the end of TS (T1p or T2 for 80386SX) with programmable wait states from 1 to 4. Shadow RAM implementation can be selected for zero wait state ROM cycles .

Single 8-bit ROM which should be resided on the upper byte CPU bus is also supported and is detected automatically upon powerup.

6.2 Address & Data Path

The OTI041 is connected directly to the address bus of CPU and it will latch the address bus internally to form an address bus PCA(0 - 19).LA(17-23) are also latched but they are changed to next cycle address towards the end of bus cycles to generate pipeline address.

The byte swapping signal ENSWAPn is also generated by this section which will enable data path between low byte and high byte PCD bus to access an 8 bit device.

6.3 Clock Generator & Reset Control

6.3.1 Clock Generator

The OTI041 supports system speeds from 8Mhz, 10Mhz,12.5Mhz 16Mhz & 20Mhz.

Two clock inputs are available:

CLKIN0 : 32MHZ

CLKIN1 : 20/25/40MHZ

CLKIN0 is mandatory, because the OTI041 uses CLKIN0 to derive the asynchronous bus clock and CPU clock for 8M/16Mhz ,sleep and slow mode. CLKIN1 is optional and a 20Mhz/25/40Mhz clock oscillator can be connected for 10/12.5/20Mhz system speed. The power-up default speed is 8Mhz and different speeds can be selected by programming indexed port 03H.

During refresh period, the OTI041 will sample the level of SEL0 sent from the OTI042 to determine whether speed should be forced to 8Mhz or kept at the value set in indexed port 03H.

The Clock Generator provides clocks to the CPU, Memory Controller, DMA controller, and the rest of the system. It can be broken down to 2 blocks based on their functions :

- Multiplexer & Deglitching Circuit based on CLKIN0, and the presence of CLKIN1.
- Dividers : by 2 ,by 4 or by 8.

6.3.2 Reset Control

The OTI041 will generate reset to the CPU under the following conditions:

- When PWRGOOD signal is low.
- When writing to port 64H or port 92H (fast reset).
- When CPU issues a shutdown cycle.

The RESETCPU signal generated will be active for 16 CPU clocks to meet the CPU specification .

The OTI041 will generate reset to the coprocessor under the following conditions:

- When PWRGOOD signal is low.
- When writing to port F1H.
- When NPCLK is enabled.

The NPRST signal generated will be active for 78 CPU clocks to meet the specification requirements .

6.4 Memory & I/O Decoder & Buffer Control

This section provides the decoder for the memory and IO devices in the system and the OTI041 and OTI042 internal buffer enable and direction controls . It also generates status signals:SEL1 and SEL0 to the OTI042 as the address range information.

6.5 Ready Generator

SRDYn will be active low only at the end of the CPU cycle. There are 3 sources that generate the ready signal to the CPU to end a cycle :

- Memory Control if the access is in the onboard memory range.
- ROM State Machine if the access is in the system BIOS ROM range.
- Command Generator that generates the cycle besides the onboard RAM and ROM.

The SRDYn signal will start at the beginning of TC(T2p or T2l for 80386SX) and end in the middle of TS(T1p or T1 for 80386SX) or Tl and will be 3 CPU clock wide.

6.6 Power Management

There are 3 power saving modes in controlling the CPU speed:

SHUTDOWN Mode	- The CPU clock is stopped. The OTI041 takes over the bus and keeps responding to refresh requests while ignoring DMA requests .Since the 8254 can be optionally stopped in this mode, the refresh request is derived from the 32.684khz clock and the arbiter in the OTI041 will respond to both edges of the REFREQ signal. When the system is waked up, the CPU can be optionally selected to be reset or not depending on whether static CPU is used.
SLEEP Mode	- The CPU is running at 2Mhz.This mode is similar to the above one except that the CPU is not reset when the system is waked up.
SLOW Mode	- The CPU is running at 4Mhz with all other respects the same as normal operation.

These 3 different CPU power-saving modes can be selected by programming indexed port 03(hex). The CPU can be awakened from the SHUTDOWN or SLEEP mode through a wakeup signal(INTAn) which is sent by the OTI042 at the end of the wakeup timer (clocked once a second or a minute) or wakeup counter(clocked by WAKEUP pin),and the OTI041 will release the bus after waked up.

6.7 Memory Control Unit

The OTI041 has a built-in Dynamic RAM memory control unit. It supports 640K bytes of conventional memory, shadow RAM , memory relocation above extended memory boundary, or expanded memory supporting full EMS 4.0. Either 256K , 1M or 4M types of DRAMs can be used and the memory size can vary from a minimum of 512Kbytes to a maximum of 8 MBytes. Detailed description of the memory system can be found in later sections.

The function of Memory Control Unit can be broken down to 4 sub-blocks :

1. Memory Configuration and Timing Control
2. EMS Mapper
3. Various Memory Cycle Generation Control
4. Memory Address Generator

6.7.1 Memory Configuration and Timing Control

6.7.1.1 Shadow RAM

The system BIOS ROM can be accessed from either of the following two address spaces:

0E0000 - 0FFFFF (128K)

FE0000 - FFFFFF (128K)

Shadow RAM implementation which will reduce the needed wait states is supported for the address spaces reserved for both the BIOS ROM and peripheral ROM and RAM area. Onboard RAM will be read for these address space when shadow RAM is enabled.

Shadow RAM address space covers:

0C0000 - 0C7FFF (video ROM area)

0C8000 - 0CFFFF (video ROM area)

0D0000 - 0D7FFF (PC bus external device ROM area)

0D8000 - 0DFFFF (PC bus external device ROM area)

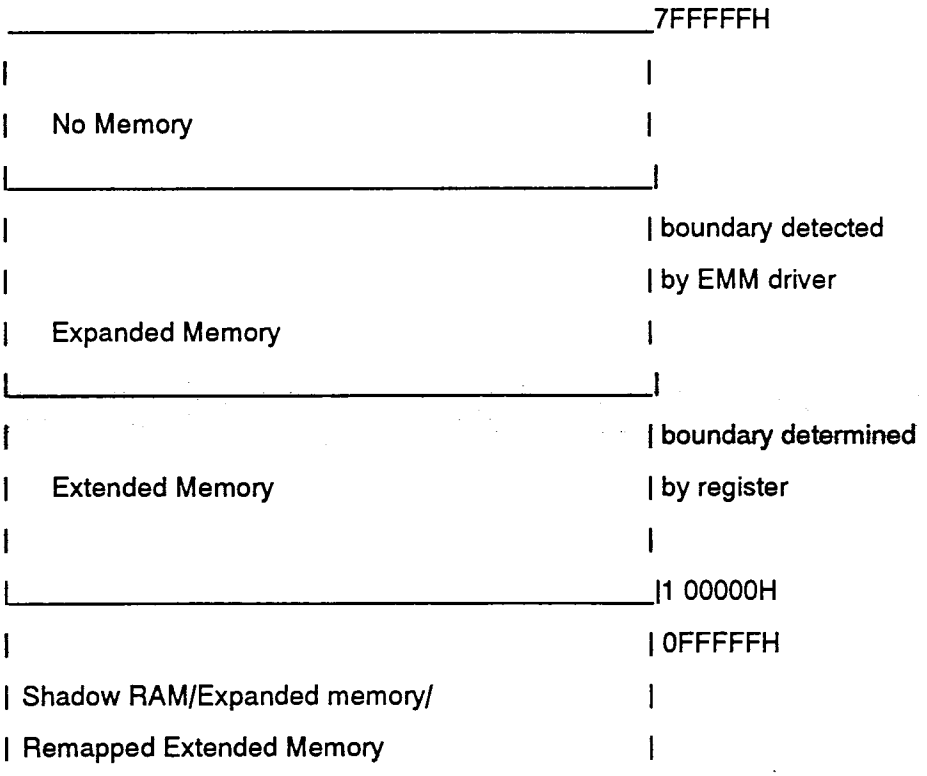
0E0000 - 0EFFFF (System BIOS area or EMS area)

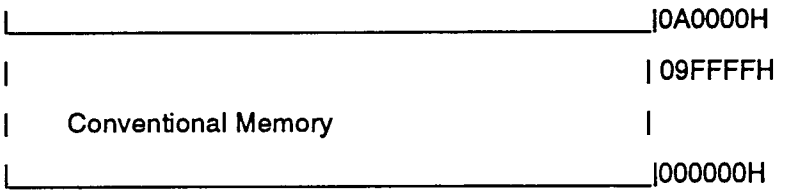
0F0000 - 0FFFFF (System BIOS area)

Two indexed ports 18H and 19H are used to enable shadow RAM . If shadow RAM is not used, onboard RAM area from above 640K to below 1M can be used as Expanded memory or mapped to above upper boundary of extended memory address space.

Protection circuitry on chip can prevent writing to the shadow RAM area after RAM content is loaded,and they are write-enabled after power-up.

6.7.1.2 Onboard Memory Map





The onboard memory cycles are generated for the 640K conventional memory space if they are enabled in the System board Memory Enable Register(POS register 104H);otherwise,MEMRD- or MEMWR- is generated.

If the onboard memory between 0A0000H to 0FFFFFH is remapped as extended memory through the POS register 103H or indexed port 'H1A,the Shadow RAM feature is disabled and the EMS manager can not map the logical page to this area.

6.7.1.3 Onboard Memory Configurations

The 640K of system memory can be disabled individually in 128Kbyte blocks. At power-up, if certain memory is determined to be bad by the BIOS, or if offboard memory is detected in any of the 5 address ranges, the BIOS is able to disable that particular memory block by writing to the System Board Memory Enable Register whose definition is listed as follows:

System Board Memory Enable Register: I/O Port 0104 (hex) R/W :

Bit	Function	
7-5	Not used	
4	Enable/Disable- 5th Bank	080000H-09FFFFH
3	Enable/Disable- 4th Bank	060000H-07FFFFH
2	Enable/Disable- 3rd Bank	040000H-05FFFFH
1	Enable/Disable- 2nd Bank	020000H-03FFFFH
0	Enable/Disable- 1st Bank	000000H-01FFFFH

At power on or Reset, the content of port 104H is 1F(hex).

The OTI041 supports 256K type, 1M type and 4M type of DRAMs. In order to extract the highest performance out of the memory system, both page and interleave mode memory accessing techniques are implemented.

Maximum Page size for 256K DRAM is 512 x 2bytes = 1 KBytes, 1K x 2 Bytes = 2 KBytes for 1M type DRAM and 2K x 2 bytes=4K bytes for 4M type DRAM. Interleave is done at page boundaries, which doubles the page size. For 4M type DRAMs, no interleave is offered.

Two-way Interleaved Memory: between BANK 0 & 1 or BANK 2 & 3

BANK 0	BANK 1
Page 0	Page 1
Page 2	Page 3

Four-way Interleaved Memory:

BANK 0	BANK 1	BANK 2	BANK 3
Page 0	Page 1	Page 2	Page 3
Page 4	Page 5	Page 6	Page 7

According to the principle of locality of reference, it is relatively unlikely that a program would reference across the page boundary. With an interleaved memory done in the above fashion, consecutive memory access would be mostly from the same page on the same bank, thus the RAS precharge time can be saved.

Possible memory configurations are:

TOTAL MEMORY SIZE VERSUS MEMORY TYPE

Memory size	BANK 0	BANK 1	BANK 2	BANK 3
512K	256K	0	0	0
1M	256K	256K	0	0
1.5M	256K	256K	256K	0
2M	256K	256K	256K	256K
2M	1M	0	0	0
3M	256K	256K	1M	0
4M	1M	1M	0	0
5M	256K	256K	1M	1M
6M	1M	1M	1M	0
8M	1M	1M	1M	1M
8M	4M	0	0	0
8M	256K	256K	4M	0

6.7.1.4 RAS Time Out

There is a limitation on the maximum RAS pulse width (10,000ns, 30,000ns or 100,000ns) for the DRAM. A register is provided to set the maximum pulse width and a timer will track the RAS pulse

width and will cause the RAS signal to be inactive if the maximum time is reached. Wait states would be inserted to accommodate the RAS precharge time, and next memory access can then continue with the timer being reset to zero.

6.7.1.5 Memory Timing Generation

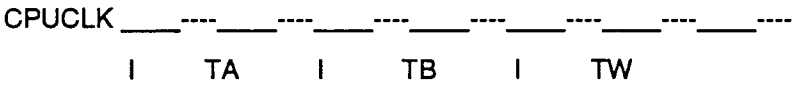
Two types of memory cycles are used to accommodate different kinds of DRAM.

Type 1 - used for nonpage-mode DRAM. These can be either zero or one wait state.

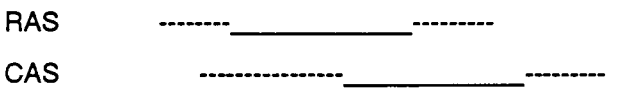
Type 2 - used for page-mode DRAM. The timing is fully programmable with selections of 0 or 1 wait state for page hit and there are various other parameters used to control the RAM access timing.

The following figures illustrate the onboard memory timing for both nopage and page modes:

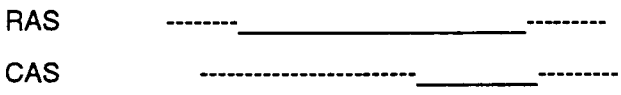
NoPage Mode Memory Timing



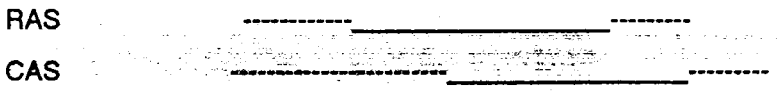
0 Wait Read Timing



0 Wait Write Timing



1 Wait Timing



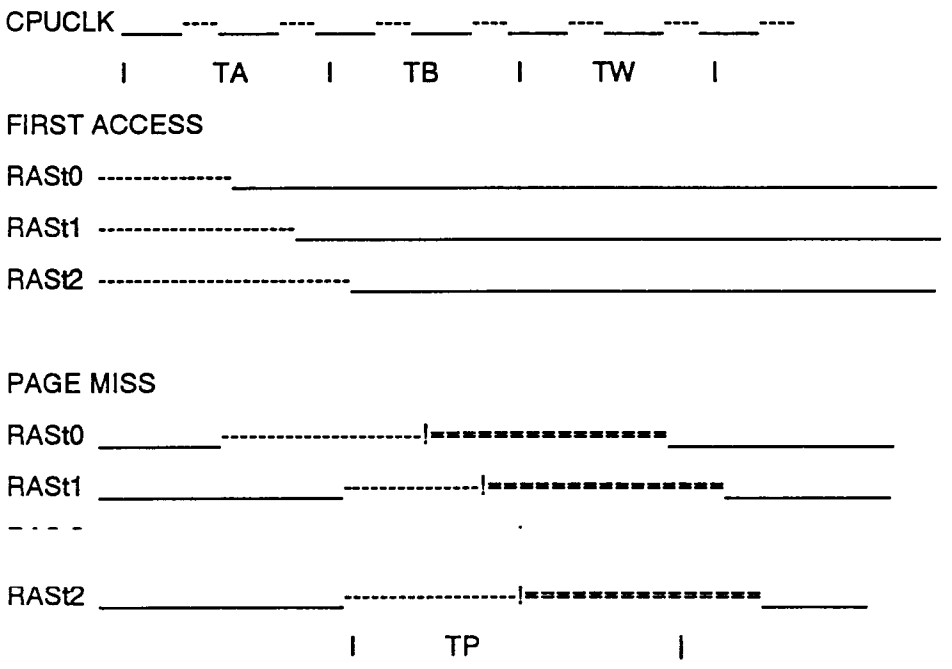
TA is the Ts cycle for 80286 and T1p or T2 cycle for 80386SX depending on whether the current cycle is pipelined or nonpipelined cycle.

TB is the Tc cycle for 80286 and T2p or T2I cycle for 80386SX depending on whether there is bus cycle pending.

A cycle immediately following a write cycle with 0 wait state will cause one wait cycle to be inserted to give enough RAS precharge time. Extended CAS is supported for 0 wait write cycle which will cause the CAS signal to extend one CPUCLK to the next TA or TI cycle.

In the case of 80386SX mode, one more wait state will be inserted for nonpipelined cycles.

Page Mode Memory Timing



TA : TS(T1p or T2) cycle when first access or page miss

TB : TS cycle when write hit or read hit for CASt0

TC(T2p or T2l) cycle when first access or page miss

TW : TS cycle when read hit for CASt1 and CASt2

TC cycle for all other cycles

TP : RAS precharge cycle. Can be 1 or 2 states.

As we can see from the above timing diagram, both RAS and CAS can drop at 3 different positions, and the timing definitions for read and write cycles are different. This is because during write cycle, CAS should delay to allow enough data setup time.

TB cycle can also be programmed to be 0 to 2 states to accommodate various DRAM speeds which may require longer RAS access time.

Extended CAS for write cycles is also supported. But if a read hit cycle immediately follows a CAS-extended write cycle, one wait state is inserted to give enough CAS precharge time.

The CAS width is controlled by another bit in the RAM Timing Control Register which is read/write hit wait state. If 1 is programmed, the CAS will be incremented by 2 CPU clocks.

The following table lists the best performance that can be obtained using popular DRAM's.

Wait States versus Memory Speed

DRAM SPEED	SYSTEM SPEED (MHZ)				
	8	10	12.5	16	20
120NS	no page	1/0/3	1/0/3	2/1/4	N.A.
100NS	no page	no page	1/0/3	1/0/3	2/0/4
80NS	no page	no page	no page	1/0/3	1/0/3
60NS	no page	no page	no page	no page	1/0/3

w.s. at 1st access / w.s. for page hit / w.s. for page miss

N.A. stands for 'not available'.

"no page" stands for zero wait state nonpage mode.

6.7.2 EMS Mapper

The EMS mapper consists of EMS Current Map registers, EMS Alternate Map registers and EMS mapper read/write control logic.

- Current and Alternate Map registers are 60 words by 10-bit register file each, containing enable bit and the map address 22 to 14 for the EMS memory. The 1MB real memory address space is logically broken down into 64 pages of 16K bytes each with the highest 4 pages(F0000 to FFFFF) reserved for BIOS ROM and any map register which is selected using one of the sixty logical pages can be programmed to map to anyone of the 16KB pages of EMS memory.

- Mapper read/write control logic provides path to access the map registers. To write the mapper involves writing to the index register first, and then writing to the low byte, and finally writing to the high byte. The low and high byte can be read independently without the low/high sequence.

6.7.3 Various Memory Cycle Generation Control

There are 3 sources generating the onboard memory cycles:

-During CPU memory access, the timing is programmable.

-During DMA or master mode transfer, RAS- follows memory read or memory write commands (MEMRD- or MEMWR-) which are synchronized using 16Mhz clock. CAS- signals are generated one 16Mhz clock after RAS-.

-During memory refresh cycle, RAS- will follow the MEMRD- command and will be asserted one by one with a time delay of approximately 60ns if staggered refresh is enabled to reduce instantaneous power surge.

CAS signals are generated based on which byte is enabled and not during memory refresh cycle.

6.7.4 Memory Address Generator

The memory address generator is used to drive the onboard memory address. During CPU memory cycle, the lower order address A(1-11) is output through MA(1-11). At 1/2 or 1 clock after RAS- is active, the higher order address starts to drive MA(1-11). During memory refresh, MA(1-11) is driven by the refresh address generator.

6.8 DMA CONTROL

DMA Control consists of 3 blocks :

- Two 82C37 DMA Controllers
- DMA Page Registers
- DMA Ready Generator

6.8.1 8237 DMA Controller

The embedded 82C37 DMA Controllers together provide 7 channel DMA operating at either 4Mhz or 8Mhz . It is used to support 8 & 16-bit transfer between memory and IO devices. The DMA channels are assigned as follow :

Channel	Assignment
Channel0 : DRQ0	Reserved
Channel1 : DRQ1	Reserved
Channel2 : DRQ2	Diskette
Channel3 : DRQ3	Fixed Disk
Channel4 : DRQ4	Cascade for Ctrl 1
Channel5 : DRQ5	Reserved
Channel6 : DRQ6	Reserved
Channel7 : DRQ7	Reserved

DMA controller 1 contains channels 0 to 3. It supports 8 bit DMA transfer. Each channel can transfer 64Kbytes data maximum at a time throughout the 16M byte system address space because the DMA controller only provides 16 address lines with the high order address lines generated by the page register. The following figure shows address generation for the DMA channels.

Source	DMA Page Register	Controller #1
Address	A23<----------->A16	A15<----------->A0

Note : PBHE- is the inversion of PCA0.

DMA controller 2 contains channels 4 to 7. Channel 4 is used to cascade with DMA controller 1. Channels 5,6,7 supports 16-bit data transfer and can transfer 128Kbytes maximum at a time throughout the 16M system address space.The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller #2
Address	A23<----------->A17	A16<----------->A1

Note : PBHE- and PCA0 are all 0.

The following table lists the DMA controller registers and their IO address:

I/O Address (in hex)	Register Function
0000	Channel 0 base & current address reg.
0001	Channel 0 base & current word count
0002	Channel 1 base & current address reg.
0003	Channel 1 base & current word count
0004	Channel 2 base & current address reg.
0005	Channel 2 base & current word count
0006	Channel 3 base & current address reg.
0007	Channel 3 base & current word count
0008	Read Status Reg./Write Command Reg.
0009	Write Request Reg.
000A	Write Single Mask Register Bit
000B	Write Mode Reg.
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Reg./Write Master Clear
000E	Clear Mask Reg.
000F	Write All Mask Register Bits
00C0	Channel 0 base & current address reg.
00C2	Channel 0 base & current word count
00C4	Channel 1 base & current address reg.
00C6	Channel 1 base & current word count
00C8	Channel 2 base & current address reg.
00CA	Channel 2 base & current word count
00CC	Channel 3 base & current address reg.
00CE	Channel 3 base & current word count
00D0	Read Status Reg./Write Command Reg.
00D2	Write Request Reg.
00D4	Write Single Mask Register Bit
00D6	Write Mode Reg.
00D8	Clear Byte Pointer Flip-Flop
00DA	Read Temporary Reg./Write Master Clear
00DC	Clear Mask Reg.
00DE	Write All Mask Register Bits

6.8.2 DMA Page Register

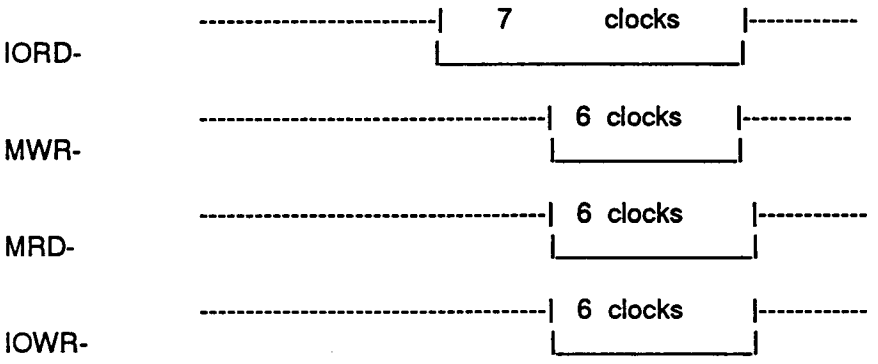
The page register generates high order address for DMA transfer and refresh cycles and will not be changed throughout the whole cycle.The following table shows the IO address for the page registers and their corresponding DMA channels:

Page Register	I/O Address (in hex)
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

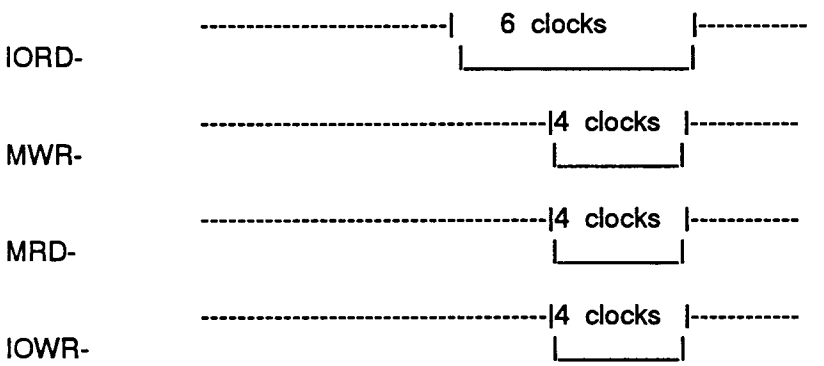
6.8.3 DMA Ready Generator

DMA Ready Generator controls the command width during the DMA cycle. The timing for each DMA cycle (IOCHRDY is not asserted) is defined in 8Mhz clock as follows :

8Mhz mode:



4Mhz mode:



IOCHRDY inactive will cause the DMA cycle to be extended in pairs of 8Mhz clocks.

6.9 Arbiter & Refresh Control

Arbiter & Refresh Control consists of :

- Arbiter
- Memory Refresh Control
- Memory Refresh Address Generator

6.9.1 Arbiter

The Arbiter is a state machine running at 8Mhz and monitoring the DMA request from DMA control unit, memory refresh request ,and CPU shutdown and sleep mode request and hold the CPU by making HOLD line active. Once the CPU recognizes the request, it will grant the bus through the HLDA line and release the bus. At the end of either DMA or memory refresh cycle , the arbiter checks if there is another request pending. If there is one, it will continue to give the bus to the one that requests, otherwise it will release the bus by making HOLD line inactive.

The CPU shutdown/sleep mode can be selected by programming index port 03.In these modes, CPU is held and refresh request is still generated from the OTI042 with the arbiter still granting refresh cycles that PCA and LA are both driven with refresh address even after the refresh cycle.

6.9.2 Memory Refresh Cycle

Memory Refresh Request is generated approximately every 15us from 8254 channel 1 inside the OTI042. REFRQT is fed to the arbiter of the OTI041. Once the arbiter grants the cycle (MREF- is asserted), it outputs the MEMRD- signals. The minimum refresh cycle is five 8Mhz clocks.

The OTI041 also supports slow refresh DRAM. When this feature is enabled, onboard memory will be refreshed 8 times slower to reduce power consumption although the arbiter still grants the refresh request at the same regular period of 15us.

In laptop application, staggered refresh can be selected by setting bit6 of index port 0EH which will make RAS signal to be asserted one after another instead of all at the same time. This can reduce instantaneous power surge during refresh. To further reduce power dissipation during refresh, CAS-before-RAS cycle is also supported and can be selected optionally with or without staggered refresh.

Setting bit1 of index port 1AH will enable CAS-before-RAS refresh cycle.

6.9.3 Memory Refresh Address Generator

Memory Refresh Address Generator drives all 24 address lines through the CPU bus during memory refresh cycle time (MREF- is low). Address 0-9 is output from a 10 bit binary counter (which will be incremented at the end of the cycle); PC address 10 - 15 are all 0 and PC16-19 and LA17-23 comes from page register during the memory refresh cycle.

6.10 Address Buffers

The OTI041 integrates all the address buffers that are used for driving the AT bus. The propagation delay for all the buffers are 25ns. The output current on the AT bus side is 12mA at a capacitive loading of 120pF for PCA bus and 8mA at a capacitive loading of 80pF for LA bus.

6.11 Local Bus Support

6.11.1 Video Interface

The OakNote™ Notebook PC subsystem features excellent video performance . The OTI041 is designed to be tightly coupled with OTI043. The OTI043 resides on the CPU local bus instead of the AT

bus. Video memory accesses can be running at zero wait state at full system speed(up to 20Mhz) as compared to one wait state on the 8Mhz AT bus. With the command caching circuitry already built-in to OTI043 & the local bus video support provided by OTI041, video performance is no longer limited by the bus bandwidth. The local bus video support function is fully integrated inside the OakNote™ subsystem. There is no need for any external component for the implementation.

6.11.2 Programmable Memory Address Space for External Memory Device

OTI041 features a programmable memory address space such that the OTI041 would not response to any memory accesses within the programmed address space. One useful implementation for this programmable feature would be to define a larger memory space for the video buffer other than the A0000-AFFFF area for VGA. Another possible application would be an external Memory Controller that can access the local on board memory.