T-52-33-05

OTI-020 286/386SX Desktop Chip Set

Features

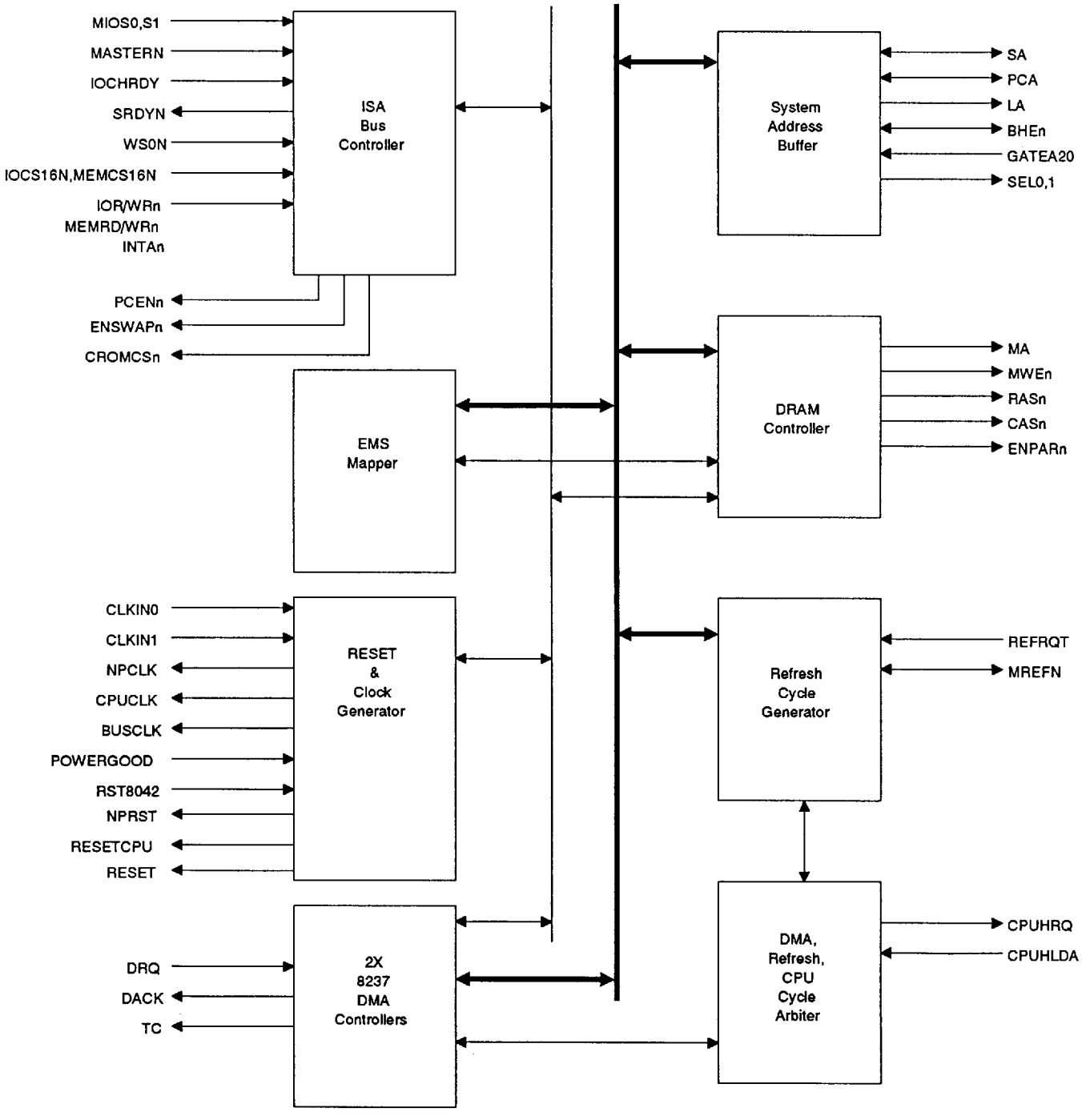
■ Supports 286 and 386SX CPU for 8 MHz to 25 MHz system speed.	*Reduced inventory, same design for 286 & 386SX systems.*
■ Highly integrated design	*OTI-021, OTI-022, I/O Controller, 8042, 1 TTL*
■ On-chip Address & Data path	*no external buffers*
■ EMS 4.0 Hardware support with 2 maps of 60 registers each	*high-performance EMS driver*
■ 287 support with 386SX	*low cost floating point solution*
■ Async/Sync AT Bus	*flexible bus speed*
■ Selectable memory cycle	*supports many vendor's DRAMs*
■ 82385SX support	*cache system support*
■ PAGE and NO PAGE mode support	*increases performance*
■ Peripheral chip select signals	*no external decode logic for HDD, FDD, Video, Keyboard, Parallel port & two serial ports*
■ Fast RESET & GATE 20	*optimized for OS/2 support*
■ In-circuit test mode	*simplifies board level testing*
■ On-chip RTC with 128 bytes RAM	*prolonged battery life*
■ 8- or 16-bit BIOS ROM	*saves board space*
■ Turbo Speed Control	*changes CPU clock speed through a hardware switch*

General Description

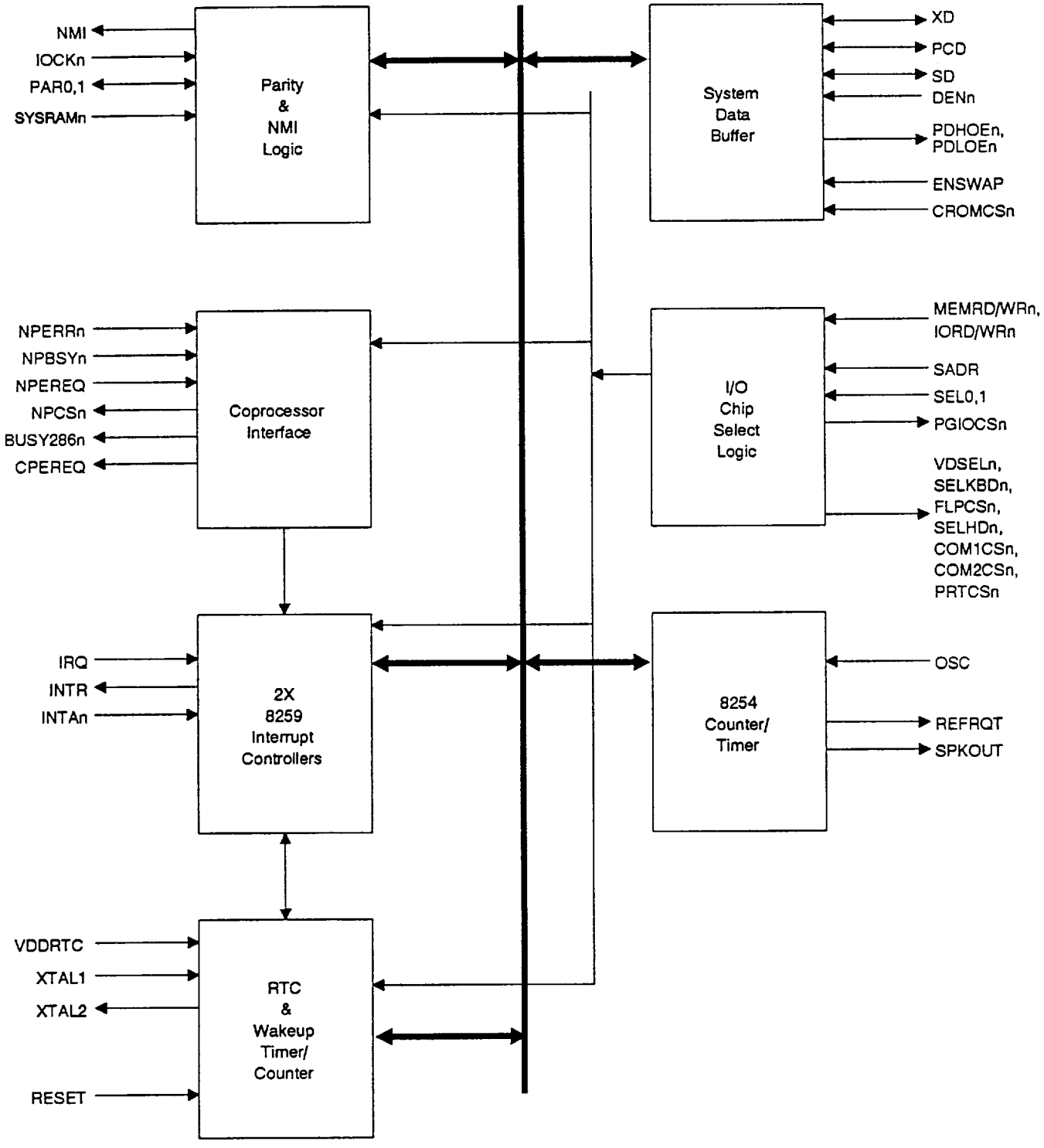
The OTI-020 system chipset is a highly integrated, semi-custom chipset designed for 80286 and 80386SX systems with clock speeds ranging from 8 MHz to 25 MHz. This chipset consists of the System Controller (OTI-021) and the Intelligent Peripheral Controller (OTI-022). Both chips are implemented with 1.2 micron HCMOS technology. The OTI-021 is packaged in a 160-pin PJQFP, and the OTI-022 is packaged in a 144-pin PJQFP.

The OTI-020 chipset brings to systems designers an optimal solution for implementing a low cost, high performance PC/AT system. The 2/4-way interleaving and page-mode addressing scheme of the OTI-020 allows system designers to achieve very high system performance without the need for a complicated cache system design. For those users who require the utmost performance, the OTI-020 chipset does support an external 82385SX cache controller. To implement a full function PC/AT system, all that is required would be the OTI-021, OTI-022, CPU, ROM, RAM, 8042, I/O Controller, graphics controller, and one 7406. This system provides an amazing PC board area savings. The single-chip AT solutions normally require a lot of external TTL components to complete the system design.

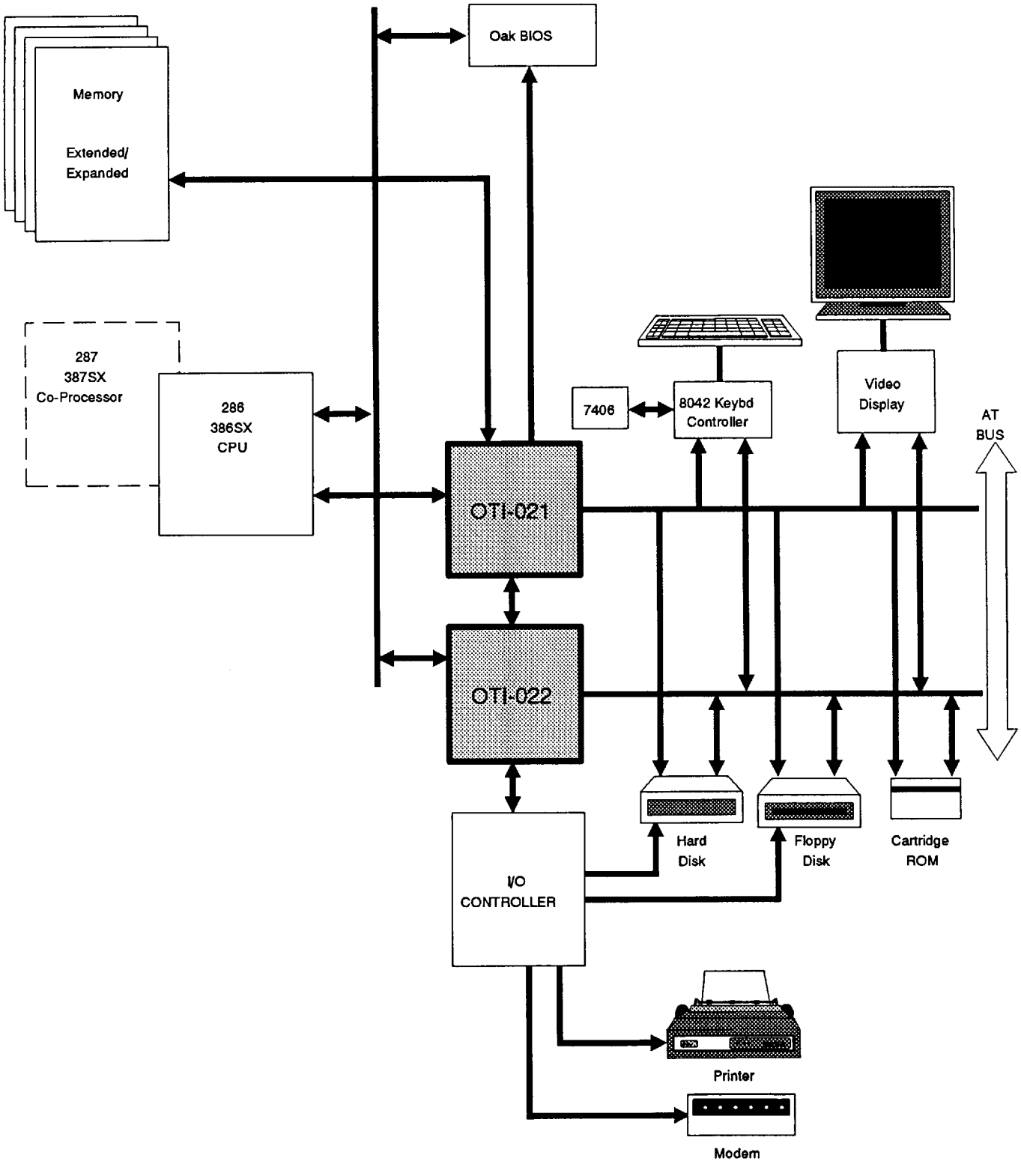
OTI-021 Chip Block Diagram



OTI-022 Chip Block Diagram



System Block Diagram



OTI-021 Pin Description

Pin Name	Pin Number	Pin Type	Description
CPU Interface			
SA[23:0]	TBA	I	CPU ADDRESS BUS
BHEn	TBA	I	BYTE HIGH ENABLE. An active-low signal used to enable data on to the most significant half of the data bus (D15 - D8).
RESETCPU	TBA	O	RESET CPU. An active-high output to reset the CPU.
NPRST	TBA	O	CO-PROCESSOR RESET. An active-high signal to reset the numerical co-processor.
ADSn	TBA	I	ADDRESS STROBE. An active-low signal coming from 80386SX. This input is also used to detect the presence of 386SX. This pin should be pulled low with a 20K-ohm resistor.
S1 - S0	TBA	I	BUS CYCLE STATUS. These signals together with M/IO and COD/INTAn are used to decode different bus cycles. S0 and S1 are connected to W/Rm and D/Cm, respectively.
M/IOn	TBA	I	MEMORY OR I/O CYCLE. An input signal from CPU indicating whether the present cycle is memory or I/O access.
CPUCLK	TBA	O	CPU CLOCK. A MOS driven clock signal to the 80286/80386SX CPU. The frequency is programmable through index port 0003H.
NPCLK	TBA	O	CO-PROCESSOR CLOCK. Clock signal for 80287 or 80387SX. This clock can be programmed to stop if co-processor is not used.
SRDYn	TBA	O	SYSTEM READY. An active-low signal to acknowledge the CPU that the data transfer for either memory or I/O is complete.
DMA Interface			
DRQ0-3 DRQ5-7	TBA	I	DMA REQUEST. These are asynchronous active-high channel request inputs used by peripheral devices to obtain DMA service.
DACK0-3 DACK5-7	TBA	O	DMA ACKNOWLEDGE. These are active-low signals to notify the individual peripheral that it has been granted a DMA cycle.
CPUHRQ	TBA	O	HOLD REQUEST. An active-high signal connected directly to HOLD of the CPU. This signal is used by the chip to request the bus from the CPU.
CPUHLDA	TBA	I	HOLD ACKNOWLEDGE. An active-high signal connected directly to HLDA of CPU. This signal is used by the chip to determine if the bus request has been granted by the CPU.
TC	TBA	O	TERMINAL COUNT. An active-high output pulse signal when the terminal count for any DMA channel is reached.

Pin Name	Pin Number	Pin Type	Description
Bus Interface			
PCA[19:0]	TBA	I/O	PC BUS ADDRESS (19-0). These are the latched version of SA(0-19) and become input during MASTER mode.
LA[23:17]	TBA	I/O	UNLATCHED ADDRESS (23-17). These are the unlatched version of SA(23-17). The bus become input when MASTERn is active.
PBHEn	TBA	I/O	I/O CHANNEL BYTE HIGH ENABLE. An active-low signal on the I/O channel. It is a latched version of BHEn. When MASTERn is low, it becomes input.
WS0n	TBA	I	ZERO WAIT STATE. An active-low signal indicating the present cycle can be completed without any more wait state.
IOCS16n	TBA	I	16-BIT I/O CHIP SELECT. An active-low input that indicates to the system that the present data transfer is a 1 wait-state, 16-bit I/O cycle.
MEMCS16n	TBA	I	16-BIT MEMORY CHIP SELECT. An active-low input that indicates to the system that the present data transfer is a 1 wait-state, 16-bit memory cycle.
PCALE	TBA	O	PC ADDRESS LATCH ENABLE. An active-high pulse signal during phase 2 of TS(T1p or T2 for 80386SX) of any bus cycle and is always high when the CPU is held. It is synchronized to BUSCLK.
IOCHRDY	TBA	I	I/O CHANNEL READY. An active-high ready signal from an I/O channel. It is pulled low by a memory or I/O device to lengthen memory or I/O cycles.
IORDn	TBA	I/O	I/O READ COMMAND. An active-low command to instruct the I/O device to drive its data onto the data bus. It is input when MASTERn is active.
IOWRn	TBA	I/O	I/O WRITE COMMAND. An active-low command to instruct the I/O device to read the data present on the data bus. It is input when MASTERn is active.
MEMRDn	TBA	I/O	MEMORY READ COMMAND. An active-low signal to instruct the memory subsystem to drive its data onto the data bus. It is input when MASTERn is active.
MEMWRn	TBA	I/O	MEMORY WRITE COMMAND. An active-low signal to instruct the memory subsystem to store the data present on the data bus. It is input when MASTERn is active.
BUSCLK	TBA	O	PC-BUS CLOCK. An MOS driven clock signal for the I/O channel.

Pin Name	Pin Number	Pin Type	Description
System Interface			
INTAn	TBA	O	INTERRUPT ACKNOWLEDGE. An active-low signal to enable the interrupt controller's interrupt-vector data onto the data bus.
GATEA20	TBA	I	GATE A20. An active-high signal from the 8042 used to gate address A20.
RST8042n	TBA	I	RESET FROM 8042. An active-low signal from the 8042 to reset the CPU.
CHKCLKn	TBA	I	CHANGE SYSTEM SPEED. An active-low input signal from the OTI-022 indicating change of system speed.
PCENn	TBA	O	PC DATA BUS ENABLE. An active-low control signal to enable the data buffer between CPU and PC data bus. PCENn is active low if: 1. CPU I/O read/write cycle, except co-processor I/O. 2. CPU memory read/write cycle, except onboard RAM and ROM. 3. Interrupt acknowledge cycle (INTAn active).
ENSWAPn	TBA	O	ENABLE DATA SWAP. An output to control the output enable of the byte swapping data buffer.
ROMCSn	TBA	O	ROM CHIP SELECT. An active-low output signal used to enable the ROM BIOS to output data onto the data bus.
CROMCSn	TBA	O	CARTRIDGE ROM CHIP SELECT. An active-low output signal used to access the cartridge ROM.
SEL0	TBA	I/O	SELECT FUNCTION 0. One of the two address encoding signals.
SEL1	TBA	O	SELECT FUNCTION 1. Together with SEL0, encodes the following address ranges: SEL1 SEL0 FUNCTION 0 0 Nothing selected 0 1 A15 - A10 = 0 (I/O) or onboard video RAM 1 0 onboard video ROM 1 1 I/O channel memory but within 1M
PWRGOOD	TBA	I	POWER GOOD. An active-high signal from the power supply after DC power level is stable.
XD[7:0]	TBA	I/O	XDATA BUS. A bidirectional data lines for accessing this chip.
REFRQT	TBA	I	MEMORY REFRESH REQUEST. The memory refresh request input signal from 8254 Timer channel 1 which comes from the OTI-022.
MREFn	TBA	I/O	MEMORY REFRESH. An active-low signal indicating that refresh cycle is going on.

Pin Name	Pin Number	Pin Type	Description
System Interface (Continued)			
ENPARn	TBA	O	ENABLE MEMORY PARITY. An active-low output signal indicating that onboard RAM is being accessed.
RMRDn	TBA	I/O	ROM/RAM READ. An active-low signal indicating that onboard ROM or RAM is being read. It is an input representing the signal NPBSYn when accessing 80287 operation code for 80386SX CPU.
Memory Interface			
MA[11:1]	TBA	I/O	MEMORY ADDRESS (1-11). During memory cycles, this is a time multiplexed memory address bus for 1M memory type (for 256K memory type MA(10,11) is not used).
RAS0n - RAS3n	TBA	O	ROW ADDRESS STROBE (0 - 3). These are active-low control signals to the onboard DRAM to strobe the row address.
CASH0-3n - CASL0-3n	TBA	O	COLUMN ADDRESS STROBE (High & Low). These are active low control signals to on board DRAM to strobe the column address: CASHn for odd bytes D(15-8) and CASLn for even bytes D(7-0).
MWEn	TBA	O	MEMORY WRITE ENABLE. An active-low output used to control memory read/write cycles.
Miscellaneous			
CLKIN0	TBA	I	CLOCK INPUT 0. A 32 MHz TTL clock input with 50% duty cycle. It is used for: the CPU clock generation with CPU running at 8 or 16 MHz, asynchronous bus clock generation, and memory refresh time.
CLKIN1	TBA	I	CLOCK INPUT 1. An optional 20/25/40/50 MHz CMOS clock input with 50% duty cycle. It is used for CPU clock generation with CPU running at 10, 12.5, 20, and 25 MHz.
VDD	TBA	I	POWER: +5 V supply.
VSS	TBA	I	GROUND:

OTI-022 Pin Description

Pin Name	Pin Number	Pin Type	Description
CPU Interface			
CPUHLDA	TBA	I	CPU HOLD ACKNOWLEDGE. This input signal is active when the CPU releases the control of the bus.
SD[15:0]	TBA	I/O	CPU DATA BUS (0-15). The CPU data bus.
System Interface			
DENn	TBA	I	DATA BUFFER ENABLE. An active-low input control signal to enable/disable the internal data transceiver between SD(0-15) and PCD(0-15).
PDLDIRn	TBA	O	EXTERNAL DATA BUFFER OUTPUT ENABLE. An active-low output control signal to enable output for the external data transceiver between PCD(0-7) and slot data bus(0-7).
PDHDIRn	TBA	O	EXTERNAL DATA BUFFER OUTPUT ENABLE. An active-low output control signal to enable output for the external data transceiver between PCD(8-15) and slot data bus(8-15).
ENSWAPn	TBA	I	ENABLE DATA SWAP. An active-low input signal used for enabling the byte swapping data buffer.
XD[7:0]	TBA	I/O	XD BUS. Bidirectional data lines to/from the XD bus for accessing onboard peripherals.
IORDn	TBA	I	I/O READ COMMAND. An active-low input command to instruct the I/O device to drive its data onto the data bus.
IOWRn	TBA	I	I/O WRITE COMMAND. An active-low input command to instruct the I/O device to read the data present on the data bus.
MEMRDn	TBA	I	MEMORY READ COMMAND. An active-low input signal to instruct the memory sub-system to drive its data onto the data bus.
MEMWRn	TBA	I	MEMORY WRITE COMMAND. An active-low input signal to instruct the memory sub-system to read the data present on the data bus.
REFRQT	TBA	O	REFRESH REQUEST. Indicates to the arbiter in the OTI-021 that DRAM needs refreshing.
CROMCSn	TBA	I	CARTRIDGE ROM CHIP SELECT. An active-low input signal from the OTI-021 indicating cartridge ROM is being accessed.
SEL0	TBA	I/O	SELECT FUNCTION 0. One of the two address encoding signals. It is output during refresh period as TURBO signal for the OTI-021.

Pin Name	Pin Number	Pin Type	Description
SEL1	TBA	I	SELECT FUNCTION 1. Together with SEL0 encodes the following address ranges: SEL1 SEL0 FUNCTION 0 0 Nothing selected 0 1 A15 - A10 = 0 (I/O) or onboard video RAM 1 0 onboard video ROM 1 1 I/O channel memory but within 1M and not including onboard video RAM and ROM
ROMCSn	TBA	I	ROM CHIP SELECT. An active-low signal used to enable the ROM BIOS to output data on to the data bus.
VDPMSELn	TBA	O	VIDEO ROM CHIP SELECT. The chip select signal for on board video ROM.
VDSEL/VGAEN	TBA	O	VIDEO CHIP SELECT/VGA ENABLE. The chip select signal for on board video I/O and RAM address space, special for OAK VGA OTI-037. If IBM compatible VGA is used, this pin becomes VGA enable signal.
82385SX Support			
FGA20	TBA	O	FAST GATE A20
FLUSH	TBA	O	FLUSH CACHE. This pin acts as cache flush when EMS mapper is updated.
Bus Interface			
PCMEMRDn	TBA	O	MEMORY READ COMMAND. An active-low signal to instruct the memory sub-system within 1M on the I/O channel to drive its data onto the data bus.
PCMEMWRn	TBA	O	MEMORY WRITE COMMAND. An active-low signal to instruct the memory sub-system within 1M on the I/O channel to store the data present on the data bus.
PCAEN	TBA	O	ADDRESS ENABLE. A signal to de-gate the I/O devices from the I/O channel and allow DMA transfers to take place.
MASTERn	TBA	I	MASTER. This signal is used together with a DRQ line to gain control of the system.
PCD[15:0]	TBA	I/O	I/O CHANNEL DATA BUS (0-15). The I/O channel data bus. There are two sets of data transceivers that are connected internally, (i.e., between SD(0-7) and PCD(0-7) and between SD(8-15) and PCD(8-15)).
SADR[9:0]	TBA	I	ADDRESS BUS. The I/O channel address bus.
PBHEn	TBA	I	BYTE HIGH ENABLE.
MREFn	TBA	I	MEMORY REFRESH CYCLE. An active-low signal indicating that the system is in the memory refresh cycle.

Pin Name	Pin Number	Pin Type	Description
Real Time Clock			
XTAL1	TBA	I	XTAL INPUT FOR RTC. The crystal input for the built-in real time clock.
XTAL2	TBA	O	XTAL OUTPUT FOR RTC. The crystal output for the built-in real time clock.
VDDRTC	TBA	I	POWER. Battery power for the built-in Real Time Clock.
Reset Generation			
PWRGOOD	TBA	I	POWER GOOD. PWRGOOD comes from the power supply to indicate that power is stable.
RESET	TBA	O	RESET. An active-high signal synchronized to the CPU clock to reset the system.
Timer Counter			
SPKOUT	TBA	O	SPEAKER DATA OUTPUT. Speaker output data, to be connected to a speaker driver to drive the speaker or beeper.
Interrupt Controller			
IRQ1, IRQ3-7 IRQ9-12, IRQ14-15	TBA	I	INTERRUPT REQUEST INPUTS. asynchronous interrupt request inputs to the internal 8259 controllers.
INTR	TBA	O	INTERRUPT REQUEST. Interrupt request to the CPU and is generated whenever a valid IRQ is received.
INTAn	TBA	I	INTERRUPT ACKNOWLEDGE. An active-low signal from the OTI-041 indicating that an interrupt acknowledge cycle is in progress.
Keyboard and Mouse Interface			
SELKBDn	TBA	O	SELECT KEYBOARD. An active-low signal indicating that the keyboard controller is selected.
Floppy Disk Controller			
FLPCSn	TBA	O	FLOPPY SELECT. An active-low signal used to select the floppy disk controller.
DACK2n	TBA	I	DMA ACKNOWLEDGE. An active-low signal indicating that the floppy disk controller has been granted a DMA cycle.
Hard Disk Controller			
SELHDK1n	TBA	O	HARD DISK SELECT2. When Conner's hard disk is installed, this pin is used as one of the chip select signal decoding addresses 3F6H & 3F7H.
SELHDK0n	TBA	O	HARD DISK SELECT1. An active-low signal to select on-board hard disk drive.

Pin Name	Pin Number	Pin Type	Description
Co-processor Interface			
NPERRn	TBA	I	NUMERICAL PROCESSOR ERROR. An active-low input indicating that an unmasked exception has occurred during numeric instruction execution when the co-processor interrupt is enabled.
NPBSYn	TBA	I	NUMERICAL PROCESSOR BUSY. An active-low input connected directly to the BUSY signal of the co-processor.
NPCSn	TBA	O	NUMERICAL PROCESSOR CHIP SELECT. An active-low output to select the co-processor.
BUSY286n	TBA	O	BUSY TO CPU. An active-low output connected directly to the BUSY input of the CPU.
NPPREQ	TBA	I	NUMERICAL PROCESSOR REQUEST. An active-high input indicating that the co-processor is requesting an operand transfer. This pin comes from the PEREQ output of the co-processor.
CPEREQ	TBA	O	CPU REQUEST. An active-high output to the CPU indicating to the CPU that the co-processor is requesting an operand transfer.
NMI Generation			
IOCKn	TBA	I	I/O CHANNEL CHECK. An active-low input indicating that an I/O channel error condition is detected.
PAR0 - PAR1	TBA	I/O	PARITY BIT (0 - 1). The memory parity bits for even and odd bytes of the memory bank. Each parity bit is generated and written during the memory write operation. Each is checked and reported on an error to the system at the end of memory read cycle. PAR0 is memory parity bit for even byte, PAR1 is the memory parity bit for odd byte.
SYSRAMn	TBA	I	ENABLE MEMORY PARITY. An active-low input indicating that onboard RAM is being accessed.
RMRDn	TBA	I/O	ROM/RAM READ. An active-low signal indicating that onboard ROM or RAM is being read. RMRDn is an output equal to NPBSYn signal when I/O address F8H is selected.
NMI	TBA	O	NON-MASKABLE INTERRUPT. An active-high output to the CPU indicating that an error has occurred in one of the following areas: memory parity error or I/O channel check signal.
Chip Select Signals			
PGIOCS0n	TBA	O	PROGRAMMABLE I/O CHIP SELECT 0. An active-low I/O chip select signal with a programmable I/O address space.
COM1CSn	TBA	O	SERIAL PORT 1 CHIP SELECT. An active-low I/O chip select signal for the serial port 1.

Pin Name	Pin Number	Pin Type	Description
Chip Select Signals (Continued)			
COM2CSn	TBA	O	SERIAL PORT 2 CHIP SELECT. An active-low I/O chip select signal for the serial port 2.
PRTCSn	TBA	O	PRINTER PORT CHIP SELECT. An active-low I/O chip select signal for the printer port.
PRTOEn	TBA	O	PRINTER PORT OUTPUT ENABLE. An active-low bidirectional printer port output enable signal.
Miscellaneous			
TURBOn	TBA	I	TURBO SPEED SELECTION INPUT. When high (inactive), forces CPUCLK to be 8MHZ. When active low, CPUCLK will be controlled by the speed control register.
OSC	TBA	I	14.318 MHz OSCILLATOR OUTPUT. A 14.318 MHz TTL level clock signal to generate the clock for on-chip 8254.
GND	TBA	I	GROUND: 0V
VCC	TBA	I	POWER: +5V