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Applications Note

Product Name: 82C621A Evaluation Board
Product Revision: 700-0012-001 Revision A.4
Date: July 13, 1994

Overview

The OPTi 82C621A Evaluation Board is a high-performance 32-bit PCI bus IDE adapter based on the OPTi 82C621A PCI bus IDE Controller (PIC) that offers exceptional performance, low part count and excellent compatibility features. The OPTi 82C621A PIC interfaces between the PCI bus and the industry-standard IDE bus (also known as the ATA or AT Attachment bus).

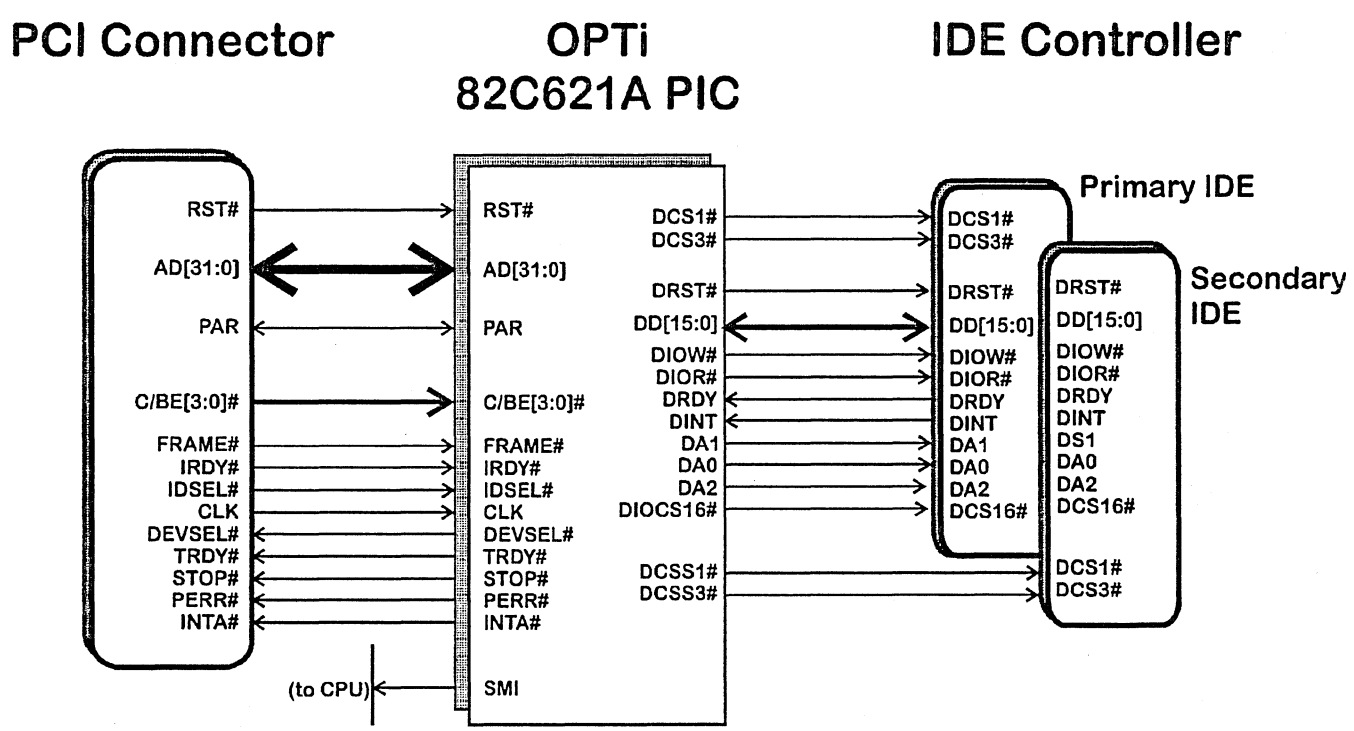
The 82C621A PIC implements single PCI functions to directly support both a Primary and Secondary IDE in a single 100-pin PQFP. This high-integration approach reduces component count, eases board design, reduces cost, and increases reliability. An integrated four-level read-prefetch FIFO and four-level posted-write FIFO supports zero-wait-state operations, substantially improving performance over other IDE implementations.

Write posting and read-prefetch allows CPU memory cycles to run concurrently with IDE cycles and also removes the synchronization penalty for AT bus transfers. IDE cycles can be fine tuned by the ANSI Mode strap options or programmable registers for ANSI-standard devices (mode 0, 1, 2, or 3)or non-standard devices. 32-bit PCI cycles are translated to two 16-bit IDE cycles for faster data access.

Although the board will work as a standard IDE interface, for top performance the OPTi supplied Setup program and device drivers should be used in DOS and Windows 3.1-based systems.

The complete design is available as a Turn-key Manufacturing Package (TMP) from OPTi, which includes complete schematics, Bill of Material (BOM), original CAD artwork (PADS PCB .JOB file), Gerber photoplotter files and design manual.

Figure 1. Evaluation Board Block Diagram



Installation

Pre-Installation Notes

1. This Quick Setup Guide contains information about how to set up and install the 82C621A adapter board into your system. Please take time to become familiar with the jumper options and locations before installing the card. Refer to the board layout diagram, Figure on page 5, for the location of the jumpers described in this manual.
2. The OPTi 82C621A Evaluation Board will operate in any 100% PCI bus compatible motherboard. Motherboards that do not conform to the PCI standard, or have proprietary extensions to the PCI standard may not function properly with this board.

NOTE *Because there are many different motherboards, controller cards, configurations and setup options, it is the sole responsibility of the user to determine the fitness and functionality of this product.*

3. The software drivers for DOS and Windows 3.1 are supplied on a single diskette.
4. It is recommended that you make a backup copy of the installation diskette(s) and use the backup diskette(s) as your working diskette(s). This will protect the original from unnecessary wear and accidental damage or erasure.

Hardware Installation

These instructions presume that the installer is familiar with both the hardware and software that comprise the target system. Systems should be stable before installing any new hardware or software!

NOTE *If any other IDE controllers have been previously installed in the target system, please remove or disable all drivers that were installed with those cards before continuing.*

1. Power OFF the computer system and connected devices before removing or installing any cards!
2. Remove the cover from the computer and remove any IDE controller boards that have been installed previously in the system.
3. Verify that the 82C621A Evaluation Board is configured with the jumpers in the default configuration, with modifications as required by the target system. It is recommended that the initial installation of the board in an unknown system NOT use any enhanced or special features.
4. It is recommended that the cables to the IDE devices be connected *before* installing the board, so that orientation of the cable is correct. Pin 1 of the connector corresponds with Pin 1 of the IDE cable (marked with a *red* stripe).

NOTE *Your computer may need to be configured for IDE interrupt for support if one of the following conditions apply:*

- **A** *Motherboard and BIOS support IDE Interrupts on the PCI bus (e.g., OPTi82C822 and Phoenix design).*
  No cable needed.
- **B** *Motherboard supports IDE Interrupt header.*
  Connect cable from JP2 to motherboard.
- **C** *Motherboard does not support IDE Interrupts on the PCI bus or header.*
  Connect cable from JP2 to ISA paddle card; insert paddle card into ISA slot.

5. Locate an empty PCI bus slot, install the board firmly into the slot and secure the board.
6. Once the 82C621A Evaluation Board has been properly installed, secure the cover of the computer, and re-attach any cables that were removed during the installation procedure.

NOTE *If the 82C621A Evaluation Board is replacing an existing IDE adapter, the computer system should power-up normally at this point. If this is a new installation, the BIOS drive parameters will need to be set for the drives that have been attached. Also, FDISK, FORMAT and Operating System Installation may need to be done before proceeding to the next step.*

Software Installation (SETUPVIC.EXE)

After you have properly installed the adapter into the target system, you need to run the SETUPVIC.EXE program to complete the installation. SETUPVIC is used to configure the 82C621A adapter and maximize the 82C621A controller, as well as install the DOS and/or Windows device drivers. These device drivers are:

OPTIVIC.SYS	DOS Device Driver Program. Substitutes portions of the BIOS int13 disk-driver to implement 32-bit I/O.
OPTIVIC.386	Windows Virtual Device Driver.

Usage:

```
SETUPVIC <switch> <options>
```

When run with no switch or options, the SETUPVIC.EXE program will run in interactive mode and set the adapter for normal operation. Interactive mode will perform one or all of the following three functions:

1. It will caution the user about any incorrect switch settings (see Section 2.3.3 *Error Messages* for a list of errors that may occur if the switch settings are not correct).
2. SETUPVIC.EXE will install the DOS and WINDOWS Drivers.

   The SETUP VIC program will:

   a. Copy itself (SETUPVIC.EXE) to the hard disk and modify C:\AUTOEXEC.BAT file to invoke itself with the -t option.

   b. Copy the DOS driver OPTIVIC.SYS and modify the CONFIG.SYS file to invoke it.

   c. Copy the WINDOWS 3.1 driver and modify the SYSTEM.INI file to invoke it.
3. SETUPVIC.EXE will initialize the VIC internal registers to fine-tune the IDE drive performance and save these parameters in the AUTOEXEC file.

   After power-up, the SETUPVIC program will automatically execute in non-interactive mode, using the -t option and the following parameters to program the VIC internal registers directly (note that the command will be placed on one line only in the AUTOEXEC.BAT file).

Switches and Options

SETUPVIC -t

```
SETUPVIC -t<drive #> <rd_puls> <rd_recovry>
<wr_puls> <wr_recovry> <prefetch> <addr_setup>
<drdy> <freq>
```

Option	Function	
<drive #>	0:	Drive-0 programming
	1:	Drive-1 programming
<rd_pulse>	Read Pulse width (low-time) in nanoseconds for 16-bit data cycles	
<rd_recovry>	Read Signal High-time in nanoseconds for 16-bit data cycles	
<wr_pulse>	Write Pulse width (low-time) in nanoseconds for 16-bit data cycles	
<wr_recovry>	Write Signal High-time in nanoseconds for 16-bit data cycles	

Option	Function
<prefetch>	ENPREF: Enable read-prefetch feature
	DISPREF: Disable read-prefetch feature
<addr_setup>	Address Setup in nanoseconds for 16-bit data cycles
<drdy>	DCHRDY to end of command pulse width in nanoseconds
<freq>	25MHz: Local-Bus speed at 25Mhz
	33MHz: Local-Bus speed at 33Mhz

NOTE *The parameters in the AUTOEXEC.BAT should not be manually modified.*

Device Drivers

OPTIVIC.SYS

This DOS Device Driver substitutes portions of the BIOS INT13 disk-driver to enable 32-bit I/O supported by the 82C621A VIC, as well as enable the read-and-write-multiple commands supported by most modern drives.

When the user elects to install the DOS driver, SETUPVIC modifies C:\CONFIG.SYS to invoke OPTIVIC.SYS as follows (note that the command should be placed on one line only):

```
DEVICE = <path-name>\OPTIVIC.SYS -m<drive_code>
-c<drive#>=n
```

The `<drive_code>` is a hex digit representing four binary bits which control the use of read/write multiple commands:

<drive_code>	Description	
Bit 0	0	Disable read multiple for Drive-0
	1	Enable read multiple for Drive-0
Bit 1	0	Disable read multiple for Drive-1
	1	Enable read multiple for Drive-1
Bit 2	0	Disable write multiple for Drive-0
	1	Enable write multiple for Drive-0
Bit 3	0	Disable write multiple for Drive-1
	1	Enable write multiple for Drive-1

The `-c` switch limits the maximum number of sectors, n in hex, that can be used in the set-multiple command to the specified drive, `<drive#>`.

NOTE *You must re-boot your system before the changes to your CONFIG.SYS and AUTOEXEC.BAT will take effect.*

OPTIVIC.386

The OPTIVIC.386 allows WINDOWS-3.1 (in Enhanced 386 mode) to utilize 32-bit I/O supported by the 82C621A VIC,

as well as the read- and write-multiple commands supported by most modern drives.

When the user elects to install the WINDOWS-3.1 driver, SETUPVIC modifies the `[386Enh]` section of the SYSTEM.INI file:

Removes:

```
DEVICE=*wdctrl
```

Adds:

```
DEVICE=<path-name>\OPTIVIC.386
```

In addition, SETUPVIC replaces any reference to 32BitDiskAccess by the following:

```
32BitDiskAccess=on
```

This line is added even if there is no reference to 32BitDiskAccess in the original SYSTEM.INI.

Error Messages

When you execute the SETUPVIC.EXE utility, the program will check the 82C621A adapter to ensure that the switch settings are set correctly for the optimum configuration of the drive.

The following messages will be generated as either an ERROR or a WARNING depending upon the capabilities of the drive.

```
Local-Bus Speed-Jumpers set to wrong value:
??MHz
Set these (on Local-IDE adapter & motherboard)
to ??MHz and run SETUPVIC again.
```

```
Mode-Jumpers set to wrong value:??
Set these to Mode-?? and run SETUPVIC again
```

```
Register value is too slow for Drive(s).
```

```
Register value is too slow for Drive-0.
```

```
Register value is too slow for Drive-1.
```

If your drive can support the detected speed or mode, you will be given a WARNING message. This means that you can continue and the drive will work correctly; it just won't be set to the optimum values. If you want the drive to perform at the optimum level, you should set the jumpers to the suggested settings and run SETUPVIC again.

If your drive cannot support the detected speed or mode, you will be given an ERROR message. You need to change the jumper settings and run SETUPVIC again to make sure that the drive will function reliably. If you do not, you will be given the following message:

```
PROCEEDING MAY CAUSE DATA LOSS.
Want to exit (y)?
```

If you respond yes at this point the following message will be displayed:

```
NOTE: Installation aborted.
If you want to see those error messages(s)
again, RE-BOOT the system by powering down and
run SETUPVIC.
```

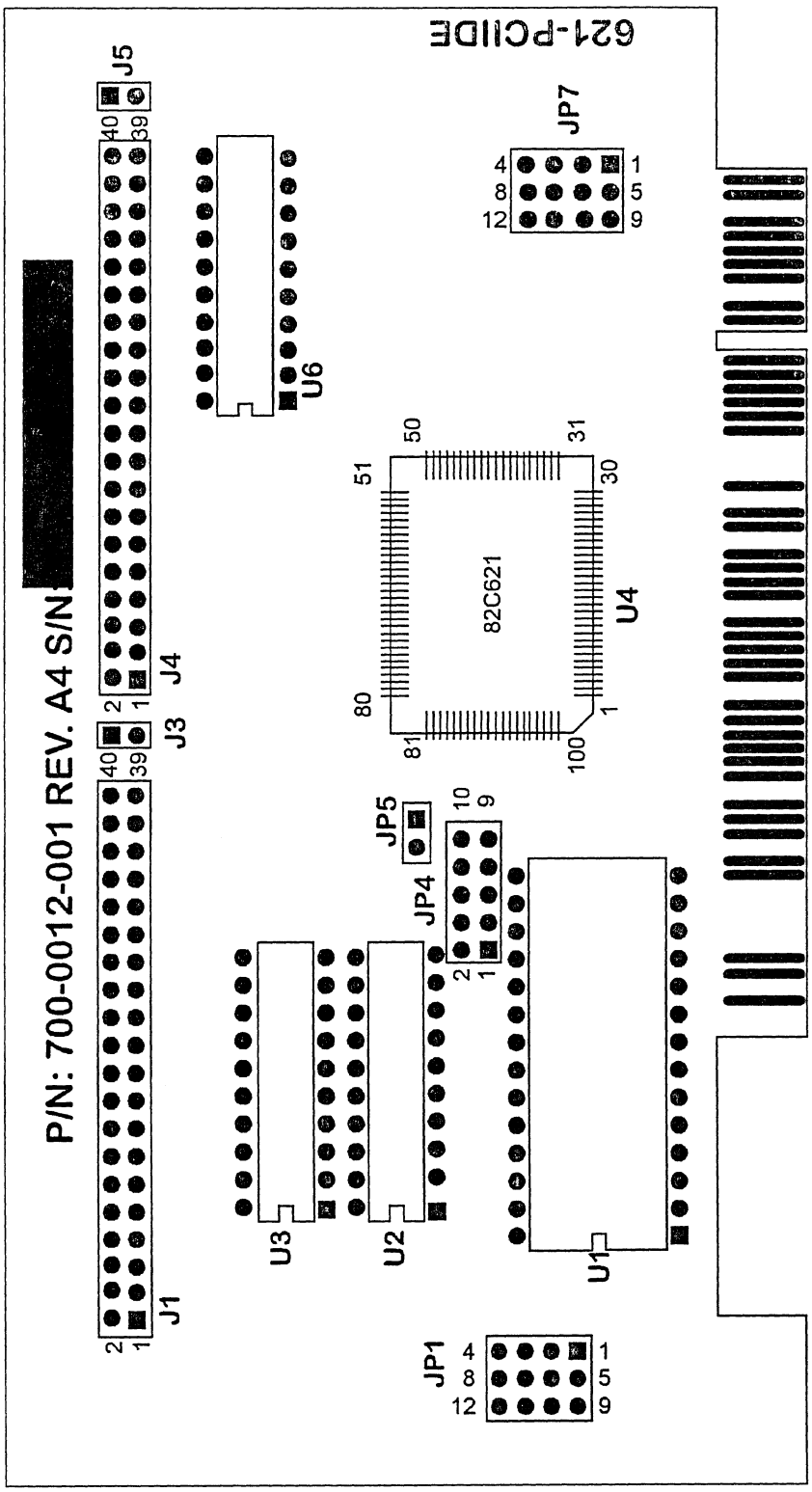
If you respond no, you will be asked:

```
Do you want the prefetch to be turned on (y)?
```

You should respond yes to this question if you insist on running under these conditions.

Hardware Configuration

Figure 2. 82C621A Evaluation Board Layout



Jumper Settings

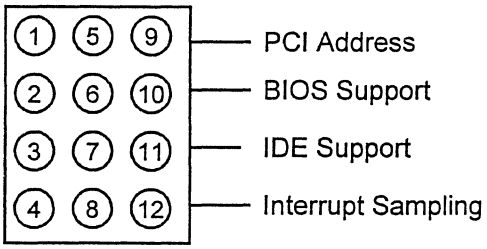
J1 - Secondary IDE Connector

J3 - Secondary HD Active LED Connector

J4 - Primary IDE Connector

J5 - Primary HD Active LED Connector

JP1 - Power On Configuration 1



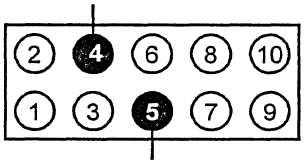
Name	Pins	Description
PCI Address	1-5	Fixed Address
	5-9	Relocatable Address
BIOS Support (with JP5)	2-6	Enabled
	6-10	Disabled
IDE Support	3-7	Primary & Secondary
	7-11	Primary Only
Interrupt Sampling (with JP4)	4-8	Level Triggered
	8-12	Edge Triggered

JP4 - Interrupt Sampling

NOTE *Use with JP1.*

NOTE *Attach cable to this connector for Edge-triggered interrupt only.*

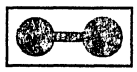
To motherboard IRQ14 line



To motherboard IRQ15 line

JP5 BIOS Enabled

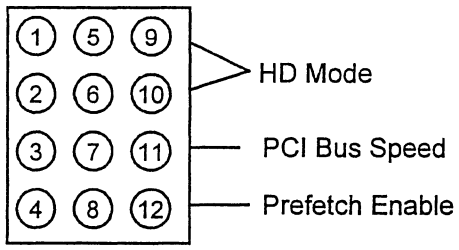
NOTE *Use with JP1.*



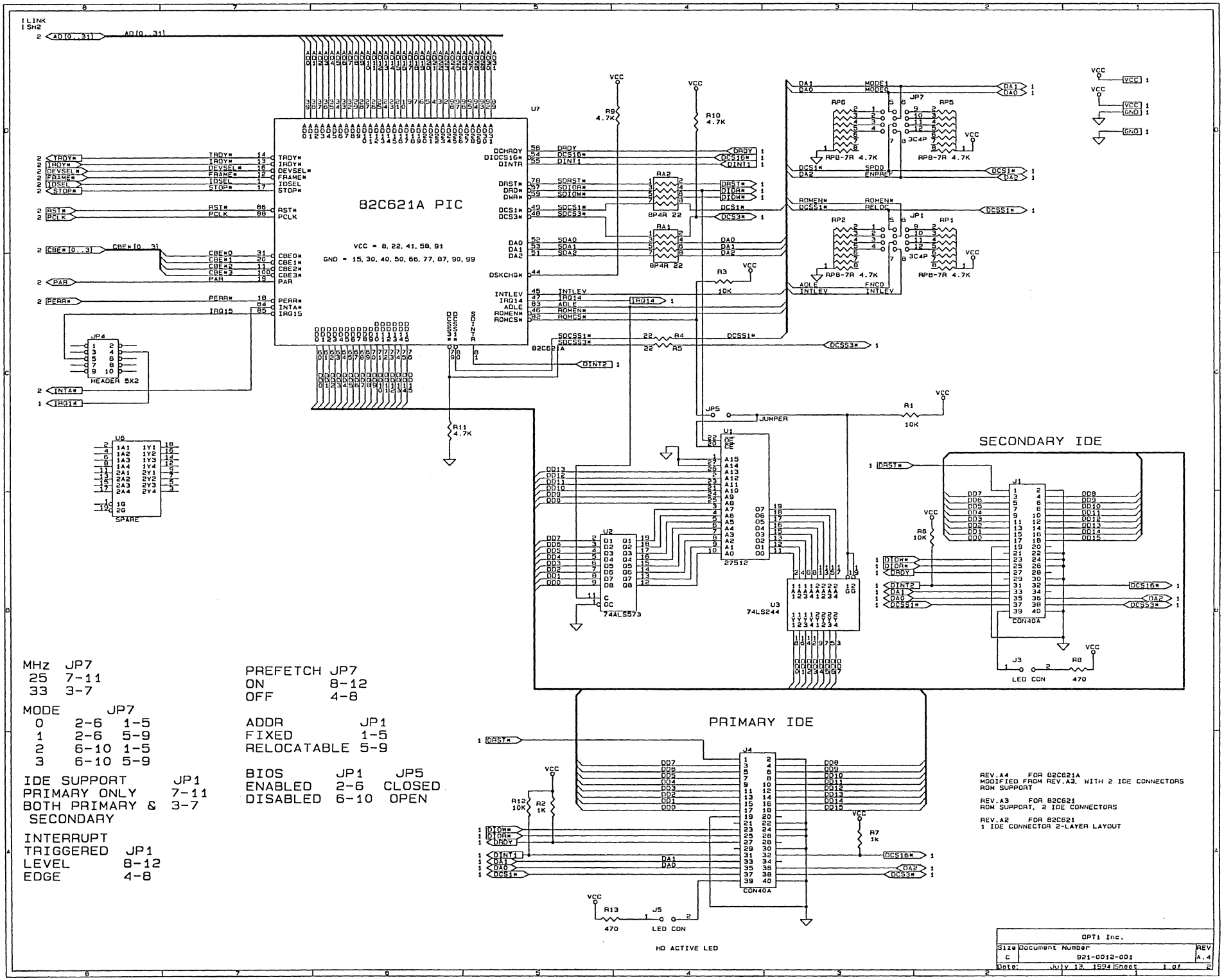
BIOS Enabled

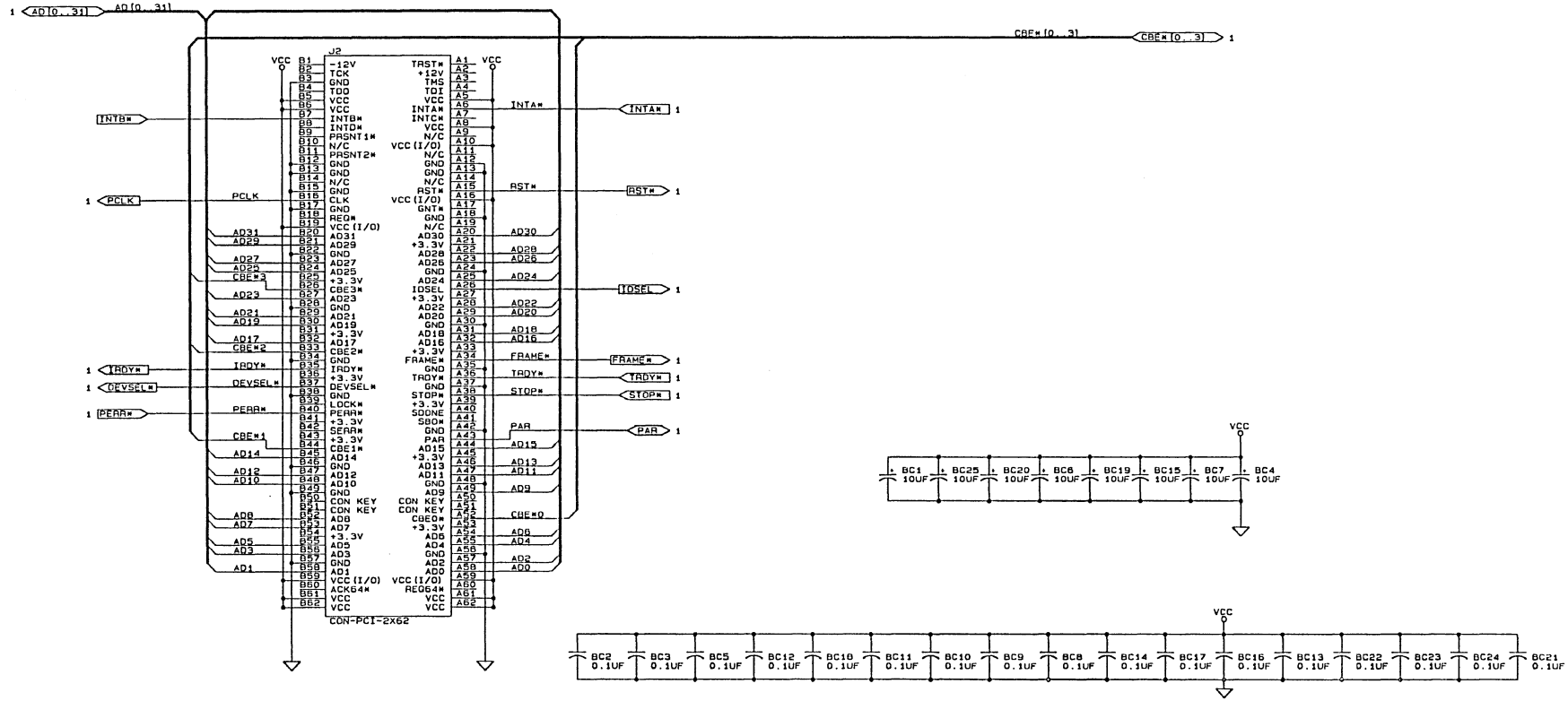
BIOS Disabled

JP7 - Power On Configuration 2



Name	Pins	Description
Hard Drive Mode	1-5 2-6	Mode 0
	5-9 2-6	Mode 1
	1-5 6-10	Mode 2
	5-9 6-10	Mode 3
PCI Bus Speed	3-7	33MHz
	7-11	25MHz
Prefetch Enable	4-8	Prefetch OFF
	8-12	Prefetch ON


82C621A PIC
VCC = 8, 22, 41, 58, 91
GND = 15, 30, 40, 50, 66, 77, 87, 90, 99
SECONDARY IDE
PRIMARY IDE
JUMPER
HEADER 5X2
SPARE
74ALS573
74LS244
27512
CON40A
LED CON
470
MHz JP7
25 7-11
33 3-7
MODE JP7
0 2-6 1-5
1 2-6 5-9
2 6-10 1-5
3 6-10 5-9
IDE SUPPORT JP1
PRIMARY ONLY 7-11
BOTH PRIMARY & SECONDARY 3-7
INTERRUPT TRIGGERED JP1
LEVEL 8-12
EDGE 4-8
PREFETCH JP7
ON 8-12
OFF 4-8
ADDR JP1
FIXED 1-5
RELOCATABLE 5-9
BIOS JP1 JP5
ENABLED 2-6 CLOSED
DISABLED 6-10 OPEN
HD ACTIVE LED
REV.A4 FOR 82C621A
MODIFIED FROM REV.A3, WITH 2 IDE CONNECTORS
ROM SUPPORT
REV.A3 FOR 82C621
ROM SUPPORT, 2 IDE CONNECTORS
REV.A2 FOR 82C621
1 IDE CONNECTOR 2-LAYER LAYOUT
OPTi Inc.
Size C
Document Number 921-0012-001
REV A.4
Date: July 13, 1994 Sheet 1 of 2



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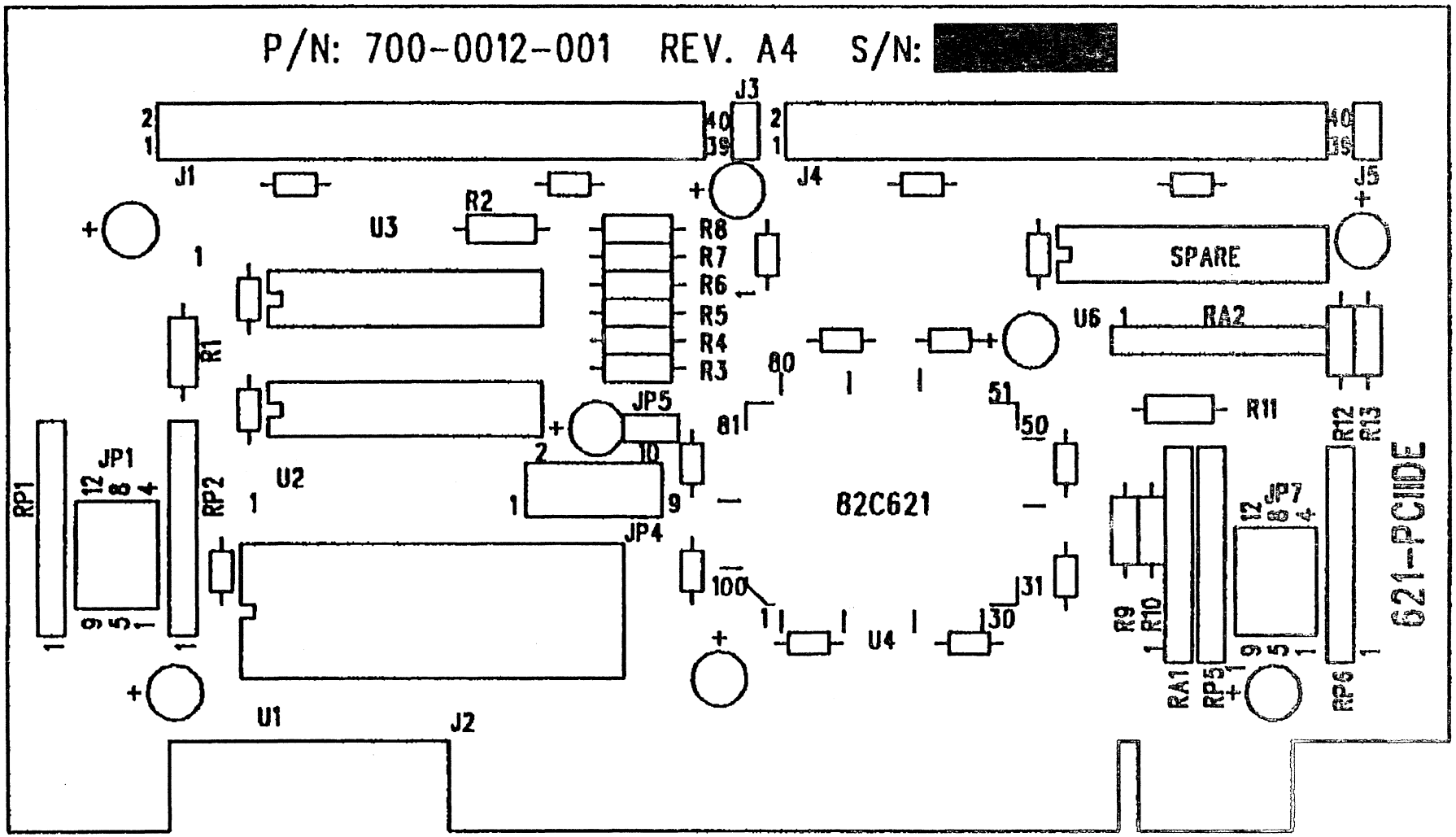

621-PCIIDE REV. A4

SILKSCREEN

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Product Alert #: 2

Date: June 15, 1994

Chipset: 82C621 PCI IDE Controller Chip

Alert Title: Changes from 82C621 to 82C621A

Scope

This alert describes the changes from the 82C621 PCI IDE controller to the 82C621A.

1. Inside the IDE configuration space, the accessing method of the Status Register (offset 06h) bit 15 (PERR) is different. When a 1 is written to this bit, the bit will be cleared. When a 0 is written, the bit remains unchanged.

2. The 82C621A will no longer respond to PCI to PCI bridge address during the configuration cycle.

3. The definition of strap ISA3F7 is changed. The name of the strap is changed to PCI3F7#. If it is 0, 3F7h is read from the local bus (same as earlier version). If it is 1, the 82C621A will not respond to a 3F7h read at all.

   In the earlier version, it will not respond on the PCI bus with DEVSEL#, STOP#, and TRDY#. However, it snooped the cycle to create an IDE cycle and generated RD3F7# and CHRDY to provide data to the ISA bus.

These differences will be reflected in the upcoming release of the 82C621A Data Sheet.