OPTi

82C499

DX System Controller

Data Book

Version 1.0
912-3000-001
August, 1994

OPTi Inc.
2525 Walsh Avenue
Santa Clara, CA 95051
Tel: (408) 980-8178
Fax: (408) 980-8860
BBS: (408) 980-9774

Table of Contents

1.0 Features 1

2.0 Overview 2

3.0 Signal Definitions 3

3.1 Signal Descriptions 6
3.1.1 CPU Interface Signals 6
3.1.2 AT Bus Interface 7
3.1.3 Bus Arbitration Interface Signals 8
3.1.4 Numeric Processor Interface Signals 8
3.1.5 Cache Interface Signals. 8
3.1.6 DRAM Interface Signals 9
3.1.7 82C206 Signal 9
3.1.8 Buffer Control Signals 10
3.1.9 Reset Signals. 10
3.1.10 Clock Signals 10
3.1.11 Miscellaneous Interface Signals 11
3.1.12 Power and Ground Pins. 11

4.0 Functional Description 13

4.1 Reset Logic. 13
4.2 System Clock Generation 13
4.3 CPU Burst Mode Control 13
4.4 Cache Subsystem. 14
4.4.1 Cache Bank Interleave 14
4.4.2 Write-Back Cache 14
4.4.3 Tag RAM 14
4.4.4 Dirty Bit Mechanism. 14
4.5 Local DRAM Control Subsystem 16
4.6 Parity Generation/Detection Logic 17
4.7 Refresh Logic 17
4.8 Shadow RAM 18
4.9 System ROM BIOS Cycles and Flash EPROM Support 18
4.10 AT Bus State Machine 18
4.11 Bus Arbitration Logic. 18
4.12 Numeric Coprocessor Cycles (NPX) 19
4.13 Local Bus Interface 19
4.14 Data Bus Conversion/Data Path Control Logic. 19
4.15 Turbo/Slow Mode Operations 19
4.16 Fast GATEA20 and RESET Emulation. 19
4.17 Special Cycles 19

5.0 Registers Descriptions 21

5.1 I/O Port 60h 27
5.2 I/O Port 64h 27

6.0 Maximum Ratings 29

6.1 Absolute Maximum Ratings 29
6.2 DC Characteristics 29
6.3 AC Timing Characteristics 30
6.4 AC Timing Waveforms 33

7.0 Mechnical Package Outline 65

List of Figures

Figure 1-1 Address and Data Path Clock Diagram 1
Figure 3-1 Pin Diagram 3
Figure 6-1 2-1-1-1 Double Bank Cache Read Hit Cycle 33
Figure 6-2 3-1-1-1 Single Bank Cache Read Hit Cycle 34
Figure 6-3 Zero-Wait State Write Hit Cycle 35
Figure 6-4 One-Wait State Cache Write Hit Cycle 36
Figure 6-5 DMA/ISA Master Transfer 37
Figure 6-6 One-Wait State DRAM Read 38
Figure 6-7 One-Wait State DRAM Page Hit Burst Read 39
Figure 6-8 One-Wait State DRAM Burst Read, RAS# Inactive 40
Figure 6-9 One-Wait State DRAM Page Miss Burst Read 41
Figure 6-10 Zero-Wait State DRAM Write 42
Figure 6-11 One-Wait State DRAM Write 43
Figure 6-12 ISA Bus Cycles 44
Figure 6-13 Keyboard Controller Access Cycles 45
Figure 6-14 CPU Reset 46
Figure 6-15 Refresh Cycle 47
Figure 6-16 Cache Read Miss Dirty: 2 banks of cache and 0/0 DRAM wait state (1 of 2) . . 48
Figure 6-17 Cache Read Miss Dirty: 2 banks of cache and 0/0 DRAM wait state (2 of 2) . . 49
Figure 6-18 Cache Read Miss Dirty: 1 bank of cache and 0/0 DRAM wait state (1 of 2) . . . 50
Figure 6-19 Cache Read Miss Dirty: 1 bank of cache and 0/0 DRAM wait state (2 of 2) . . . 51
Figure 6-20 Cache Read Miss Dirty: 2 banks of cache and 1/1 DRAM wait state (1 of 2) . . 52
Figure 6-21 Cache Read Miss Dirty: 2 banks of cache and 1/1 DRAM wait state (2 of 2) . . 53
Figure 6-22 Cache Read Miss Dirty: 1 bank of cache and 1/1 DRAM wait state (1 of 2) . . . 54
Figure 6-23 Cache Read Miss Dirty: 1 bank of cache and 1/1 DRAM wait state (2 of 2) . . . 55
Figure 6-24 Cache Read Miss Not Dirty: 2 banks of cache and 0 DRAM read wait state . . . 56
Figure 6-25 Cache Read Miss Not Dirty: 2 banks of cache and 1 DRAM read wait state . . . 57
Figure 6-26 ROM Access Cycle (1 of 2) 58
Figure 6-27 ROM Access Cycle (2 of 2) 59
Figure 6-28 DMA Device Read from VESA Slave 60
Figure 6-29 DMA Device Write to VESA Slave 61
Figure 6-30 ISA Master Read from VESA Slave 62
Figure 6-31 ISA Master Write to VESA Slave 63

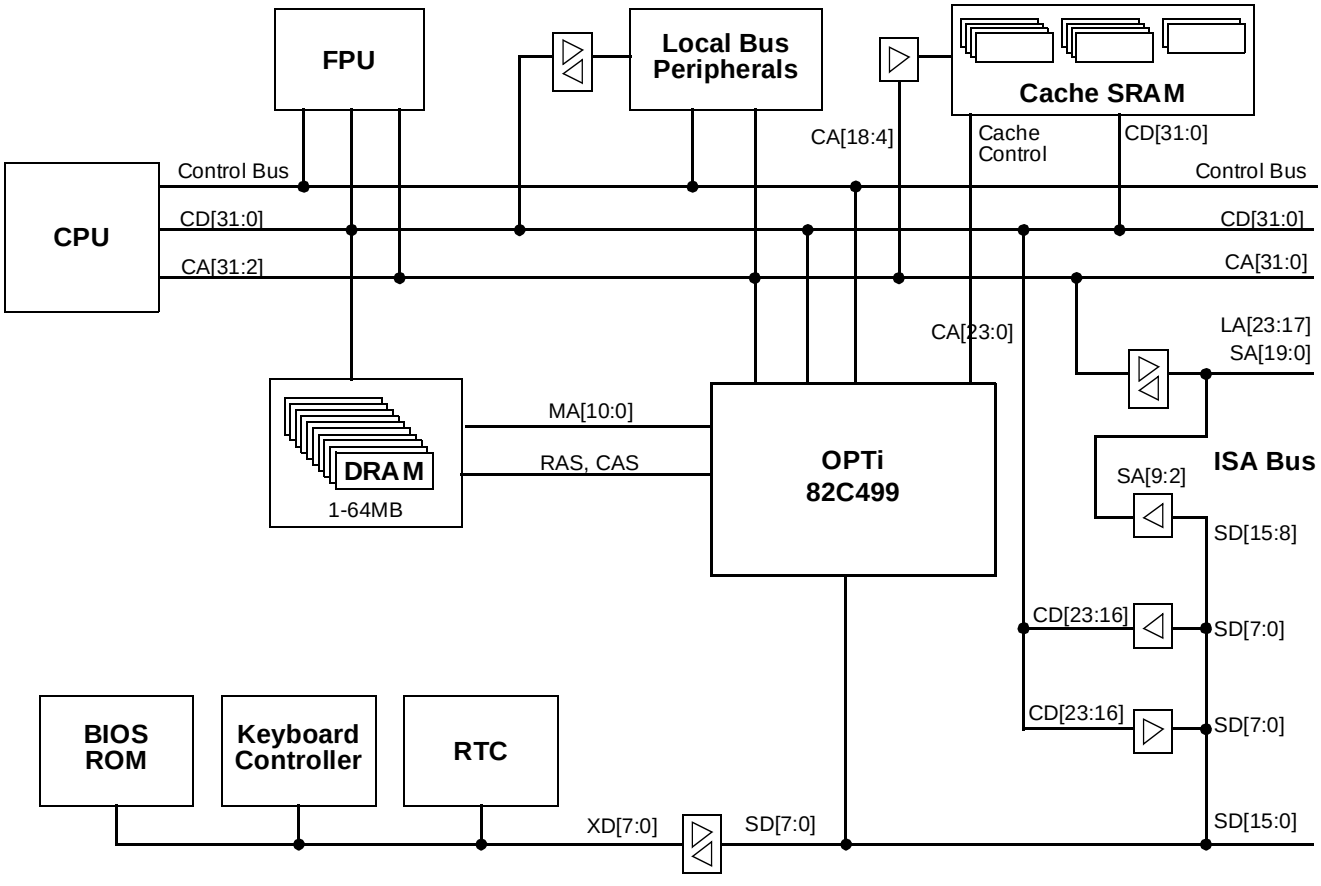
List of Tables

Table 3-1 Numerical Pin Cross-Reference List 4
Table 3-2 Alphabetical Pin Cross-Reference List 5
Table 4-1 Address to Tag Bit Mapping 14
Table 4-2 Cache SRAM Requirements 15
Table 4-3 SRAM Speed Requirements 15
Table 4-4 DRAM Configurations 16
Table 4-5 CPU Address to MA Bus Mapping 17
Table 5-1 Control Register 1 - Index: 20h 21
Table 5-2 Control Register 2 - Index: 21h 21
Table 5-3 Shadow RAM Control Register I - Index: 22h 22
Table 5-4 Shadow RAM Control Register II - Index: 23h 22
Table 5-5 DRAM Control Register I - Index: 24h 23
Table 5-6 DRAM Control Register II - Index: 25h 23
Table 5-7 Shadow RAM Control Register III - Index: 26h 24
Table 5-8 Control Register 3 - Index: 27h 24
Table 5-9 Non-Cacheable Block 1 Register - Index: 28h 25
Table 5-10 Non-Cacheable Block 1 Register II - Index: 29h 25
Table 5-11 Non-Cacheable Block 2 Register I - Index: 2Ah 26
Table 5-12 Non-Cacheable Block 2 Register II - Index: 2Bh 26
Table 5-13 ROM Chip Select (ROMCS#) Control Register - Index: 2Dh 26
Table 5-14 I/O Port 61h(Port B) 27
Table 5-15 I/O Port 70h 27
Table 5-16 Port 92h - System Controller Port A, PS/2 Compatibility Port 27
Table 6-1 82C499 B1 AC Characteristics 30

1.0 Features

- Supports Intel® 486 SX/DX/DX2, 487SX, and Intel 386DX/Cyrix® 486DLC/IBM 486DLC microprocessors
- Single-chip PC/AT® solution: one 208-pin Plastic Flat Package (PFP)
- 1X and 2X clock source, supporting systems running from 16MHz to 50MHz
- Write-back direct mapped, bank interleave cache with size selections: 64KB, 128KB, 256KB, and 512KB
- Supports 2-1-1-1, 3-1-1-1, 2-2-2-2, and 3-2-2-2 cache burst cycles
- Support for two programmable non-cacheable regions
- Built-in tag auto-invalidation circuitry
- Option for write-protected, cacheable video and system BIOS
- Programmable cache and DRAM read/write cycles
- Supports four banks of 256KB, 1MB, and 4MB DRAMs for configurations up to 64MB
- Shadow RAM option
- Flash ROM support
- Hidden refresh and slow refresh supported using the CAS-before-RAS refresh method
- Comprehensive VESA VL and OPTi high-performance local bus support
- Turbo/slow speed selection
- Synchronous AT bus clock with programmable clock division options:
- CLKI(/6, /5 /4, /3), or CLK2I(/6, /5, /4, /3)
- Zero or one wait state options for 16-bit AT bus cycles
- Transparent 8042 emulation for fast CPU reset and GATEA20 generation
- Supports the 80387 numeric coprocessor
- Low-power, high-speed 0.8-micron CMOS technology
- Integrated peripherals controller

Figure 1-1 Address and Data Path Clock Diagram



2.0 Overview

The OPTi 82C499 provides a highly integrated solution for fully compatible, high-performance PC/AT platforms. This chip will support the Intel 486SX/DX/DX2/487SX, Intel 386DX and IBM/Cyrix 486DLC microprocessors in the most cost effective and power efficient designs available today. Since the device is so critical to the performance and cost structure of a PC, this highly integrated approach provides the foundation for a very cost effective platform without compromising performance. For power users, this chip offers optimum performance for systems running up to 50MHz. The OPTi DXSC chip provides a solution positioned to deliver value, without neglecting quality, compatibility, or reliability.

The 82C499 integrates a write-back cache controller, a local DRAM controller, an integrated peripherals controller (82C206), the CPU state machine, the AT bus state machine, and data buffers all in a single 208-pin PFP. New on-chip hardware provides the hooks for OPTi and VESA local bus device support.

3.0 Signal Definitions

Figure 3-1 Pin Diagram

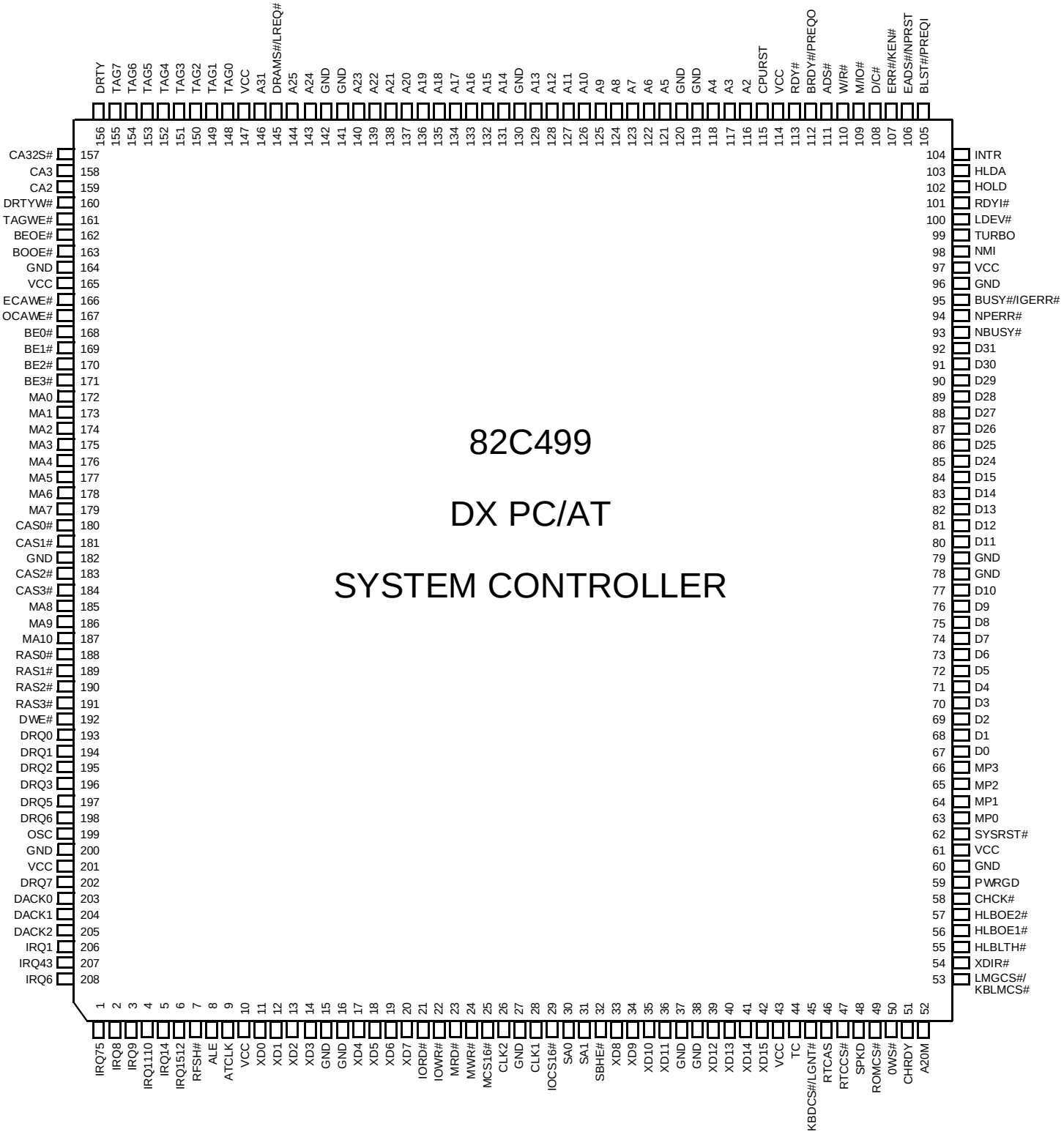


Table 3-1 Numerical Pin Cross-Reference List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	IRQ75	53	LMGCS#/KBLMCS#	105	BLST#/PREQI	157	CA32S#
2	IRQ8	54	XDIR#	106	EADS#/NPRST	158	CA3
3	IRQ9	55	HLBLTH#	107	ERR#/KEN#	159	CA2
4	IRQ1110	56	HLBOE1#	108	D/C#	160	DRTYW#
5	IRQ14	57	HLBOE2#	109	M/IO#	161	TAGWE#
6	IRQ1512	58	CHCK#	110	W/R#	162	BEOE#
7	RFSH#	59	PWRGD	111	ADS#	163	BOOE#
8	ALE	60	GND	112	BRDY#/PREQO	164	GND
9	ATCLK	61	VCC	113	RDY#	165	VCC
10	VCC	62	SYSRST#	114	VCC	166	ECAWE#
11	XD0	63	MP0	115	CPURST	167	OCAWE#
12	XD1	64	MP1	116	A2	168	BE0#
13	XD2	65	MP2	117	A3	169	BE1#
14	XD3	66	MP3	118	A4	170	BE2#
15	GND	67	D0	119	GND	171	BE3#
16	GND	68	D1	120	GND	172	MA0
17	XD4	69	D2	121	A5	173	MA1
18	XD5	70	D3	122	A6	174	MA2
19	XD6	71	D4	123	A7	175	MA3
20	XD7	72	D5	124	A8	176	MA4
21	IORD#	73	D6	125	A9	177	MA5
22	IOWR#	74	D7	126	A10	178	MA6
23	MRD#	75	D8	127	A11	179	MA7
24	MWR#	76	D9	128	A12	180	CAS0#
25	MCS16#	77	D10	129	A13	181	CAS1#
26	CLK2	78	GND	130	GND	182	GND
27	GND	79	GND	131	A14	183	CAS2#
28	CLK1	80	D11	132	A15	184	CAS3#
29	IOCS16#	81	D12	133	A16	185	MA8
30	SA0	82	D13	134	A17	186	MA9
31	SA1	83	D14	135	A18	187	MA10
32	SBHE#	84	D15	136	A19	188	RAS0#
33	XD8	85	D24	137	A20	189	RAS1#
34	XD9	86	D25	138	A21	190	RAS2#
35	XD10	87	D26	139	A22	191	RAS3#
36	XD11	88	D27	140	A23	192	DWE#
37	GND	89	D28	141	GND	193	DRQ0
38	GND	90	D29	142	GND	194	DRQ1
39	XD12	91	D30	143	A24	195	DRQ2
40	XD13	92	D31	144	A25	196	DRQ3
41	XD14	93	NBUSY#	145	DRAMS#/LREQ#	197	DRQ5
42	XD15	94	NPERR#	146	A31	198	DRQ6
43	VCC	95	BUSY#/IGERR#	147	VCC	199	OSC
44	TC	96	GND	148	TAG0	200	GND
45	KBDCS#/LGNT#	97	VCC	149	TAG1	201	VCC
46	RTCAS	98	NMI	150	TAG2	202	DRQ7
47	RTCCS#	99	TURBO	151	TAG3	203	DACK0
48	SPKD	100	LDEV#	152	TAG4	204	DACK1
49	ROMCS#	101	RDYI#	153	TAG5	205	DACK2
50	0WS#	102	HOLD	154	TAG6	206	IRQ1
51	CHRDY	103	HLDA	155	TAG7	207	IRQ43
52	A20M	104	INTR	156	DRTY	208	IRQ6

Table 3-2 Alphabetical Pin Cross-Reference List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
116	A2	69	D2	141	GND	189	RAS1#
117	A3	70	D3	142	GND	190	RAS2#
118	A4	71	D4	164	GND	191	RAS3#
121	A5	72	D5	182	GND	113	RDY#
122	A6	73	D6	200	GND	101	RDYI#
123	A7	74	D7	55	HLBLTH#	7	RFSH#
124	A8	75	D8	56	HLBOE1#	49	ROMCS#
125	A9	76	D9	57	HLBOE2#	46	RTCAS
126	A10	77	D10	103	HLDA	47	RTCCS#
127	A11	80	D11	102	HOLD	30	SA0
128	A12	81	D12	104	INTR	31	SA1
129	A13	82	D13	206	IRQ1	32	SBHE#
131	A14	83	D14	2	IRQ8	48	SPKD
132	A15	84	D15	3	IRQ9	62	SYSRST#
133	A16	85	D24	208	IRQ6	44	TC
134	A17	86	D25	5	IRQ14	99	TURBO
135	A18	87	D26	207	IRQ43	148	TAG0
136	A19	88	D27	1	IRQ75	149	TAG1
137	A20	89	D28	4	IRQ1110	150	TAG2
52	A20M	90	D29	6	IRQ1512	151	TAG3
138	A21	91	D30	29	IOCS16#	152	TAG4
139	A22	92	D31	21	IORD#	153	TAG5
140	A23	108	D/C#	22	IOWR#	154	TAG6
143	A24	203	DACK0	45	KBDCS#/LGNT#	155	TAG7
144	A25	204	DACK1	100	LDEV#	161	TAGWE#
146	A31	205	DACK2	53	LMGCS#/KBLMCS#	10	VCC
111	ADS#	145	DRAMS#/LREQ#	109	M/IO#	43	VCC
8	ALE	193	DRQ0	172	MA0	61	VCC
9	ATCLK	194	DRQ1	173	MA1	97	VCC
168	BE0#	195	DRQ2	174	MA2	114	VCC
169	BE1#	196	DRQ3	175	MA3	147	VCC
170	BE2#	197	DRQ5	176	MA4	165	VCC
171	BE3#	198	DRQ6	177	MA5	201	VCC
162	BEOE#	202	DRQ7	178	MA6	110	W/R#
105	BLST#/PREQI	156	DRTY	179	MA7	11	XD0
163	BOOE#	160	DRTYW#	185	MA8	12	XD1
112	BRDY#/PREQO	192	DWE#	186	MA9	13	XD2
95	BUSY#/IGERR#	106	EADS#/NPRST	187	MA10	14	XD3
159	CA2	166	ECAWE#	25	MCS16#	17	XD4
158	CA3	107	ERR#/KEN#	63	MP0	18	XD5
157	CA32S#	15	GND	64	MP1	19	XD6
180	CAS0#	16	GND	65	MP2	20	XD7
181	CAS1#	27	GND	66	MP3	33	XD8
183	CAS2#	37	GND	23	MRD#	34	XD9
184	CAS3#	38	GND	24	MWR#	35	XD10
58	CHCK#	60	GND	93	NBUSY#	36	XD11
51	CHRDY	78	GND	98	NMI	39	XD12
28	CLK1	79	GND	94	NPERR#	40	XD13
26	CLK2	96	GND	167	OCAWE#	41	XD14
115	CPURST	119	GND	199	OSC	42	XD15
67	D0	120	GND	59	PWRGD	54	XDIR#
68	D1	130	GND	188	RAS0#	50	0WS#

3.1 Signal Descriptions

3.1.1 CPU Interface Signals

Name	Pin	Type	I_{OL}	Description
BLST#/PREQI	105	I		***486 Burst Last Cycle Indication:*** The 82C499 terminates the burst cycle as long as BLST# sampled low at the end of each T2 when BRDY# is active. During Intel 386DX and IBM/Cyrix 486DLC Mode, this is the PREQI signal from the 387.
BRDY#/ PREQO	112	O	8mA	***Burst Ready:*** An output for the CPU to sample the read data during burst cycles. This pin becomes PREQO for the Intel 386DX and IBM/ Cyrix 486DLC Mode of operation.
BE[3:0]#	171:168	I/O	4mA	***Byte Enables 3 through 0:*** These signals are inputs during CPU cycles and are outputs during non-CPU cycles.
A31, A[25:24]	156, 144:143	I		***CPU Address Lines 31, 25, and 24.***
A[23:17]	140-134	I/O	4mA	***CPU Address Lines 23 through 17:*** These signals are inputs during CPU, refresh and Master cycles. They become outputs during DMA cycles.
A[16:8]	133:131, 129:124	I/O	4mA	***CPU Address Lines 16 through 8:***These signals are inputs during non-DMA cycles. A[16:9] become outputs which convey DMA address lines A[16:9] by latching XD[7:0] during 16-bit DMA cycles. A[15:8] convey DMA address lines A[15:8] by latching XD[7:0] during 8-bit DMA cycles.
A[7:2]	123:121, 118:116	I/O	4mA	***CPU Address Lines 7 through 2:*** These signals become outputs during DMA cycles.
D[31:24], D[15:0]	80:92, 67:77	I/O	4mA	***CPU Data Bus bits 31 through 24 and 15 through 0.***
D/C#	108	I		***CPU Data or Code Cycle Status:*** When high, this signal indicates data transfer operations. When low, it indicates control operations (code fetch, halt, etc.).
M/IO#	109	I/O	8mA	***CPU Memory or I/O Cycle Status:*** When high, this signal indicates a memory cycl. When low, it indicates an I/O cycle. M/IO# becomes an output during DMA/master cycles for local device accesses and IBM 486DLC snooping cycles.
W/R#	110	I/O	8mA	***CPU Write or Read Cycle Status:*** This signal indicates a write cycle if high and read cycle if low. It becomes an output during DMA/master cycles for local device accesses and IBM 486DLC snooping cycles.
A20M#	52	O	4mA	***Emulation of GateA20*** OR'ed with internal fast GATEA20 output to Intel 486, IBM/Cyrix 486DLC CPU. This signal must remain high during the power-up CPU reset period. In Intel 386DX Mode, this is the GA20 signal indirectly buffered to the AT bus line LA20.
LDEV#	100	I		***Local Bus Device Cycle Indication:*** This signal is sampled at the end of the first T2, or at the end of the second T2 at 50MHz.
DRAMS#/ LREQ#	145	I		A[30:25] are low decode, connected to A26 normally, except during local bus master support, when MP1 is sampled low by RST4's rising edge, this signal becomes LREQ# (Local Bus Master Request).

3.1.1 CPU Interface Signals (cont.)

Name	Pin	Type	I_{OL}	Description
RDYI#	101	I		***Local Device Ready Input:*** This signal is synchronized by the 82C499 before sending it to CPU.
RDY#	113	I/O	8mA	***Ready Output*** for the CPU to terminate the current cycle. This pin becomes an input during local device cycles if a tristated local bus device's ready was connected.
ADS#	111	I/O	8mA	***Address Strobe:*** A status input from CPU. This active low signal indicates the CPU is starting a new cycle. It becomes an output pin during DMA/master cycles for local device accesses and IBM 486DLC snooping cycles.
TURBO	99	I		***Turbo Mode Selection:*** If the TURBO pin is tied low, the CPU will be forced idle for 2/3 period.

3.1.2 AT Bus Interface

Name	Pin	Type	I_{OL}	Description
MCS16#	25	I/O	18mA	***16-bit AT Memory Slave Cycle Status:*** This pin is a Schmitt-trigger input pin normally and is driven low during master cycle.
IOCS16#	29	I		***16-bit I/O Slave Cycle Status:*** This is a Schmitt trigger input pin.
ALE	8	O	18mA	***AT Bus Address Latch Enable:*** Represents that an AT cycle has started.
SBHE#	32	I/O	18mA	***AT Bus High Byte Enable:*** This signal is an input pin during master cycles.
XD[15:0]	42:39, 36:33, 20:17, 14:11	I/O	18mA	***AT Data Bus lines.***
IORD#	21	I/O	24mA	***AT I/O Read Command:*** This pin is an input during master cycles and an output for CPU and DMA cycles.
IOWR#	22	I/O	24mA	***AT I/O Write Command:*** This pin is an input during master cycles and an output for CPU and DMA cycles.
MRD#	23	I/O	18mA	***AT Memory Read Command:*** This pin is an input during master cycles and an output for CPU and DMA cycles.
MWR#	24	I/O	18mA	***AT Memory Write Command:*** This pin is an input during master cycles and an output for CPU and DMA cycles.
ROMCS#	49	O	4mA	***BIOS ROM Output Enable:*** System BIOS ROM accesses could be either 8- or 16-bit. This signal will be asserted from the end of the first T2 to the end of the last T2.
CHRDY	51	I/O	18mA	***Channel Ready:*** This pin is a Schmitt-trigger input from the AT bus.
LMGCS#/ KBLMCS#	53	O	4mA	***Lower Memory Space (below one megabyte) Indicator:*** This signal is active during refresh cycles. When MP1 is sampled low, this pin becomes KBLMCS# only during I/O cycles. This pin must be qualified with M/IO# before it goes to the 8042 chip select.

3.1.2 AT Bus Interface (cont.)

Name	Pin	Type	I_{OL}	Description
SA0	30	I/O	24mA	***System Address Line 0:*** This pin is an input during master cycles; an output during CPU, DMA, or refresh cycles.
SA1	31	I/O	24mA	***System Address Line 1:*** This pin is an input during master cycles and output during CPU, DMA, or refresh cycles.
0WS#	50	I		***Zero Wait State:*** This pin is a Schmitt-trigger input pin from the AT bus. Note that the system BIOS ROM is accessed as a one wait state AT cycle.

3.1.3 Bus Arbitration Interface Signals

Name	Pin	Type	I_{OL}	Description
RFSH#	7	I/O	18mA	***AT Refresh Cycle Indication:*** This signal is an input pin master or DMA cycles. Note that the 82C499 will not HOLD the CPU during AT refresh cycles. The 82C499 puts the CPU on "waiting" if an AT refresh cycle is underway.
HLDA	103	I		***Hold Acknowledge*** from CPU.
HOLD	102	O	4mA	***HOLD Request*** to CPU: Hidden refresh will not hold the CPU.

3.1.4 Numeric Processor Interface Signals

Name	Pin	Type	I_{OL}	Description
NPBUSY#	93	I		***Numeric Processor Busy:*** also used to determine Intel 386, IBM/ Cyrix 486DLC, or Intel 486 Mode. A high indicates an Intel 386 or IBM/Cyrix 486 DLC. A low indicates an Intel 486.
EADS#/ NPRST	106	O	4mA	***486 Address Snooping Strobe:*** This signal is asserted for two T-states during DMA or master cycles. In the Intel 386DX or IBM/Cyrix 486DLC Mode, a reset of the numeric coprocessor can be generated by an I/O write to Port F1h, which will trigger NPRST.
NPERR#	94	I		***Numeric Processor Error Indication:*** Used to generate IGERR# for the Intel 486 CPU. Also, it generates NPINT for AT/PC-compatability and will generate BUSY# for the Intel 386 or IBM/Cyrix 486DLC.
BUSY#/ IGERR#	95	O	4mA	***Busy or Ignore Error:*** This is a normally high signal and will become low as soon as the NPERR# is asserted. An I/O write to Port F0h, or a CPU reset will force this signal back to high. During the Intel 386DX or IBM/Cyrix486DLC Mode, this signal is the BUSY# signal to the CPU.

3.1.5 Cache Interface Signals

Name	Pin	Type	I_{OL}	Description
ERR#/KEN#	107	O	4mA	***Error/Cache Enable:*** Cacheable or non-cacheable status for the internal cache of Intel 486 and IBM/Cyrix 486DLC. This signal is low normally and is brought high at the end of T1. The 82C499 asserts KEN# again if it is a cacheable cycle. During the Intel 386 Mode, this pin is ERR# to the CPU. ERR# for the IBM/Cyrix 486DLC needs to be generated externally.

3.1.5 Cache Interface Signals (cont.)

Name	Pin	Type	I_{OL}	Description
CA[3:2]	158:159	O	8mA	***CPU Address Lines 3 and 2.***
DRTY	156	I/O	4mA	***Dirty bit*** of tag RAM to indicate its line has been written into.
CA32S#	157	O	4mA	***External Cache Address line 3 and line 2 Select.***
BEOE#	162	O	8mA	***External Cache Output Enable.***
BOOE#	163	O	8mA	***External Cache Output Enable.***
ECAWE#	166	O	8mA	***External Cache Write Enable*** for the even Cache bank.
OCAWE#	167	O	8mA	***External Cache Write Enable*** for the odd Cache bank.
TAG[7:0]	155:148	I/O	4mA	***Tag RAM Output*** lines 7 through 0.
TAGWE#	161	O	4mA	***Tag RAM Write Enable:*** Used to update the tag RAM.
DRTYW#	160	O	8mA	***Write Strobe to Dirty bit*** of tag RAM.

3.1.6 DRAM Interface Signals

Name	Pin	Type	I_{OL}	Description
CAS[3:0]#	184, 183, 181, 180	O	8mA	***DRAM Column Address Strobe*** bits 3 through 0.
MP[3:0]	66-63	I/O	4mA	***DRAM Parity bits*** 3 through 0: In addition, MP1 is used to enable the internal VESA bus arbitration circuitry. This pin must be pulled down with a 1K resistor if the internal VESA bus arbitration is to be used. MP2 is used to determine the Intel 386 or IBM/Cyrix 486DLC. This pin must be pulled down with a 1K resistor if the IBM/Cyrix 486DLC is used. MP1 and MP2 are sampled on the rising edge of RST4.
RAS[3:0]#	188:191	O	8mA	***DRAM Row Address Strobe*** bits 3 through 0.
MA[10:0]	187:185, 179:172	O	8mA	***DRAM Row/Column Address*** lines 10 through 0.
DWE#	192	O	8mA	***DRAM Write Enable signal.***

3.1.7 82C206 Signal

Name	Pin	Type	I_{OL}	Description
DRQ[7:0]	202, 198:193	I		***DMA request lines***
DACK[2:0]	205:203	O	5mA	***Encoded DMA Acknowledgement*** lines 2 through 0.
INTR	104	O	4mA	***Interrupt Request***
IRQ1	206	I		***Interrupt Request*** line 1: Schmitt-trigger input.
IRQ43	207	I		***Interrupt*** Request lines 4 and 3: Schmitt-trigger input.
IRQ6	208	I		***Interrupt Request*** line 6: Schmitt-trigger input.
IRQ75	1	I		***Interrupt Request*** lines 7 and 5: Schmitt-trigger input.

3.1.7 82C206 Signal (cont.)

Name	Pin	Type	I_{OL}	Description
IRQ8	2	I		***Interrupt Request*** line 8: Schmitt-trigger input.
IRQ9	3	I		***Interrupt Request*** line 9: Schmitt-trigger input.
IRQ1110	4	I		***Interrupt Request*** lines 11 and 10: Schmitt-trigger input.
IRQ14	5	I		***Interrupt Request*** line 14: Schmitt-trigger input.
IRQ1512	6	I		***Interrupt Request*** lines 15 and 12: Schmitt-trigger input.
TC	44	O	12mA	***Terminate Count.***

3.1.8 Buffer Control Signals

Name	Pin	Type	I_{OL}	Description
HLBOE1#	56	O	4mA	***Byte 2 Data Buffer Output Enable:*** This signal becomes active when: CPU DRAM cycles for parity checking and generation, CPU AT byte 2 write cycle at 486 Mode, DMA or master byte 2 read DRAM or, Local device cycle.
HLBLTH#	55	O	4mA	***Byte 2 Data Latch Enable:*** This signal becomes high when: CPU AT byte 2 read cycle, DMA or master cycle.
HLBOE2#	57	O	4mA	***Byte 2 Data Latch Output Enable:*** This signal becomes active when: CPU AT byte 2 read cycle DMA or master byte 2 write to local DRAM or local device.
XDIR#	54	O	4mA	***SD[7:0] to XD[7:0] Direction Control:*** This signal is normally high and is driven low when the devices located on XD[7:0] are read.

3.1.9 Reset Signals

Name	Pin	Type	I_{OL}	Description
CPURST	115	O	8mA	***CPU Reset*** for the microprocessor.
SYSRST#	62	O	8mA	Debounced PWRGD# output.
PWRGD	59	I		***Power good*** status or reset switch on indication.

3.1.10 Clock Signals

Name	Pin	Type	I_{OL}	Description
OSC	199	I		***14.3MHz Oscillator*** input.

3.1.10 Clock Signals (cont.)

Name	Pin	Type	I_{OL}	Description
ATCLK	9	O	18mA	***ATCLK to AT bus.*** This is a free running clock output. It could be CLKI/3, CLKI/4, CLKI/5 or CLKI/6 (indicates that 82C499 is running at 50MHz and LDEV# will be sampled at the end of second T2 clock cycle).
CLK2	26	I		***Clock Input*** which has a frequency equal to twice the rated CPU clock if the 2X-clock scheme is chosen. This signal is used for secondary cache early write option only. If the 1X clock scheme is used, this pin is connected to the same clock source as CLKI.
CLK1	28	I		***Single phase clock input*** for the 82C499 internal state machine.

3.1.11 Miscellaneous Interface Signals

Name	Pin	Type	I_{OL}	Description
CHCK#	58	O		***Channel Check:*** An input from the AT bus to indicate that a parity error was generated by the AT memory card. (NMI interrupt request.)
KBDCS#/ LGNT#	45	O	4mA	***Keyboard Controller Chip Select or Local Grant:*** When I/O to Port 60h or 64h is detected, this signal is decoded for the keyboard A[9:0]. When MP1 is pulled low, this signal becomes the VESA bus local grant signal.
NMI	98	O	4mA	***Non-Maskable Interrupt:*** Sent to the CPU and caused by system parity error or AT bus channel check.
RTCAS	46	O	4mA	***Real-time Clock Address Strobe.***
RTCCS#	47	O	4mA	***Real-time Clock Chip Select.***
SPKD	48	O	4mA	***Speaker Data Output:*** Generated by OUT2 and Port 61h, bit 1.

3.1.12 Power and Ground Pins

Name	Pin	Type	I_{OL}	Description
VCC	10, 43, 61, 97, 114, 147, 165, 201	PWR		***Power Connection:*** +5V
GND	15, 16, 27, 37, 38, 60, 78, 79, 96, 119, 120, 130, 141, 142, 164, 182, 200	GND		***Ground Connection***

4.0 Functional Description

4.1 Reset Logic

The RST1# input to the 82C499 is used to generate the CPU reset (CPURST), the numeric coprocessor reset (NPRST), and the system reset (SYSRST#) signals. RST1# is a “cold reset” which is generated when either PWRGD goes low (from the power supply, indicating a low power condition) or when the system reset button is activated. This reset signal is used to force the system to begin execution at a known state. When RST1# is sensed active, the 82C499 will assert CPURST, NPRST, and SYSRST#. CPURST is also generated when a shutdown condition is decoded from the CPU bus definition signals. CPURST, NPRST, and SYSRST# are asserted for (128) CLK2 cycles.

The 82C499 emulates the keyboard reset function. The keyboard reset is intercepted by monitoring the I/O write cycle “FE” command to Port 64h. This fast CPU reset from the chipset will be generated directly after the I/O write is decoded unless bit 1 of Index Register 20h is disabled, in which case the reset will not start until a “halt” instruction is executed.

When configured to interface with a math coprocessor, the 82C499 will generate the NPRST signal when CPURST is activated or if an I/O write to Port F1h is issued.

4.2 System Clock Generation

The 82C499 has two high frequency clock inputs, CLK and CLK2. This clocking scheme provides both single and double frequency operation to support all 486 platforms at system speeds up to 50MHz.

The 486 is driven by a 1X clock as opposed to the 2X clock required by the 486DLC and 386 microprocessor. Single frequency clocking is only necessary during 486 40MHz and 50MHz operation. In this mode, CLK and CLK2 are generated by the same source so that the 82C499 will receive only a single 1X clock source (this avoids the necessity of a 100MHz oscillator for 486 50MHz operation). Double frequency operation requires that the CLK2 input be fed directly by the crystal oscillator, while the CLK input is derived from the oscillator output divided by two externally. In this mode, the 82C499 will receive both a 1X and 2X clock source. Typically for Intel 486 CPUs, a double frequency clock is recommended for 20, 25, and 33MHz operation, while 40 or 50MHz operation requires a single frequency clocking scheme.

CLK is a master single-phase clock which is used to drive all host CPU synchronous signals and the 82C499's internal state machines. CLK2 is used by the cache/DRAM controller logic and to maintain the clock phase between the CPU and the 82C499 by controlling the CPU reset timing.

The 82C499 generates the AT bus clock (ATCLK) from an internal division of CLK or CLK2. The ATCLK frequency is programmable and can be set to any of four clock division options by programming Index Register 25h[1:0]. This allows the system designer to tailor the AT bus clock frequency to support a wide range of system designs and performance platforms.

A 2X clock is necessary for running the system with zero-wait-state-cache-write enabled and to conform to the timing requirements specified by t100a and t100b.

At 40MHz, Intel 386 or IBM 486DLC applications CLKI, CLK2I, and CPUCLK must be within 1ns clock skew of each other. This is required for the proper setup of hold time to be met for the CPU and proper synchronization of CLKI to the system.

4.3 CPU Burst Mode Control

The DXSC chipset fully supports 486 burst cycles. The 82C499 cache and DRAM controllers insure that data is burst into the CPU whenever the 486 requests a burst linefill. The secondary cache provides data on read-hits and the DRAM supplies the data during cache read-misses.

For the cache read-hit cycle, BRDY# is asserted at the middle of the first T2 state when a 2-1-1-1 (zero wait state) cache burst cycle is chosen, otherwise it is asserted at the middle of the second T2 state when one wait state is required. If a read-miss occurs, the DRAM data is first written into cache memory, then it is burst from the cache to the 486 CPU. BRDY# is asserted after cache memory is updated for cache read-misses. Once asserted, BRDY# stays active until BLST# is detected during a zero wait state burst cycle. BRDY# is never active during DMA or master cycles.

The 82C499 contains separate burst counters to support DRAM and external cache burst cycles. The DRAM burst counter performs the cache read-miss linefill (DRAM to external cache) and the cache burst counter supports the 486 burst linefill (external cache to the 486 CPU). The burst order of the cache burst counter exactly matches the double-word address sequencing expected by the 486 CPU. The DRAM burst counter is used for cache read-miss cycles and dirty linefill write operations.

4.4 Cache Subsystem

The integrated cache controller, which uses a direct-mapped, bank-interleaved scheme dramatically boosts the overall performance of the local memory subsystem by caching writes as well as reads (write-back mode). Cache memory can be configured as one or two banks, and sizes of 64, 128, 256, and 512KB are supported. Provisions for two programmable non-cacheable regions are provided. The cache controller operates in non-pipeline mode, with a fixed 16-byte line size (optimized to match a 486 burst linefill) in order to simplify the motherboard design without increasing cost or degrading system performance. For 486 systems, the secondary cache operates independently and in addition to the CPU's internal cache.

The cache controller works as the front-end for both the DRAM and AT bus controllers. ADS# from the CPU must pass through the cache logic first. When the cache is disabled, ADS# just falls through the cache controller and delivers an internal MADS# to the DRAM and AT bus controllers. When the cache is enabled, ADS# is blocked when a cache cycle is detected. If this cycle is determined to be a NCA (non-cacheable address) or a cache miss cycle, ADS# is delayed one CLK before outputting an internal MADS# due to the time needed for NCA and cache hit/miss detections.

4.4.1 Cache Bank Interleave

In order to support cache burst cycles at elevated frequencies and still utilize conventional speed SRAMs, a bank interleave cache access method is employed. The addresses are applied to the cache memory one cycle earlier, while cache output enable signals control even/odd bank selection and enable cache RAM data to the CPU data bus. Since the output enable time is about one-half of the address access time, the 82C499 can achieve a high performance cache burst mode without using the more expensive high speed SRAMs.

The 82C499 supports one or two cache banks. Two cache banks are required to interleave and realize the performance advantages of this cache scheme. Cache sizes of 128KB and 512KB are single-bank caches, while 64KB and 256KB cache sizes are double-bank. When using a double-bank configuration, the even and odd banks receive the same address lines. Signals A2/A3, ECAWE#/OCAWE#, and BEOE#/BOOE# are used to dictate the even or odd bank access.

4.4.2 Write-Back Cache

The write-back cache scheme derives its superior performance by optimizing write cycles. There is no performance penalty in the cache write cycle, since the cache controller does not need to wait for the much slower DRAM controller to finish its cycle before proceeding to the next cycle.

4.4.3 Tag RAM

A built-in tag comparator improves system performance while reducing component count on the system board. The comparator internally detects the cache hit/miss status by comparing the high-order address bits (for the memory cycle in progress) with the stored tag bits from previous cache entries (see Table 4-1). When a match is detected, and the location is cacheable, a cache hit cycle takes place. If the comparator does not match, or a non-cacheable location is accessed (based on the internal non-cacheable region registers), the current cycle is a cache miss. The tag is invalidated automatically during memory reads when the cache is disabled; each memory read will write into the corresponding tag location a non-cacheable address (such as A0000 or B0000 of the video memory area). To invalidate the cache, simply disable the cache in Configuration Register 21h, bit 4, and read a block of memory equal to the size of the cache. The advantage of this invalidation scheme is that no valid bit is necessary and expensive SRAM can be conserved. To flush the cache, simply read a block twice the size of the cache. This will guarantee that every dirty cache location is flushed to DRAM.

The following table details which CPU address bits are stored as tags for the various cache sizes supported in the 82C499 and how the tag RAM bits are addressed for different cache sizes.

Table 4-1 Address to Tag Bit Mapping

Tag Bit	64KB	128KB	256KB	512KB
7	A22	A22	A22	A22
6	A21	A21	A21	A21
5	A20	A20	A20	A20
4	A19	A19	A19	A19
3	A18	A18	A18	X
2	A17	A17	A25	A25
1	A16	A24	A24	A24
0	A23	A23	A23	A23

4.4.4 Dirty Bit Mechanism

The “dirty bit” is a mechanism for monitoring coherency between the cache system and DRAM. Each tag entry has a corresponding dirty bit to indicate whether the data in the represented cache line has been modified

since it was loaded from system memory. This allows the 82C499 to determine whether the data in memory is “stale” and needs to be updated before a new memory location is allowed to overwrite the currently indexed cache entry. The write-back cycle causes an entire cache line (16 bytes) to be written back to memory, followed by a line burst from the new memory location into the cache, and then the final line burst from the cache to the CPU. Normally, the performance advantage of completing fast writes to the cache outweigh the “write-back” read-miss penalties which are incurred while operating the write-back scheme.

Cache Read-Hit
The secondary cache provides data to the CPU. For 486 systems, the 82C499 follows the CPU's burst protocol to fill the processor's internal cache line.

Cache Read-Miss (DIRTY bit negated)
The cache controller does not need to update the system memory with the cache's current data because that data has not been modified (evidenced by the dirty bit negation). The cache controller asserts TAGWE# causing the tag RAMs to update with the new address, and asserts ECAWE#/OCAWE# causing the cache memory to update with data from DRAM. This data is then presented to the CPU (following burst protocol for 486 systems).

Cache Read-Miss (DIRTY Bit Asserted)
The cache controller must update the system memory with data from the cache location that is going to be overwritten. The controller writes the 16-byte line from cache memory into DRAM, then reads the new line from DRAM into the cache memory and deasserts the DIRTY bit. The cache controller asserts TAGWE#, ECAWE#/OCAWE#, and DRTYW# during this linefill. This new data is presented to the CPU (following burst protocol for 486 systems).

Cache Write-Hit
Because this is a write-back cache, the cache controller does not need to update the much slower DRAM memory. Instead, the controller updates the cache memory and sets the DIRTY bit. DIRTY may already be set, but that does not affect this cycle. The contents of the tag RAM remains unmodified.

Cache Write-Miss
The cache controller bypasses the cache entirely and writes the data directly into DRAM. DIRTY is unchanged.

Table 4-2 shows the cache sizes supported by the 82C499, with the corresponding tag RAM address bits, tag RAM size, cache RAM address bits, cache RAM size, and cacheable main memory size.

Table 4-2 Cache SRAM Requirements

Cache Size	TAG Field Address / TAG RAM Size	Dirty SRAMs Size	Cache SRAM Address Qty / Cache RAM Size	Cacheable Main Memory
64KB	A[23:16] / 8Kx8	16Kx1	A[15:2] / 8ea, 8Kx8	16MB
128KB	A[24:17] / 8Kx8	16Kx1	A[16:2] / 4ea, 32Kx8	32MB
256KB	A[25:18] / 32Kx8	16Kx1	A[17:2] / 8ea, 32Kx8	64MB
512KB	A[25:19] / 32Kx8	64Kx1	A[18:2] / 4ea, 128Kx8	64MB

Table 4-3 shows what speed SRAM and TAG SRAM to use for a particular CPU clock rate.

Table 4-3 SRAM Speed Requirements

Speed	OSC	Cache SRAM	Tag SRAM	DRAM speed	Note*
16MHz	32MHz	25ns	25ns	80ns	Cache Write 0ws, Cache read burst 2-1-1-1
20MHz	40MHz	25ns	25ns	80ns	Cache Write 0ws, Cache read burst 2-1-1-1
25MHz	50MHz	25ns	25ns	80ns	Cache Write 0ws, Cache read burst 2-1-1-1
33MHz	66/33MHz	20ns	15ns	80ns	Cache Write 0ws, Cache read burst 2-2-2-2 1 bank of cache
33MHz	66/33MHz	20ns	15ns	80ns	Cache Write 0ws, Cache read burst 2-1-1-1 2 banks of cache
40MHz	80MHz	20ns	15ns	80ns	Cache Write 1ws, Cache read burst 3-2-2-2
50MHz	50MHz	20ns	15ns	80ns	Cache Write 1ws, Cache read burst 3-2-2-2

*. For the Intel 386 or IBM/Cyrix 486DLC, only the lead-off cycles of the above corresponding cache read burst cycles will be used (i.e., 33MHz and below: 2).

Note DRAM and cache cycles are at their minimum wait states.

4.5 Local DRAM Control Subsystem

The 82C499 supports up to four banks of page-mode local DRAM memory for configurations of up to 64MB. 256KB, 1MB, or 4MB page-mode DRAM devices may be used. The DRAM configuration is programmable through Configuration Register 24h. DRAM performance features are programmable through Configuration Register 25h. Table 4-4 illustrates the DRAM configurations supported.

Table 4-5 describes how the DRAM address lines are multiplexed when different memory device types are used.

Table 4-4 DRAM Configurations

Bank0	Bank1	Bank2	Bank3	Total	Register Bits [7:4] - [2:0]
256KB	x	x	x	1MB	0 0 0 0 - 1 1 1
256KB	256KB	x	x	2MB	0 0 0 1 - 1 1 1
1MB	x	x	x	4MB	1 0 0 0 - 1 1 1
256KB	1MB	x	x	5MB	0 0 1 0 - 1 1 1
1MB	1MB	x	x	8MB	1 0 0 1 - 1 1 1
1MB	1MB	1MB	x	12MB	1 0 0 1 - 0 0 0
256KB	1MB	1MB	1MB	13MB	0 0 1 0 - 0 0 1
1MB	1MB	1MB	1MB	16MB	1 0 0 1 - 0 0 1
4MB	x	x	x	16MB	1 1 0 0 - 1 1 1
256KB	256KB	4MB	x	18MB	0 0 0 1 - 1 0 0
1MB	4MB	x	x	20MB	1 0 1 0 - 1 1 1
4MB	1MB	x	x	20MB	1 0 1 1 - 1 1 1
1MB	1MB	4MB	1MB	28MB	1 0 0 1 - 0 1 1
1MB	4MB	1MB	1MB	28MB	1 0 1 0 - 0 0 1
4MB	1MB	1MB	1MB	28MB	1 0 1 1 - 0 0 1
4MB	4MB	x	x	32MB	1 1 0 1 - 1 1 1
1MB	1MB	4MB	4MB	40MB	1 0 0 1 - 1 0 1
1MB	4MB	4MB	1MB	40MB	1 0 1 0 - 0 1 1
4MB	1MB	4MB	1MB	40MB	1 0 1 1 - 0 1 1
4MB	4MB	1MB	1MB	40MB	1 1 0 1 - 0 0 1
4MB	4MB	4MB	x	48MB	1 1 0 1 - 1 0 0
1MB	4MB	4MB	4MB	52MB	1 0 1 0 - 1 0 1
4MB	1MB	4MB	4MB	52MB	1 0 1 1 - 1 0 1
4MB	4MB	4MB	1MB	52MB	1 1 0 1 - 0 1 1
4MB	4MB	4MB	4MB	64MB	1 1 0 1 - 1 0 1

Table 4-5 CPU Address to MA Bus Mapping

Memory Address	256KB		1MB		4MB	
	Column	Row	Column	Row	Column	Row
MA0	A2	A11	A2	A21	A2	A21
MA1	A3	A12	A3	A12	A3	A23
MA2	A4	A13	A4	A13	A4	A13
MA3	A5	A14	A5	A14	A5	A14
MA4	A6	A15	A6	A15	A6	A15
MA5	A7	A16	A7	A16	A7	A16
MA6	A8	A17	A8	A17	A8	A17
MA7	A9	A18	A9	A18	A9	A18
MA8	A10	A19	A10	A19	A10	A19
MA9	X	X	A11	A20	A11	A20
MA10	X	X	X	X	A12	A22

4.6 Parity Generation/Detection Logic

During local DRAM write cycles, the 82C499 generates a parity bit for each byte of write data from the processor. Parity bits are stored into local DRAM along with each data byte. During a DRAM read, the parity bit is checked for each data byte. If the logic detects incorrect parity, the 82C499 will generate NMI to the CPU. The parity error will invoke the NMI, providing that the parity check is enabled in the Configuration Register 21h, bit 5. Parity check must also be enabled in the Port B (61h) register, bits [2:3].

4.7 Refresh Logic

The 82C499 supports both normal and hidden refresh. Normal refresh refers to the classical refresh implementation which places the CPU on “hold” while a refresh cycle takes place to both the local DRAM and any AT bus memory. This is the default condition at power-up. However, hidden refresh is performed independent of the CPU and does not suffer from the performance restriction of losing processor bandwidth by forcing the CPU into its hold state. Hidden refresh delivers higher system performance and is recommended over normal refresh. As long as the CPU does not try to access local memory or the AT bus during a hidden refresh cycle, refresh will be transparent to the CPU. The CPU can continue to execute from its internal and secondary caches as well as execute internal instructions during hidden refresh without any loss in performance due to refresh arbitration. If a local memory or AT bus access is required during hidden refresh, wait states will be added to the CPU cycle until the resource becomes available. Hidden refresh also separates refreshing of the AT bus and local DRAM. The DRAM controller arbitrates between CPU DRAM accesses and DRAM refresh cycles, while the AT bus controller arbitrates between CPU accesses to the AT bus, DMA, and AT refresh. The AT bus controller asserts the RFSH# and MEMR# commands and outputs the refresh address during AT bus refresh cycles.

The 82C499 implements refresh cycles to the local DRAM using CAS-before-RAS timing. CAS-before-RAS refresh has lower power consumption than RAS-only refresh, which is important when dealing with large memory arrays. CAS-before-RAS refresh is used for both normal and hidden refresh to local memory.

The output of internal counter 1/timer 1 (OUT1) inside the 82C499 is programmed as a rate generator to produce the periodic refresh request signal which occurs every 15.9µs. Requests for refresh cycles are generated by two sources: counter1/timer1, or 16-bit ISA masters that activate refresh when they have bus ownership. These ISA masters supply refresh cycles because the refresh controller cannot preempt the bus master to perform the necessary refresh cycles. 16-bit ISA masters that hold the bus longer than 15µs must supply refresh cycles.

By programming Configuration Register 25h, bit 1, slow refresh is enabled which will further divide the 15.9µs period by four to provide a 63.6µs “slow refresh” interval (slow refresh DRAMs must be used with the slow refresh feature).

4.8 Shadow RAM

Since accesses to local DRAM are much faster than those to EPROM, the 82C499 provides shadow RAM capability. With this feature, code from slow devices like ROM and EPROM memories can be copied to local DRAM to speed up memory accesses. Accesses to the specified EPROM space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h-FFFFFh. 16KB granularity is provided for the address range C0000h-EFFFFh, while the 64KB range from F0000h-FFFFFh (the location of system BIOS) can be shadowed as an entire segment.

The shadow RAM control is setup in the configuration registers. First, the ROM contents must be copied into the shadow RAM area. Next, the shadow RAM enable bit is set in the configuration register. For the system BIOS area, once the bit is set, the RAM area becomes read-only. For the video and adapter BIOS area, the user can select read-only or read/write by setting the write protect bit in Index Register 26h accordingly. Video BIOS at the C0000h-C8000h area can be shadowed and cached if bit 4 of Register 27h is set to 1. System BIOS at F0000-FFFFF can also be shadowed if Register 22h bit 7 is set to 1. The system BIOS at F0000-FFFFF is non-cacheable.

4.9 System ROM BIOS Cycles and Flash EPROM Support

The 82C499 supports both 8- and 16-bit EPROM cycles. If the system BIOS is 16 bits wide, ROMCS# should be connected to M16# through an open collector gate indicating to the 82C499 that a 16-bit EPROM is responding. The system BIOS resides on the XD bus. The XD to SD data buffer is normally disabled (XDIR# inactive) except during I/O read cycles at addresses below 100h (byte-wide I/O), INTA cycles, and 8-bit ROM BIOS cycles.

ROMCS# is generated for the both the E0000-EFFFFh and F0000-FFFFFh segments. If a combined video/system ROM BIOS is desired, these two segments should be used.

For flash EPROM support, Register 26h, bit 7, can be set to 1 to enable write cycles for ROMCS# to support flash EPROMs. The desired segment must be selected via register 2Dh. Memory shadowing and caching should be disabled prior to making write accesses to the flash EPROM.

4.10 AT Bus State Machine

The AT bus state machine gains control when the 82C499's decoding logic detects a non-local memory cycle. It monitors status signals M16#, IO16#, CHRDY, and NOWS# and performs the necessary synchronization of control and status signals between the AT bus and the microprocessor. The 82C499 supports 8- and 16-bit memory and I/O devices located on the AT bus.

An AT bus cycle is initiated by asserting ALE in AT-TS1 state. On the trailing edge of ALE, M16# is sampled for a memory cycle to determine the bus size. It then enters AT-TC state and provides the command signal. For an I/O cycle, IO16# is sampled after the trailing edge of ALE until the end of the command. Typically, the wait state for an AT 8/16-bit transaction is 5/1, respectively. The command cycle is extended when CHRDY is detected inactive, or the cycle is terminated when zero wait state request signal (NOWS#) from the AT bus is active. Upon expiration of the wait states, the AT state machine terminates itself and passes an internal Ready to the CPU state machine for outputting a synchronous RDY# to the CPU. Bit 2 of Index Register 20h allows for the addition of an AT cycle wait state; bit 3 of this same register allows for the generation of a single ALE instead of multiple ALEs during bus conversion cycles. The AT bus state machine also routes data and address when an AT bus master or DMA controller accesses memory.

4.11 Bus Arbitration Logic

The 82C499 provides arbitration between the CPU, DMA controller, AT bus masters, and the refresh logic. During DMA, AT bus master, and conventional refresh cycles, the 82C499 asserts HOLD to the CPU. The CPU will respond to an active HOLD signal by generating HLDA (after completing its current bus cycle) and placing most of its output and I/O pins in a high impedance state. After the CPU relinquishes the bus, the 82C499 responds by issuing RFSH# (refresh cycle) or HLDA (AT bus master or DMA cycle), depending on the requesting device. During hidden refresh, HOLD remains negated and the CPU continues its current program execution as long as it services internal requests or achieves cache hits (please refer to the refresh section for additional information).

The AT bus controller in the 82C499 arbitrates between hold and refresh requests, deciding which will own the bus once the CPU relinquishes control with the HLDA signal. The arbitration between refresh and DMA/master is based on a FIFO (first in-first out) priority. However, a refresh request (RFSH#) will be inter-

nally latched and serviced immediately after DMA/ master finishes its request if queued behind HRQ. HRQ must remain active to be serviced if a refresh request comes first. DMA and bus masters share the same request pin, HRQ.

4.12 Numeric Coprocessor Cycles (NPX)

The 82C499 monitors NPERR# and NPBUSY# to provide support for the 80387 coprocessor. A coprocessor asserts NPERR# during a power-on reset to indicate its presence. The coprocessor asserts NPBUSY# while executing a floating-point calculation and asserts RDYI# to the chipset when it is finished. If NPBUSY# is active and a coprocessor error occurs, (coprocessor asserts NPERR#) the 82C499 latches NPBUSY# and generates INT13. Latched BUSY# and INT13 can be cleared by an I/O Port F0h write command. If the NPU is not installed, the 82C499 treats any access to the NPU address space as an AT cycle. With the NPU in place, CPU accesses to the NPU address space are direct, except for the re-synchronizing of the numerics coprocessor ready signal (RDYI#) before sending READY# back to the CPU.

4.13 Local Bus Interface

The 82C499 allows peripheral devices to share the “local bus” with the CPU and numerics coprocessor. The performance of these devices (which may include the video subsystem, hard disk adapters, LAN and other PC/AT controllers) will dramatically increase when allowed to operate in this high-speed environment. These devices are responsible for their own address and bus cycle decode and must be able to operate compatibly at the elevated frequencies required for operation on the local CPU bus.

The LDEV# input signal to the 82C499 indicates that a local device is intercepting the current cycle. If this signal is sampled at the end of the first T2 clock cycle (end of the second T2 at 50MHz, whenever ATCLK = CLKI/ 6), then the 82C499 will allow the responding local device to assume responsibility for the current local cycle. When the device has completed its operation, it must terminate the cycle by asserting the RDYI# pin of the 82C499. The RDYI# signal is synchronized by the 82C499 before being sent to the CPU via the RDY# line. Alternatively, the local bus device may drive RDY# directly to the CPU. In this case, the local READY signal should be connected to the CPU and 82C499 READY signal. The 82C499 READY signal is bidirectional.

4.14 Data Bus Conversion/Data Path Control Logic

The 82C499 performs data bus conversion when the CPU accesses 16- or 8-bit devices through 16- or 32-bit instructions. It also handles DMA and AT master cycles that transfer data between local DRAM or cache memory and locations on the AT bus. The 82C499 provides all of the signals to control external bidirectional data buffers.

4.15 Turbo/Slow Mode Operations

Turbo Mode is controlled through pin 99 of 82C499. If the TURBO input is asserted high, (the jumper on the board is opened) the system will always run at full speed and Non-turbo (slow) Mode when the TURBO input is pulled low (jumper is closed). Slow mode operation is implemented by applying a periodic clock to the HOLD input of the CPU. OSC12 is the clock source used for this operation. OSC12 is internally derived from the 14.31818MHz OSC clock input to the 82C499. The HOLD is maintained for approximately two-thirds of the time, while the CPU is allowed to perform normal external operations during the remaining one-third interval. For system design, the TURBO pin should be pulled high through a 10Kohm resistor.

4.16 Fast GATEA20 and RESET Emulation

The 82C499 will intercept commands to Ports 60h and 64h so that it can emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast CPURST signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast GATEA20 generation sequence involves writing “D1h” to Port 64h, then writing data “02h” to Port 60h. The fast CPU “warm reset” function is generated when a Port 64h write cycle with data “FEh” is decoded. A write to Port 64h with data “D0h” will enable the status of GATEA20 (bit 1 of Port 60h) and the warm reset (bit 0 of Port 60h) to be readable.

4.17 Special Cycles

The 486 microprocessors provide special bus cycles to indicate that certain instructions have been executed, or certain conditions have occurred internally. Special cycles such as Shutdown and Halt cycles are covered by dedicated handling logic in the 82C499. Based on the operating microprocessor mode, this logic decodes the CPU bus status signals M/IO#, D/C# and W/R# and takes the appropriate action.

5.0 Registers Descriptions

Table 5-1 Control Register 1 - Index: 20h

Bit(s)	Default	Function
7:6	00	Revision of 82C499 and is read-only.
5	0	Burst Wait State Control: 1 = Secondary Cache Read-Hit Cycle is x-2-2-2. 0 = Secondary Cache Read-Hit Cycle is x-1-1-1. No effect on Intel 386, IBM/Cyrix 486DLC.
4	0	AT Clock Source Selections: 0 = Source from CLK2I 1 = Source from CLK1
3	0	Single ALE Enable: 82C499 will activate single ALE instead of multiple ALEs during bus conversion cycle if this bit is enabled. 0 = Disable 1 = Enable
2	0	Extra AT Cycle Wait State Enable: Insert one extra wait state for the command signals in standard AT bus cycle. 0 = Disable 1 = Enable
1	0	Emulation keyboard Reset Control: 1 = CPU reset is generated immediately after a write to Port 64h. 0 = A “halt” instruction needs to execute after a write to Port 64h in order to cause a CPU reset.
0	0	Fast Reset: The 82C499 generates a CPU reset whenever a “halt” instruction is executed. 0 = Disable 1 = Enable

Table 5-2 Control Register 2 - Index: 21h

Bits	Default	Function
7	0	Master Mode Byte Swap Enable: 0 = Disable 1 = Enable
6	0	Cache Write Wait States Control 1 = 2 wait states, bit 1 of Index Register 21h will be ignored 0 = Either 0 or 1 wait state, refer to bit 1 of Index Register 21h
5	0	Parity Check: 0 = Enable 1 = Disable
4	0	Cache Enable: 0 = cache is disabled and DRAM burst mode is enabled 1 = cache enable and DRAM burst mode is disabled
3:2	00	Cache Size: **3 2 Cache Size** 0 0 64KB 0 1 128KB 1 0 256KB 1 1 512KB
1	00	Cache Write 0/1 Wait State Control with bit 6 of Index Register 21h = 0: 0 = 1 wait state 1 = 0 wait state

Bits	Default	Function
0	00	Cache Read Wait State Control: For Intel 486: 0 = 3-x-x-x cycle 1 = 2-x-x-x cycle For Intel 386, IBM/Cyrix 486DLC: 0 = 1ws 1 = 0ws

Table 5-3 Shadow RAM Control Register I - Index: 22h

Bit(s)	Default	Function
7	1	ROM(F0000-FFFFFh) Enable: 1 = Read from ROM, write to DRAM. ROMCS# is generated during read access only. 0 = Read/write on DRAM and DRAM is write-protected.
6	0	Shadow RAM at D0000h-DFFFFh Area: 0 = Disable 1 = Enable
5	0	Shadow RAM at E0000h-EFFFFh Area: 0 = Disable shadow RAM, enable ROMCS#. The E0000-EFFFFh ROM is defaulted to reside on XD bus. 1 = Enable shadow RAM and disable ROMCS# generation.
4	0	Shadow RAM at D0000h-DFFFFh Area Write Protect Enable: 0 = Disable 1 = Enable
3	0	Shadow RAM at E0000h-EFFFFh Area Write Protect Enable: 0 = Disable 1 = Enable
2	1	Hidden Refresh Enable (without holding CPU): 1 = Disable 0 = Enable.
1	0	Fast GATEA20/A20M#: **Intel 386 Mode:** 1 = GA20 is high 0 = Controlled by keyboard emulation **Intel486 IBM/Cyrix 486DLC Mode:** 1 = A20M# is always high, no address wraps around 0 = Controlled by keyboard emulation
0	0	Slow Refresh Enable (four times slower than the normal refresh) 0 = Disable 1 = Enable

Table 5-4 Shadow RAM Control Register II - Index: 23h

Bit	Default	Function
7	0	Shadow RAM at EC000h-EFFFFh Area: 0 = Disable 1 = Enable
6	0	Shadow RAM at E8000h-EBFFFh Area: 0 = Disable 1 = Enable
5	0	Shadow RAM at E4000h-E7FFFh Area: 0 = Disable 1 = Enable
4	0	Shadow RAM at E0000h-E3FFFh Area: 0 = Disable 1 = Enable

Bit	Default	Function
3	0	Shadow RAM at DC000h-DFFFFh Area: 0 = Disable 1 = Enable
2	0	Shadow RAM at D8000h-DBFFFh Area: 0 = Disable 1 = Enable
1	0	Shadow RAM at D4000h-D7FFFh Area: 0 = Disable 1 = Enable
0	0	Shadow RAM at D0000h-D3FFFh area 0 = Disable 1 = Enable

Table 5-5 DRAM Control Register I - Index: 24h

Bit(s)	Default	Function
7	1	0 = 256KB DRAM mode 1 = 1MB and 4MB DRAM mode. See Table 4, “DRAM Configurations,” on page 16.
6:4	000	DRAM types used for Bank 0 and Bank 1. Refer to Table 4-4 for detailed description.
3	0	Unused
2:0	111	DRAM types used for Bank 2 and Bank 3. Refer to Table 4-4 for detailed description.

Table 5-6 DRAM Control Register II - Index: 25h

Bit(s)	Default	Function
7:6	11	CAS# Wait State Control for DRAM Read Cycle: **7 6 CAS# Pusle width Cycle Time Notes** 0 0 n/a n/a Not used. 0 1 3 CLKs 7-5-5-5 CAS# will shift later by 1 CLK and the CAS# pulse width will increase by 1 CLK 1 0 4 CLKs 8-6-6-6 Only CAS# pulse width increases 1 1 5 CLKs 9-7-7-7 Only CAS# pulse width increases
5:4	11	CAS# Wait State Control for DRAM Write Cycle: 5 4 CAS# Pulse Width CAS# Precharge Cycle Time 0 0 2 CLKs 1 CLK 6-3-3-3 0 1 2 CLKs 3 CLKs 8-5-5-5 1 0 3 CLKs 3 CLKs 9-6-6-6 1 1 4 CLKs 3 CLKs 10-7-7-7
3	0	Fast Decode Enable. This function may be enabled in 20/25MHz operation to speed up the DRAM access. 0 = Disable fast decode, DRAM base wait states is not changed 1 = Enable fast decode, DRAM base wait states is decreased by 1 This bit is automatically disabled even when it is set to 1 when bit 4 of Index register 21h (cache enable bit) is enabled. It only affects the DRAM lead-off cycle.
2	0	CAS# Delay for DMA/Master Cycles: 0 = Disable - CAS# will be generated one CPUCLK after RAS# is asserted. 1 = Enable - CAS# will be generated after RAS# is asserted for two CPUCLKs.

Bit(s)	Default	Function
1:0	00	ATCLK Selection (refer to bit 4 of Index Register 20h): **1 0 ATCLK Selection** 0 0 CLKI/6 (Default, indicate 82C499 is running at 50MHz, LDEV# will be sampled at the end of the second T2) 0 1 CLKI/5 1 0 CLKI/4 1 1 CLKI/3

Table 5-7 Shadow RAM Control Register III - Index: 26h

Bit(s)	Default	Function
7	0	Enable ROMCS# for Write Cycles: 1 = Enable, generates ROMCS# for write cycles to support flash ROMs. 0 = Disable
6	0	Shadow RAM copy enable for address area C0000h-CFFFFh: 0 = Read/write at AT bus 1 = Read from AT bus and write into shadow RAM
5	0	Shadow write protect at address area C0000h-CFFFFh: 0 = Write protect disable 1 = Write protect enable
4	0	Shadow RAM enable at C0000h-CFFFFh Area: 0 = Disable 1 = Enable
3	0	Enable shadow RAM at CC000h-CFFFF Area: 0 = Disable 1 = Enable
2	0	Enable shadow RAM at C8000h-CBFFF Area: 0 = Disable 1 = Enable
1	0	Enable shadow RAM at C4000h-C7FFFh Area: 0 = Disable 1 = Enable
0	0	Enable shadow RAM at C0000h-C3FFFh Area: 0 = Disable 1 = Enable

Table 5-8 Control Register 3 - Index: 27h

Bit(s)	Default	Function
7	1	Global Cache Enable: This bit determines whether all cycles are cacheable in L1 and L2 cache. 0 = Disable L1 and L2 cache 1 = Enable L1 and L2 cache
6	1	Fast AT Cycle: 0 = Disable, BALE# will be asserted 1 ATCLK late as standard AT cycles 1 = Enable, standard AT cycles
5	0	Back-to-Back I/O Delay Control: 0 = Three BLK back-to-back I/O delay 1 = Zero back-to-back I/O delay
4	1	Video BIOS at C0000h-C8000h area non-cacheable: 0 = Cacheable 1 = Non-cacheable

Bit(s)	Default	Function
3:0	0001	Cacheable Address Range for Local Memory: **3 2 1 0 Cacheable Address Range** 0 0 0 0 0-64MB 0 0 0 1 0-4MB 0 0 1 0 0-8MB 0 0 1 1 0-12MB 0 1 0 0 0-16MB 0 1 0 1 0-20MB 0 1 1 0 0-24MB 0 1 1 1 0-28MB 1 0 0 0 0-32MB 1 0 0 1 0-36MB 1 0 1 0 0-40MB 1 0 1 1 0-44MB 1 1 0 0 0-48MB 1 1 0 1 0-52MB 1 1 1 0 0-56MB 1 1 1 1 0-60MB **Note** If total memory is 1MB or 2MB, the cacheable range is 0-1 or 0-2MB respectively and independent of the value of bits [3:0] of Index Register 27h.

Note Memory area at 640KB-1MB is defaulted to be non-cacheable.

Table 5-9 Non-Cacheable Block 1 Register - Index: 28h

Bit(s)	Default	Function
7:5	100	Size of Non-cachable Memory Block 1: **7 6 5 Block Size** 0 0 0 64KB 0 0 1 128KB 0 1 0 256KB 0 1 1 512KB 1 X X Disabled
4:2	000	Unused
1:0	00	Address bits of A25 and A24 of Non-cachable Memory Block 1

This register is used in conjunction with Index Register 29h to define a non-cacheable block. The starting address for the non-cacheable block must have the same granularity as the block size. For example, if a 512KB non-cacheable block is selected, its starting address is a multiple of 512KB; consequently, only address bits of A[23:19] are significant, A18:16] are "don't care".

Table 5-10 Non-Cacheable Block 1 Register II - Index: 29h

Bit(s)	Default	Function
7:0	0001 XXXX	Address bits A[23:16] of Non-cacheable Memory Block 1 **Valid Starting Address Bits** **Block Size A23 A22 A21 A20 A19 A18 A17 A16** 64KB V V V V V V V V 128KB V V V V V V V X 256KB V V V V V V X X 512KB V V V V V X X X

X = Don't Care
V = Valid Bit

Table 5-11 Non-Cacheable Block 2 Register I - Index: 2Ah

Bit(s)	Default	Function
7:5	100	Size of Non-cacheable Memory Block 2: **7 6 5 Block Size** 0 0 0 64KB 0 0 1 128KB 0 1 0 256KB 0 1 1 512KB 1 X X Disabled
4:3	00	ECAWE#/OCAWE# Pulse Width for Master Cache Write-Hit Cycles: 4 3 Selections 0 0 3 CLKs (default) 1 0 1 CLK 1 1 Unused 0 1 Unused
2	0	Unused, must be set to 1 by BIOS.
1:0	0	Address bits of A25 and A24 of Non-cacheable Memory Block 2

This register is used in conjunction with Index Register 2Bh to define a non-cacheable block. The starting address for the non-cacheable block must have the same granularity as the block size. For example, if a 512KB non-cacheable block is selected, its starting address is a multiple of 512KB; consequently, only address bits of A[23:19] are significant, [A18:16] are "don't care".

Table 5-12 Non-Cacheable Block 2 Register II - Index: 2Bh

Bit(s)	Default	Function
7:0	0001 XXXX	Address bits A[23:16] of Non-cacheable Memory Block 2

	Valid Starting Address Bits							
Block Size	**A23**	**A22**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**
64KB	V	V	V	V	V	V	V	V
128KB	V	V	V	V	V	V	V	X
256KB	V	V	V	V	V	V	X	X
512KB	V	V	V	V	V	X	X	X

X = Don't Care
V = Valid Bit

Table 5-13 ROM Chip Select (ROMCS#) Control Register - Index: 2Dh

Bit(s)	Default	Function
7	0	Unused
6	1	0 = IBM 486DLC CPU. This bit is write-only. **Note:** This bit must be cleared to 0 by the BIOS to support the IBM 486DLC (Blue Lightning) CPU.
5	0	Enable ROMCS# at E8000h-EFFFFh Segment: 0 = Disable 1 = Enable

4	0	Enable ROMCS# at E0000h-E7FFFh Segment: 0 = Disable 1 = Enable
3	0	Enable ROMCS# at D8000h-DFFFFh Segment: 0 = Disable 1 = Enable
2	0	Enable ROMCS# at D0000h-D7FFFh Segment: 0 = Disable 1 = Enable
1	0	Enable ROMCS# at C8000h-CFFFFh Segment: 0 = Disable 1 = Enable
0	0	Enable ROMCS# at C0000h-C7FFFh Segment: 0 = Disable 1 = Enable

5.1 I/O Port 60h

Port 60h and 64h emulate the registers of a keyboard controller, allowing the generation of a fast gate A20 signal. The sequence here is BIOS transparent and there is no need for the modification of the current BIOS. The sequence involves writing data D1h to Port 64h, then writing data 02h to Port 60h.

Table 5-14 I/O Port 61h(Port B)

Bit(s)	Type	Function
0	R/W	Timer 2 Gate
1	R/W	Speaker Output Enable
2	R/W	Parity Check Enable
3	R/W	I/O Channel Check Enable
4	R	Refresh Detect
5	R	Timer OUT2 Detect
6	R	I/O Channel Check
7	R	System Parity Check

5.2 I/O Port 64h

I/O Port 64h emulates the register inside a keyboard controller by generating a fast reset pulse. Writing data FEh to Port 64h asserts the reset pulse. The pulse is generated immediately after the I/O write if bit 6 of Index Register 21h is set, otherwise the pulse is asserted 2µs after the write.

Table 5-15 I/O Port 70h

Bit(s)	Default	Function
7	0	NMI Enable

Table 5-16 Port 92h - System Controller Port A, PS/2 Compatibility Port

Bit(s)	Default	Function
1		1 = Set Alernate Fast GATEA20 Active
0		1 = Set Alternate Fast Reset Active

6.0 Maximum Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage		+6.5	V
V_I	Input Voltage	-0.5	V_{CC} + 0.3	V
V_O	Output Voltage	-0.5	V_{CC} + 0.3	V
T_{OP}	Operating Temperature	-25	+70	°C
T_{STG}	Storage Temperature	-40	+125	°C

6.2 DC Characteristics

Ta = -25°C to +70°C, Vcc = 5.0V ±5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.4	V	L_{OL} = 4.0mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1.6mA
I_{IL}	Input Leakage Current		10	µA	$V_{IN} = V_{CC}$
I_{OZ}	Tristate Leakage Current		10	µA	
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	
I_{CC}	Power Supply Current		80	mA	

6.3 AC Timing Characteristics

Preliminary - Temperature: 0°C to +70°C, VCC: 5V +/- 5%

Table 6-1 82C499 B1 AC Characteristics

Sym	Description	Min	Typ	Max	Units
t100a	CLKI↑ delay from CLK2I↑	3		7	ns
t100b	CLKI↓ delay from CLK2I↑	3		7	ns
t103	CPURST active delay from CLKI↑	4		20	ns
t103a	CPURST active delay from CLK2I↑	3		7	ns
t104	CPURST inactive delay from CLKI↑	4		20	ns
t104a	CPURST inactive delay from CLK2I↑	3		7	ns
t201	CLKI↑ to CAS# active delay, refresh	7		21	ns
t202	CLKI↓ to CAS# inactive delay, refresh	7		21	ns
t203	CLKI↑ or CLKI↓ to RAS# active delay, refresh	7		21	ns
t204	CLKI↑ or CLKI↓ to RAS# inactive delay, refresh	7		21	ns
t205	RAS# pulsh width, refresh		4CLKs		
t206	CAS# pulsh width, refresh		5.5CLKs		
t210	LDEV# setup time to CLKI↑	4			ns
t211	LDEV# hold time to CLKI↑	5			ns
t213	KEN# active delay from CLKI↑			15	ns
t214	KEN# inactive delay from Address			20	ns
t215	RDYI# setup time to CLKI↑	4			ns
t216	RDYI hold time to CLKI↑	5			ns
t301	D(31:0) valid to SD(15:0) valid delay	10		100	ns
t302	D(31:0) valid to MP(3:0) valid delay	15		30	ns
t303	D(31:0) invalid to SD(15:0) invalid delay	10		25	ns
t304	D(31:0) invalid to MP(3:0) invalid delay	15		30	ns
t305	SD(15:0) valid to D(31:0) valid delay	10		20	ns
t306	SD(15:0) invalid to D(31:0) invalid delay	10		20	ns
t313	A(9:0) to KBDCS# active delay	10		100	ns
t314	A(9:0) to KBDCS# inactive delay	10		30	ns
t402	CPU address and status valid to BEOE# active delay	5		21	ns
t403	CLKI↑ to BEOE# /BOOE# inactive delay	5		13	ns
t404	CLKI↑ to BEOE#/BOOE# active delay	5		14	ns
t405	CLKI↑ to CA32S# inactive delay	5		14	ns
t406	CLKI↑ to CA32S# active delay	5		14	ns
t407	CLKI↑ (from TAG address valid) to BRDY# active delay	5 (9)		15 (15)	ns
t408	CLKI↑ to BRDY# inactive delay	5		15	ns
t411	CLK2I↑ to ECAWE#/OCAWE# active delay, 0WS (requires 2X clock input)	5		10	ns
t412	CLK2I↑ to ECAWE#/OCAWE# inactive delay, 0WS (requires 2X clock input)	5		10	ns
t413	CLKI↓ to ECAWE#/OCAWE# active delay, 1WS	20		22	ns

Table 6-1 82C499 B1 AC Characteristics (cont.)

Sym	Description	Min	Typ	Max	Units
t413a	CLKI↑ to ECAWE#/OCAWE# active delay, cache line fill	7		21	ns
t414	CLKI↓ to ECAWE#/OCAWE# inactive delay, 1WS	10		12	ns
t414a	CLKI↑/CLKI↓ to ECAWE#/OCAWE# inactive delay, cache line fill	7		21	ns
t415	CLK2I↑ to DTYWE# active delay, 0WS (requires 2X clock input)	5		10	ns
t416	CLK2I↑ to DTYWE# inactive delay, 0WS (requires 2X clock input)	5		10	ns
t417	CLKI↓ to DTYWE# active delay, 1WS	20		22	ns
t418	CLKI↓ to DTYWE# inactive delay, 1WS	10		12	ns
t419	CLKI↑ (from TAG address valid) to RDY# active delay	5 (9)		15 (15)	ns
t420	CLKI↑ to RDY# inactive delay	5		15	ns
t421	DTYWE# active to DRTY active	2		4	ns
t422	DTYWE# inactive to DRTY inactive	2		4	ns
t423	CLKI↓ to TAGWE# active delay	20		22	ns
t424	CLKI↓ to TAGWE# inactive delay	10		12	ns
t425	CLKI↑ to BEA3/BEA2OA3 active delay, cache hit (cache line fill)	5 (7)		15 (21)	ns
t425a	CLKI↓ to BEA3/BEA2OA3 active delay, cache hit	5		15	ns
t426	CLKI↑ to BEA3/BEA2OA3 hi-Z	5		15	ns
t427	TAGWE# active to TAG data active	2		4	ns
t428	TAGWE# inactive to TAG data inactive	2		4	ns
t429	CLKI↑ to CAS# active delay	5		15	ns
t430	CLKI↑ to CAS# inactive delay	5		15	ns
t433	CLKI↑ to RAS# inactive delay	5		15	ns
t434	CLKI↑ to RAS# active delay	5		15	ns
t435	CLKI↑ to column address valid delay	5		15	ns
t436	CPU address valid to row/column address valid delay	5		15	ns
t437	CLKI↑ to DWE# active delay	5		15	ns
t438	CLKI↓ to DWE# inactive delay	5		15	ns
t439	CLKI↑ to new row address delay	10		25	ns
t440	RAS# precharge time		3 CLKI		
t441	CAS# precharge time	1 CLKI			
t442	CLKI↑ to ROMCS# active delay	7		21	ns
t443	CLKI↑ to ROMCS# inactive delay	7		21	ns
t454	MEMR# active to BEOE#/BOOE# active delay, DMA	10		20	ns
t455	MEMR# inactive to BEOE#/BOOE# inactive delay, DMA	10		20	ns
t456	CLKI↑ to EADS# active delay, DMA	6		18	ns
t457	CLKI↑ to EADS# inactive delay, DMA	6		18	ns
t458	MEMR#/MEMW# active to RAS# active delay, DMA	10		20	ns
t459	MEMR#/MEMW# inactive to CAS# inactive delay, DMA	10		20	ns
t465	MEMW# active to DWE# active delay, DMA	10		20	ns
t466	MEMW# inactive to DWE# inactive delay, DMA	10		20	ns
t467	DRTY set up time to CLKI↑	4			ns

Table 6-1 82C499 B1 AC Characteristics (cont.)

Sym	Description	Min	Typ	Max	Units
t468	DRTY hold time to CLKI↑	5			ns
t501	BCLK↓ to ALE active delay	2		20	ns
t502	BCLK↑ to ALE inactive delay	2		20	ns
t503	BCLK↓ to CMD active delay	2		20	ns
t504	BCLK↑ to CMD inactive delay	2		20	ns
t505	BCLK↑ to CMD active delay	2		20	ns
t506	MCS16# to BCLK↑ setup time	10			ns
t507	MCS16# to BCLK↑ hold time	10			ns
t508	IOCS16# to BCLK↑ setup time	10			ns
t509	IOCS16# to BCLK↑ hold time	10			ns
t510	OWS# to BCLK↓ setup time	10			ns
t511	OWS# to BCLK↓ hold time	20			ns
t512	CHRDY to BCLK↑ setup time	10			ns
t513	CHRDY to BCLK↑ hold time	20			ns
t515	CLK↑ to HOLD active delay	7		21	ns
t516	CLK↑ to HOLD inactive delay	7		21	ns
t517	BCLK↑ to REF# active delay	8		30	ns
t518	BCLK↑ to REF# inactive delay	8		30	ns
t519	BCLK↑ to MEMR# active delay, refresh	5		25	ns
t520	BCLK↑ to MEMR# inactive delay, refresh	5		25	ns
t521	BCLK↑ to SA[1:0] active delay	7		21	ns
t522	BCLK↑ to SA[1:0] inactive delay	7		21	ns
t523	CMD# active to XDIR# active delay	5		15	ns
t524	CMD# inactive to XDIR# inactive delay	5		15	ns
t530	CLK↑ to ADS# active delay, DMA	6		18	ns
t531	CLK↑ to ADS# inactive delay, DMA	6		18	ns
t532	MEMR#/MEMW# active to M/IO valid delay, DMA	7		21	ns
t533	MEMR#/MEMW# inactive to M/IO invalid delay, DMA	7		21	ns
t534	MEMR#/MEMW# active to W/R valid delay, DMA	7		21	ns
t535	MEMR#/MEMW# inactive to W/R invalid delay, DMA	7		21	ns
t536	LREQ# setup time to CLK↑	4			ns
t537	LREQ# hold time to CLK↑	5			ns
t538	HLDA setup time to CLK↑	4			ns
t539	HLDA hold time to CLK↑	5			ns
t540	CLK↑ to LGNT# active delay	10		25	ns

Note Notes:*1.*↑ means rising edge

Note *2.*↓ means falling edge

Note 3.The capacitance loading is 50pF

6.4 AC Timing Waveforms

Figure 6-1 2-1-1-1 Double Bank Cache Read Hit Cycle

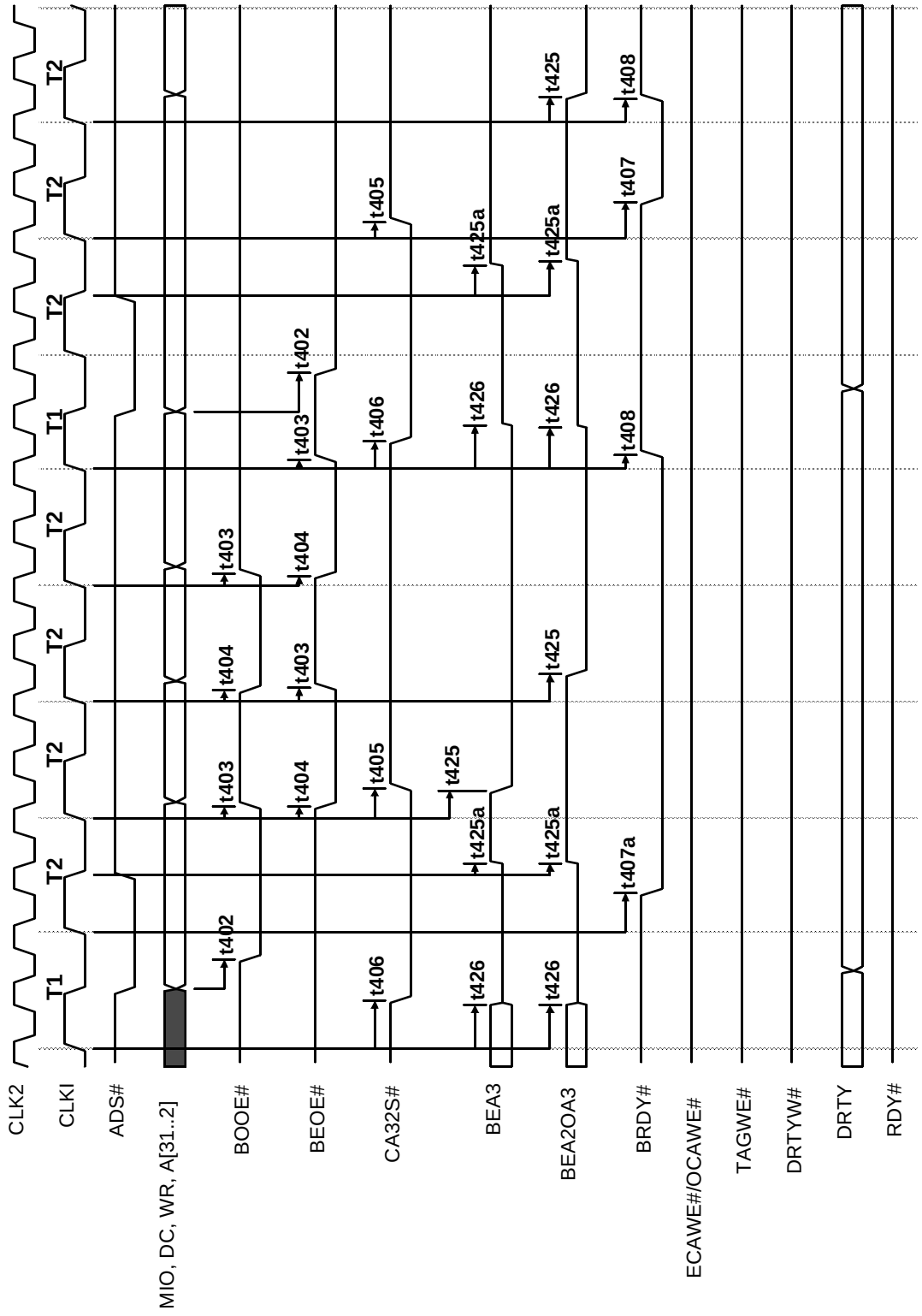


Figure 6-2 3-1-1-1 Single Bank Cache Read Hit Cycle

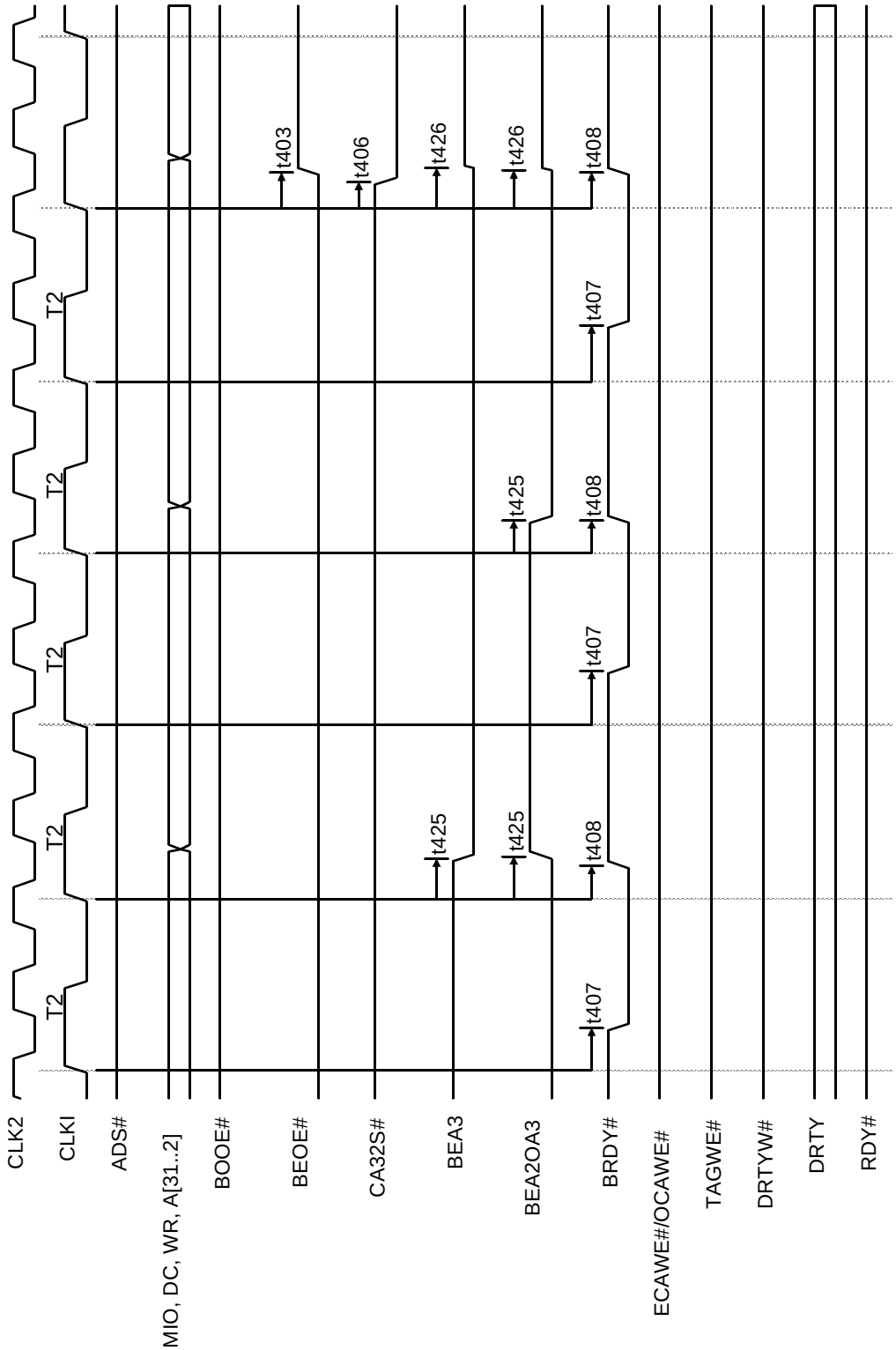


Figure 6-3 Zero-Wait State Write Hit Cycle

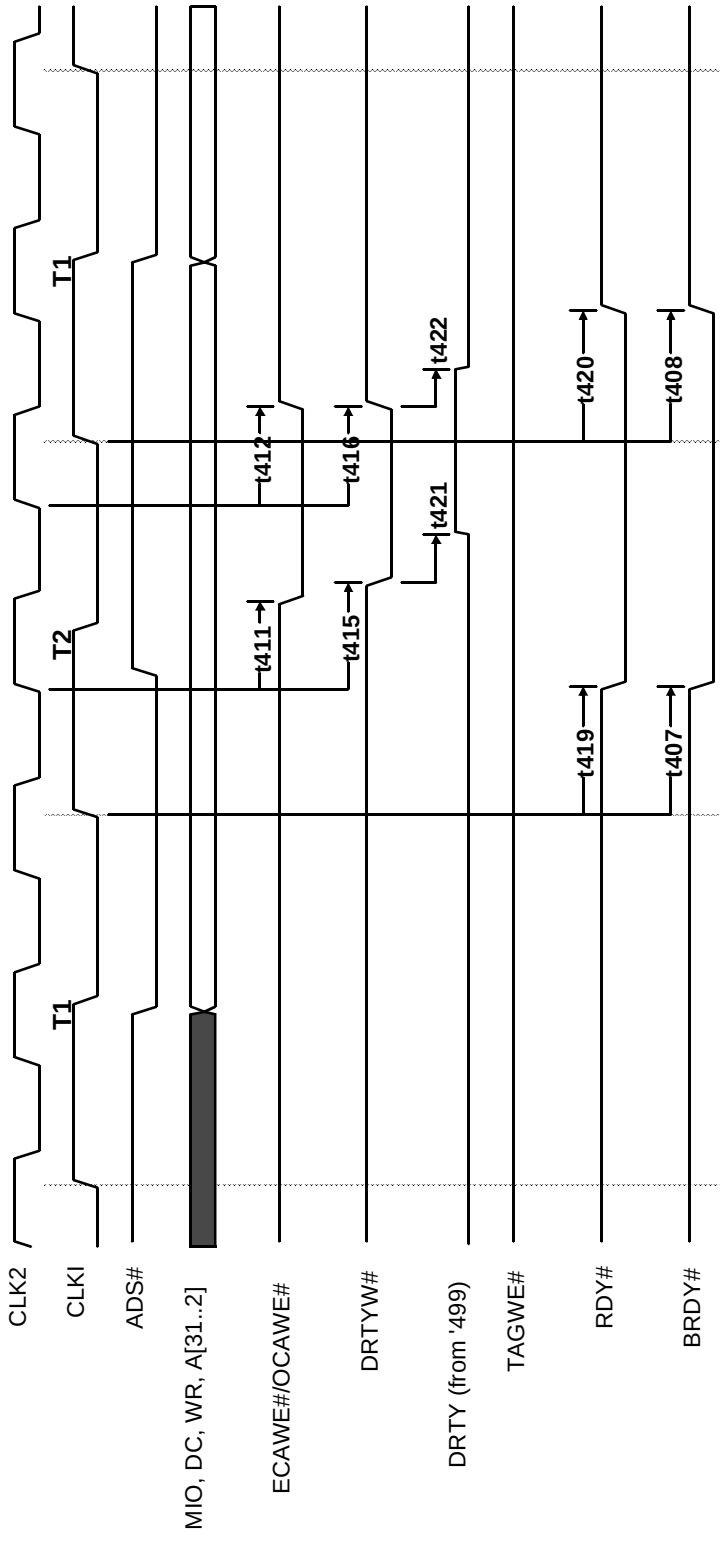


Figure 6-4 One-Wait State Cache Write Hit Cycle

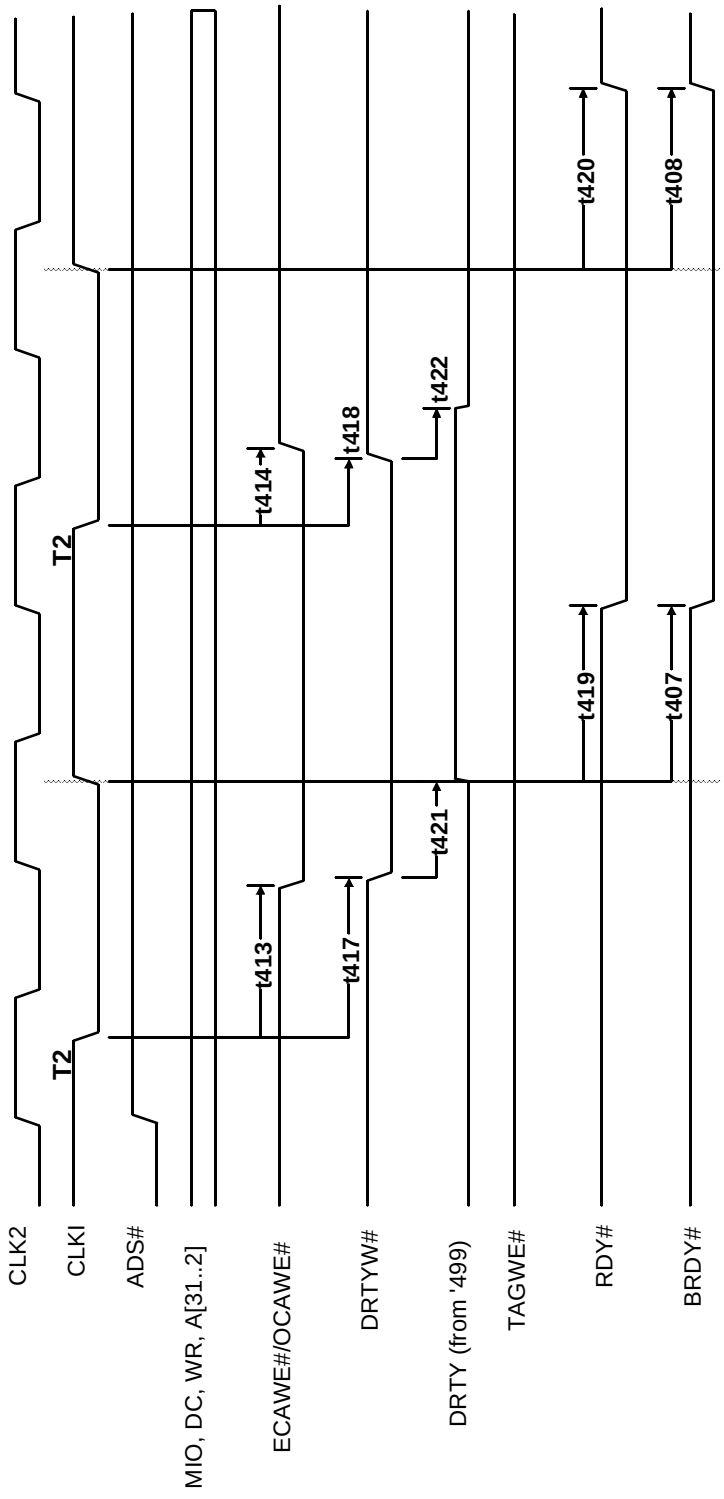


Figure 6-5 DMA/ISA Master Transfer

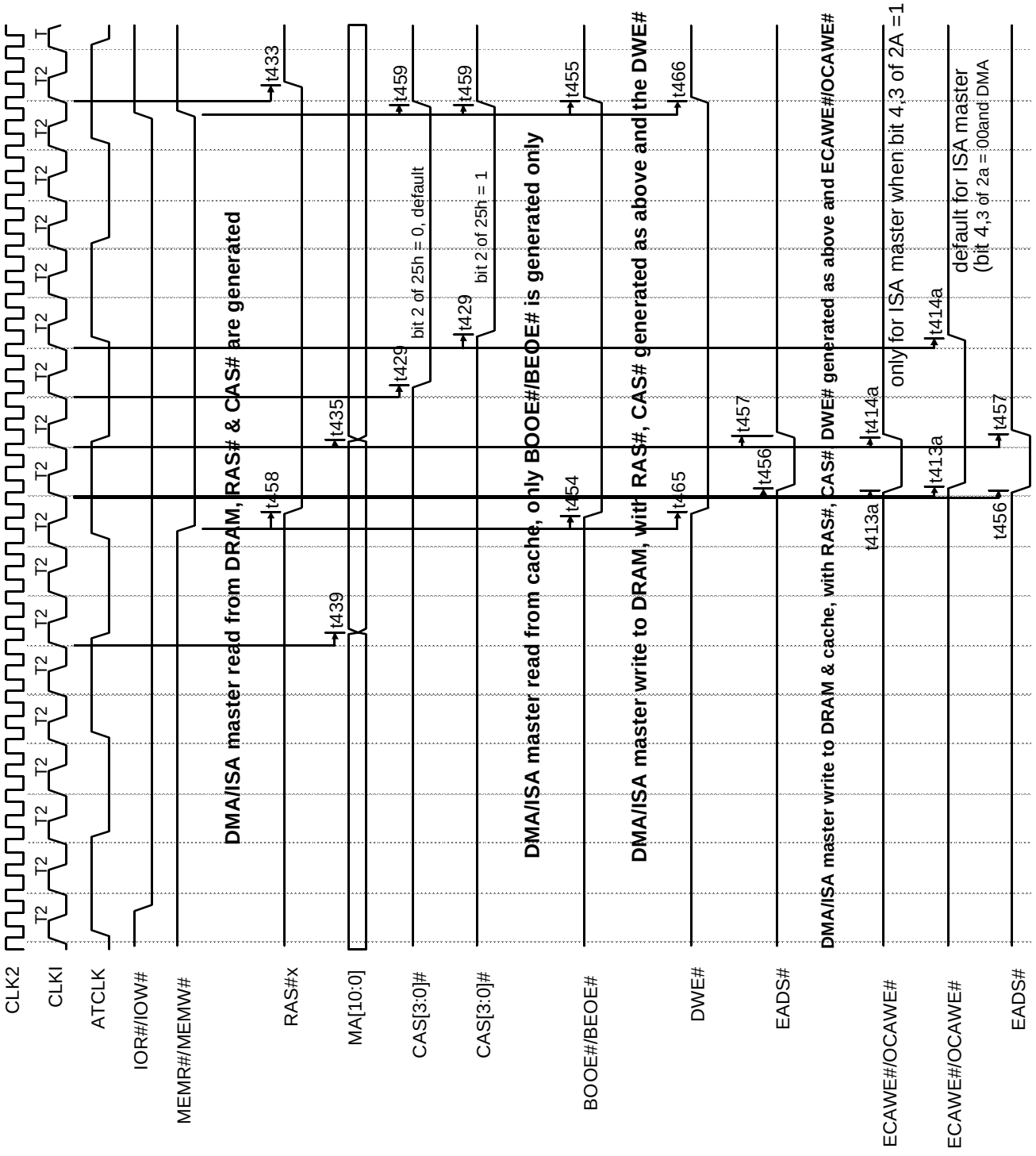


Figure 6-6 One-Wait State DRAM Read

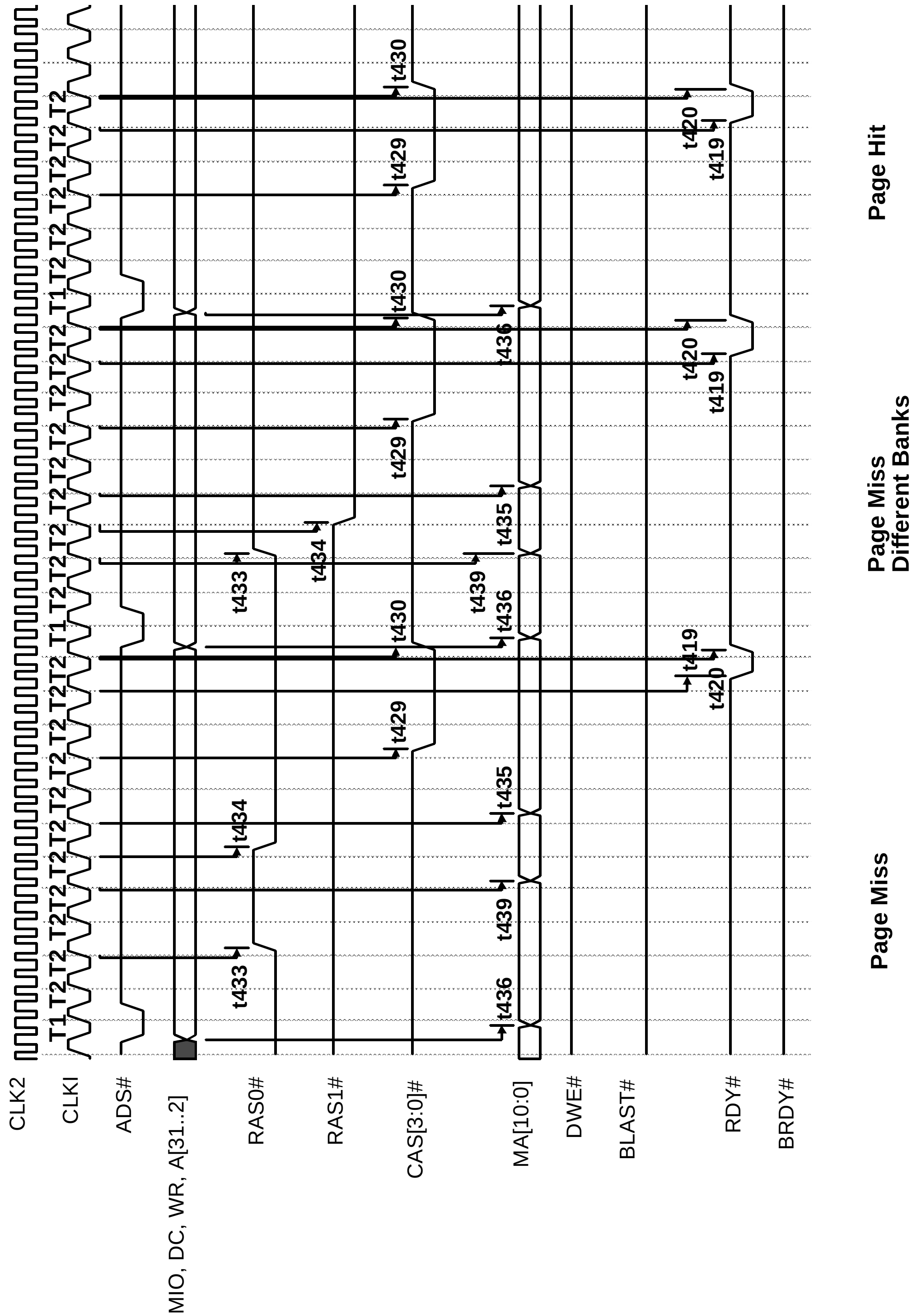


Figure 6-7 One-Wait State DRAM Page Hit Burst Read

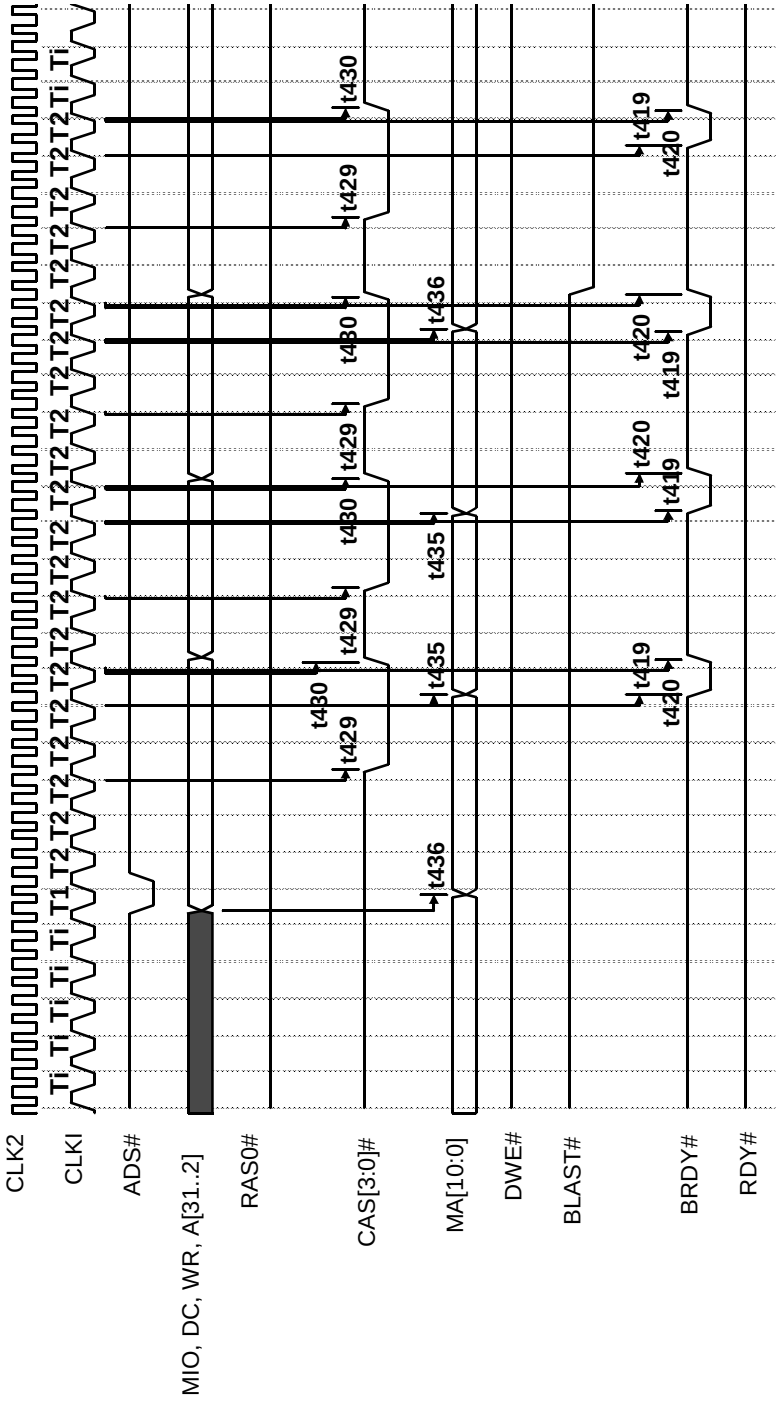


Figure 6-8 One-Wait State DRAM Burst Read, RAS# Inactive

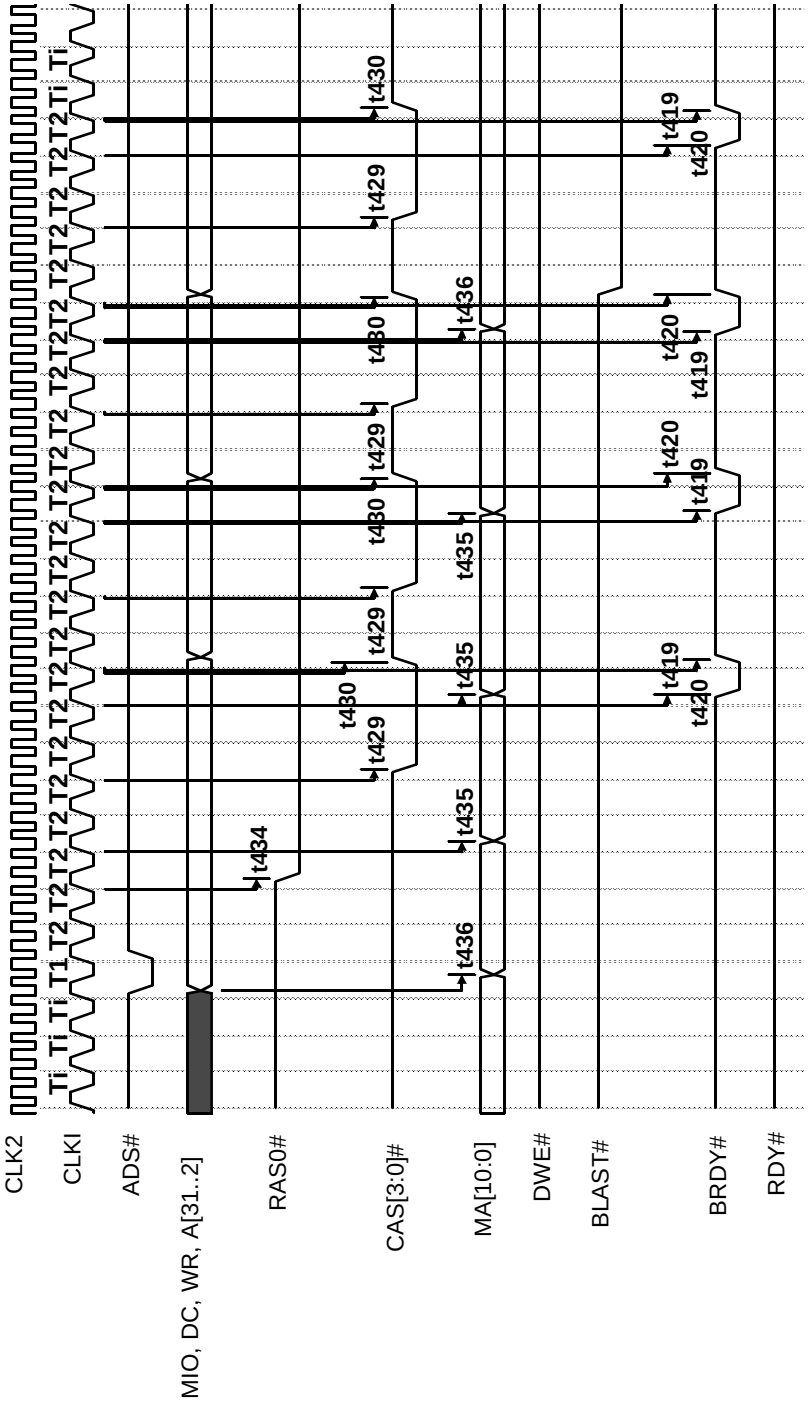


Figure 6-9 One-Wait State DRAM Page Miss Burst Read

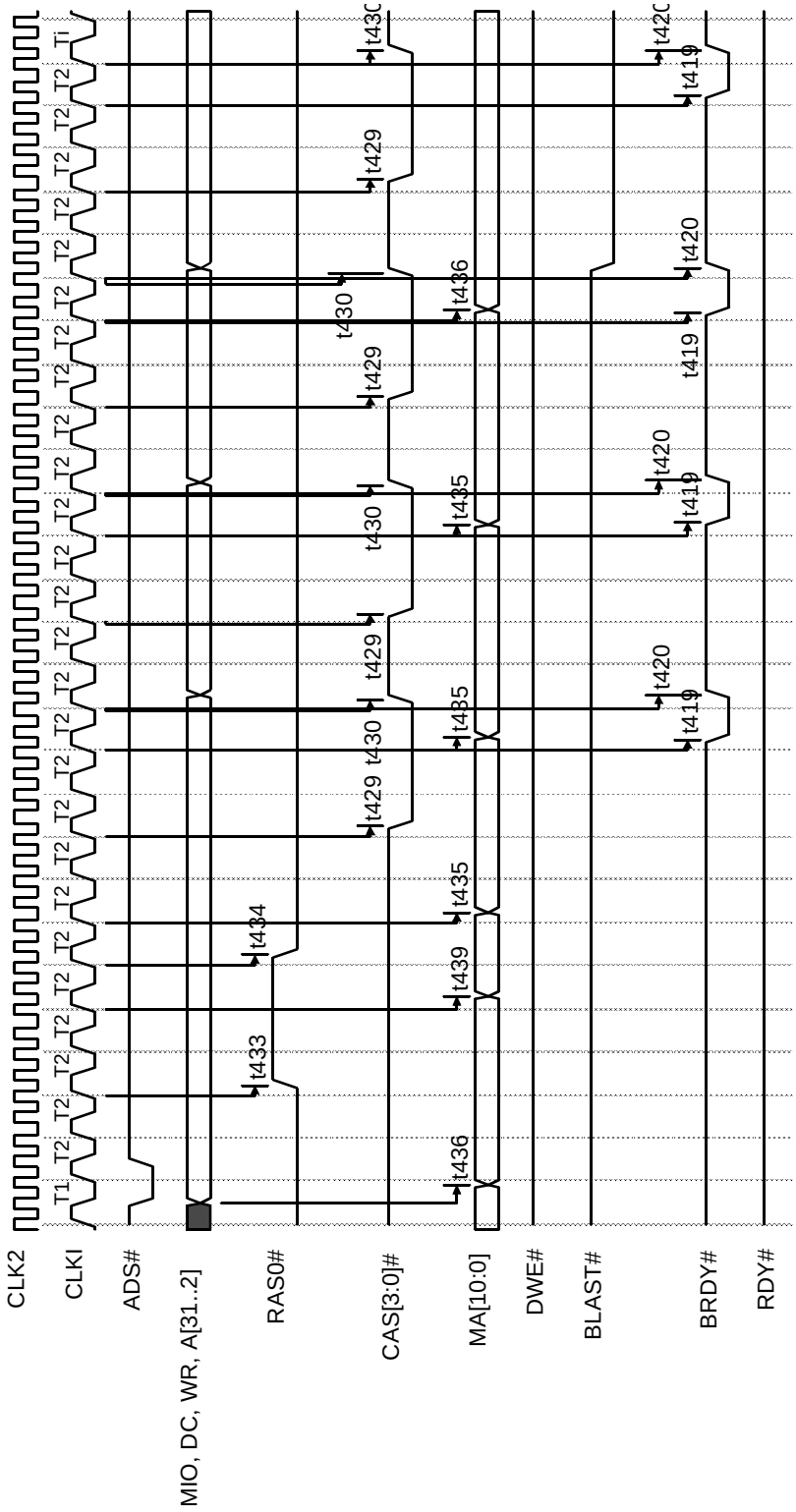


Figure 6-10 Zero-Wait State DRAM Write

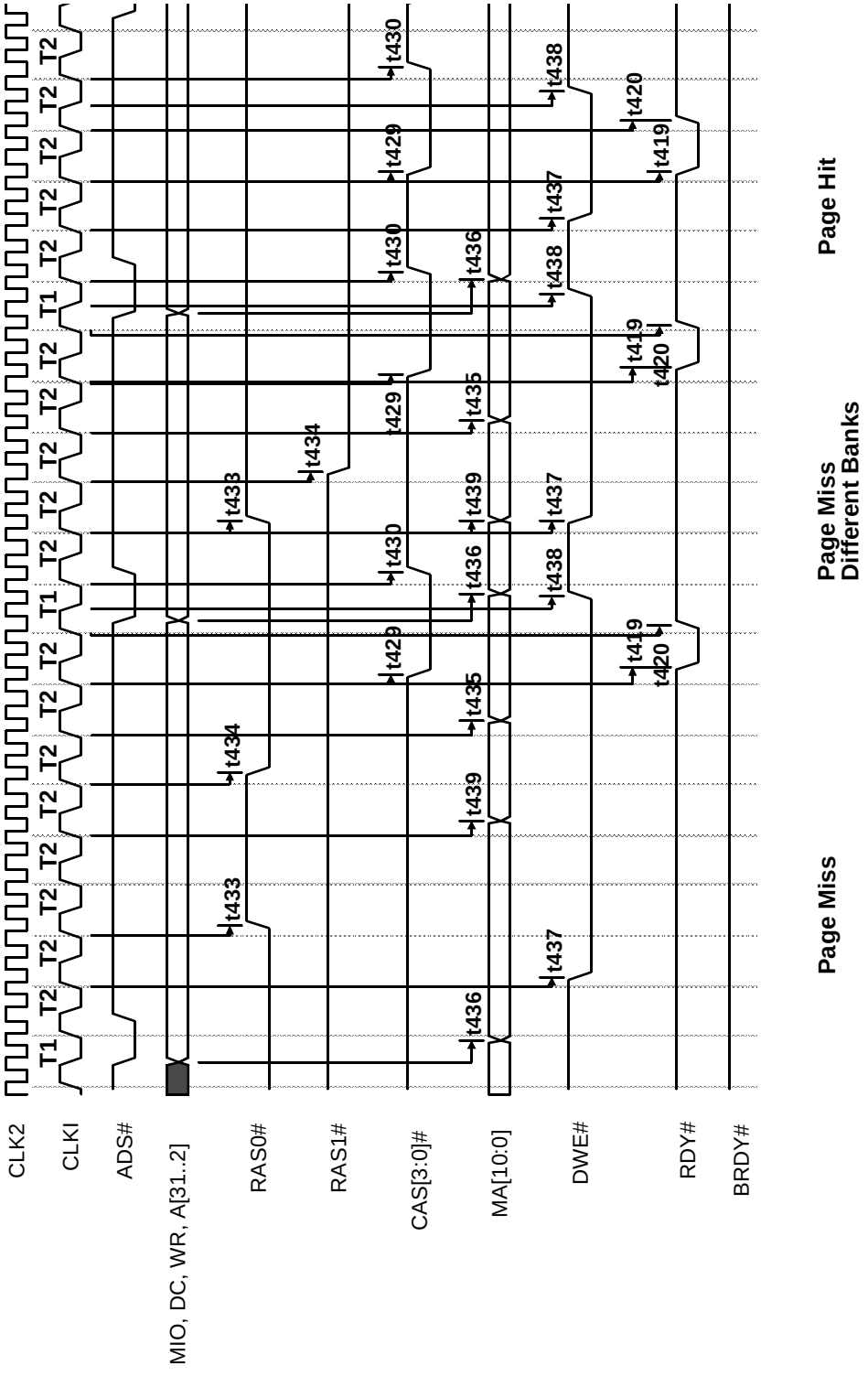


Figure 6-11 One-Wait State DRAM Write

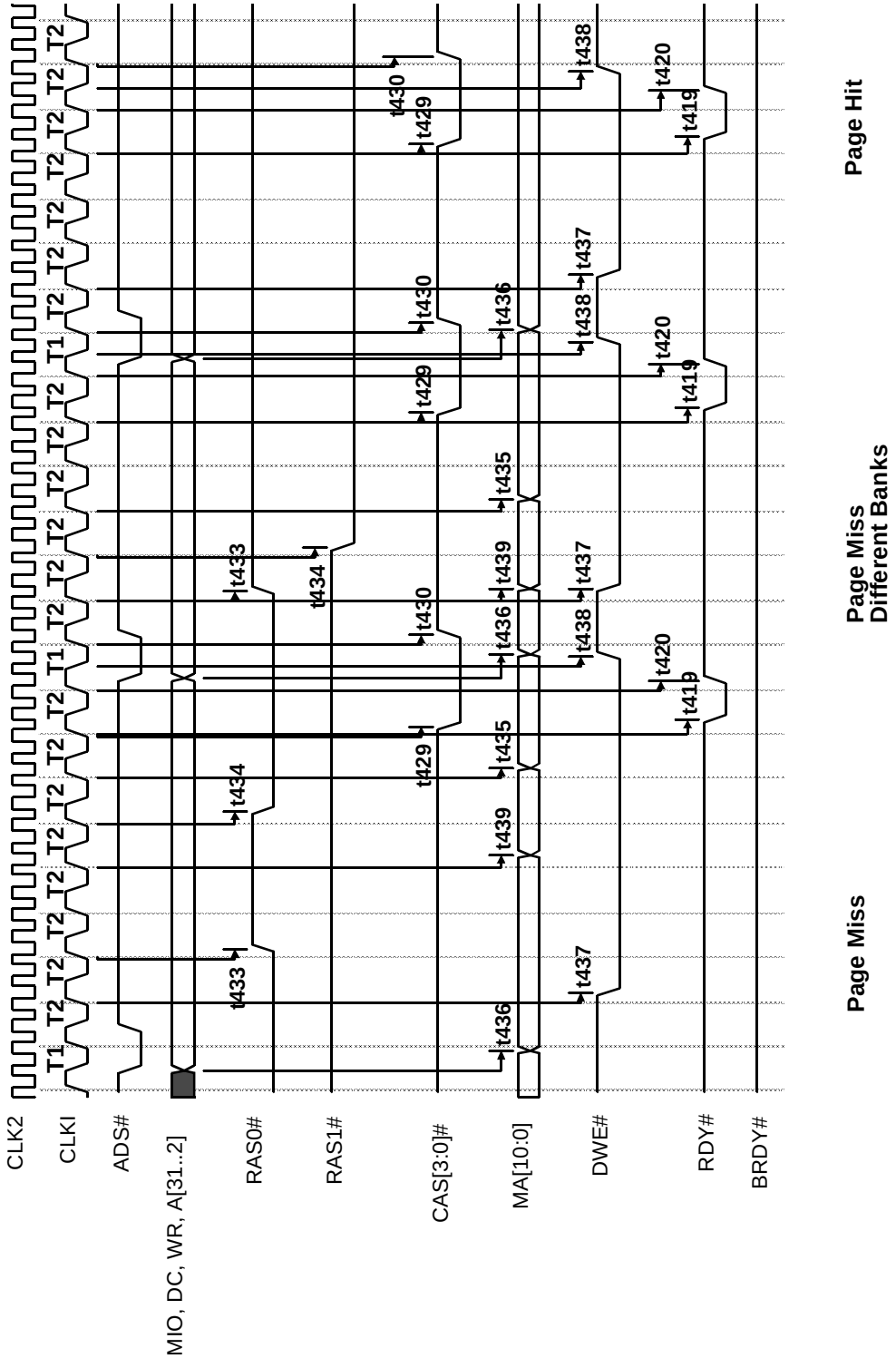


Figure 6-12 ISA Bus Cycles

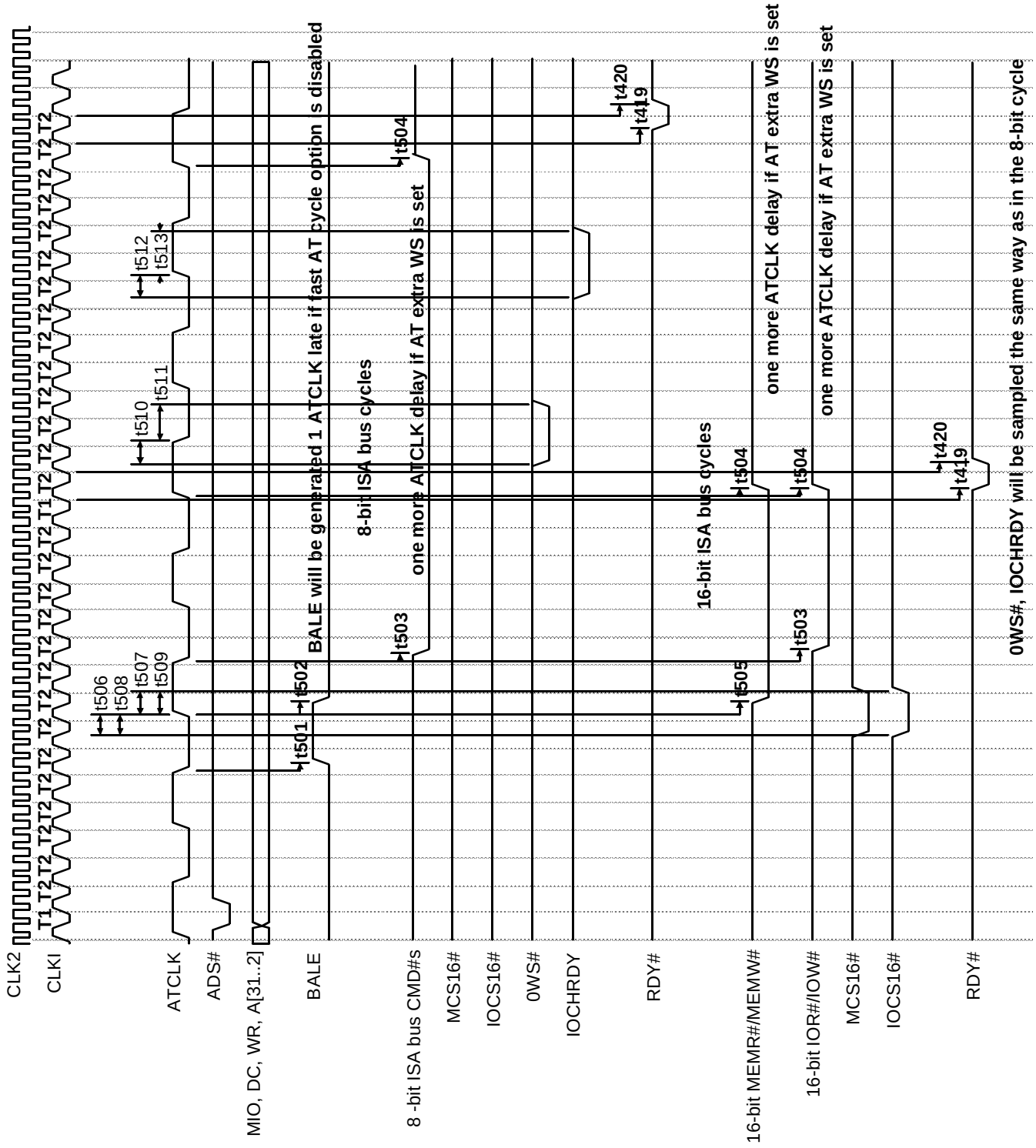


Figure 6-13 Keyboard Controller Access Cycles

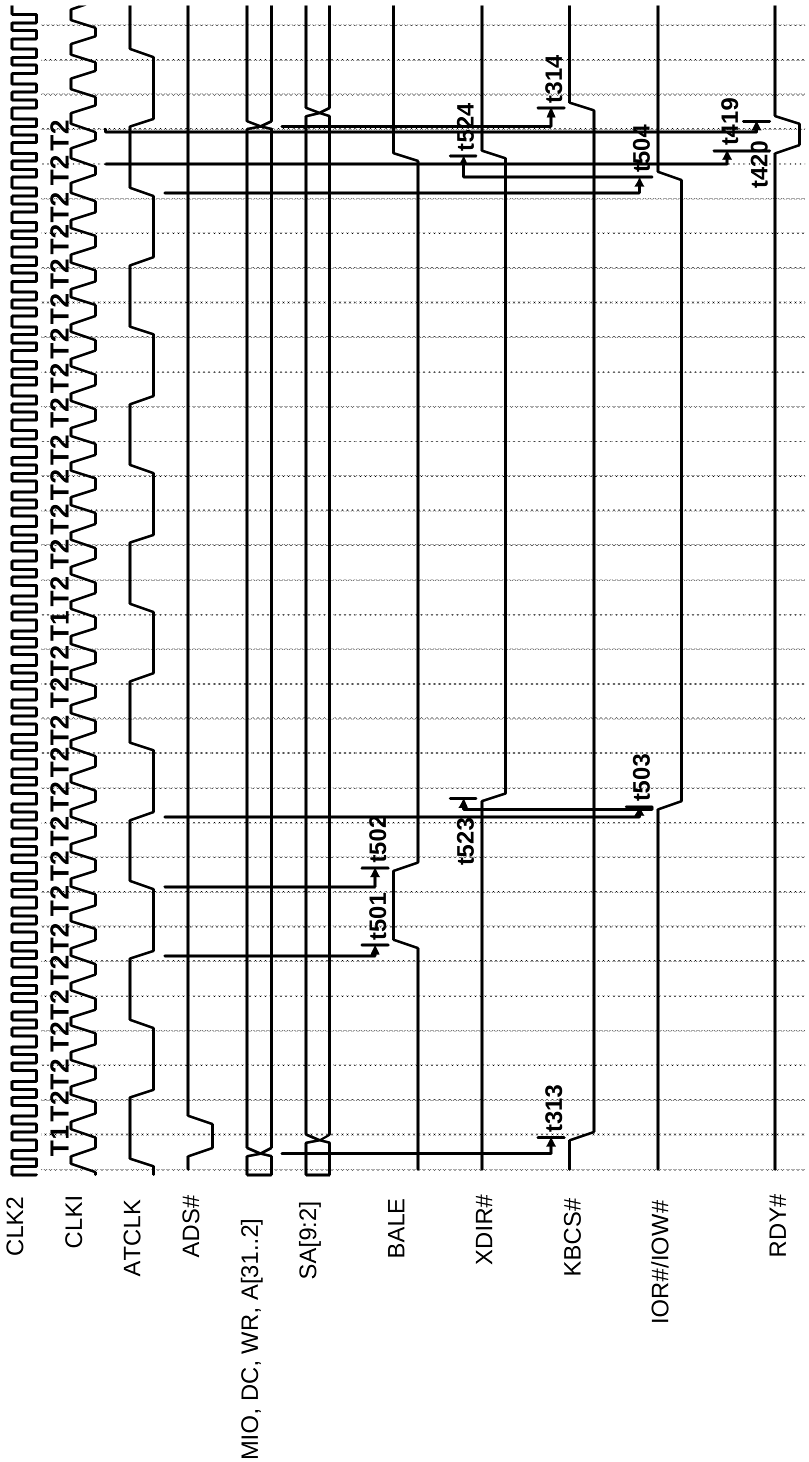


Figure 6-14 CPU Reset

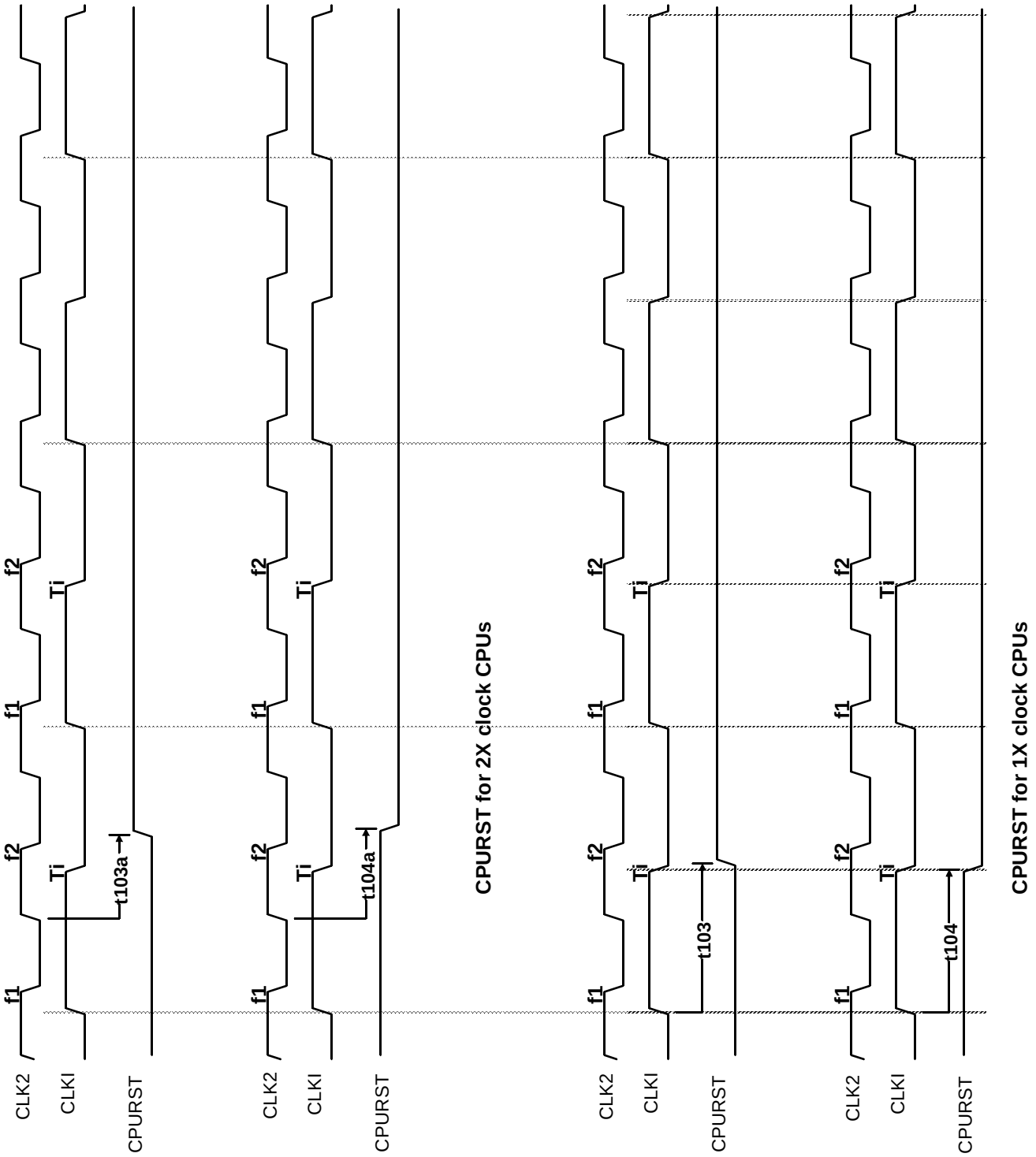


Figure 6-15 Refresh Cycle

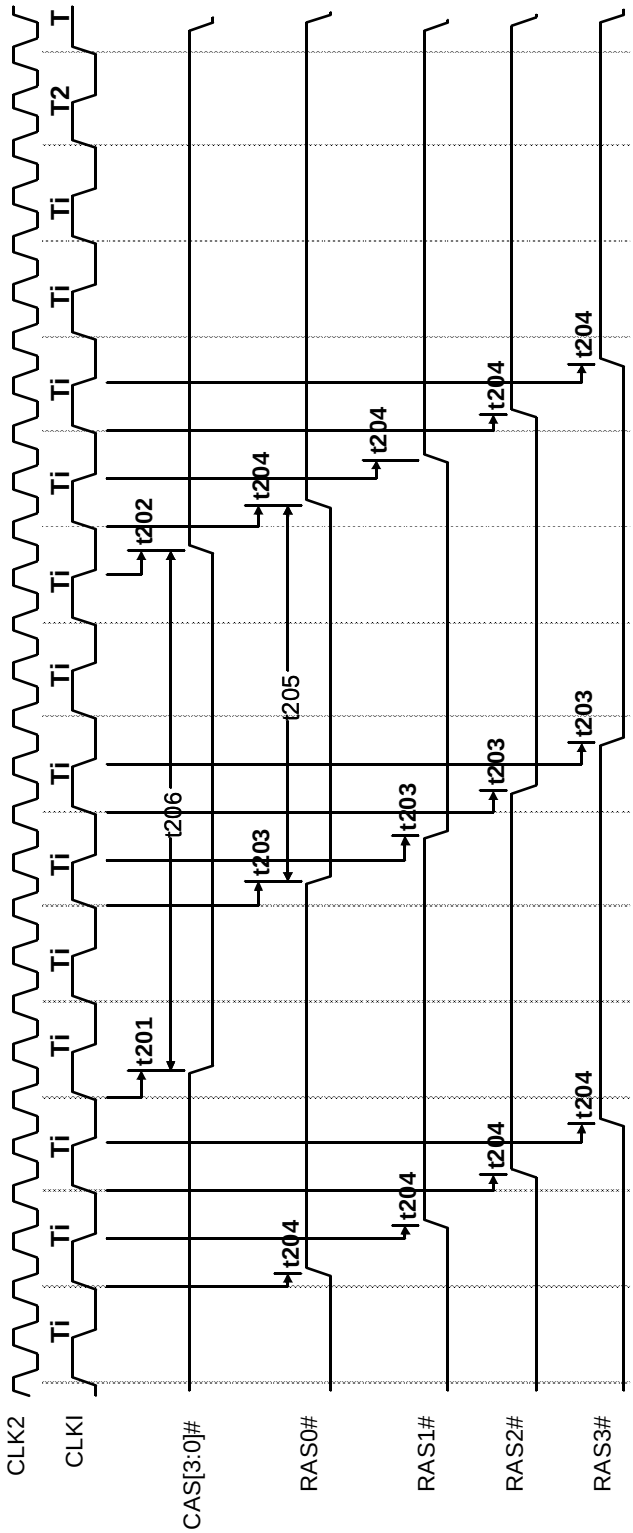


Figure 6-16 Cache Read Miss Dirty: 2 banks of cache and 0/0 DRAM wait state (1 of 2)

Figure 6-17 Cache Read Miss Dirty: 2 banks of cache and 0/0 DRAM wait state (2 of 2)

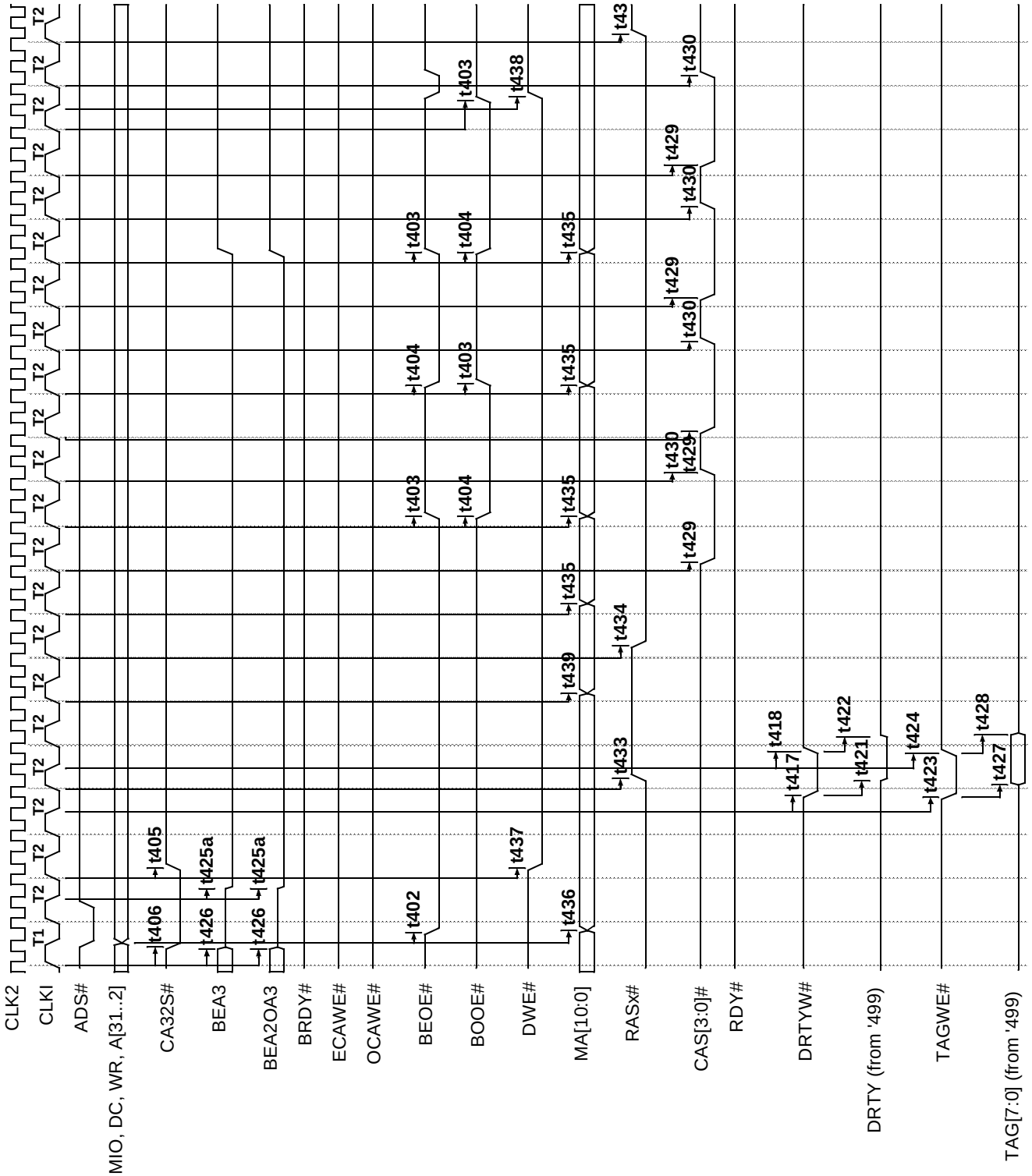


Figure 6-18 Cache Read Miss Dirty: 1 bank of cache and 0/0 DRAM wait state (1 of 2)

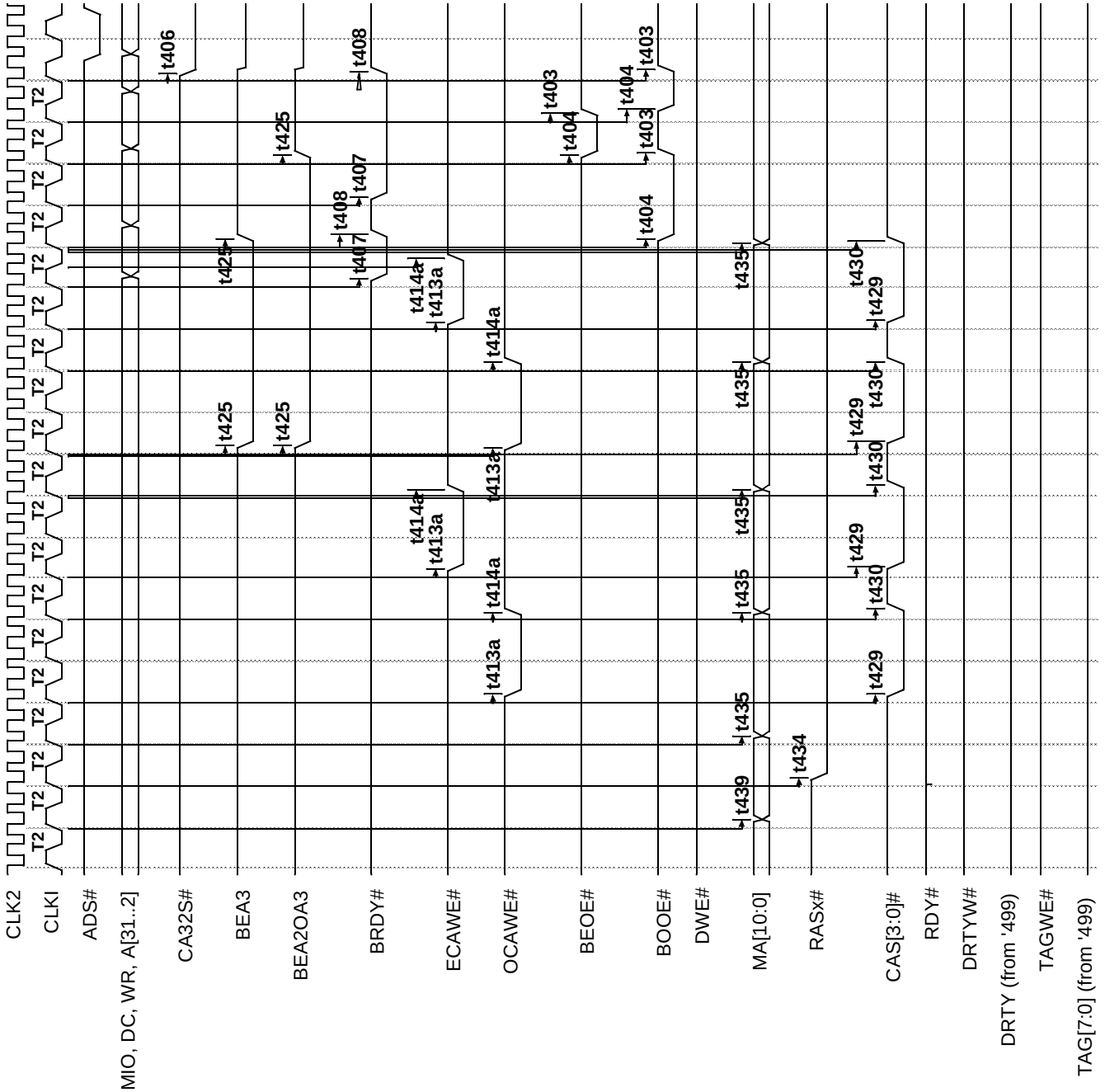


Figure 6-19 Cache Read Miss Dirty: 1 bank of cache and 0/0 DRAM wait state (2 of 2)

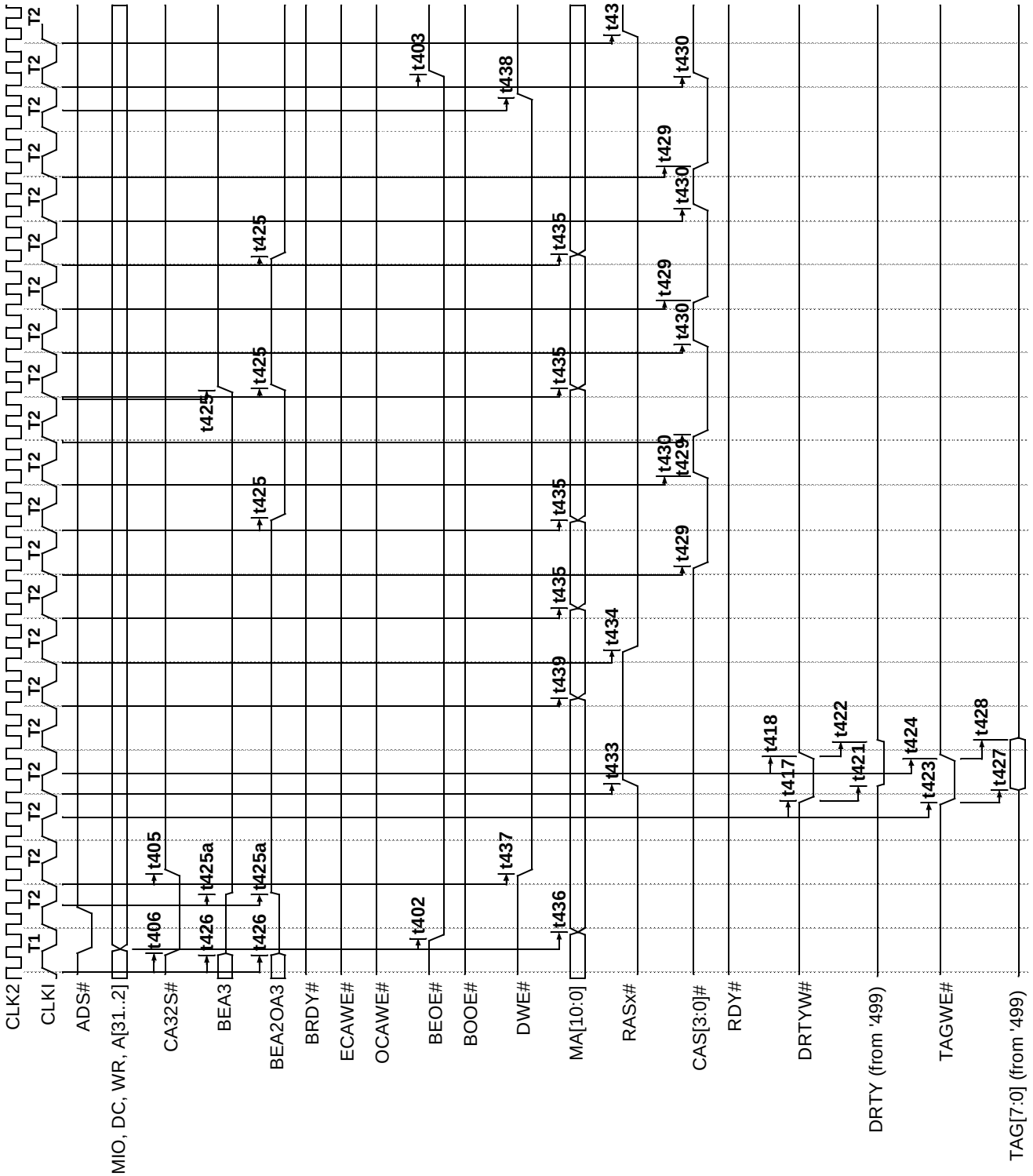


Figure 6-20 Cache Read Miss Dirty: 2 banks of cache and 1/1 DRAM wait state (1 of 2)

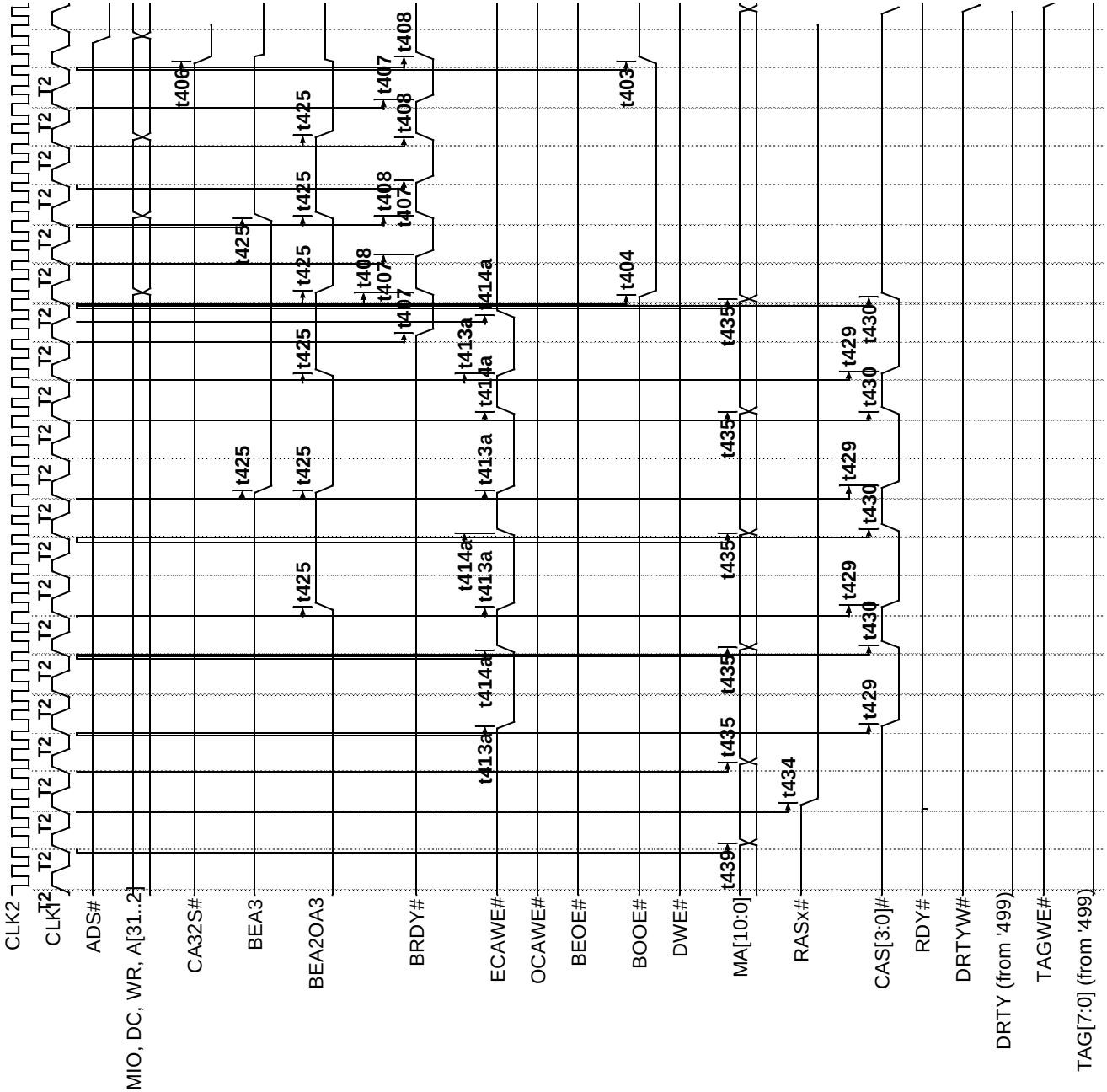


Figure 6-21 Cache Read Miss Dirty: 2 banks of cache and 1/1 DRAM wait state (2 of 2)

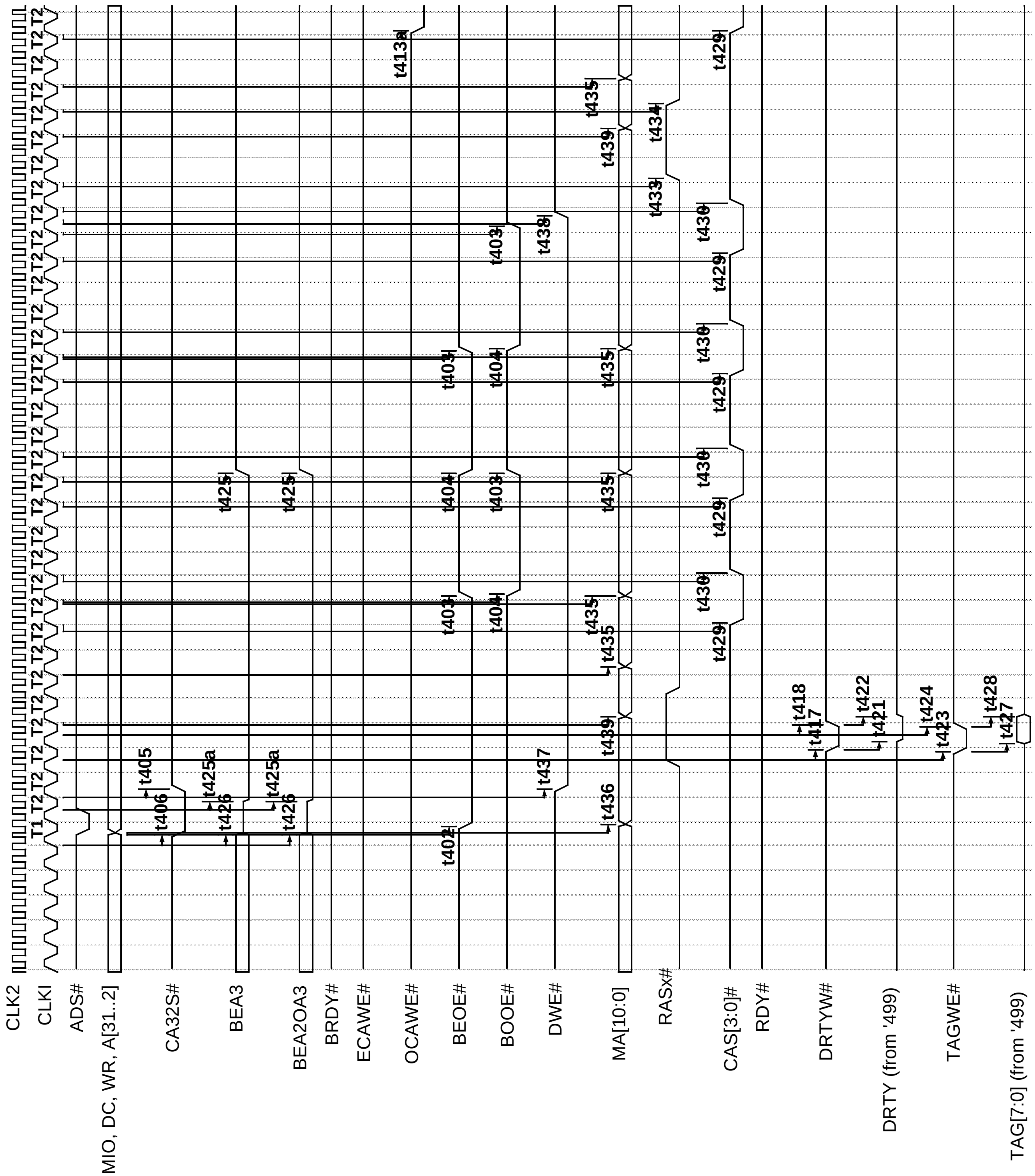


Figure 6-22 Cache Read Miss Dirty: 1 bank of cache and 1/1 DRAM wait state (1 of 2)

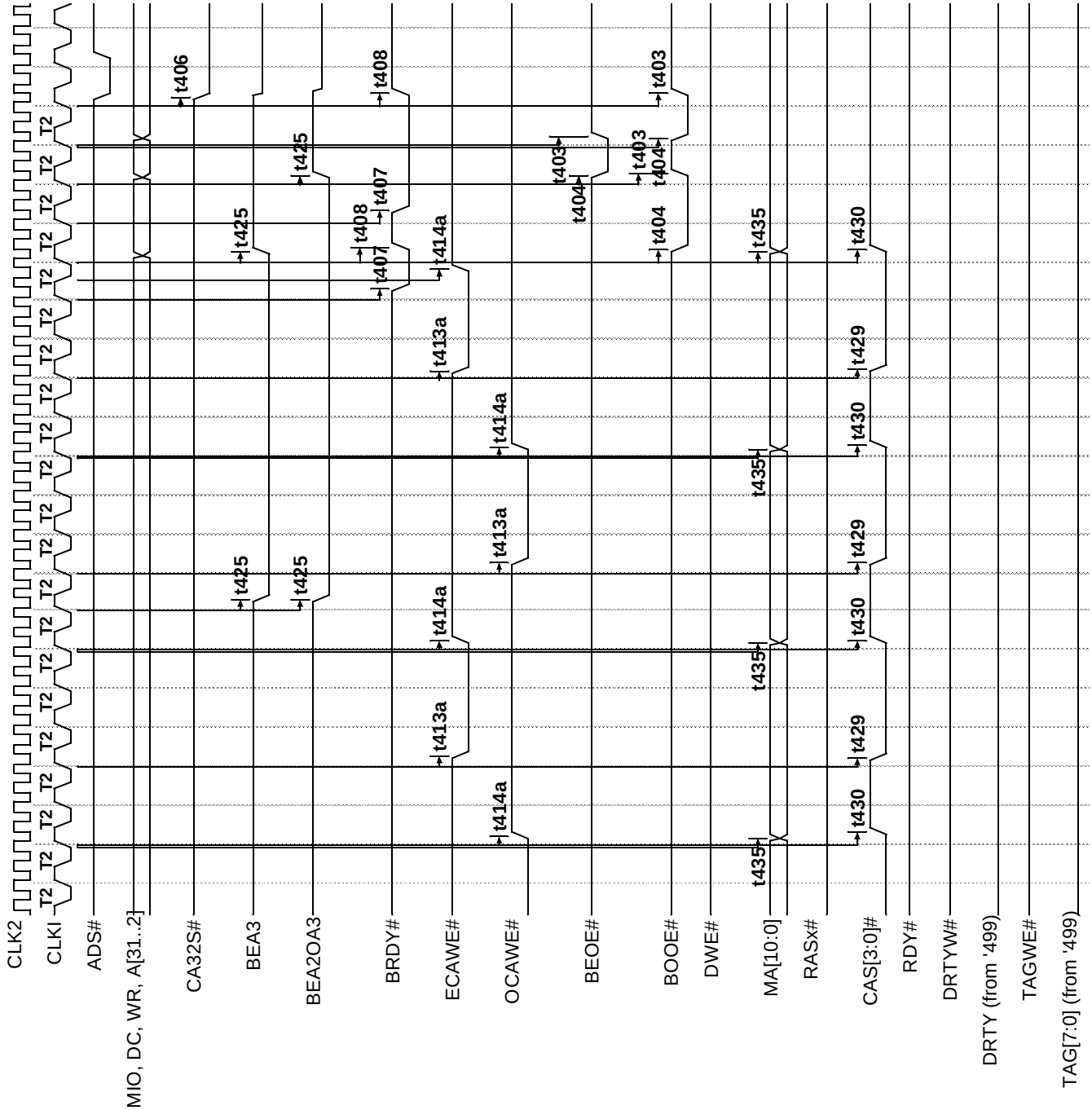


Figure 6-23 Cache Read Miss Dirty: 1 bank of cache and 1/1 DRAM wait state (2 of 2)

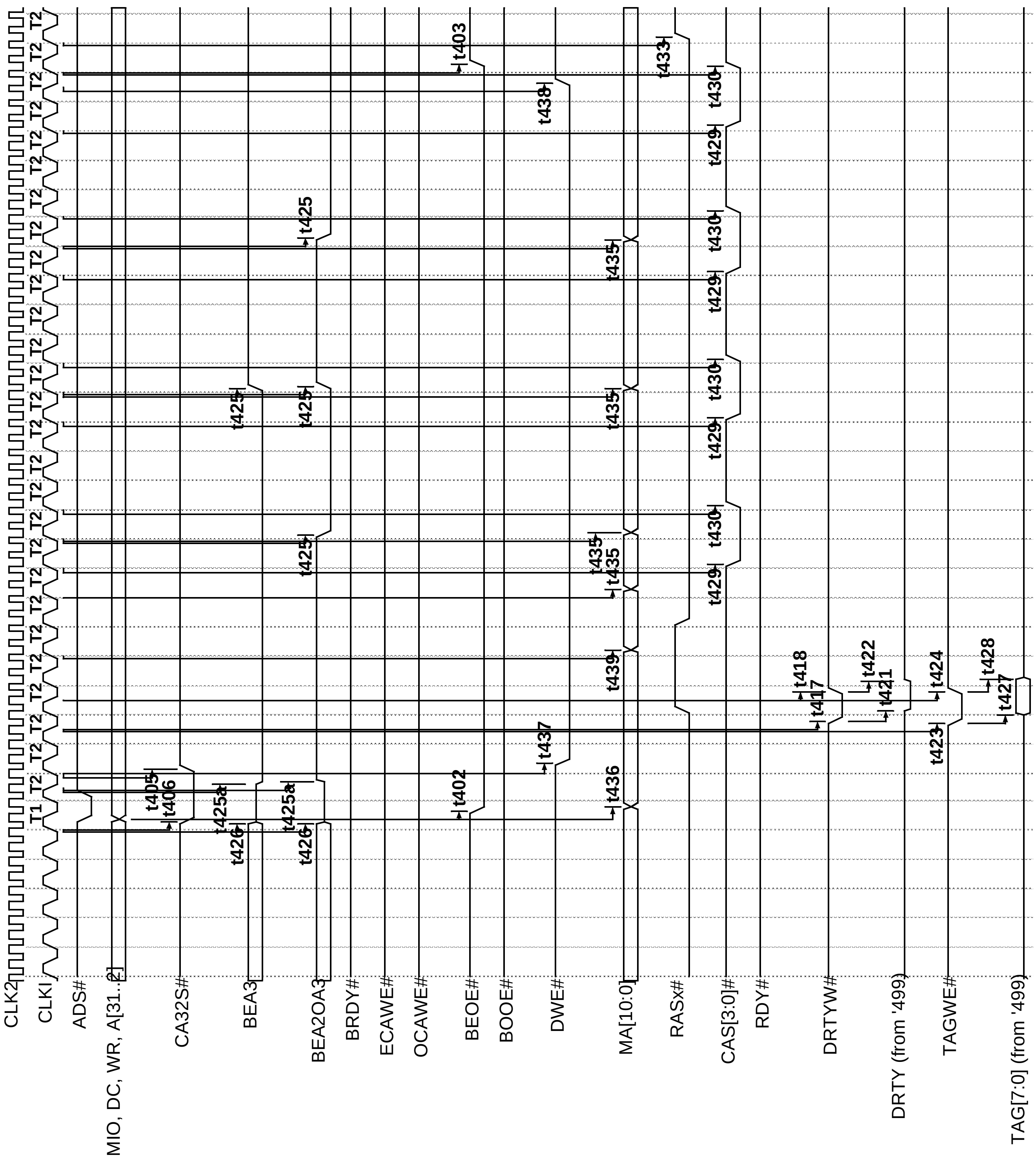


Figure 6-24 Cache Read Miss Not Dirty: 2 banks of cache and 0 DRAM read wait state

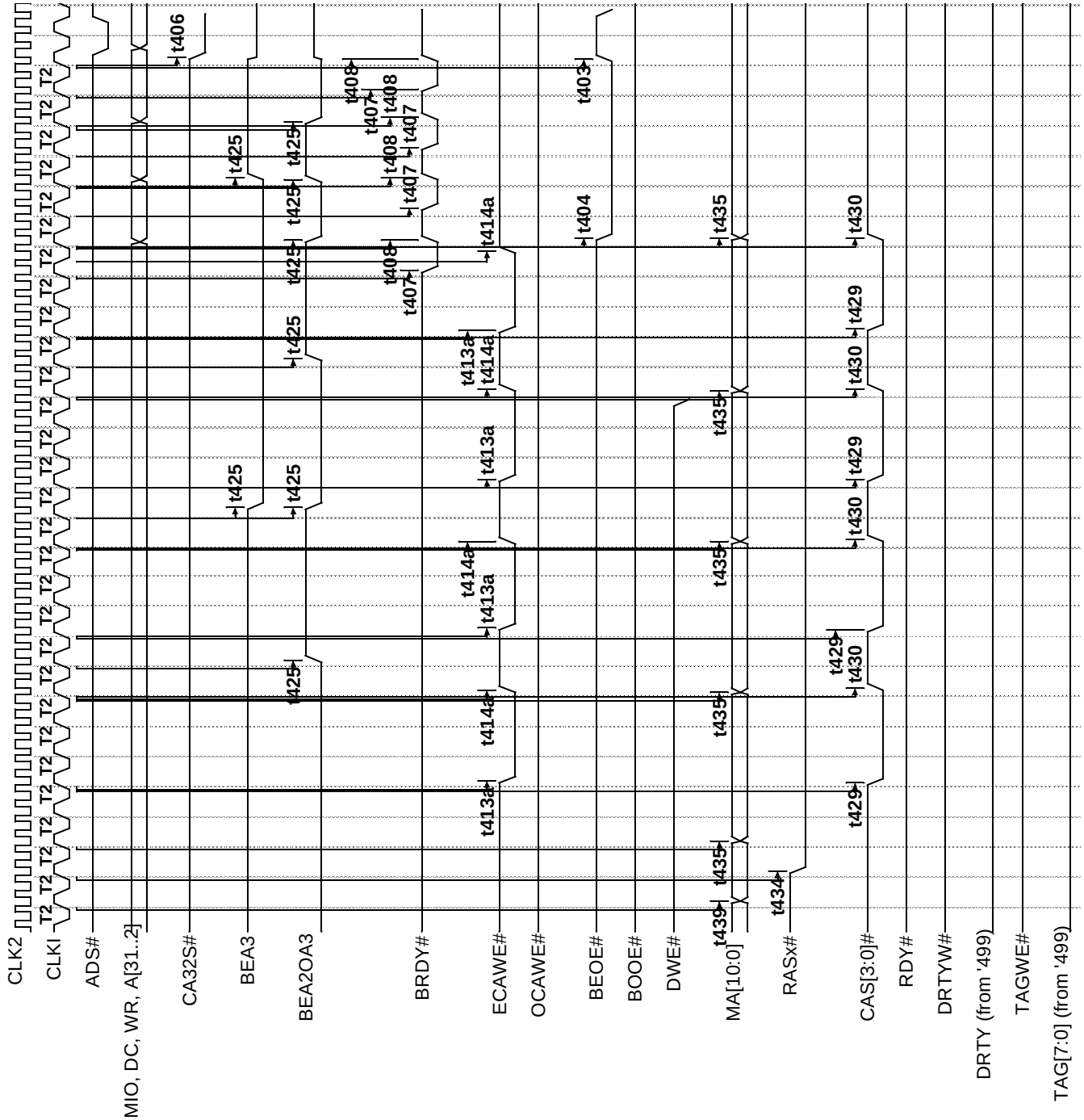


Figure 6-25 Cache Read Miss Not Dirty: 2 banks of cache and 1 DRAM read wait state

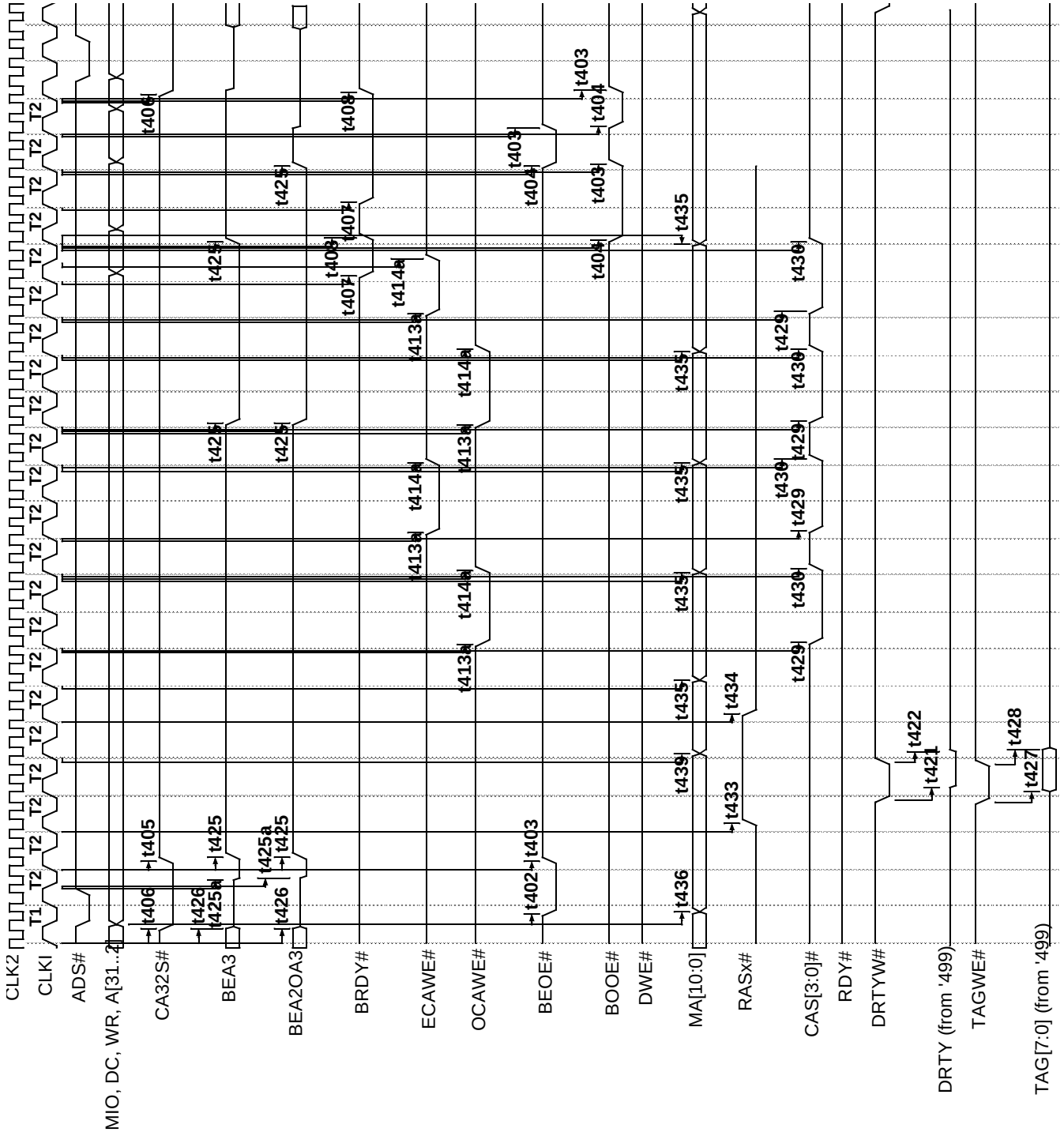


Figure 6-26 ROM Access Cycle (1 of 2)

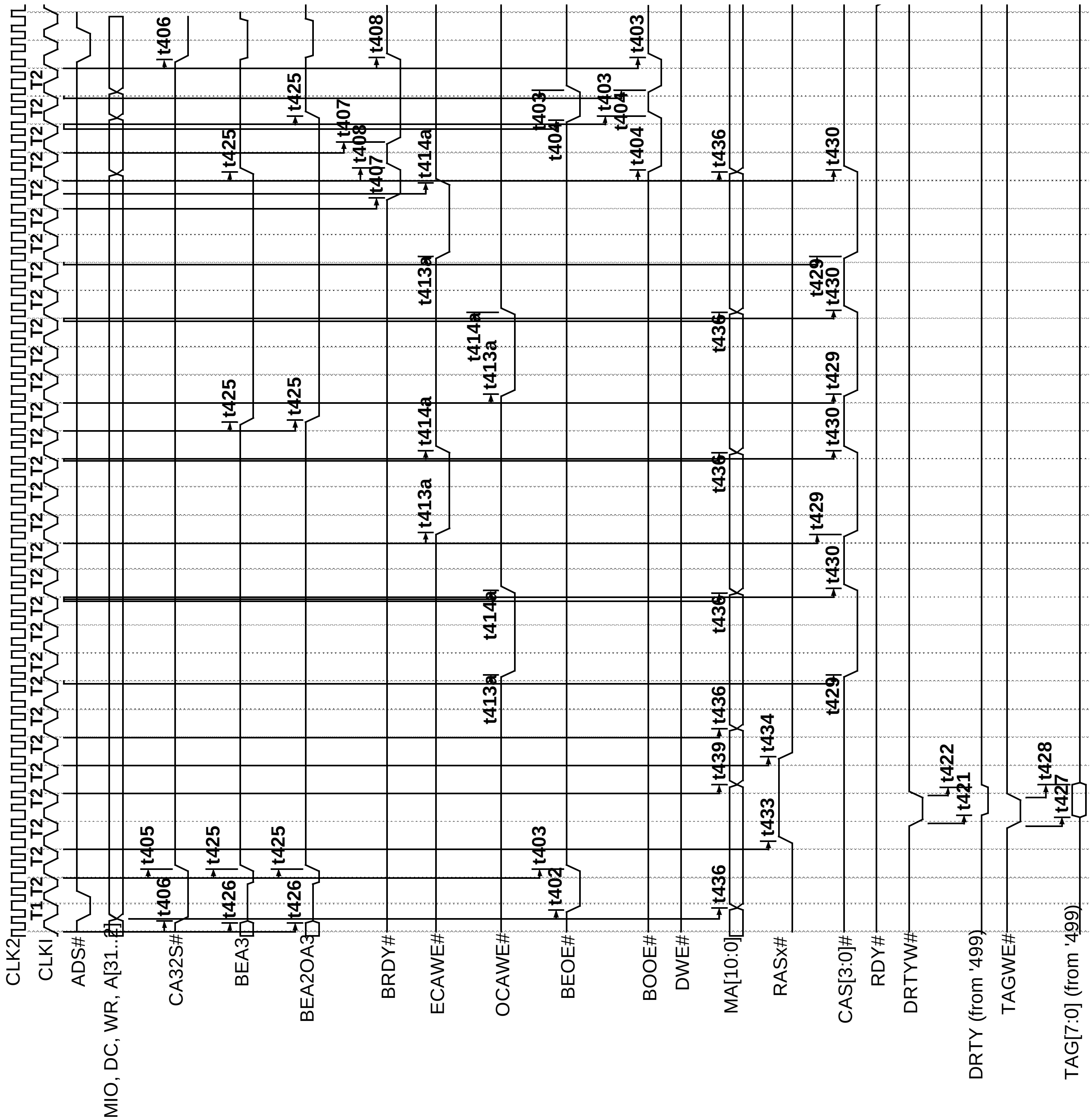


Figure 6-27 ROM Access Cycle (2 of 2)

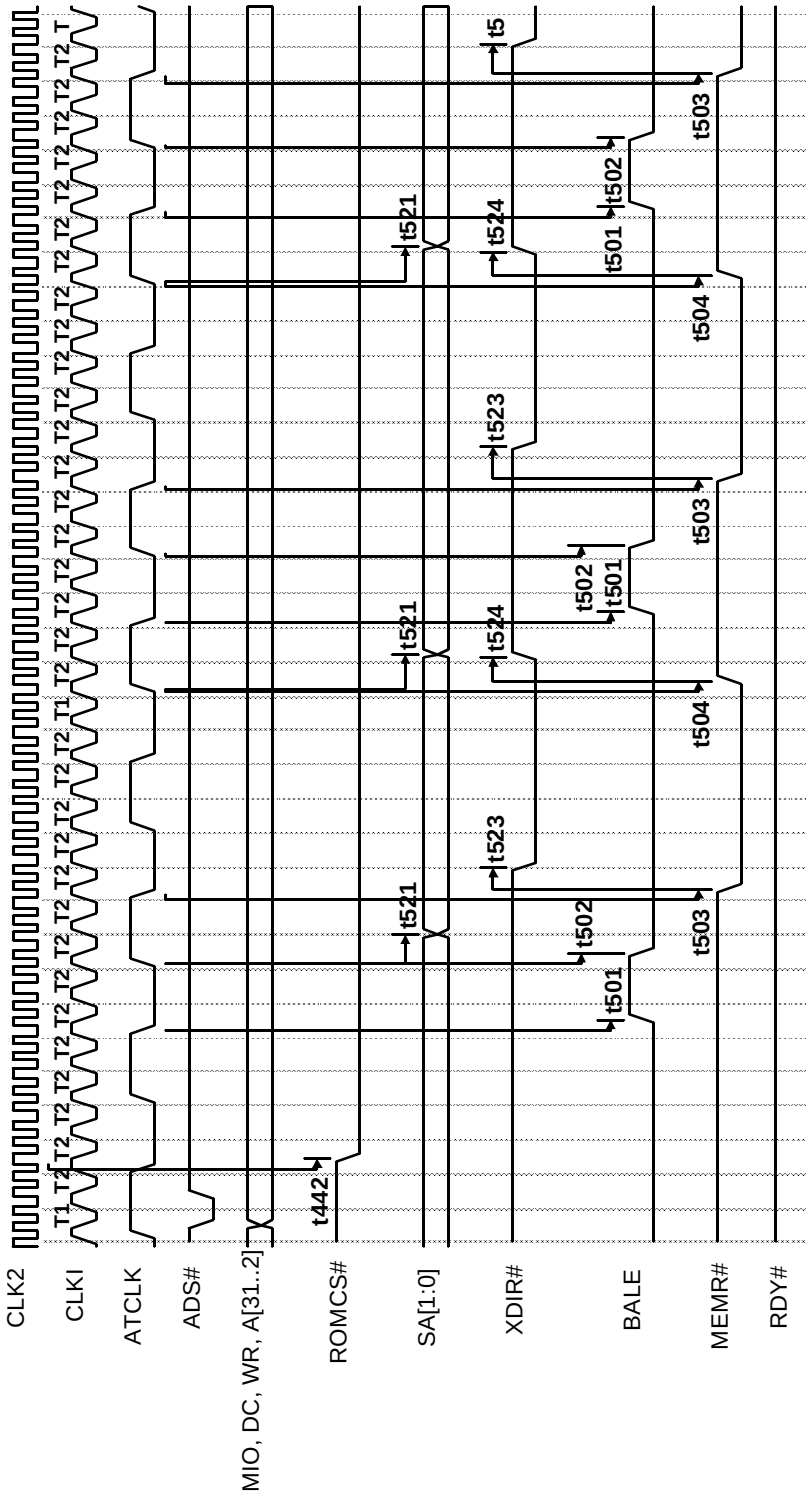


Figure 6-28 DMA Device Read from VESA Slave

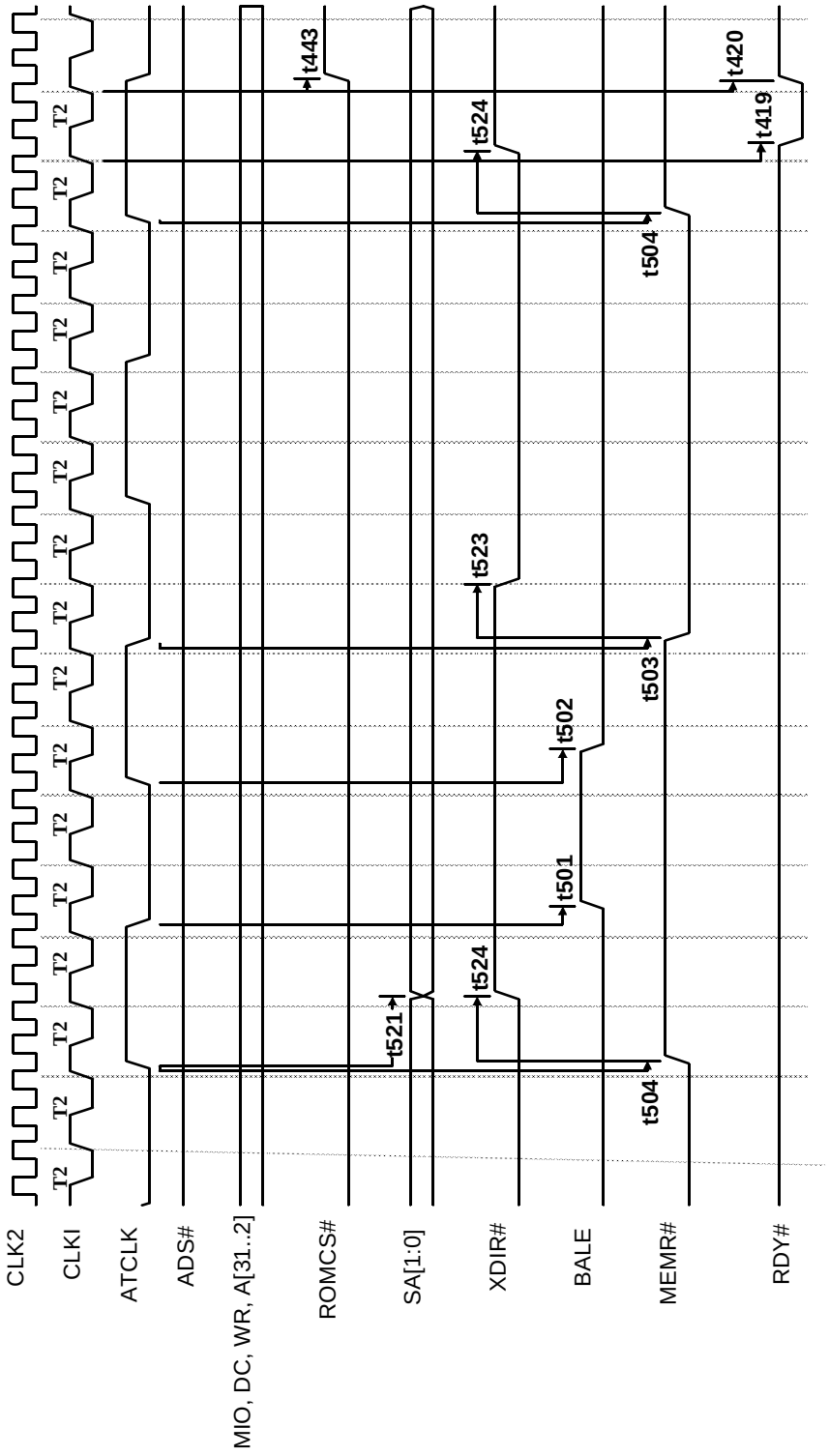


Figure 6-29 DMA Device Write to VESA Slave

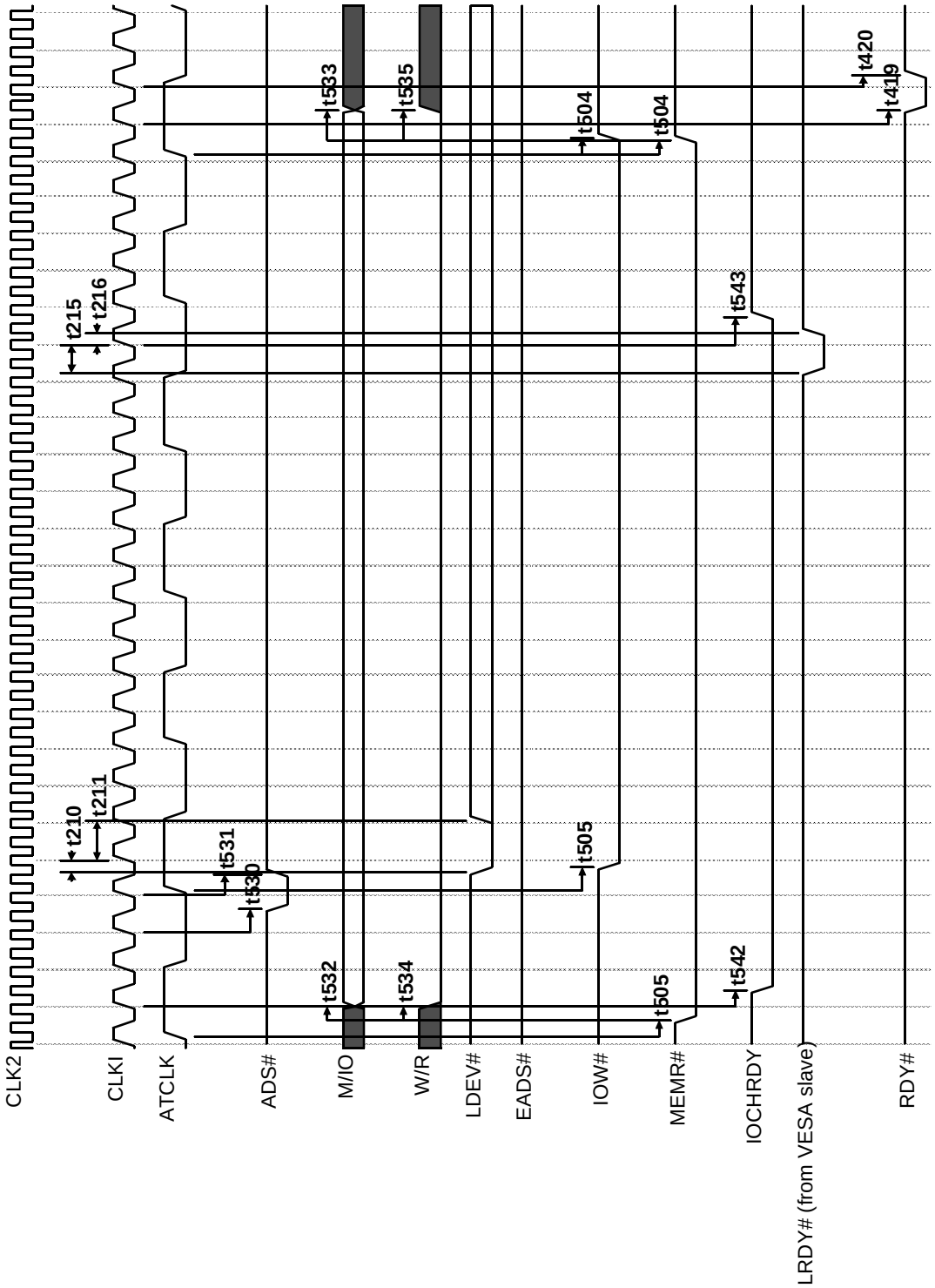


Figure 6-30 ISA Master Read from VESA Slave

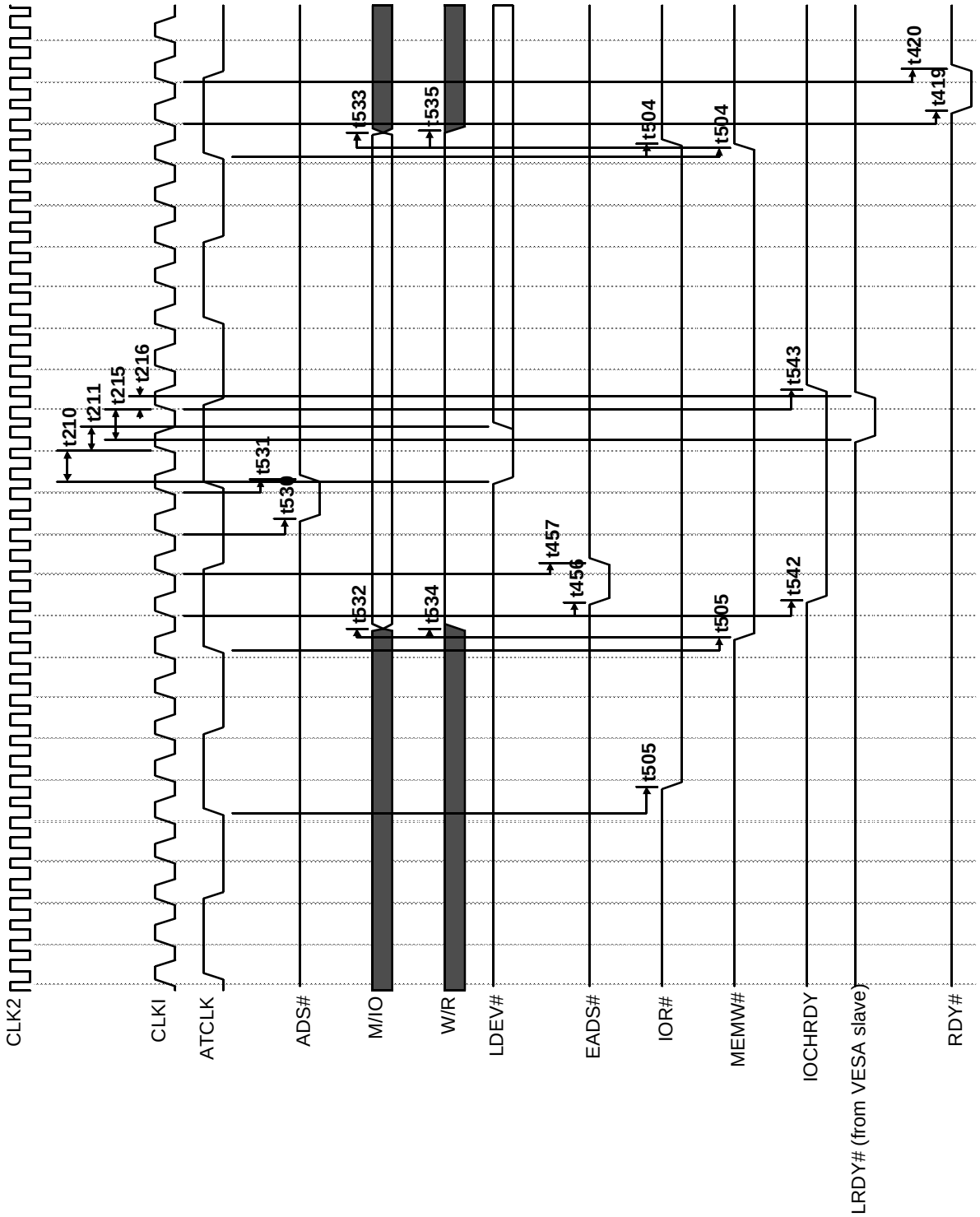
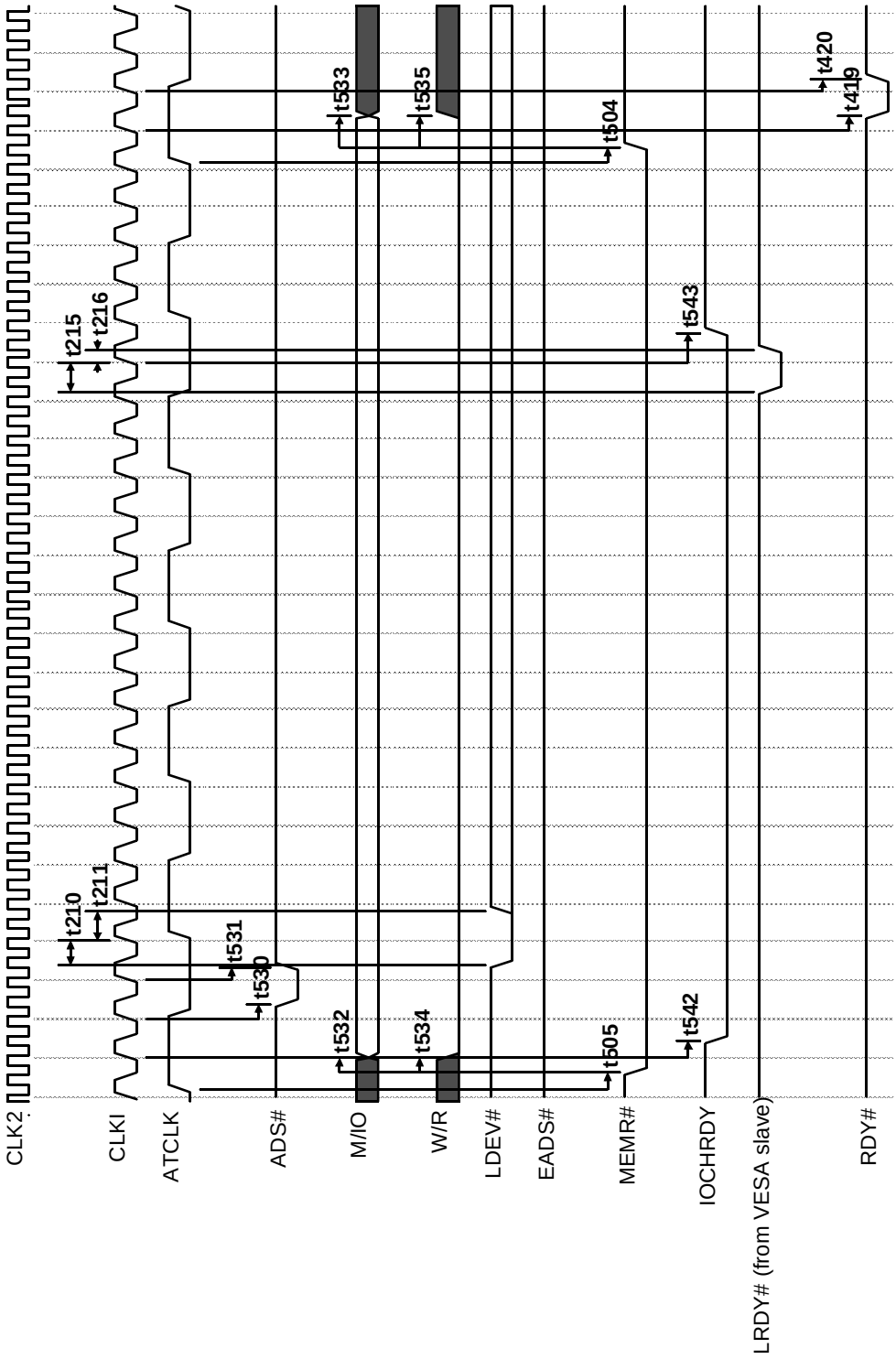
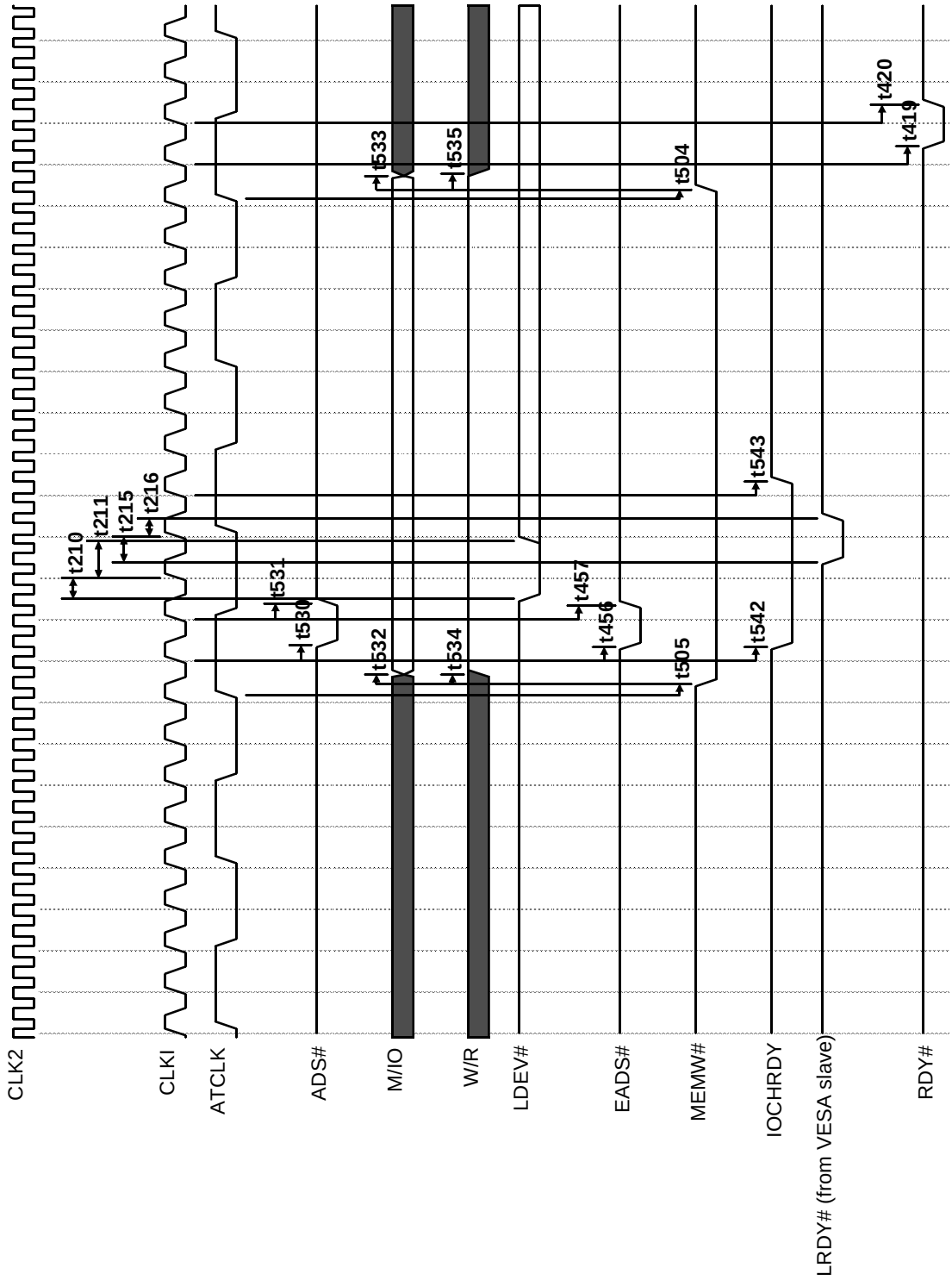
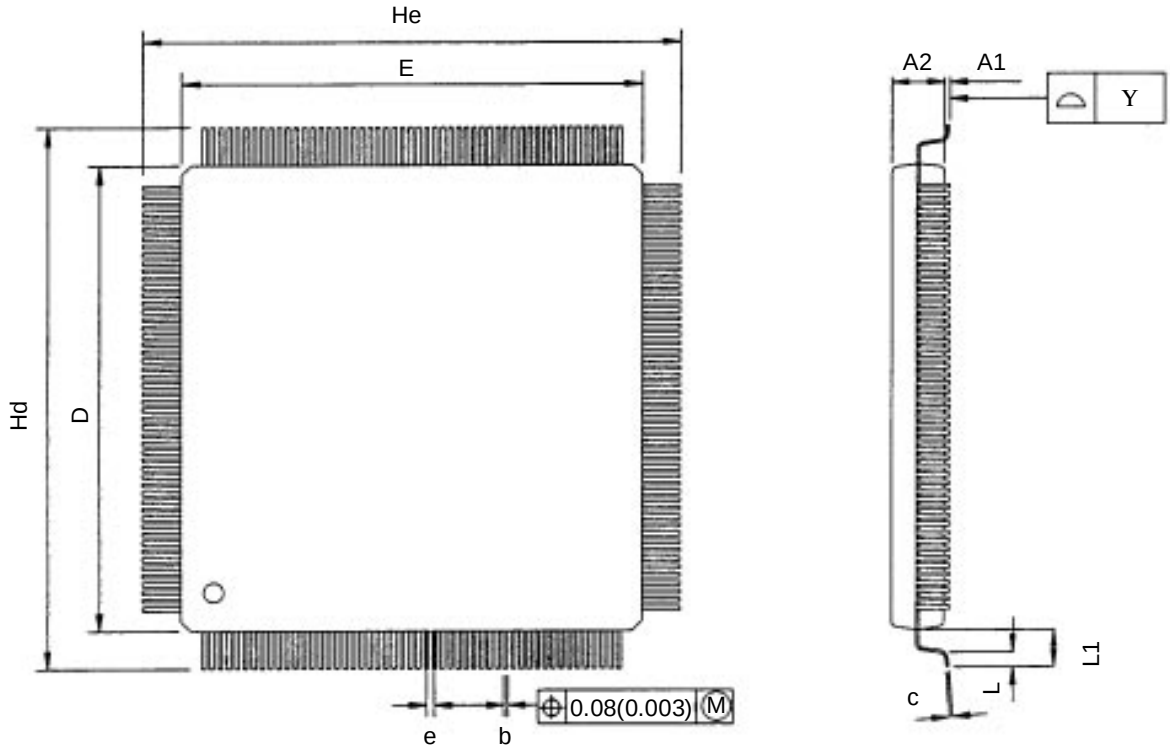


Figure 6-31 ISA Master Write to VESA Slave




CLK2
CLKI
ATCLK
ADS#
M/IO
W/R
LDEV#
EADS#
MEMW#
IOCHRDY
LRDY# (from VESA slave)
RDY#
t210
t211
t215
t216
t530
t531
t532
t533
t534
t535
t456
t457
t504
t505
t542
t543
t419
t420

7.0 Mechnical Package Outline



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.50			0.020	
Hd	30.35	30.60	30.85	1.195	1.205	1.215
He	30.35	30.60	30.85	1.195	1.205	1.215
L	0.35	0.50	0.65	0.014	0.020	0.026
L1		1.30			0.051	
Y			0.08			0.003
θ	0		10	0		10